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DATA SHEET
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Ideal Diode and High Side Switch NMOS Controller

NCV68261



WDFNW6
CASE 511DW

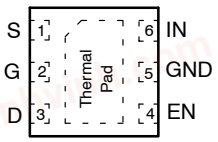
The NCV68261 is a Reverse Polarity Protection and Ideal Diode NMOS Controller with optional High Side Switch function, intended as a lower loss and lower forward voltage replacement for power rectifier diodes and mechanical power switches. The controller operates in conjunction with one or two N−channel MOSFETs and sets the ON/OFF state of the transistors based on the state of the Enable pin and the Input−to−Drain differential voltage polarity.

Depending on the Drain pin connection, both Ideal Diode and High Side Switch applications can operate in two different modes. With the Drain pin connected to the load, the applications are in Ideal Diode mode, whereas with the Drain pin connected to ground, the applications are merely in Reverse Polarity Protection mode.

Features

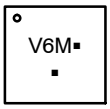
- Operating Voltage Range: up to 32 V
- Immune to 60 V Load Dump Pulse
- Immune to −40 V Negative Transient
- Overvoltage Protection
  - Disconnects the load from battery at V_{IN} = 35.6 V typ
- Enable Function (3.3 V Logic Compatible Thresholds)
- Ideal Diode Function
  - Protecting against Reverse Current Flow (from Output to Input)
- Reverse Polarity Protection (RPP) Function
  - Protecting against Negative Supply
- High Side Switch with Ideal Diode
- High Side Switch with Reverse Polarity Protection
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Grade 1 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

PIN ASSIGNMENT



WDFNW6
(Top View)

MARKING DIAGRAMS



V6 = Specific Device Code
M = Month Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

Typical Applications

- Automotive Battery Regulation
- Industrial Power Supply
- Rectifier
- High Side Switch
- Vehicle Control Module

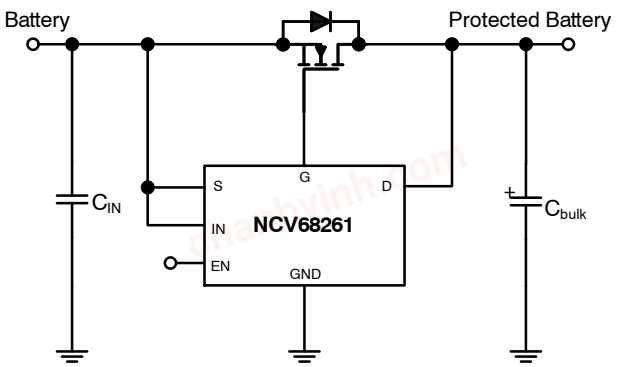


Figure 1. NCV68261 Application Schematic (Ideal Diode)

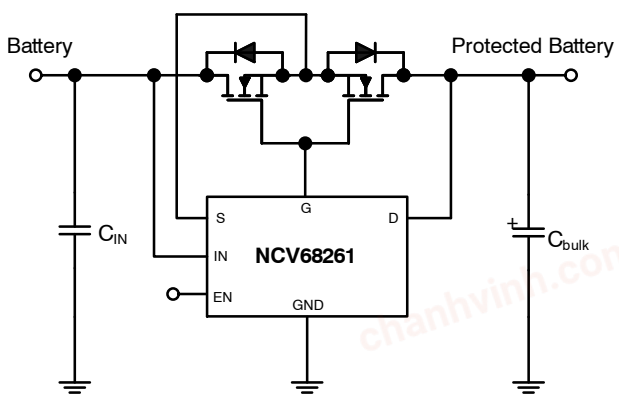


Figure 2. NCV68261 Application Schematic (Ideal Diode + High Side Switch)

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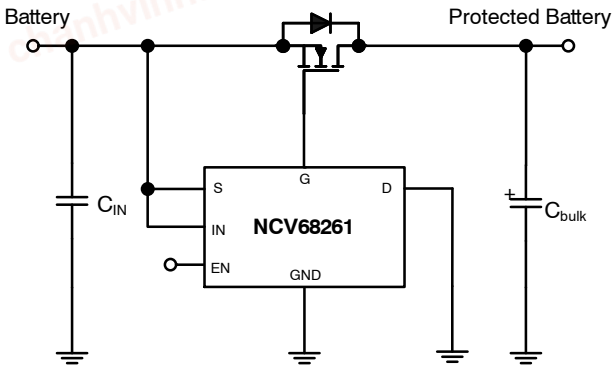


Figure 3. NCV68261 Application Schematic (Reverse Polarity Protection)

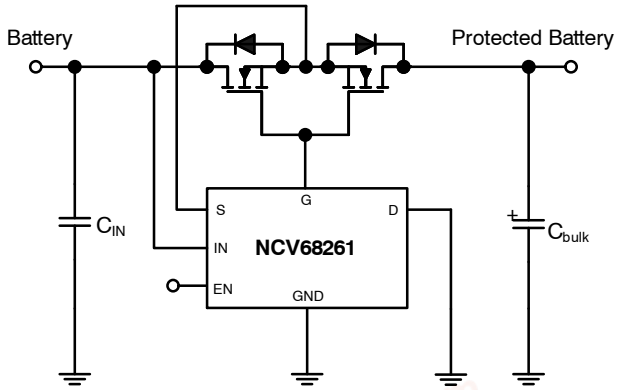


Figure 4. NCV68261 Application Schematic (Reverse Polarity Protection + High Side Switch)

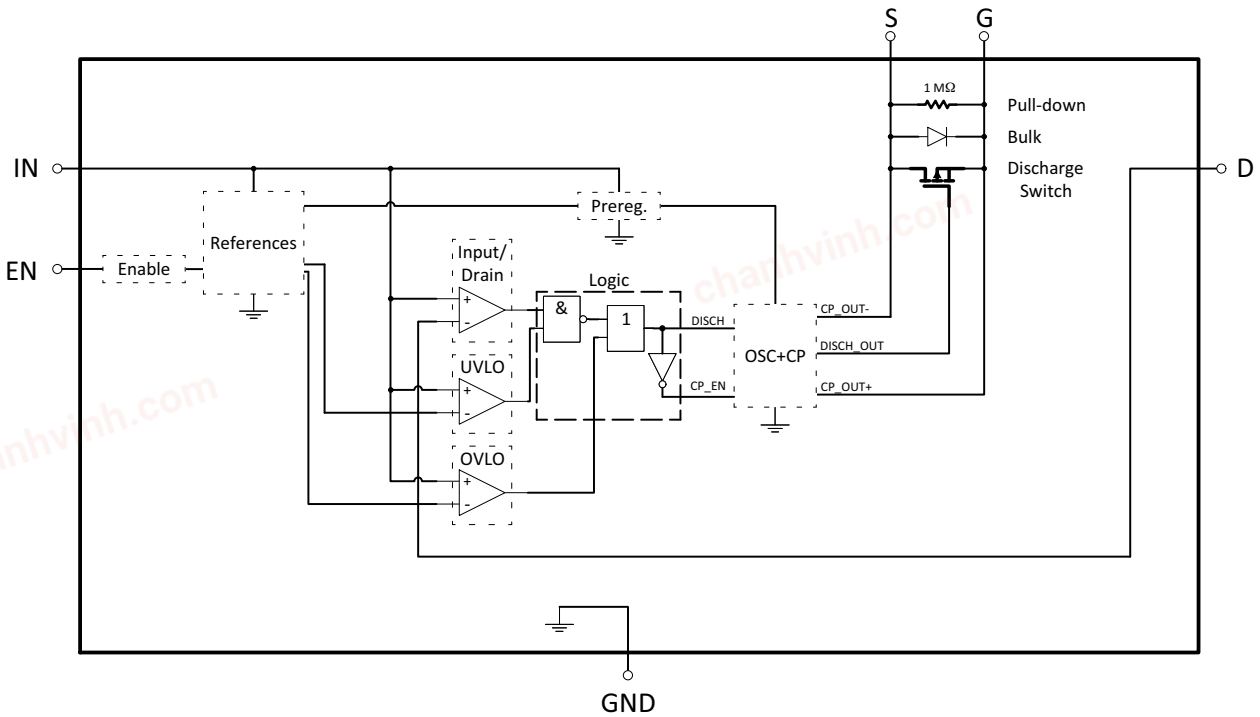


Figure 5. NCV68261 Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No. WDFNW6	Pin Name	Description
6	IN	Supply voltage input, Anode of the diode and Non−inverting input of the internal comparator. Bypass directly to GND with a ceramic capacitor. Connect to the Drain of the High Side Switch NMOS or to the Source pin (see the application schematics).
5	GND	Ground potential.
4	EN	Enable Input. High Level enables the chip. Connect to IN if enable function is not required.
3	D	Cathode of the diode and Inverting input of the internal comparator. Bypass directly to GND with a ceramic capacitor. Connect to the Drain of the Diode NMOS or to the GND (see the application schematics).
2	G	Charge pump output with discharge function. Connect to the Gate of the external NMOS (see application schematics).
1	S	Reference for the Charge pump output. Connect to the Source of the external NMOS (see application schematics).

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Table 2. MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Input and Source Voltage DC (Note 1)	V_S	−18	45	V
Input, Source, Drain, Gate and Enable Voltage (Note 2) Load Dump − Suppressed	U_{s*}	−	60	V
Input, Source, Gate and Enable Voltage (Note 3) Test Pulse 1	U_s	−40	−	V
Gate Voltage	V_G	−18	45	V
Gate−to−Source Voltage	V_{GS}	−0.3	19	V
Drain Voltage	V_D	−5	45	V
Input and Source−to−Drain Voltage DC	V_{SD}	−45	45	V
Input and Source−to−Drain Voltage transient (Test Pulse 1)	V_{SD}	−60	−	V
Enable Voltage	V_{EN}	−18	45	V
Operating Junction Temperature	T_J	−40	150	°C
Storage Temperature	T_{STG}	−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. Load Dump Test B (with centralized load dump suppression) according to ISO 16750−2 standard. Guaranteed by design. Not tested in production. Passed Class A according to ISO 16750−1.
3. Test Pulse 1 according to ISO 7637−2 standard. Guaranteed by design. Not tested in production. Passed Class A according to ISO 16750−1. More ISO 7637−2: 2011(E) PULSE TEST RESULTS are in Table 8.

Table 3. ESD CAPABILITY (Note 4)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESD_{HBM}	−2	2	kV
ESD Capability, Charged Device Model	ESD_{CDM}	−1	1	kV

4. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JS−001−2017)
   Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes smaller than 2×2 mm due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS−002−2018.

Table 4. LEAD SOLDERING TEMPERATURE AND MSL (Note 5)

Rating	Symbol	Min	Max	Unit
Moisture Sensitivity Level	MSL	1		−

5. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 5. THERMAL CHARACTERISTICS (Note 6)

Rating	Symbol	Value	Unit
Thermal Characteristics, WDFNW−6 Thermal Resistance, Junction−to−Ambient Thermal Reference, Junction−to−Case Top	 $R_{\theta JA}$ $\Psi_{\theta JT}$	 157.8 37.4	°C/W

6. Mounted onto a 80 x 80 x 1.6 mm single layer FR4 board (645 sq mm, 1 oz. Cu, steady state).

Table 6. RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Input Voltage	V_{IN}	3	32	V
Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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Table 7. ELECTRICAL CHARACTERISTICS
V_{IN} = 13.5 V, V_{EN} = 5 V, C_{IN} = 0.1 μF, C_{bulk} = 1 μF, Min and Max values are valid for temperature range −40°C ≤ T_J ≤ +150°C unless noted otherwise and are guaranteed by test, design or statistical correlation. Typical values are referenced to T_J = 25°C

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
CHARGE PUMP OPERATION						
Undervoltage Lockout	V_{IN} rising V_{IN} falling (Gate Discharge)	V_{IN_UVLO}	– 3	3.4 3.25	3.65 –	V
Overvoltage Lockout	V_{IN} rising Hysteresis (V_{IN} falling)	V_{IN_OVLO}	32 –	35.6 0.8	42 –	V
Gate−to−Source Charged Voltage	V_{IN} = 4 V V_{IN} ≥ 8 V	V_{GS}	3 9	4 11.3	– 15	V
Input−to−Drain Voltage Threshold Gate Charge Gate Discharge	 V_{IN-D} rising V_{IN-D} falling	$V_{th(IN-D)}$	 100 −40	 140 −10	 220 0	mV
Gate Charge Current	V_{GS} = 0 V, V_{IN-D} = 220 mV V_{IN} = 4 V V_{IN} = 13.5 V	I_{G_Charge}	 70 170	 100 320	 – –	μA
Gate Discharge Peak Current	V_{GS} = 10 V, V_{IN-D} ≤ −100 mV	I_{G_Disch}	–	1.65	–	A
Discharge Switch $R_{DS(ON)}$	V_{GS} = 100 mV, V_{IN-D} ≤ −100 mV	$R_{DS(on)}$	1	2.4	5	Ω
Response Time (Time from Reverse Voltage Condition to V_{GS} = 9 V)	V_{GS} = 10 V, V_{IN} = 13.5 V, V_{IN-D} = step from 250 mV to −150 mV	t_{rt_OFF}	–	0.2	0.6	μs
Gate−to−Source Static Resistance			–	1.1	–	MΩ
DISABLE AND QUIESCENT CURRENTS						
Disable Current	V_{EN} = 0 V	I_{DIS}	–	–	5	μA
Quiescent Current	I_{GS} = 0 mA, V_{IN-D} = 220 mV (CP active)	I_q	–	210	295	μA
ENABLE						
Enable Input Threshold Voltage Logic Low Logic High	 V_{GS} ≤ 0.1 V V_{GS} ≥ 4.9 V	$V_{th(EN)}$	 0.99 –	 1.7 1.8	 – 2.31	V
Enable Input Current Logic High Logic High Logic Low	 V_{EN} = 13.5 V V_{EN} = 5 V V_{EN} = 0 V	 I_{EN_ON} I_{EN_ON} I_{EN_OFF}	 – – –	 11 3.2 0.010	 – 5 1	μA
Response Time (Time from EN High−to−Low to V_{GS} = 9 V)	V_{GS} = 10 V, V_{IN} = 13.5 V, V_{EN} = step from 5 V to 0 V	$t_{rt_EN_OFF}$	–	0.9	4	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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TYPICAL CHARACTERISTICS

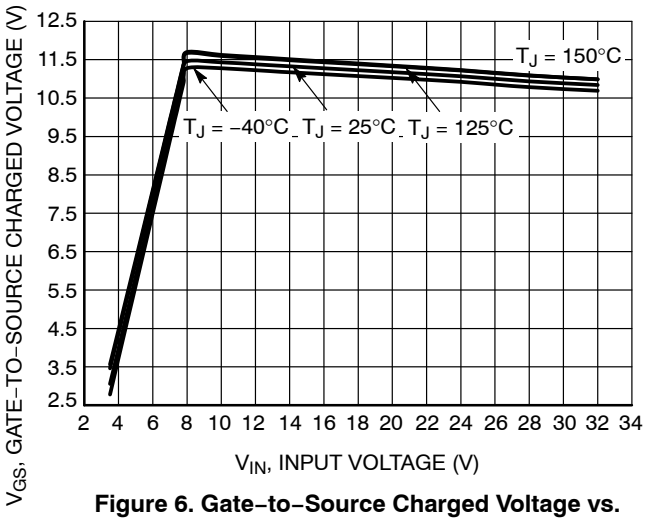


Figure 6. Gate−to−Source Charged Voltage vs. Input Voltage

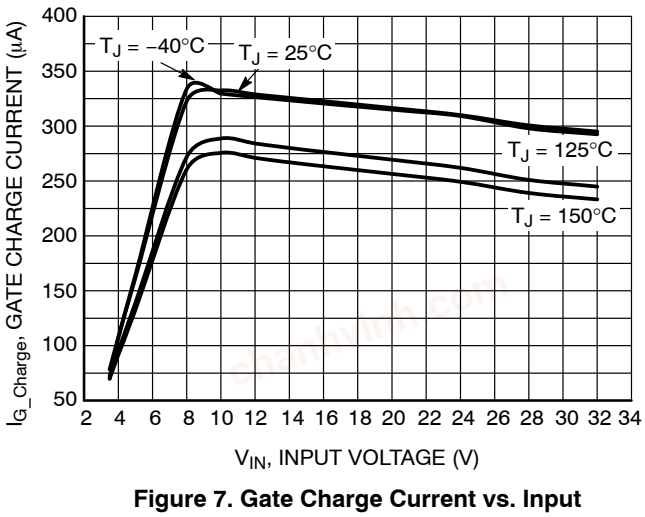


Figure 7. Gate Charge Current vs. Input Voltage

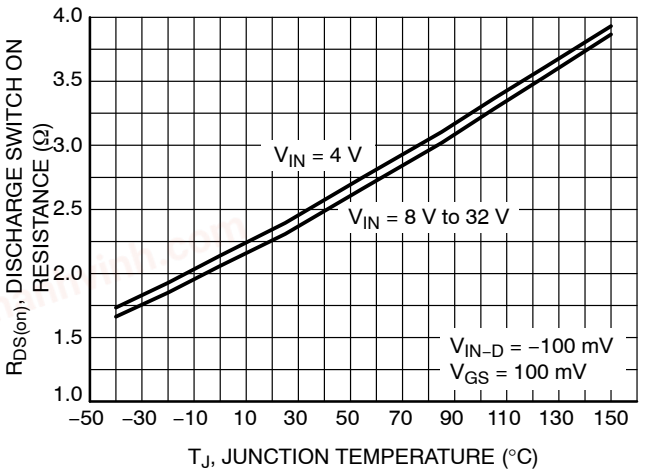


Figure 8. Discharge Switch On Resistance vs. Temperature

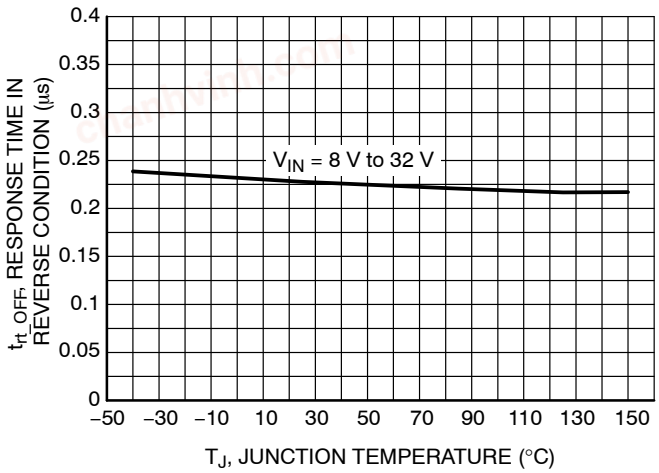


Figure 9. Charge Pump Output Response Time in Reverse Condition (from $V_{IN−D}$ = 0 V to V_{GS} = 9 V) vs. Temperature

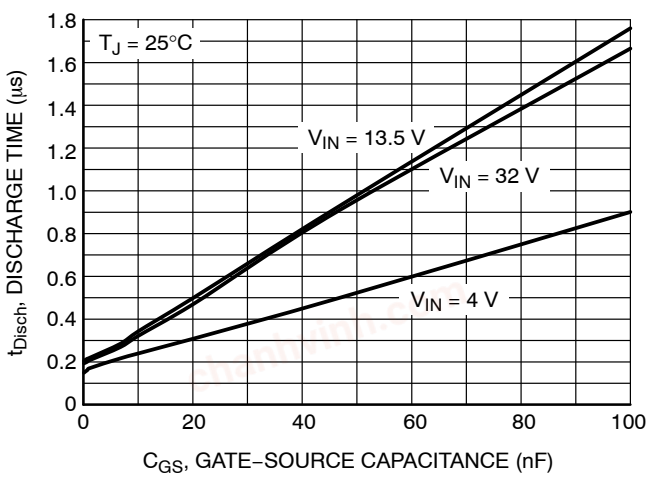


Figure 10. Discharge Time (from $V_{IN−D}$ = 0 V to V_{GS} = 0 V) vs. Gate−Source Capacitance

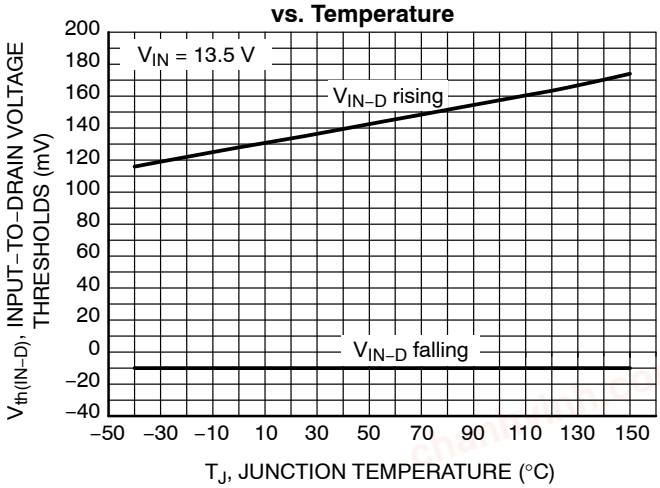


Figure 11. Input−to−Drain Voltage Thresholds vs. Temperature

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TYPICAL CHARACTERISTICS

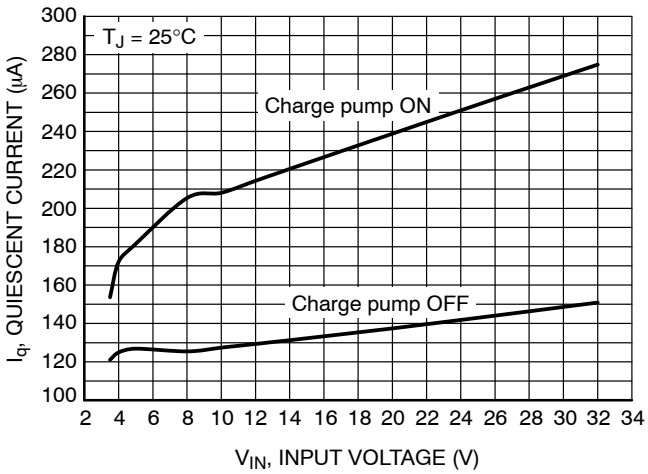


Figure 12. Quiescent Current vs. Input Voltage

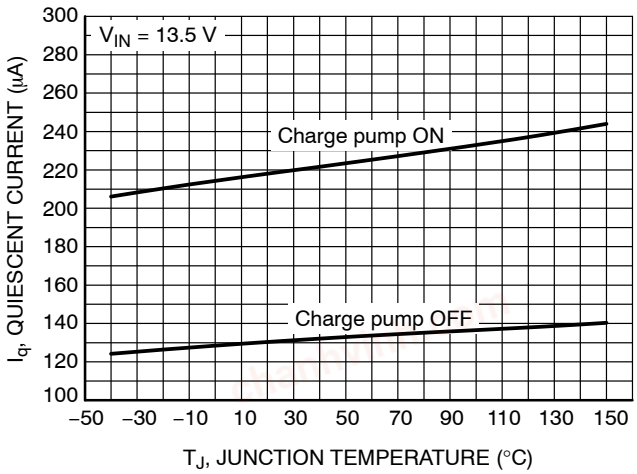


Figure 13. Quiescent Current vs. Temperature

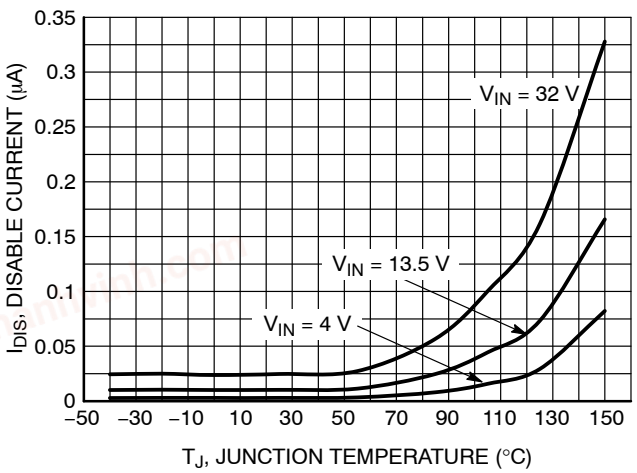


Figure 14. Disable Current vs. Temperature

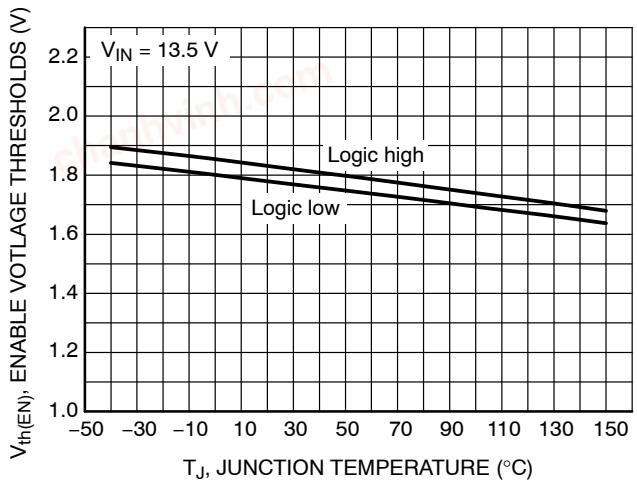


Figure 15. Enable Voltage Thresholds vs. Temperature

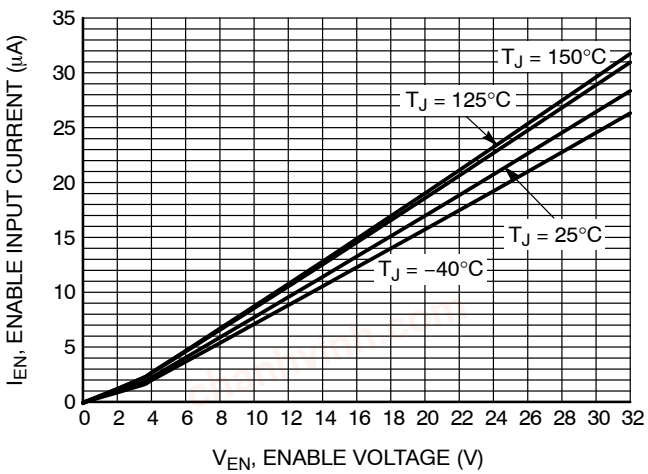


Figure 16. Enable Input Current vs. Enable Voltage

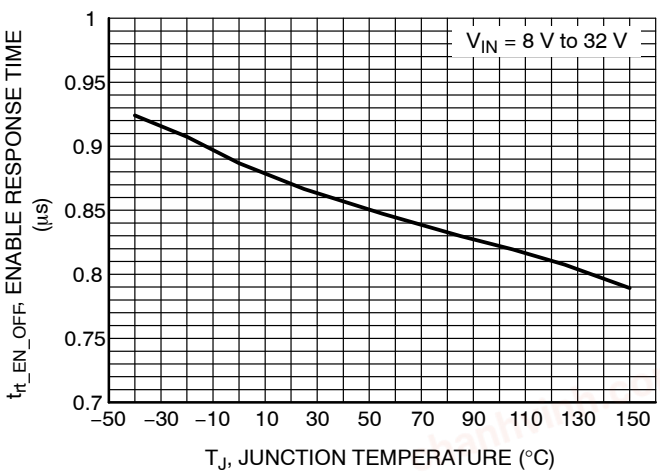


Figure 17. Enable Response Time (from EN High−to−Low to V_{GS} = 9 V) vs. Temperature

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TYPICAL CHARACTERISTICS

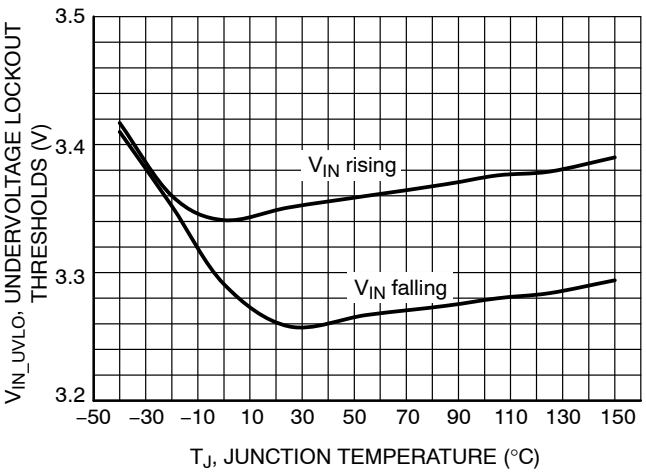


Figure 18. Undervoltage Lockout (UVLO) Thresholds vs. Temperature

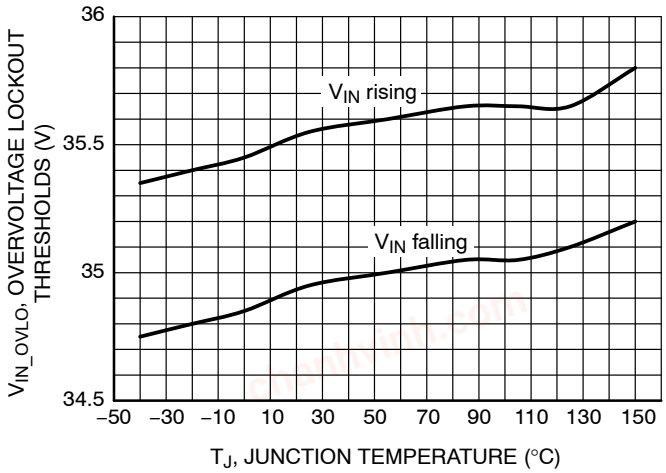


Figure 19. Overvoltage Lockout (OVLO) Thresholds vs. Temperature

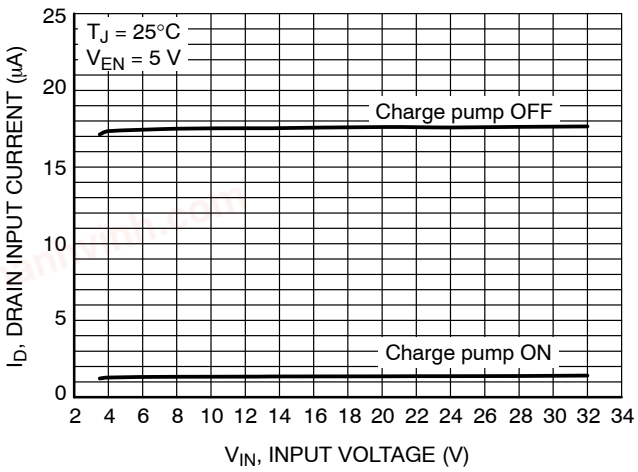


Figure 20. Drain Input Current vs. Input Voltage

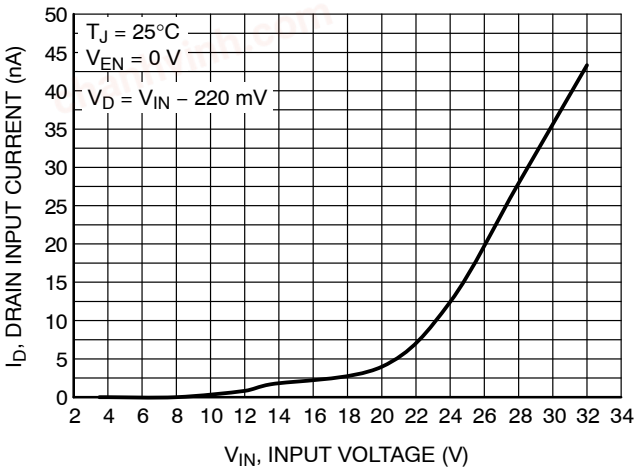


Figure 21. Drain Input Current vs. Input Voltage

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TYPICAL CHARACTERISTICS

Table 8. ISO 7637−2: 2011(E) PULSE TEST RESULTS

ISO 7637−2:2011(E) Test Pulse	Test Severity Levels, 12 V System			Delays and Impedance	# of Pulses or Test Time	Pulse / Burst Rep. Time
	I / II	III	IV			
1	−75	−112	−150	2 ms, 10 Ω	500 pulses	0.5 s
2a	+37	+55	+112	0.05 ms, 2 Ω	500 pulses	0.5 s
3a	−112	−165	−220	0.1 μs, 50 Ω	1 h	100 ms
3b	+75	+112	+150	0.1 μs, 50 Ω	1 h	100 ms

ISO 7637−2:2011(E) Test Pulse	Test Results		
	I / II	III	IV
1	A	E	
2a		A	E
3a	A	E	
3b		A	E

Class	Functional Status
A	All functions of a device perform as designed during and after exposure to disturbance.
B	All functions of a device perform as designed during exposure. However,one or more of them can go beyond specified tolerance. All functions return automatically to within normal limits after exposure is removed. Memory functions shall remain class A.
C	One or more functions of a device do not perform as designed during exposure but return automatically to normal operation after exposure is removed.
D	One or more functions of a device do not perform as designed during exposure and do not return to normal operation until exposure is removed and the device is reset by simple ”operator/use” action.
E	One or more functions of a device do not perform as designed during and after exposure and cannot be returned to proper operation without replacing the device.

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APPLICATION INFORMATION

INTEGRATED CIRCUIT AND BLOCK DIAGRAM DESCRIPTION

Integrated Circuit Description

The NCV68261 can operate in conjunction with one or two external NMOS transistors. Two basic applications can be configured: an Ideal diode application or a Reverse Polarity Protection application defined by the Drain pin connection as shown in the Table 9. The applications with single NMOS are always forward conductive. The applications with two NMOS transistors provide a High Side Switch function to control the power supplied to the application.

Enable

The Enable block turns the controller ON and OFF. If the Enable function is not needed, then the Enable pin can be connected to the Input pin for permanent operation.

References

The References block provides voltage references and voltage supply for other internal circuitry. This block is supplied from the Input and controlled by the Enable block.

Input/Drain Comparator

This comparator compares voltage levels at the Input and Drain pins. Based on the Drain pin connection, the applications can be designed with both Reverse Current Protection and Reverse Polarity Protection features active (Figures 22 and 23) or with Reverse Polarity Protection only (Figures 24 and 25).

UVLO Comparator

The undervoltage lockout (UVLO) comparator compares the Input voltage level with an internal reference voltage level. When the Input voltage falls below the UVLO threshold, the output of the UVLO comparator is set to low resulting in turning OFF the charge pump and switching OFF the external NMOS transistors.

OVLO Comparator

The overvoltage lockout (OVLO) comparator compares the Input voltage level with an internal reference voltage level. When the Input voltage rises above the OVLO threshold, the output of the OVLO comparator is set to high resulting in turning OFF the charge pump and switching OFF the external NMOS transistors.

Logic

The Logic block controls the Charge Pump block according to the inputs from the Input/Drain, UVLO and OVLO comparators. The truth table of the logic function is shown in Table 10.

Pre−regulator

The pre−regulator provides a stable voltage supply for the Charge Pump block.

Oscillator and Charge Pump

The oscillator generates an approximately 2 MHz clock signal that drives the charge pump. The charge pump generates the Gate−Source voltage from the voltage provided by the pre−regulator. The OSC+CP block drives the discharge switch as well.

Table 9. AVAILABLE PROTECTION FEATURES

	Protection Features	
Drain Pin Connection	**Reverse Current Protection**	**Reverse Polarity Protection**
Load Side (Protected Battery) (see Figures 22 and 23)	Yes	Yes
GND (see Figures 24 and 25)	No	Yes

Table 10. TRUTH TABLE OF THE LOGIC BLOCK (@ EN = HIGH)

Input/Drain Comparator	UVLO Comparator	OVLO Comparator	Disch	CP_EN	NMOS
$V_{IN} < V_D$	$V_{IN} < V_{IN_UVLO}$	X	TRUE	FALSE	OFF
$V_{IN} < V_D$	$V_{IN} > V_{IN_UVLO}$	$V_{IN} < V_{IN_OVLO}$	TRUE	FALSE	OFF
$V_{IN} < V_D$	$V_{IN} > V_{IN_UVLO}$	$V_{IN} > V_{IN_OVLO}$	TRUE	FALSE	OFF
$V_{IN} > V_D$	$V_{IN} < V_{IN_UVLO}$	X	TRUE	FALSE	OFF
$V_{IN} > V_D$	$V_{IN} > V_{IN_UVLO}$	$V_{IN} < V_{IN_OVLO}$	FALSE	TRUE	ON
$V_{IN} > V_D$	$V_{IN} > V_{IN_UVLO}$	$V_{IN} > V_{IN_OVLO}$	TRUE	FALSE	OFF

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Operation

The main function of the NCV68261 is to control the ON/OFF state of one or two external NMOS transistors depending on the state of the Enable pin and the difference between the voltages at the Input and Drain pins – as shown in Figures 22 to 25. Figure 5 illustrates the internal connections between the functional blocks described above.

OFF state: When the Enable input is low, the IC is in disable mode. All the internal blocks are turned OFF, and the current consumption is reduced – typically down to tens of nano−amps. In this state, the external transistors are kept OFF by an integrated 1 MΩ resistor between the Gate and Source pins.

ON state: When the Enable input is high, the IC is active. Further operation depends on the output state of the UVLO, OVLO and Input/Drain comparators. Table 10 shows the charge pump, gate discharge, and NMOS transistor states based on the output states of these comparators. The charge pump is turned ON only when the Input voltage level is between the UVLO and OVLO thresholds and above the Drain voltage level.

Undervoltage Lockout: When the Input voltage falls below the UVLO thresholds (typ. 3.25 V), the charge pump is disabled and the external NMOS transistors are turned OFF by an internal PMOS transistor. By decreasing the Input voltage further, the chip is insufficiently powered, and the external NMOSs are kept in OFF state by the integrated 1 MΩ resistor (see Figure 5).

Overvoltage Lockout: When the Input voltage rises above the OVLO thresholds (typ. 35.6 V), the charge pump is disabled and the external NMOS transistors are turned OFF by an internal PMOS transistor.

APPLICATION CONFIGURATIONS

Ideal Diode

In the Ideal Diode configuration (Figure 22), the input voltage is not allowed to discharge the output.

Conduction Mode: Prior to entering the conduction mode, the Input voltage is lower than the Drain voltage, and the charge pump and the NMOS transistor are disabled. As the Input voltage becomes greater than the Drain voltage, forward current flows through the body diode of the NMOS transistor. Once this forward voltage drop exceeds the Input−to−Drain Gate Charge Voltage Threshold level (typ. 140 mV), the charge pump is turned ON and the NMOS transistor becomes fully conductive.

Reverse Current Blocking: When the Input voltage becomes less than the Drain voltage, a reverse current initially flows through the conductive channel of the NMOS transistor. This current creates a voltage drop across the conductive channel of the NMOS transistor which is proportional to its $R_{DS(ON)}$ resistance. When this voltage crosses below the Input−to−Drain Gate Discharge Voltage Threshold (typ. −10 mV), the charge pump is disabled and the external NMOS transistor is turned OFF by an internal PMOS transistor (see Figure 5).

Reverse Polarity Protection (RPP)

By connecting the Drain pin to the GND potential (Figure 24), the NCV68261 does not allow a falling input voltage to discharge the output below GND potential, but it does allow the output to follow any positive input voltage between the UVLO and OVLO thresholds. When the Input voltage is between the UVLO (typ. 3.4 V) and OVLO (typ. 34.8 V) thresholds, the Input/Drain, UVLO and OVLO comparators enable the charge pump to provide Gate−Source voltage to the external NMOS transistor, which is fully conductive. For Input voltage below the UVLO (typ. 3.25 V) or above the OVLO (typ. 35.6 V) thresholds, the charge pump and the NMOS transistor are disabled, and any load current flows through the body diode of the NMOS transistor.

High Side Switch (HSS)

The applications with two NMOS transistors provide High Side Switch function to control the power supply of the application. The first transistor operates as a switch, while the second operates as an Ideal Diode and/or Reverse polarity protection.

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The **Ideal Diode** application in Figure 22 has rectifying properties as a common diode application, while reducing the forward voltage drop on the diode. Th application is in reverse mode as long as the Input voltage is lower than the Drain voltage.

The **Ideal Diode + High Side Switch** (HSS) application in Figure 23 combines the features of the Ideal Diode and an Ideal Switch depending on the Enable (EN) state. If the EN is high the application is in Ideal Diode mode. If the EN is low, the application behaves as an Ideal Switch and the protected battery line is disconnected from the battery line.

The **Reverse Polarity Protection** (RPP) application in Figure 24 protects the load from negative voltages at the battery line.

The **Reverse Polarity Protection + High Side Switch** application in Figure 25 combines the features of the RPP and HSS, similarly to the Ideal Diode + HSS.

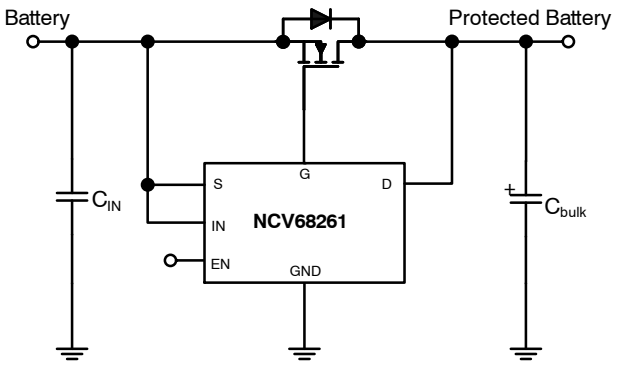


Figure 22. Ideal Diode

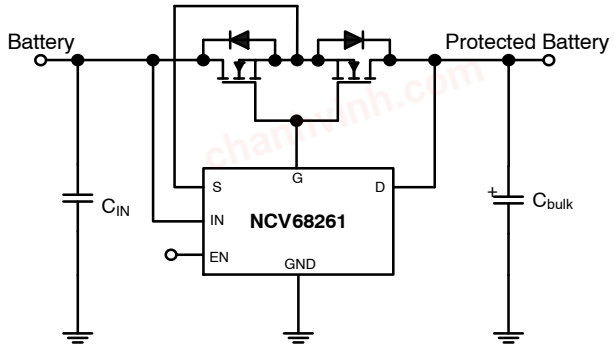


Figure 23. Ideal Diode + High Side Switch

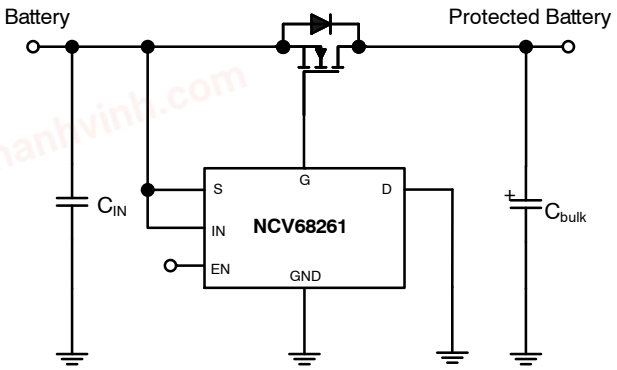


Figure 24. Reverse Polarity Protection

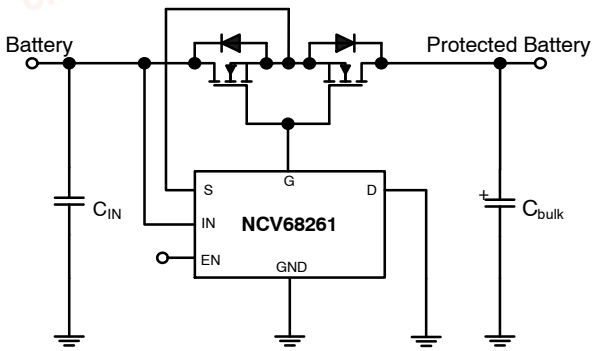


Figure 25. Reverse Polarity Protection + High Side Switch

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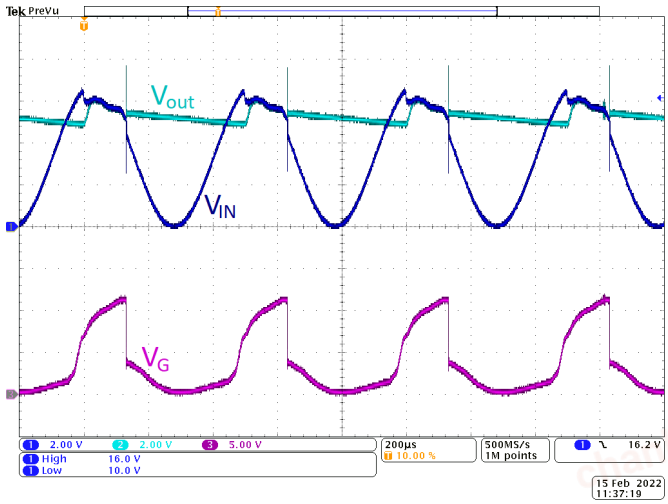


Figure 26. Application Response to 13 V + 6 V_{pp} Sine Wave on the Input (V_{IN}) – Ideal Diode + High Side Switch Application (see Figure 23)

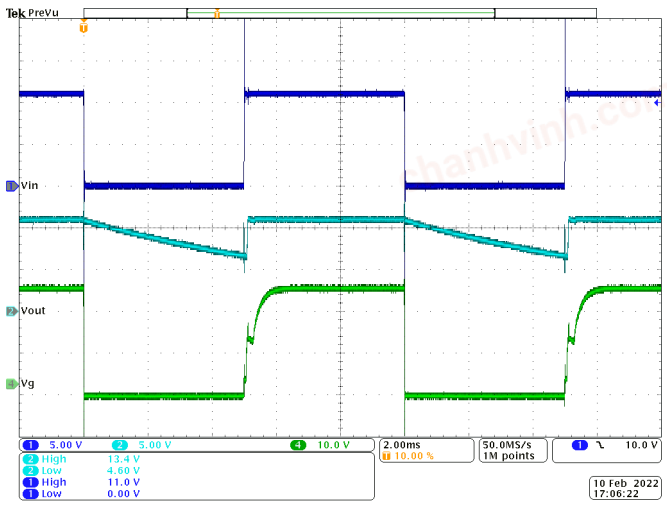


Figure 27. Application Response to 11 V to 0 V Transient on the Input (V_{IN}) – Ideal Diode + High Side Switch Application (see Figure 23)

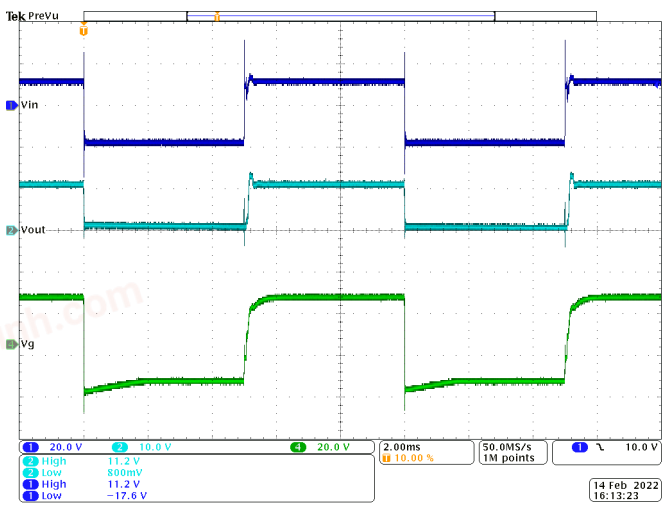


Figure 28. Application response to 11 V to −18 V transient on the Input (V_{IN}) – Reverse Polarity Protection + High Side Switch Application (see Figure 25)

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C_{IN} Capacitor Considerations

For proper device performance, it is recommended that a 0.1 μF ceramic capacitor be placed as close as possible to the NCV68261 and connected with the shortest possible traces. If the device is used in High Side Switch configuration, the C_{IN} capacitor should be large enough to cover the inrush currents flowing into the application during the startup event.

C_{bulk} (Output) Capacitor Considerations

Besides presenting a sufficiently low impedance for the load input rail, in an Ideal Diode application the C_{bulk} capacitance should be high enough to maintain adequate voltage while providing load current for the duration of battery sag plus the charge from reverse current spike before the NMOS transistor turns off. Capacitor ESR is also limited by the $R_{DS(ON)}$ of the NMOS, as high ESR can reduce reverse current flow below that needed to create sufficient NMOS reverse voltage drop (see Figure 26). The value of the C_{bulk} capacitor can be calculated according to the Equation 1:

$$C_{bulk} = \frac{t_{Disch} \cdot \frac{\Delta U_{in}}{n \cdot R_{DS(ON)}} + I_{load} \cdot t_{drop}}{\Delta U_{out}} \quad \text{(eq. 1)}$$

where:

- t_{Disch} – discharge time for the given Gate−Source capacity of the external NMOS (see Figure 10)
- ΔU_{in} – expected battery voltage drop
- n – the number of external transistors used in the application (n = 1 for Ideal Diode or RPP applications, n = 2 for Ideal Diode +HSS or RPP +HSS)
- $R_{DS(ON)}$ – ON resistance of the external NMOS transistor
- t_{drop} – the expected duration of the battery voltage drop
- ΔU_{out} – the maximum allowed drop of the output voltage

NMOS Transistor Considerations

In general, any NMOS can be connected to the NCV68261. There are no special requirements for the transistor. From the NCV68261 perspective, the Gate to Source maximum voltage of the transistor should be rated above a 15 V level (see Table 7 with electrical characteristics) unless an external voltage protection is applied to protect the Gate−Source structure from a breakdown.

EMC and Dynamic Performance Considerations

To improve the EMC immunity to Direct Power Injection, it is recommended to use the application example and PCB layout shown in Figures 29 and 30. The recommended application contains additional capacitor connected to the Gate and GND pins respectively. The recommended component values are listed in the Table 11.

The C_G capacitance limits inrush current as well. The typical measurements are shown in Figures 31 to 33. The R_{G_Q1} and R_S mitigate potential oscillations of the output voltage during start up.

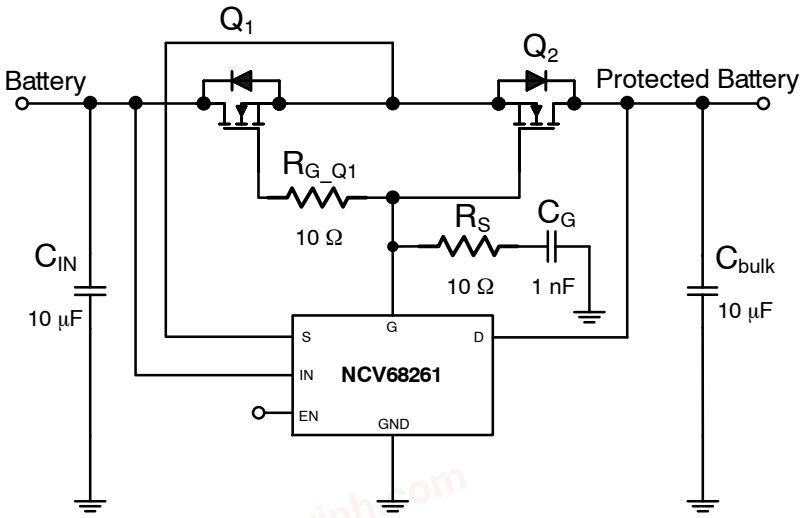


Figure 29. Application Example for Optimized EMC Performance and Inrush Current Control

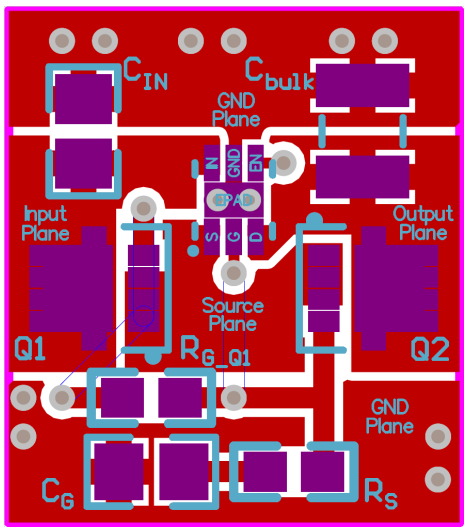


Figure 30. PCB Layout Example

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Table 11. RECOMMENDED COMPONENTS FOR OPTIMAL EMC PERFORMANCE (Note 7)

C_{IN} (µF)	C_{bulk} (µF)	C_G (nF)	R_S (Ω)	R_{G_Q1} (Ω)
0.1	1	1	10	10
0.1	10			
4.7	10			
10	10			
10	10	4.7		

7. Global pins: up to 33 dBm
   Local pins: up to 17 dBm

Table 12. RECOMMENDED EXTERNAL COMPONENT PART NUMBERS

Component	Value/Rating	Part Number
C_G	1 nF/100 V	GCM1885C2A102JA16
C_G	4.7 nF/100 V	GCM188R72A472KA37
C_{IN}	100 nF/100 V	GRM188R72A104KA64
C_{bulk}	1 µF/50 V	GCM21BR71H105KA03
C_{IN}	4.7 µF/50 V	GCM32ER71H475KA55
C_{IN}, C_{bulk}	10 µF/50 V	GCM32EC71H106KA03
R_S, R_{G_Q1}	10 Ω	MC0063W0603110R

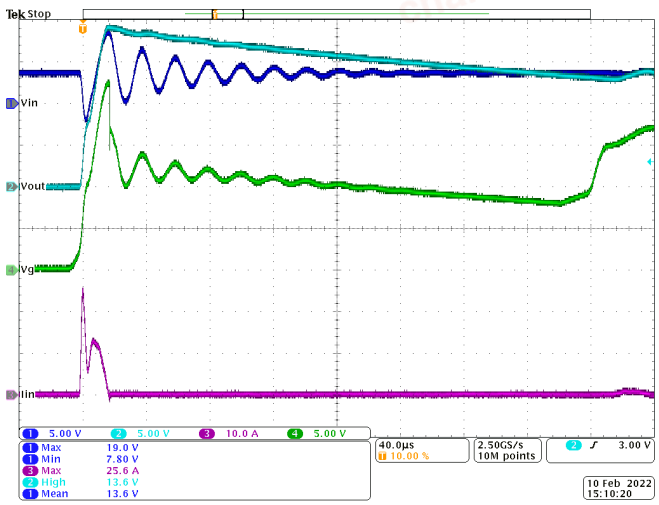


Figure 31. Startup with EN − No Inrush Current Reduction

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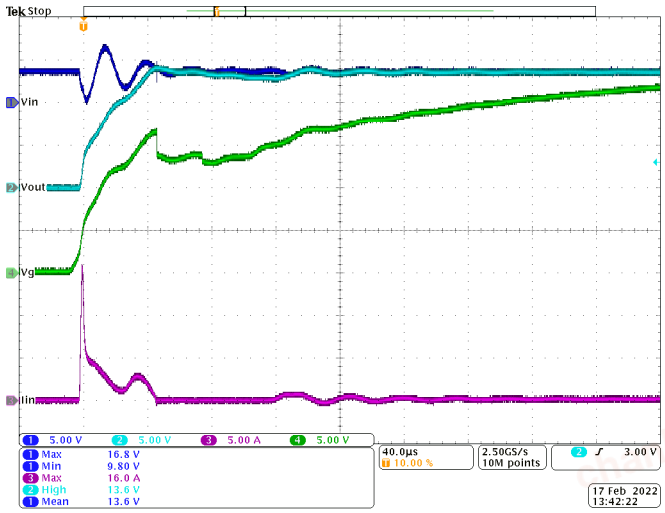


Figure 32. Startup with EN – C_G = 1 nF Inrush Current Reduction

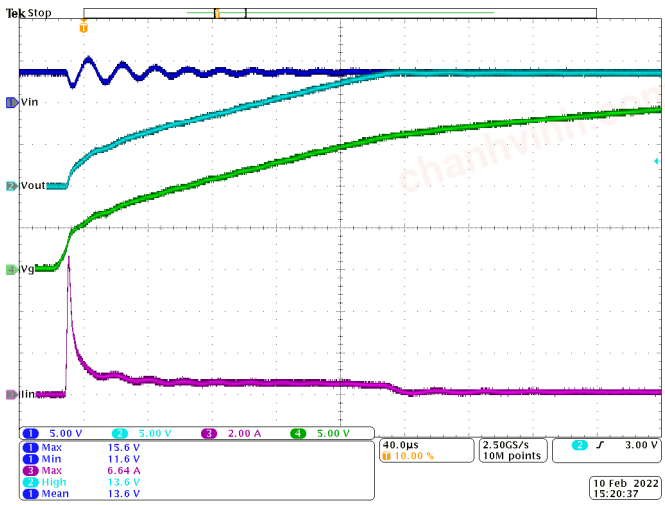


Figure 33. Startup with EN – C_G = 4.7 nF Inrush Current Reduction

Thermal Considerations

The NCV68261 has no thermal protection function as it is not designed to handle large currents itself. Regarding the application, the most heated elements are the external NMOS transistors. In case an SMD transistors are used, maximum power dissipation, thermal resistance of the NMOSs and cooling area of the PCB should be considered to keep the junction temperature of the controller below 150°C.

PCB Layout Considerations

For optimal performance, place the transistors and the input and output capacitors as close as possible to the NCV68261. Tracks carrying high load current – Input (Battery), Source, Drain (Protected Battery) and GND are recommended to connect using power planes on the PCB. An example PCB Layout with inrush current reduction circuitry is shown in Figure 30.

ORDERING INFORMATION

Device	Application	Marking	Package	Shipping†
NCV68261MTWAITBG	Ideal Diode and High Side Switch	V6	WDFNW6 (Pb–Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

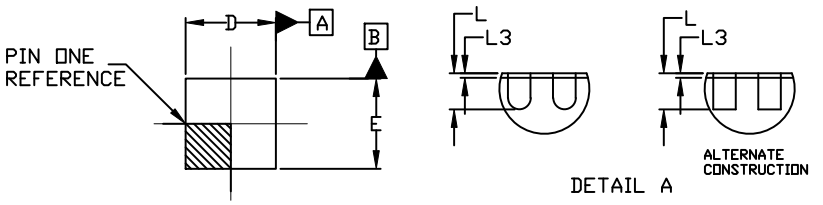
ON Semiconductor®

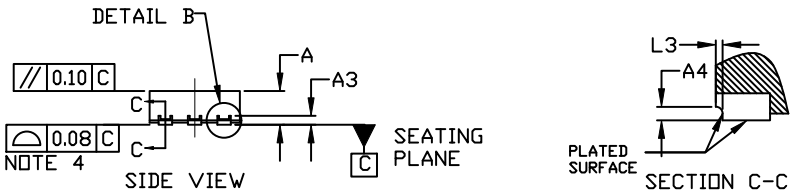
WDFNW6 2x2, 0.65P
CASE 511DW
ISSUE B

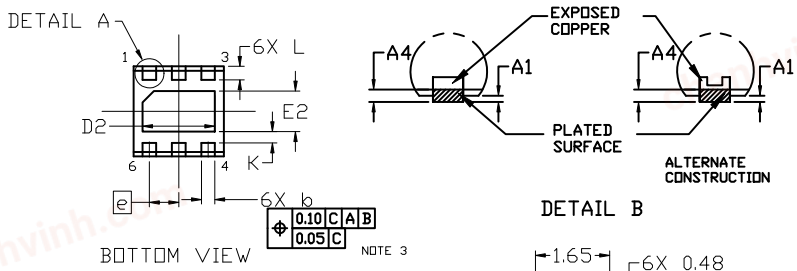
DATE 15 JUN 2018

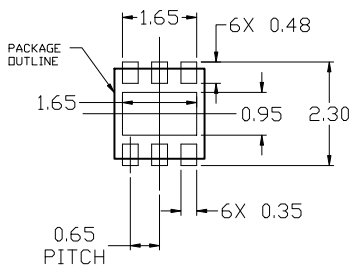


SCALE 4:1







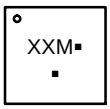


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	---	---	0.05
A3	0.20 REF		
A4	0.10	---	---
b	0.25	0.30	0.35
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	1.90	2.00	2.10
E2	0.80	0.90	1.00
e	0.65 BSC		
K	0.25 REF		
L	0.25	0.30	0.35
L3	0.05 REF		

GENERIC MARKING DIAGRAM*



M = Month Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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