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DATA SHEET
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Isolated High Current IGBT/MOSFET Gate Driver

NCx57080y, NCx57081y
(x = D or V, y = A, B or C)



SOIC−8 NB
CASE 751−07

NCx57080y, NCx57081y are high−current single channel IGBT/MOSFET gate drivers with 3.75 kVrms internal galvanic isolation, designed for high system efficiency and reliability in high power applications. The devices accept complementary inputs and depending on the pin configuration, offer options such as Active Miller Clamp (version A), negative power supply (version B) and separate high and low (OUTH and OUTL) driver outputs (version C) for system design convenience. The driver accommodate wide range of input bias voltage and signal levels from 3.3 V to 20 V and they are available in narrow−body SOIC−8 package.

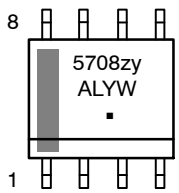
Features

- High Peak Output Current (+6.5 A/−6.5 A)
- Low Clamp Voltage Drop Eliminates the Need of Negative Power Supply to Prevent Spurious Gate Turn−on (Version A)
- Short Propagation Delays with Accurate Matching
- IGBT/MOSFET Gate Clamping during Short Circuit
- IGBT/MOSFET Gate Active Pull Down
- Tight UVLO Thresholds for Bias Flexibility
- Wide Bias Voltage Range including Negative V_{EE2} (Version B)
- 3.3 V, 5 V, and 15 V Logic Input
- 3.75 kV_{RMS} $V_{ISO\ (I-O)}$ (to meet UL1577 Requirements)
- Safety and Regulatory Approvals:
  - UL1577 Certified, 3750 VAC_{RMS} for 1 Minute
  - DIN VDE V 0884−11 Certification Pending, 870 V_{PK} Working Insulation Voltage
- High Transient Immunity
- High Electromagnetic Immunity
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Motor Control
- Uninterruptible Power Supplies (UPS)
- Automotive Applications
- Industrial Power Supplies
- Solar Inverters
- HVAC

MARKING DIAGRAM



5708zy	= Specific Device Code z = 0/1 y = A/B/C
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS

See detailed pin connection information on page 2 of this data sheet.

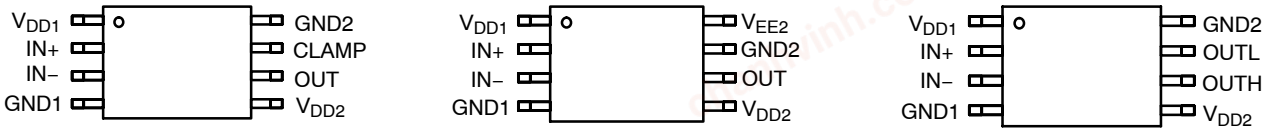
ORDERING INFORMATION

See detailed ordering and shipping information on page 21 of this data sheet.

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PIN CONNECTIONS



NCx57080A, NCx57081A **NCx57080B, NCx57081B** **NCx57080C, NCx57081C**

NOTE: x = D or V

Figure 1. Pin Connections

BLOCK DIAGRAM AND APPLICATION SCHEMATIC – NCx5708zA

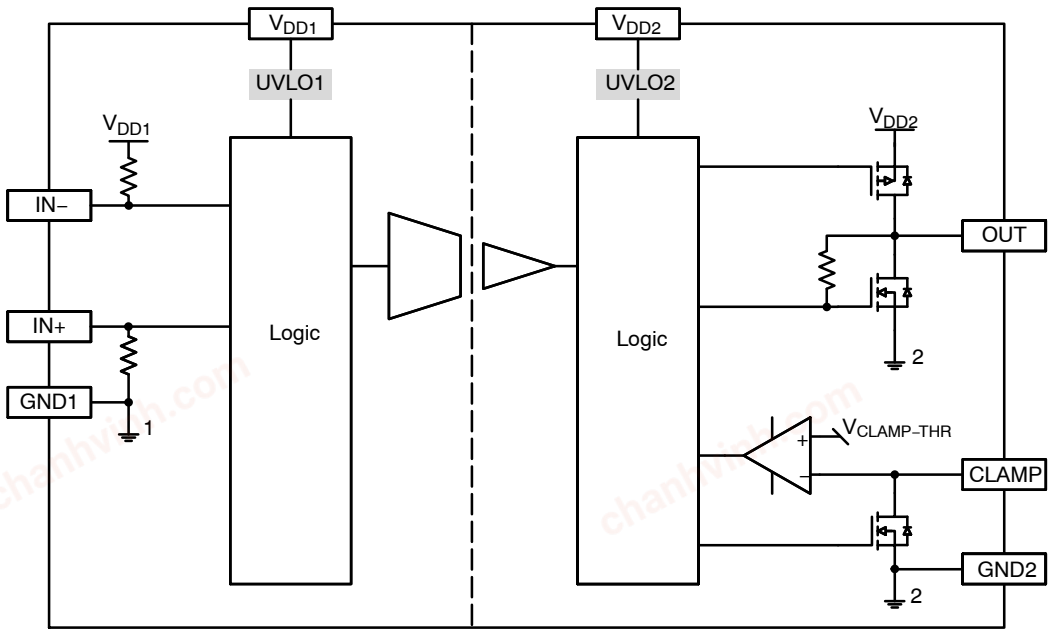


Figure 2. Simplified Block Diagram, NCx5708zA

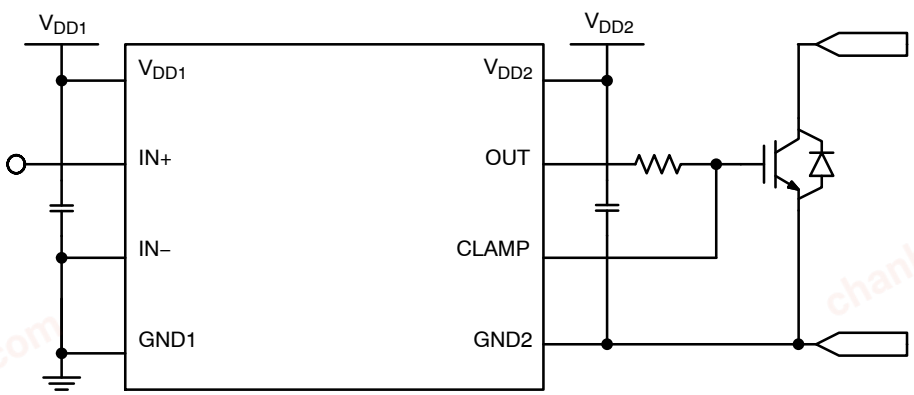


Figure 3. Simplified Application Schematics, NCx5708zA

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BLOCK DIAGRAM AND APPLICATION SCHEMATIC – NCx5708zB

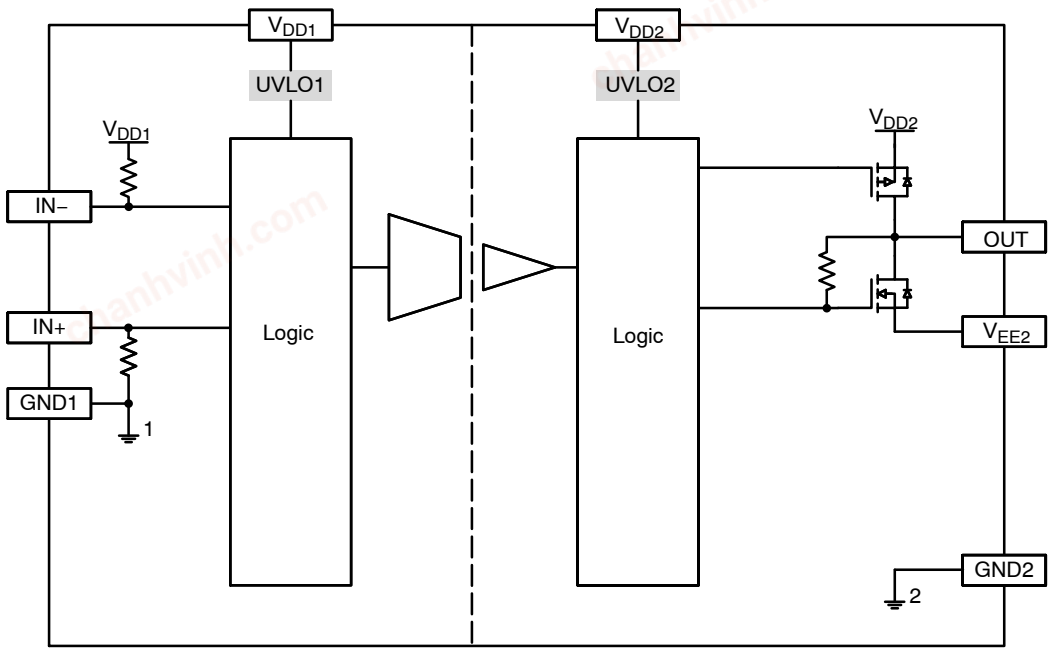


Figure 4. Simplified Block Diagram, NCx5708zB

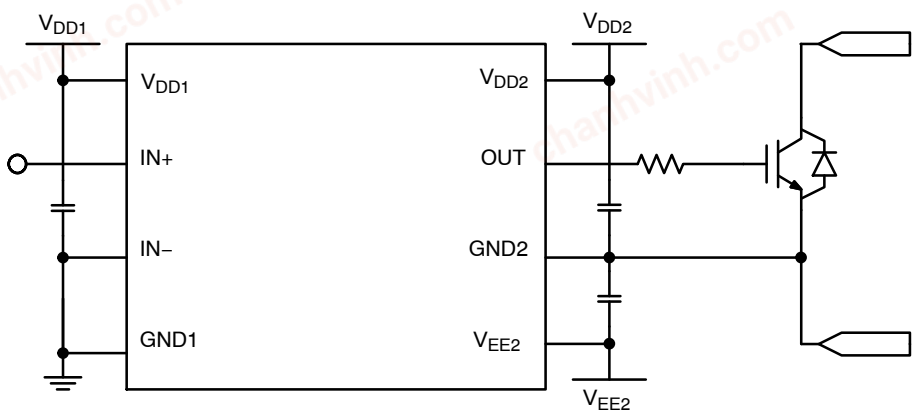


Figure 5. Simplified Application Schematics, NCx5708zB

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BLOCK DIAGRAM AND APPLICATION SCHEMATIC – NCx5708zC

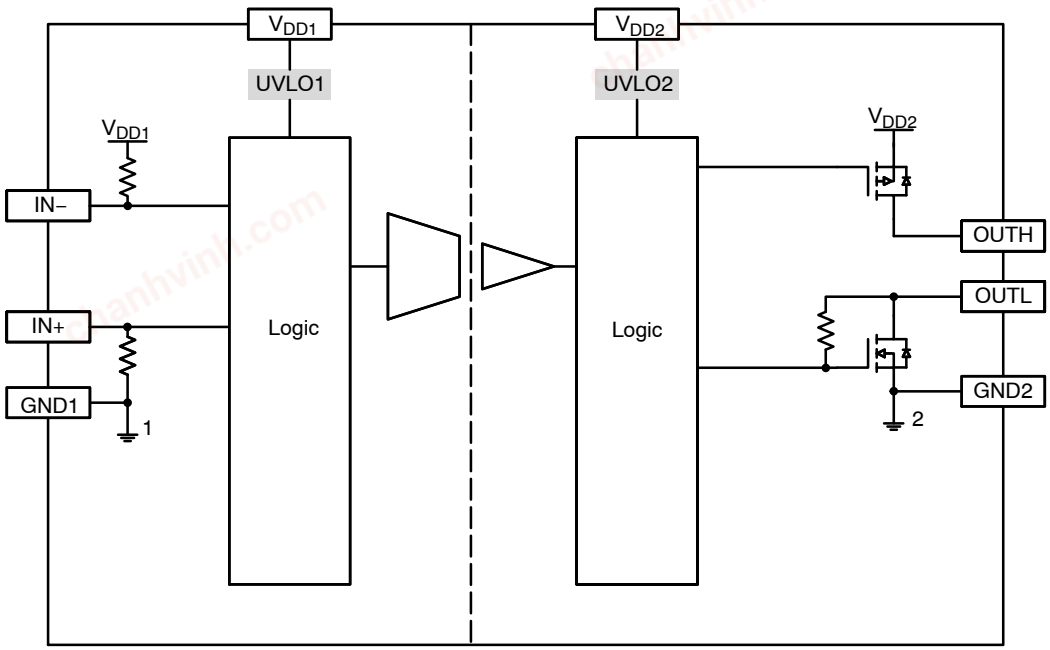


Figure 6. Simplified Block Diagram, NCx5708zC

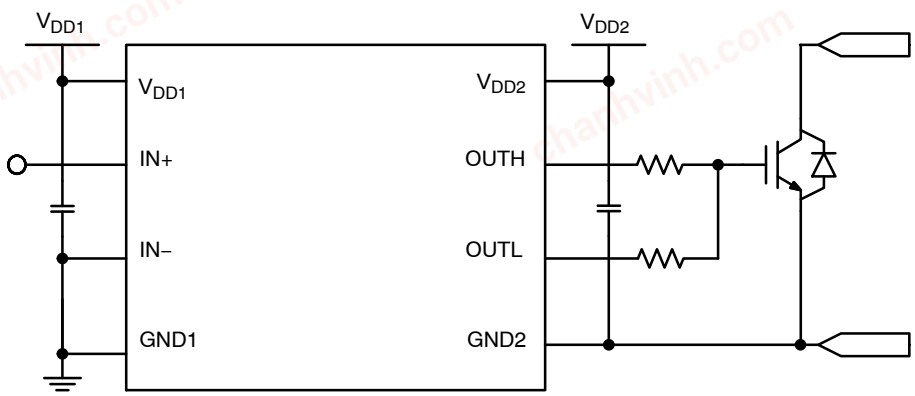


Figure 7. Simplified Application Schematics, NCx5708zC

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Table 1. FUNCTION DESCRIPTION

Pin Name	No.	I/O	Description
V_{DD1}	1	Power	Input side power supply. A good quality bypassing capacitor is required from this pin to GND1 and should be placed close to the pins for best results. The under voltage lockout (UVLO) circuit enables the device to operate at power on when a typical supply voltage higher than $V_{UVLO1-OUT-ON}$ is present. Please see Figures 9A and 9B for more details.
IN+	2	I	Non inverted gate driver input. It is internally clamped to GND1 and has an equivalent pull−down resistor of 125 kΩ to ensure that output is low in the absence of an input signal. A minimum positive or negative pulse−width is required at IN+ before OUT or OUTH/OUTL responds.
IN−	3	I	Inverted gate driver input. It is internally clamped to V_{DD1} and has an equivalent pull−up resistor of 125 kΩ to ensure that output is low in the absence of an input signal. A minimum positive or negative pulse−width is required at IN− before OUT or OUTH/OUTL responds.
GND1	4	Power	Input side ground reference.
V_{DD2}	5	Power	Output side positive power supply. The operating range for this pin is from UVLO2 to its maximum allowed value. A good quality bypassing capacitor is required from this pin to GND2 and should be placed close to the pins for best results. The under voltage lockout (UVLO) circuit enables the device to operate at power on when a typical supply voltage higher than $V_{UVLO2-OUT-ON}$ is present. Please see Figure 9C and 9D for more details.
GND2 (NCx5708zA, NCx5708zC)	8	Power	Output side gate drive reference connecting to IGBT emitter or MOSFET source.
GND2 (NCx5708zB)	7		
OUT (NCx5708zA, NCx5708zB)	6	O	Driver output that provides the appropriate drive voltage and source/sink current to the IGBT/MOSFET gate. OUT is actively pulled low during start−up.
OUTH (NCx5708zC)	6	O	Driver high output that provides the appropriate drive voltage and source current to the IGBT/MOSFET gate.
OUTL (NCx5708zC)	7	O	Driver low output that provides the appropriate drive voltage and sink current to the IGBT/MOSFET gate. OUTL is actively pulled low during start−up.
CLAMP (NCx5708zA)	7	O	Provides clamping for the IGBT/MOSFET gate during the off period to protect it from parasitic turn−on. Its internal N FET is turned on when the voltage of this pin falls below $V_{CLAMP-THR}$. It is to be tied directly to IGBT/MOSFET gate with minimum trace length for best results.
V_{EE2} (NCx5708zB)	8	Power	Output side negative power supply. A good quality bypassing capacitor is required from this pin to GND2 and should be placed close to the pins for best results.

NOTE: (x = D or V, z = 0 or 1)

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Table 2. SAFETY AND INSULATION RATINGS

Symbol	Parameter		Value	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1 Rated Mains Voltage	< 150 V_{RMS}	I – IV	
		< 300 V_{RMS}	I – IV	
		< 450 V_{RMS}	I – IV	
		< 600 V_{RMS}	I – IV	
		< 1000 V_{RMS}	I – III	
CTI	Comparative Tracking Index (DIN IEC 112/VDE 0303 Part 1)		600	
	Climatic Classification		40/125/21	
	Pollution Degree (DIN VDE 0110/1.89)		2	
V_{PR}	Input−to−Output Test Voltage, Method b, $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with tm = 1 s, Partial Discharge < 5 pC		2250	V_{pk}
V_{IORM}	Maximum Repetitive Peak Voltage		1200	V_{pk}
V_{IOWM}	Maximum Working Voltage		870	V_{RMS}
V_{IOTM}	Highest Allowable Over Voltage		6300	V_{pk}
E_{CR}	External Creepage		4.0	mm
E_{CL}	External Clearance		4.0	mm
DTI	Insulation Thickness		17.3	μm
T_{Case}	Safety Limit Values – Maximum Values in Failure; Case Temperature		150	°C
$P_{S,INPUT}$	Safety Limit Values – Maximum Values in Failure; Input Power		121	mW
$P_{S,OUTPUT}$	Safety Limit Values – Maximum Values in Failure; Output Power		1194	mW
R_{IO}	Insulation Resistance at TS, V_{IO} = 500 V		10^9	Ω

Table 3. ABSOLUTE MAXIMUM RATINGS (Note 1)

Over operating free−air temperature range unless otherwise noted.

Symbol	Parameter	Minimum	Maximum	Unit
V_{DD1}−GND1	Supply Voltage, Input Side	−0.3	22	V
V_{DD2}−GND2	Positive Power Supply, Output Side	−0.3	32	V
V_{EE2}−GND2	Negative Power Supply, Output Side	−18	0.3	V
V_{DD2}−V_{EE2} (V_{MAX2})	Differential Power Supply, Output Side (NCx5708zB)	0	36	V
V_{OUT}−GND2 V_{OUTH}−GND2	Gate−driver Output High Voltage NCx5708zA/B NCx5708zC	– –	V_{DD2} + 0.3 –	V
V_{OUT}−GND2 V_{OUTL}−GND2	Gate−driver Output Low Voltage NCx5708zA/B NCx5708zC	−0.3 –	– –	V
I_{PK-SRC}	Gate−driver Output Sourcing Current (maximum pulse width = 10 μs, maximum duty cycle = 0.2%, V_{DD2} = 15 V, V_{EE2} = 0 V)	–	6.5	A
I_{PK-SNK}	Gate−driver Output Sinking Current (maximum pulse width = 10 μs, maximum duty cycle = 0.2%, V_{DD2} = 15 V, V_{EE2} = 0 V)	–	6.5	A
$I_{PK-CLAMP}$	Clamp Sinking Current (maximum pulse width = 10 μs, maximum duty cycle = 0.2%, V_{CLAMP} = 2.5 V)	–	2.5	A
t_{CLP}	Maximum Short Circuit Clamping Time (I_{OUT_CLAMP} = 500 mA)	–	10	μs
V_{LIM}−GND1	Voltage at IN+, IN−	−0.3	V_{DD1} + 0.3	V
V_{CLAMP}−GND2	Clamp Voltage	−0.3	V_{DD2} + 0.3	V
P_D	Power Dissipation (SOIC−8 Narrow Package)	–	1315	mW

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Table 3. ABSOLUTE MAXIMUM RATINGS (Note 1) (continued)
Over operating free−air temperature range unless otherwise noted.

Symbol	Parameter	Minimum	Maximum	Unit
T_J(max)	Maximum Junction Temperature	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
ESDHBM	ESD Capability, Human Body Model (Note 2)	−	±2	kV
ESDCDM	ESD Capability, Charged Device Model (Note 2)	−	±2	kV
MSL	Moisture Sensitivity Level	−	1	−
T_{SLD}	Lead Temperature Soldering Reflow, Pb−Free (Note 3)	−	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114).
   ESD Charged Device Model tested per AEC−Q100−011 (EIA/JESD22−C101).
   Latchup Current Maximum Rating: ≤ 100 mA per JEDEC standard:
   JESD78, 25°C (absolute maximum ratings for all tests)
   JESD78, 125°C (limitation for IN+ test, V_{DD1} = IN+ = 12 V maximum)
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 4. THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Characteristics, SOIC−8 narrow body (Note 4) Thermal Resistance, Junction−to−Air (Note 5)	95 (4−Layer) 175 (1−Layer)	°C/W

4. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
5. Values based on copper area of 100 mm² (or 0.16 in²) of 1 oz copper thickness and FR4 PCB substrate.

Table 5. OPERATING RANGES (Note 6)

Symbol	Parameter	Min	Max	Unit
V_{DD1}−GND1	Supply Voltage, Input Side	UVLO1	20	V
V_{DD2}−GND2	Positive Power Supply, Output Side	UVLO2	30	V
V_{EE2}−GND2	Negative Power Supply, Output Side (NCx5708zB)	−15	0	V
V_{DD2}−VEE2 (V_{MAX2})	Differential Power Supply, Output Side (NCx5708zB)	0	32	V
V_{IL}	Low Level Input Voltage at IN+, IN− (Note 7)	0	0.3 × V_{DD1}	V
V_{IH}	High Level Input Voltage at IN+, IN− (Note 7)	0.7 × V_{DD1}	V_{DD1}	V
$\lvert dV_{ISO}/dt \rvert$	Common Mode Transient Immunity (Note 8)	100	−	kV/μs
T_A	Ambient Temperature	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
7. Table values are valid for 3.3 V and 5 V V_{DD1}, for higher V_{DD1} voltages, the threshold values are maintained at the 5 V V_{DD1} levels.
8. Was tested by ±1500 V pulses up to 100 kV/μs.

Table 6. ISOLATION CHARACTERISTICS

Symbol	Parameter	Conditions	Value	Unit
$V_{ISO,\ input-output}$	Input−Output Isolation Voltage	T_A = 25°C, Relative Humidity < 50%, t = 1.0 minute, I_{I-O} < 30 μA, 50 Hz (Note 9, 10, 11)	3750	V_{RMS}
R_{ISO}	Isolation Resistance	V_{I-O} = 500 V (Note 9)	10^{11}	Ω

9. Device is considered a two−terminal device: pins 1 to 4 are shorted together and pins 5 to 9 are shorted together.
10. 3750 V_{RMS} for 1−minute duration is equivalent to 4500 V_{RMS} for 1−second duration.
11. The input−output isolation voltage is a dielectric voltage rating per UL1577. It should not be regarded as an input−output continuous voltage rating. For the continuous working voltage rating, refer to equipment−level safety specification or DIN VDE V 0884−11 Safety and Insulation Ratings Table.

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ELECTRICAL CHARACTERISTICS V_{DD1} = 5 V, V_{DD2} = 15 V, (V_{EE2} = 0 V for NCx5708zB).
For typical values T_A = 25°C, for min/max values, T_A is the operating ambient temperature range that applies, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VOLTAGE SUPPLY						
$V_{UVLO1-OUT-ON}$	UVLO1 Output Enabled		–	–	3.1	V
$V_{UVLO1-OUT-OFF}$	UVLO1 Output Disabled		2.4	–	–	V
$V_{UVLO1-HYST}$	UVLO1 Hysteresis		0.1	–	–	V
$V_{UVLO2-OUT-ON}$	UVLO2 Output Enabled	NCx57080y	12.4	12.9	13.4	V
		NCx57081y	8.6	9	9.5	V
$V_{UVLO2-OUT-OFF}$	UVLO2 Output Disabled	NCx57080y	11.5	12	12.5	V
		NCx57081y	7.6	8	8.5	V
$V_{UVLO2-HYST}$	UVLO2 Hysteresis		0.7	1	–	V
$I_{DD1-0-3.3}$	Input Supply Quiescent Current	IN+ = Low, IN– = Low, V_{DD1} = 3.3 V	–	–	2	mA
$I_{DD1-0-5}$		IN+ = Low, IN– = Low	–	–	2	mA
$I_{DD1-0-15}$		IN+ = Low, IN– = Low, V_{DD1} = 15 V	–	–	2	mA
$I_{DD1-100-5}$		IN+ = High, IN– = Low	–	–	5.5	mA
I_{DD2-0}	Output Positive Supply Quiescent Current	IN+ = Low, IN– = Low, no load	–	–	2	mA
$I_{DD2-100}$		IN+ = High, IN– = Low, no load	–	–	2	mA
I_{EE2-0}	Output Negative Supply Quiescent Current (NCx5708zB)	IN+ = Low, IN– = Low, no load, V_{EE2} = –8 V	–	–	2	mA
$I_{EE2-100}$		IN+ = High, IN– = Low, no load, V_{EE2} = –8 V	–	–	2	mA
LOGIC INPUT AND OUTPUT						
V_{IL}	IN+, IN–, Low Input Voltage	Level scale for V_{DDI} = 3.3 to 5 V for V_{DDI} > 5 V is the same as for V_{DDI} = 5 V	–	–	0.3 × V_{DD1}	V
V_{IH}	IN+, IN–, High Input Voltage	Level scale for V_{DDI} = 3.3 to 5 V for V_{DDI} > 5 V is the same as for V_{DDI} = 5 V	0.7 × V_{DD1}	–	–	V
$V_{IN-HYST}$	Input Hysteresis Voltage	Level scale for V_{DDI} = 3.3 to 5 V for V_{DDI} > 5 V is the same as for V_{DDI} = 5 V	–	0.15 × V_{DD1}	–	V
$I_{IN-L-3.3}$	IN– Input Current	V_{IN-} = 0 V, V_{DD1} = 3.3 V	–	–	100	μA
I_{IN-L-5}		V_{IN-} = 0 V	–	–	100	μA
$I_{IN-L-15}$		V_{IN-} = 0 V, V_{DD1} = 15 V	–	–	100	μA
$I_{IN-L-20}$		V_{IN-} = 0 V, V_{DD1} = 20 V	–	–	100	μA
$I_{IN+H-3.3}$	IN+ Input Current	V_{IN+} = V_{DD1} = 3.3 V	–	–	100	μA
I_{IN+H-5}		V_{IN+} = V_{DD1} = 5 V	–	–	100	μA
$I_{IN+H-15}$		V_{IN+} = V_{DD1} = 15 V	–	–	100	μA
$I_{IN+H-20}$		V_{IN+} = V_{DD1} = 20 V	–	–	100	μA
$t_{ON-MIN1}$	Input Pulse Width of IN+, IN– for Guaranteed No Response at Output		–	–	10	ns
$t_{ON-MIN2}$	Input Pulse Width of IN+, IN– for Guaranteed Response at Output		40	–	–	ns

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ELECTRICAL CHARACTERISTICS V_{DD1} = 5 V, V_{DD2} = 15 V, (V_{EE2} = 0 V for NCx5708zB).
For typical values T_A = 25°C, for min/max values, T_A is the operating ambient temperature range that applies, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DRIVER OUTPUT						
V_{OUTL1}	Output Low State (V_{OUT} – GND2 for NCx5708zA) (V_{OUT} – V_{EE2} for NCx5708zB) (V_{OUTL} – GND2 for NCx5708zC)	I_{SINK} = 200 mA	–	0.15	0.3	V
V_{OUTL2}		I_{SINK} = 1.0 A, T_A = 25°C (Note 12)	–	–	0.8	
V_{OUTH1}	Output High State (V_{DD2} – V_{OUT} for NCx5708zA/B) (V_{DD2} – V_{OUT} for NCx5708zB) (V_{DD2} – V_{OUTL} for NCx5708zC)	I_{SRC} = 200 mA	–	0.2	0.35	V
V_{OUTH2}		I_{SRC} = 1.0 A, T_A = 25°C (Note 12)	–	–	1.0	
$I_{PK-SNK1}$	Peak Driver Current, Sink (Note 12)		–	6.5	–	A
$I_{PK-SRC1}$	Peak Driver Current, Source (Note 12)		–	6.5	–	A
MILLER CLAMP (NCx5708zA)						
V_{CLAMP}	Clamp Voltage	I_{CLAMP} = 2.5 A, T_A = 25°C	–	2	–	V
		I_{CLAMP} = 2.5 A, T_A = –40°C to 125°C	–	–	3.5	
$V_{CLAMP-THR}$	Clamp Activation Threshold		1.5	2	2.5	V
IGBT SHORT CIRCUIT CLAMPING						
$V_{CLAMP-OUTH}$	Clamping Voltage, Sourcing (V_{OUT} / V_{OUTH} – V_{DD2})	IN+ = Low, IN– = High, $I_{CLAMP-OUT/OUTH}$ = 500 mA, (pulse test, t_{CLPmax} = 10 μs)	–	0.7	1.3	V
$V_{CLAMP-OUTL}$	Clamping Voltage, Sinking (V_{OUTL} – V_{DD2})	IN+ = High, IN– = Low, $I_{CLAMP-OUTL}$ = 500 mA, (pulse test, t_{CLPmax} = 10 μs)	–	0.8	1.5	V
$V_{CLAMP-CLAMP}$	Clamping Voltage, Clamp (V_{CLAMP} – V_{DD2}) (NCx5708zA)	IN+ = High, IN– = Low, $I_{CLAMP-CLAMP}$ = 500 mA (pulse test, t_{CLPmax} = 10 μs)	–	1.1	1.7	V
DYNAMIC CHARACTERISTIC						
	IN+, IN– to Output High Propagation Delay	C_{LOAD} = 10 nF V_{IH} to 10% of output change Pulse Width > 150 ns.	–	–	–	–
$t_{PD-ON-3.3}$		V_{DD1} = V_{IN+} = 3.3V, V_{IN-} = 0 V	40	60	90	ns
$t_{PD-ON-5}$		V_{DD1} = V_{IN+} = 5 V, V_{IN-} = 0 V	40	60	90	ns
$t_{PD-ON-15}$		V_{DD1} = V_{IN+} = 15 V, V_{IN-} = 0 V	40	60	90	ns
$t_{PD-ON-20}$		V_{DD1} = V_{IN+} = 20 V, V_{IN-} = 0 V	40	60	90	ns
	IN+, IN– to Output Low Propagation Delay	C_{LOAD} = 10 nF V_{IH} to 10% of output change Pulse Width > 150 ns.	–	–	–	–
$t_{PD-OFF-3.3}$		V_{DD1} = V_{IN+} = 3.3 V, V_{IN-} = 0 V	40	60	90	ns
$t_{PD-OFF-5}$		V_{DD1} = V_{IN+} = 5 V, V_{IN-} = 0 V	40	60	90	ns
$t_{PD-OFF-15}$		V_{DD1} = V_{IN+} = 15 V, V_{IN-} = 0 V	40	60	90	ns
$t_{PD-OFF-20}$		V_{DD1} = V_{IN+} = 20 V, V_{IN-} = 0 V	40	60	90	ns
$t_{DISTORT}$	Propagation Delay Distortion (= t_{PD-ON} – t_{PD-OFF})	T_A = 25°C, PW > 150 ns	–	0	–	ns
		T_A = –40°C to 125°C, PW > 150 ns	–25	–	25	ns
$t_{DISTORT_TOT}$	Prop Delay Distortion between Parts	PW > 150 ns	–30	0	30	ns
t_{RISE}	Rise Time (see Figure 8)	C_{LOAD} = 1 nF, 10% to 90% of Output Change	–	13	–	ns
t_{FALL}	Fall Time (see Figure 8)	C_{LOAD} = 1 nF, 90% to 10% of Output Change	–	13	–	ns

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ELECTRICAL CHARACTERISTICS V_{DD1} = 5 V, V_{DD2} = 15 V, (V_{EE2} = 0 V for NCx5708zB).
For typical values T_A = 25°C, for min/max values, T_A is the operating ambient temperature range that applies, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTIC						
t_{UVF1}	UVLO1 Fall Delay (Note 12)		–	1500	–	ns
t_{UVR1}	UVLO1 Rise Delay (Note 12)		–	770	–	ns
t_{UVF2}	UVLO2 Fall Delay (Note 12)		–	1000	–	ns
t_{UVR2}	UVLO2 Rise Delay (Note 12)		–	1000	–	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
12. Values based on design and/or characterization.

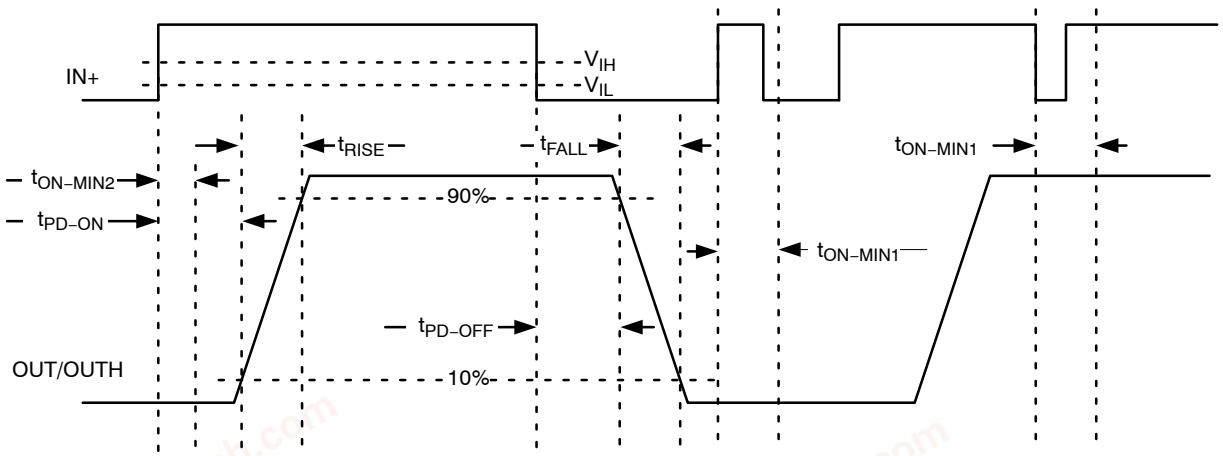
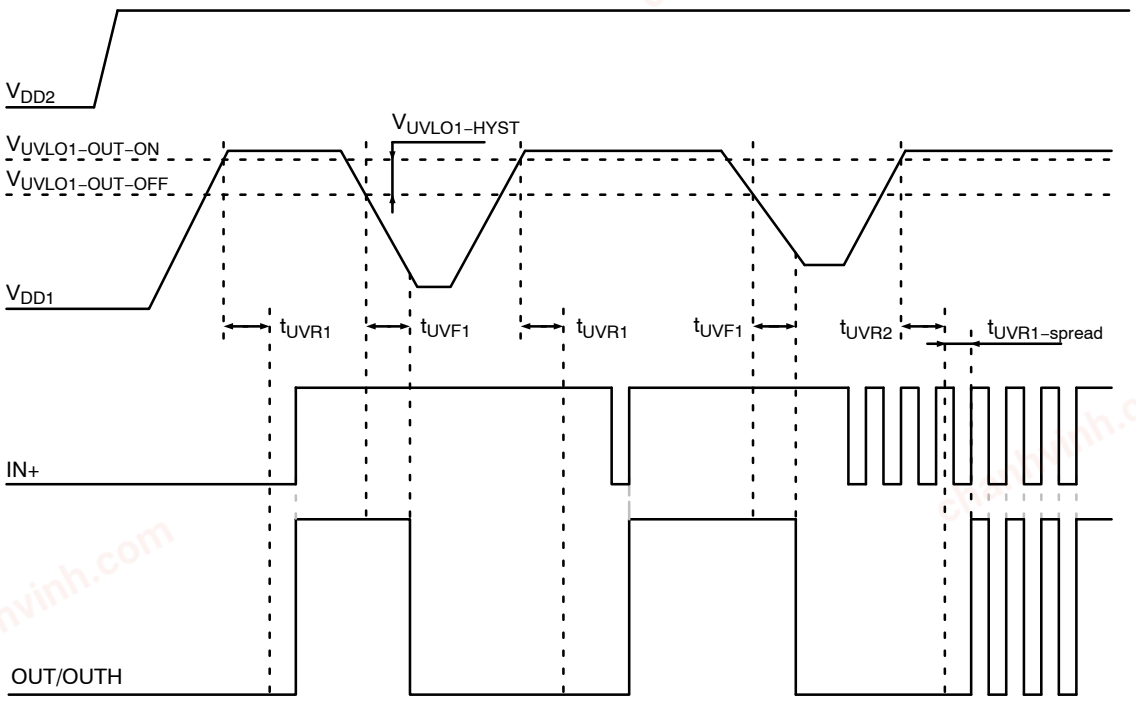


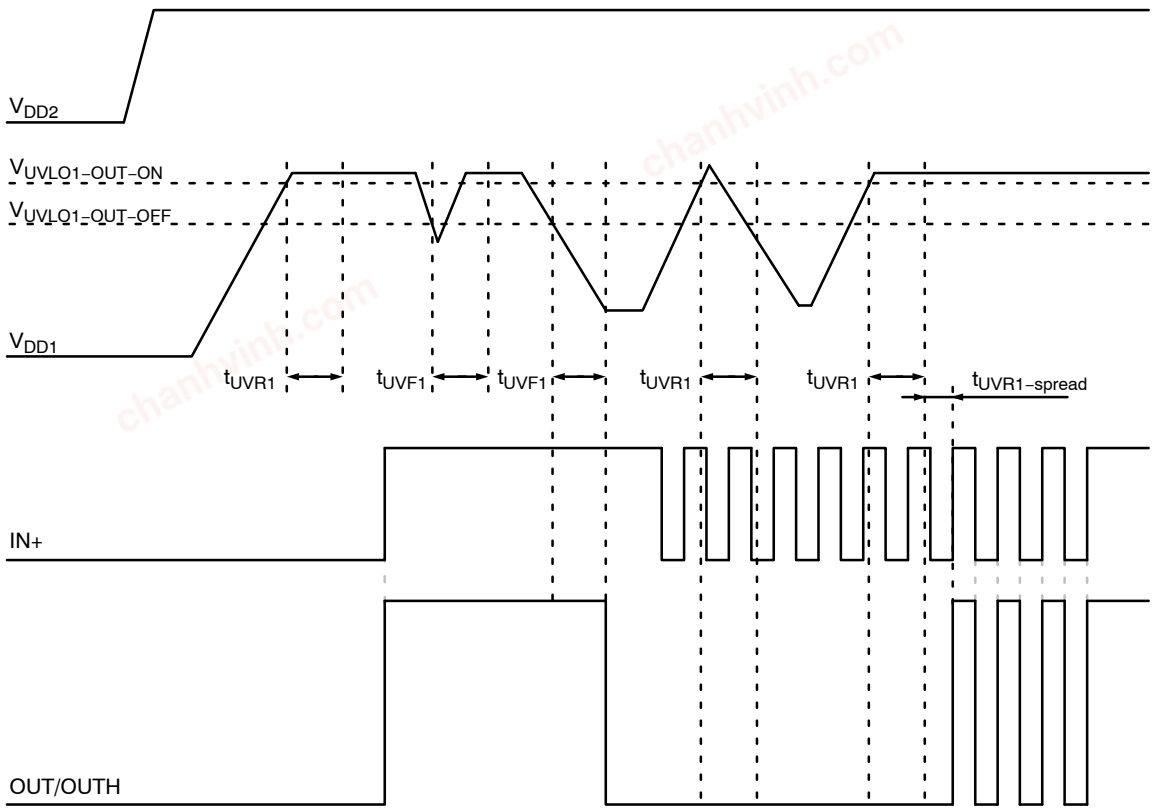
Figure 8. Propagation Delay, Rise and Fall time



Output Ramp−up and Ramp−down Times during UVLO1

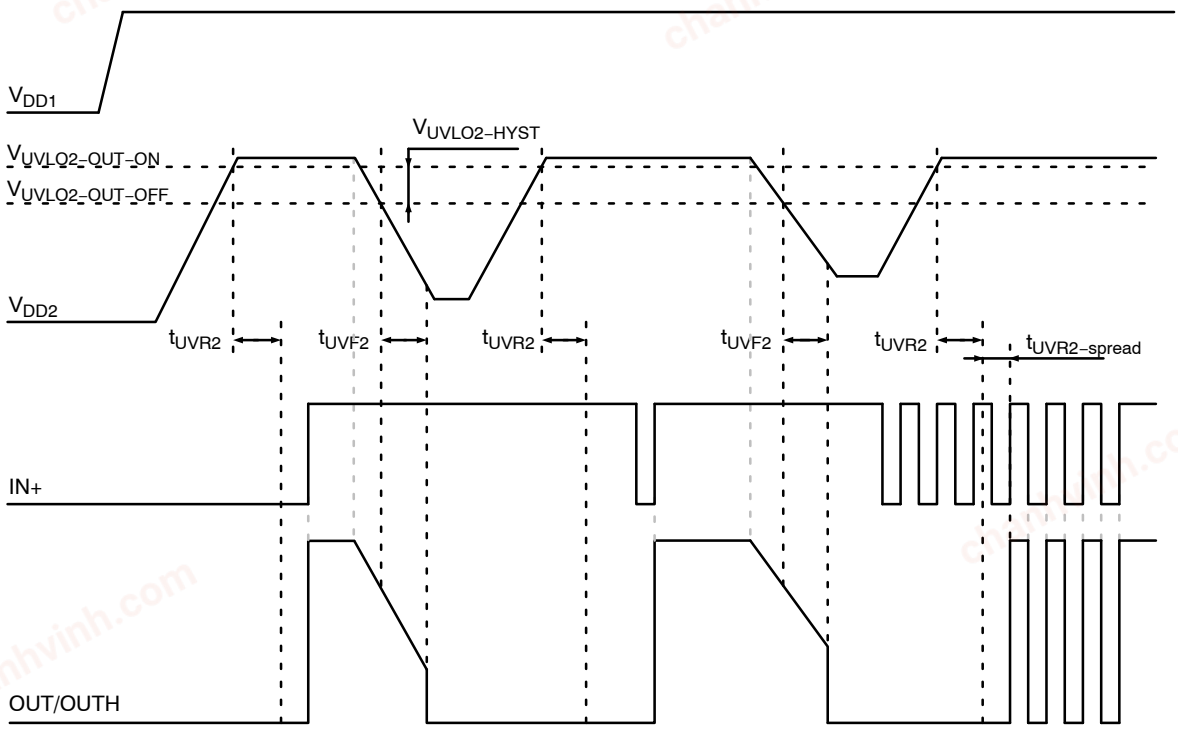
Figure 9A. UVLO1 and Associated Timing Waveforms

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V_{DD1} Glitch Filtering

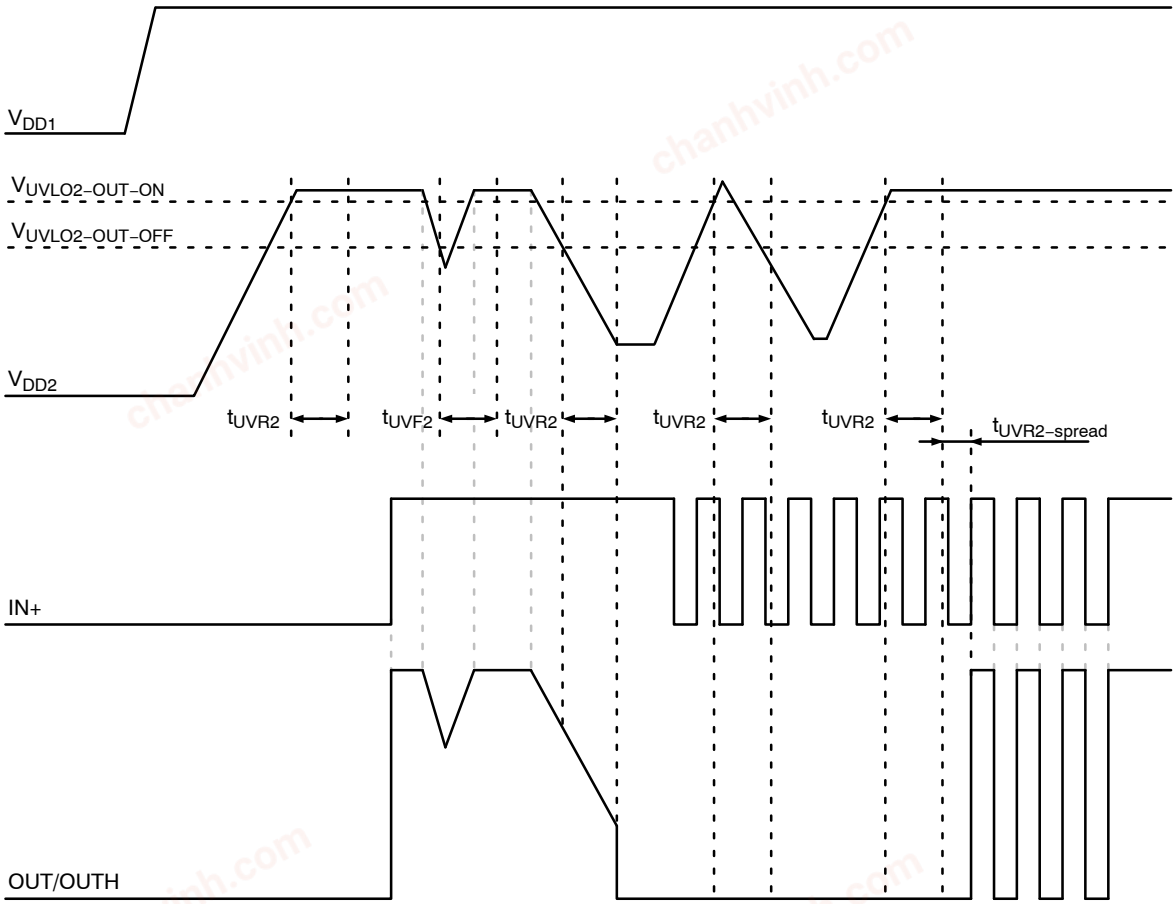
Figure 9B. UVLO1 Waveforms Depicting V_{DD1} Glitch Filtering



Output Ramp−up and Ramp−down Times during UVLO2

Figure 9C. UVLO2 and Associated Timing Waveforms

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V_{DD2} Glitch Filtering

Figure 9D. UVLO2 Waveforms Depicting V_{DD2} Glitch Filtering

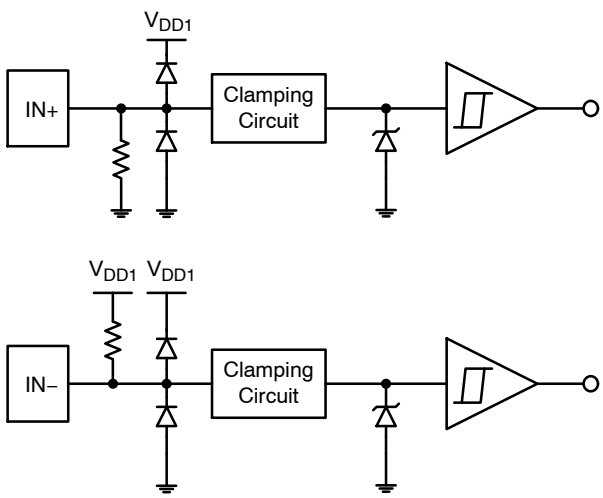


Figure 10. Input Pin Structure

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TYPICAL CHARACTERISTICS

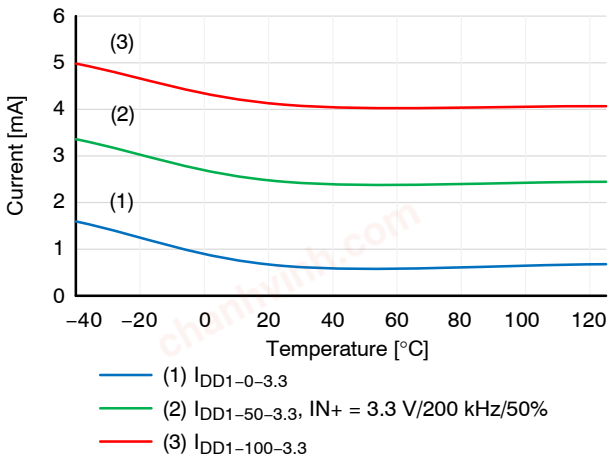


Figure 11. I_{DD1} Supply Current V_{DD1} = 3.3 V

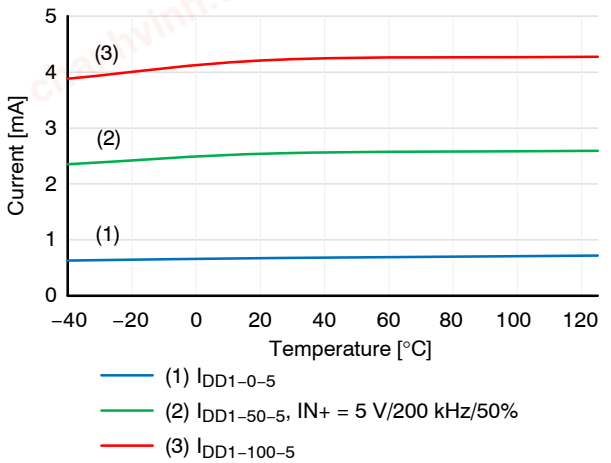


Figure 12. I_{DD1} Supply Current V_{DD1} = 5 V

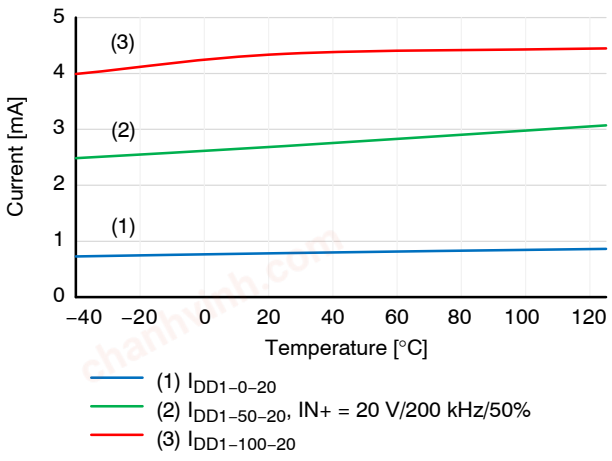


Figure 13. I_{DD1} Supply Current V_{DD1} = 20 V

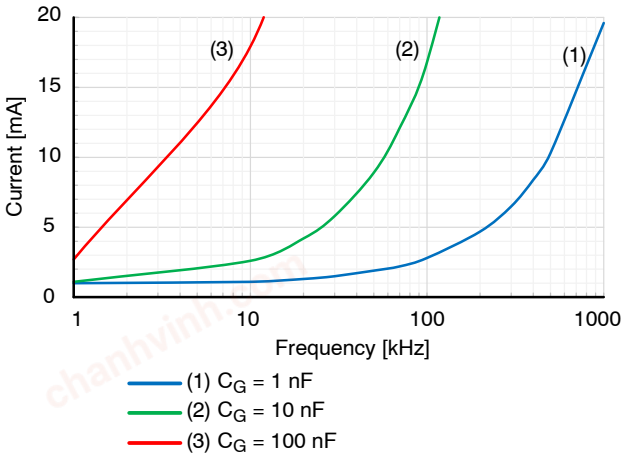


Figure 14. I_{DD2} vs. Switching Frequency

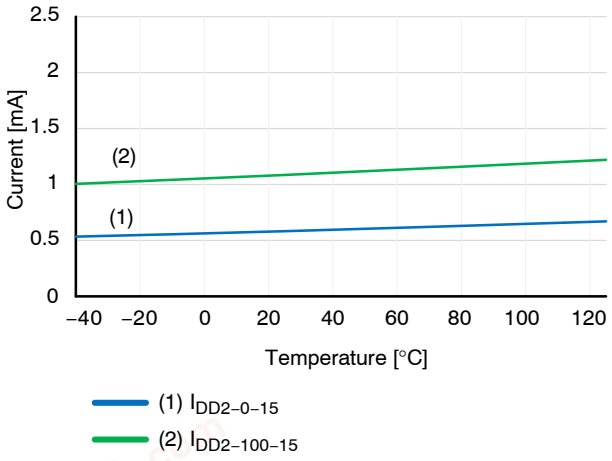


Figure 15. I_{DD2} Supply Current V_{DD2} = 15 V

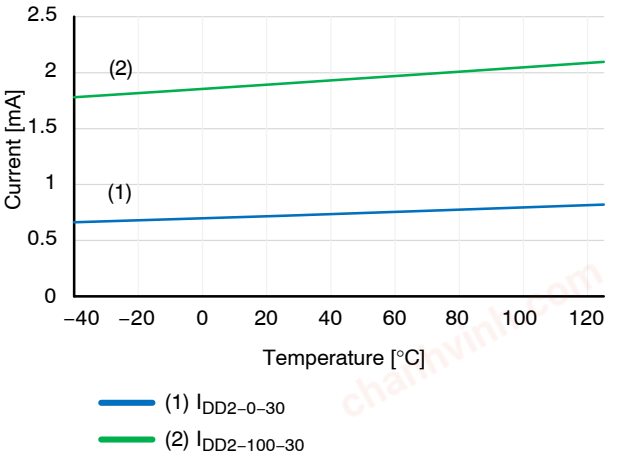


Figure 16. I_{DD2} Supply Current V_{DD2} = 30 V

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TYPICAL CHARACTERISTICS (continued)

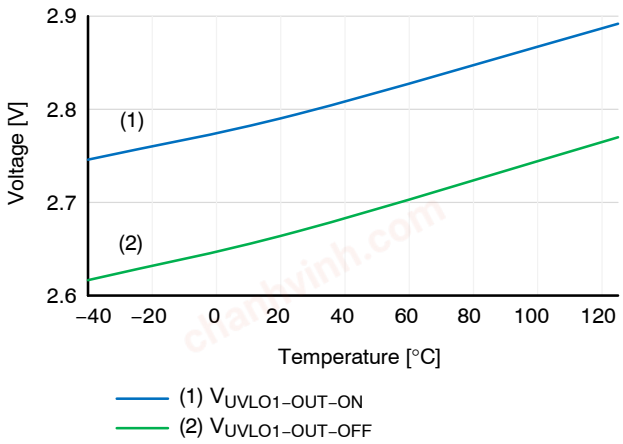


Figure 17. UVLO1 Threshold Voltage

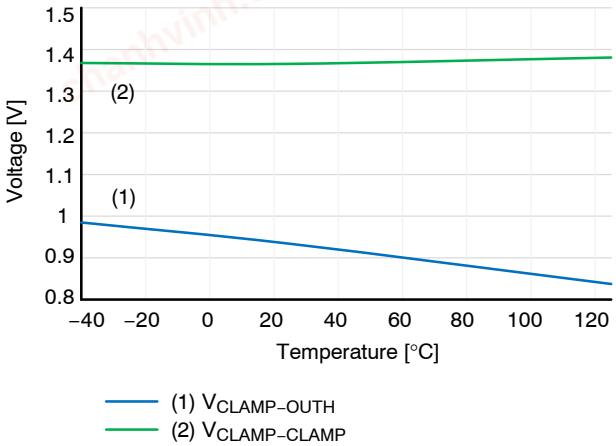


Figure 18. IGBT Short Circuit CLAMP Voltage Drop

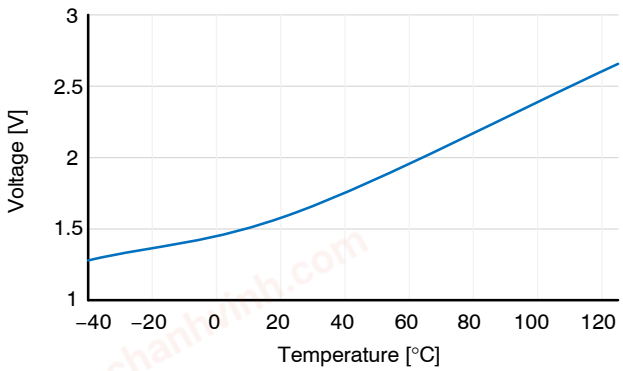


Figure 19a. Miller Clamp Voltage (2.5 A)

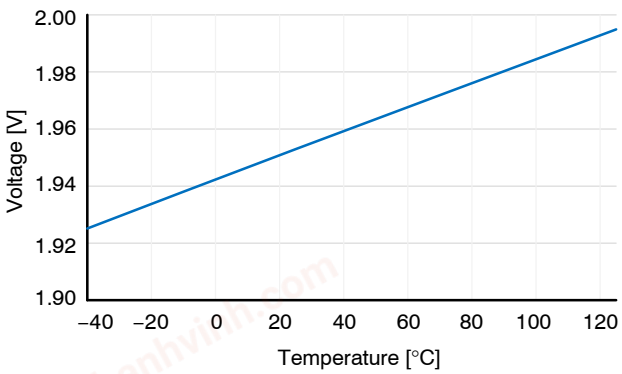


Figure 19b. Miller Clamp Activation Voltage Threshold

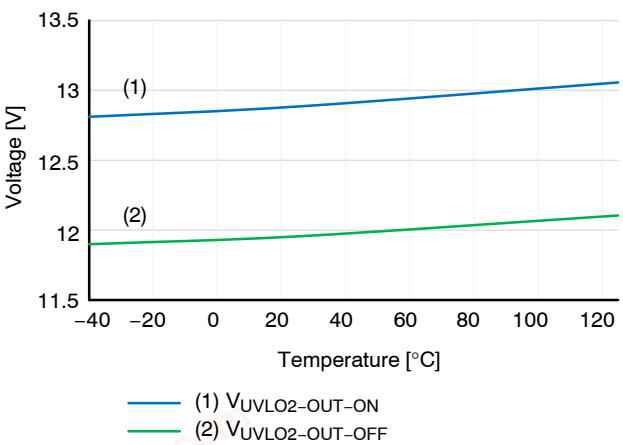


Figure 20. NCx57080 UVLO2 Threshold Voltage

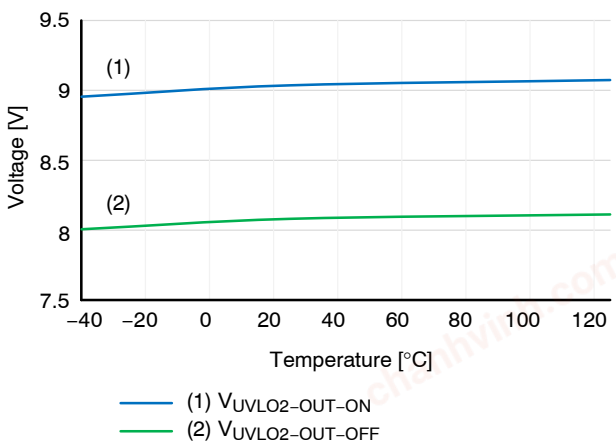


Figure 21. NCx57081 UVLO2 Threshold Voltage

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TYPICAL CHARACTERISTICS (continued)

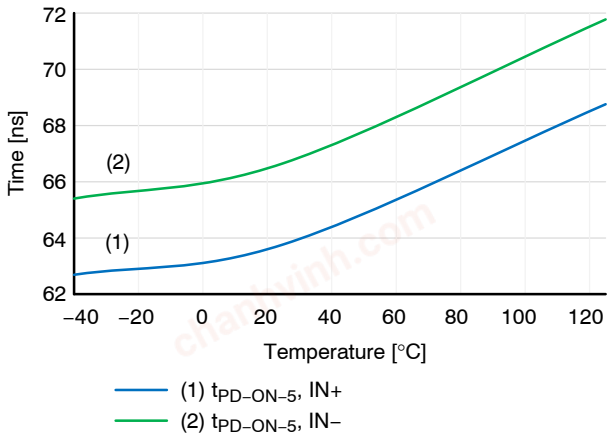


Figure 22. Propagation Delay Turn−on

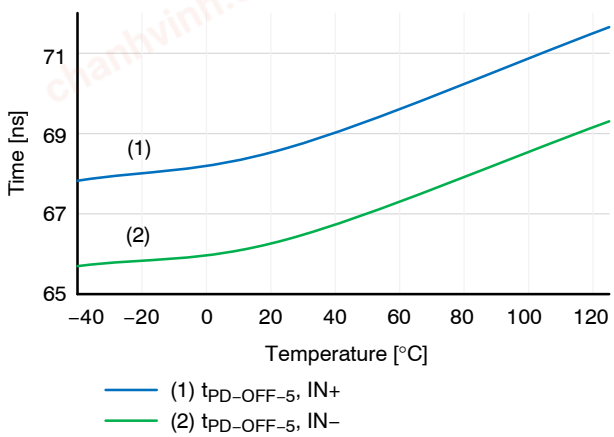


Figure 23. Propagation Delay Turn−off

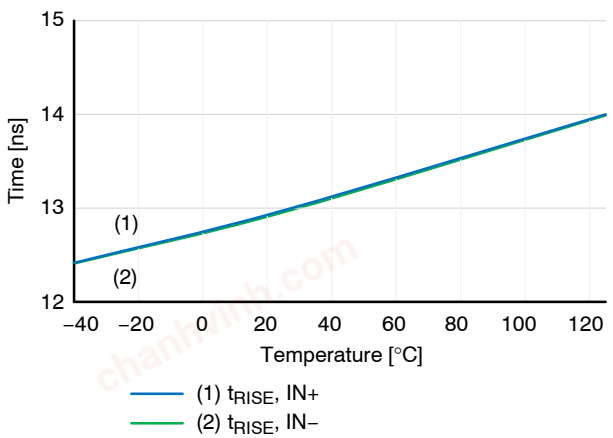


Figure 24. Rise Time, V_{DD1} = 5 V

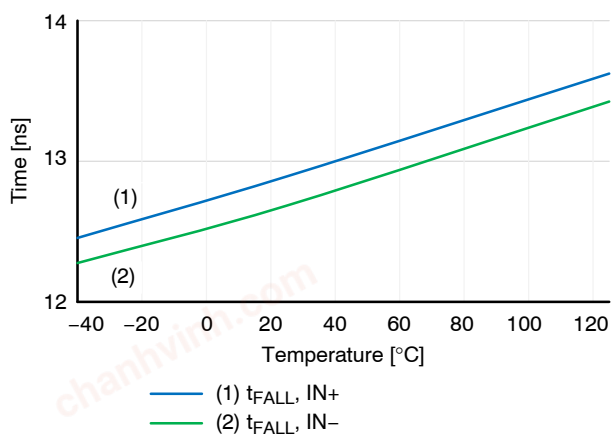


Figure 25. Fall Time, V_{DD1} = 5 V

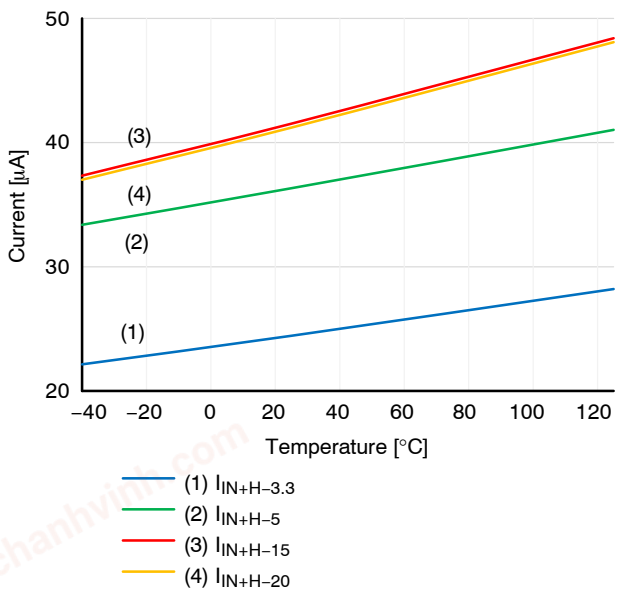


Figure 26. Input Current – Positive Input

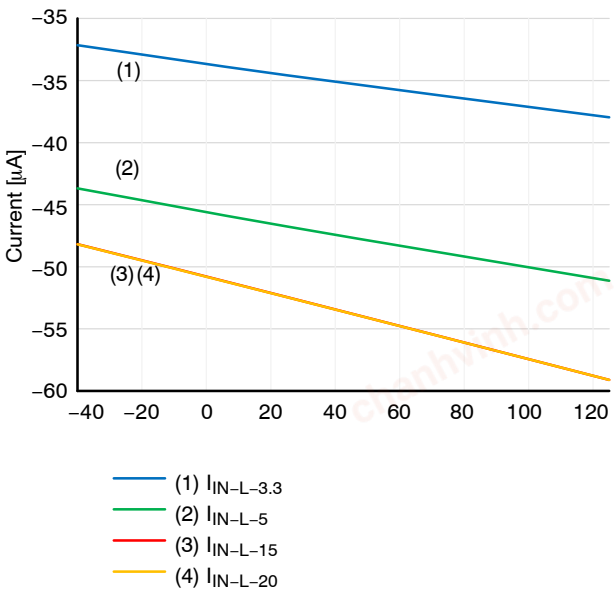


Figure 27. Input Current – Negative Input

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Under Voltage Lockout (Refer to Figure 9x)

UVLO ensures correct switching of IGBT/MOSFET connected to the driver output.

- The IGBT/MOSFET is turned−off and the output is disabled if the supply V_{DD1} drops below $V_{UVLO1−OUT−OFF}$ or V_{DD2} drops below $V_{UVLO2−OUT−OFF}$.
- The driver output does not follow the input signal on IN+ or IN− until the V_{DDX} rises above the $V_{UVLOX−OUT−ON}$ and the input signal rising edge is applied to the IN+ or IN−
- V_{EE2} is not monitored (NCx5708zB)

With high loading gate capacitances over 10 nF it is important to follow the decoupling capacitor routing guidelines as shown on Figure 35. The decoupling capacitor value should be at least 10 μF. Also gate resistor of minimal value of 2 Ω has to be used in order to avoid interference of the high di/dt with internal circuitry (e.g. UVLO2).

After the power−on of the driver there has to be a rising edge applied to the IN+ or falling edge to the IN− in order for the output to start following the inputs. This serves as a protection against producing partial pulses at the output if the V_{DD1} or V_{DD2} is applied in the middle of the input PWM pulse.

If the V_{DD2} rises over $V_{UVLO2−OUT−ON}$ level the PWM will appear on the output after $t_{UVR2} + t_{UVR2−spread}$. The $t_{UVR2−spread}$ time is variable and is defined as a time from end of t_{UVR2} to first rising edge on IN+ input. If the V_{DD2} is starting from 0 V the time until PWM is at the output of the driver is longer than $t_{UVR2} + t_{UVR2−spread}$. This is caused by start up time of internal circuits of the driver.

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ACTIVE MILER CLAMP PROTECTION (CLAMP)

NCx5708yB supports bipolar power supply to prevent unintentional turning on.

For operation with bipolar supplies, the IGBT/MOSFET is turned off with a negative voltage through OUT with respect to its emitter. This prevents the IGBT/MOSFET from unintentionally turning on because of current induced from its collector to its gate due to Miller effect. Typical values for bipolar operation are V_{DD2} = 15 V and V_{EE2} = −5 V with respect to GND2.

Driver version A supports unipolar power supply with active Miller clamp.

For operation with unipolar supply, typically, V_{DD2} = 15 V with respect to GND2, and V_{EE2} = GND2. In this case, the IGBT/MOSFET can turn on due to additional charge from IGBT/MOSFET Miller capacitance caused by a high voltage slew rate transition on the IGBT collector/MOSFET drain. To prevent IGBT/MOSFET to turn on, the CLAMP pin is connected directly to IGBT/MOSFET gate and Miller current is sinked through a low impedance CLAMP transistor. When the IGBT/MOSFET is turned−off and the gate voltage transitions below V_{CLAMP}, the CLAMP output is activated.

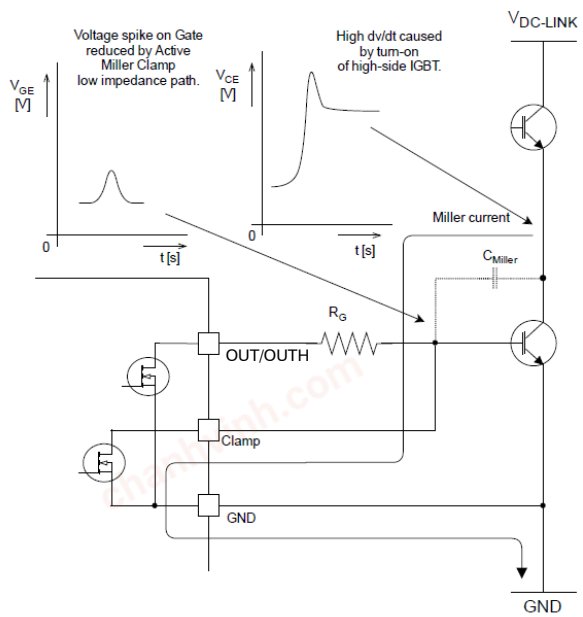


Figure 28. Current Path with Miler Clamp Protection

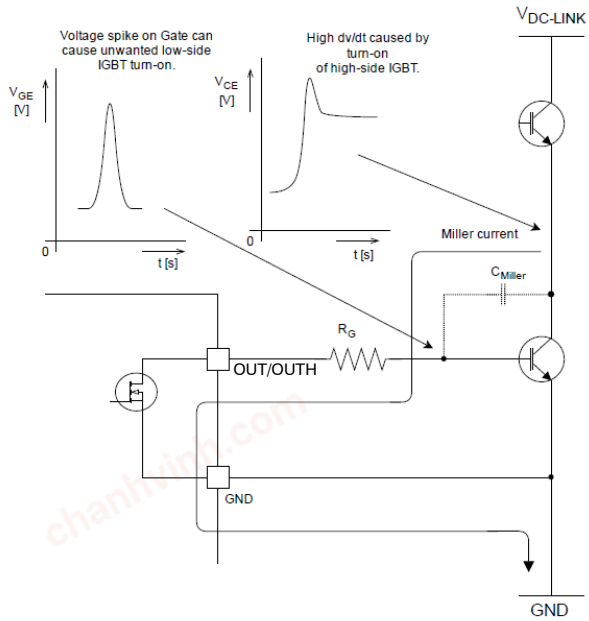


Figure 29. Current Path without Miler Clamp Protection

Non−inverting and Inverting Input Pin (IN+, IN−)

The driver has two possible input modes to control IGBT/MOSFET. Both inputs have defined minimum input pulse width to filter occasional glitches.

- Non−inverting input IN+ controls the driver output while inverting input IN− is set to LOW
- Inverting input IN− controls the driver output while non−inverting input IN+ is set to HIGH

WARNING: When the application uses an independent or separate power supply for the control unit and the input side of the driver, all inputs should be protected by a serial resistor (In case of a power failure of the driver, the driver may be damaged due to overloading of the input protection circuits)

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Power Supply (V_{DD1}, V_{DD2}, V_{EE2})

The driver variant A and C are designed to support unipolar power supply.

The driver variant B is designed to support bipolar power supply.

Suitable external power capacitors are required for reliable driving of IGBT/MOSFET gate with high current. Parallel combination of 100 nF + 4.7 μF low ESR ceramic capacitors is optimal for a wide range of applications using IGBT/MOSFET. For reliable driving of IGBT modules (containing several parallel IGBT's) with a gate capacitance over 10 nF a higher decoupling capacity is required (typically 100 nF + 10 μF). Capacitors should be as close as possible to the driver's power pins. The recommended layout is provided in the Figure 35.

- In bipolar power supply the driver is typically supplied with a positive voltage of 15 V at V_{DD2} and negative voltage −5 V at V_{EE2} (Figure 30). Negative power supply prevents a dynamic turn on through the internal IGBT/MOSFET input capacitance
- In Unipolar power supply the driver is typically supplied with a positive voltage of 15 V at V_{DD2}. Unwanted turn−on caused by the internal IGBT/MOSFET Miller capacitance could be prevented by Active Miler Clamp function (variant A). CLAMP output should be directly connected to IGBT/MOSFET gate (Figure 28)

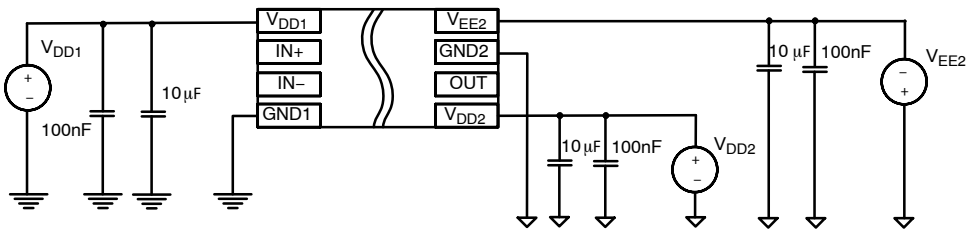


Figure 30. Bipolar Power Supply (NCx5708zB)

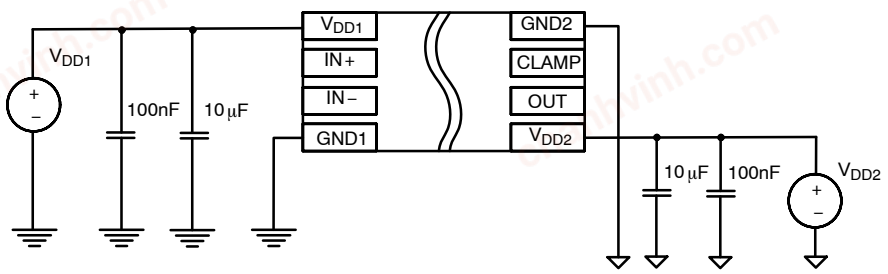


Figure 31. Unipolar Power Supply (NCx5708zA)

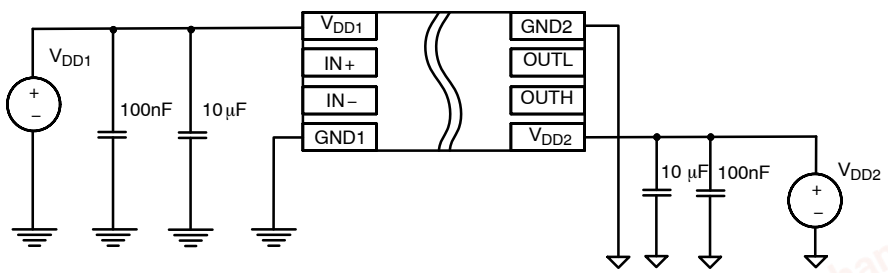


Figure 32. Unipolar Power Supply (NCx5708zC)

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Common Mode Transient Immunity (CMTI)

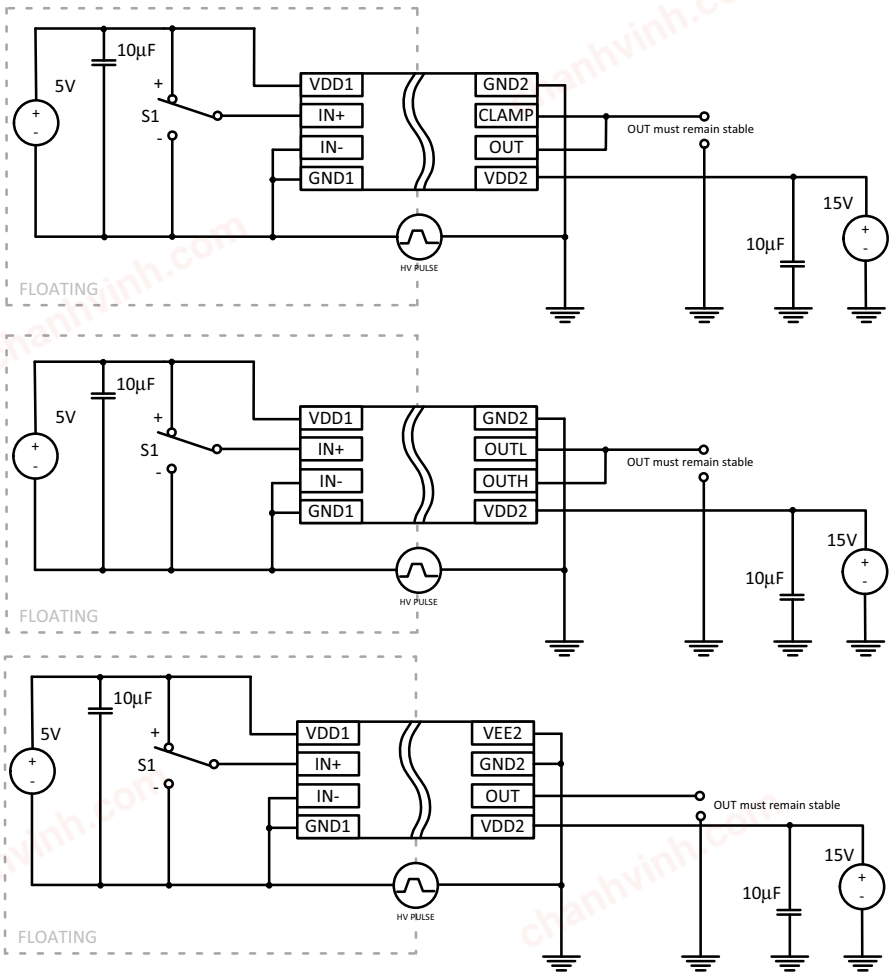


Figure 33. Common−Mode Transient Immunity Test Circuit

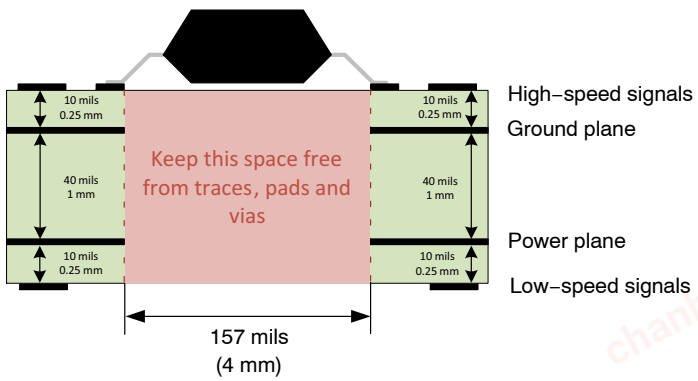


Figure 34. Recommended Layer Stack

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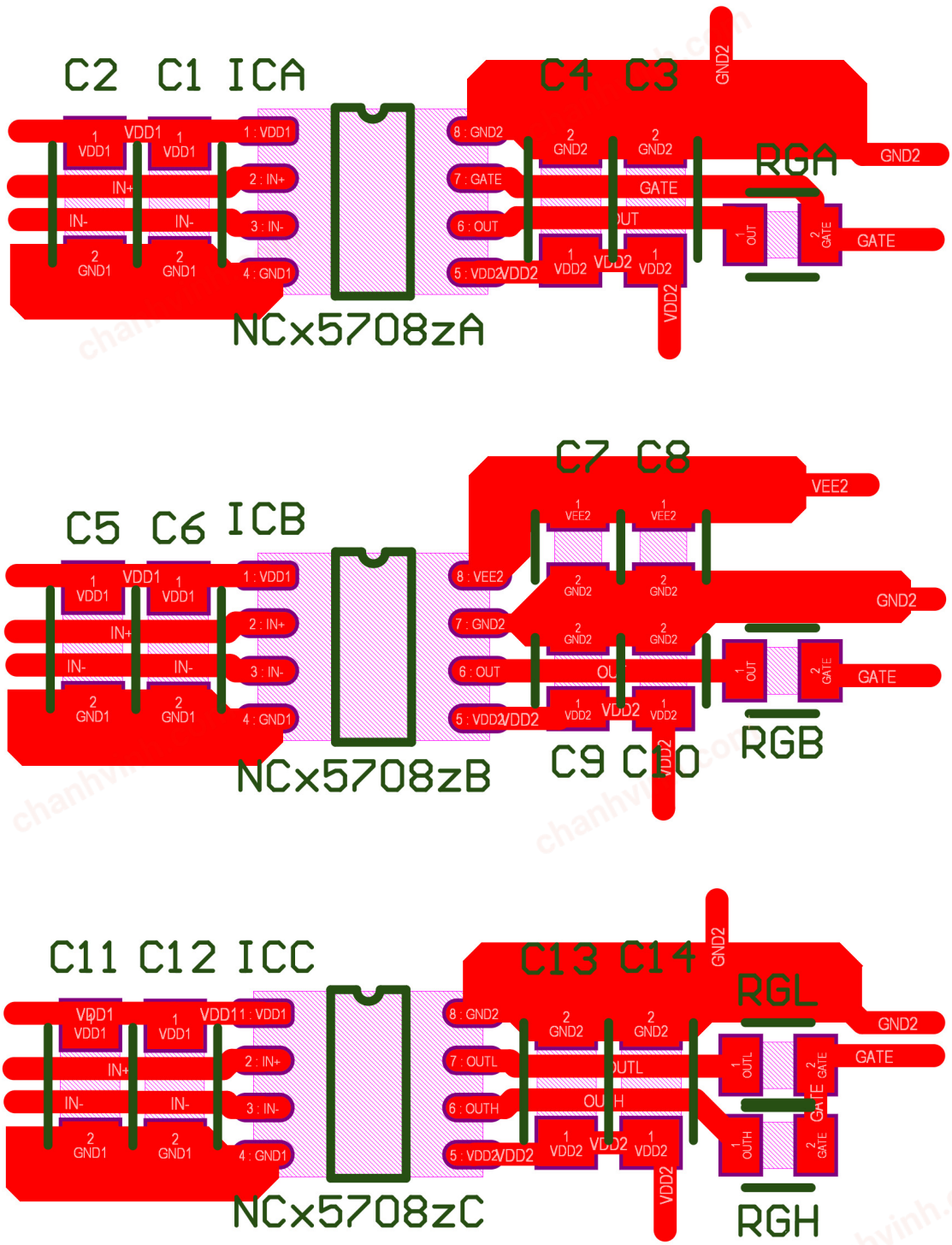


Figure 35. Recommended Layout for Version A/B/C

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ORDERING INFORMATION

Device	Qualification	Package	Shipping†
NCD57080ADR2G	Industrial	SOIC−8 Narrow Body (Pb−Free)	2500 / Tape & Reel
NCD57080BDR2G			
NCD57080CDR2G			
NCV57080ADR2G*	Automotive (AEC−Q100 Qualified and PPAP Capable)	SOIC−8 Narrow Body (Pb−Free)	2500 / Tape & Reel
NCV57080BDR2G*			
NCV57080CDR2G*			
NCD57081ADR2G	Industrial	SOIC−8 Narrow Body (Pb−Free)	2500 / Tape & Reel
NCD57081BDR2G			
NCD57081CDR2G			
NCV57081ADR2G*	Automotive (AEC−Q100 Qualified and PPAP Capable)	SOIC−8 Narrow Body (Pb−Free)	2500 / Tape & Reel
NCV57081BDR2G*			
NCV57081CDR2G*			

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

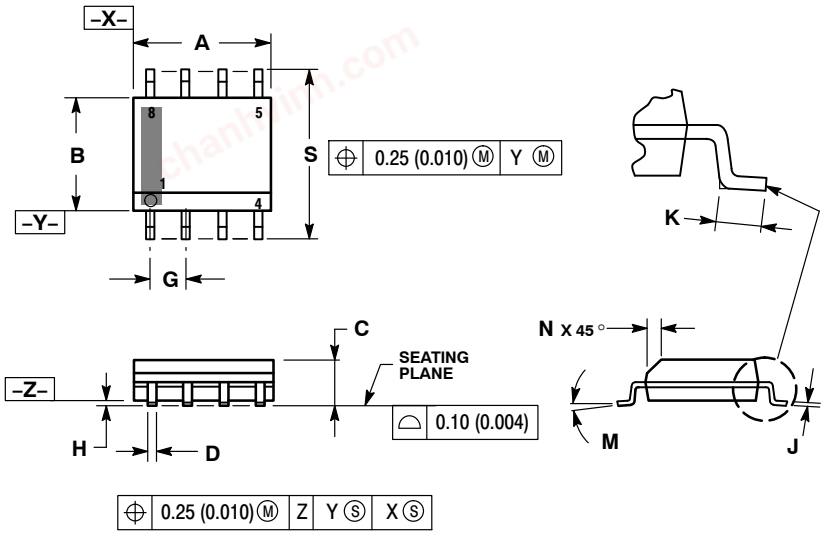
ON Semiconductor®



SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

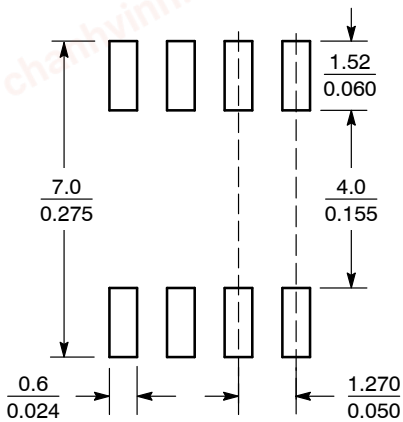
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

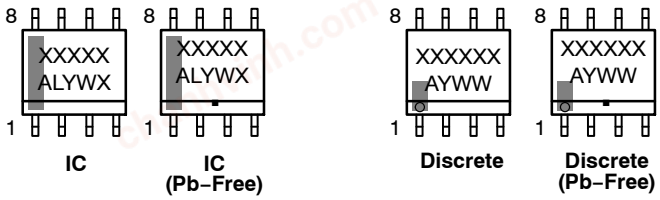
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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