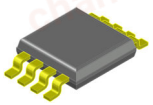
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DATA SHEET
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LDO Regulator, Low Noise (8 μV_{RMS}), ADJ/FIX

38 V, 150 mA

NCP731



MSOP8 EP 3x3
CASE 846AT

The NCP731 device is based on unique combination of features – very low noise, low quiescent current, fast transient response and high input and output voltage ranges. The NCP731 is CMOS LDO regulator designed for up to 38 V input voltage and 150 mA output current. Very low noise (8 μV_{RMS}) makes this device an ideal solution for application where clean voltage rails are critical for system performance (power operational amplifiers, analog–to–digital / digital–to–analog converters and other precision analog circuitry).

Internal short circuit and over temperature protections saves the device against overload conditions.

Features

- Operating Input Voltage Range: 2.7 V to 38 V
- Output Voltage Adjustable Range: 1.2 V to 35 V
- Fixed Output Voltage Versions: 3.3 V and 5.0 V (other voltage versions on request)
- Very Low Noise: 8 μV_{RMS} (10 Hz to 100 kHz)
- Low Quiescent Current: 48 µA typ.
- Low Shutdown Current: 100 nA typ.
- Low Dropout: 290 mV typ. at 150 mA
- Output Voltage Accuracy ±0.6% (25°C)
- Programmable Soft Start Circuit
- Stable with Small 1 µF Ceramic Capacitors
- Over–Current and Thermal Shutdown Protections
- Available in Micro–8 EP Package
- Device is Pb–Free and RoHS Compliant

Typical Applications

- Supply Rails for OpAmps, ADCs, DACs and other Precision Analog Circuitry and Audio
- Post DC–DC Converter Regulation and Ripple Filtering
- Test and Measurement
- Industrial Instrumentation
- Metering
- Battery Powered Devices

MARKING DIAGRAM



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code

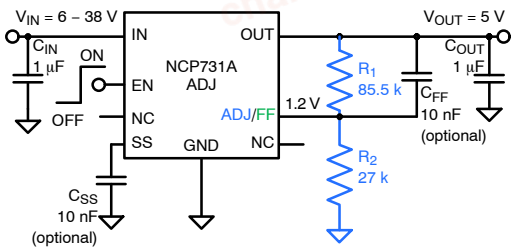


Figure 1. Adjustable Output Voltage Application

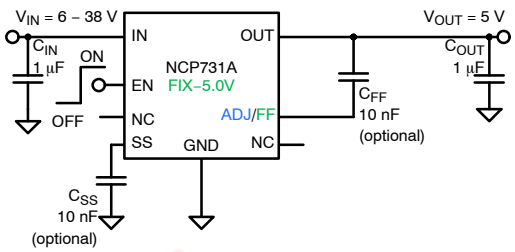


Figure 2. Fixed Output Voltage Application

Notes:
Blue objects are valid for ADJ version only
Green objects are valid for FIX version only
Black objects are common for all version

ORDERING INFORMATION

See detailed ordering and shipping information on page 16 of this data sheet.

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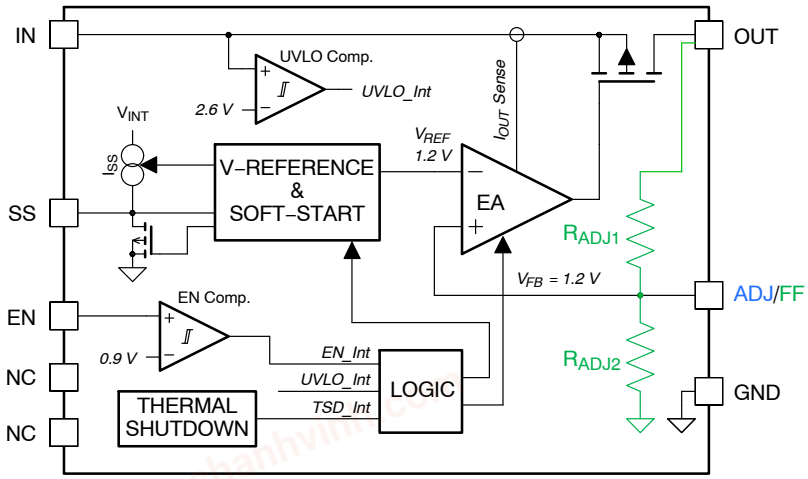


Figure 3. Internal Block Diagram

Notes:
Blue objects are valid for ADJ version only
Green objects are valid for FIX version only
The rest valid for both versions

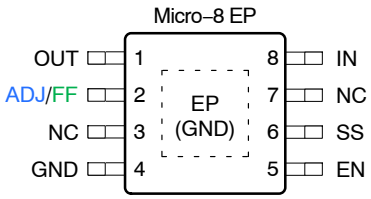


Figure 4. Pin Assignments

PIN DESCRIPTION

Pin Number	Pin Name	Description
8	IN	Power supply input pin.
4	GND	Ground pin.
1	OUT	LDO output pin.
5	EN	Enable input pin (high = enable, low = disable). If this pin is not needed it should be conned to IN pin. No internal pull–up or pull–down circuit is present.
2	ADJ/FF	ADJ version – pin is ADJ • Adjust input pin. Could be connected directly or by the resistor divider to the output pin. FIX versions – pin is FF • Feed forward capacitor pin. Could be connected by C_{FF} capacitor to OUT pin for better dynamic performance & lower noise or left unconnected.
3, 7	NC	Not internally connected. Could be left unconnected or connected to GND.
6	SS	Soft–start input pin. Connect a C_{SS} capacitor to set soft–start time. Could be left floating if not used.
EP	EPAD	Exposed pad, must be connected to GND.

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Table 1. MAXIMUM RATINGS

Rating		Symbol	Value	Unit
IN Voltage (Note 1)		V_{IN}	−0.3 to 40	V
OUT Voltage	ADJ Version and FIX Versions with $V_{OUT-NOM}$ > 6.0 V	V_{OUT}	−0.3 to [(V_{IN} + 0.3) or 40; whichever is lower]	V
	FIX Versions with $V_{OUT-NOM} \leq$ 6.0 V		−0.3 to [(V_{IN} + 0.3) or 7; whichever is lower]	
EN Voltage		V_{EN}	−0.3 to (V_{IN} + 0.3)	V
ADJ/FF Voltage		V_{ADJ}	−0.3 to 5.5	V
SS Voltage		V_{SS}	−0.3 to 5.5	V
Output Current		I_{OUT}	Internally limited	mA
Maximum Junction Temperature		$T_{J(MAX)}$	150	°C
Storage Temperature		T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)		ESD_{HBM}	2000	V
ESD Capability, Charged Device Model (Note 2)		ESD_{CDM}	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per ANSI/ESDA/JEDEC JS−001, EIA/JESD22−A114
   ESD Charged Device Model tested per ANSI/ESDA/JEDEC JS−002, EIA/JESD22−C101

Table 2. THERMAL CHARACTERISTICS (Note 3)

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	44	°C/W
Thermal Resistance, Junction−to−Case (top)	$R_{\theta JCt}$	99	°C/W
Thermal Resistance, Junction−to−Case (bottom)	$R_{\theta JCb}$	19	°C/W
Thermal Characterization Parameter, Junction−to−Case (top)	Ψ_{JCt}	12	°C/W
Thermal Characterization Parameter, Junction−to−Board [FEM]	Ψ_{JB}	16	°C/W

3. Measured according to JEDEC board specification (board 2S2P, Cu layer thickness 1 oz, Cu area 645mm^2, no airflow). Detailed description of the board can be found in JESD51−7.

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Table 3. ELECTRICAL CHARACTERISTICS $V_{IN} = V_{OUT-NOM} + 1$ V and $V_{IN} \geq 2.7$ V, $V_{EN} = 1.2$ V, $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 1.0$ µF (Note 4), $C_{SS} = 0$ nF, $C_{FF} = 0$ nF, $T_J = -40°C$ to 125°C, ADJ tied to OUT, unless otherwise specified.

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Recommended Input Voltage			V_{IN}	2.7	–	38	V
Output Voltage Accuracy (Note 5)	T_J = +25°C		V_{OUT}	−0.6	–	0.6	%
	$V_{IN} = V_{OUT-NOM}$ + 1 V to 38 V I_{OUT} = 0.1 mA to 150 mA T_J = −40°C to +85°C			−1.0	–	1.0	
	$V_{IN} = V_{OUT-NOM}$ + 1 V to 38 V I_{OUT} = 0.1 mA to 150 mA T_J = −40°C to +125°C			−1.5	–	1.5	
Output Voltage Range (Note 6)			$V_{OUT-ADJ}$	V_{ADJ}	–	35	V
ADJ Reference Voltage (Note 6)			V_{ADJ}	–	1.2	–	V
ADJ Input Current (Note 6)	V_{ADJ} = 1.2 V		I_{ADJ}	−0.05	0.01	0.05	µA
Quiescent Current	$V_{IN} = V_{OUT-NOM}$ + 1 V to 38 V, I_{OUT} = 0 mA		I_Q	–	48	100	µA
Ground Current	I_{OUT} = 150 mA		I_{GND}	–	400	–	µA
Shutdown Current	V_{EN} = 0 V, V_{IN} = 38 V		I_{SHDN}	–	0.07	1.0	µA
Output Current Limit	$V_{OUT} = V_{OUT-NOM}$ − 100 mV		I_{OLIM}	210	295	450	mA
Short Circuit Current	V_{OUT} = 0 V		I_{OSC}	210	365	450	mA
Dropout Voltage (Note 7)	I_{OUT} = 150 mA		V_{DO}	–	230	480	mV
Power Supply Ripple Rejection	$V_{IN} = V_{OUT-NOM}$ + 2 V I_{OUT} = 10 mA	10 Hz	PSRR	–	80	–	dB
		10 kHz		–	70	–	
		100 kHz		–	42	–	
		1 MHz		–	48	–	
Output Noise Voltage	f = 10 Hz to 100 kHz, ADJ version, $V_{OUT} = V_{ADJ}$		V_N	–	8.1	–	µVRMS
	f = 10 Hz to 100 kHz, ADJ version, V_{OUT} = 3.3 V, C_{FF} = 10 nF, R_1 = 47.3 kΩ, R_2 = 27 kΩ		V_N	–	15	–	
	f = 10 Hz to 100 kHz, ADJ version, V_{OUT} = 5 V, C_{FF} = 10 nF, R_1 = 85.5 kΩ, R_2 = 27 kΩ		V_N	–	20	–	
EN Threshold	V_{EN} rising		V_{EN-TH}	0.7	0.9	1.1	V
EN Hysteresis	V_{EN} falling		V_{EN-HY}	0.02	0.1	0.2	V
EN Input Current	V_{EN} = 30 V, V_{IN} = 30 V		I_{EN}	−1	0.15	1	µA
Internal UVLO Threshold	V_{IN} voltage rising		$V_{UVLO-TH}$	2.43	2.55	2.69	V
Internal UVLO Hysteresis	V_{IN} voltage falling		$V_{UVLO-HY}$	0.01	0.04	0.07	V
SS Charging Current	V_{SS} = 0 V		I_{SS}	–	910	–	nA
SS High Voltage	SS pin floating		V_{SS-HI}	–	2.4	–	V
SS Time (Note 8)	C_{SS} = 10 nF		$t_{SS-10nF}$	–	14	–	ms
	C_{SS} not connected		t_{SS-0nF}	–	0.5	–	
Thermal Shutdown Temperature	Temperature rising from T_J = +25°C		T_{TSD}	–	170	–	°C
Thermal Shutdown Hysteresis	Temperature falling from TSD		T_{TSDH}	–	10	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Effective capacitance, including the effect of DC bias, tolerance and temperature. See the Application Information section for more information.
5. Output voltage accuracy of ADJ version is guaranteed when ADJ pin is connected to OUT pin. The $V_{OUT-NOM}$ is then equal to V_{ADJ}.
6. Applicable only to ADJ version.
7. Dropout voltage is measured when the output voltage falls 100 mV below the nominal output voltage. ADJ version is measured with ADJ pin connected to resistor divider which sets V_{OUT} to 5.0 V. Limits are valid for all voltage versions.
8. Startup time is the time from EN assertion to point when output voltage is equal to 95% of $V_{OUT-NOM}$.

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TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM}$ + 1 V and $V_{IN} \geq 2.7$ V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 1.0 μF (effective), C_{SS} = 10 nF, C_{FF} = 10 nF, R_{ADJ1} = 85.5 kΩ, R_{ADJ2} = 27 kΩ (R_{ADJx} applicable to ADJ application only), T_J = −40°C to 125°C, all output voltage versions, unless otherwise specified.

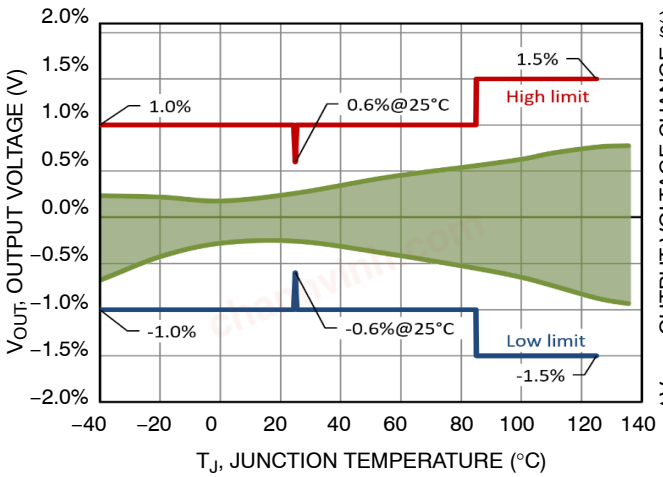


Figure 5. Output Voltage vs. Temperature

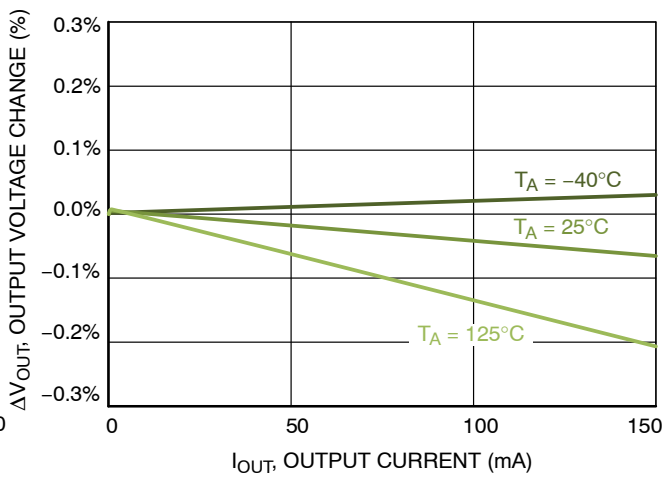


Figure 6. Load Regulations

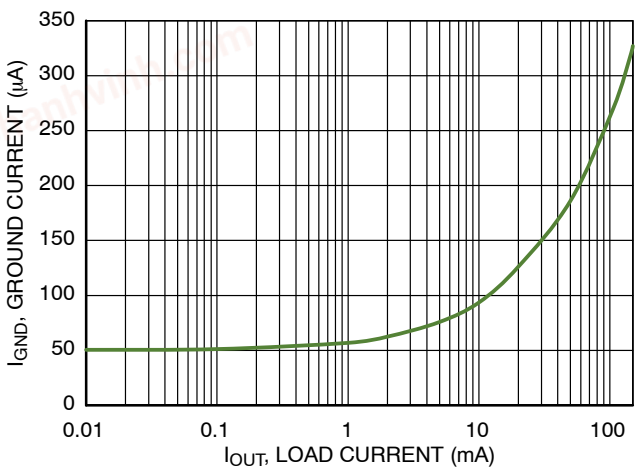


Figure 7. Ground Current vs. Load

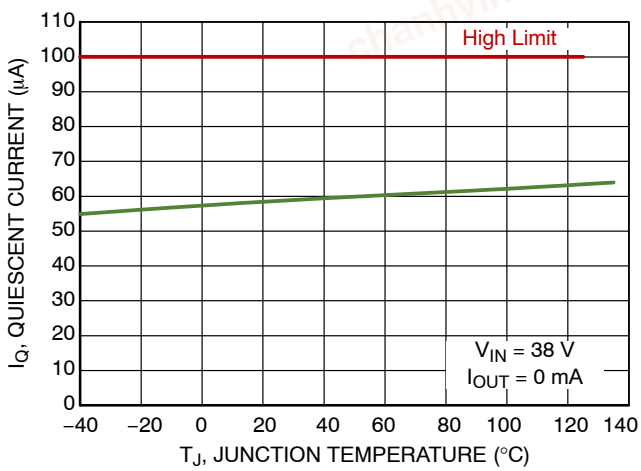


Figure 8. Quiescent Current vs. Temperature

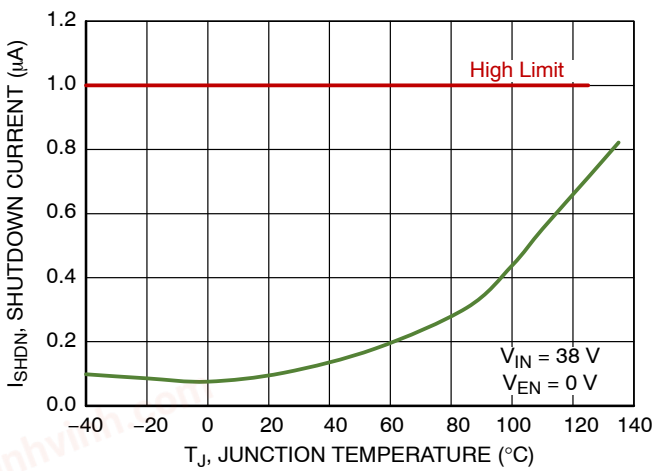


Figure 9. Shutdown Current vs. Temperature

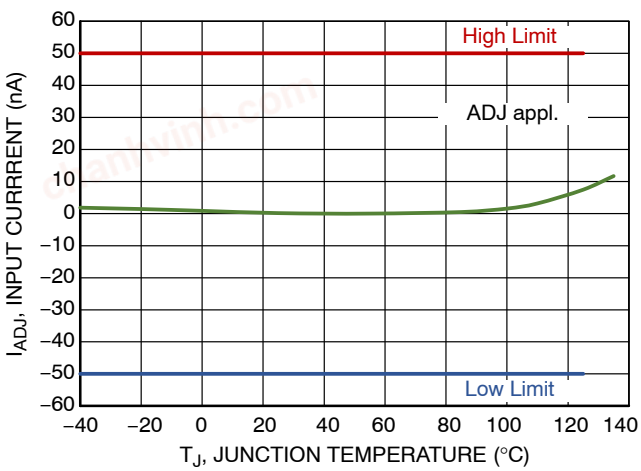


Figure 10. ADJ Input Current vs. Temperature

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TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 1 V and V_{IN} ≥ 2.7 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF (effective), C_{SS} = 10 nF, C_{FF} = 10 nF, R_{ADJ1} = 85.5 kΩ, R_{ADJ2} = 27 kΩ (R_{ADJx} applicable to ADJ application only), T_J = −40°C to 125°C, all output voltage versions, unless otherwise specified.

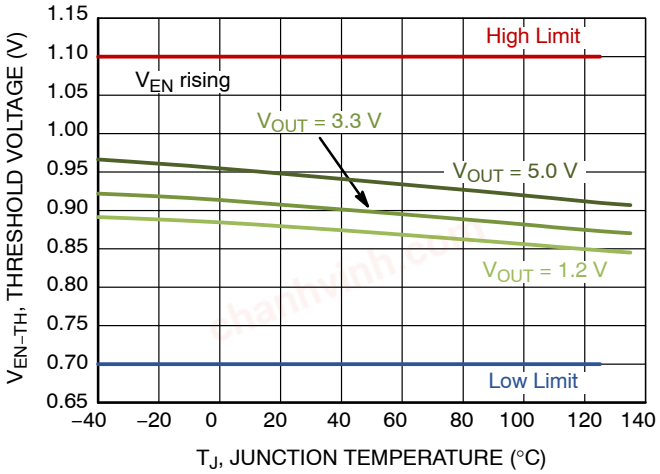


Figure 11. Enable Threshold Voltage vs. Temperature

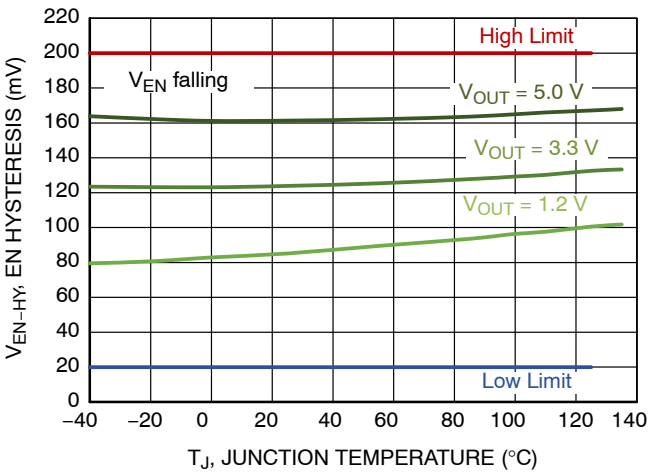


Figure 12. Enable Hysteresis vs. Temperature

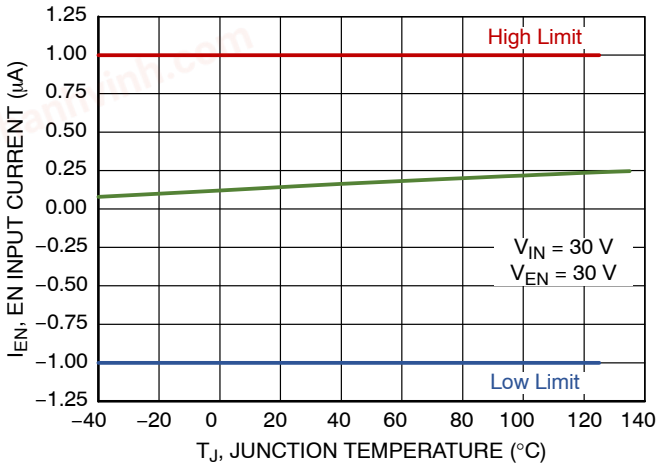


Figure 13. Enable Input Current vs. Temperature

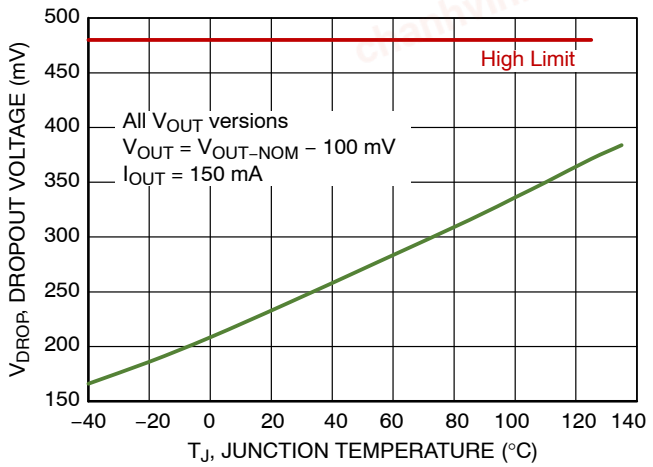


Figure 14. Dropout Voltage vs. Temperature

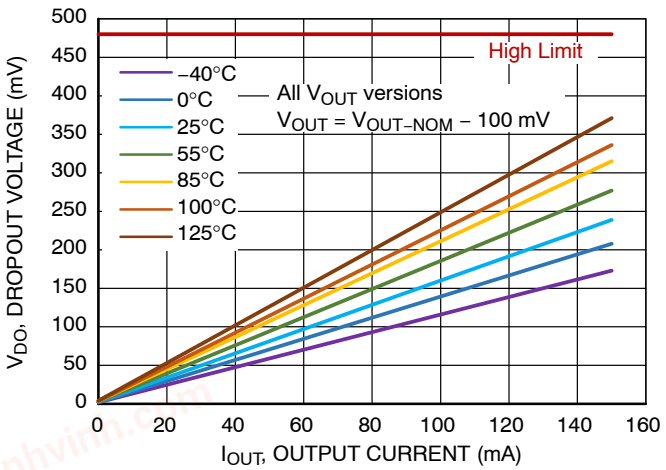


Figure 15. Dropout Voltage vs. I_{OUT}

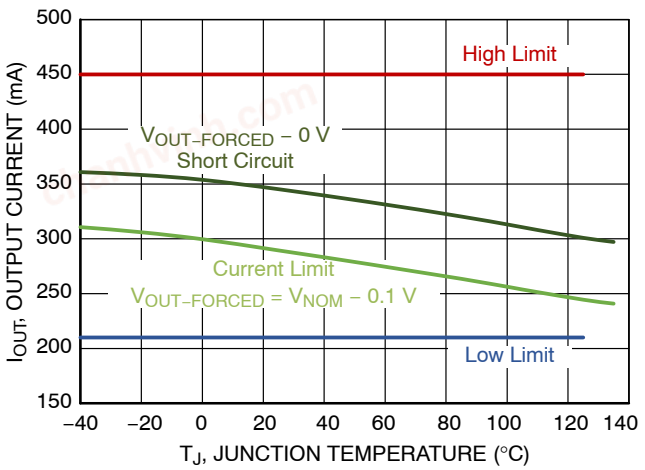


Figure 16. Maximum Output Current vs. Temperature

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TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 1 V and V_{IN} ≥ 2.7 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF (effective), C_{SS} = 10 nF, C_{FF} = 10 nF, R_{ADJ1} = 85.5 kΩ, R_{ADJ2} = 27 kΩ (R_{ADJx} applicable to ADJ application only), T_J = −40°C to 125°C, all output voltage versions, unless otherwise specified.

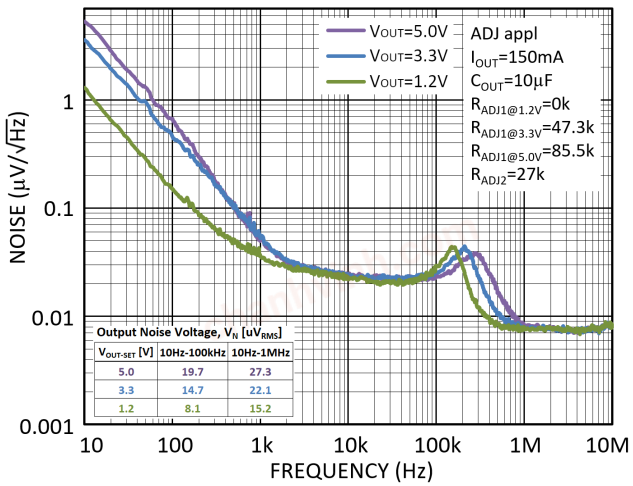


Figure 17. V_{OUT} Noise Density vs. V_{OUT}

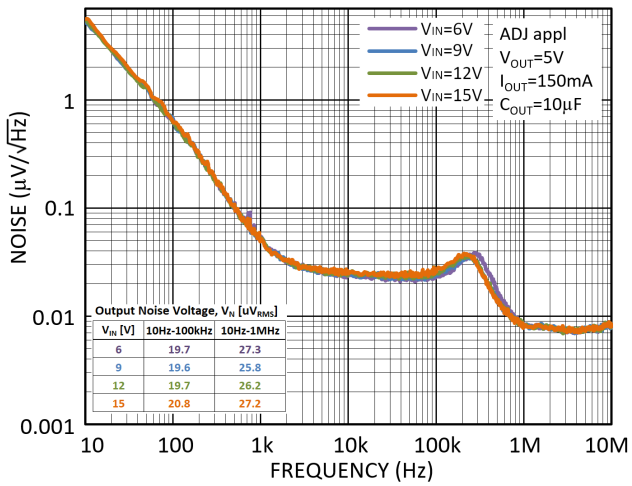


Figure 18. V_{OUT} Noise Density vs. V_{IN}

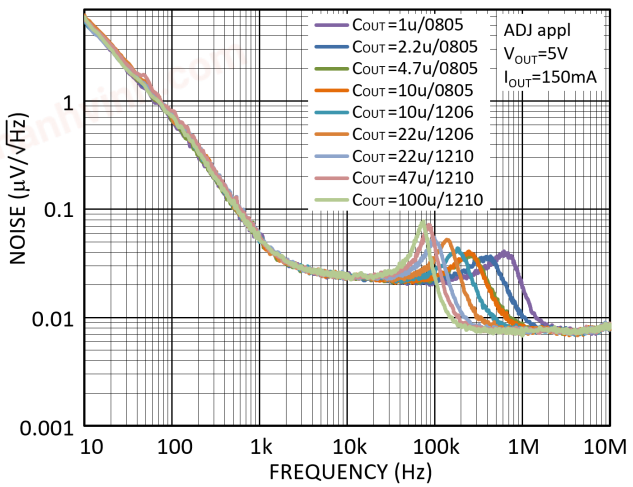


Figure 19. V_{OUT} Noise Density vs. C_{OUT}

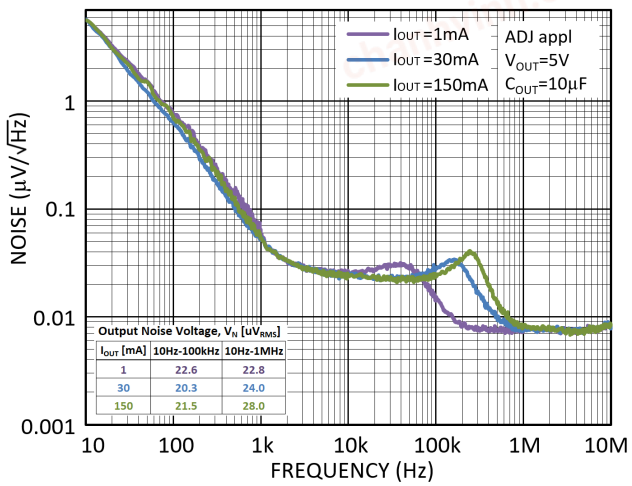


Figure 20. V_{OUT} Noise Density vs. I_{OUT}

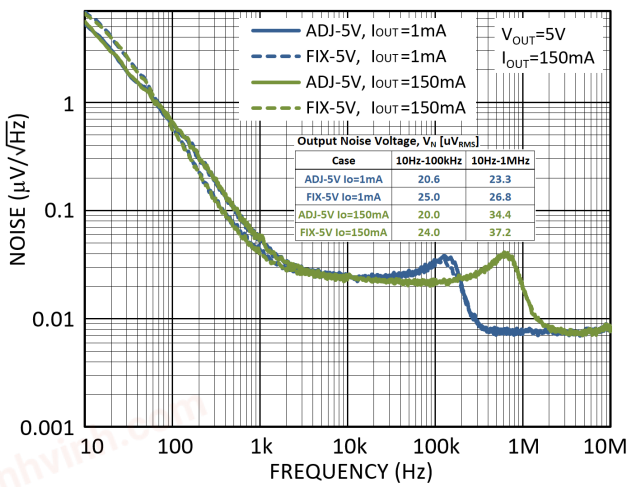


Figure 21. V_{OUT} Noise Density vs. Part−type and I_{OUT}

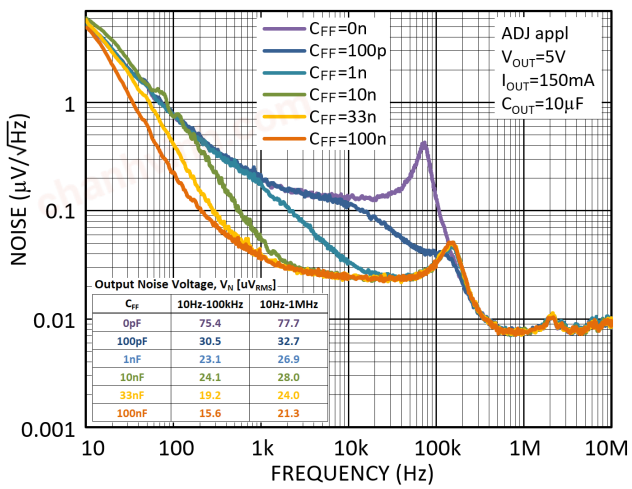


Figure 22. V_{OUT} Noise Density vs. C_{FF}

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TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 1 V and V_{IN} ≥ 2.7 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF (effective), C_{SS} = 10 nF, C_{FF} = 10 nF, R_{ADJ1} = 85.5 kΩ, R_{ADJ2} = 27 kΩ (R_{ADJx} applicable to ADJ application only), T_J = −40°C to 125°C, all output voltage versions, unless otherwise specified.

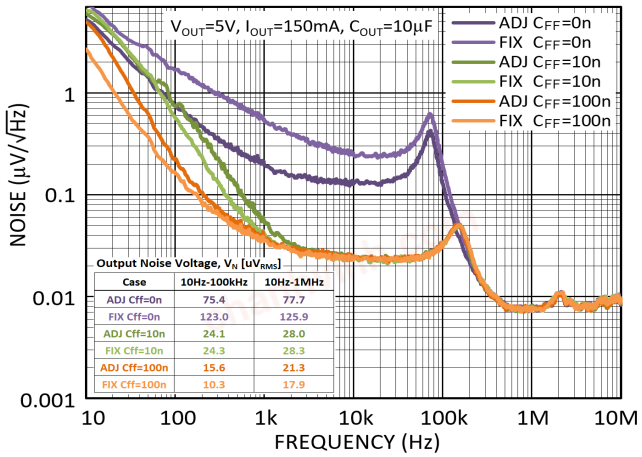


Figure 23. V_{OUT} Noise Density vs. Part−type and C_{FF}

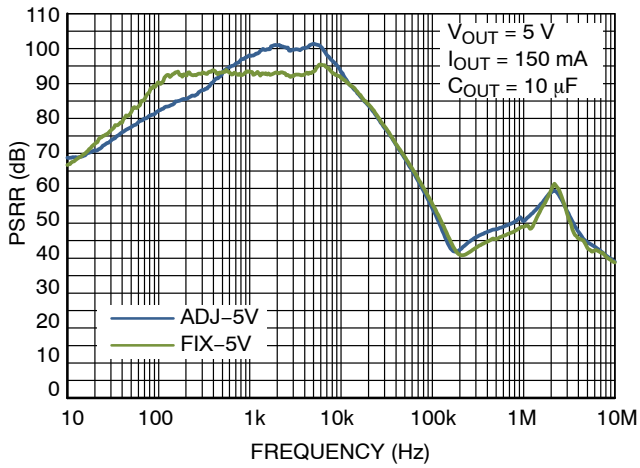


Figure 24. PSRR vs. Part−type

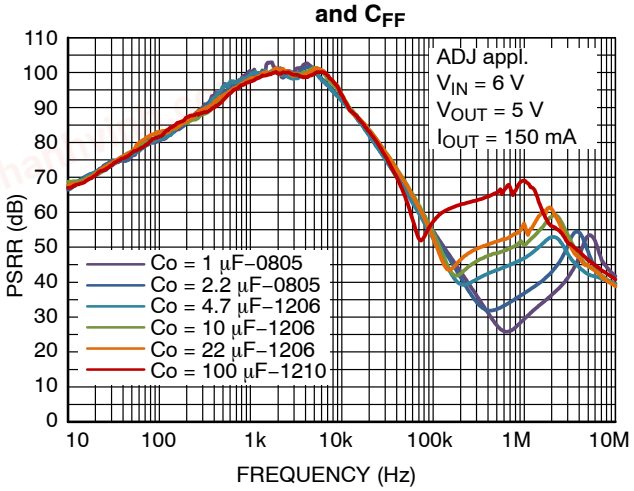


Figure 25. PSRR vs. C_{OUT} (6.0 V, 150 mA)

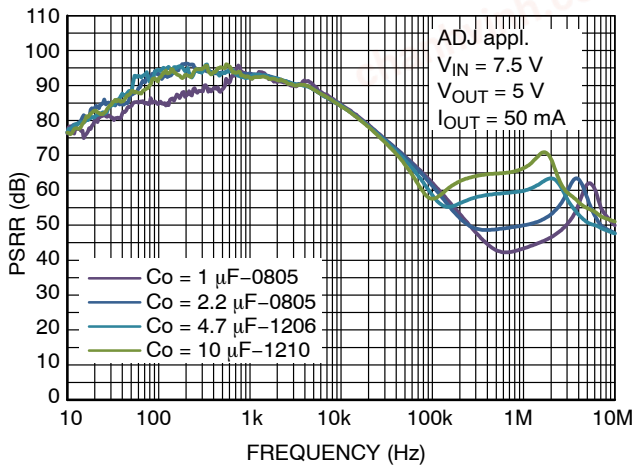


Figure 26. PSRR vs. C_{OUT} (7.5 V, 50 mA)

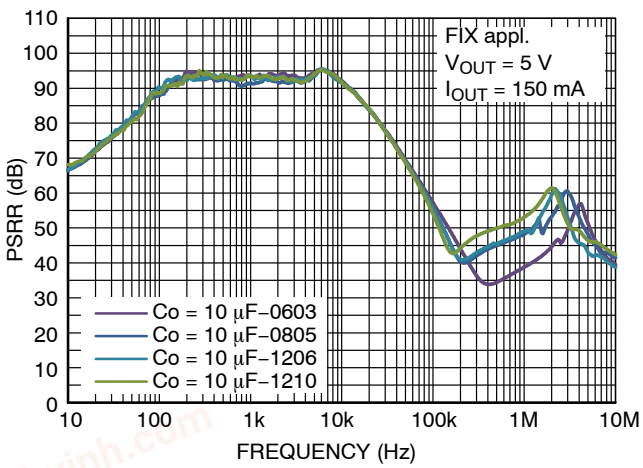


Figure 27. PSRR vs. C_{OUT} Package Size

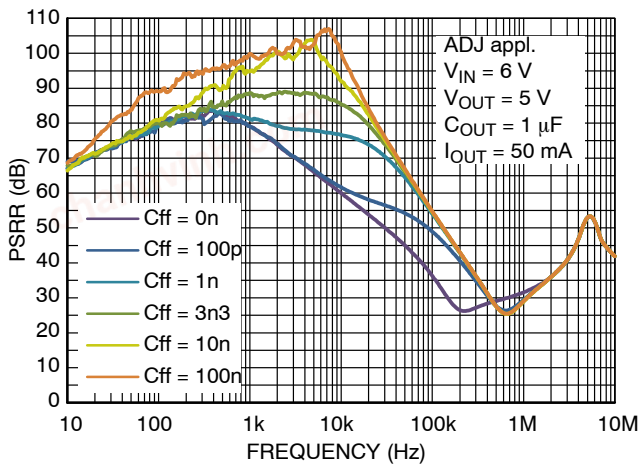


Figure 28. PSRR vs. C_{FF}

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TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 1 V and V_{IN} ≥ 2.7 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF (effective), C_{SS} = 10 nF, C_{FF} = 10 nF, R_{ADJ1} = 85.5 kΩ, R_{ADJ2} = 27 kΩ (R_{ADJx} applicable to ADJ application only), T_J = −40°C to 125°C, all output voltage versions, unless otherwise specified.

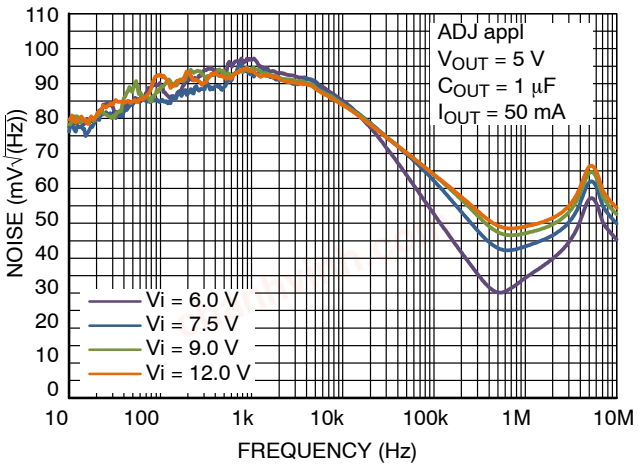


Figure 29. PSRR vs. V_{IN} (50 mA, 1 μF)

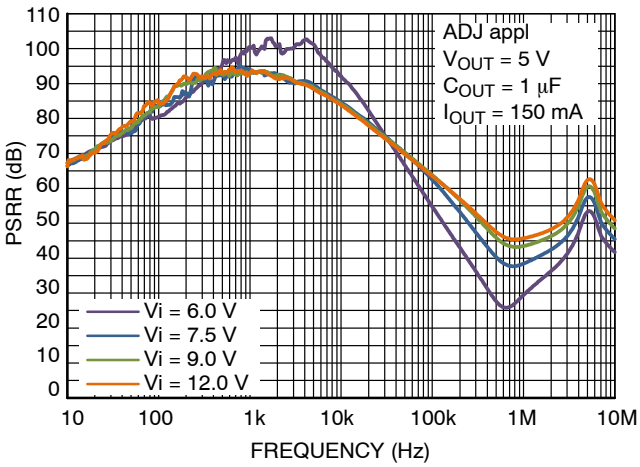


Figure 30. PSRR vs. V_{IN} (150 mA, 1 μF)

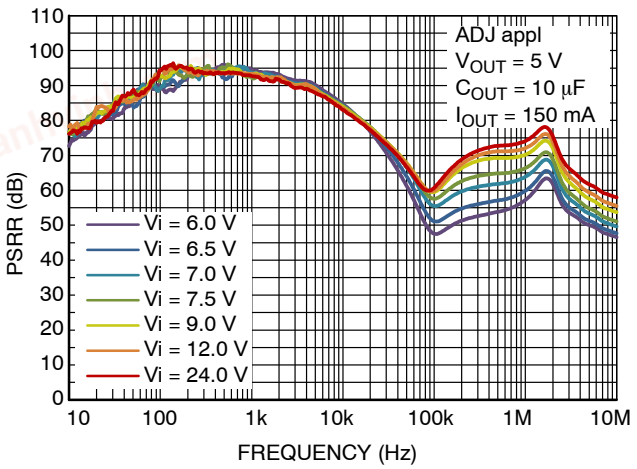


Figure 31. PSRR vs. V_{IN} (50 mA, 10 μF)

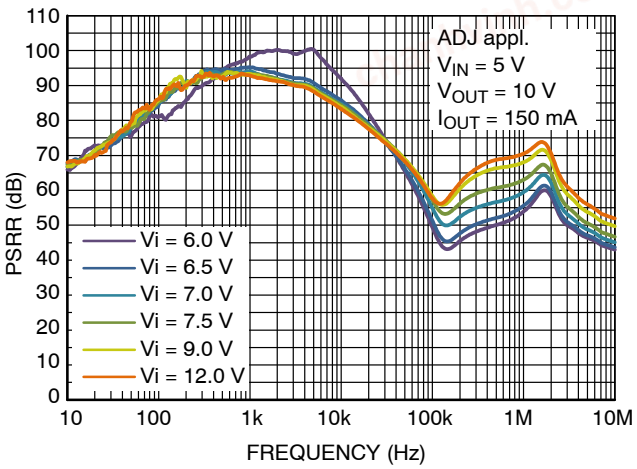


Figure 32. PSRR vs. V_{IN} (150 mA, 10 μF)

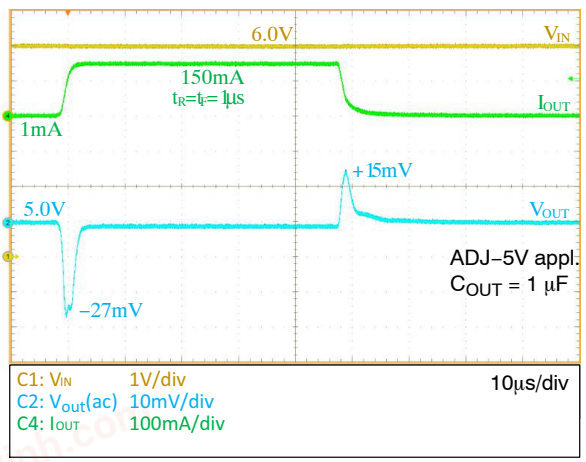


Figure 33. Load Transient Response (ADJ−5V, V_{IN} = 6.0 V, C_{OUT} = 1 μF)

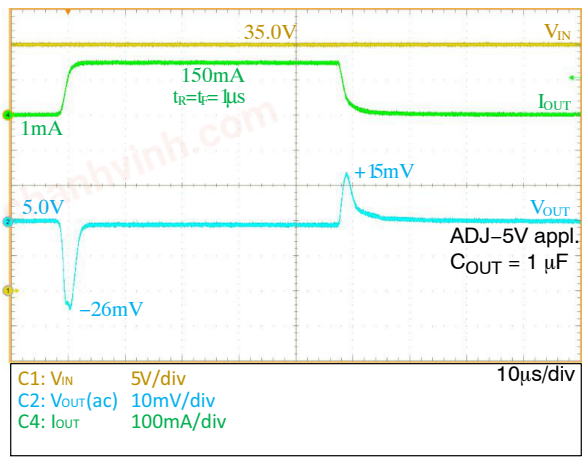


Figure 34. Load Transient Response (ADJ−5V, V_{IN} = 35.0 V, C_{OUT} = 1 μF)

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TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM}$ + 1 V and $V_{IN} \geq$ 2.7 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 1.0 μF (effective), C_{SS} = 10 nF, C_{FF} = 10 nF, R_{ADJ1} = 85.5 kΩ, R_{ADJ2} = 27 kΩ (R_{ADJx} applicable to ADJ application only), T_J = −40°C to 125°C, all output voltage versions, unless otherwise specified.

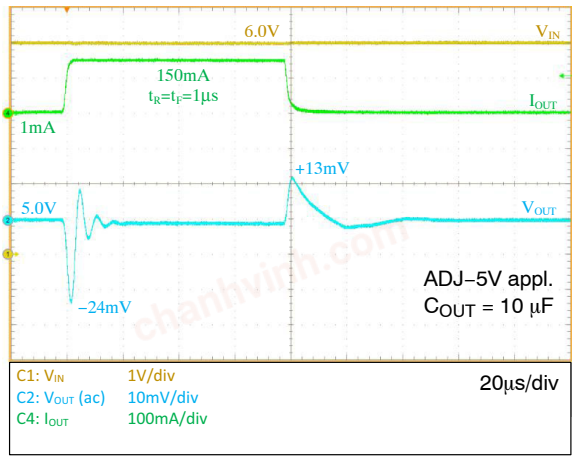


Figure 35. Load Transient Response (ADJ−5V, V_{IN} = 6.0 V, C_{OUT} = 10 μF)

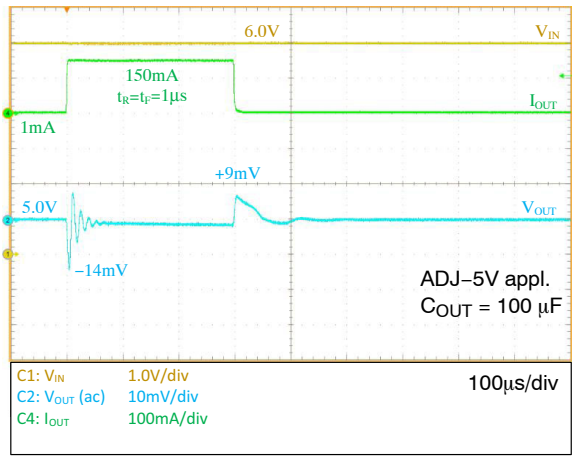


Figure 36. Load Transient Response (ADJ−5V, V_{IN} = 6.0 V, C_{OUT} = 100 μF)

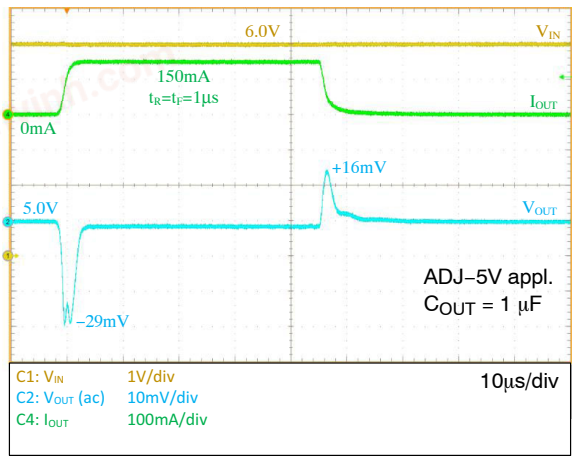


Figure 37. Load Transient Response (V_{IN} = 6.0 V, I_{OUT} = 0 − 150 mA)

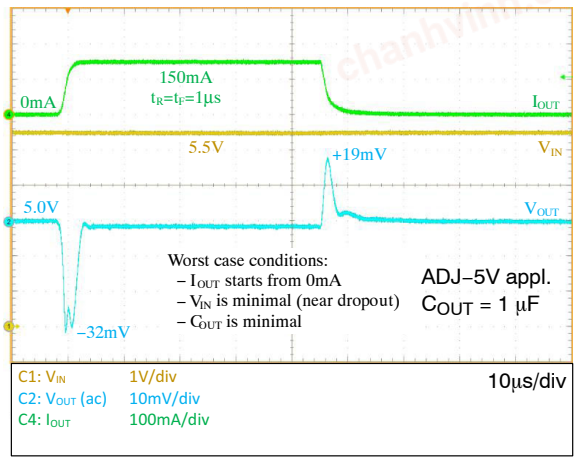


Figure 38. Load Trans. Response (V_{IN} = 5.5 V, I_{OUT} = 0 − 150 mA ~ Worst Conditions)

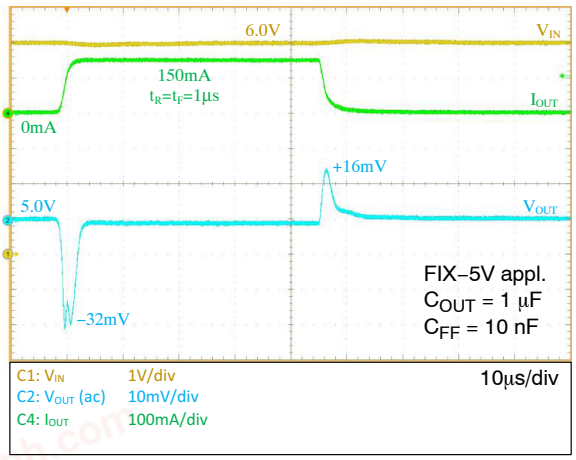


Figure 39. Load Transient Response (FIX−5V, V_{IN} = 6.0 V, C_{OUT} = 1 μF)

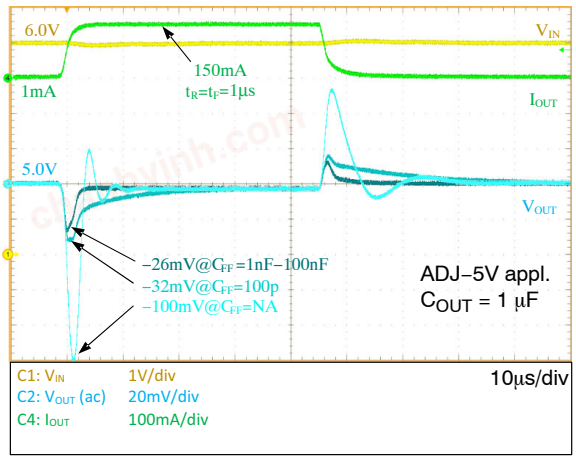


Figure 40. Load Transient Response (ADJ−5V, C_{FF} = variable)

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TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM}$ + 1 V and $V_{IN} \geq 2.7$ V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 1.0 μF (effective), C_{SS} = 10 nF, C_{FF} = 10 nF, R_{ADJ1} = 85.5 kΩ, R_{ADJ2} = 27 kΩ (R_{ADJx} applicable to ADJ application only), T_J = −40°C to 125°C, all output voltage versions, unless otherwise specified.

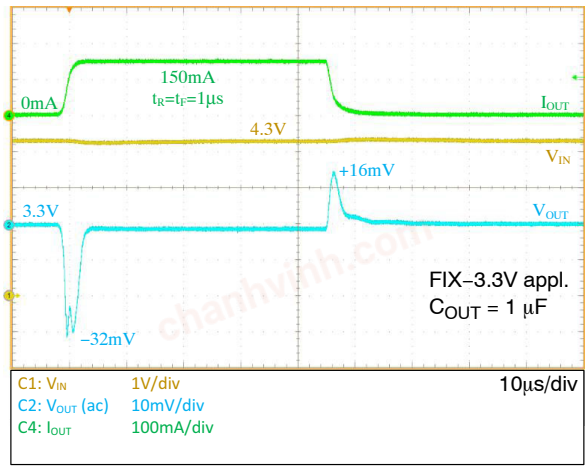


Figure 41. Load Transient Response (FIX−3.3V, V_{IN} = 4.3 V, C_{OUT} = 1 μF)

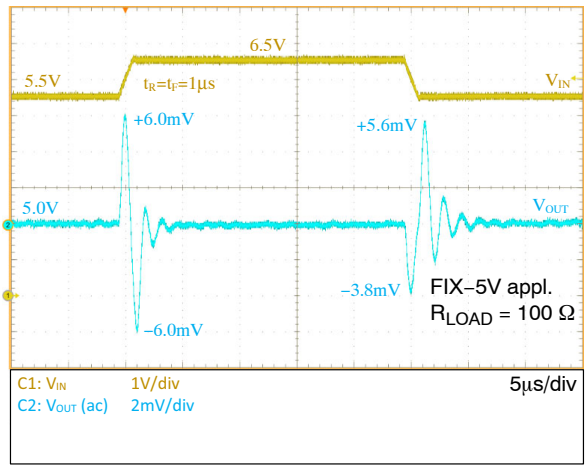


Figure 42. Line Transient Response (V_{OUT} = 5.0 V, V_{IN} = 5.5 – 6.5 V)

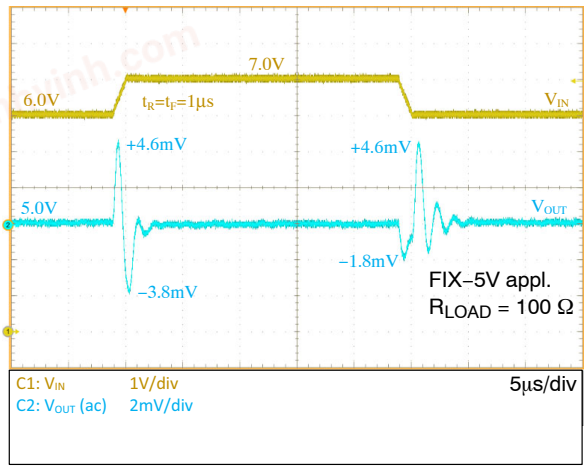


Figure 43. Line Transient Response (V_{OUT} = 5.0 V, V_{IN} = 6.0 – 7.0 V)

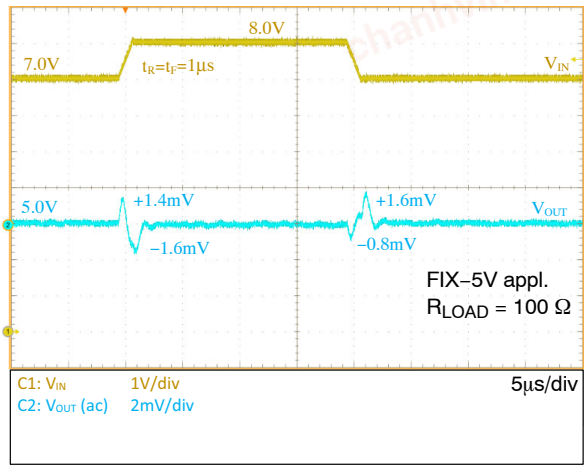


Figure 44. Line Transient Response (V_{OUT} = 5.0 V, V_{IN} = 7.0 – 8.0 V)

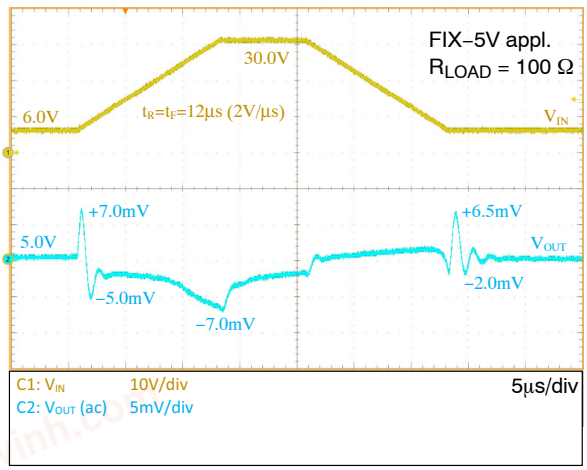


Figure 45. Line Transient Response (V_{OUT} = 5.0 V, V_{IN} = 6.0 – 30.0 V)

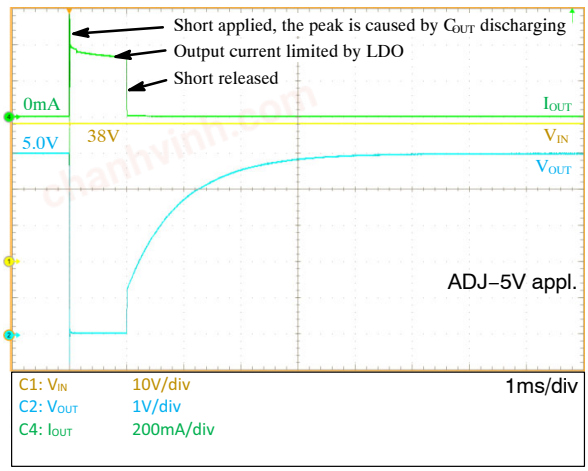


Figure 46. Short Circuit (1 ms)

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TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 1 V and $V_{IN} \geq$ 2.7 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF (effective), C_{SS} = 10 nF, C_{FF} = 10 nF, R_{ADJ1} = 85.5 kΩ, R_{ADJ2} = 27 kΩ (R_{ADJx} applicable to ADJ application only), T_J = −40°C to 125°C, all output voltage versions, unless otherwise specified.

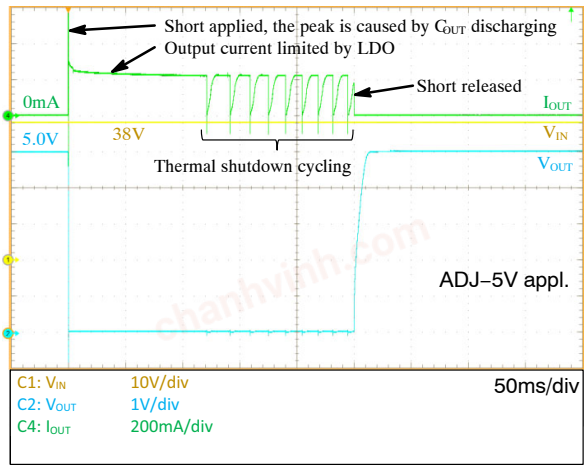


Figure 47. Short Circuit (250 ms)

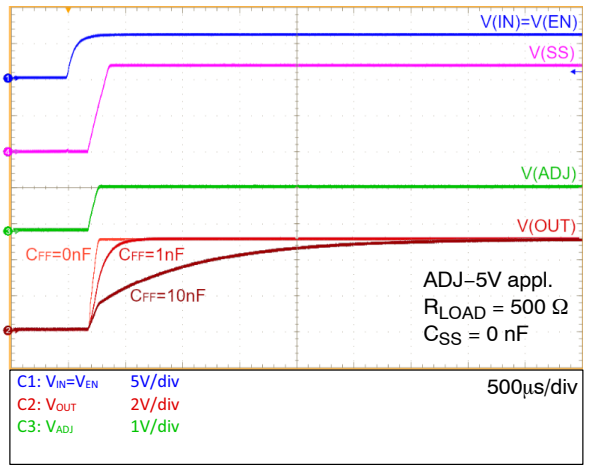


Figure 48. Startup by V_{IN} (ADJ−5V, C_{SS} = 0 nF)

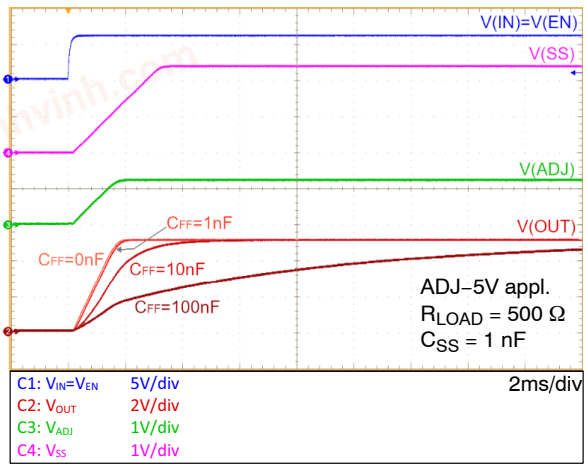


Figure 49. Startup by V_{IN} (ADJ−5V, C_{SS} = 1 nF)

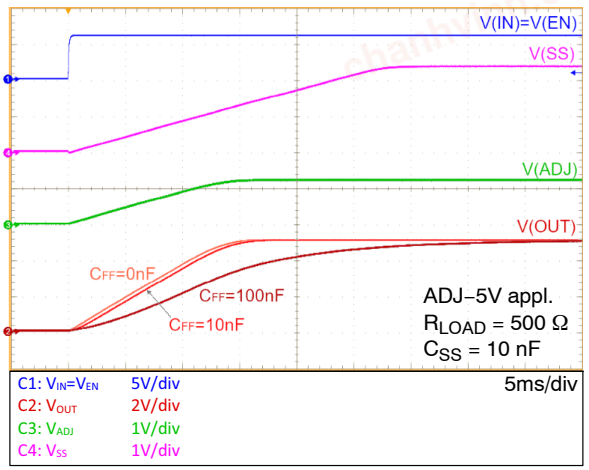


Figure 50. Startup by V_{IN} (ADJ−5V, C_{SS} = 10 nF)

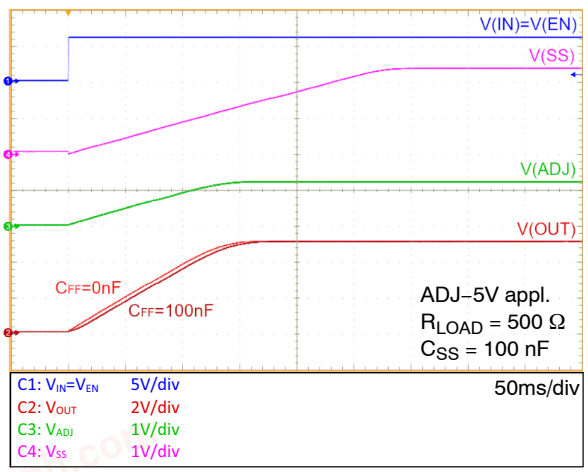


Figure 51. Startup by V_{IN} (ADJ−5V, C_{SS} = 100 nF)

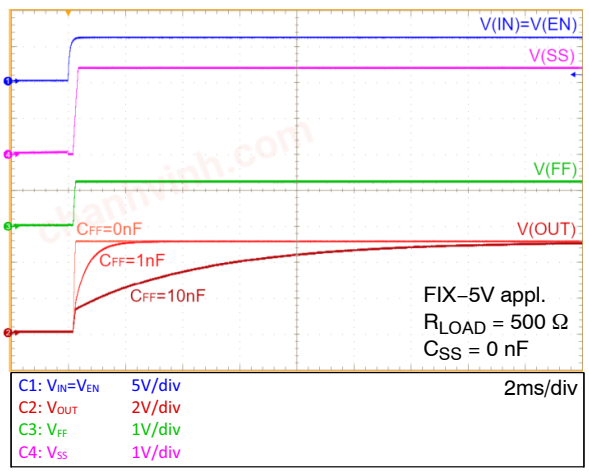


Figure 52. Startup by V_{IN} (FIX−5 V, C_{SS} = 0 nF)

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TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM}$ + 1 V and $V_{IN} \geq$ 2.7 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 1.0 μF (effective), C_{SS} = 10 nF, C_{FF} = 10 nF, R_{ADJ1} = 85.5 kΩ, R_{ADJ2} = 27 kΩ (R_{ADJx} applicable to ADJ application only), T_J = −40°C to 125°C, all output voltage versions, unless otherwise specified.

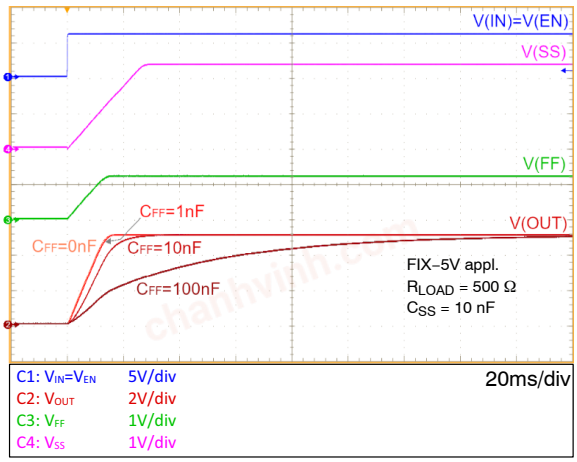


Figure 53. Startup by V_{IN} (FIX−5V, C_{SS} = 10 nF)

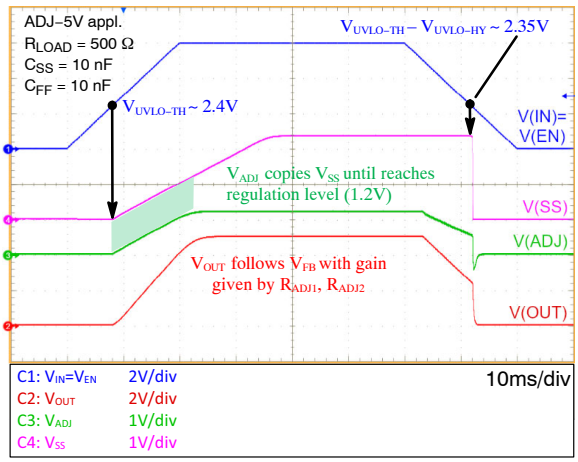


Figure 54. Startup/Shutdown by V_{IN} (Slow Rising Edge)

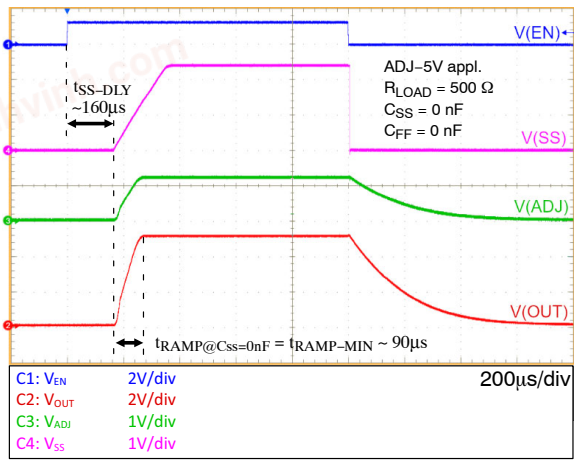


Figure 55. Startup/Shutdown by V_{EN} (Fast Rising Edge)

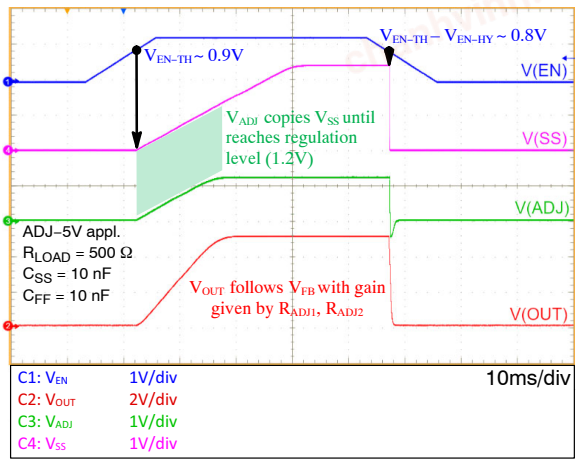


Figure 56. Startup/Shutdown by V_{EN} (Slow Rising Edge)

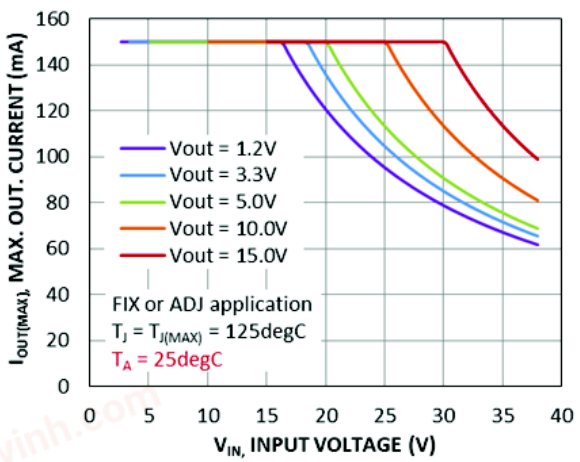


Figure 57. Max. Allowable Output Current vs. V_{IN}, FIX & ADJ Applications, T_A = 25°C

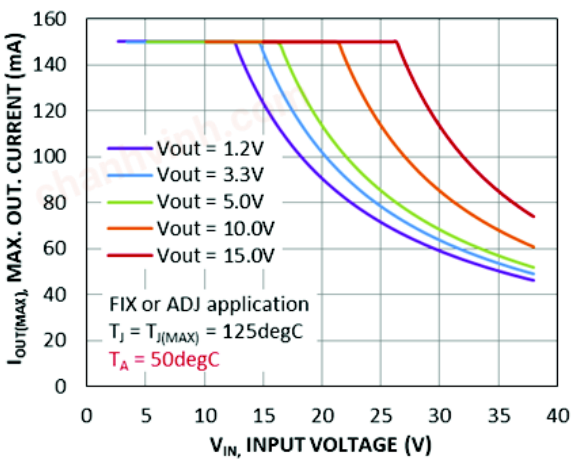


Figure 58. Max. Allowable Output Current vs. V_{IN}, FIX & ADJ Applications, T_A = 50°C

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APPLICATIONS INFORMATION

Input Capacitor Selection (C_{IN})

Input capacitor connected as close as possible is necessary for device stability. The value of the input capacitor should be at least 1 μF. Maximum value is not limited and the higher means better, because it filters unwanted input voltage AC component modulated onto the input DC voltage and provides energy to charge output capacitor in case of load transient. There is no requirement for the ESR of the input capacitor but it is recommended to use ceramic type (X5R, X7R etc.) for its low ESR and ESL. In cases when LDO's input power supply has a poor load transient response or it has high output impedance (ex: long connection wires) then the input capacitor needs to be significantly bigger (in range of tens of μF) to avoid of LDO's input voltage drop below the minimum level, given by the sum of output voltage and dropout voltage, otherwise the output voltage drop could happen.

Output Capacitor Selection (C_{OUT})

The LDO requires the output capacitor connected as close as possible to the output and ground pins. The LDO is designed to remain stable with output capacitor's effective capacitance in range from 1 μF to 1000 μF and ESR from 1 mΩ to 50 mΩ. The ceramic X5R, X7R or better type is recommended due to its low capacitance variations over the specified temperature range and low ESR. When selecting the output capacitor, the value deviation caused by temperature and DC bias voltage needs to be considered. Especially for small package size capacitors below 0805 the effective capacitance drops rapidly with the applied DC bias voltage (refer the capacitor's datasheet for details).

Larger capacitance and lower capacitor ESR improve the load transient response, PSRR and output voltage noise, therefore recommended output capacitor value is 10 μF.

Output Voltage

NCP731 part is available in several fixed output voltage versions (FIX) and adjustable version (ADJ). Both versions allow connection of external feed forward capacitor (C_{FF}) which improves dynamic performance (PSRR, noise, transient response) but prolongs the startup time, see charts in Typical characteristics section.

Application with FIX LDO version provides output voltage equal to LDO's nominal output voltage $V_{OUT-NOM}$ (given by OPN, see Ordering information table), while application with ADJ LDO version allows adjustability of the output voltage by external resistor divider connected to OUT, ADJ and GND pins. Then the output voltage can be computed by the following equation:

$$V_{OUT} = V_{ADJ} \cdot \left(1 + \frac{R_1}{R_2}\right) + I_{ADJ} \cdot R_1 \qquad \text{(eq. 1)}$$

Where:

V_{OUT} is output voltage of the circuit with resistor divider (adjustable application)

V_{ADJ} is the ADJ version reference voltage (1.2 V)

I_{ADJ} is the ADJ pin input current

R_1 is the upper resistor in resistor divider

R_2 is the lower resistor in resistor divider

Recommended values of R_1 and R_2 are in range from 1 kΩ to about 300 kΩ. Higher resistor values are better from current consumption point of view.

Both circuits of FIX (non−adjustable) and ADJ (adjustable) applications are shown at the following figures.

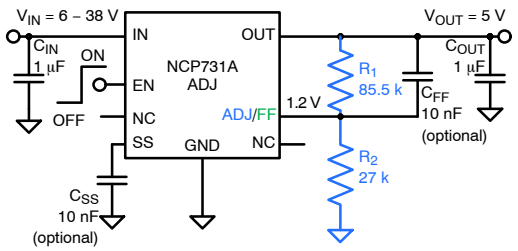


Figure 59. ADJ (adjustable) Application Schematic

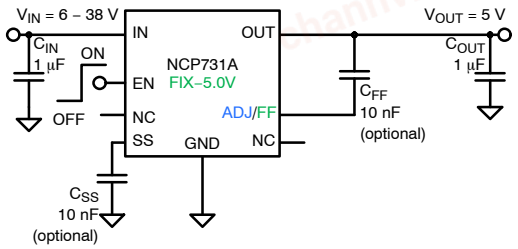


Figure 60. FIX (non−adjustable) Application Schematic

Next table lists recommended resistor divider values (R_1 and R_2) selected from E24 series.

Table 4. EXAMPLES OF RESISTOR DIVIDER VALUES

V_{OUT} [V]	R_1 [kΩ]	R_2 [kΩ]	V_{OUT2} [V]	err [%]
1.2	Short	None	1.200	0.00
2.5	39	36	2.500	0.02
3.3	82	47	3.294	−0.17
5.0	51	16	5.026	0.51
8.0	68	12	8.001	0.01
10.0	220	30	10.002	0.02
12.0	270	30	12.003	0.02
15.0	150	13	15.048	0.32

Where:

V_{OUT} [V] is desired output voltage

V_{OUT2} [V] is calculated output voltage

err [%] is difference between desired and calculated output voltage

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Of course, the table above is just an example and other values of output voltage divider resistors are possible.

Listed V_{OUT2} values were computed according to Equation 1, for zero R_1, R_2 and V_{ADJ} errors and I_{ADJ} = 10 nA.

Startup

In the NCP731 device there are two main internal signals which triggers the startup process, the IN−pin under−voltage lockout (UVLO) signal and enable signal. The first one comes from UVLO comparator, which monitors if the IN−pin voltage is high enough, while the second one comes from EN−pin comparator. Both comparators have embedded hysteresis to be insensitive to input noise. When both signals turn into high level, the startup process is initiated. The feed−forward capacitor, used to improve dynamic behavior, unintentionally influences the rise time and the shape of output voltage ramp−up. When C_{FF} is lower or just slightly higher than C_{SS}, the output voltage rises linearly and the rise time is programmable by external soft−start capacitor (C_{SS}). The influence of both these capacitors to IN−pin resp. EN−pin startup behavior is shown at Typical characteristics section. Total startup time, combined from startup delay time and output voltage rise time, could be computed by this equation (when $C_{FF} \le C_{SS}$):

$$t_{SS} = t_{SS-DLY} + t_{RAMP} \quad \text{(eq. 2)}$$

$$t_{SS} = t_{SS-DLY} + t_{RAMP-MIN} + \frac{V_{REF}}{I_{SS}} \cdot C_{SS}$$

$$t_{SS}[\mu s] = 160 + 90 + \frac{1.2\ V}{910\ nA} \cdot C_{SS}[nF] \cdot 1e6$$

$$t_{SS}[\mu s] = 250 + 1319 \cdot C_{SS}[nF]$$

Where:

- t_{SS} is overall startup time
- t_{SS-DLY} is startup delay time (160 μs typ.)
- t_{RAMP} is output voltage ramp−up time
- $t_{RAMP-MIN}$ is shortest output voltage ramp−up time (90 μs typ. for C_{SS} = 0 nF)
- V_{REF} is internal voltage reference (1.2 V typ.)
- I_{SS} is soft−start charging current (910 nA typ.)

Thermal Protection

When the LDO's die temperature exceeds the thermal shutdown threshold value, the device is internally disabled. The IC will remain in disabled state until the die temperature decreases by the thermal shutdown hysteresis value. Then the LDO is back enabled.

The thermal shutdown feature provides the protection against overheating due to application failure and it is not intended to be used as a normal working function.

Power Dissipation

Power dissipation caused by voltage drop across the LDO and by the output current flowing through the device needs to be dissipated out from the chip. The maximum power dissipation is dependent on the PCB layout, number of used Cu layers, Cu layers thickness and the ambient temperature. The maximum power dissipation can be computed by one of the following equations:

$$P_{DIS} = \frac{T_J - T_A}{R_{\theta JA}}$$

Or

$$P_{DIS} = \frac{T_J - T_B}{R_{\theta JB}}$$

Where:

- T_J is the desired junction temperature
- T_A is the ambient temperature
- T_B is the board temperature (on the trace within 1 mm of the package body)
- $R_{\theta JA}$ is junction to ambient thermal resistance
- $R_{\theta JB}$ is junction to board thermal resistance

If we enter the maximum junction temperature for the junction temperature $T_J = T_{J(MAX)}$, we obtain a maximum allowable power dissipation $P_{DIS(MAX)}$. Then, if higher power dissipation than maximum power dissipation is applied ($P_{DIS} > P_{DIS(MAX)}$), the device will be overheated ($T_J > T_{J(MAX)}$).

We can substitute for the power dissipation the following equation:

$$P_{DIS} = (V_{IN} - V_{OUT}) \cdot I_{OUT}$$

To obtain:

$$P_{DIS} = \frac{T_J - T_X}{R_{\theta JX}} = (V_{IN} - V_{OUT}) \cdot I_{OUT}$$

And then express the output current:

$$I_{OUT} = \frac{T_J - T_X}{R_{\theta JX} \cdot (V_{IN} - V_{OUT})}$$

Where:

- T_X is T_A resp. T_B
- $R_{\theta JX}$ is $R_{\theta JA}$ resp. $R_{\theta JB}$

And similarly, if we enter the maximum junction temperature for the junction temperature $T_J = T_{J(MAX)}$, we obtain an equation for the maximum allowable load current $I_{OUT(MAX)}$.

$$I_{OUT(MAX)} = \frac{T_{J(MAX)} - T_X}{R_{\theta JX} \cdot (V_{IN} - V_{OUT})}$$

Then, if higher load current than maximum load current is applied ($I_{OUT} > I_{OUT(MAX)}$), the device will be overheated ($T_J > T_{J(MAX)}$).

Maximum allowable output current charts are shown at Figures 57 and 58. Note, $I_{OUT(MAX)}$ at such figures is based

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on previous equation and is limited to nominal current I_{NOM} (nominal LDO's output current).

PCB Layout Recommendations

To obtain good LDO's stability and the best transient, PSRR and output voltage noise performance, place both C_{IN} and C_{OUT} capacitors as close as possible to the device pins, make the PCB traces wide and short and place capacitors to the same PCB Cu layer as the LDO is (avoid connections through vias). The same rules should be applied to the connections between C_{OUT} and the load – the less parasitic impedance the better dynamic performance at the point of load.

Regarding high impedance ADJ/FF and SS pins, prevent capacitive coupling of their traces to any switching signals in the application.

EN input doesn't need any special care.

GND pin and exposed pad should be connected to PCB GND plane for the best power spreading out of the chip. NC pins could be connected the PCB GND plane as well.

ORDERING INFORMATION

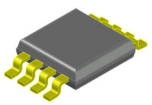
Part Number	Marking	Voltage Option ($V_{OUT-NOM}$)	Package	Shipping†
NCP731ADN330R2G	731A33	FIX, 3.3 V	MSOP8 EP (Pb−Free)	3000 / Tape & Reel
NCP731ADN500R2G	731A50	FIX, 5.0 V		
NCP731ADNADJR2G	731AAD	ADJ, 1.2 V		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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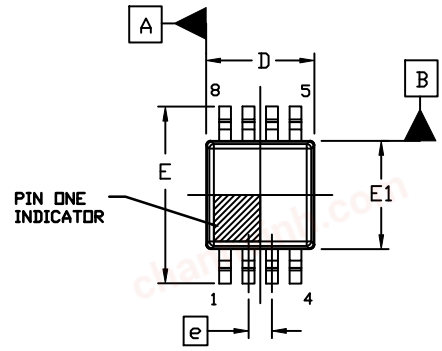
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

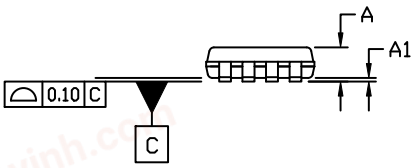


MSOP8 EP 3x3
CASE 846AT
ISSUE O

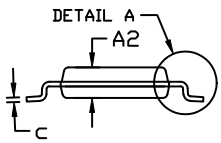
DATE 01 OCT 2020



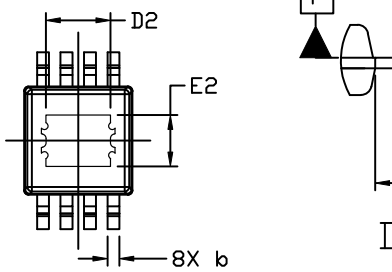
TOP VIEW



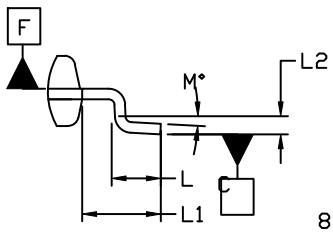
SIDE VIEW



END VIEW



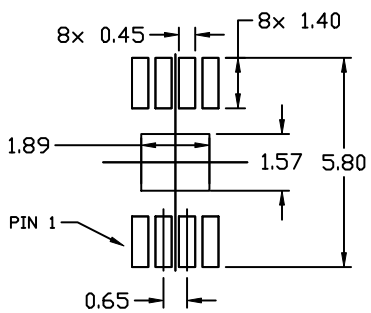
BOTTOM VIEW NOTE 3



DETAIL A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS b AND c APPLY TO THE PLATED LEADS.
5. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. PIN 1 INDICATOR IS LOCATED HERE. MAY APPEAR AS A LASER MARKED, OR A MOLDED (CIRCLE OR HALF MOON), INDENT.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.10	0.15
A2	0.813	0.863	0.914
b	0.28	---	0.38
c	0.139	---	0.23
D	2.90	3.00	3.10
D2	1.50	1.70	1.80
E	4.775	4.876	4.978
E1	2.90	3.00	3.10
E2	1.14	1.40	1.50
e	0.65 BSC		
L	0.40	---	---
L1	0.94 REF		
L2	0.25 REF		
M	0°	---	8°



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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