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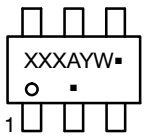
Secondary Side Synchronous Rectification Driver for High Efficiency SMPS Topologies

NCP4307



TSOP−6
SN SUFFIX
CASE 318G−02

MARKING DIAGRAM



XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

The NCP4307 is high performance driver tailored to control a synchronous rectification MOSFET in switch mode power supplies. Thanks to its high performance drivers and versatility, it can be used in various topologies such as DCM or CCM flyback, quasi resonant flyback and forward.

Internal minimum off−time and on−time blanking periods help to fight the ringing induced by the PCB layout and other parasitic elements. A reliable and noise less operation of the SR system is ensured due to the Self Synchronization feature. The NCP4307 also utilizes Kelvin connection of the driver to the MOSFET to achieve high efficiency operation at full load and utilizes a light load detection architecture to achieve high efficiency at light load.

The precise turn−off threshold, extremely low turn−off delay time and high sink current capability of the driver allow the maximum synchronous rectification MOSFET conduction time and enables maximum SMPS efficiency.

Self−supply capability allows to use NCP4307 in high side configuration and/or in low output voltage SMPS without auxiliary winding or other power source.

Features

- Self−Contained Control of Synchronous Rectifier in CCM, DCM and QR for Flyback Applications
- Precise True Secondary Zero Current Detection
- Typically 15 ns Turn off Delay from Current Sense Input to Driver
- Rugged Current Sense Pin (up to 200 V)
- Self−Supply Capability in Case of High Side Operation or Low V_{OUT}
- Ultrafast Turn−off Trigger Interface/Disable Input (10.5 ns)
- Internal Minimum ON−Time With Reverse Current Protection
- Internal Minimum OFF−Time with Ringing Detection
- Improved Robust Self Synchronization Capability
- 7 A / 2 A Peak Current Sink / Source Drive Capability
- Operating Voltage Range up to V_{CC} = 35 V
- Automatic Light−Load Disable Mode
- High Side Operation Capability without External Components or Auxiliary Winding
- Two VCC Pins Option Allows to Optimize Power Consumption in Wide V_{OUT} Range Applications
- Low Startup and Disable Current Consumption
- TSOP6 Package
- These are Pb−Free Devices

Typical Applications

- Notebook Adapters
- High Power Density AC/DC Power Supplies (Cell Phone Chargers)
- LCD TVs
- All SMPS with High Efficiency Requirements

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ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Shipping†
NCP4307FASNT1G	7FA	TSOP−6 (Pb−Free)	3000 / Tape and Reel
NCP4307FBSNT1G	7F2		
NCP4307AASNT1G	7AA		
NCP4307WASNT1G	7WA		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

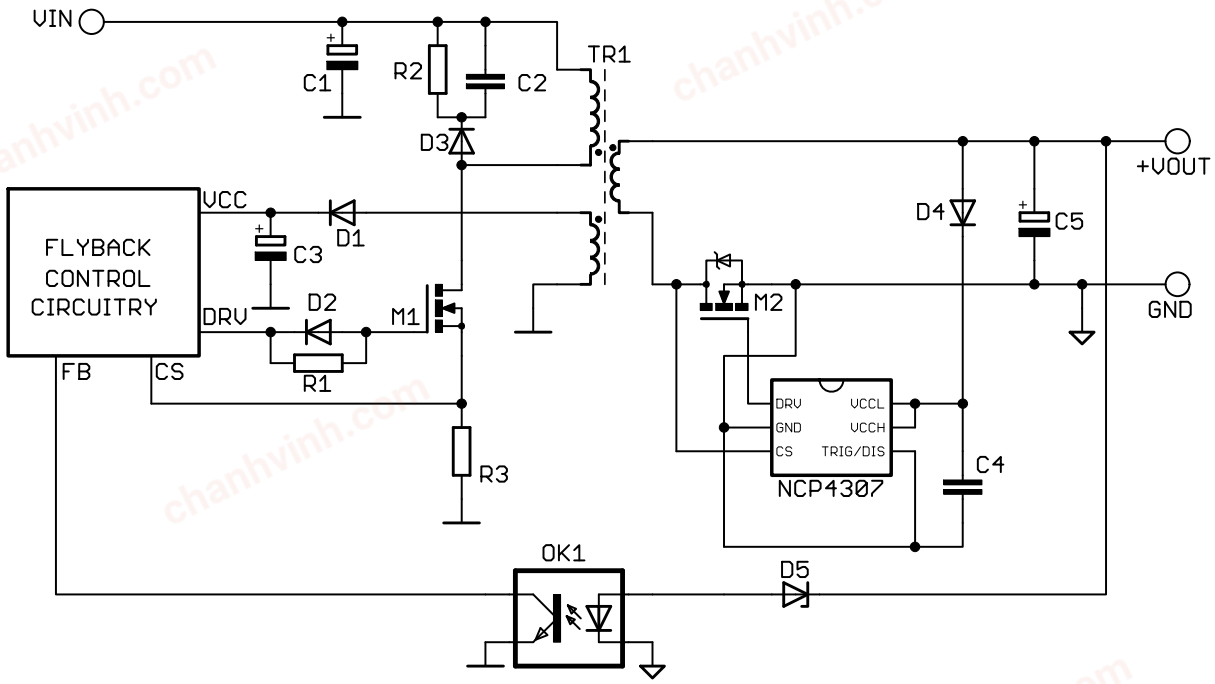


Figure 1. Typical Application Example – DCM, CCM or QR Flyback Converter

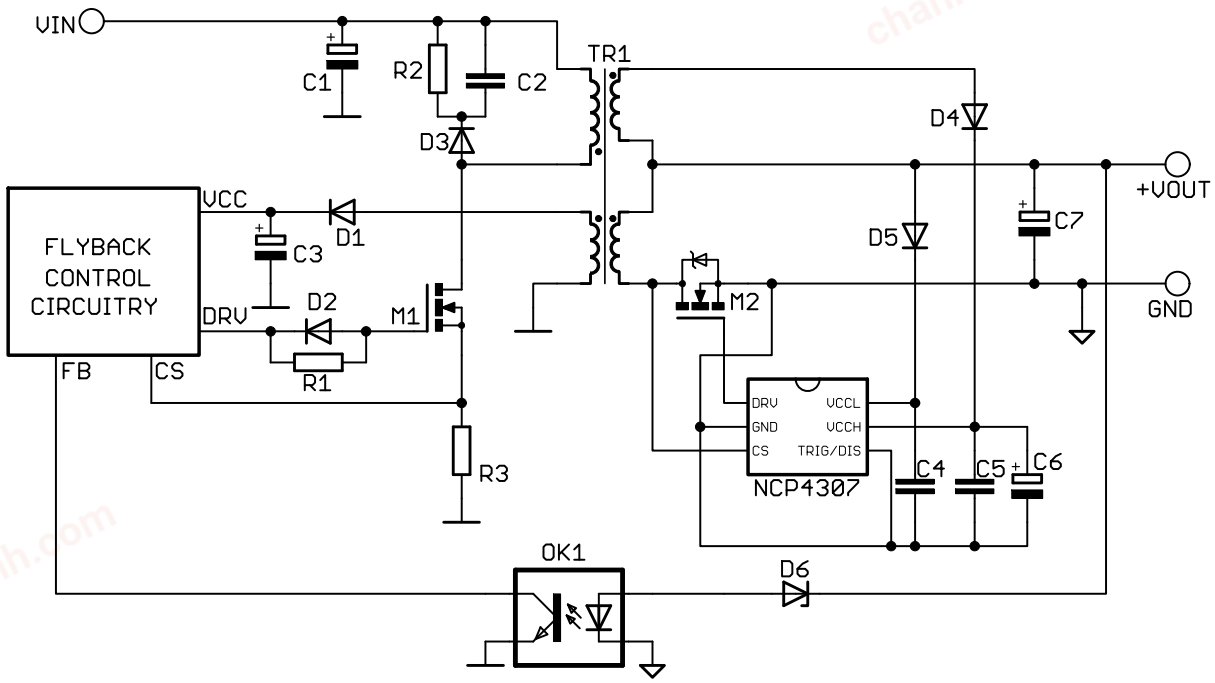


Figure 2. Typical Application Example – DCM, CCM or QR Flyback Converter with Two VCC Sources

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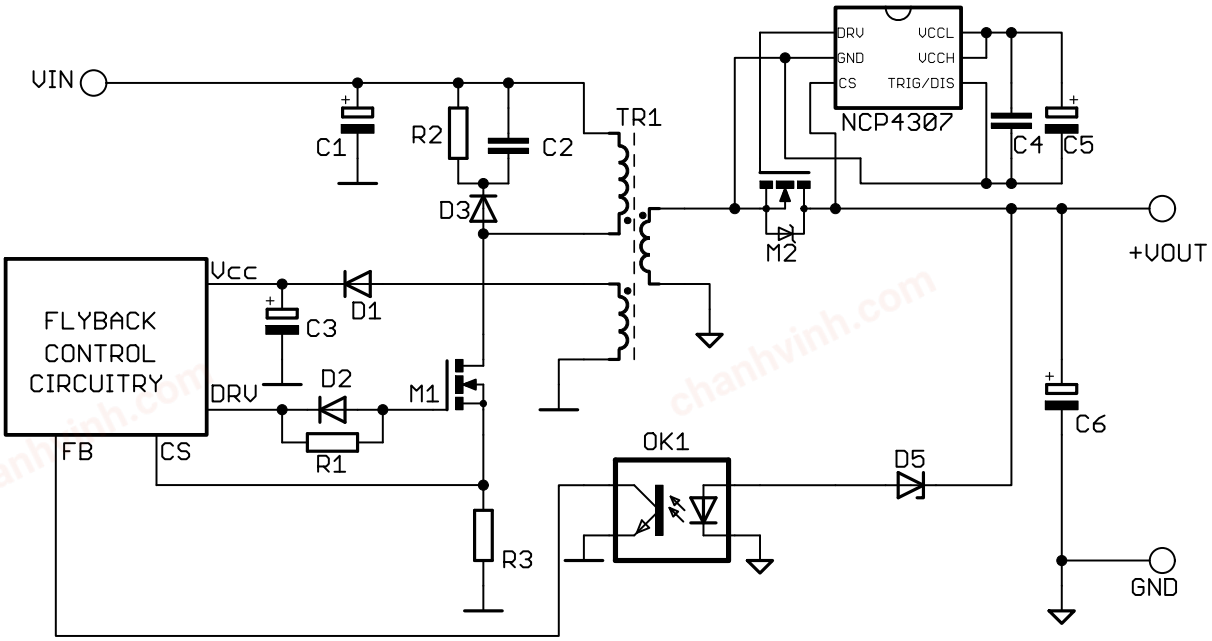


Figure 3. Typical Application Example – DCM, CCM or QR Flyback Converter with NCP4307 in High Side Configuration with Self−Supply

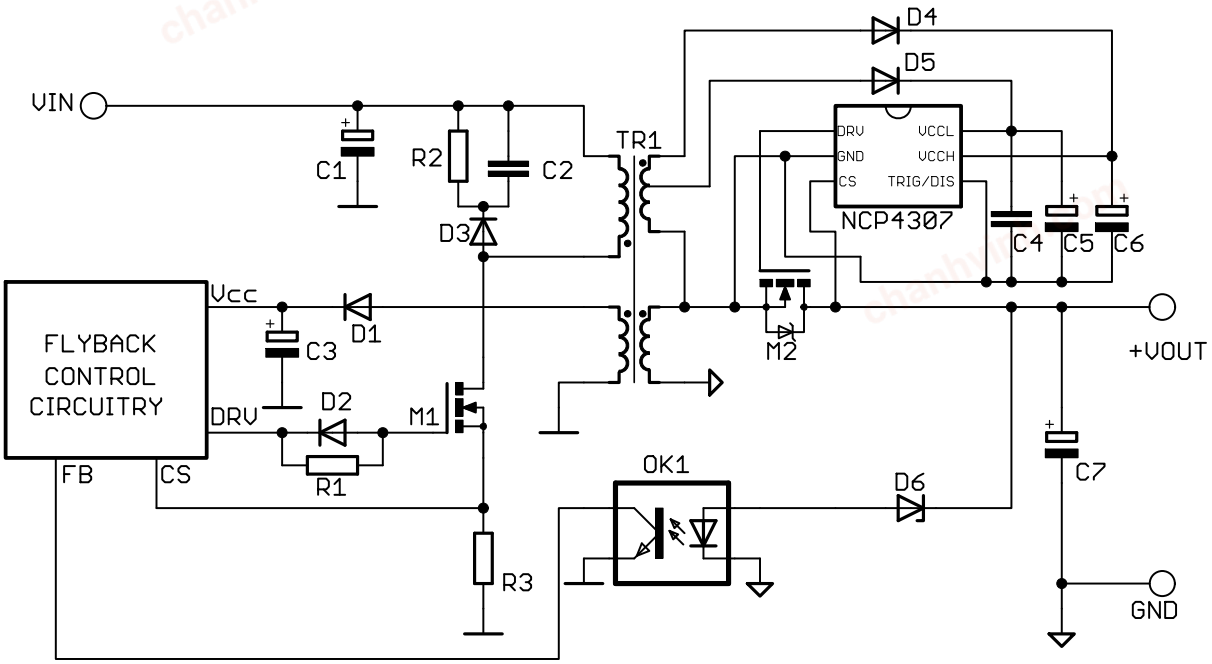


Figure 4. Typical Application Example – DCM, CCM or QR Flyback Converter with NCP4307 in High Side Configuration with Dual Aux Supply

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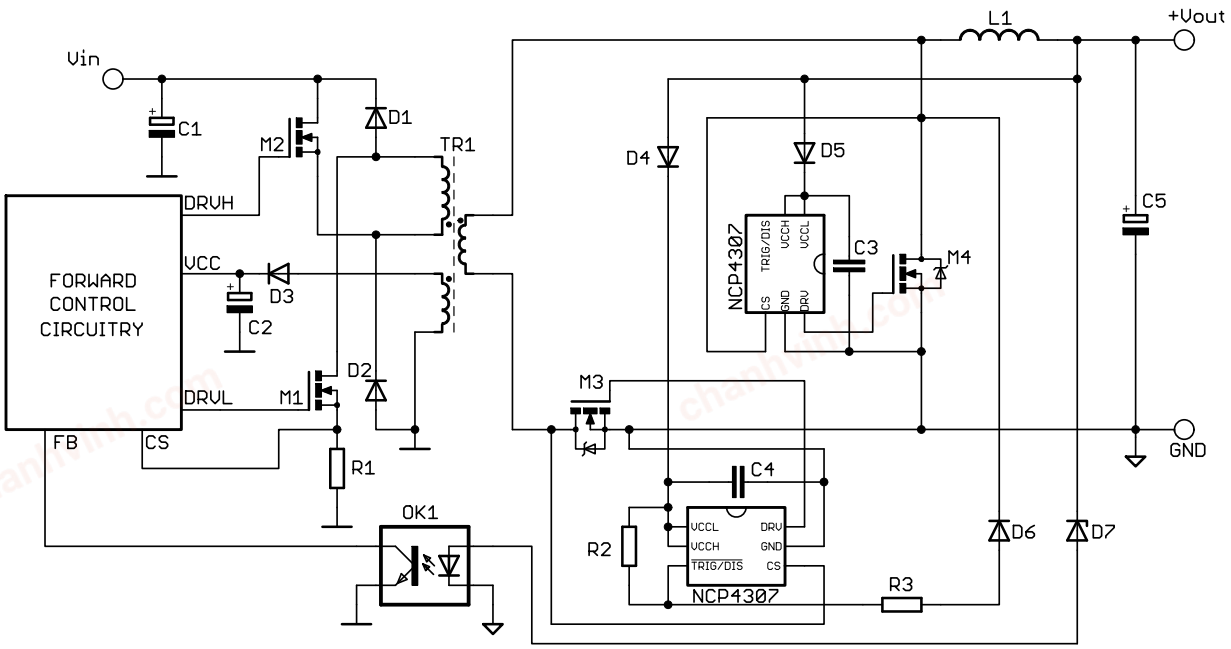


Figure 5. Typical Application Example – Two Switch Forward with Freewheeling and Forward Synchronous Rectifications. Forward SR Uses Special Version with Trigger Blocking Function

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PIN FUNCTION DESCRIPTION

TSOP6	Pin Name	Description
1	DRV	Driver output for the SR MOSFET
2	GND	Ground connection for the SR MOSFET driver and V_{CCL} decoupling capacitor. GND pin should only be connected directly to the SR MOSFET source terminal/soldering point using Kelvin connection.
3	CS	Current sense pin detects if the current flows through the SR MOSFET and/or its body diode. Basic turn−off detection threshold is 0 mV. Internal current source takes supply from this pin for SR self−supply.
4	TRIG/DIS	Ultrafast turn−off input that can be used to turn off the SR MOSFET in CCM applications in order to improve efficiency. Activates disable mode if pulled−up for more than 100 μs. It is also used as +dV/dt detector pin or driver blocking in special cases. This pin is mostly active high (positive logic), but some device versions may have active low (negative logic) option. See OPN coding table for details.
5	VCCH	Connected to higher than VCCL pin voltage in VCCH range, or connect it to VCCL pin if not used
6	VCCL	Main supply voltage pin. Decoupling capacitor should be connected to this pin and GND pin. Connect it to power source with voltage of V_{CCL} range via diode or connect capacitor there, in case if self−supply is wanted

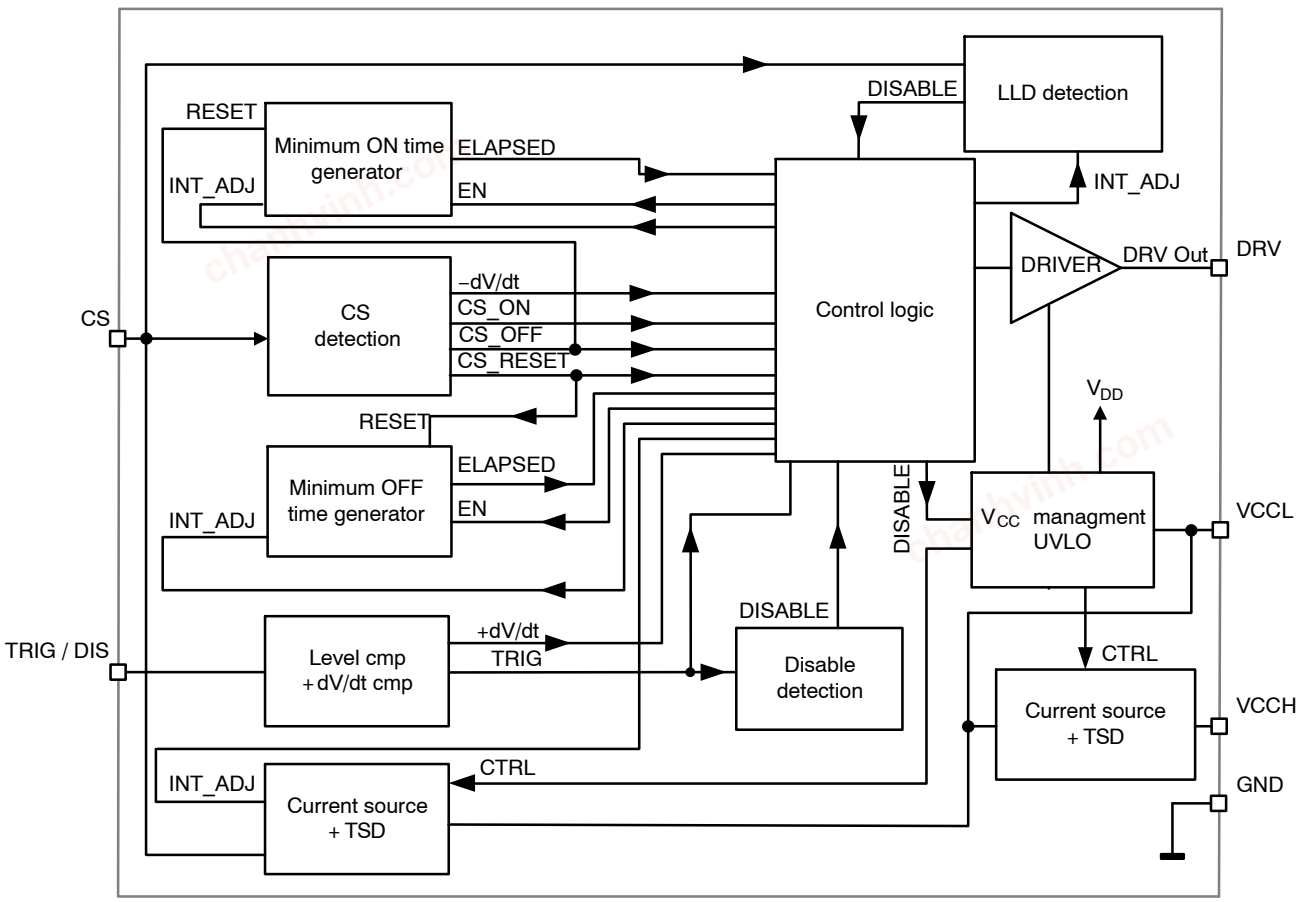


Figure 6. Internal Circuit Architecture – NCP4307

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ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{CCL}	Supply Voltage at VCCL Pin	−0.3 to 37.0	V
V_{CCH}	Supply Voltage at VCCH Pin	−0.3 to 37.0	V
$V_{TRIG/DIS}$	TRIG/DIS Pin Voltage	−0.3 to 37.0	V
V_{DRV}	Driver Output Voltage	−0.3 to 17.0	V
V_{CS}	Current Sense Input Voltage	−1 to 200	V
V_{CS_DYN}	Current Sense Dynamic Input Voltage (t_{PW} = 200 ns)	−10 to 200	V
I_{DRV_DYN}	DRV Pin Current (t_{PW} = 4 μs)	−3 to 12	A
I_{VCCL_DYN}	VCCL Pin Current (t_{PW} = 4 μs)	3	A
I_{CS}	CS Pin Current	250	mA
$R_{\theta J-A_TSOP6}$	Junction to Air Thermal Resistance, TSOP6	250	°C/W
T_{JMAX}	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	−60 to 150	°C
ESD_{HBM}	ESD Capability, Human Body Model (Note 1)	2000	V
ESD_{CDM}	ESD Capability, Charged Device Model (Note 1)	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per JEDEC Standard JESD22−A114E.
   Charged Machine Model per JEDEC Standard JESD22−C101F
2. This device meets latch−up tests defined by JEDEC Standard JESD78D.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CCL}, V_{CCH}	Maximum Operating Voltage	−	35	V
T_J	Operating Junction Temperature	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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ELECTRICAL CHARACTERISTICS ($-40°C \le T_J \le 125°C$; V_{CCL} = 12 V; V_{CCH} = 0 V; C_{DRV} = 0 nF; $V_{TRIG/DIS}$ = 0 V ($V_{TRIG/DIS}$ = 5 V or V_{CCL} whichever is lower for negative trigger logic); V_{CS} = 0 V, unless otherwise noted. Typical values are at T_J = +25°C)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
SUPPLY SECTION							
V_{CCL_ON}	VCCL UVLO	V_{CCL} rising		3.7	4.0	4.2	V
V_{CCL_OFF}		V_{CCL} falling		3.2	3.5	3.7	
V_{CCL_HYS}	VCCL UVLO Hysteresis			–	0.5	–	V
t_{START_DEL}	Start−up Delay	V_{CCL} rising from 0 to V_{CCL_ON} + 1 V @ t_R = 10 μs		–	55	80	μs
I_{CCL_D}	Dynamic Current Consumption	C_{DRV} = 0 nF, f_{CS} = 100 kHz	V_{DRVMAX} = 10 V	–	0.8	1.6	mA
			V_{DRVMAX} = 5 V	–	0.8	1.6	
		C_{DRV} = 1 nF, f_{CS} = 100 kHz	V_{DRVMAX} = 10 V	–	1.8	3.0	
			V_{DRVMAX} = 5 V	–	1.2	2.4	
		C_{DRV} = 10 nF, f_{CS} = 100 kHz	V_{DRVMAX} = 10 V	–	12	18	
			V_{DRVMAX} = 5 V	–	6.0	12	
I_{CCL_Q}	Quiescent Current Consumption			–	0.50	0.75	mA
I_{CCL_UVLO}	Current Consumption below UVLO	positive trigger logic, $V_{CCL} = V_{CCL_OFF} - 0.1$ V		–	50	80	μA
		negative trigger logic, $V_{CCL} = V_{CCL_OFF} - 0.1$ V		–	60	90	
I_{CCL_LL}	Current Consumption in Light Load Mode	V_{CS} = 4 V; t > t_{LLD}		–	185	250	μA
I_{CCL_DIS}	Current Consumption in Disable Mode	positive trigger logic, $V_{TRIG/DIS}$ = 5 V		–	45	70	
		negative trigger logic, $V_{TRIG/DIS}$ = 0 V		–	55	80	
I_{CCH}	VCCH Current	V_{CCL} = 4.0 V, V_{CCH} = 12.0 V		20	30	40	mA
$V_{CCL_SB_A}$	VCCH Current Activation Threshold	V_{CCH} = 12 V, $V_{CCL_SB_A}$ = 4.7 V		4.4	4.7	4.9	V
		V_{CCH} = 16 V, $V_{CCL_SB_A}$ = 9.0 V		8.4	8.9	9.4	
$V_{CCL_SB_D}$	VCCH Current Deactivation Threshold	V_{CCH} = 12 V, $V_{CCL_SB_A}$ = 4.7 V		4.9	5.2	5.4	V
		V_{CCH} = 16 V, $V_{CCL_SB_A}$ = 9.0 V		8.9	9.4	9.9	
DRIVER OUTPUT							
t_R	Output Voltage Rise−Time	C_{DRV} = 10 nF, 10 % to 90 % V_{DRVMAX}, V_{CS} = 4 to −1 V		–	60	100	ns
t_F	Output Voltage Fall−Time	C_{DRV} = 10 nF, 90 % to 10 % V_{DRVMAX}, V_{CS} = −1 to 4 V		–	25	50	ns
R_{DRV_SOURCE}	Driver Source Resistance	Guaranteed by Design		–	2	–	Ω
R_{DRV_SINK}	Driver Sink Resistance	Guaranteed by Design		–	0.5	–	Ω
I_{DRV_SOURCE}	Output Peak Source Current	Guaranteed by Design		–	2	–	A
I_{DRV_SINK}	Output Peak Sink Current	Guaranteed by Design		–	7	–	A
$t_{DRV_ON_MAX}$	Maximum Driver Pulse Length	If it takes longer, DRV output voltage and comparators thresholds may be affected		–	4	–	ms
V_{DRV_MAX}	Maximum Driver Output Voltage	V_{CCL} = 35 V, C_{DRV} > 1 nF, V_{DRVMAX} = 10 V		9	10	11	V
		V_{CCL} = 35 V, C_{DRV} > 1 nF, V_{DRVMAX} = 5 V		4.5	5.0	5.5	
V_{DRV_MIN}	Minimum Driver Output Voltage	V_{CCL} = 3.8 V, V_{DRVMAX} = 10 V		3.6	3.8	4.0	V
		V_{CCL} = 3.8 V, V_{DRVMAX} = 5 V		3.6	3.8	4.0	

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ELECTRICAL CHARACTERISTICS ($-40°C \le T_J \le 125°C$; V_{CCL} = 12 V; V_{CCH} = 0 V; C_{DRV} = 0 nF; $V_{TRIG/DIS}$ = 0 V ($V_{TRIG/DIS}$ = 5 V or V_{CCL} whichever is lower for negative trigger logic); V_{CS} = 0 V, unless otherwise noted. Typical values are at T_J = +25°C) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
CS INPUT						
$t_{CS_ON_PD}$	Total Propagation Delay From CS to DRV Output On	V_{CS} goes down from 4 to −1 V, $t_{CS_F} \le 5$ ns	–	30	60	ns
$t_{CS_OFF_PD}$	Total Propagation Delay From CS to DRV Output Off	V_{CS} goes up from −1 to 4 V, $t_{CS_R} \le 5$ ns	–	15	23	ns
V_{CS_ON}	Turn On CS Threshold Voltage		−120	−85	−40	mV
V_{CS_OFF}	Turn Off CS Threshold Voltage	Guaranteed by Design	−1		0	mV
V_{CS_RESET}	Turn Off Timer Reset Threshold Voltage		0.4	0.5	0.6	V
$t_{CS_OFF_BLK}$	Off Comparator Blanking Time	Minimum on time is running; $t_{CS_OFF_BLK}$ = 105, 155 ns	−20%	$t_{CS_OFF_BLK}$	+30%	ns
		Minimum on time is running; $t_{CS_OFF_BLK}$ = 205, 255, 300, 390, 485, 600 ns	−15%		+15%	
$I_{CS_LEAKAGE}$	CS Leakage Current	V_{CS} = 200 V	–		10	μA
$V_{CS_DVDT_H}$	−dV/dt Detector High Threshold		–	3	–	V
$V_{CS_DVDT_L}$	−dV/dt Detector Low Threshold		–	0.5	–	V
$t_{CS_-DV/DT}$	−dV/dt Detector Threshold	Note 3; $t_{CS_-DV/DT}$ = 45 ns	–	45	–	ns
		Note 3; $t_{CS_-DV/DT}$ = 35 ns	–	35	–	
		Note 3; $t_{CS_-DV/DT}$ = 25 ns	18	25	32	
		Note 3; $t_{CS_-DV/DT}$ = 15 ns	–	15	–	
I_{CS_SS}	Supply Current	V_{CS} = 50 V, V_{CCL} = 4 V, V_{CCH} = 0 V, T_J = 25°C	90	105	120	mA
		V_{CS} = 50 V, V_{CCL} = 0 V, V_{CCH} = 0 V, T_J = 25°C	–	10	–	
TSD_{SS}	Supply Block Thermal Shut Down		–	170	–	°C
TSD_{SS_H}	Supply Block Thermal Shut Down Hysteresis		–	20	–	°C
$V_{CCL_SB_A}$	Supply Block Activation Threshold	V_{CS} = 20 V, $V_{CCL_SB_A}$ = 4.7 V	4.4	4.7	4.9	V
		V_{CS} = 20 V, $V_{CCL_SB_A}$ = 9.0 V	8.4	8.9	9.4	
$V_{CCL_SB_D}$	Supply Block Deactivation Threshold	V_{CS} = 20 V, $V_{CCL_SB_A}$ = 4.7 V	4.9	5.2	5.4	V
		V_{CS} = 20 V, $V_{CCL_SB_A}$ = 9.0 V	8.9	9.4	9.9	
TRIGGER DISABLE INPUT						
$t_{TRIG_PW_MIN}$	Minimum Trigger Pulse Duration	$V_{TRIG/DIS}$ = 5 V ($V_{TRIG/DIS}$ = 0 V for negative trigger logic); Shorter pulses may be not proceeded	–	–	10	ns
V_{TRIG_TH}	Trigger Threshold Voltage		1.7	2.0	2.3	V
t_{TRIG_PD}	Trigger to DRV Propagation Delay	positive trigger logic, $V_{TRIG/DIS}$ goes from 0 to 5 V, $t_{TRIG/DIS_R} \le 5$ ns	–	5	15	ns
		negative trigger logic, $V_{TRIG/DIS}$ goes from 5 to 0 V, $t_{TRIG/DIS_R} \le 5$ ns	–	11	20	
t_{TRIG_BLANK}	Trigger Blank Time After DRV Turn−on Event	V_{CS} drops below V_{CS_ON}	30	50	70	ns
t_{DIS_TIM}	Delay to Disable Mode	$V_{TRIG/DIS}$ goes from 0 – 5 V (5 – 0 V for negative trigger logic)	75	100	125	μs
t_{DIS_REC}	Disable Recovery Timer	$V_{TRIG/DIS}$ goes down from 5 – 0 V (0 – 5 V for negative trigger logic)	–	1.5	3.0	μs

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ELECTRICAL CHARACTERISTICS ($-40°C \le T_J \le 125°C$; V_{CCL} = 12 V; V_{CCH} = 0 V; C_{DRV} = 0 nF; $V_{TRIG/DIS}$ = 0 V ($V_{TRIG/DIS}$ = 5 V or V_{CCL} whichever is lower for negative trigger logic); V_{CS} = 0 V, unless otherwise noted. Typical values are at T_J = +25°C) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{DIS_END}	Minimum Pulse Duration to Disable Mode End	$V_{TRIG/DIS}$ = 0 V; Shorter pulses may be not proceeded	–	–	200	ns
$I_{TRIG/DIS}$	Positive Trigger Logic, Pull Down Current	$V_{TRIG/DIS}$ = 5 V	5	10	14	μA
	Negative Trigger Logic, Pull Up Current	$V_{TRIG/DIS}$ = 0 V	−14	−10	−5	
t_{TRIG_TRAN}	Maximum Transition Time	$V_{TRIG/DIS}$ goes from 1 to 3 V or from 3 to 1 V	–	–	10	μs
V_{TRIG_DVDT}	+dV/dt Detector Threshold		1.70	1.95	2.20	V
MINIMUM t_{ON} AND t_{OFF}						
t_{ON_MIN}	Minimum On Time	t_{ON_MIN} = 500, 600, 800, 900, 1100, 1400, 1700, 2000 ns	−10%	t_{ON_MIN}	+10%	ns
$t_{ON_INIT_BLK}$	Initial On Blank Time	$t_{ON_INIT_BLK}$ = 55 ns	33	50	72	ns
		$t_{ON_INIT_BLK}$ = 90 ns	70	90	120	
		$t_{ON_INIT_BLK}$ = 200 ns	170	200	230	
t_{OFF_MIN}	Internal Minimum t_{OFF} Time	t_{OFF_MIN} = 1.00, 1.75, 2.50, 3.25, 4.00, 4.75, 5.50, 6.25 μs	−10%	t_{OFF_MIN}	+10%	μs
LIGHT LOAD DETECTION						
t_{LLD}	LLD Main Time	$V_{CS} > V_{CS_LLD}$	80	100	120	μs
V_{CS_LLD}	LLD Detection Threshold	Detected at CS pin	–	100	–	mV
t_{LLD_REC}	Light Load Recovery Time	Guaranteed by Design	–	–	100	ns
$t_{LLD_EXIT_BLK}$	Light Load Exit On Comparator Blank Time	V_{CS} < 0 V, $t_{LLD_EXIT_BLK}$ = 45 ns	−30%	$t_{LLD_EXIT_BLK}$	+20%	ns
		V_{CS} < 0 V, $t_{LLD_EXIT_BLK}$ = 100 ns	−20%		+20%	
		V_{CS} < 0 V, $t_{LLD_EXIT_BLK}$ = 200, 300 ns	−15%		+15%	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Test signal

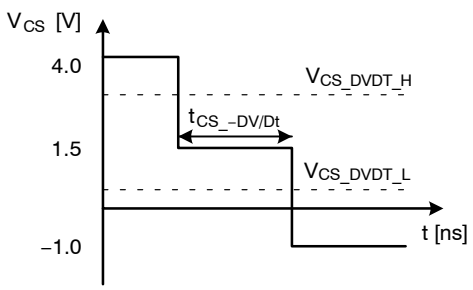


Figure 7. Test Signal

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TYPICAL CHARACTERISTICS

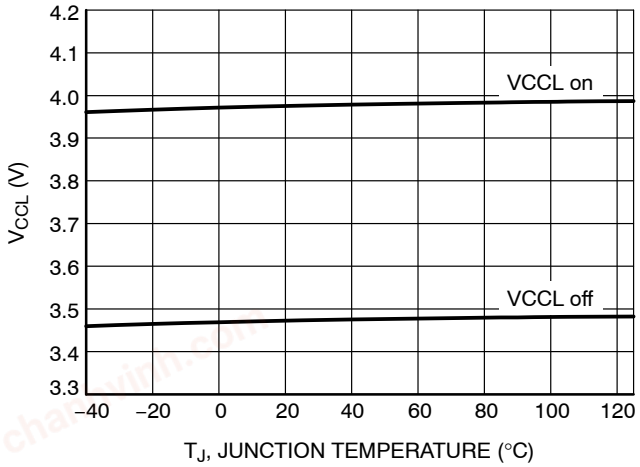


Figure 8. V_{CCLON} and V_{CCLOFF} Levels

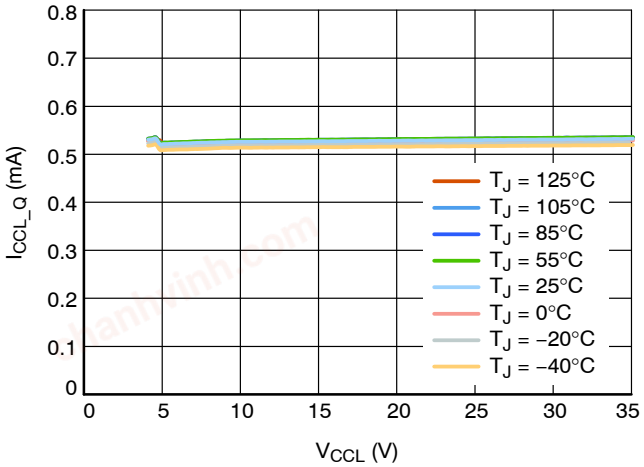


Figure 9. VCCL Quiescent Current Consumption V_{CS} = 0 V

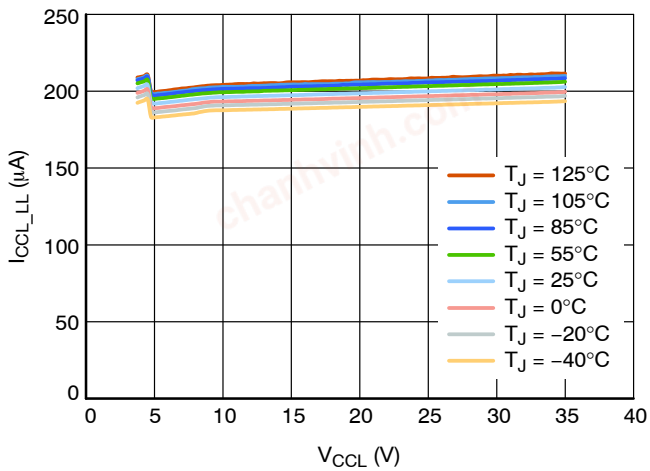


Figure 10. VCCL Current Consumption in Disable by LLD Function, V_{CS} = 4 V, t > t_{LLD}

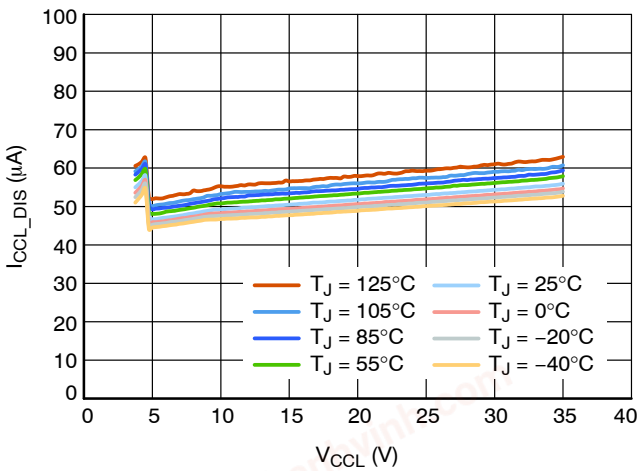


Figure 11. VCCL Current Consumption in Disable by TRIG/DIS Function, V_{CS} = 0 V and $V_{TRIG/DIS}$ = 5 V

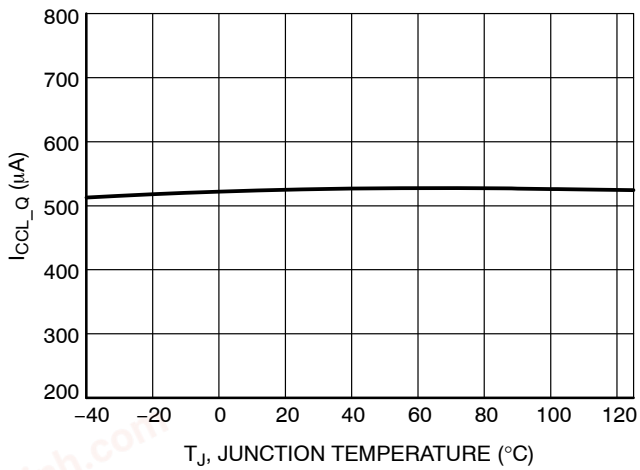


Figure 12. VCCL Quiescent Current Consumption

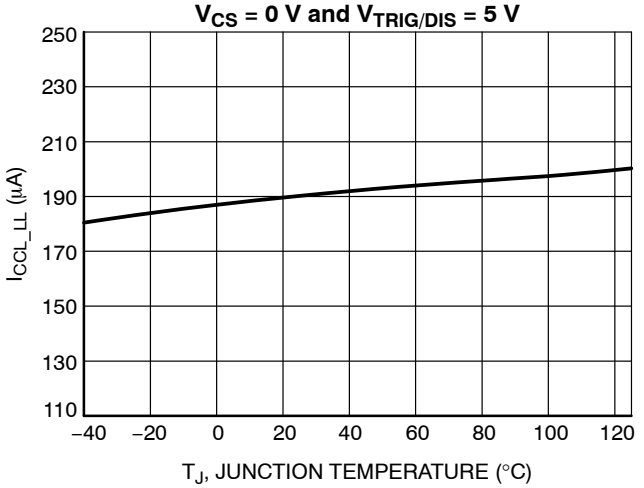


Figure 13. VCCL Current Consumption in Disable Caused by LLD Function

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TYPICAL CHARACTERISTICS

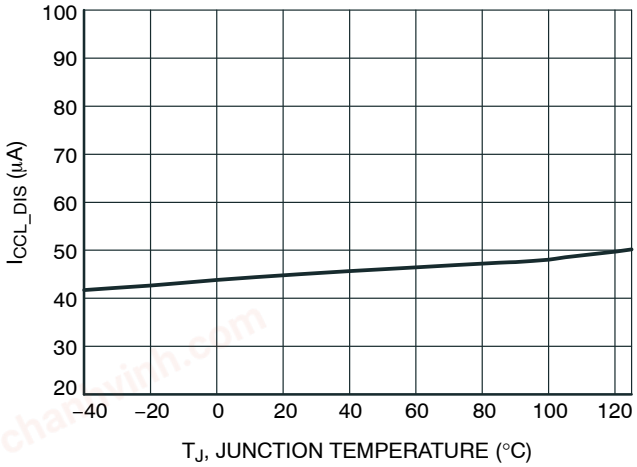


Figure 14. VCCL Current Consumption in Disable Activated by TRIG

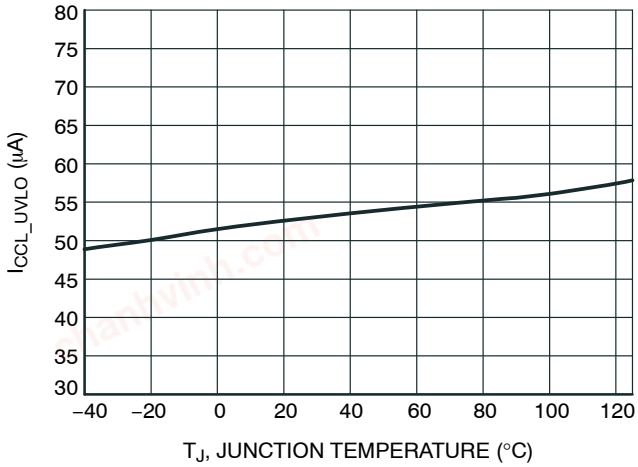


Figure 15. VCCL Current Consumption Below UVLO, VCCL = V_{CCLOFF} − 0.1 V

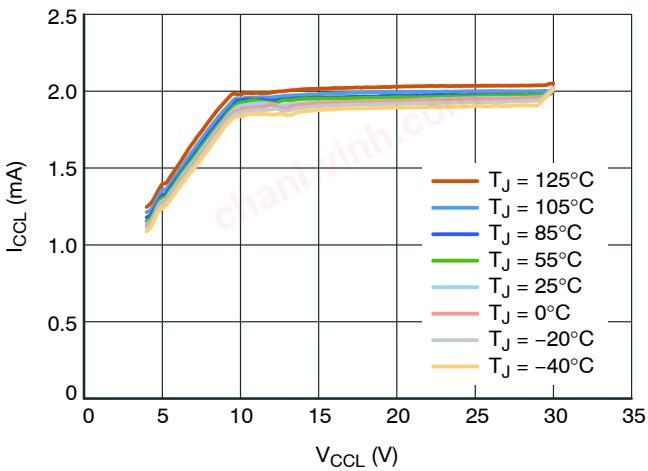


Figure 16. VCCL Current Consumption for 10 V Driver, V_{CS} = −1 to 4 V, f_{CS} = 100 kHz, C_{DRV} = 1 nF

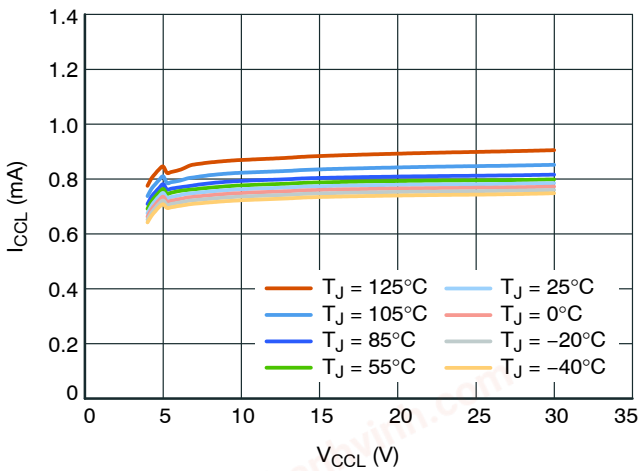


Figure 17. VCCL Current Consumption for 5 V Driver, V_{CS} = −1 to 4 V, f_{CS} = 100 kHz, C_{DRV} = 1 nF

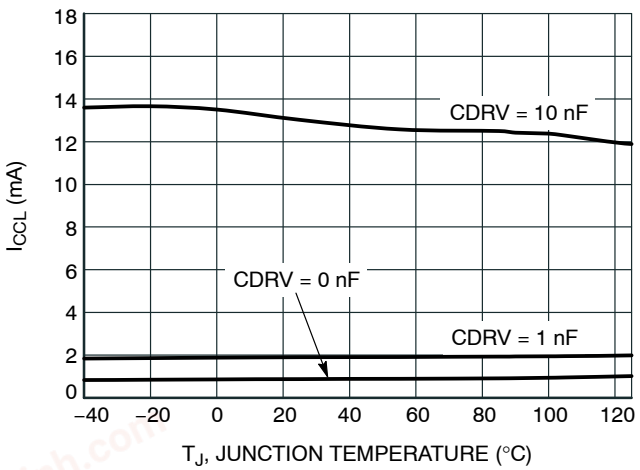


Figure 18. VCCL Current Consumption for 10 V Driver, V_{CS} = −1 to 4 V, f_{CS} = 100 kHz, V_{CCL} = 12 V

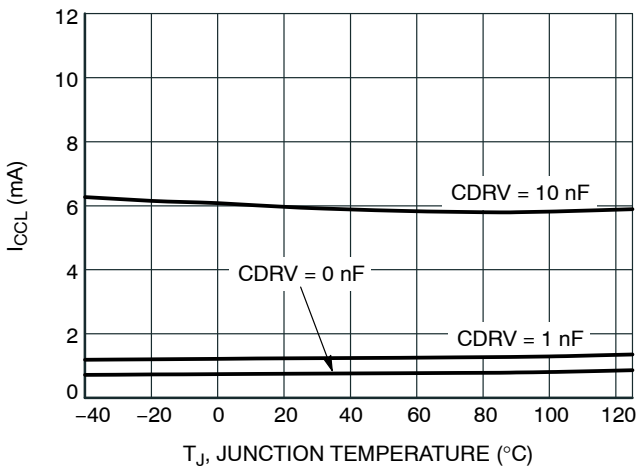


Figure 19. VCCL Current Consumption for 5 V Driver, V_{CS} = −1 to 4 V, f_{CS} = 100 kHz, V_{CCL} = 12 V

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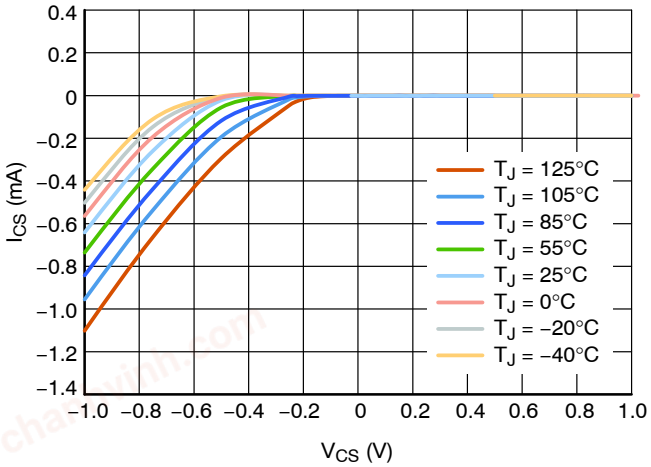


Figure 20. CS Current, V_{CCL} = 12 V

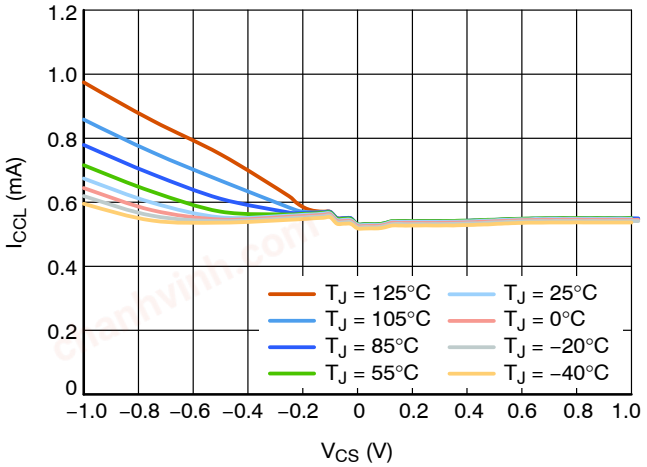


Figure 21. Supply Current vs. CS Voltage at V_{CCL} = 12 V

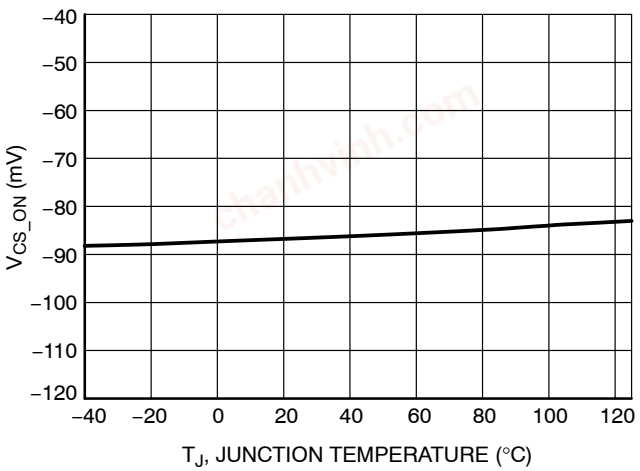


Figure 22. CS Turn−on Threshold

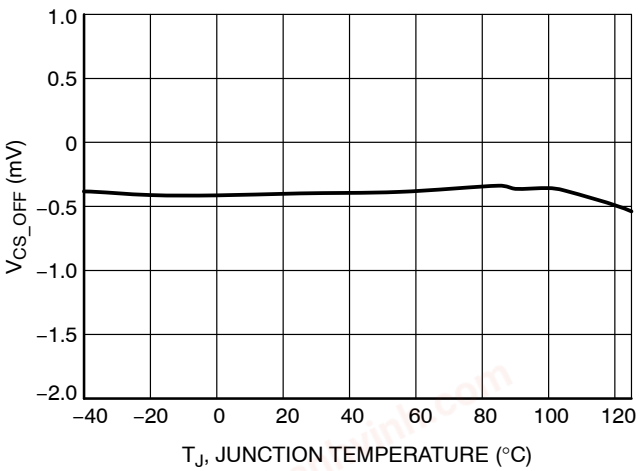


Figure 23. CS Turn−off Threshold

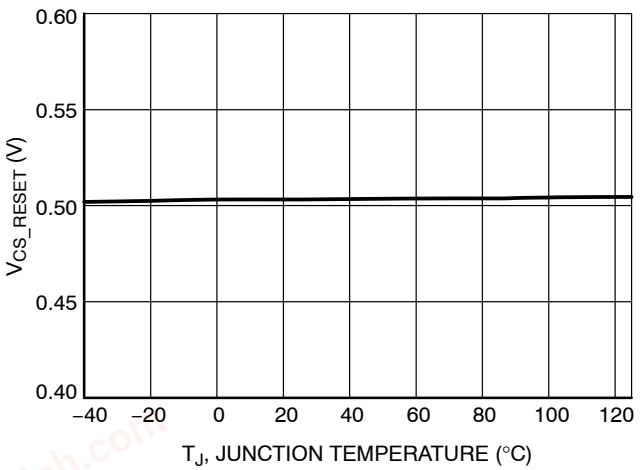


Figure 24. CS Reset Threshold

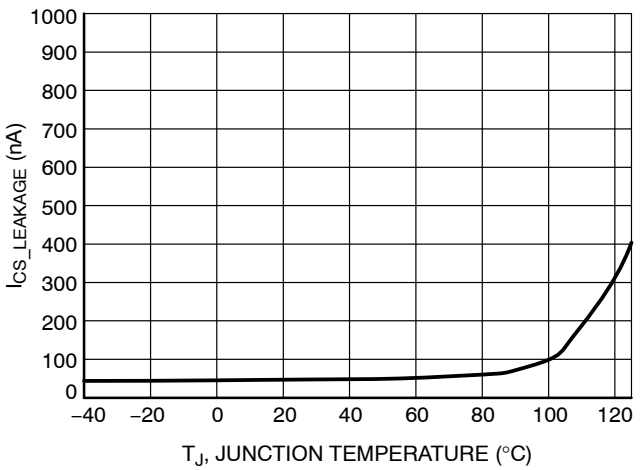


Figure 25. CS Leakage Current V_{CS} = 200 V

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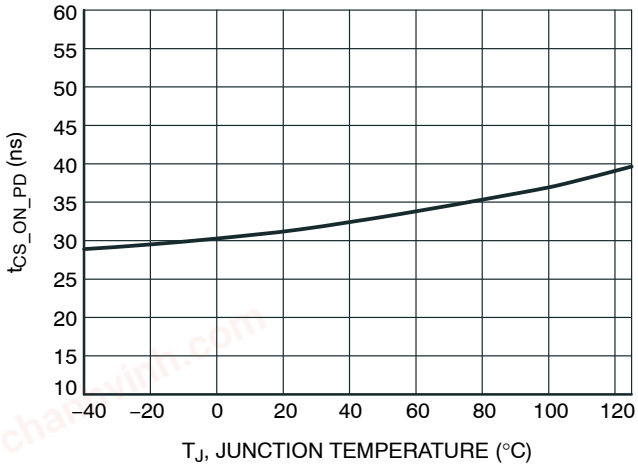


Figure 26. Propagation Delay from CS to DRV Output On

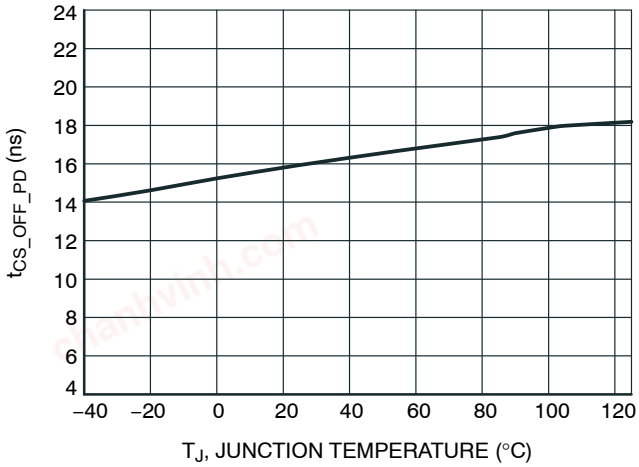


Figure 27. Propagation Delay from CS to DRV Output Off

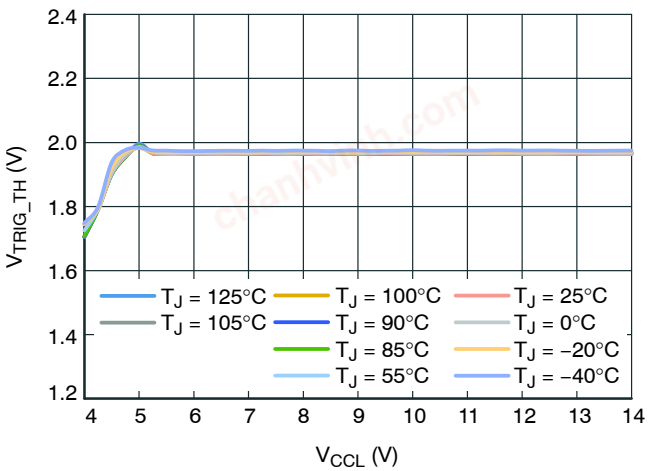


Figure 28. Trigger Threshold

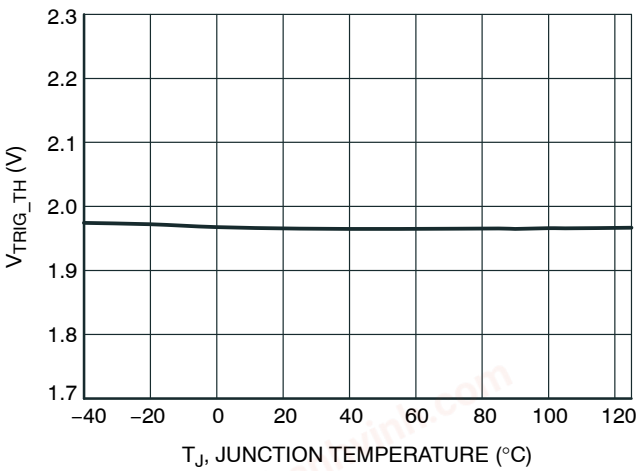


Figure 29. Trigger Threshold V_{CC} = 12 V

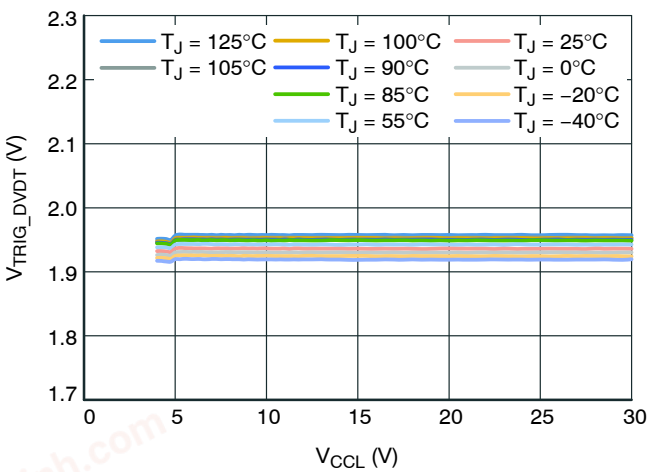


Figure 30. Trigger +dV/dt Threshold

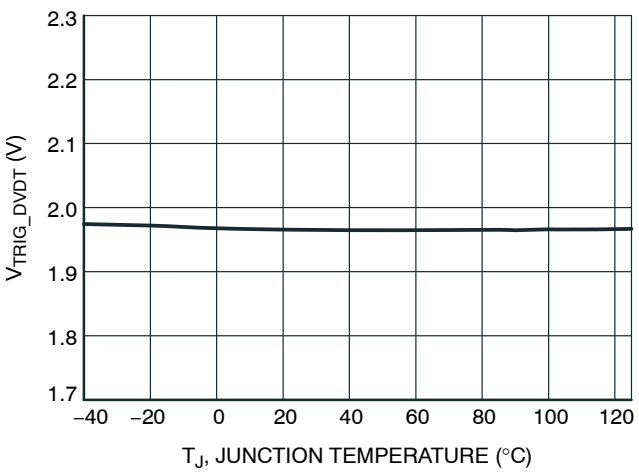


Figure 31. Trigger +dV/dt Threshold

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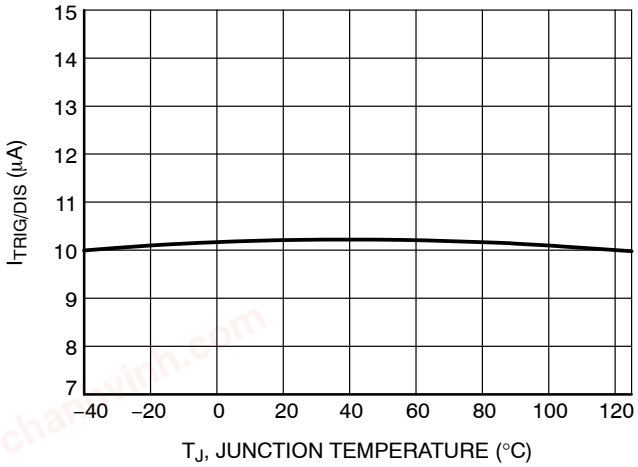


Figure 32. TRIG/DIS Pull Down Current

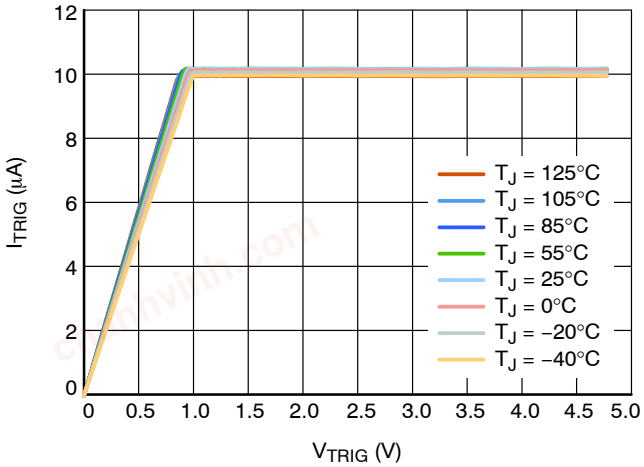


Figure 33. TRIG/DIS Pull Down Current to $V_{TRIG/DIS}$

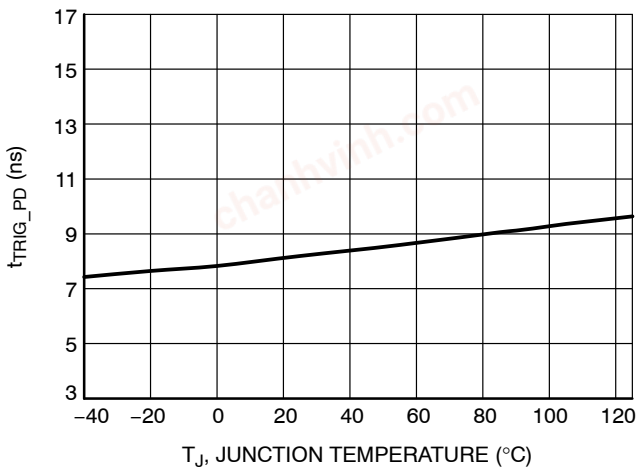


Figure 34. Propagation Delay from TRIG/DIS to DRV Output Off

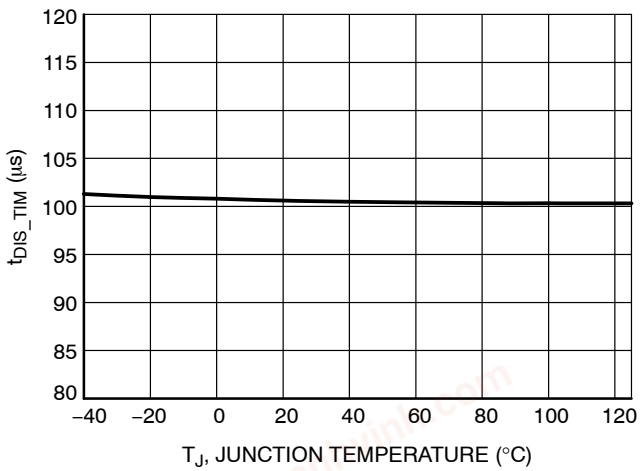


Figure 35. Delay to Disable Mode, V_{TRIG} = 5 V

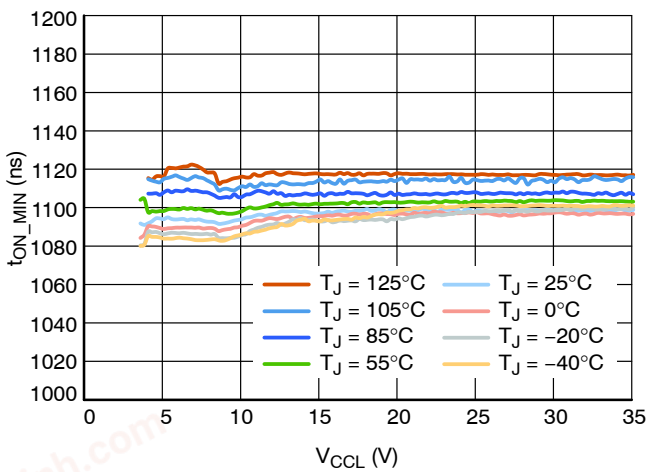


Figure 36. Minimum On Time t_{ON_MIN} = 1.1 μs

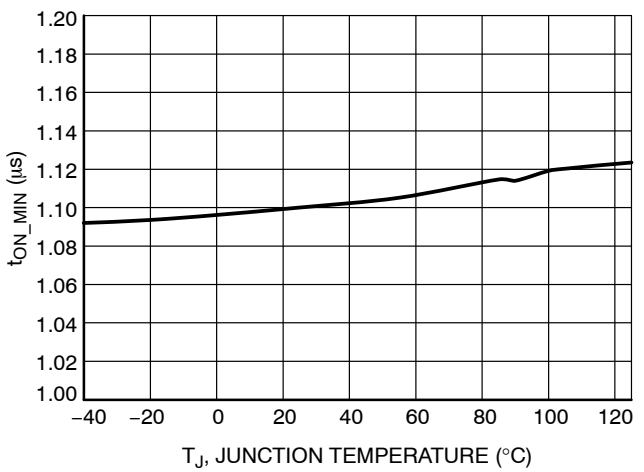


Figure 37. Minimum On Time t_{ON_MIN} = 1.1 μs

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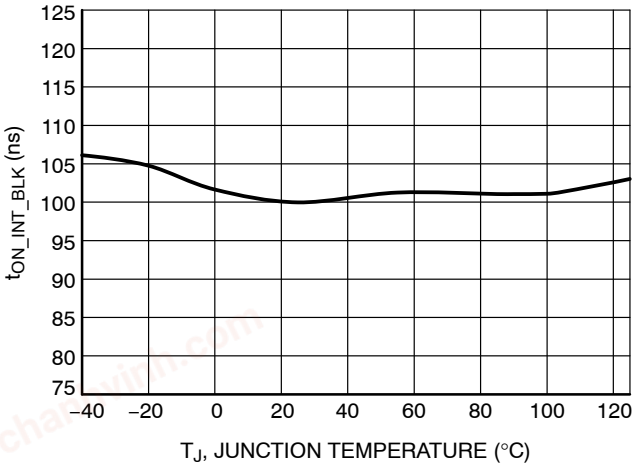


Figure 38. Initial On Blank Time $t_{ON_INIT_BLK}$ = 100 ns

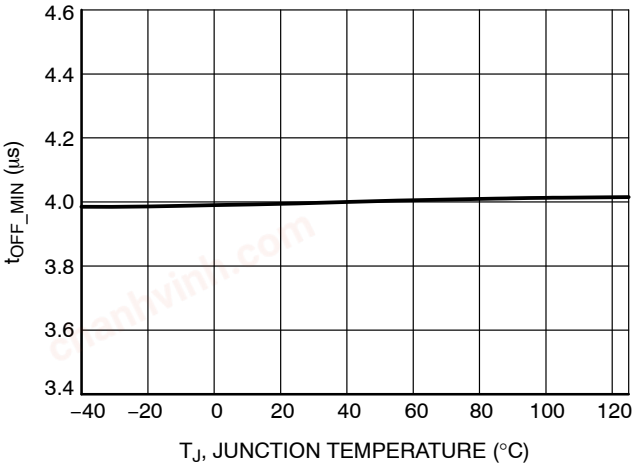


Figure 39. Minimum Off−time t_{OFF_MIN} = 4 μs

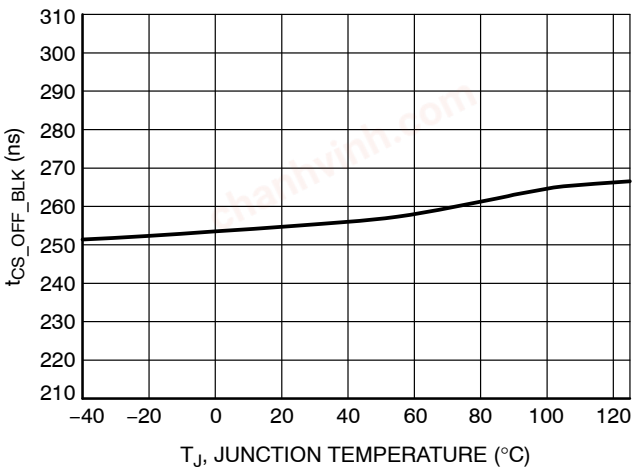


Figure 40. Off Comparator Blanking Time $t_{CS_OFF_BLK}$ = 255 ns

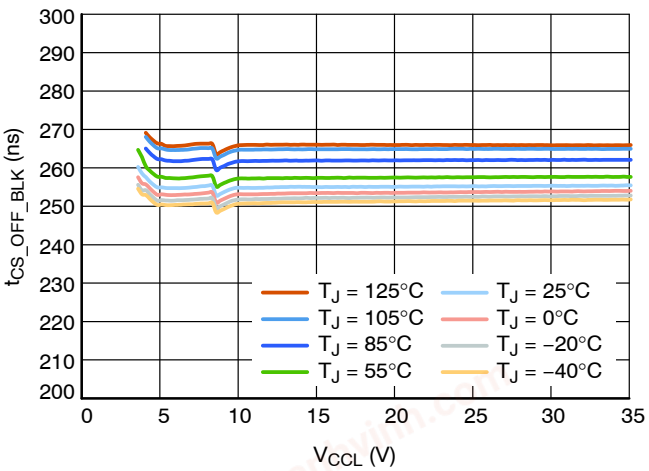


Figure 41. Off Comparator Blanking Time $t_{CS_OFF_BLK}$ = 255 ns

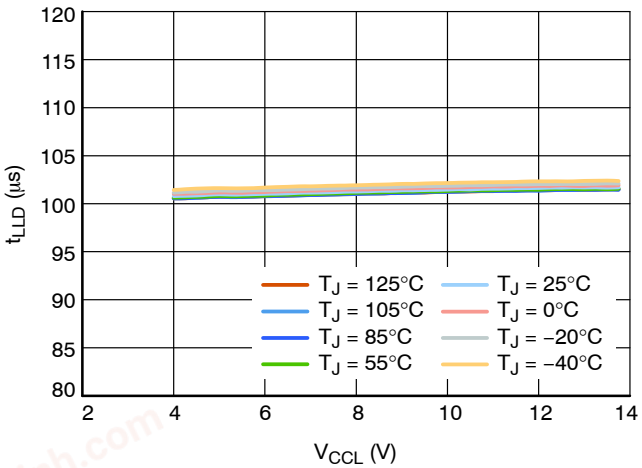


Figure 42. Light Load Detection Time t_{LLD} = 100 μs

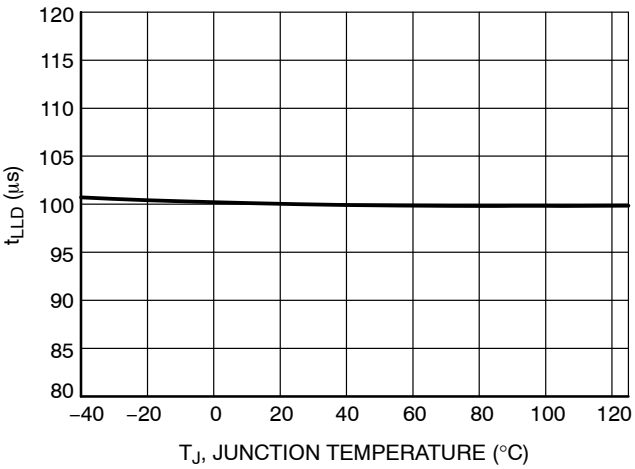


Figure 43. Light Load Detection Time t_{LLD} = 100 μs

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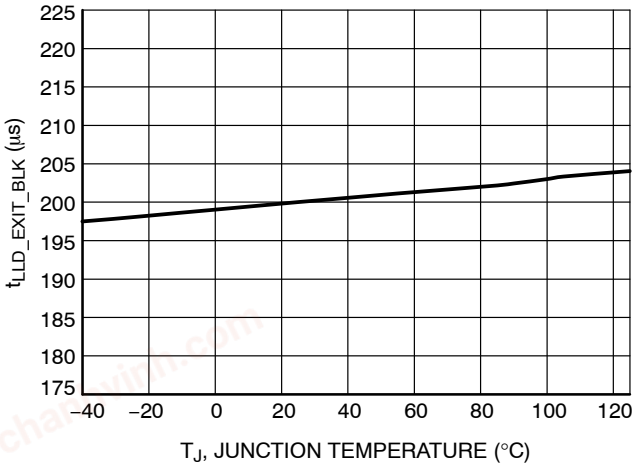


Figure 44. LLD Exit On Comparator Blank Time $t_{LLD_EXIT_BLK}$ = 200 ns

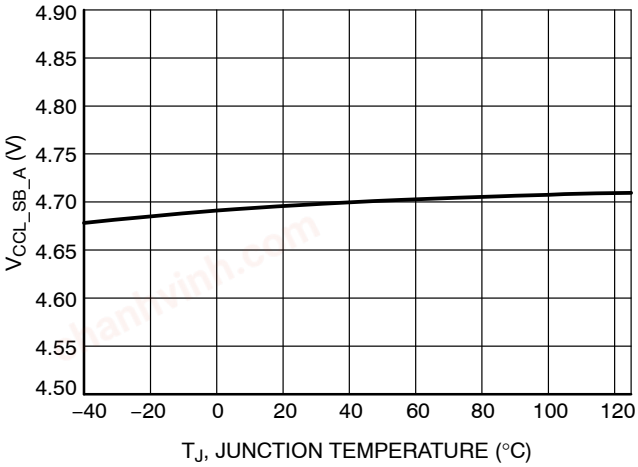


Figure 45. VCCH Current Activation Threshold $V_{CCH_SB_A}$ = 4.7 V

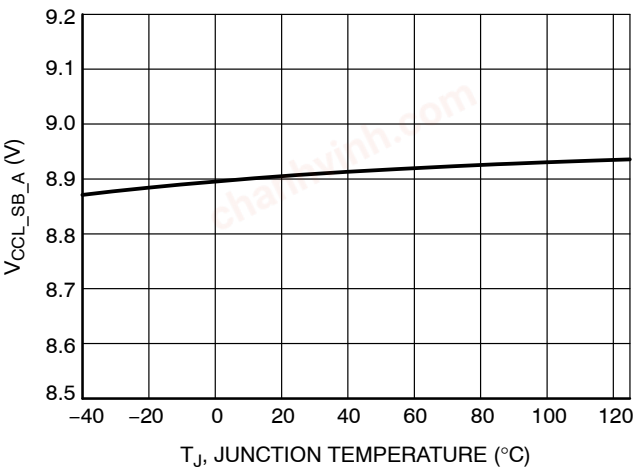


Figure 46. VCCH Current Activation Threshold $V_{CCH_SB_A}$ = 9.0 V

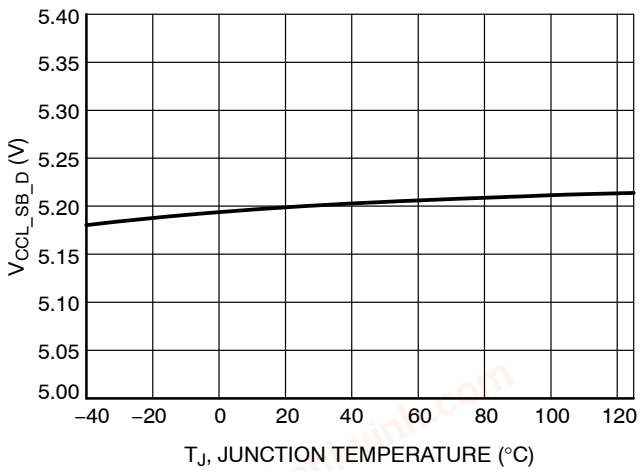


Figure 47. VCCH Current Deactivation Threshold $V_{CCH_SB_D}$ = 5.2 V

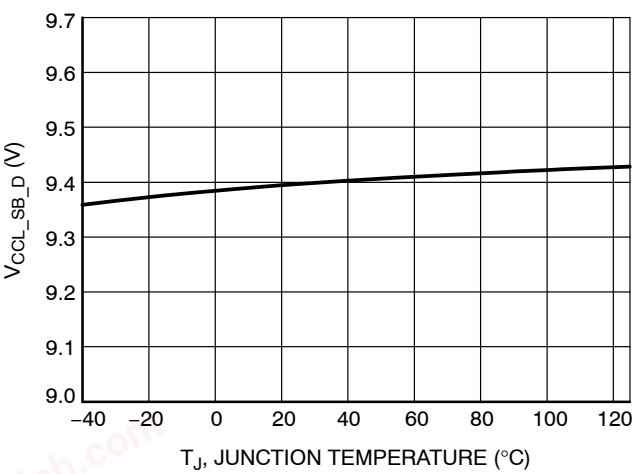


Figure 48. VCCH Current Deactivation Threshold $V_{CCH_SB_D}$ = 9.5 V

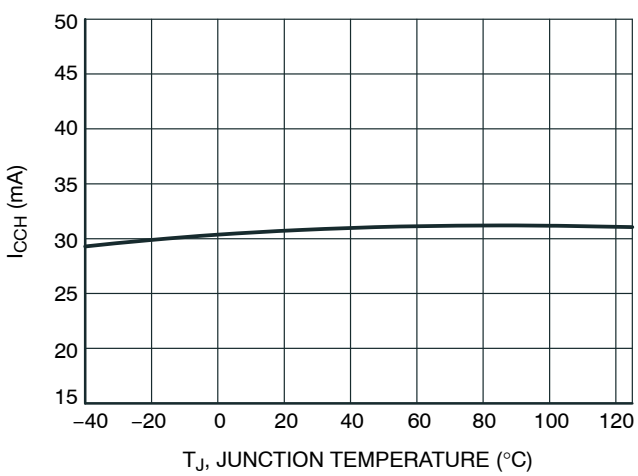


Figure 49. CCH Current to VCCL Pin, V_{CCH} = 8.0 V, V_{CCL} = 4.0 V

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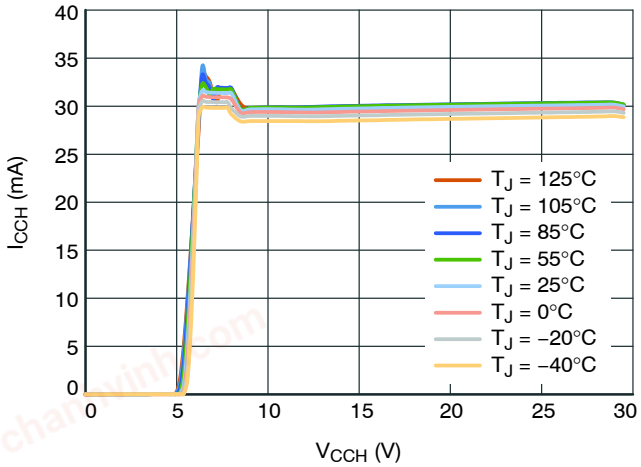


Figure 50. CCH Current to VCCL Pin, V_{CCL} = 4.0 V

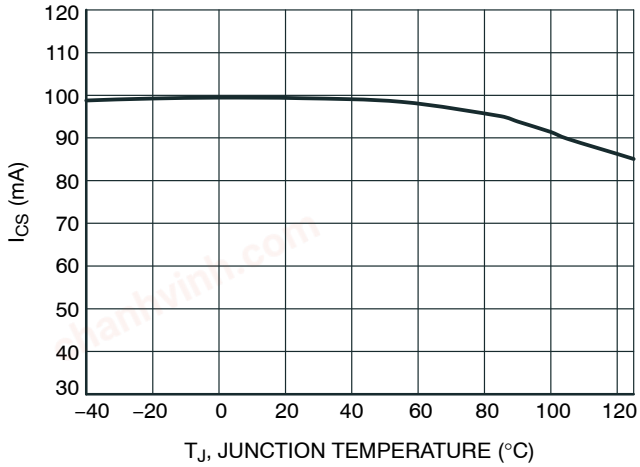


Figure 51. CS Current to VCCL Pin, V_{CS} = 50 V, V_{CCL} = 4.0 V

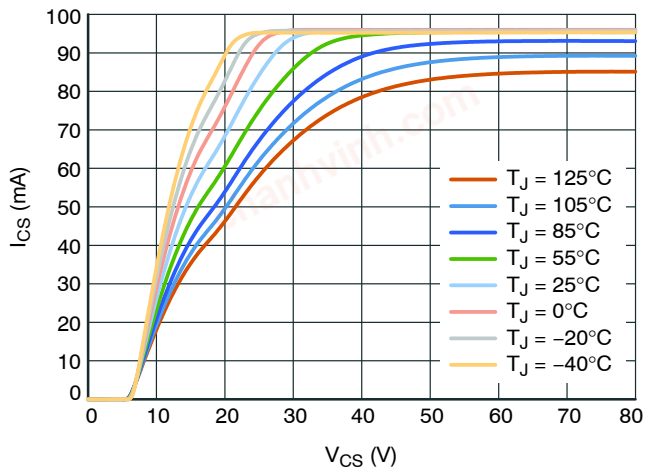


Figure 52. CS Current to VCCL Pin, V_{CCL} = 4.0 V

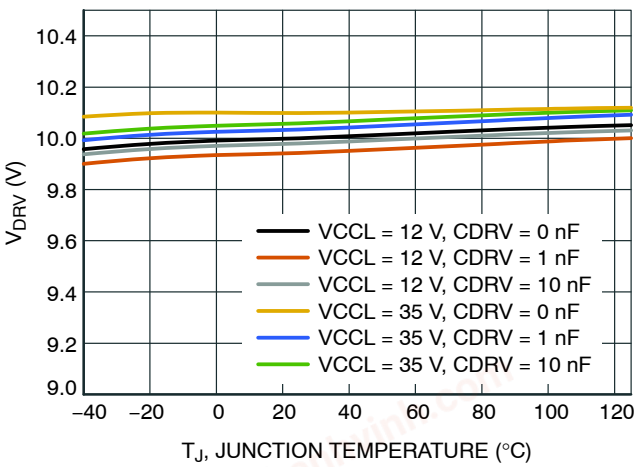


Figure 53. Driver Output Voltage, 10 V

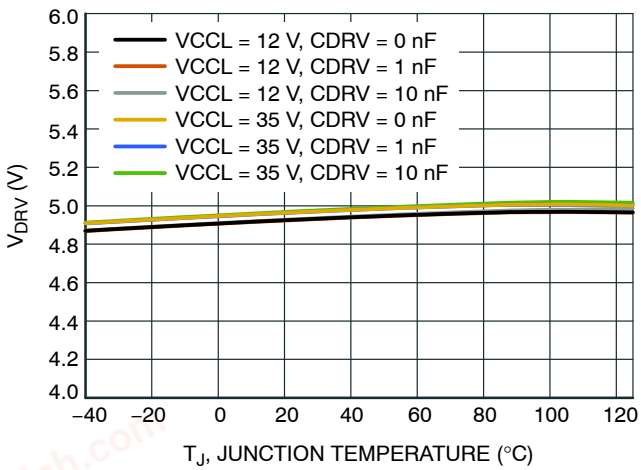


Figure 54. Driver Output Voltage, 5 V

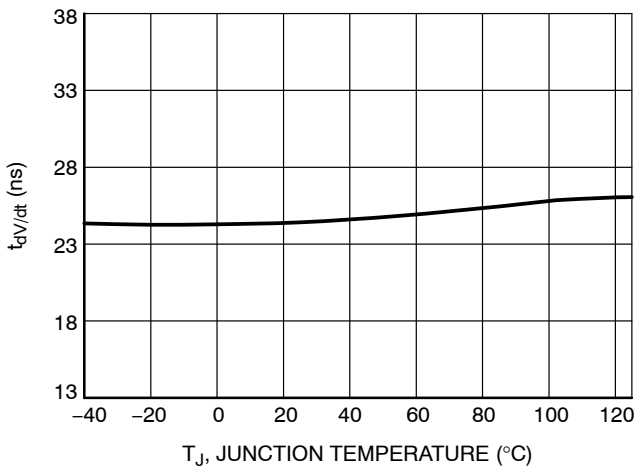


Figure 55. Negative dV/dt Detector Threshold

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INITIAL INFORMATION
APPLICATION INFORMATION

General Description

The NCP4307 is designed to operate either as a standalone IC or as a companion IC to a primary side controller to help achieve efficient synchronous rectification in switch mode power supplies. This controller features a high current gate driver along with high−speed logic circuitry to provide appropriately timed drive signals to a synchronous rectification MOSFET. With its novel architecture, the NCP4307 has enough versatility to keep the synchronous rectification system efficient under any operating mode.

The NCP4307 works from an available voltage with range from 4.0 / 3.5 V to 35 V (typical). The wide V_{CCL} range allows direct connection to the SMPS output voltage of most adapters such as notebooks, cell phone chargers and LCD TV adapters. If system offers two different voltage levels, V_{CCH} pin can be used for higher one. NCP4307 selects better voltage from V_{CCL} and V_{CCH} to minimize power consumption. Self−supply feature allows to use controller in system without suitable supply voltage that is mainly case of high side configuration.

Compared to other SR controllers that provide turn−off thresholds in the range of −10 mV to −5 mV, the NCP4307 offers a turn−off threshold of 0 mV. When using a low R_{DS_ON} SR (1 mΩ) MOSFET, our competition, with a −10 mV turn off, will turn off with 10 A still flowing through the SR FET, while our 0 mV turn off turns off the FET at 0 A; significantly reducing the turn−off current threshold and improving efficiency. Many of the competitor parts maintain a drain source voltage across the MOSFET, causing the SR MOSFET to operate in the linear region to reduce turn−off time. NCP4307 significantly reduces turn off time, allowing for a minimal drain source voltage to be utilized and efficiency maximized, thanks to the 7 A sink current.

To overcome false triggering issues after turn−on and turn−off events, the NCP4307 provides internal fixed minimum on−time and off−time blanking periods. Blanking times can be set internally during production.

An extremely fast turn−off comparator, implemented on the current sense pin, allows for NCP4307 implementation in CCM applications without any additional components or external triggering.

An ultrafast trigger input offers the possibility to further increase efficiency of synchronous rectification systems operated in CCM mode (for example, CCM flyback or forward). The time delay from trigger input to driver turn off event is t_{TRIG_PD}. Additionally, the trigger input can be used to disable the IC and activate a low consumption standby mode. This feature can be used to decrease standby consumption of an SMPS. If the trigger input is not wanted, then the trigger pin can be tied to GND (or tied to V_{CCL} in case of negative TRIG/DIS logic).

An output driver features capability to keep SR transistor turned−off even when there is no supply voltage for the NCP4307. SR transistor drain voltage goes up and down during SMPS operation and this is transferred through drain gate capacitance to gate and may open transistor. The NCP4307 keeps DRV pin pulled low even without any supply voltage and thanks to this the risk of turned−on SR transistor, before enough V_{CCL} is applied to the NCP4307, is eliminated.

Finally, the NCP4307 features a Light Load Detection (LLD) function. This function detects light load or no load conditions, and decreases current consumption during and between conduction phases. This helps to improve SMPS efficiency.

Supply Section

Supply section block diagram is shown in Figure 56. Main supply voltage pin is VCCL. Minimum voltage for proper operation is typically 4.0 / 3.5 V and maximum level is 35 V. Decoupling capacitor between VCCL and GND pin is needed for proper operation and its recommended value is 1 μF. Voltage to VCCL pin can be delivered from external power source through external diode or from VCCH or CS pin via internal current sources. Internal current sources are activated in case of low voltage at VCCL (voltage threshold depends on version). Current source from VCCH has higher priority than current source from CS pin, because of lower power loss in case of VCCH. If VCCH doesn't have enough voltage, CS current source is used. Higher capacitance of capacitor at VCCL pin is needed in case of supply from CS pin, because energy from CS is not delivered constantly, but just according to voltage situation at SR transistor drain.

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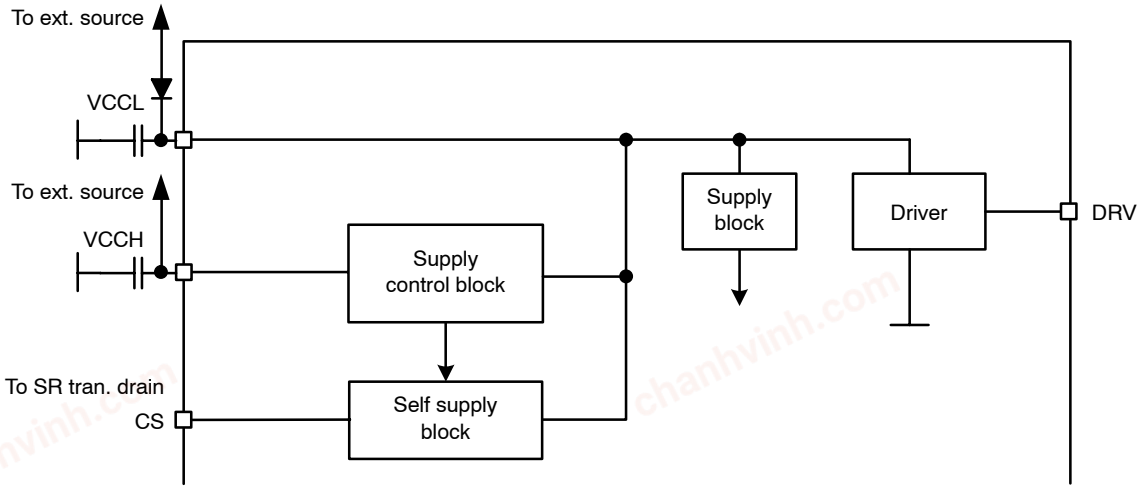


Figure 56. Supply Section Block Diagram

SR transistor is usually used in low side configuration (placed in return path), but it may be also used in high side configuration (placed in positive line). It is not possible to use SMPS output voltage for SR supply in high side configuration so it is needed to provide supply differently. One possibility is to use auxiliary winding as shown at Figure 4. It is also possible to use AUX winding with two outputs and connect it to VCCL and VCCH pins. If auxiliary winding is not acceptable, SR transistor drain voltage can be used as supply source (Figure 3). Drain voltage is used as supply source for internal current source that charges external VCCL capacitor. Operation of CS current supply block is shown in Figure 57. CS current is reduced when VCCL is low to avoid CS current block damage in case of shorted VCCL pin and when VCCL gets higher CS current gets its nominal value. Supply current is activated when CS voltage is high enough and VCCL is below $V_{CCL_SB_A}$ level. CS current is also activated for short time when V_{CS} goes high even when there is high enough voltage at VCCL pin, this is beneficial to limit voltage overshoot at SR transistor.

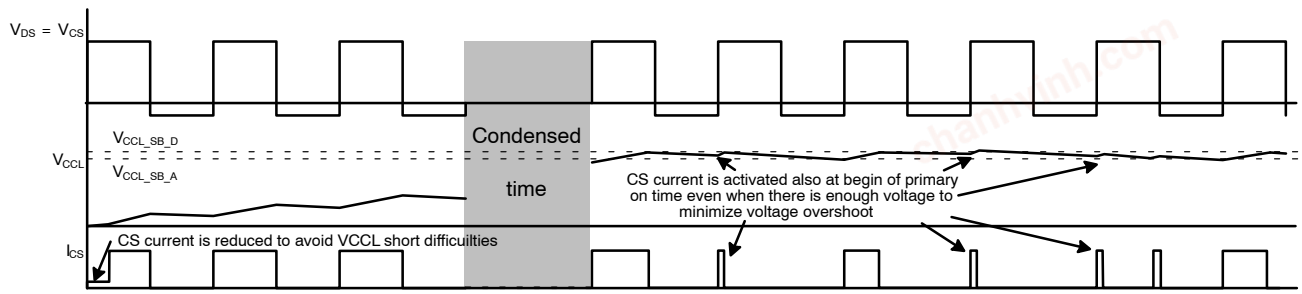


Figure 57. CS Current Source Operation

Current Sense Input

Figure 58 shows the internal connection of the CS circuitry on the current sense input. When the voltage on the secondary winding of the SMPS reverses, the body diode of SR transistor M1 starts to conduct current and the voltage of M1's drain drops to approximately −1 V. Once the voltage on the CS pin is lower than V_{CS_ON} threshold, M1 is turned−on. Because of parasitic impedances, significant ringing can occur in the application. To overcome false sudden turn−off due to mentioned ringing, the minimum conduction time of the SR MOSFET is activated.

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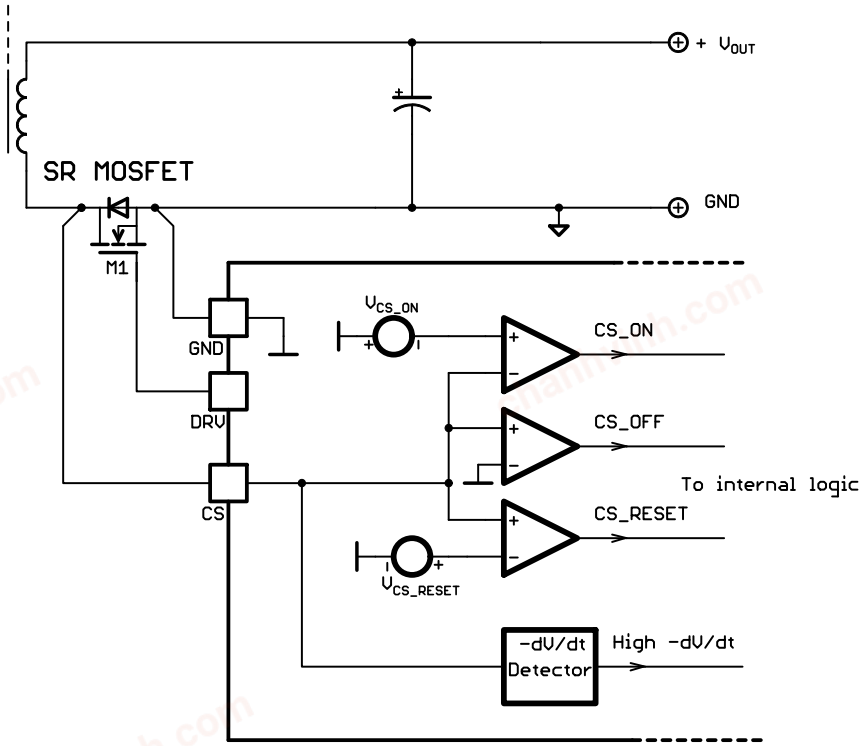


Figure 58. Current Sensing Circuitry Functionality

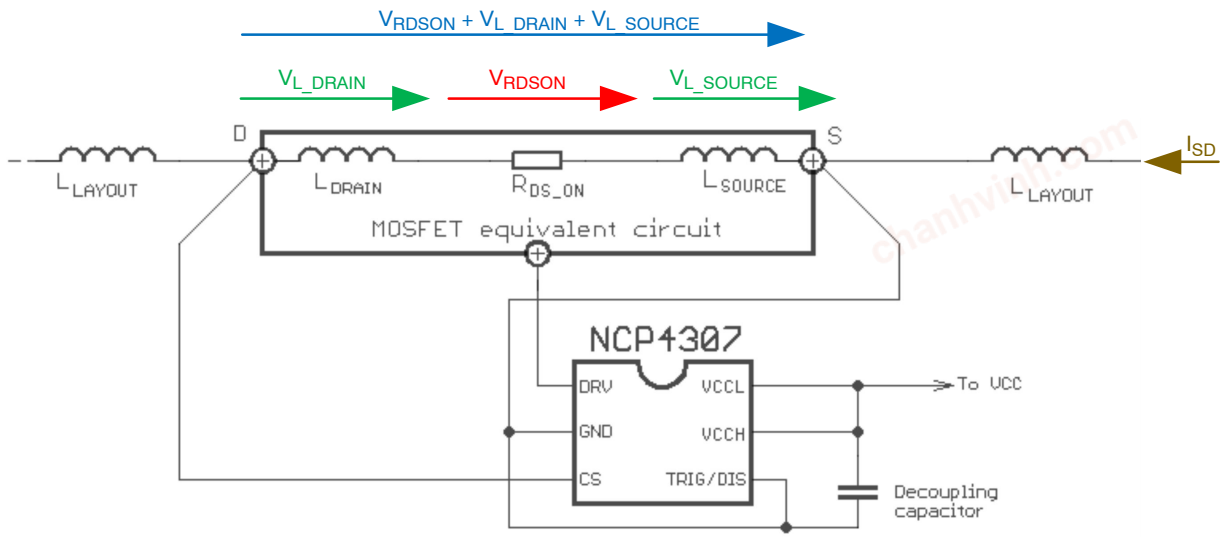


Figure 59. Current Sensing Equivalent Circuit

Sensing equivalent circuit is shown in Figure 59. SR MOSFET consists of silicon die with channel resistance R_{DS_ON} and from bonding connection to drain and source. These connections have not just resistance, but also inductance, so sensed voltage is sum of drops at all of these elements. Flyback secondary side current shape is triangular, which means it is decreasing most time of conduction phase. dI/dt of secondary current makes drop at inductive part of equivalent MOSFET circuit that is opposite to drop at resistive part. Inductive drop moves overall drop to positive values and causes SR transistor turn−off sooner than current reaches 0 A. Secondary side current also usually has ringing with very high dI/dt, that leads to positive drop at SR transistor even when there is still current in correct direction. This situation has to be solved by SR controller to avoid incorrect very early turn−off of SR transistor. Example of sensed voltages for 65 kHz flyback with parameters of SR transistor R_{DS_ON} = 4 mΩ and $L_{DRAIN} + L_{SOURCE}$ = 1.5 nH is shown in Figure 60.

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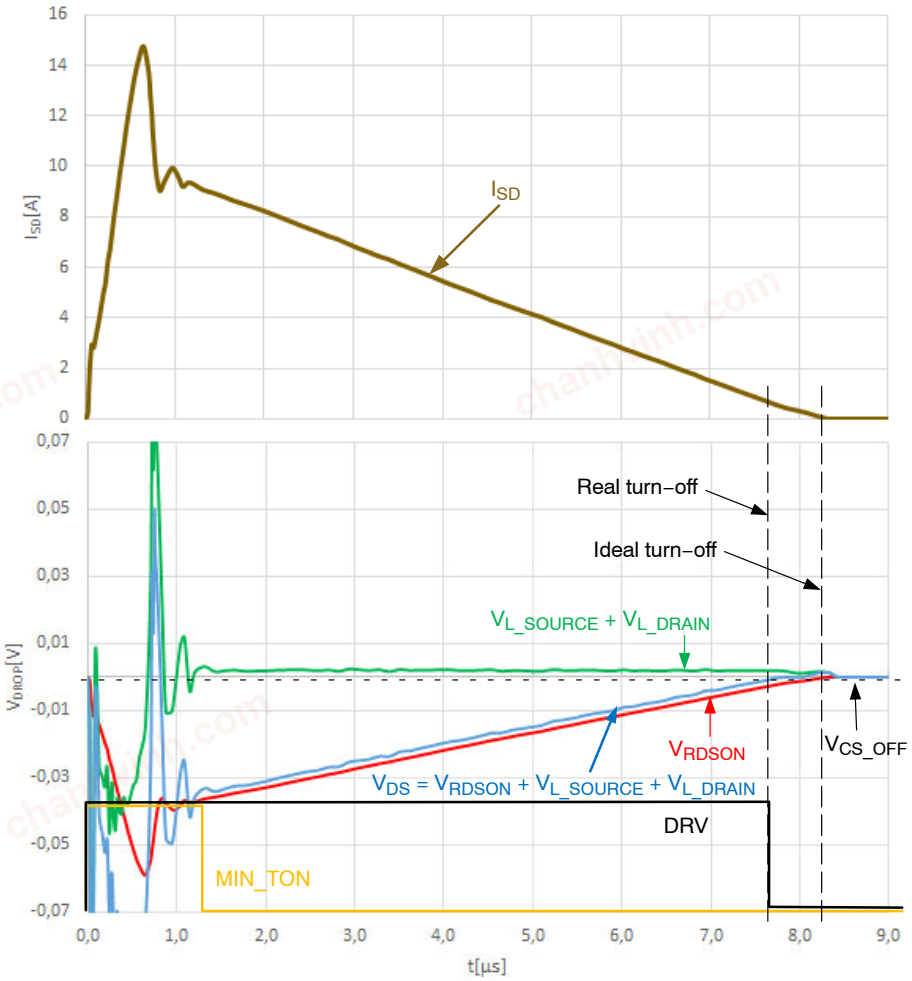


Figure 60. Drops at SR Transistor in Flyback Application

The SR MOSFET is turned−off as soon as the voltage on the CS pin is higher than V_{CS_OFF} (typically −0.5 mV). For the same ringing reason, a minimum off−time timer is asserted once the V_{CS} goes above V_{CS_RESET}. The minimum off−time generator can be re−triggered by CS reset comparator if some spurious ringing occurs on the CS input after SR MOSFET turn−off event. This feature significantly simplifies SR system implementation in flyback converters.

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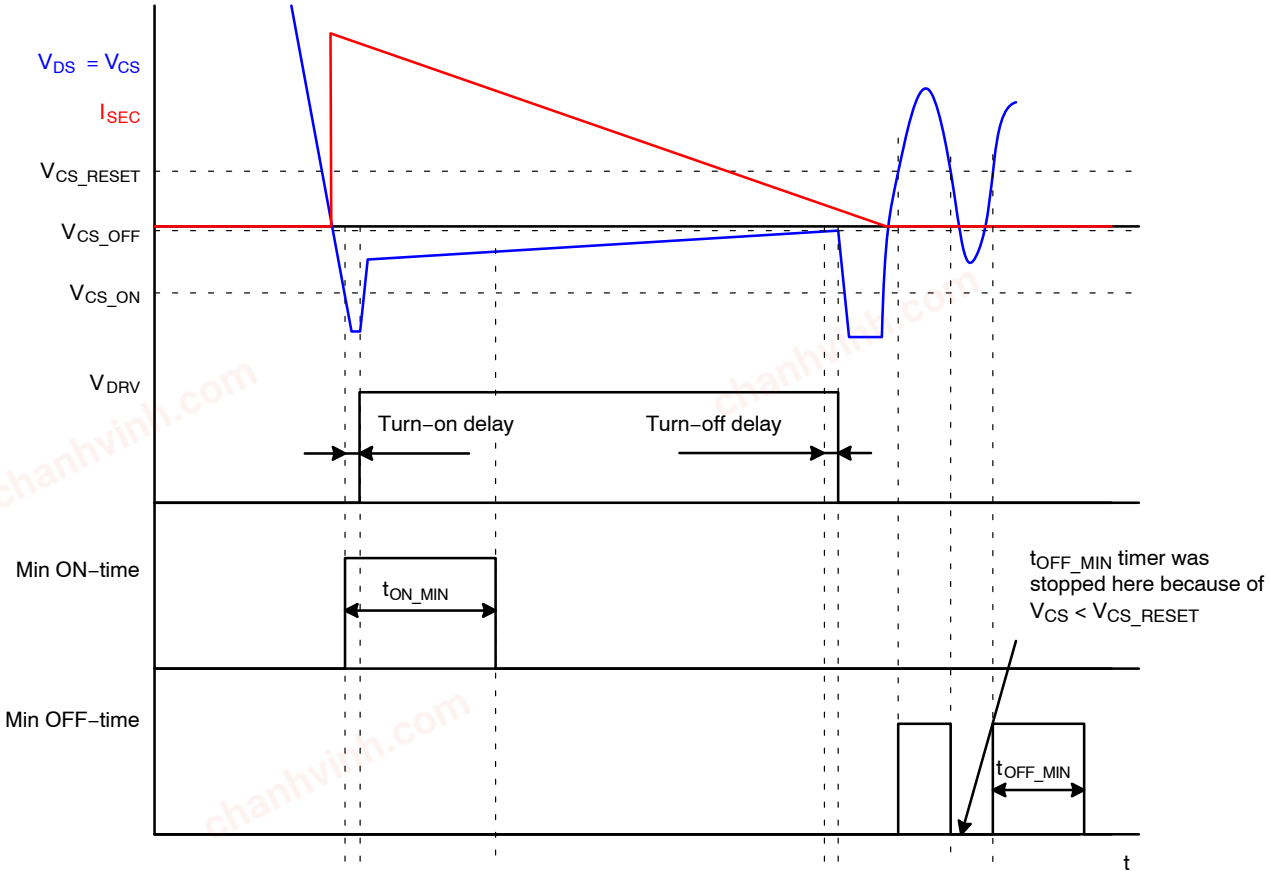


Figure 61. CS Input Comparators Thresholds and Blanking Periods Timing in Flyback

Minimum On Time Generation

Minimum on−time purpose is to blank noisy current during beginning of conduction phase to minimize risk of early turn−off of SR transistor. Off comparator is blanked during minimum on−time (except initial blank where OFF comparator is fully ignored, initial blank should cover SR transistor turn−on time) for $t_{CS_OFF_BLK}$. If CS pin voltage is above turn−off threshold for more than $t_{CS_OFF_BLK}$, SR transistor is turned−off. OFF comparator reacts within propagation delay when minimum on time elapses. Minimum on−time interval (t_{ON_MIN}) starts simultaneously with initial on blank time ($t_{ON_INIT_BLK}$) at the beginning of secondary side conduction phase. OFF comparator is fully disabled during $t_{ON_INIT_BLK}$, but it is just partly blanked during minimum on−time interval. If OFF comparator detects higher voltage than V_{CS_OFF} for shorter time than $t_{CS_OFF_BLK}$, SR transistor is kept on, but if OFF comparator stays high longer, SR transistor is turned−off. This helps with minimizing risk of negative current or cross conduction conditions.

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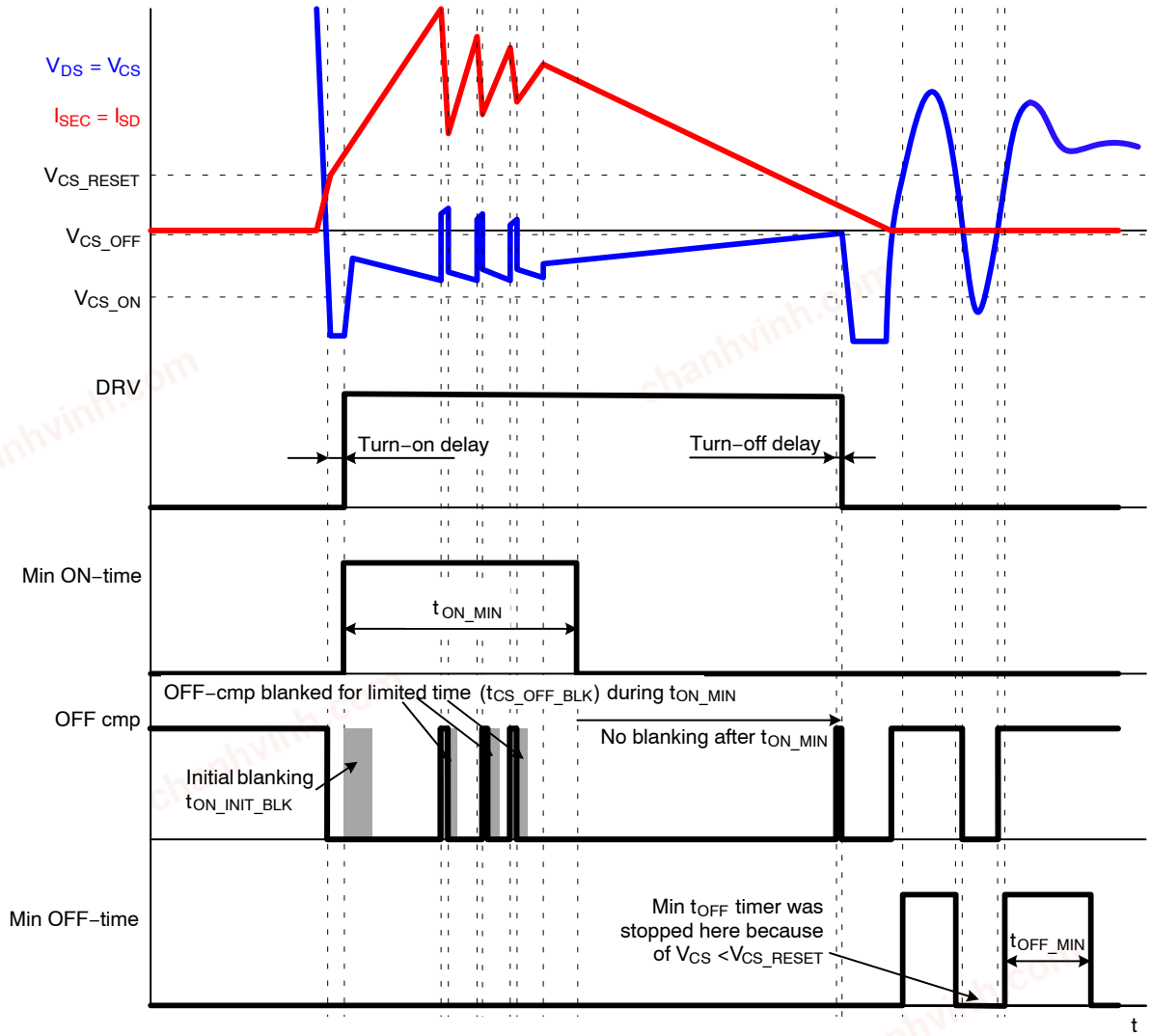


Figure 62. CS Input Comparators Thresholds and Blanking Periods Timing in Flyback

The fact that driver can be turned off also during minimum on time helps to solve reverse current issue. This means, that when current starts to flow in opposite direction for any reason (too long minimum on time, primary side turns on, etc.), driver is turned off after blank time $t_{CS_OFF_BLK}$ elapses. This significantly reduces risk and impact of shot through condition. Figure 63 shows situation when primary switch suddenly turns on during minimum on time. Driver is turned off very soon after reverse condition is detected and minimizes impact of shot through condition even when minimum on time is still running.

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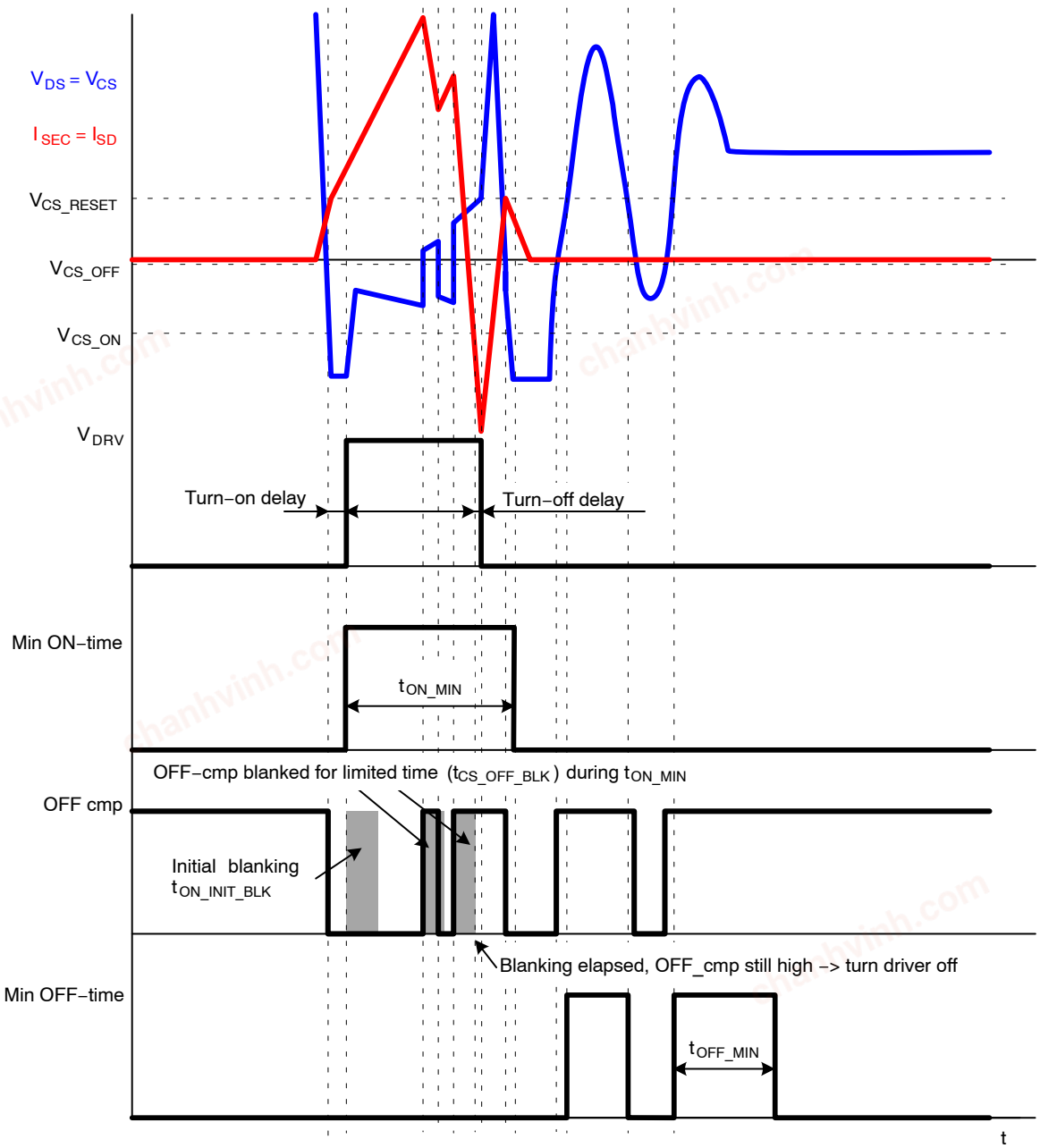


Figure 63. Driver Behavior in Case of Suddenly Turned on Primary Side Switch

Minimum on time should be set longer than current ringing takes at the beginning of conduction phase in different operation conditions. Longer than necessary minimum on time is not an issue, because the driver can also be safely turned off during the minimum on time interval, so there is no risk of deep reverse conduction or shot through event.

Minimum Off Time Generation

Main purpose of minimum off time timer is to blank ON comparator during DCM ringing at SR transistor drain after conduction phase. This ringing may take drain voltage down below V_{CS_ON} and driver may be incorrectly triggered without off timer. Off timer is started after conduction phase when CS pin voltage (SR transistor V_{DS} voltage) goes above V_{CS_RESET}. If V_{CS} drops down below V_{CS_RESET} during timer execution, timer is reset and next start is triggered by getting V_{CS} above V_{CS_RESET} (see Figure 62). This happens until minimum off time completely elapses during $V_{CS} > V_{CS_RESET}$. SR controller is then ready to turn on driver when ON comparator detects that $V_{CS} < V_{CS_ON}$. Minimum off time should be set to longer time than ringing period.

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Negative dV/dt Detection

The NCP4307 includes optional feature for flyback type converters, which operates with shorter primary on−time than ringing period after demagnetization phase during medium/high loads. These applications are for example USB−PD, Quick Charge adapters or other SMPS with wide range input and output voltage. Difficulty with this situation is that minimum off−time doesn't elapse before primary side switch is turned on and off again so SR controller doesn't turn on SR MOSFET. Whole secondary side current then flows through body diode that makes power loss. Figure 64 shows situation without −dV/dt detection. Here it can be seen that without −dV/dt detection next conduction cycle may not be taken through activated SR transistor. Reason is not elapsed minimum off−time blanking interval before next conduction cycle begins.

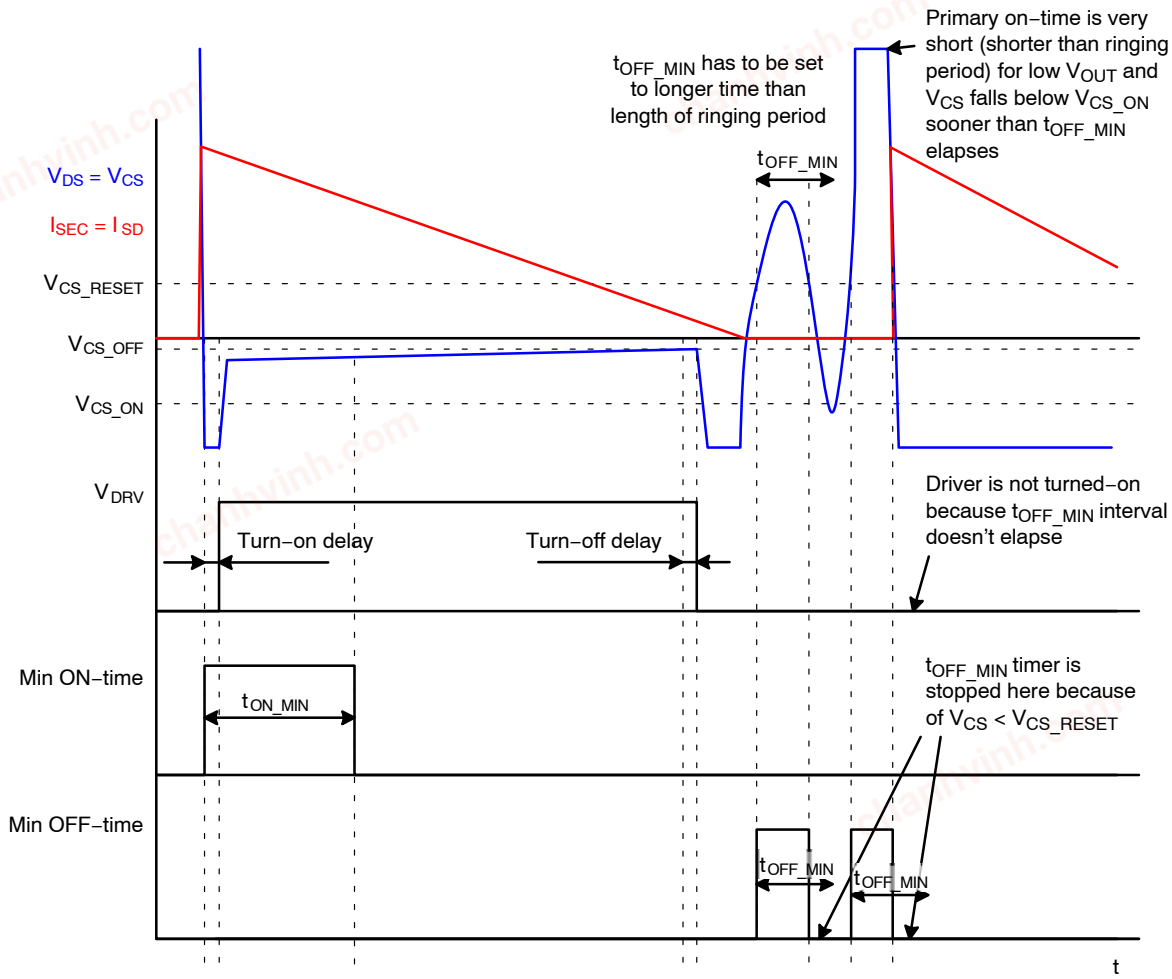


Figure 64. Situation without −dV/dt Detection Feature

Figure 65 shows how system with activated −dV/dt detection behaves. Minimum off−time blanking interval is also reset during voltage drops at CS pin, but if high negative dV/dt event occurs at CS pin, t_{OFF_MIN} interval is shorted and SR controller is ready to detect CS voltage lower than V_{CS_ON} and turn SR transistor on. Negative dV/dt at CS pin when primary low side switch is turned off is high in compare to slope that comes during ringing after demagnetization. Thanks to this we can safely differentiate end of primary on−time (and beginning of secondary side conduction period) from ringing. Negative dV/dt at CS pin is detected as time that CS voltage needs to fall from 3.0 V ($V_{CS_DVDT_H}$) down to 0.5 V ($V_{CS_DVDT_L}$). If CS voltage goes from $V_{CS_DTDT_H}$ to $V_{CS_DVDT_L}$ in shorter time than t_{CS_-DVDT}, negative dV/dt is detected.

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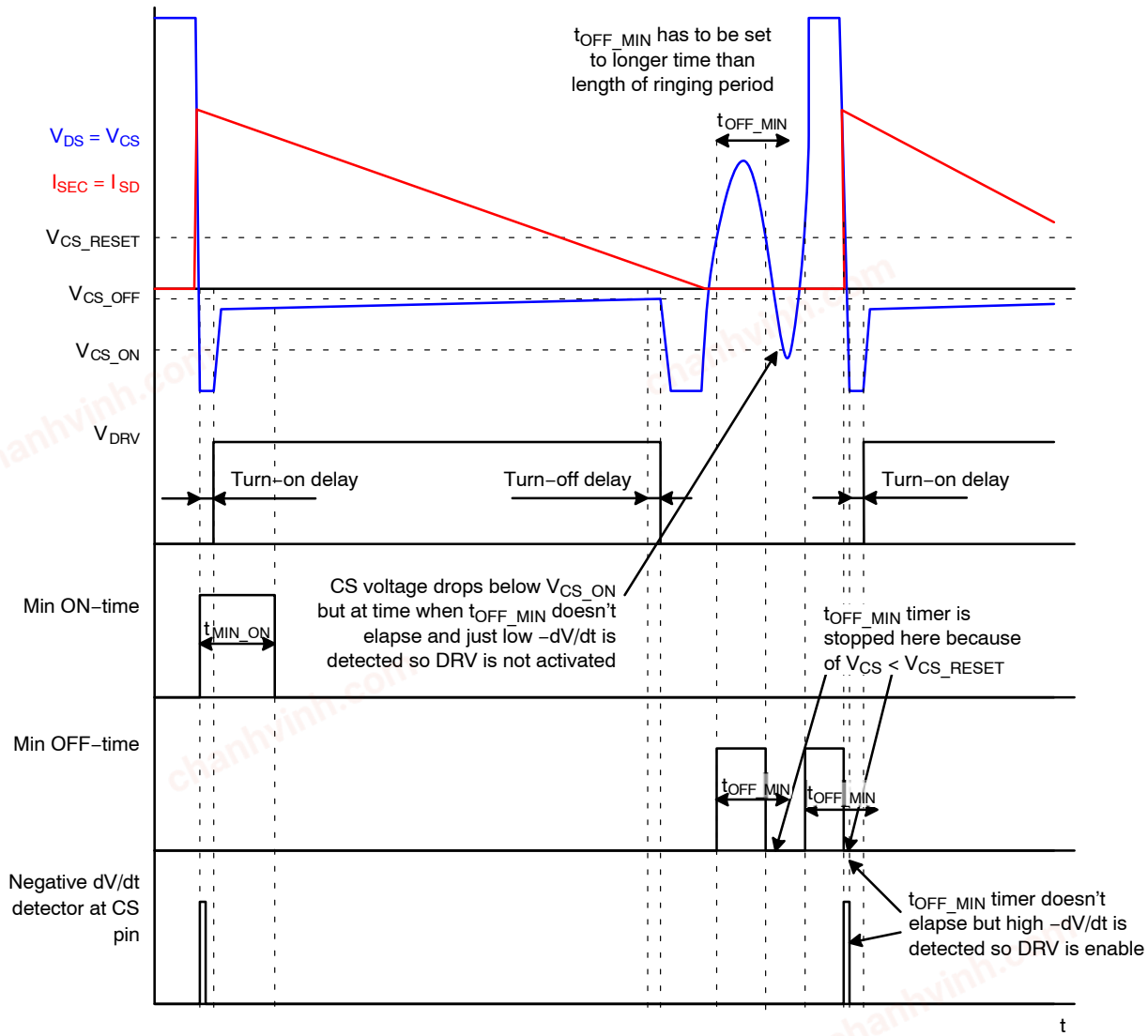


Figure 65. Situation with Enabled −dV/dt Detection

Positive dV/dt Detection

Active clamp flyback SMPS such as the NCP1568 operates in DCM (discontinuous conduction mode) at light load and in ACM (active clamp mode) during heavy load. When load is changed from light load to heavy load, the SMPS operation changes from DCM to ACM where primary high side (clamp) transistor is activated with slowly increasing on−time. This transition, often referred to as leading edge modulation (LEM), results in very difficult operating conditions for the SR controller. The main issues arise at the start of clamp transistor activation. The high side clamp transistor is turned on for very short time (low hundreds of ns) at the beginning of transition. When the clamp transistor is turned on, secondary side current flows such that the SR transistor is (can be) turned−on, because secondary side current flows from source to drain. Since the clamp transistor pulse sequence starts at 200 ns and increases in 200 ns increments the ideal minimum on time to set for the transition from ACF to DCM (LEM) would be less than 200 ns. Unfortunately, during normal operation for DCM or ACM the small minimum on time would result in poor efficiency, because necessary minimum on time for normal DCM and ACM operation is significantly longer to keep SR transistor on during current oscillations than clamp transistor on−time. Primary low side transistor is turned on soon after the turn−off of clamp transistor, which can occur while the SR transistor is still conducting. If the SR transistor is still conducting when the low side transistor turns on this can cause a cross current condition between primary and secondary side. The cross conduction decreases efficiency and increases overshoots at SR transistor V_{DS}. See Figure 65.

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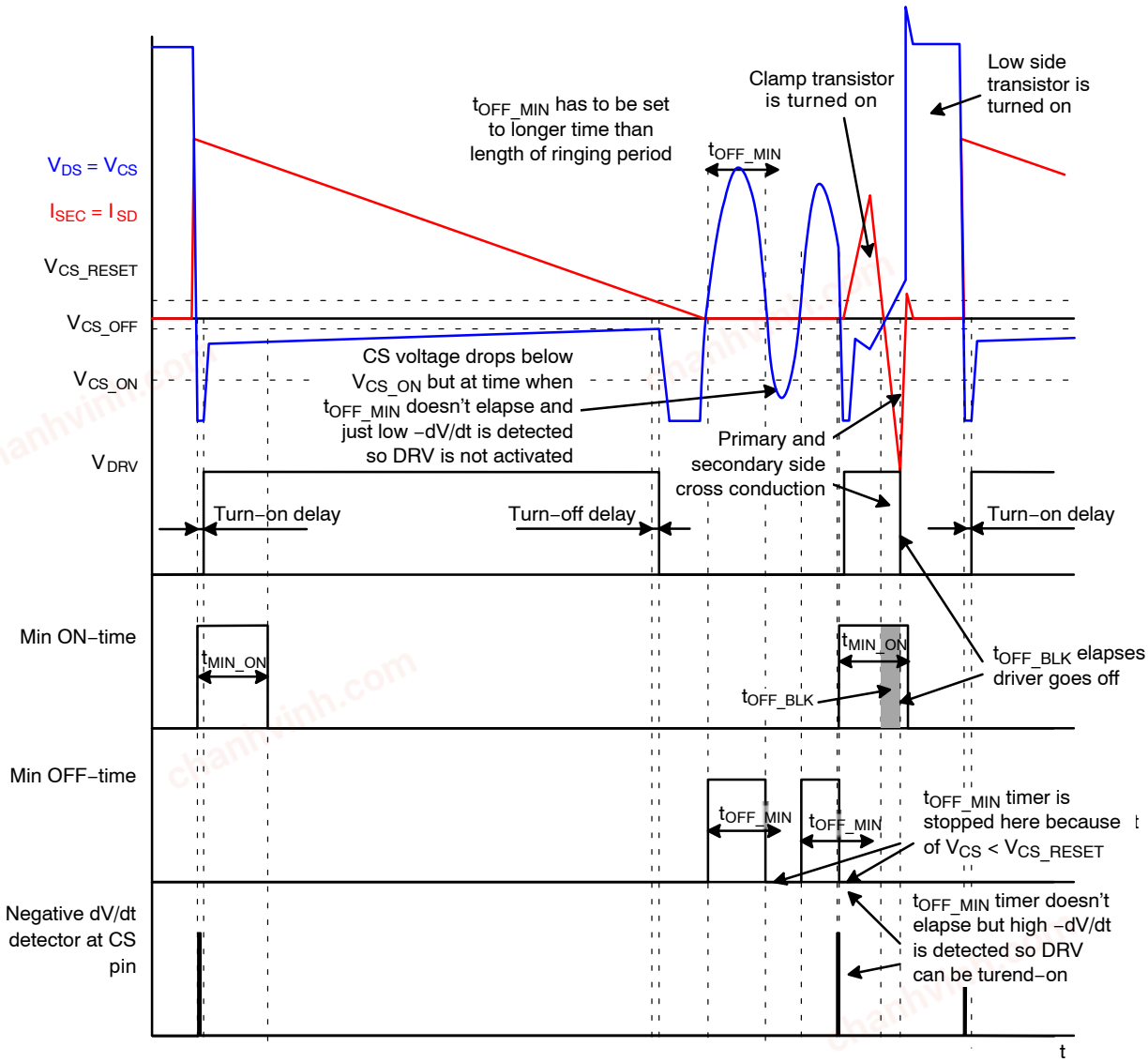


Figure 66. Situation with Disabled Positive dV/dt Detection

The SR needs to differentiate between conduction cycles on the secondary side caused by the primary clamp transistor or by the end of the primary low side switch conduction phase. A positive dV/dt detector is used to identify the LEM process. There is high positive dV/dt at the SR transistor drain voltage when primary low side switch is turned on. If high dV/dt is detected it is clear that the next SR conduction cycle will be a normal ACM or DCM operation and a long minimum on−time can be used by the SR transistor without any risk. When the SR conduction phase ends the SR controller waits again for positive dV/dt detection before it allows activation of the driver by CS on comparator. Figure 67 illustrates the activated positive dV/dt function in action.

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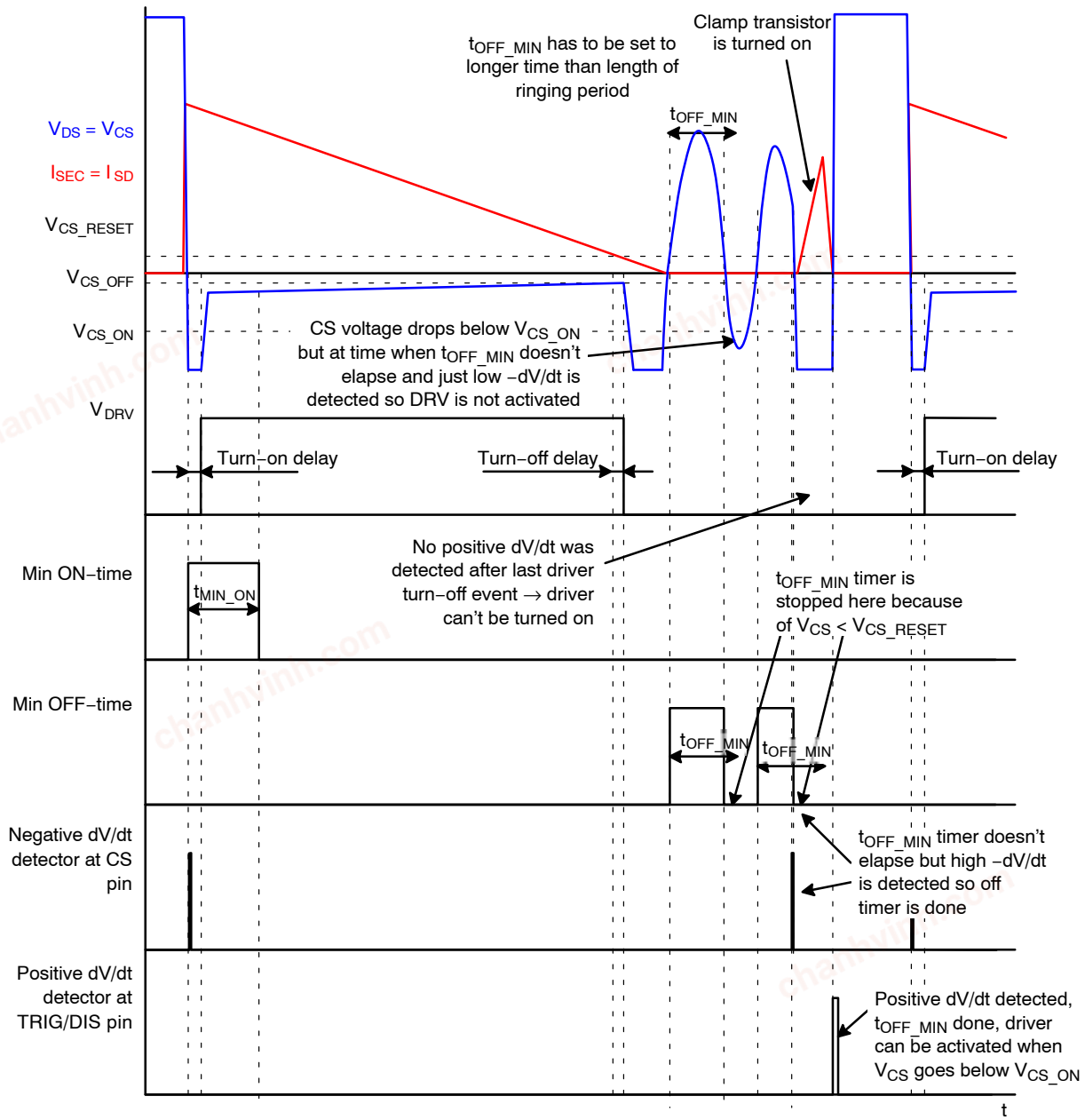


Figure 67. Situation with Enabled Positive dV/dt Detection that Fully Blocks Driver

Fully disabled driver until +dV/dt is detected may cause issue for some application in different operation conditions. No driver output then causes lower efficiency and may lead to over temperature. It may be better not to block driver fully, but it may be advantageous to allow driver to turn−on, but without full minimum on−time. Minimum on−time should be shortened just to $t_{ON_INIT_BLK}$ that minimizes risk of potential cross conduction and also even so short minimum on−time is usually enough in conditions with low dV/dt. Operation with short minimum on−time when no +dV/dt is detected is shown in Figure 68.

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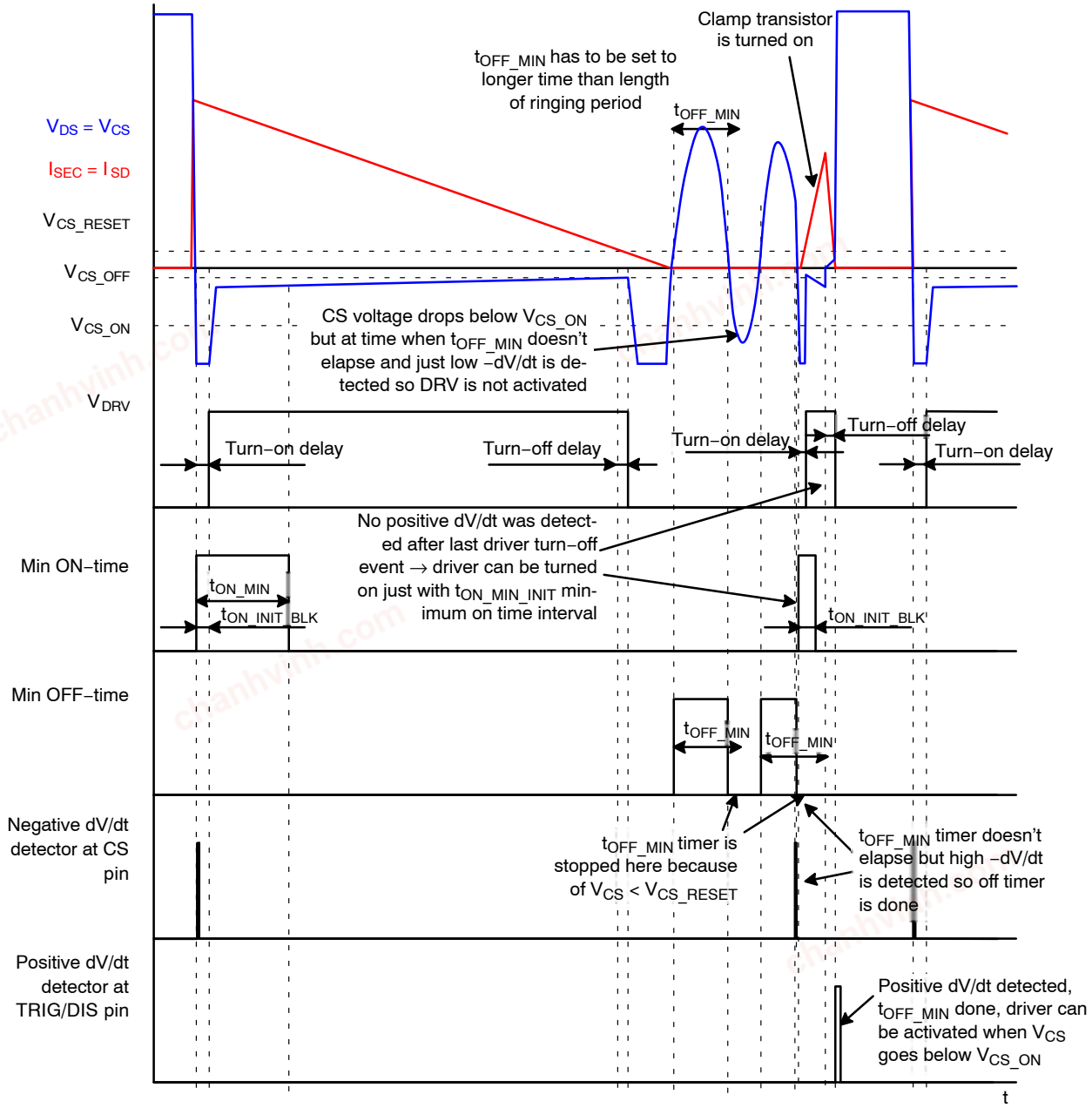


Figure 68. Situation with Enabled Positive dV/dt Detection that Shorts Minimum On−Time

Positive dV/dt is detected by external RC network connected from the SR transistor drain to the TRIG/DIS pin that has modified operation. There is a comparator at TRIG/DIS pin with V_{TRIG_DVDT} threshold. When voltage at TRIG/DIS pin crosses threshold +dV/dt flag is set that means driver can be activated when other parameters (elapsed minimum off time, V_{CS} below CS on threshold) are fulfilled.

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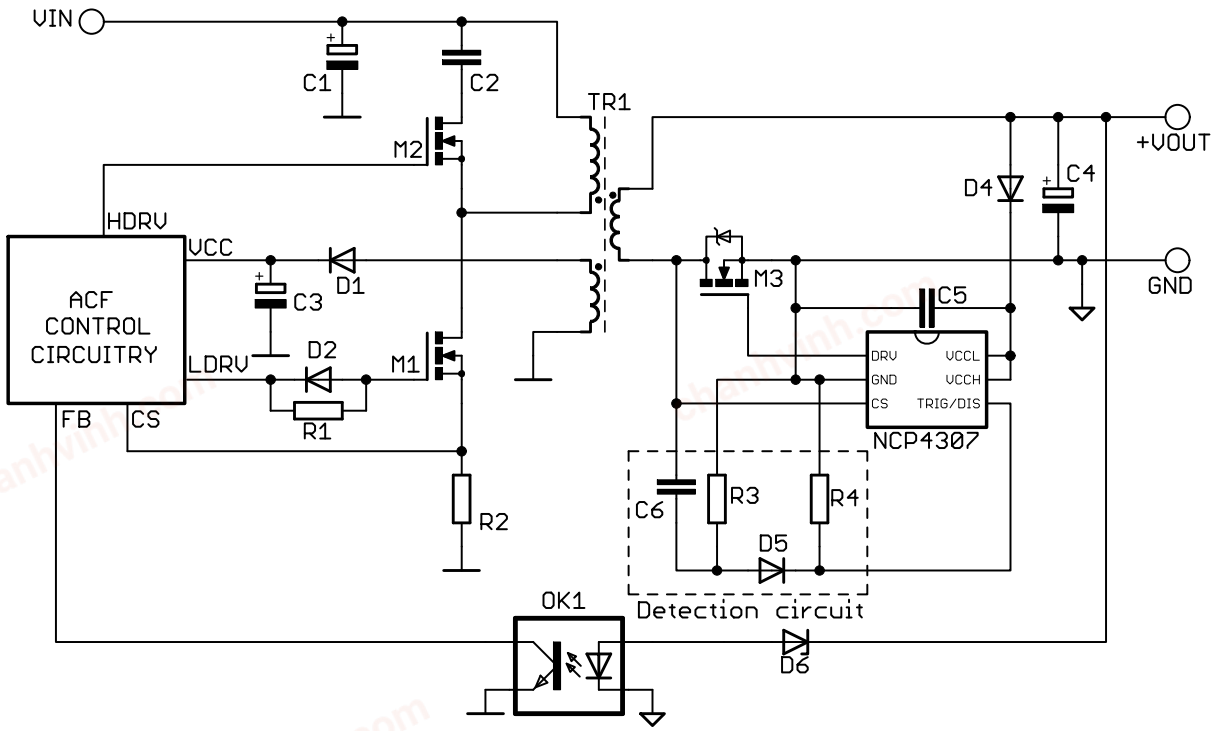


Figure 69. +dV/dt Detector Schematic in ACF SMPS (TRIG/DIS Pin Operation Changed)

Trigger/Disable Input

The NCP4307 features an ultrafast trigger input that exhibits a maximum of t_{TRIG_PD} delay from its activation to the start of SR MOSFET turn−off process. This input can be used in applications operated in deep Continues Conduction Mode (CCM) to further increase efficiency and/or to activate disable mode of the SR driver in which the consumption of the NCP4307 is reduced to I_{CCL_DIS}. Trigger pin input is mainly positive logic (active high), but specific versions may be in negative logic (active low). Please see OPN coding table for details. Following text will show and describe just positive trigger logic, negative logic works the same way just with inverted signal.

The NCP4307 is capable to turn−off the SR MOSFET reliably in CCM applications based solely on CS pin information, without using the trigger input. However, high frequency applications, with small parasitics, feature very fast and strong secondary side current changes that do not allow even for a few ns prolonging of turn off event without a cross current condition. It may be advantageous to use triggering from primary side to speed up turn−off process in these cases.

Trigger reacts normally within t_{TRIG_PD} except situation when TRIG signal comes during t_{TRIG_BLANK} interval that starts from driver turn−on event. This interval protects against false TRIG detection during SR transistor turn−on process that may be very noisy. The trigger input has higher priority than CS input except during trigger blank period. TRIG/DIS signal turns the SR transistor off or prohibits its turn−on when TRIG/DIS pin voltage is pulled above V_{TRIG_TH}.

Same pin can be used also to activate disable mode when it is pulled up for longer than t_{DIS_TIM}. Supply current is significantly reduced down to I_{CCL_DIS}. IC exits disable mode when TRIG/DIS pin goes back low below V_{TRIG_TH} at least for t_{DIS_END} time.

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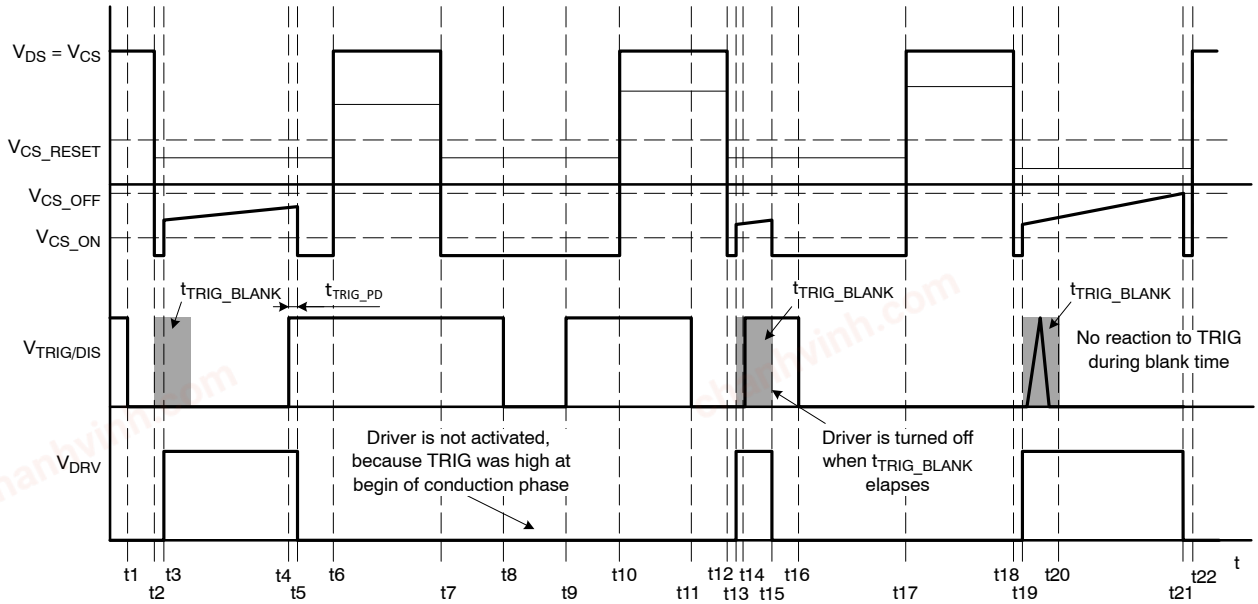


Figure 70. Trigger Input Functionality Waveforms Using the Trigger to Turn−off and Block the DRV Signal

Figure 70 shows basic TRIG/DIS pin functionality. TRIG/DIS is pulled low at time t1 for normal operation, CS pin voltage goes below V_{CS_ON} at time t2 that actives driver at time t3 (after turn on propagation delay $t_{CS_ON_PD}$). Trigger blanking starts also at time t3 that means no reaction to TRIG/DIS pin until t_{TRIG_BLANK} elapses. TRIG/DIS goes high at time t4 that causes after t_{TRIG_PD} driver turn−off event (t5) and rest of conduction period is taken through bodydiode. Next conduction cycle begins at time t7, but driver is not turned−on because TRIG/DIS pin is high. TRIG/DIS falls down at time t8 during same conduction cycle that causes no change, because driver can be turned−on just at the beginning of conduction cycle. There is also no reaction to TRIG/DIS pin rise up at time t9, because driver is off. TRIG/DIS goes low at time t11, next conduction cycle starts at t12 and driver is turned on after on propagation delay at time t13. TRIG/DIS blanking time (t_{TRIG_BLANK}) is also started at t13. TRIG/DIS goes high at t14, which is during the t_{TRIG_BLANK} period. That is why there is no reaction until blanking time elapses at t15 and driver goes low. Last example shows beginning of conduction phase at time t18, driver activation and t_{TRIG_BLANK} at t19. There is some noise at TRIG/DIS during t_{TRIG_BLANK} that has no effect on system and driver is kept on up to point t21 where V_{CS} voltage reaches V_{CS_OFF}.

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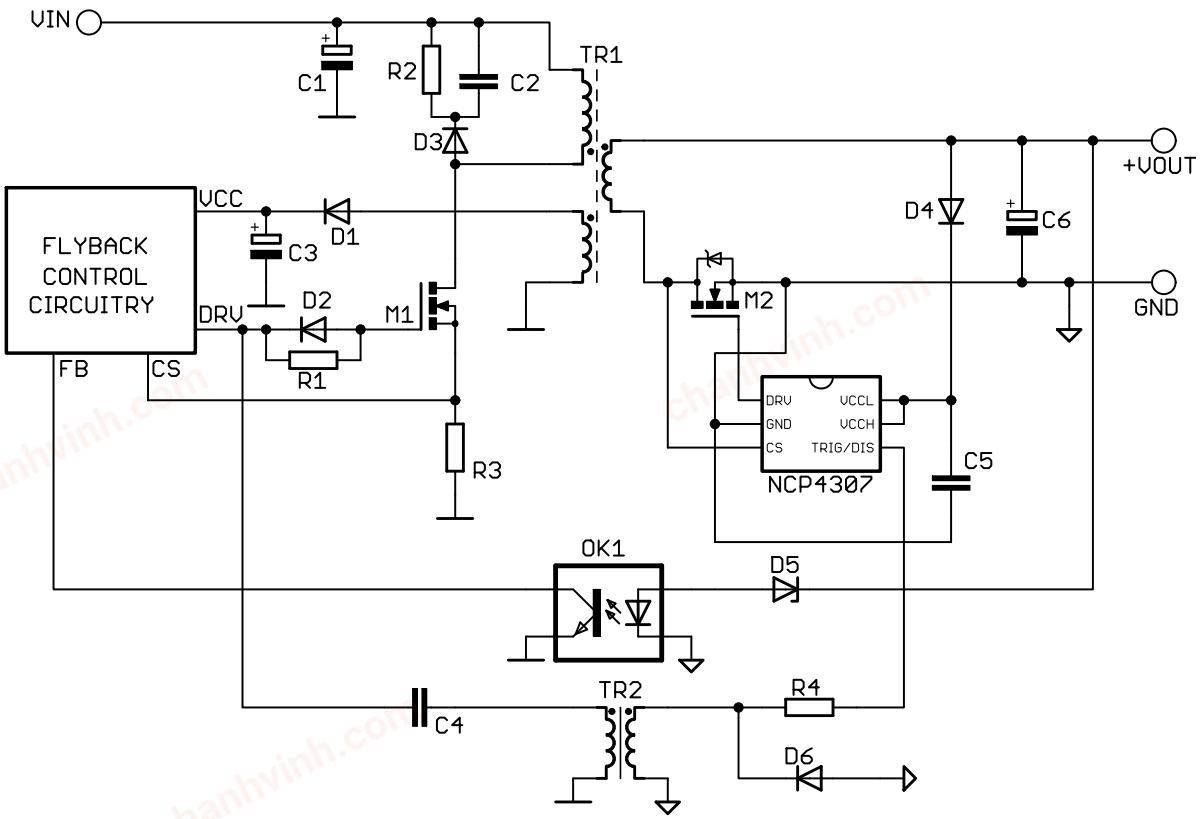


Figure 71. Optional Triggering from Primary Side through Signal Transformer

Possible usage of triggering is shown in Figure 71. If desired, the trigger can be connected with primary side via small signal transformer. Signal at primary side DRV pin comes sooner than primary transistor is turned−on (turn−on process is slowed down by gate resistor) and it goes through transformer TR2 to secondary side with almost no delay. TR2 secondary winding is connected directly to TRIG/DIS pin. SR transistor starts to turn off after propagation delay and SR transistor is turned off sooner than primary side switch is fully turned−on. This ensures no risk of cross conduction between primary and secondary side.

Continuous conduction mode (CCM) operation without triggering is shown in Figure 72. Left side shows overall operation, right side is zoomed in grey area to show timing details during turning off of the SR transistor at the end of secondary side conduction cycle. The primary side driver is activated at time t1 (blue line) that causes charging of the primary transistor gate capacitance via the gate resistor (red line). The primary transistor V_{GS} voltage gets to the threshold level around time t2 that causes start of the turn−on phase. The primary transistor V_{DS} voltage starts to decrease, secondary side current changes its dI/dt. The SR transistor drop across drain source also changes, because it is given by R_{DSON} multiplied by current level plus drop at package parasitic inductance multiplied by dI/dt and dI/dt changes significantly. That's why voltage drop measured by the SR controller seems to be positive even when there is still current that flows from source to drain (normal direction). Voltage drop across the SR transistor DS is shown in blue and its vertically zoomed level by red color. Once SR V_{DS} crosses V_{CS_OFF} (time t2) SR controller detects turn−off event and starts to turn−off driver after propagation delay at time t3. Turn off process takes t_F to time t4, where gate voltage drops below threshold. Turn−off process is done sooner than secondary side current falls below 0 A and changes it direction so there is no cross current condition in properly set system. Secondary side current goes negative little bit, because it is needed to charge transistor output capacitance and other parasitics. This also causes some overshoot at SR transistor V_{DS}. Properly set system can be identified by simple test, check CCM operation waveforms with activated SR controller and compare them to waveforms with disabled SR controller (TRIG/DIS pin held high). Secondary side current waveform and the SR transistor V_{DS} waveform should be similar in both cases.

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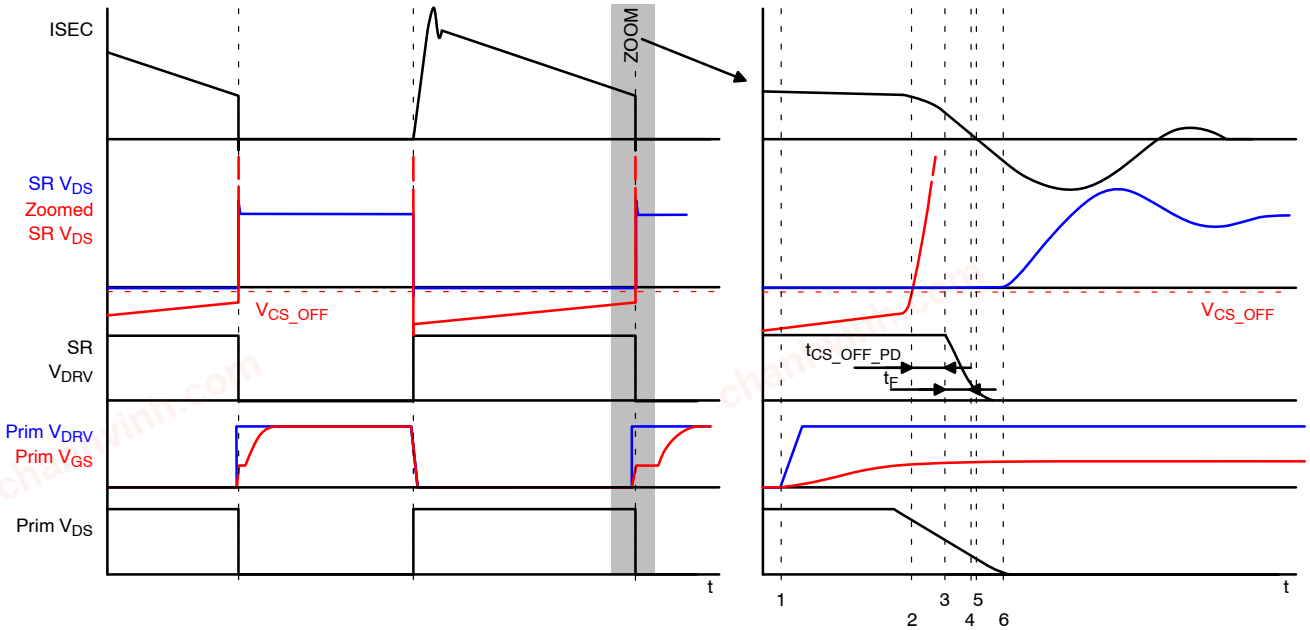


Figure 72. CCM Operation without Triggering from Primary Side

Operation waveforms for CCM system with triggering from primary side are shown in Figure 73. Figure is done similarly as previous one, there is just added TRIG/DIS signal that comes from primary side through signal transformer like is shown in Figure 71. This signal comes from primary DRV pin with short delay to secondary side TRIG/DIS pin. When the TRIG/DIS voltage rises above V_{TRIG_TH} (time t2) the SR controller starts with turn−off process after propagation delay t_{TRIG_PD} at t3. SR transistor is practically turned−off at time t4, when its gate voltage drops below $V_{GS(TH)}$. This happens sooner that secondary side current changes its direction, so rest of the conduction phase up is taken by transistor's bodydiode. Optional solution with triggering turns SR transistor off sooner than without it, which gives more confidence, that there will be no cross current condition and that there will be long enough deadtime between SR turn−off and primary on time.

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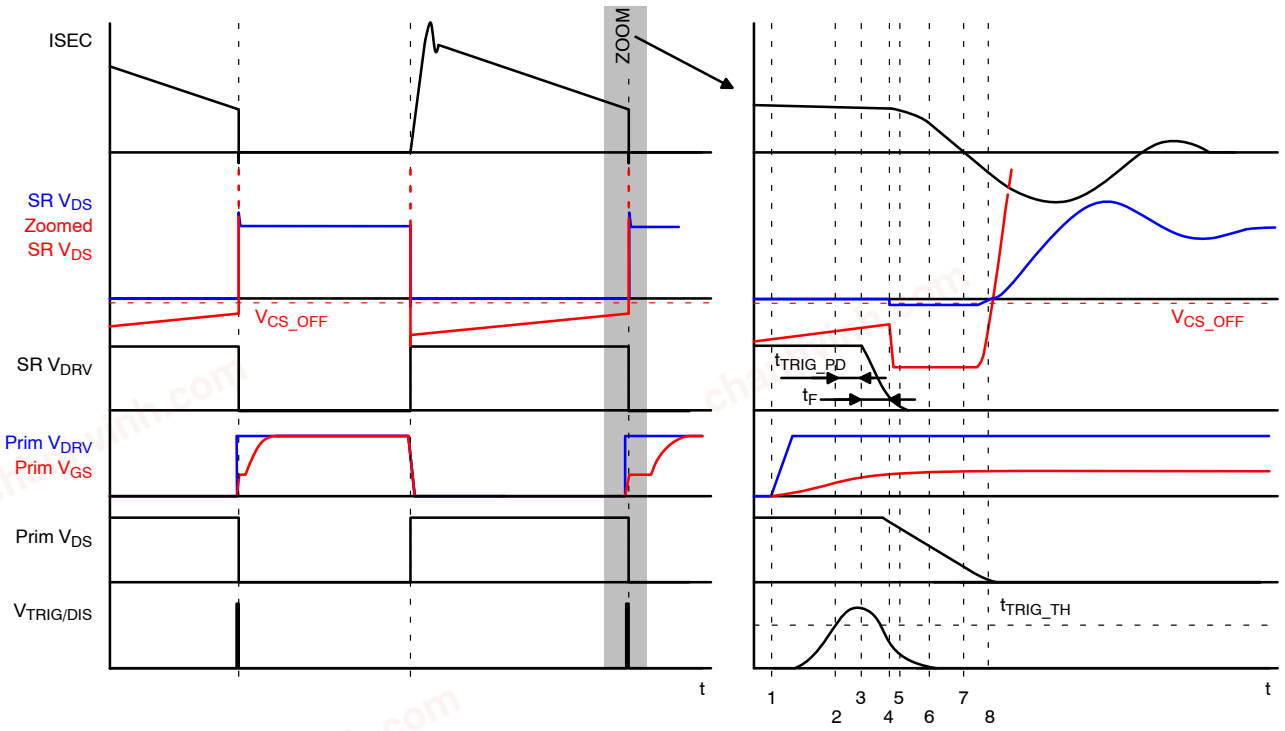


Figure 73. CCM Operation with Triggering from Primary Side

The TRIG/DIS pin allows to send IC into disable mode by pulling this pin up for more than t_{DIS_TIM}. Pulling pin up disables SR operation and significantly decreases current consumption. Disable mode activation is shown in Figure 74. The TRIG/DIS pin goes high at t3, driver stays low from that time and after t_{DIS_TIM} (at t4) disable mode is activated.

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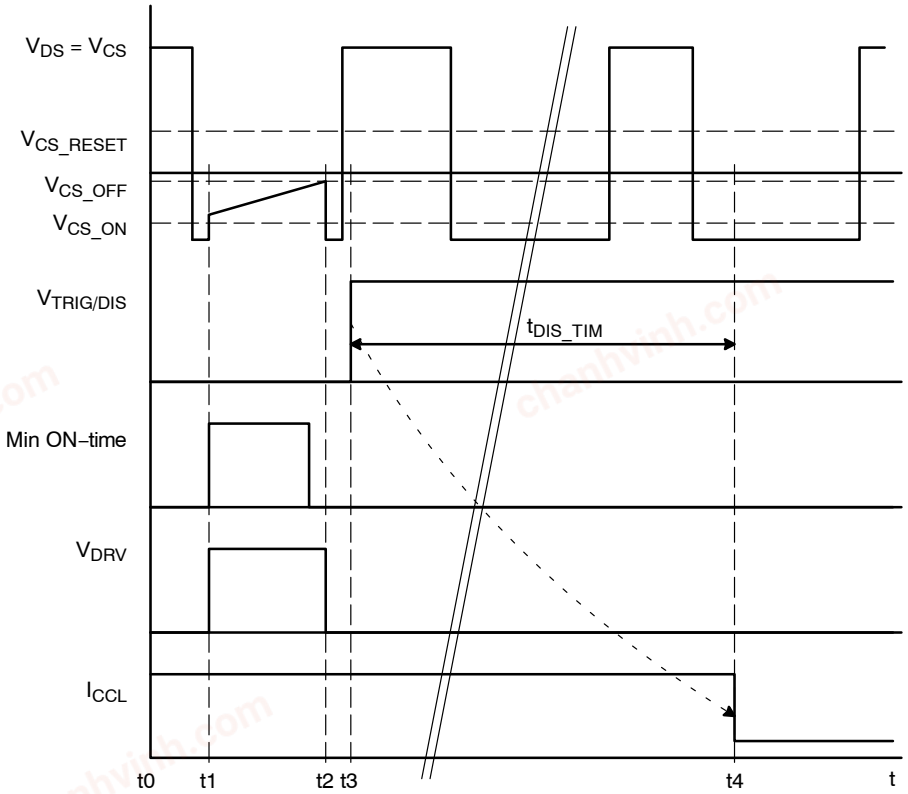


Figure 74. Disable Mode Activation by TRIG/DIS Pin

The disable mode is ended when the TRIG/DIS pin voltage falls below V_{TRIG_TH} for more than t_{DIS_END}. There is recovery phase where internal references are stabilized that takes t_{DIS_REC}. Recovery phase is finished at t3. The SR controller starts synchronization phase where it waits for V_{CS} to get above V_{CS_RESET} for more than t_{OFF_MIN} or for negative dV/dt detector trigger. Picture shows situation with disabled negative dV/dt detector, in case of enabled −dV/dt, controller turns driver on at t4 (high enough −dV/dt is detected).

Trigger Blocking Option

The trigger input can be changed to different function. The trigger keeps state machine at state “Waiting for CS_ON” when is triggered at TRIG pin (high for positive logic setting and low for negative logic pin setting). TRIG signal operates normally during time when driver is turned on. The trigger signal has to be well synchronized to the primary side otherwise there is a risk of losing synchronization and improper SR transistor control. Target of this feature is SR controller driving the SR transistor at position of forward diode in forward convertor.

Secondary side of forward converter is shown in Figure 75.

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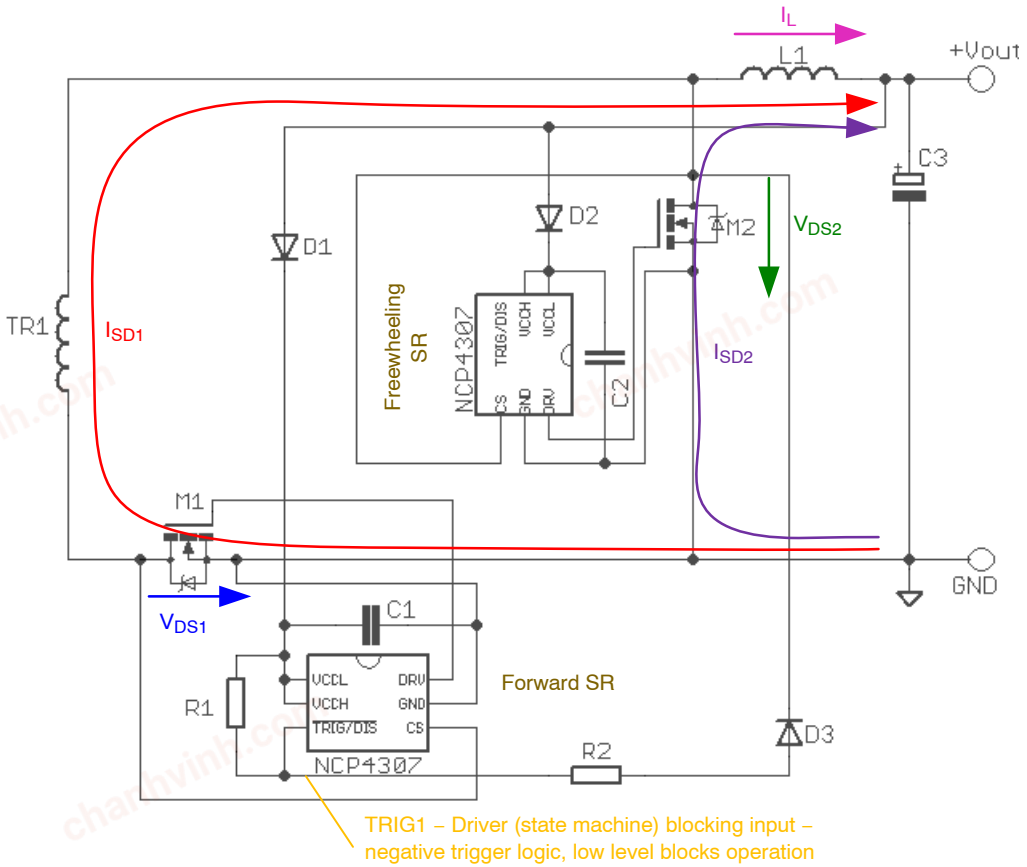


Figure 75. Secondary Side of Forward Converter with SRs

Operation with two similar SR controllers without trigger blocking function is shown in Figure 76. Difficult situation may appear when a transformer is demagnetized sooner than a freewheeling conduction period ends, because part of a freewheeling current may start to flow through a forward diode and a secondary transformer winding. This situation activates the forward SR controller that turns on the SR transistor (current flows in correct direction). A minimum on−time blanking interval may elapse sooner than real forward conduction cycle begins. This causes an issue, because there is noise during this reconfiguration that can trigger the forward SR controller off comparator. The SR controller has to turn its driver off, because its off comparator is not blanked after the minimum on−time blanking interval ends. Rest of the forward conduction cycle is taken through the SR transistor bodydiode with high power loss.

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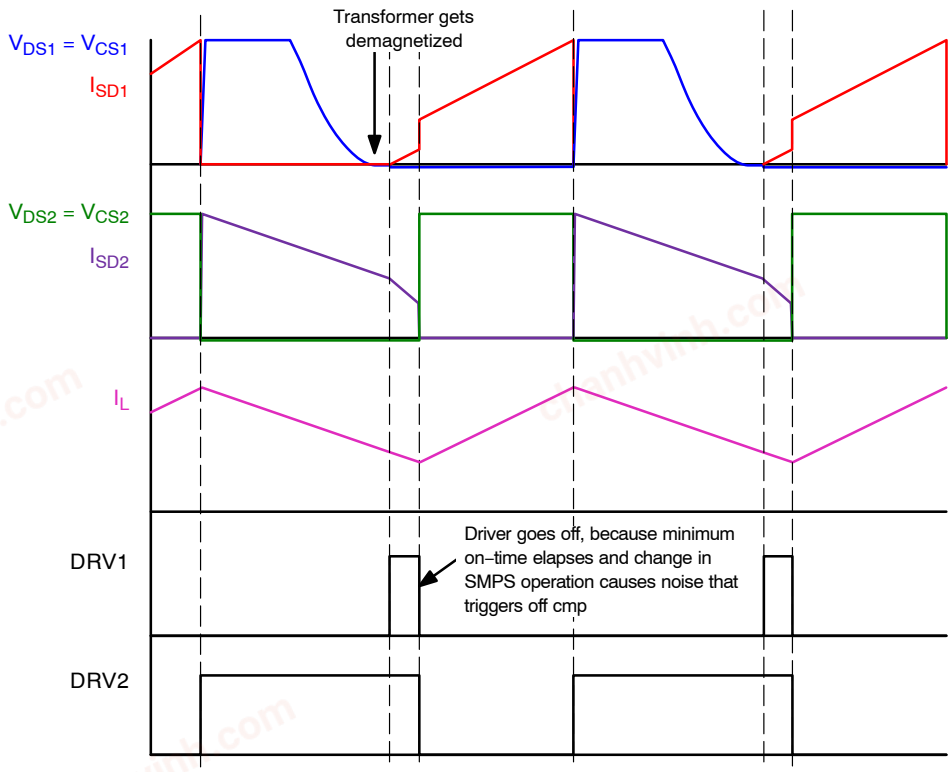


Figure 76. Operation without Trigger Blocking Option at Forward Position

The situation can be solved by the trigger blocking function that doesn't allow the forward SR driver to be activated until the freewheeling conduction ends. Forward SR controller has set trigger blocking function with negative logic (high level – controller enabled, low level – controller blocked) for easier implementation. Pin is connected via diode (to minimize risk of the TRIG/DIS pin damage by high voltage) to drain of the freewheeling SR (if a diode rectifier is used instead of a SR, use rectifier's cathode voltage). Freewheeling drain voltage is low whenever current flows through freewheeling SR. Improved behavior is shown in Figure 77.

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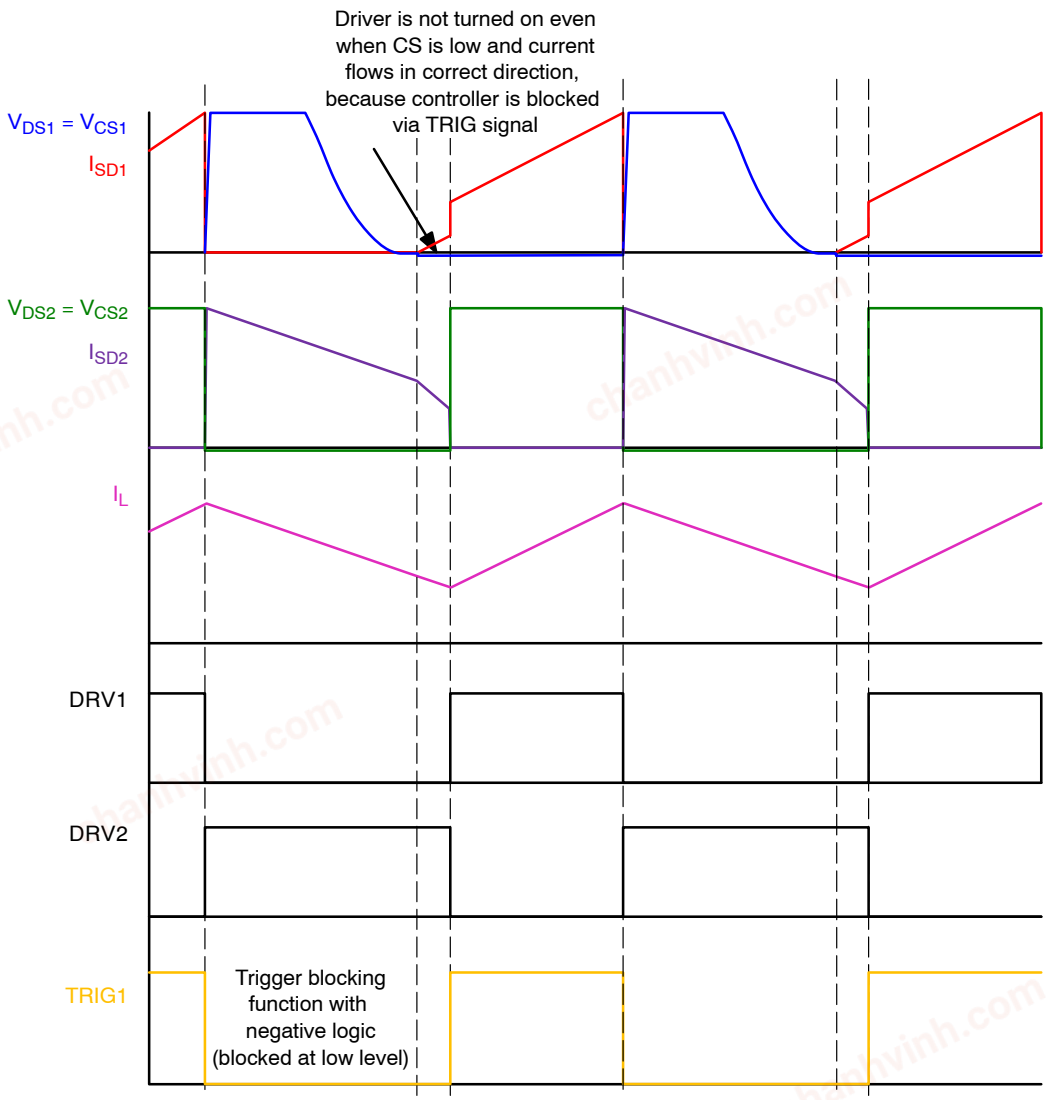


Figure 77. Operation with Trigger Blocking Option at Forward Position

Light Load Detection

Internal light load detection is tailored to detect no or light load condition and lower power consumption of the SR during this conditions. CS pin signal is used to detect if there is a light load condition or not. A light load is detected in case when there is the V_{CS} above the V_{CS_LLD} for more than t_{LLD}. A current consumption is reduced to I_{CCL_LL} during the light load mode. The light load mode is ended when the CS voltage goes below V_{CS_LLD}. The IC needs t_{LLD_REC} time to recover from the light load mode, to establish voltage references etc. The first driver pulse after the light load mode pulse is generated just in case that the V_{CS} is below V_{CS_ON} for more than $t_{LLD_EXIT_BLK}$. Reason for this is that a primary voltage clamp is discharged during long no switching time and part of the first pulse energy is used to recharge it instead of going to the secondary side so there is long and deep ringing that would cause longer period when $V_{CS} > V_{CS_OFF}$ than $t_{CS_OFF_BLK}$ and the driver will be incorrectly turned immediately off. Ringing elapses when $V_{CS} < V_{CS_ON}$ long enough so the driver can be activated without any risk. Figure 78 shows typical behavior of the LLD circuit in flyback application. The SR controller is in normal mode from time 0, the driver is activated according to the secondary side conduction phase, and current consumption is I_{CCL_Q} plus short peaks caused by charging the SR MOSFET gate charge. V_{CS} stays above V_{CS_LLD} from time 1, because skip mode was activated (no switching at primary side). t_{LLD} is running from time 1 and elapses at time 2. The light load mode is activated at time 2 that means decrease of current consumption down to I_{CCL_LL}. The controller stays in the light load mode up to time when V_{CS} falls below 0 V (time 3) that starts a wake up process. This part is showed in detail in Figure 79. The wake−up process takes approximately t_{LLD_REC} and ends at time 4 during which current consumption returns back to I_{CCL_Q}. The controller now waits for signal from the CS on comparator (threshold V_{CS_ON}) that takes longer than $t_{LLD_EXIT_BLK}$ (blank interval is showed by grey box or dimensions). There

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are two high level outputs from the CS on comparator that are shorter than $t_{LLD_EXIT_BLK}$ so no action is taken by the driver, the third pulse is longer than $t_{LLD_EXIT_BLK}$ that leads to the driver turn−on at time 9. There are just 2 pulses in this skip burst that ends at time 10. The LLD timer elapses at time 11 and the light load mode is activated again.

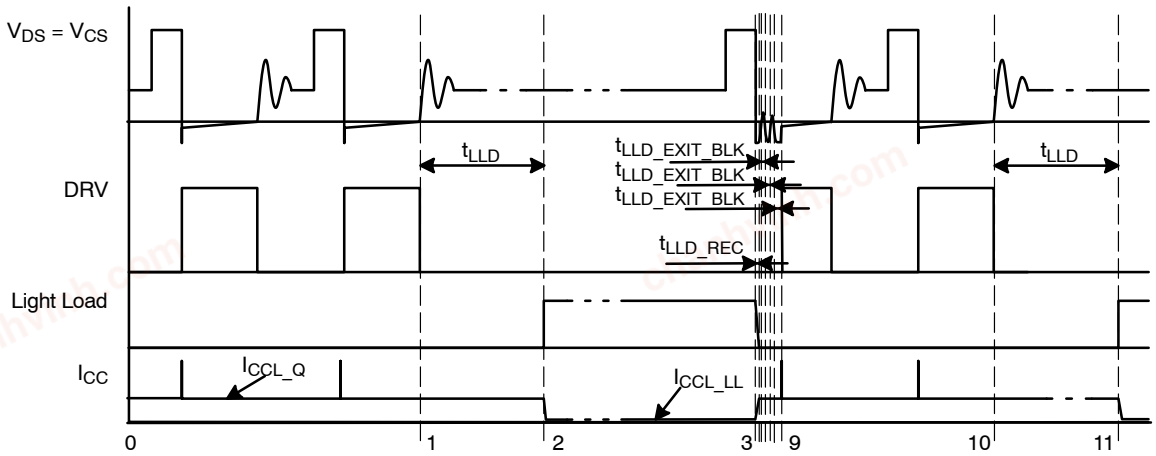


Figure 78. Light Load Detection Waveforms

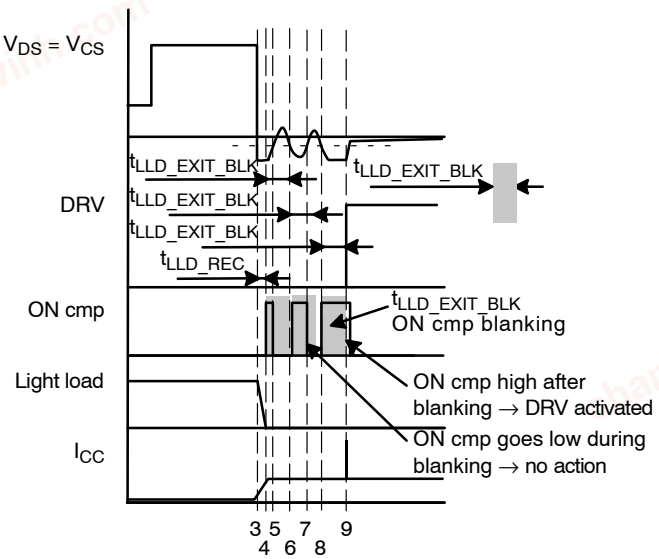


Figure 79. Light Load Detection Waveforms – Detail of LLD Exit

Operation Flow

Following bubble diagram at Figure 80 shows overall operation flow. Black bubbles are fundamental parts of the system. States for −dV/dt feature are colored by blue color, states for minimum on time generation are in red and states for +dV/dt are green. The trigger blocking option is in violet color. There are two operation options of blocking function and just one of them can be active at same time. Operation starts in the bubble start where the system comes when VCCL is higher than UVLO level and/or the disable mode is activated (by the TRIG/DIS pin).

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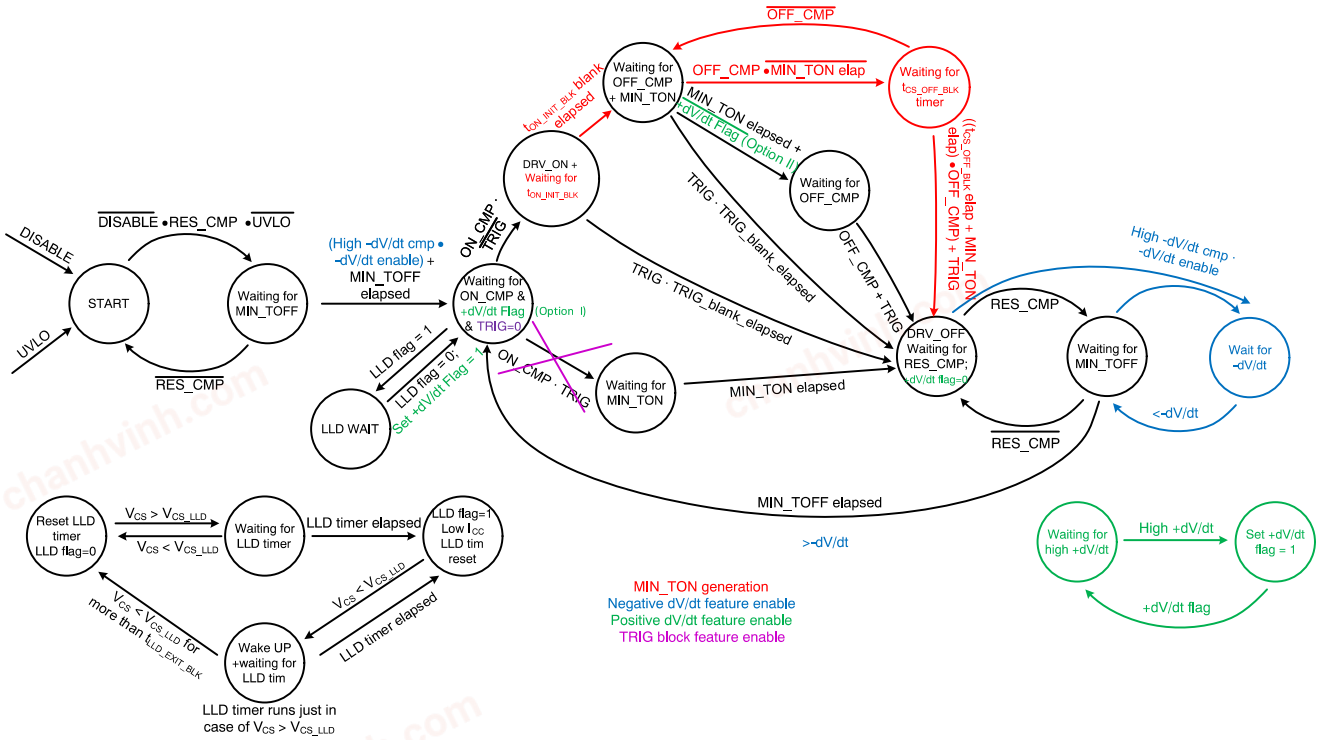


Figure 80. Overall Operation Bubble Diagram

OPN CODING

OPN	FA	FB	AA	WA
V_{DRV}	10 V	10 V	10 V	10 V
t_{ON_MIN}	1100 ns	1100 ns	1400 ns	500 ns
$t_{CS_OFF_BLK}$	250 ns	250 ns	155 ns	NA
t_{OFF_MIN}	4.00 μs	4.00 μs	4.00 μs	1.00 μs
$t_{CS_-DV/DT}$	24 ns	24 ns	24 ns	NA
$t_{LLD_EXIT_BLK}$	200 ns	200 ns	200 ns	200 ns
$V_{CCL_SB_A}$	4.7 V	8.9 V	4.7 V	4.7 V
+dV/dT	No	No	Yes/Short min_ton	No
Extra	–	–	–	Negative TRIG/DIS logic, TRIG blocking function, CS reset level disabled
Target application	Flyback/Forward freewheel position	Flyback/Forward freewheel position	Active clamp flyback	Forward forward position

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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

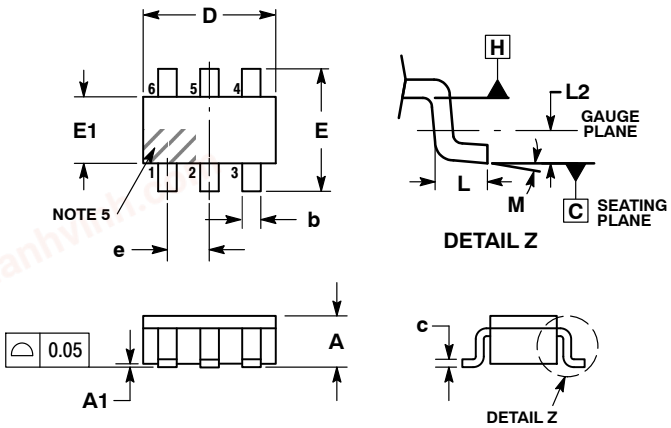
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SCALE 2:1

TSOP−6
CASE 318G−02
ISSUE V

DATE 12 JUN 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2		0.25 BSC	
M	0°	–	10°

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

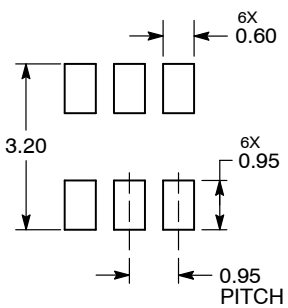
STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

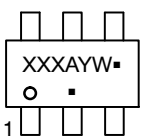
RECOMMENDED SOLDERING FOOTPRINT*



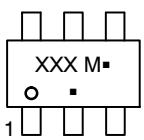
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC



STANDARD

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present.

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