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8 A Integrated Synchronous Buck Converter

Product Preview

NCP3237

The NCP3237 is a single−phase synchronous buck converter that integrates power MOSFETs to provide a high−efficiency and compact−footprint power management solution. This device is able to deliver up to 8 A output current over a wide output voltage range from 0.6 V to 12 V (up to 80% of V_{IN}). The NCP3237 offers a fixed frequency regulator ideally suited for noise sensitive systems.

Features

- V_{IN} = 4.7 V ~ 16 V
- V_{OUT} = 0.6 V ~ 0.80*V_{IN} and up to 12 V
- Integrated Power MOSFETs
- Up to 8 A Output Current
- Integrated 5 V LDO or External 5 V Supply (Fuse Option)
- Programmable Switching Frequency from 300 kHz to 1.2 MHz
- Selectable Forced CCM or PSM for High Efficiency at Light Load (Fuse Option)
- Both High−side and Low−side OCP Operation
- Hiccup Over−Current Protection
- Hiccup Over−Voltage and Under−Voltage Protection
- Recoverable Thermal Shutdown Protection
- 3.5 mm x 3.5 mm, FCQFN18 Package
- Safe Startup into Pre−biased Voltage
- This is a Pb−Free Device

Typical Application

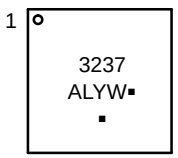
- Base Station Radio Units
- Point of Load
- Telecom and Networking
- Server and Storage System

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MARKING DIAGRAM

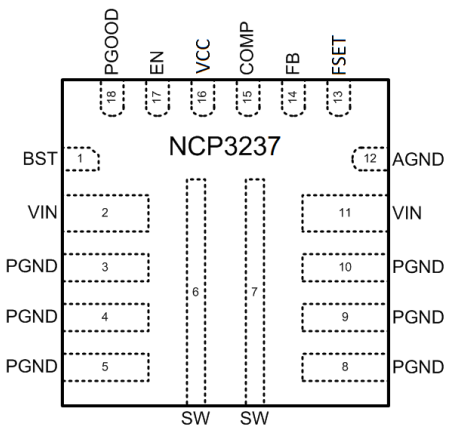
QFN18 3.5x3.5, 0.5P
CASE 485FR



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PINOUT DIAGRAM



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP3237MNTXG	QFN18 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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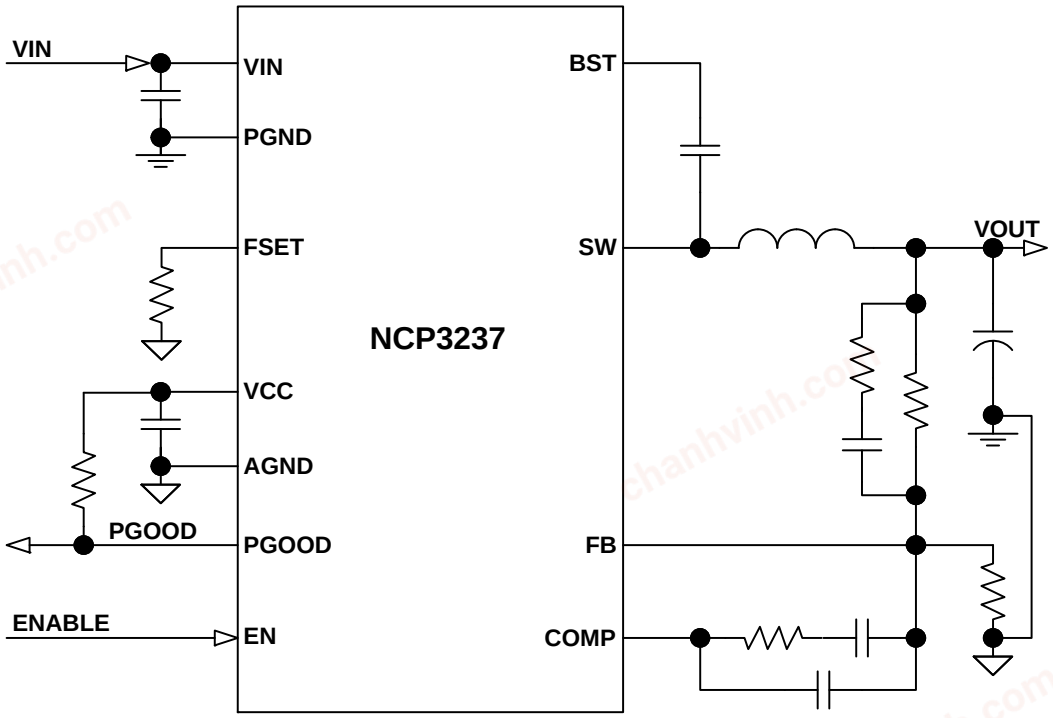


Figure 1. Typical Application Circuit

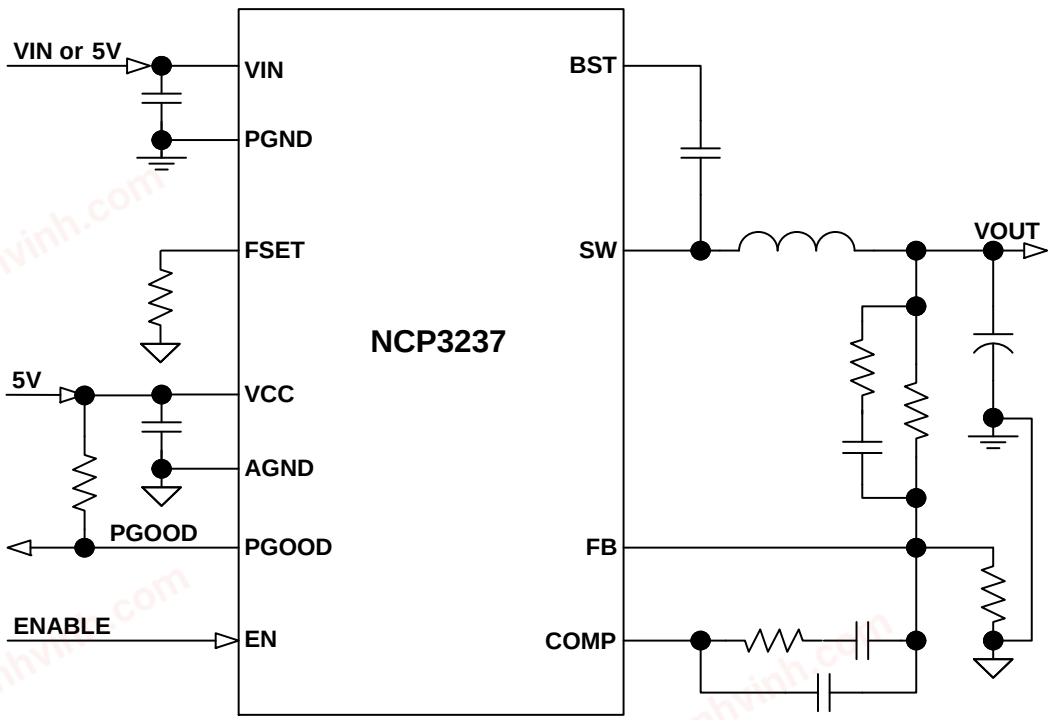


Figure 2. Typical Application Circuit with External 5 V Supply (Fuse Option)

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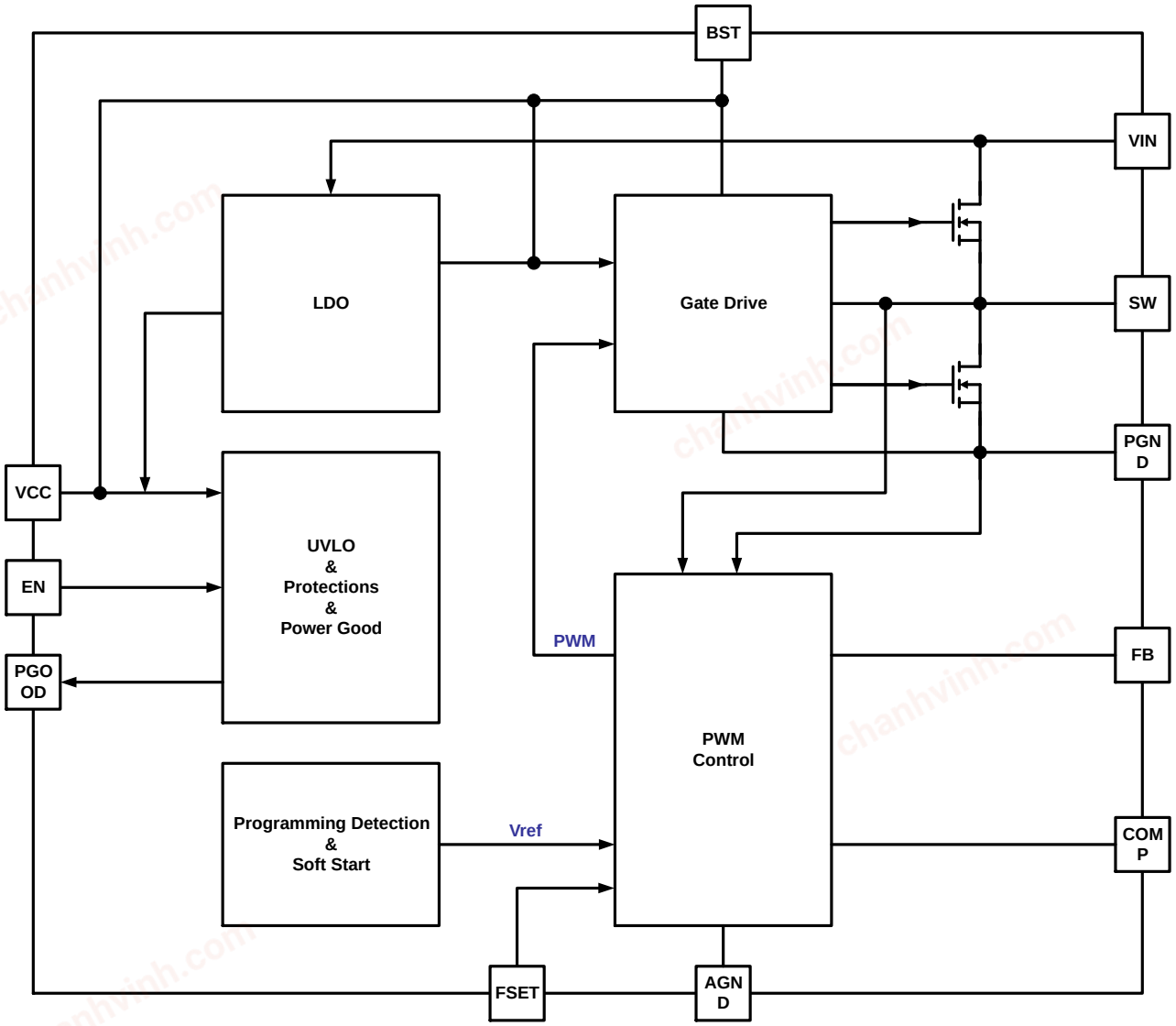


Figure 3. Functional Block Diagram

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PIN DESCRIPTION

Pin	Name	Type	Description
1	BST	Power Bidirectional	**Bootstrap**. Provides bootstrap voltage for the high−side gate driver. A 0.1 μF ~ 1 μF ceramic capacitor is required from this pin to SW.
2, 11	VIN	Power Input	**Power Supply Input**. Power supply input pin of the device, which is connected to drain of internal high−side power MOSFET. Ceramic capacitors must bypass this input to power ground. The capacitors should be placed as close as possible to this pin.
3, 4, 5, 8, 9, 10	PGND	Power Ground	**Power Ground**. These pins are the power supply ground pins of the device, which are connected to source of internal low−side power MOSFET.
6, 7	SW	Power Output	**Switching Node**. Pins to be connected to an external inductor. These pins are interconnection between internal high−side MOSFET and low−side MOSFET.
12	AGND	Analog Ground	**Analog Ground**. Ground of internal gate divers. Must be connected to the power ground.
13	FSET	Analog Input	**Frequency Option**. A resistor from this pin to AGND programs switching frequency.
14	FB	Analog Input	**Feedback**. Inverting input to error amplifier.
15	COMP	Analog Output	**Compensation**. Output pin of error amplifier.
16	VCC	Analog Power	**Voltage Supply of Controller**. Power supply input pin of control circuits. A 4.7 μF or larger ceramic capacitor bypasses this input to AGND. This capacitor should be placed as close as possible to this pin.
17	EN	Logic Input	**Enable**. Logic high enables the device and logic low shuts down the device.
18	PGOOD	Logic Output	**Power Good**. Open−drain output. Provides a logic high valid power good output signal, indicating the regulator's output is in regulation window.

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MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		Min	Max	
Power Supply Voltage to PGND	V_{VIN}		TBD (17)	V
Switch Node to PGND	V_{SW}	−2 −3 (<10ns)	TBD (17)	V
Analog Supply Voltage to GND	V_{PVCC}, V_{VCC}	−0.3	TBD (6.0)	V
BST to PGND	BST_PGND	−0.3	TBD (21) TBD (30) (<10ns)	V
BST to SW	BST_SW	−0.3	TBD (6.0)	V
FB to AGND	FB	−0.3	TBD (6.0)	V
AGND to PGND	VSNS	−0.3	0.3	V
Exposed Pad to PGND		−0.3	0.3	V
Other Pins		−0.3	VCC+0.3	V
Latch up Current: (Note 1)	I_{LU}	−100	100	mA
Operating Junction Temperature Range	T_J	−40	150	°C
Operating Ambient Temperature Range	T_A	−40	150	°C
Storage Temperature Range	T_{STG}	−55	150	°C
Thermal Resistance Junction to Top Case (Note 2)	$R_{\Psi JC}$	2		°C/W
Thermal Resistance Junction to Board (Note 2)	$R_{\Psi JB}$	12		°C/W
Thermal Resistance Junction to Ambient (Note 2)	$R_{\theta JA}$	31		°C/W
Power Dissipation at T_A = 25°C (Note 3)	P_D	TBD (2.25)		W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Latch up Current per JEDEC standard: JESD78 class II.
2. The thermal resistance values are dependent of the internal losses split between devices and the PCB heat dissipation. This data is based on a typical operation condition with a 4−layer FR−4 PCB board, which has two, 1−ounce copper internal power and ground planes and 2−ounce copper traces on top and bottom layers with approximately 80% copper coverage. No airflow and no heat sink applied (reference EIA/JEDEC 51.7). It also does not account for other heat sources that may be present on the PCB next to the device in question (such as inductors, resistors etc.)
3. The maximum power dissipation (PD) is dependent on input voltage, output voltage, output current, external components selected, and PCB layout The reference data is obtained based on T_{JMAX}=125^{o}C and $R_{\theta JA}$ =**TBD**.

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ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, typical values are referenced to $T_A = T_J$ = 25°C, Min and Max values are referenced to $T_A = T_J$ = −40°C to 150°C. unless otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Units
SUPPLY VOLTAGE MONITOR						
V_{IN} Supply Voltage Range	(Note 4)	V_{IN}	4.7		16	V
VCC Under−Voltage (UVLO) Threshold	VCC falling	V_{CCUV-}	3.7			V
VCC OK Threshold	VCC rising	V_{CCOK}			4.3	V
VCC UVLO Hysteresis		V_{CCHYS}		260		mV
SUPPLY CURRENT						
V_{IN} Quiescent Supply Current	EN high, V_{FB} = 600 mV	I_{QIN_CCM}		TBD	TBD	mA
V_{IN} Shutdown Current	EN low	I_{SD_IN}			TBD	μA
VCC						
Output Voltage	6V < VIN < 16V, IPVCC = 20mA (External), EN High, V_{FB} = 600mV	V_{PVCC}	4.85	5.0	5.15	V
Load Regulation	6V < VIN < 16V, IPVCC = 5mA to 50mA (External), EN High, V_{FB} = 600mV		−3.0		3.0	%
Dropout Voltage	VIN = 5V, IPVCC = 50mA (External), EN High, V_{FB} = 600mV	V_{DC_PVCC}		400		mV
ENABLE						
EN High Threshold	Normal Operation	V_{H_EN}	1.6			V
EN Low Threshold	Shutdown	V_{L_EN}			1.2	V
EN Input Impedance	Resistance from EN pin to AGND	R_{EN}		1.6		MΩ
SOFT START						
System Reset Time	From EN High to BST Refresh (Note 4)	T_{RST}		0.8		ms
BST Refresh Time		T_{BST}		10		μs
Soft Start Slew Rate	Refer to Internal VREF FUSE_SR = 00, default FUSE_SR = 01 FUSE_SR = 10 FUSE_SR = 11	SR_{SS}		 0.6 1.2 0.3 0.15		mV/μs
PGOOD						
PGOOD Startup Delay	Measured from end of Soft Start to PGOOD Assertion (Note 4)	T_{d_PGOOD}		100		μs
PGOOD Shutdown Delay	Measured from EN to PGOOD de−assertion			1		μs
PGOOD Low Voltage	I_{PGOOD} = −4 mA	V_{I_PGOOD}			0.3	V
PGOOD Leakage Current	PGOOD = 5 V	I_{lkg_PGOOD}			1.0	μA
SWITCHING FREQUENCY						
Switching Frequency in CCM	1% Resistor from FSET Pin to AGND (trimmed at 40 kΩ, 550 kHz) 40k 20k	F_{SW}	 495	 550 1100	 605	kHz
VOLTAGE REGULATION						
Regulated Feedback Voltage	EN = High 0°C to 85°C −40°C to 150°C	V_{FB}	 595 594	 600 600	 605 606	mV
PWM MODULATION						
PWM Ramp Amplitude	(Note 4)	V_{RAMP}		V_{IN} / 9		V
Minimum On Time	(Note 4)	T_{on_min}		50		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Guaranteed by design, not tested in production.

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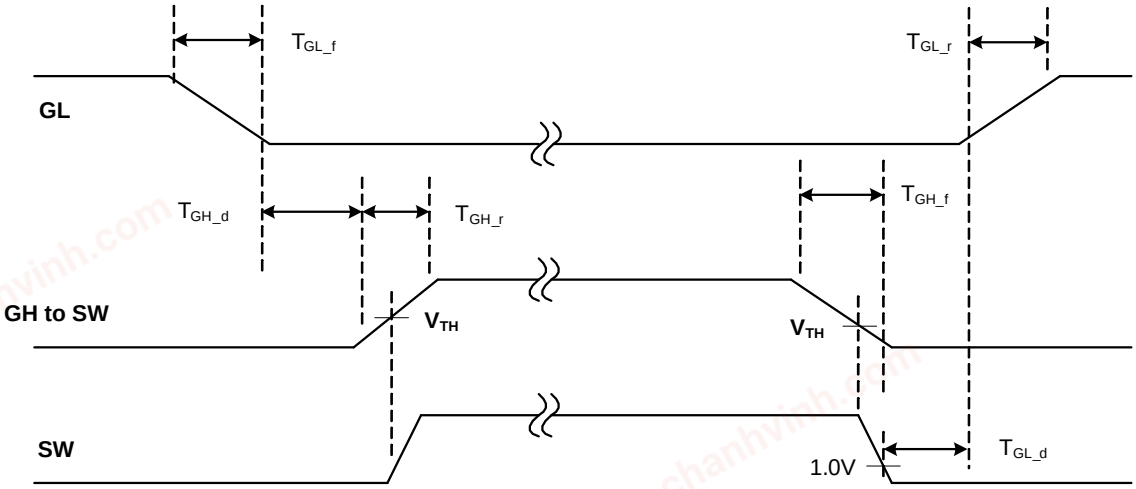
ELECTRICAL CHARACTERISTICS (continued)
(V_{IN} = 12V, typical values are referenced to $T_A = T_J$ = 25°C, Min and Max values are referenced to $T_A = T_J$ = −40°C to 150°C. unless otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Units
PWM MODULATION						
Minimum Off Time	(Note 4)	T_{off_min}		200		ns
VOLTAGE ERROR AMPLIFIER						
Open−Loop DC Gain	(Note 4)	$GAIN_{EA}$		80		dB
Unity Gain Bandwidth	(Note 4)	GBW_{EA}		20		MHz
Slew Rate	(Note 4)	SR_{COMP}		20		V/μs
COMP Voltage Swing	I_{COMP}(source) = 2 mA	$V_{maxCOMP}$	3.1	3.3		V
	I_{COMP}(sink) = 2 mA	$V_{minCOMP}$		0.75	0.85	
FB Bias Current	V_{FB} = 0.6 V	I_{FB}	−100		100	nA
HIGH−SIDE MOSFET						
Drain−to−Source ON Resistance	BST − SW = 5 V, $T_A = T_J$ = 25°C	R_{ON_H}		14		mΩ
LOW−SIDE MOSFET						
Drain−to−Source ON Resistance	V_{PVCC} = 5 V, $T_A = T_J$ = 25°C	R_{ON_L}		6		mΩ
PROTECTIONS						
Over Current Threshold	High−side Current Limit for 8A part	I_{LMT_HS}	10.5			A
	Low−side Current Limit for 8A part	I_{LMT_LS}	9.6			
Negative Over Current Threshold	Low−side negative current limit for 6A part	$I_{LMT_LS_NEG}$			−4.8	A
Under Voltage Protection (UVP) Threshold	Voltage from FB to GND	V_{UVTH}		DAC − 250		mV
Under Voltage Protection (UVP) Hysteresis		V_{UVHYS}		20		mV
Under Voltage Protection (UVP) Debounce Time	(Note 4)			2		μs
Absolute Over Voltage Protection (AOVP) Threshold during Soft Start	Voltage from FB to GND	V_{AOVTH}		850		mV
Absolute Over Voltage Protection (AOVP) Hysteresis during Soft Start		V_{AOVHYS}		−25		mV
Over Voltage Protection (OVP) Threshold	Voltage from FB to GND	V_{OVTH}		DAC + 150		mV
Over Voltage Protection (OVP) Hysteresis		V_{OVHYS}		−25		mV
Over Voltage Protection (OVP) Debounce Time	(Note 4)			1		μs
Thermal Shutdown (TSD) Threshold	(Note 4)	T_{sd}		160		°C
Recovery Temperature Threshold	(Note 4)	T_{rec}		135		°C
BOOTSTRAP						
On Resistance of Rectifier Switch	V_{PVCC} = 5 V, Id = 2 mA, $T_A = T_J$ = 25°C (Note 4)	R_{BST}		50		Ω
Rectifier Switch Leakage Current	(Note 4)	I_{lkgBST}			3	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Guaranteed by design, not tested in production.

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Note: Timing is referenced to the 90% and 10% points, unless otherwise noted.

Figure 4. Timing Diagram of Gate Drivers

DETAILED DESCRIPTION

General

NCP3237 is a single−phase synchronous buck converter with two integrated N−type power MOSFETs to provide a high−efficiency and compact−footprint power management solution. The device is able to deliver up to 8A output current on a wide output voltage range from 0.6 V to 0.8 × VIN and no higher than 12 V. It has a wide input voltage range from 4.7 V to 16 V.

The NCP3237 features including a resistor adjustable frequency input to optimize the output filter size, an enable and power good indicator for sequencing and an internal soft−start function during the initial power up. These devices offer safe start up into a pre−biased output condition and offer multiple protection features including cycle−by−cycle high side and low side over−current limiting, output over−voltage protection (OVP), under voltage protection (UVP) and thermal shutdown protection (TSD). During overcurrent and undervoltage conditions, these devices enter hiccup protection and offers latch off protection during output over−voltage conditions.

NCP3237 provides Pulse−Skipping Mode (PSM) to fit the requirements for light load application. PSM operation provides reduced power loss and increases the efficiency at light load. The adaptive power control architecture enables smooth transition between light load and heavy load while maintaining fast response to load transients.

Operation Options

NCP3237 operates in either forced CCM or PSM by fuse option. In forced CCM, the high−side FET is ON during the on−time and the low−side FET is ON during the entire off−time. The switching is synchronized to an internal clock thus the switching frequency is fixed.

The converter will enter PSM when the load current decreases to a certain level. An internal zero−crossing comparator detects the zero crossing (ZCD) of the inductor current from positive to negative. The converter will enter PSM when 32 consecutive ZCD are detected by the ZCD counter. Any non−ZCD event would reset the counter to 0. In PSM, when the inductor current reaches zero, the comparator sends a signal to the logic circuitry and turns off the low−side FET to stop the inductor current becoming negative.

Since the clock is turned off in PSM, the switching frequency is no longer controlled by the master clock, but by the ripple voltage appearing on COMP. The ramp signal starts to ramp up when the COMP signal intercepts with internal comp threshold (comp_th). The gate signal terminates when ramp intercepts with the COMP. This is also called ramp pulse modulation.

When the load increases, the inductor current becomes all−time positive so that the zero−crossing comparator does not capture any zero−crossing event. The converter enters into CCM directly when no zero−crossing is detected for just one PWM pulse. In CCM, the switching synchronizes to the internal clock and the switching frequency is fixed.

Sonic Mode

In PSM, the switching frequency is determined by the load. The converter enters sonic mode in very light load so that the lowest switching frequency is limited above 30 kHz to stay out of audible noise frequency range. In this mode, if the low side switch does not turn on for 33 us, the controller turns on the low side switch to discharge the output voltage. Then the COMP signal will go high until it intercepts with comp_th and the low side switch turns off.

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After that, the high side switch turns on and the PSM operation continues.

Reference Voltage

The NCP3237 incorporates an internal reference that allows output voltage to be as low as 0.6 V. The tolerance of the internal reference is guaranteed over the entire operating temperature range of the controller. The reference voltage is trimmed using a test configuration that accounts for error amplifier offset and bias currents.

Oscillator Ramp

The ramp waveform is a saw tooth formed at the PWM frequency with a peak−to−peak amplitude of VIN/9, offset from GND by typically 1.0 V. The PWM duty cycle is limited to a typical 80%, allowing the bootstrap capacitor to charge during each cycle.

Soft Start

The NCP3237 has the soft start function. The output starts to ramp up following a system reset period after the device is enabled. Four choices of soft−start time can be selected by a 2−bit fuse option. The device is able to start up smoothly under an output pre−biased condition.

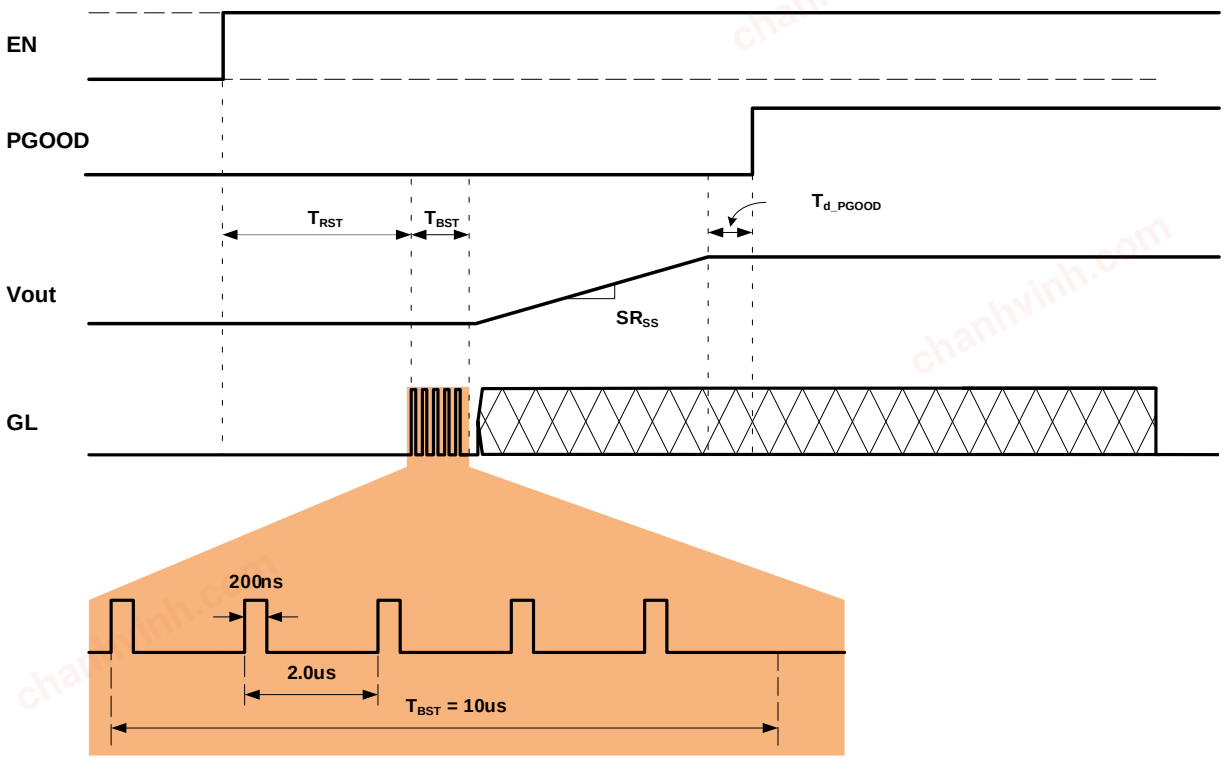


Figure 5. Timing Diagram of Soft Start

High−side MOSFET Over−Current Protection (HSOCP)

The NCP3237 protects converter from high−side MOSFET over current by a cycle−by−cycle current limitation. The high−side MOSFET current is monitored by differential voltage sensing between VIN pin and SW pin, and compared with the internal OCP limit value ILMT_HS. If it reaches the ILMT_HS level on any given clock cycle, the cycle terminates to prevent the current from increasing any further.

If HSOCP happens and lasts for more than 3 consecutive times, the device shuts down and enters into a continuous hiccup mode. To prevent nuisance trips, the internal HSOCP counter adds 2 for a HSOCP event, and subtracts 1 for every normal switching cycle (not LSOCP cycles). The counter reset when it counts up to 6 and the device shuts down. Upon shut down, the high side switch keeps off, while the low side switch keeps on until a ZCD is detected. This is to prevent the switching node going very negative which can cause malfunction.

The device implements a 6 soft−start cycle time−out from HSOCP get asserted. After the time−out, it implements BST refresh cycles before a normal soft−start attempt. Please see Figure 6 for the timing diagram.

The device may enter into under voltage protection before OCP hiccup happens if the output voltage drops down very fast.

HSOCP detection starts from the beginning of soft−start, and ends in shutdown and idle time of hiccup mode.

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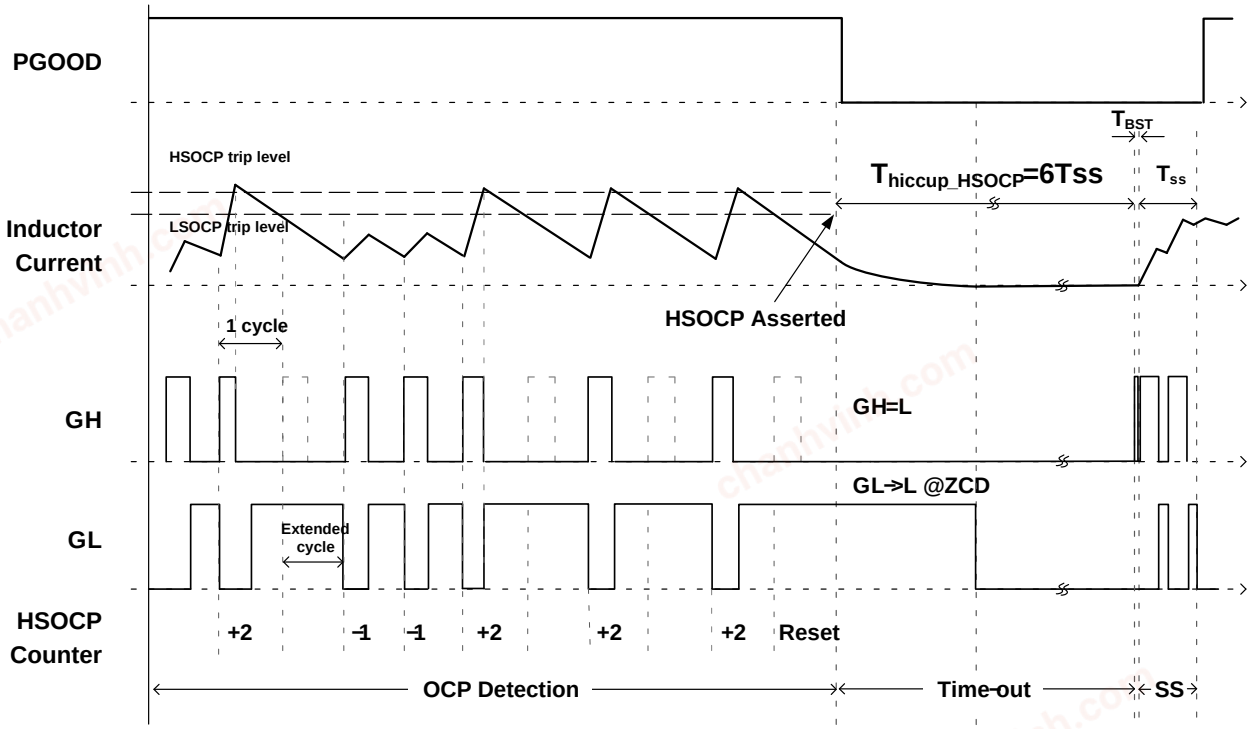


Figure 6. Timing Diagram of High−Side Over Current Protection (Internal Use)

Low−side MOSFET Over−Current Protection (LSOCP)

The NCP3237 protects converter from low−side MOSFET over current by a cycle−by−cycle current limitation. The low−side MOSFET current is monitored by voltage sensing between SW pin and PGND pin, and compared with the internal OCP limit value ILMT_LS. If it is higher than ILMT_LS level on any given clock cycle, the high−side MOSFET will not be turned on and the low−side MOSFET stays on for the next switching cycle. The high−side MOSFET is turned on again only when the low−side current is below the OCP limit value during the previous switching cycle.

If LSOCP happens and lasts for more than 4 consecutive times, the device shuts down and enters into a hiccup mode. To prevent nuisance trips, the internal LSOCP counter adds 2 for a LSOCP event, and subtracts 1 for every normal switching cycle (not extended cycles). The counter reset when it counts up to 8 and the device shuts down. Upon shut down, the high side switch keeps off all the time, while the low side switch keeps on until a ZCD is detected. This is to prevent the switching node going very negative which can cause malfunction.

The device implements a 4 soft−start cycle time−out from the LSOCP get asserted. After the time−out, it implements BST refresh cycles before a normal soft−start attempt. Please see Figure 7 for the timing diagram.

The device may enter into under voltage protection before OCP hiccup happens if the output voltage drops down very fast.

LSOCP detection starts from the beginning of soft−start time, and ends in shutdown and idle time of hiccup mode.

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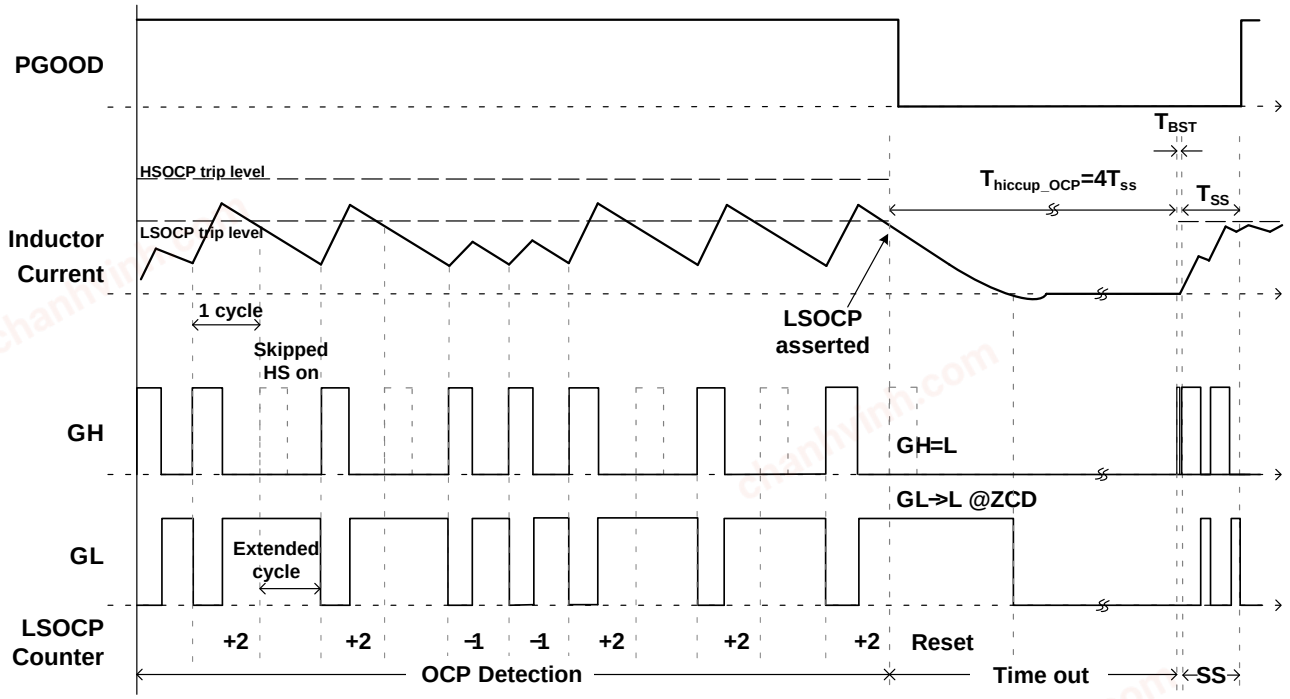


Figure 7. Timing Diagram of Low−Side Over Current Protection (Internal Use)

Under Voltage Protection (UVP)

NCP3237 monitors the FB voltage to detect a UVP event. A UVP is asserted once FB voltage drops below DAC−250mV for more than UVP debounce time. When UVP is asserted, it pulls PGOOD low, turns off the high side FET, and keep the low−side FET on until a ZCD is detected. It implements a 5 soft−start cycle time−out from UVP get asserted. After the time−out, it implements BST refresh cycles before a normal soft−start attempt. Please see Figure 8 for the timing diagram.

UVP detection starts when PGOOD delay Td_PGOOD is expired right after a soft start, and ends in shutdown and idle time of hiccup mode.

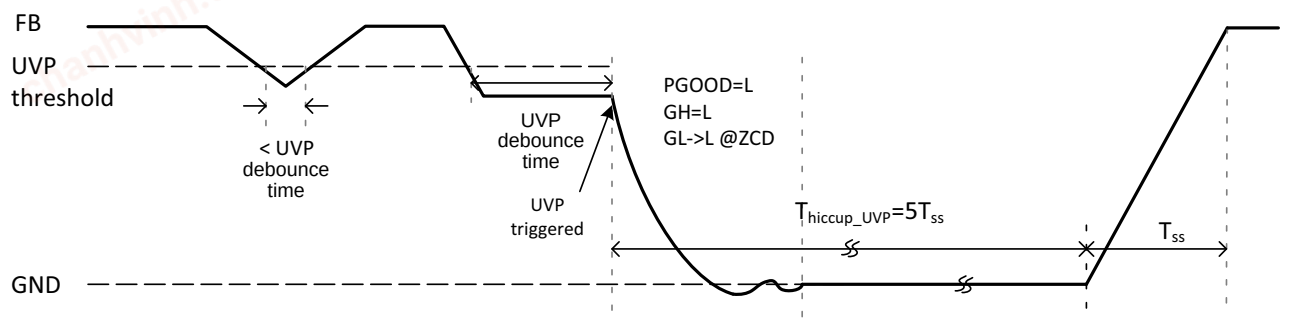


Figure 8. Timing Diagram of Non−latched Under Voltage Protection

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Over Voltage Protection (OVP)

During normal operation the output voltage is monitored at FB pin. If FB voltage exceeds the OVP threshold for more than 1 μs, OVP is triggered and PGOOD is pulled low. In the meanwhile, the high−side MOSFET is latched off and the low−side MOSFET is turned on. After the OVP trips, the DAC immediately goes down to zero. The low−side MOSFET current would become negative during OVP. If the low−side negative current limit is exceeded, the low−side MOSFET is turned off immediately. In this scenario, both MOSFETs are off. After negative over current protection trips, the low−side MOSFET turns off and stays off for at least 640 ns. If the OVP is still not cleared, the low−side MOSFET will turn on again. The OVP threshold is set to a fixed value of 750 mV.

After the OVP gets asserted, NCP3237 implements an 8 normal soft−start cycle time−out. Then it is followed by BST refresh cycles before a normal soft−start attempt. Please see Figure 9 for the timing diagram.

To restart the device after latch−off OVP, the system needs to have either VCC or EN toggled state.

OVP detection starts from the beginning of soft−start and ends in shutdown, latch−off, and idle time of hiccup mode caused by OCP.

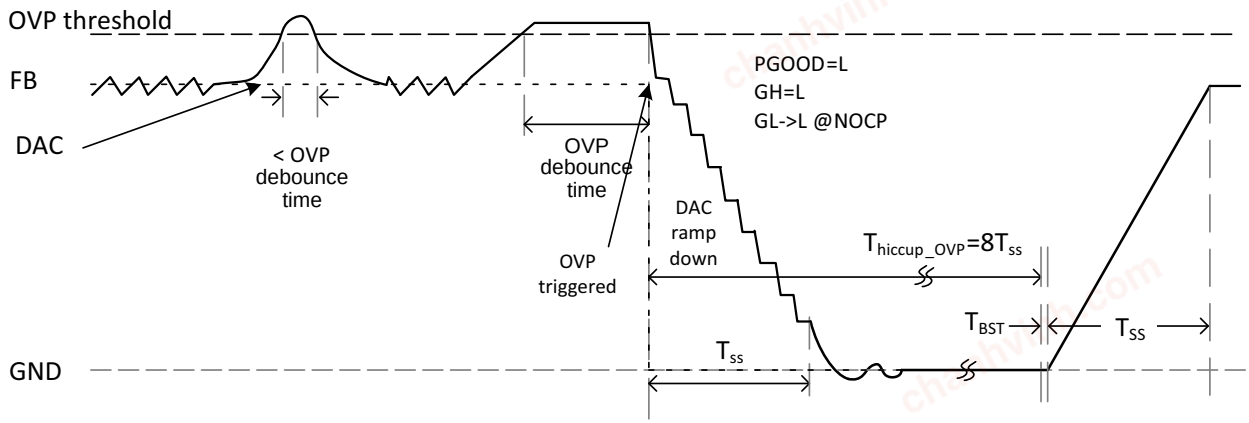


Figure 9. Function of Non Latch−Off Over Voltage Protection

Thermal Shutdown (TSD)

The NCP3237 has an internal thermal shutdown protection to protect the device from overheating in an extreme case that the die temperature exceeds 160°C. TSD detection starts from the beginning of soft−start. Once the thermal protection is triggered, the whole chip shuts down. If the temperature drops below 135°C, the system automatically recovers and a normal power sequence follows.

Power Good Monitor (PGOOD)

The NCP3237 provides a window comparator to monitor the voltage at FB pin. The open−drain PG goes high when the device is operating in a normal operating condition (no UVLO, UVP, OVP, OCP or TSD faults). Connect a pull up resistor to VCC for simplicity or to an external voltage to interfacing to other logic such as 3.3 V or 2.5. When a fault occurs, PGOOD goes low. Choose a pull up to limit the sink current to 4 mA. During soft start, PGOOD stays low until the feedback voltage is within the specified range for about 100 μs. The PGOOD pin de−asserts as the EN pin pulled low for 1 μs. For an under−voltage event on VCC, PGOOD goes low immediately.

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LAYOUT GUIDELINES

Electrical Layout Considerations

Good electrical layout is a key to make sure proper operation, high efficiency, and noise reduction.

- **Power Paths**: Use wide and short traces for power paths (such as VIN, VOUT, SW, and PGND) to reduce parasitic inductance and high−frequency loop area. It is also good for efficiency improvement.
- **Power Supply Decoupling**: The device should be well decoupled by input capacitors and input loop area should be as small as possible to reduce parasitic inductance, input voltage spike, and noise emission. Usually, a small low−ESL MLCC is placed very close to VIN and PGND pins.
- **VCC Decoupling**: Place decoupling caps as close as possible to the controller VCC and PVCC pins. The filter resistor at VCC pin should be not higher than 4.7 Ω to prevent large voltage drop.
- **Output Decoupling**: The output capacitors should be as close as possible to the load. If the load is distributed, the capacitors should also be distributed and generally placed in greater proportion where the load is more dynamic.
- **Switching Node**: SW node should be a copper pour, but compact because it is also a noise source.
- **Bootstrap**: The bootstrap cap and an option resistor need to be very close and directly connected between pin 17 (BST) and pin 16 (SW).
- **Ground**: It would be good to have separated ground planes for PGND and AGND and connect the AGND planes to the exposed pad GND through vias.
- **Voltage Sense**: Route a “quiet” path for the output voltage sense. AGND could be used as a remote ground sense when differential sense is preferred.
- **Compensation Network**: The compensation network should be close to the NCP3237. Keep FB trace short to minimize it capacitance to ground.

Thermal Layout Considerations

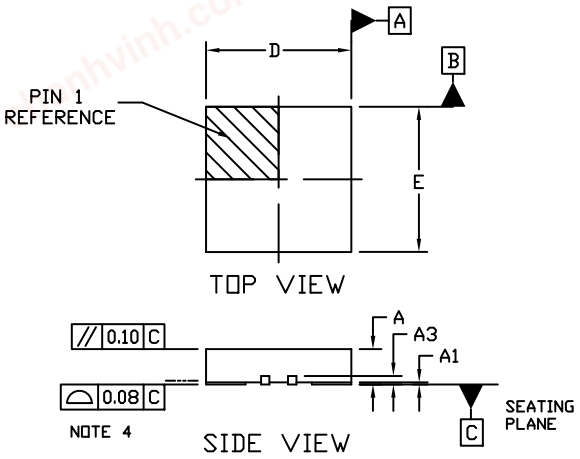
Good thermal layout helps high power dissipation from a small−form factor VR with reduced temperature rise.

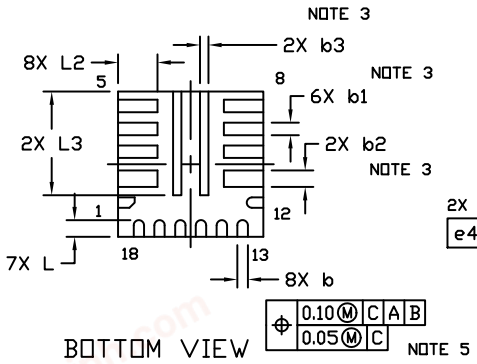
- The exposed pads must be well soldered on the board.
- A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.
- More free vias are welcome to be around IC and underneath the exposed pads to connect the inner ground layers to reduce thermal impedance.
- Use large area copper pour to help thermal conduction and radiation.
- Do not put the inductor to be too close to the IC, thus the heat sources are distributed.

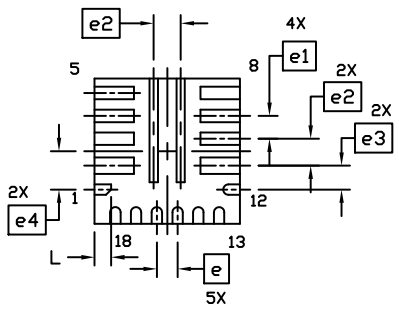
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PACKAGE DIMENSIONS

QFN18 3.5x3.5, 0.5P
CASE 485FR
ISSUE O



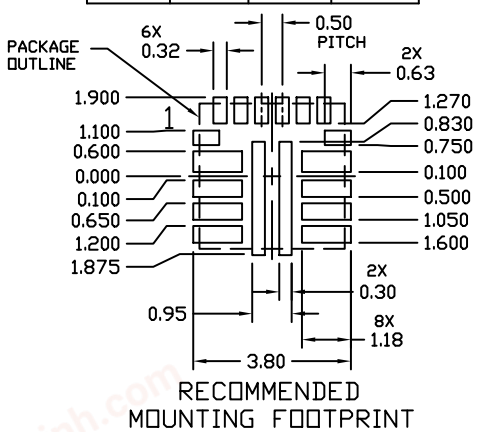




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS b AND b1 APPLY TO THE PLATED TERMINAL AND ARE MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO ALL OF THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO ALL OF THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM..	MAX.
A	0.80	0.85	0.90
A1	0.00	---	0.05
A3	0.20 REF		
b	0.20	0.25	0.30
b1	0.25	0.30	0.35
b2	0.35	0.40	0.45
b3	0.15	0.20	0.25
D	3.40	3.50	3.60
E	3.40	3.50	3.60
e	0.50 BSC		
e1	0.55 BSC		
e2	0.65 BSC		
e3	0.575 BSC		
e4	0.925 BSC		
L	0.30	0.40	0.50
L2	0.85	0.95	1.05
L3	2.40	2.50	2.60



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NCP3237

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