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CCM Buck Controller for Precise Current Regulation and Wide Analog Dimming

NCL35076

The NCL35076 is a DC−DC buck controller for wide dimming range down to 1% by analog dimming control to relieve audible noise and flicker in PWM dimming. ON Semiconductor's proprietary LED current calculation technique driven by zero input offset amplifiers performs precise constant current in the whole analog dimming range. Multi−mode operation provides low LED current ripple with small output capacitor by CCM at heavy load and deep analog dimming by DCM at light load.

PWM dimming is also provided in case that constant LED color temperature is required. NCL35076 ensures high system reliability with LED short protection, over current protection and thermal shutdown.

Features

- Wide Analog Dimming Range: 1~100%
- Low CC Tolerance: ±2% at 100% Load & ±20% at 1% Load
- Low System BOM
- LED Off Mode at Standby
- Low Standby Current
- PWM Dimming Available
- Gate Sourcing and Sinking Current of 0.5 A/0.8 A
- Robust Protection Features
  - LED Short Protection
  - Over Current Protection
  - Thermal Shutdown
  - V_{DD} Over Voltage Protection

Typical Applications

- LED Lighting System

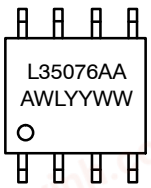
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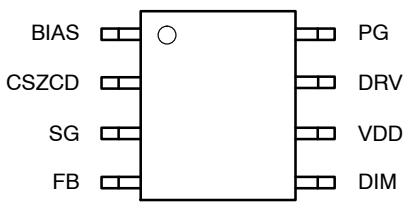
SOIC−8 NB
CASE 751

MARKING DIAGRAM



L30076	= Specific Device Code
AA	= Default Trimming Option
A	= Assembly Location
WL	= Wafer Lot Traceability Code
YYWW	= 4 Digit Data Code

PIN ASSIGNMENT



(Top View)

ORDERING INFORMATION

Device	Package	Shipping
NCL35076AADR2G	SOIC−8 NB	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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APPLICATION SCHEMATIC

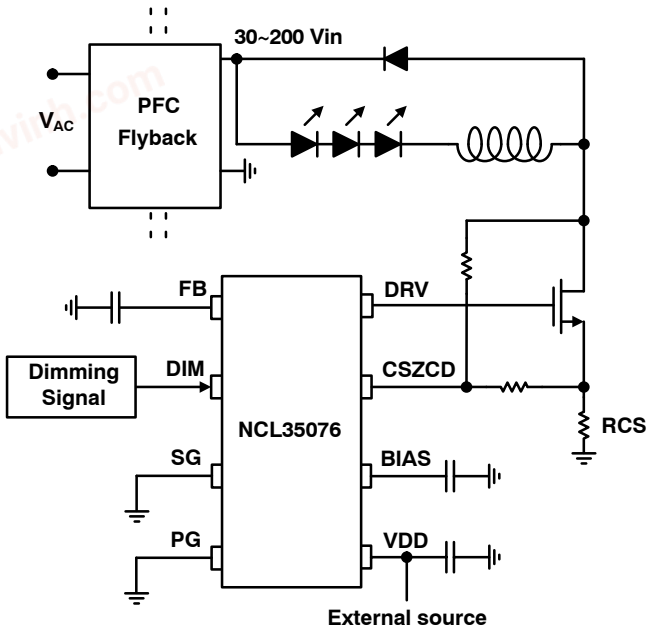


Figure 1. Application Schematic

BLOCK DIAGRAM

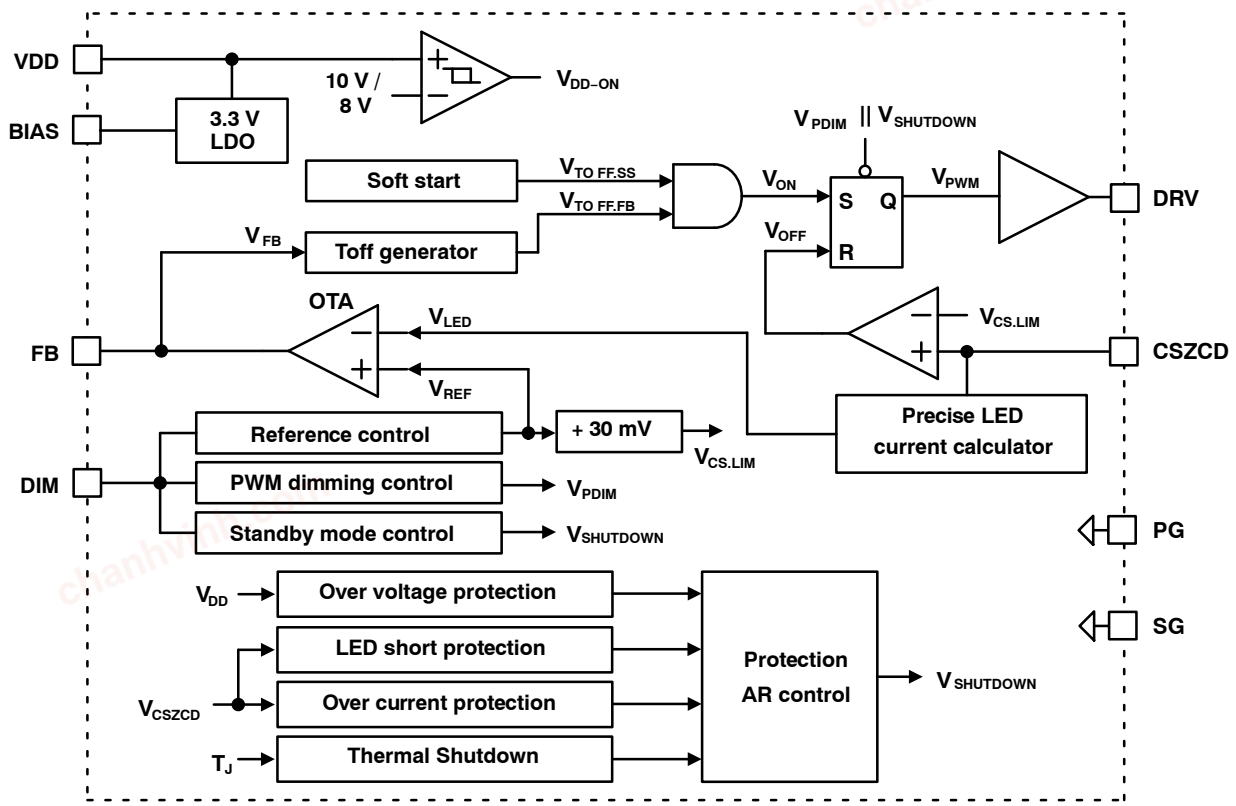
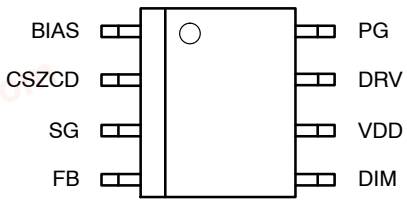


Figure 2. Simplified Block Diagram

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PIN CONFIGURATION



(Top View)

Figure 3. Pin Configuration

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Description
1	BIAS	3.3 V BIAS	This pin is 3.3 V LDO output to bias the internal digital circuit
2	CSZCD	CS and ZCD Sensing	This pin detects the switch current and the inductor current zero cross time
3	SG	Signal Ground	Signal Ground is close to control pin circuit such as CSZCD, DIM and FB
4	FB	Feedback	Output of feedback OTA
5	DIM	Dimming Input	Dimming signal is provided to this pin
6	VDD	Power Supply	IC operating current is supplied to this pin
7	DRV	Output Drive	This pin is connected to drive external switch
8	PG	Power Ground	Power Ground is close to the capacitors at BIAS and VDD pin

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SPECIFICATIONS

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
VDD, DRV Pin Voltage Range	$V_{MV(MAX)}$	−0.3 to 30	V
DIM, FB, CSZCD, BIAS Pin Voltage Range	$V_{LV(MAX)}$	−0.3 to 5.5	V
Maximum Power Dissipation (T_A < 50°C)	$P_{D(MAX)}$	550	mW
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	T_{STG}	−55 to 150	°C
Junction−to−Ambient Thermal Impedance	$R_{\theta JA}$	145	°C/W
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2	kV
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	1	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. This device series incorporates ESD protection and is tested by the following methods:
   - ESD Human Body Model per JEDEC Standard JESD22−A114
   - ESD Charged Device Model per JEDEC Standard JESD22−C101
   - Latch−up Current Maximum Rating ±100 mA per JEDEC Standard JESD78

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Min	Max	Unit
Junction Temperature	T_J	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{DD} = 15 V and T_J = −40~125°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
VDD SECTION						
IC Turn−On Threshold Voltage		$V_{DD(ON)}$	9.3	10.0	10.7	V
IC Turn−Off Threshold Voltage		$V_{DD(OFF)}$	7.4	8.0	8.6	V
Startup Current	V_{DD} = $V_{DD(ON)}$ − 1.6 V	$I_{DD(ST)}$	−	250	400	μA
Operating Current		$I_{DD(OP)}$	−	6.5	8.0	mA
Standby Current		$I_{DD(SB)}$	−	200	300	μA
BIAS SECTION						
BIAS Voltage		V_{BIAS}	3.23	3.30	3.37	V
	T_J = 25~100°C (Note 4)		3.25	3.30	3.35	V
DIM SECTION						
DIM Voltage for 100% V_{REF}	V_{DIM} = 2.6 V	$V_{DIM(REF−MAX)}$	2.44	2.50	2.56	V
DIM Voltage for 99% V_{REF}		$V_{DIM(MAX−EFF)}$	2.400	2.475	2.528	V
Standby Enabling DIM Voltage		$V_{DIM(SB−ENA)}$	50	75	100	mV
Standby Disabling DIM Voltage		$V_{DIM(SB−DIS)}$	60	100	140	mV
Standby Delay Time		$t_{SB(DELAY)}$	9	10	11	ms
FB SECTION						
FB OTA Source Current	IFB = (V_{LED} − V_{REF}) x $g_{M(FB)}$ x 12.5 V_{REF} = 120 mV, V_{LED} = 80 mV	$I_{FB(SOURCE)}$	−14.0	−11.5	−9.0	μA
FB OTA Sink Current	IFB = (V_{LED} − V_{REF}) x $g_{M(FB)}$ x 12.5 V_{REF} = 40 mV, V_{LED} = 80 mV	$I_{FB(SINK)}$	9.0	11.5	14.0	μA

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ELECTRICAL CHARACTERISTICS (V_{DD} = 15 V and T_J = −40~125°C unless otherwise specified) (continued)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
FB SECTION						
FB OTA Transconductance	$g_{M(FB)} = I_{FB} / \{(V_{REF} - V_{LED}) \times 12.5\}$	$g_{M(FB)}$	18	23	28	μmho
FB OTA High Voltage	V_{REF} = 120 mV, V_{LED} = 80 mV	$V_{FB(HIGH)}$	4.7	–	–	V
FB Minimum Clamping Voltage	V_{REF} = 0 mV, V_{LED} = 80 mV	$V_{FB(CLP)}$	0.4	0.5	0.6	V
CS SECTION						
CS Regulation		$V_{CS(REG-MAX)}$	175	180	185	mV
CS Current Ripple Voltage		$V_{CS(RIPPLE)}$	25	30	35	mV
CS Current Limit Minimum		$V_{CS(LIM-MIN)}$	72	80	88	mV
DUTY SECTION						
Leading Edge Blanking Time at Turn−on		$t_{LEB(TON)}$	360	400	440	ns
Maximum Ton Time		$t_{ON(MAX)}$	45	50	55	μs
Minimum Toff Time	V_{FB} = 3.8 V	$t_{OFF(MIN)}$	400	850	1000	ns
Maximum Toff Time	V_{FB} = 0.5 V	$t_{OFF(MAX)}$	1.17	1.30	1.43	ms
Maximum FB Voltage for Min. Toff		$V_{FB(MAX-TOFF)}$	3.30	3.43	3.55	V
Minimum FB Voltage for Max. Toff		$V_{FB(MIN-TOFF)}$	0.9	1.1	1.3	V
DRV SECTION						
DRV Low Voltage		$V_{DRV(LOW)}$	–	–	0.2	V
DRV High Voltage	V_{DD} = 15 V	$V_{DRV(HIGH)}$	11	12	13	V
DRV Rising Time	C_{DRV} = 3.3 nF	$t_{DRV(R)}$	60	100	145	ns
DRV Falling Time	C_{DRV} = 3.3 nF	$t_{DRV(F)}$	25	55	105	ns
AUTO RESTART SECTION						
Auto Restart Time at Protection		$t_{AR(PROT)}$	0.9	1.0	1.1	s
VDD OVER VOLTAGE PROTECTION SECTION						
VDD Over Voltage Threshold Voltage		$V_{DD(OVP)}$	22	23	24	V
SHORT LED PROTECTION SECTION						
SLP Monitoring Triggering Delay Time		$t_{SLP(MON-DEL)}$	18	20	22	ms
SLP Monitoring Disable Time at Startup		$t_{SLP(MON-DIS)}$	10.8	12.0	13.2	ms
OVER CURRENT PROTECTION SECTION						
CS Over Current Protection Threshold		$V_{CS(OCP)}$	0.4	0.5	0.6	V
THERMAL SHUTDOWN SECTION						
Thermal Shut Down Temperature (Note 3)		T_{SD}	130	150	170	°C
Thermal Shut Down Hysteresis (Note 3)		$T_{SD(HYS)}$	25	30	35	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Guaranteed by design.
4. Guaranteed by characterization.

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TYPICAL CHARACTERISTICS

(These characteristic graphs are normalized at T_A = 25°C)

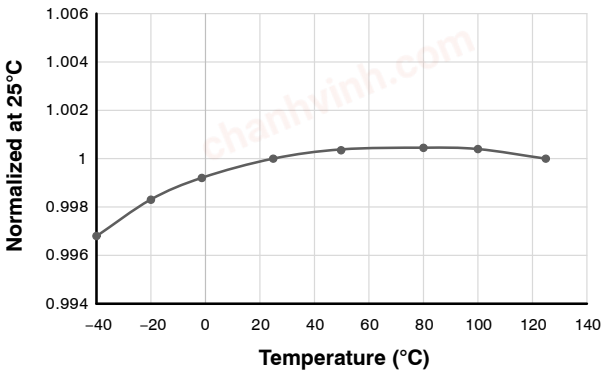


Figure 4. V_{BIAS} vs. Temperature

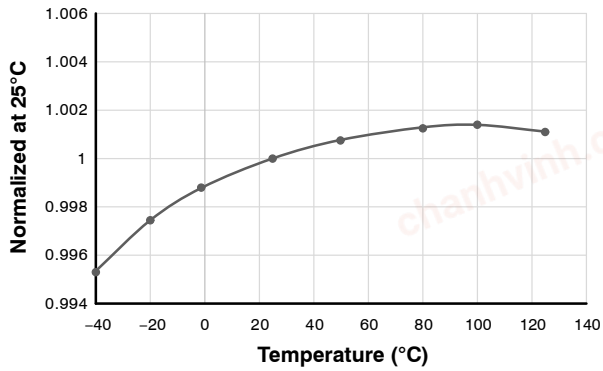


Figure 5. $V_{DIM(MAX)}$ vs. Temperature

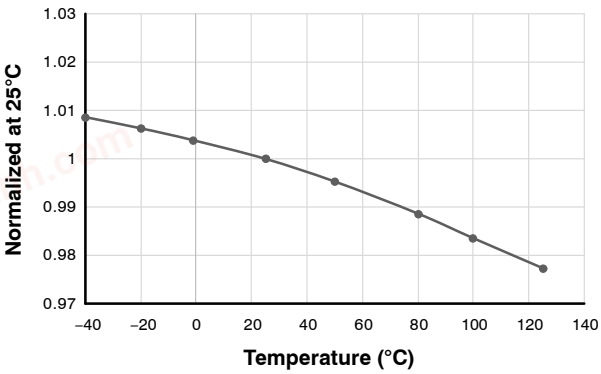


Figure 6. $g_{M(FB)}$ vs. Temperature

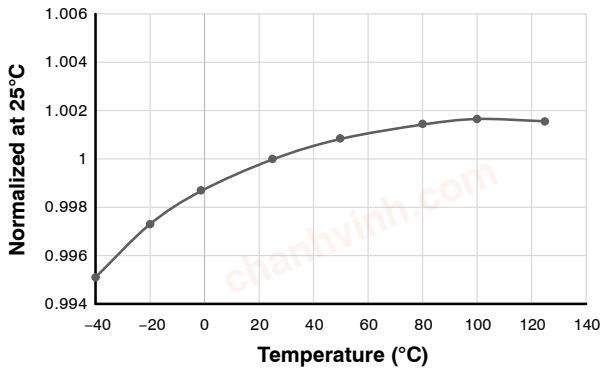


Figure 7. $V_{CS(REG−MAX)}$ vs. Temperature

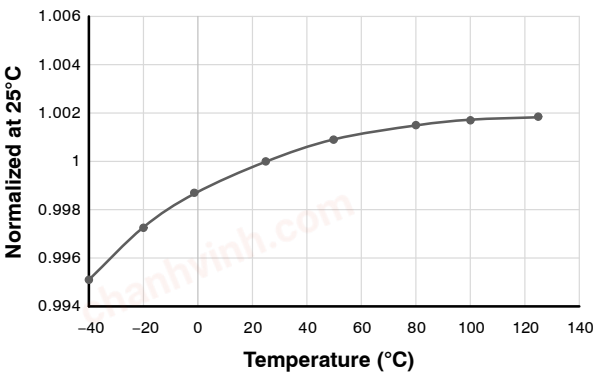


Figure 8. $V_{CS(LIM−MIN)}$ vs. Temperature

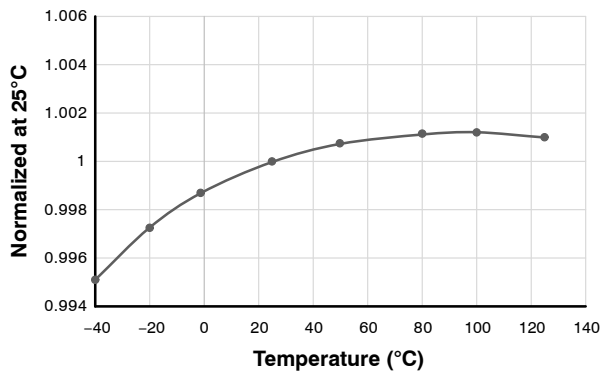


Figure 9. $V_{DD(OVP)}$ vs. Temperature

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APPLICATION INFORMATION

General

NCL35076 provides wide analog dimming down to 1% with high CC accuracy. According to buck inductor, input voltage and output voltage, deep dimming down to 0.1~0.2% load can be achieved. Thanks to the ON semiconductor's proprietary LED current calculation technique, NCL35076 is able to measure the current of LED load connected at input voltage node without the upper limit of the input voltage with high system reliability. LED current is sensed and regulated by internal zero input offset amplifiers so that NCL35076 performs precise CC regulation in the whole analog dimming range. Therefore, CC tolerance is tightly controlled in ±2% at 100% load and ±20% at 1% load.

Wide Analog Dimming

Wide analog dimming range is obtained by transitioning multi−mode between CCM and DCM according to the dimming condition. At full load condition, CCM with ±17% inductor current ripple minimizes the conduction loss with high efficiency and DCM is entered at light load condition to perform analog deep dimming. Dimming curve linearity is obtained by a digital compensator in the entire dimming range.

PWM Dimming

Analog dimming has benefits for less audible noise and flicker compared to PWM dimming. However, there is a need of PWM dimming method to keep the constant LED color temperature in specific applications. NCL35076 supports PWM dimming by simply inputting PWM dimming signal to DIM pin.

Precise CC Regulation

CC regulation is very important especially in programmable LED driver because the driver should keep precise CC control under the system variation of LED load, inductor, temperature, etc. Since NCL35076 applies zero input offset amplifiers at LED current calculator block and OTA, CC tolerance is less than ±2% at 100% load and ±20% at 1% load in the system variation.

Soft start

Without soft start in the closed loop CC control, the LED current overshoot is easily occurred at startup so that the overshoot can affect a lifetime of LEDs and incur an undesirable flash. NCL35076 provides soft start technique to prevent the LED current overshoot by T_{OFF} time control.

Standby Mode

When V_{DIM} is lower than a standby threshold voltage for 10 ms, standby mode is triggered with LED turn−off and IC current consumption is minimized.

Auto Restart (AR) at Protection

Once protection is triggered, IC operation stops for 1 second and begins soft start operation after the auto restart time delay.

VDD Over Voltage Protection (OVP)

When VDD is higher than 23 V, over voltage protection is triggered.

Short LED Protection (SLP)

When LED is short circuited, the buck stage operates in CCM with maximum turn−off time. By detecting this condition, short LED protection is triggered.

Over Current Protection (OCP)

When CSZCD voltage exceeds the over current threshold voltage, switching is immediately shut down after leading edge blanking time in the short circuit condition of the inductor, the freewheeling diode or the LED load.

Thermal Shot Down (TSD)

When IC junction temperature is higher than 150°C, TSD is triggered and released when the temperature is lower than 120°C.

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BASIC OPERATION

NCL35076 is the current mode buck controller in which DRV is off when V_{CSZCD} reaches to $V_{CS.LIM}$ (= V_{REF} + 30 mV) and DRV is on by T_{OFF} generator controlled by V_{FB}. V_{LED} is calculated based on V_{CSZCD} in precise LED current calculator block composed of zero input offset amplifiers and V_{REF} is controlled by DIM signal. In reference control block, V_{REF} is obtained by below equation.

$$V_{REF}\,[V] = \frac{V_{DIM} - 0.25\ V}{12.5} \qquad \text{(eq. 1)}$$

V_{LED} is compared with V_{REF} at OTA to generate V_{FB} which controls T_{OFF} time in T_{OFF} generator. T_{OFF} is inversely proportional to V_{FB}. Therefore, T_{OFF} is shorter as V_{FB} increases. T_{OFF} is set by below equation.

$$T_{OFF}\,[\mu s] = \frac{1.8}{V_{FB} - 1.1} + 0.1 \qquad \text{(eq. 2)}$$

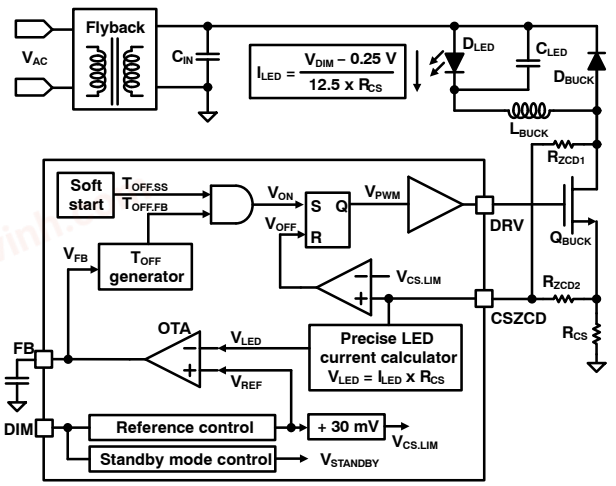


Figure 10. NCL35076 Block Diagram

Wide Analog Dimming

NCL35076 operates in CCM at heavy load and in DCM at light load for a wide analog dimming. Figure 11 shows how NCL35076 operates with V_{DIM}.

- A: $V_{CS.LIM}$ follows V_{REF} + 30 mV which is ±17% inductor current ripple at 2.5 V_{DIM}. V_{FB} is almost constant with same T_{OFF} in the CCM region.
- B: $V_{CS.LIM}$ is clamped to 80 mV and doesn't changed by V_{DIM}. T_{OFF} is lengthened for dimming as V_{FB} is decreased. Operating mode is transitioned from CCM to DCM at the boundary of A and B region.
- C: When V_{DIM} is lower than 0.25 V, V_{REF} is set to 0 V and V_{FB} is pulled down to 0.5 V clamping voltage with min. LED current under open loop control. When V_{DIM} is further lower than 0.1/0.075 V, standby is triggered with LED turn−off.

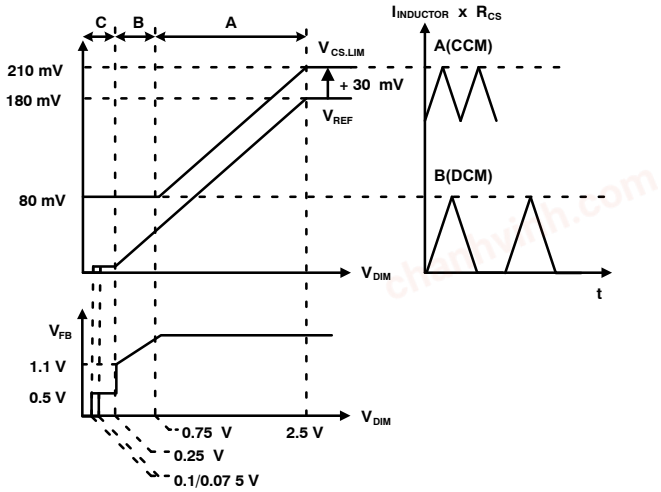


Figure 11. Operation Mode vs. V_{DIM}

Precise CC Regulation

The output of the precise LED current calculator, V_{LED}, is generated by analog sensing amplifiers and V_{LED} is compared with V_{REF} by OTA to generate V_{FB}. Those sensing amplifiers and OTA have zero input offset compensation technique which performs the excellent CC regulation.

Figure 12 shows dimming curves and CC tolerance. They are measured by changing inductor (±20%), temperature (−10, 25, 90°C) and output voltage (10, 30, 50 V) in 60 V input 75 W driver. As a result, CC tolerance at 1% deep dimming condition is less than ±10% and less than ±1.5% at full load condition.

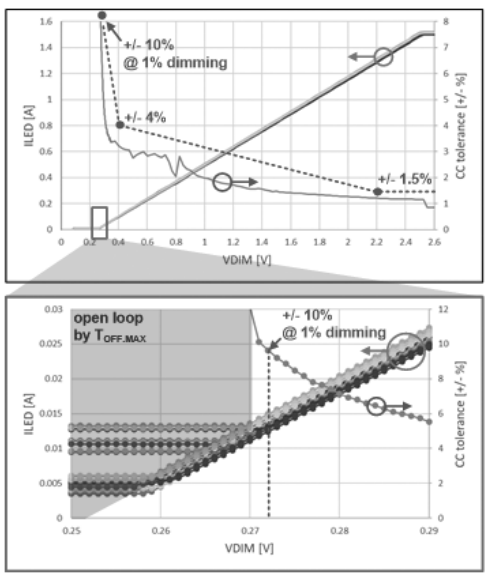


Figure 12. NCL35076 Dimming Curve and CC Tolerance

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Standby Mode

Standby mode is triggered by V_{DIM} as shown in Figure 13.

- A: When V_{DIM} is lower than $V_{DIM(SB-ENA)}$, DRV block is shut down. So, LED lamps turn off.
- B: After $t_{SB(DELAY)}$ (10 ms), standby mode is entered and NCL35076 current consumption drops to $I_{DD(SB)}$.
- C: When V_{DIM} is higher than $V_{DIM(SB-DIS)}$, standby mode is immediately terminated and IC starts up.

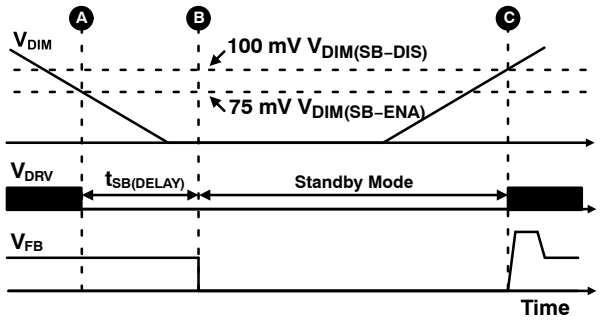


Figure 13. NCL35076 Standby Mode

Soft Start

During soft start operation, T_{OFF} is decided by either T_{OFF_SS} or T_{OFF_FB}. T_{OFF} is governed by T_{OFF_SS} in early start up because T_{OFF_SS} decreases from $t_{OFF(MAX)}$. When T_{OFF_SS} reaches to the steady state level, V_{FB} is settled to the regulation level and T_{OFF} is finally decided by T_{OFF_FB}. In the end of the soft start time, T_{OFF_SS} reaches to 0 and doesn't affect T_{OFF} control anymore. Figure 14 shows how the soft start operates.

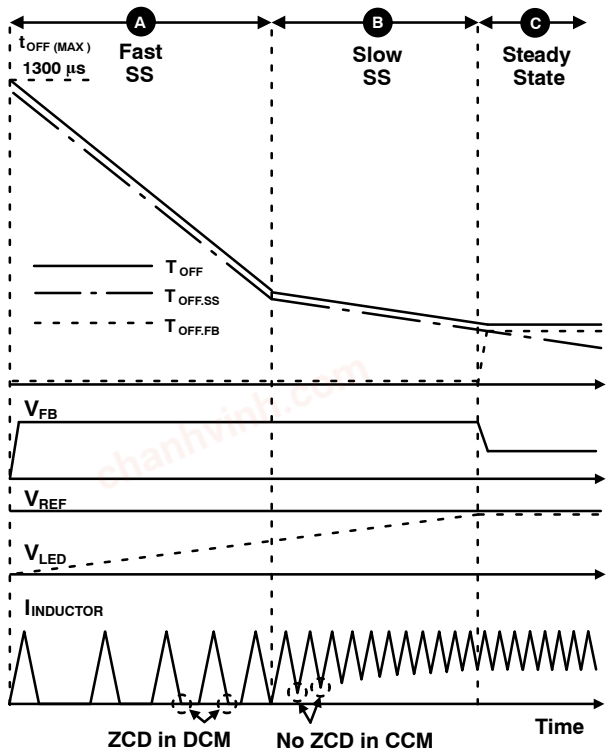


Figure 14. Soft Start Sequence

- A: V_{FB} is pulled up as V_{LED} is far below V_{REF}. T_{OFF_SS} is reduced quickly from $t_{OFF(MAX)}$ in Fast SS. Fast SS ends when inductor current zero cross (ZCD) is not detected.
- B: Slow SS starts when there is no ZCD in CCM.
- C: V_{LED} is closer to V_{REF}, and V_{FB} starts falling. Then, T_{OFF} is determined by T_{OFF_FB} and the steady state starts.

Protections

When protection is triggered, all functional blocks stop operating and begin to start up after 1 second AR time.

- VDD Over Voltage Protection (OVP)
  When VDD is higher than $V_{DD(OVP)}$ (23 V), VDD OVP is triggered. Open LED protection can be implemented by VDD OVP when VDD is supplied by auxiliary winding in the buck inductor.
- Over Current Protection (OCP)
  When CSZCD voltage is higher than $V_{CS(OCP)}$ (0.5 V) after leading edge blanking time, $t_{LEB(TON)}$ (400 ns), IC immediately shuts down.

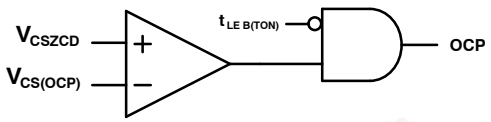
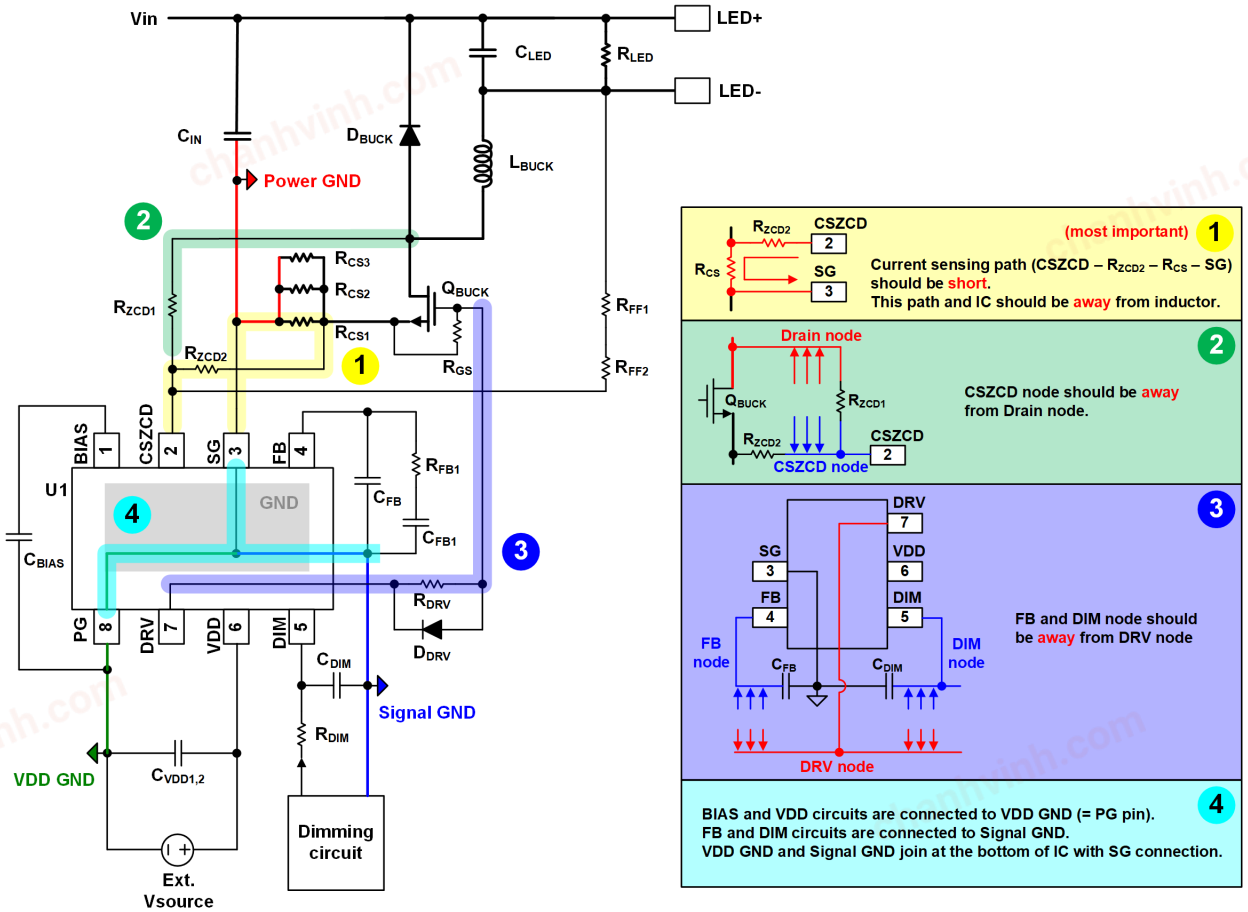


Figure 15. OCP Block

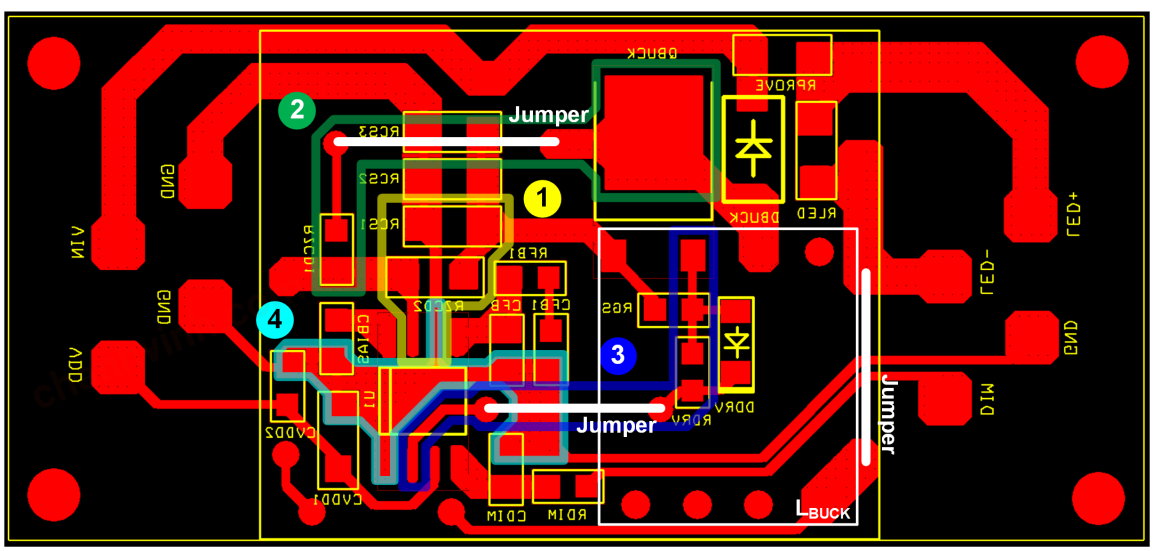
- Short LED Protection (SLP)
  When LED load is short−circuited, demagnetizing time of the inductor is very long due to zero output voltage so that T_{OFF} is lengthened and T_{ON} is very short. If CCM and $t_{OFF(MAX)}$ are detected for SLP monitoring time, $t_{SLP(MON-DEL)}$ (20 ms), SLP is triggered. In order to prevent abnormal SLP triggering at startup, SLP monitoring is disabled for $t_{SLP(MON-DIS)}$ (12 ms) after 1st switching begins.
- Thermal Shut Down (TSD)
  When the junction temperature is higher than T_{SD}, the system shuts down and the junction temperature is monitored at every 1 second delay time (AR time). When the temperature is lower than $T_{SD} - T_{SD(HYS)}$, the system restarts.

NCL35076

PCB LAYOUT GUIDANCE



(75−W Demo Board Schematic) (PCB Layout Guidance)



(75−W Demo Board PCB Layout − Bottom)

Figure 16. Layout Guidance

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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

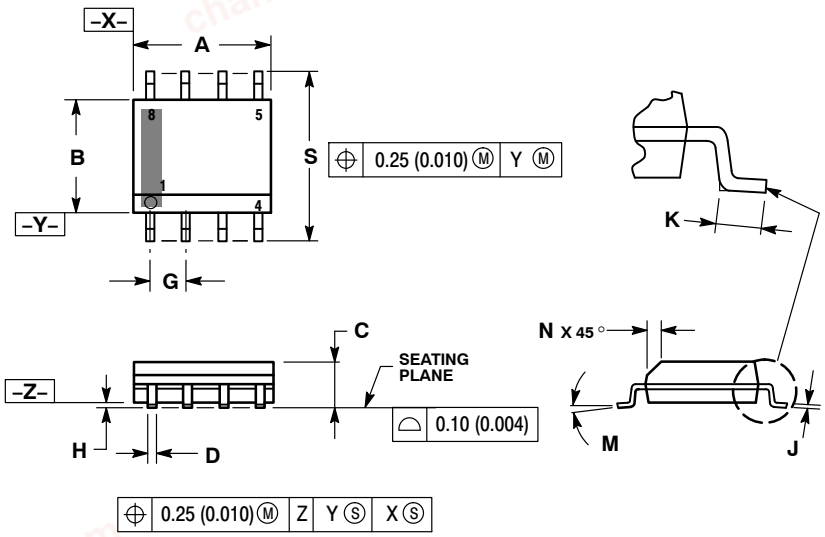
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SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

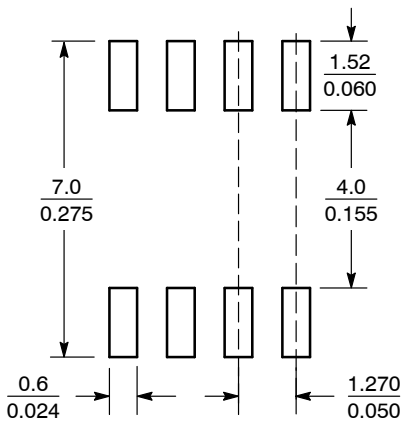
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

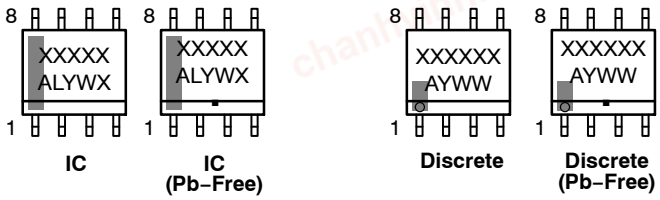
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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