chanhvinh.com

DATA SHEET
www.onsemi.com

Dimmable Power Factor Corrected LED Driver



SOIC−9 NB
CASE 751BP

Product Preview

NCL30486B

The NCL30486B is a power factor corrected flyback controller targeting isolated constant current LED drivers. The controller operates in a quasi−resonant mode to provide high efficiency. Thanks to a novel control method, the device is able to tightly regulate a constant LED current from the primary side. This removes the need for secondary side feedback circuitry, its biasing and for an optocoupler.

The device is highly integrated with a minimum number of external components. A robust suite of safety protection is built in to simplify the design. This device is specifically intended for very compact space efficient designs and supports analog and digital dimming with two dedicated dimming inputs control ideal for Smart LED Lighting applications.

Features

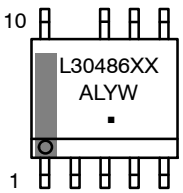
- High Voltage Startup
- Quasi−resonant Peak Current−mode Control Operation
- Primary Side Feedback
- CC / CV Accurate Control V_{in} up to 320 V rms
- Tight LED Constant Current Regulation of ±2% Typical
- Digital Power Factor Correction
- Analog and Digital Dimming
- Dimming Standby Mode (*Dim CV Mode*)
- Standby Mode
- Cycle by Cycle Peak Current Limit
- Wide Operating V_{CC} Range
- −40 to +125°C
- Robust Protection Features
  - Brown−Out
  - OVP on V_{CC}
  - Constant Voltage / LED Open Circuit Protection
  - Winding Short Circuit Protection
  - Secondary Diode Short Protection
  - Output Short Circuit Protection
  - Thermal Shutdown
  - Line over Voltage Protection
- This is a Pb−Free Device

Typical Applications

- Integral LED Bulbs
- LED Power Driver Supplies
- LED Light Engines

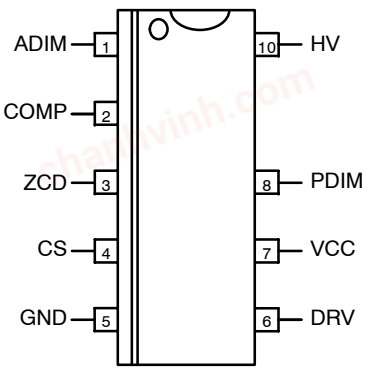
This document contains information on a product under development. **onsemi** reserves the right to change or discontinue this product without notice.

MARKING DIAGRAM



L30486	= Specific Device Code
XX	= Version
A	= Assembly Location
L	= Wafer Lot
YW	= Assembly Start Week
▪	= Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 30 of this data sheet.

© Semiconductor Components Industries, LLC, 2021

chanhvinh.com

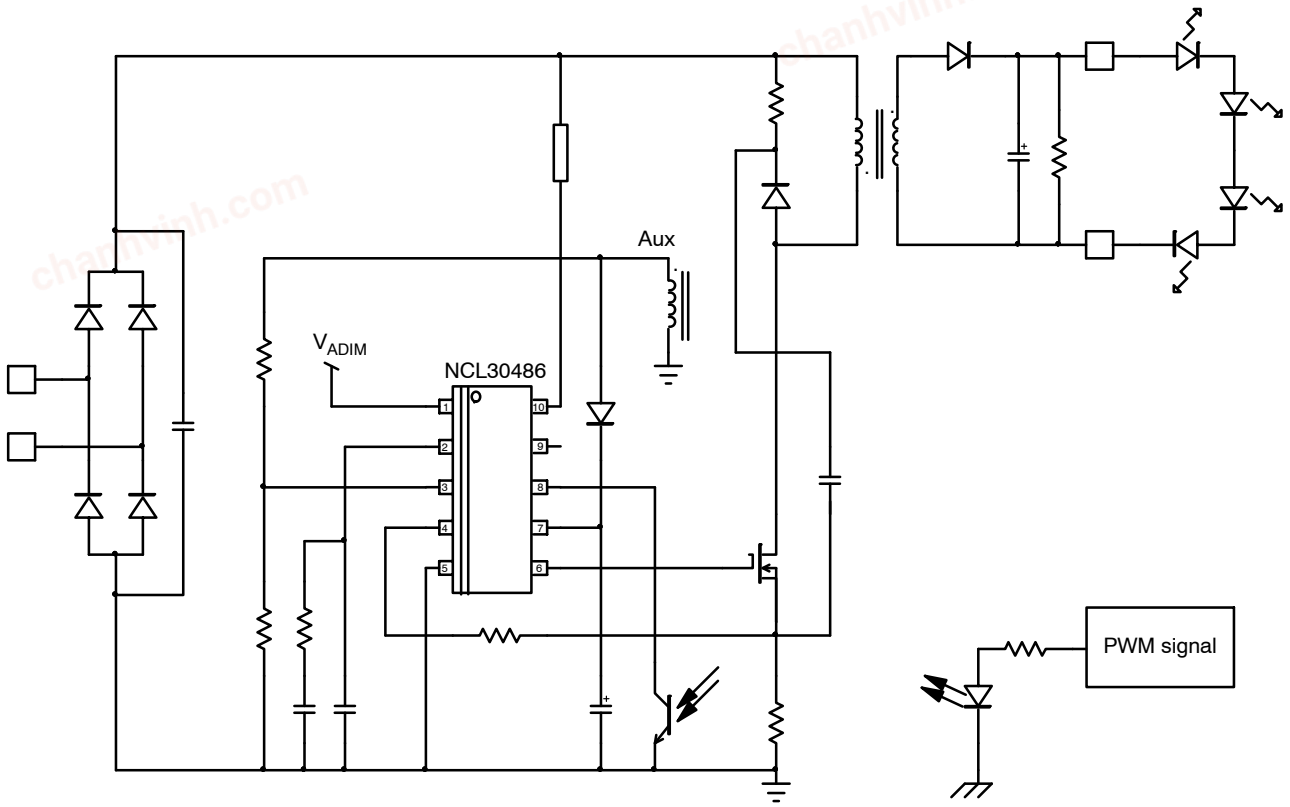


Figure 1. Typical Application Schematic for NCL30486B

PIN FUNCTION DESCRIPTION NCL30486B

Pin N°	Pin Name	Function	Pin Description
1	ADIM	Analog dimming	This pin is used for analog control of the output current. Applying a voltage varying between $V_{DIM(EN)}$ and V_{DIM100} will dim the output current from 0% to 100%.
2	COMP	OTA output for CV loop	This pin receives a compensation network to stabilize the constant voltage loop
3	ZCD	Zero crossing Detection V_{aux} sensing	This pin connects to the auxiliary winding and is used to detect the core reset event. This pin also senses the auxiliary winding voltage for accurate output voltage control
4	CS	Current sense	This pin monitors the primary peak current.
5	GND	–	The controller ground
6	DRV	Driver output	The driver's output to an external MOSFET
7	VCC	Supplies the controller	This pin is connected to an external auxiliary voltage.
8	PDIM	PWM dimming	This pin is used for PWM dimming control. An optocoupler can be connected directly to the pin if the PWM control signal is from the secondary side
9	NC	creepage	
10	HV	High Voltage sensing	This pin connects after the diode bridge to provide the startup current and internal high voltage sensing function.

chanhvinh.com

INTERNAL CIRCUIT ARCHITECTURE

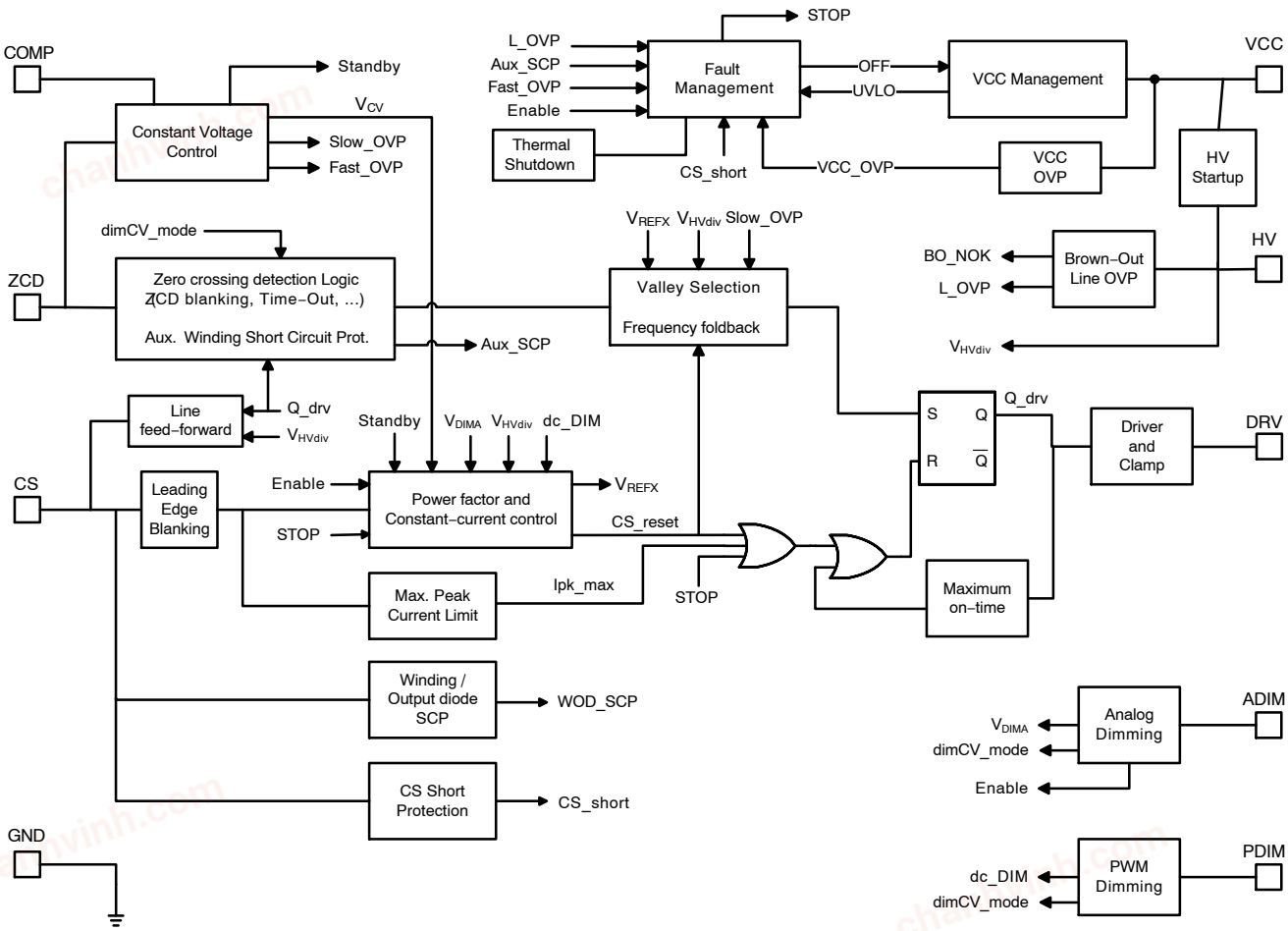


Figure 2. Internal Circuit Architecture NCL30486B

chanhvinh.com

MAXIMUM RATINGS TABLE

Symbol	Rating	Value	Unit
$V_{CC(MAX)}$ $I_{CC(MAX)}$	Maximum Power Supply Voltage, VCC Pin, Continuous Voltage Maximum Current for VCC Pin	−0.3 to 30 Internally limited	V mA
$V_{DRV(MAX)}$ $I_{DRV(MAX)}$	Maximum Driver Pin Voltage, DRV Pin, Continuous Voltage Maximum Current for DRV Pin	−0.3, V_{DRV} (Note 1) −300, +500	V mA
$V_{HV(MAX)}$ $I_{HV(MAX)}$	Maximum Voltage on HV Pin Maximum Current for HV Pin (dc Current Self−limited if Operated within the Allowed Range)	−0.3, +700 ±20	V mA
V_{MAX} I_{MAX}	Maximum Voltage on Low Power Pins (Except Pins DRV and VCC) Current Range for Low Power Pins (Except Pins DRV and VCC)	−0.3, 5.5 (Note 2) −2, +5	V mA
$R_{\theta J-A}$	Thermal Resistance Junction−to−Air	210	°C/W
$T_{J(MAX)}$	Maximum Junction Temperature	150	°C
	Operating Temperature Range	−40 to +125	°C
	Storage Temperature Range	−60 to +150	°C
	ESD Capability, HBM Model Except HV Pin (Note 3)	4	kV
	ESD Capability, HBM Model HV Pin	1.5	kV
	ESD Capability, CDM Model (Note 3)	1	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. V_{DRV} is the DRV clamp voltage $V_{DRV(high)}$ when V_{CC} is higher than $V_{DRV(high)}$. V_{DRV} is V_{CC} otherwise.
2. This level is low enough to guarantee not to exceed the internal ESD diode and 5.5 V ZENER diode. More positive and negative voltages can be applied if the pin current stays within the −2 mA / 5 mA range.
3. This device series contains ESD protection and exceeds the following tests: Human Body Model 4000 V per Mil−Std−883, Method 3015. Charged Device Model 1000 V per JEDEC Standard JESD22−C101D.
4. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: For typical values T_J = 25°C, V_{CC} = 12 V, V_{ZCD} = 0 V, V_{CS} = 0 V. For min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
HIGH VOLTAGE SECTION						
High Voltage Current Source	$V_{CC} = V_{CC(on)} - 200$ mV	$I_{HV(start2)}$	3.4	4.6	6.2	mA
High Voltage Current Source	V_{CC} = 0 V	$I_{HV(start1)}$	–	300	–	μA
V_{CC} Level for $I_{HV(start1)}$ to $I_{HV(start2)}$ Transition		$V_{CC(TH)}$	–	0.8	–	V
Minimum Startup Voltage	V_{CC} = 0 V	$V_{HV(MIN)}$	–	15	–	V
HV Source Leakage Current	V_{HV} = 450 V	$I_{HV(leak)}$	–	4.5	10	μA
Maximum Input Voltage (rms) for Correct Operation of the PFC Loop		$V_{HV(OL)}$	320	–	–	V rms
SUPPLY SECTION						
Supply Voltage Startup Threshold Minimum Operating Voltage Hysteresis $V_{CC(on)} - V_{CC(off)}$ Internal Logic Reset	 V_{CC} increasing V_{CC} decreasing V_{CC} decreasing	 $V_{CC(on)}$ $V_{CC(off)}$ $V_{CC(HYS)}$ $V_{CC(reset)}$	 16 9.3 7.6 4	 18 10.2 – 5	 20 10.7 – 6	V
Over Voltage Protection VCC OVP Threshold		$V_{CC(OVP)}$	25	26.5	28	V
$V_{CC(off)}$ Noise Filter (Note 5) $V_{CC(reset)}$ nOise Filter (Note 5)		$t_{VCC(off)}$ $t_{VCC(reset)}$	– –	5 20	– –	μs
Supply Current Device Disabled/Fault Device Enabled/No Output Load on Pin 5 Device Switching (F_{sw} = 65 kHz) Device Switching (F_{sw} = 700 Hz)	 $V_{CC} > V_{CC(off)}$ F_{sw} = 65 kHz C_{DRV} = 470 pF, F_{sw} = 65 kHz $V_{COMP} \le 0.9$ V	 I_{CC1} I_{CC2} I_{CC3} I_{CC4}	 1.1 – – –	 1.4 3.3 3.6 1.7	 1.7 3.9 4.3 2	mA

chanhvinh.com

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: For typical values T_J = 25°C, V_{CC} = 12 V, V_{ZCD} = 0 V, V_{CS} = 0 V. For min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V) (continued)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
CURRENT SENSE						
Maximum Internal Current Limit		V_{ILIM}	1.28	1.40	1.50	V
Leading Edge Blanking Duration for V_{ILIM}		t_{LEB}	240	300	360	ns
Propagation Delay from Current Detection to Gate Off−state		t_{ILIM}	–	50	150	ns
Maximum On−time OPN1		$t_{on(MAX)1}$	10.5	14.0	17.5	μs
Maximum On−time OPN2		$t_{on(MAX)2}$	16	20	24	μs
Maximum On−time V_{REFX} < 0.15 V (OPN1)		$t_{on(MAX)12}$	5.3	7.0	8.7	μs
Maximum On−time V_{REFX} < 0.15 V (OPN2)		$t_{on(MAX)22}$	8	10	12	μs
Threshold for Immediate Fault Protection Activation (140% of V_{ILIM})		$V_{CS(stop)}$	1.9	2.0	2.1	V
Leading Edge Blanking Duration for $V_{CS(stop)}$		t_{BCS}	–	170	–	ns
Current Source for CS to GND Short Detection		$I_{CS(short)}$	400	500	600	μA
Current Sense Threshold for CS to GND Short Detection	V_{CS} rising	$V_{CS(low)}$	20	60	90	mV
Maximum Peak Current in Standby Mode Option 1 Option 2 Option 3		$V_{CS(SBY)}$	 342 297 252	 380 330 280	 418 363 308	mV
GATE DRIVE						
Drive Resistance DRV Sink DRV Source		 R_{SNK} R_{SRC}	 – –	 13 30	 – –	Ω
Drive Current Capability DRV Sink (Note GBD) DRV Source (Note GBD)		 I_{SNK} I_{SRC}	 – –	 500 300	 – –	mA
Rise Time (10% to 90%)	C_{DRV} = 470 pF	t_r	–	30	–	ns
Fall Time (90 %to 10%)	C_{DRV} = 470 pF	t_f	–	20	–	ns
DRV Low Voltage	V_{CC} = $V_{CC(off)}$+0.2 V C_{DRV} = 470 pF, R_{DRV} = 33 kΩ	$V_{DRV(low)}$	8	–	–	V
DRV High Voltage	V_{CC} = $V_{CC(MAX)}$ C_{DRV} = 470 pF, R_{DRV} = 33 kΩ	$V_{DRV(high)}$	10	12	14	V
ZERO VOLTAGE DETECTION CIRCUIT						
Upper ZCD Threshold Voltage	V_{ZCD} rising	$V_{ZCD(rising)}$	–	90	150	mV
Lower ZCD Threshold Voltage	V_{ZCD} falling	$V_{ZCD(falling)}$	35	55	–	mV
Threshold to Force V_{REFX} Maximum During Startup		$V_{ZCD(start)}$	–	0.7	–	V
ZCD Hysteresis		$V_{ZCD(HYS)}$	15	–	–	mV
Propagation Delay from Valley Detection to DRV High	V_{ZCD} decreasing	$t_{ZCD(DEM)}$	–	–	150	ns
Equivalent Time Constant for ZCD Input (GBD)		t_{PAR}	–	20	–	ns
Blanking Delay after On−time (option 1)	V_{REFX} > 0.35 V	$t_{ZCD(blank1)}$	1.1	1.5	1.9	μs
Blanking Delay after On−time (option 2)	V_{REFX} > 0.35 V	$t_{ZCD(blank1)}$	0.75	1.0	1.25	μs
Blanking Delay at Light Load (option 1)	V_{REFX} < 0.25 V	$t_{ZCD(blank2)}$	0.6	0.8	1.0	μs
Blanking Delay at Light Load (option 2)	V_{REFX} < 0.25 V	$t_{ZCD(blank2)}$	0.45	0.6	0.75	μs
Timeout after Last DEMAG Transition		t_{TIMO}	5	6.5	8	μs
Time−out after Last DEMAG Transition V_{ZCD} < $V_{ZCD(start)}$ (Note 5)		$t_{TIMOstart}$	–	50	–	μs
Pulling−down Resistor	V_{ZCD} = $V_{ZCD(falling)}$	$R_{ZCD(pd)}$	–	200	–	kΩ
ZCD Pin Current Source for Forcing CV Mode when Minimum Dimming	V_{ADIM} = 0.5 V	I_{ZCDdim}	140	165	190	μA

chanhvinh.com

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: For typical values T_J = 25°C, V_{CC} = 12 V, V_{ZCD} = 0 V, V_{CS} = 0 V. For min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V) (continued)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
CONSTANT CURRENT CONTROL						
Reference Voltage	T_j = 25°C – 85°C	$V_{REF/3}$	327.9	334.2	341.2	mV
Reference Voltage	T_j = −40°C to 125°C	$V_{REF/3}$	324.1	334.2	346.0	mV
10% Reference Voltage	T_j = 25°C – 85°C	$V_{REF10/3}$	30	33.33	36.66	mV
10% Reference Voltage	T_j = −40°C to 125°C	$V_{REF10/3}$	27.33	33.33	39.33	mV
5% Reference Voltage	T_j = 25°C – 85°C	$V_{REF05/3}$	14.17	17	19.17	mV
5% Reference Voltage	T_j = −40°C to 125°C	$V_{REF05/3}$	13.34	17	20	mV
Current Sense Lower Threshold for Detection of the Leakage Inductance Reset Time	V_{CS} falling	$V_{CS(low)}$	20	50	100	mV
Blanking Time for Leakage Inductance Reset Detection		$t_{CS(low)}$	–	120	–	ns
POWER FACTOR CORRECTION						
Clamping Value for $V_{REF(PFC)}$	T_J = 0°C to 125°C	$V_{REF(PFC)CLP}$	2.06	2.20	2.34	V
Line Range Detector for PFC Loop	V_{HV} increases	$V_{HL(PFC)}$	–	240	–	Vdc
Line Range Detector for PFC Loop	V_{HV} decreases	$V_{LL(PFC)}$	–	230	–	Vdc
CONSTANT VOLTAGE SECTION						
Internal Voltage Reference for Constant Voltage Regulation		$V_{REF(CV)}$	3.41	3.52	3.63	V
CV Error Amplifier Gain		G_{EA}	40	50	60	μS
Error Amplifier Current Capability	V_{REFX} = V_{REF} (no dimming)	I_{EA}	–	±60	–	μA
COMP Pin Lower Clamp Voltage		$V_{CV(clampL)}$	–	0.6	–	V
COMP Pin Higher Clamp Voltage	T_J = 0°C to 125°C	$V_{CV(clampH)}$	4.05	4.12	4.25	V
COMP Pin Higher Clamp Voltage	T_J = −40°C to 125°C	$V_{CV(clampH)}$	4.01	4.12	4.25	V
Internal ZCD Voltage below which the CV OTA is Boosted	$V_{REF(CV)}$ * 85%	$V_{boost(CV)}$	2.796	2.975	3.154	V
Threshold for Releasing the CV Boost	$V_{REF(CV)}$ * 90%	$V_{boost(CV)RST}$	2.96	3.15	3.34	V
Error Amplifier Current Capability During Boost Phase		$I_{EAboost}$	–	±140	–	μA
ZCD OVP 1st Level (Slow OVP) Option 1	$V_{REF(CV)}$ * 115%	V_{OVP1}	3.783	4.025	4.267	V
ZCD Voltage at which Slow OVP is Exit (Option 1)	$V_{REF(CV)}$ * 105%	$V_{OVP1rst}$	–	3.675	–	V
Switching Period During Slow OVP		$T_{sw(OVP1)}$	–	1.5	–	ms
ZCD Fast OVP Option 1	$V_{ref(CV)}$ * 125% + 150 mV	V_{OVP2}	4.253	4.525	4.797	V
Number of Switching Cycles before Fast OVP Confirmation		T_{OVP2_CNT}	–	4	–	
Duration for Disabling DRV Pulses During ZCD Fast OVP		$T_{recovery}$	–	4	–	s
COMP Pin Voltage below which Standby Mode is Entered (Note 5)	V_{COMP} decreasing	$V_{CMP(SBY)}$	–	0.895	–	V
COMP Standby Comparator Hysteresis (Note 5)	V_{COMP} increasing	$V_{CMP(SBY)HYS}$	–	18	–	mV
LINE FEED FORWARD						
V_{HV} to $I_{CS(offset)}$ Conversion Ratio		K_{LFF}	0.189	0.21	0.231	μA/V
Offset Current Maximum Value	V_{HV} > (450 V or 500 V)	$I_{offset(MAX)}$	76	95	114	μA
Line Feed−forward Current	DRV high, V_{HV} = 200 V	I_{FF}	35	40	45	μA
VALLEY LOCKOUT SECTION						
Threshold for Line Range Detection V_{HV} Increasing (1st to 2nd Valley Transition for V_{REFX} > 80% V_{REF}) (Prog. Option: 1st to 3rd Valley Transition)	V_{HV} increases	V_{HL}	228	240	252	V
Threshold for Line Range Detection V_{HV} Decreasing (2nd to 1st Valley Transition for V_{REFX} > 80% V_{REF}) (Prog. Option: 3rd to 1st Valley Transition)	V_{HV} decreases	V_{LL}	218	230	242	V
Blanking Time for Line Range Detection		$t_{HL(blank)}$	15	25	35	ms

chanhvinh.com

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: For typical values T_J = 25°C, V_{CC} = 12 V, V_{ZCD} = 0 V, V_{CS} = 0 V. For min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V) (continued)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
VALLEY LOCKOUT SECTION						
Valley Thresholds 1st to 2nd Valley Transition at LL and 2nd to 3rd Valley HL, V_{REF} Decr. (Prog. Option: 3rd to 4th Valley HL) 2nd to 1st Valley Transition at LL and 3rd to 2nd Valley HL, V_{REF} Incr. (Prog. Option: 4th to 3rd Valley HL) 2nd to 3rd Valley Transition at LL and 3rd to 4th Valley HL, V_{REF} Decr. (Prog. Option: 4th to 5th Valley HL) 3rd to 2nd Valley Transition at LL and 4th to 3rd Valley HL, V_{REF} Incr. (Prog. Option: 5th to 4th Valley HL) 3rd to 4th Valley Transition at LL and 4th to 5th Valley HL, V_{REF} Decr. (Prog. Option: 5th to 6th Valley HL) 4th to 3th Valley Transition at LL and 5th to 4th vAlley HL, V_{REF} Incr. (Prog. Option: 6th to 5th Valley HL) 4th to 5th Valley Transition at LL and 5th to 6th Valley HL, V_{REF} Decr. (Prog. Option: 6th to 7th Valley HL) 5th to 4th Valley Transition at LL and 6th to 5th Valley HL, V_{REF} Incr. (Prog. Option: 7th to 6th Valley HL)	V_{REF} decreases V_{REF} increases V_{REF} decreases V_{REF} increases V_{REF} decreases V_{REF} increases V_{REF} decreases V_{REF} increases	$V_{VLY1-2/2-3}$ $V_{VLY2-1/3-2}$ $V_{VLY2-3/3-4}$ $V_{VLY3-2/4-3}$ $V_{VLY3-4/4-5}$ $V_{VLY4-3/5-4}$ $V_{VLY4-5/5-6}$ $V_{VLY5-4/6-5}$	– – – – – – – –	0.80 0.90 0.65 0.75 0.50 0.60 0.35 0.45	– – – – – – – –	V
V_{REF} Value at which the FF Mode is Activated	V_{REF} decreases	$V_{FFstart}$	–	0.25	–	V
V_{REF} Value at which the FF Mode is Removed	V_{REF} increases	V_{FFstop}	–	0.35	–	V
FREQUENCY FOLDBACK						
Added Dead Time (Note 5)	V_{REFX} = 0.25 V	t_{FF1LL}	–	2	–	μs
Added Dead Time (Note 5)	V_{REFX} = 0.08 V	t_{FFchg}	–	35	–	μs
Dead−time Clamp (Option 1) (Note 5)	V_{REFX} < 3 mV	t_{FFend1}	–	687	–	μs
Dead−time Clamp (Option 2) (Note 5)	V_{REFX} < 11.2 mV	t_{FFend2}	–	250	–	μs
Minimum Added Dead−time in Standby (Note 5)	V_{REFX} = 0	$t_{DT(min)SBY}$	–	640	–	μs
Maximum Added Dead−time in Standby (Option 2) (Note 5)	V_{REFX} = 0, V_{COMP} < 0.7 V	$t_{DT(max)SBY2}$	–	1.8	–	ms
V_{REFX} Threshold below which Valley Synchronization in Frequency Foldback is Turned Off (Note 5)	V_{REFX} decreasing	$V_{REFXsyncD}$	0.14	0.15	0.16	V
V_{REFX} Threshold above which Valley Synchronization in Frequency Foldback is Turned On (Note 5)	V_{REFX} increasing	$V_{REFXsyncI}$	0.165	0.18	0.195	V
DIMMING SECTION						
DIM Pin Voltage for Zero Output Current (OFF Voltage)		$V_{ADIM(EN)}$	0.475	0.5	0.525	V
ADIM Pin Voltage for 1% Reference Voltage		$V_{ADIM(MIN)}$	0.668	0.7	0.732	V
Minimum Dimming Level (Option 1)		$K_{DIM(MIN)1}$	–	0	–	%
Minimum Dimming Level (Option 2)		$K_{DIM(MIN)2}$	–	1	–	%
Minimum Dimming Level (Option 3)		$K_{DIM(MIN)3}$	–	5	–	%
Minimum Dimming Level (Option 4)		$K_{DIM(MIN)4}$	–	8	–	%
ADIM Pin Voltage for Maximum Output Current (V_{REFX} = 1 V)		$V_{ADIM100}$	–	3.0	3.1	V
Dimming Range		$V_{ADIM(range)}$	–	2.3	–	V
Clamping Voltage for DIM Pin		$V_{ADIM(CLP)}$	–	6.8	–	V
Dimming Pin Pull−up Current Source		$I_{ADIM(pullup)1}$	8	10	12	μA
Current Comparator Low Threshold for PDIM		$I_{PDIM(THR)}$	60	70	80	μA
Current Comparator High Threshold for PDIM		$I_{PDIM(THD)}$	131	153	175	μA
Cascode Current Limit for PDIM		$I_{PDIM(LIM)}$	–	1080	–	μA
PDIM Pin Voltage		V_{PDIM}	–	3	–	V
Maximum Period of the PWM Dimming Signal			–	6	–	ms
Minimum On−time for PWM Signal Applied on PDIM			–	8	–	μs

chanhvinh.com

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: For typical values T_J = 25°C, V_{CC} = 12 V, V_{ZCD} = 0 V, V_{CS} = 0 V. For min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V) (continued)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
FAULT PROTECTION						
Thermal Shutdown (Note 5)	Device switching (F_{SW} around 65 kHz)	T_{SHDN}	130	150	170	°C
Thermal Shutdown Hysteresis		$T_{SHDN(HYS)}$	–	20	–	°C
Threshold Voltage for Output Short Circuit or Aux. Winding Short Circuit Detection		$V_{ZCD(short)}$	0.6	0.65	0.7	V
Short Circuit Detection Timer	$V_{ZCD} < V_{ZCD(short)}$	t_{OVLD}	70	90	110	ms
Auto−recovery Timer		$t_{recovery}$	3	4	5	s
Line OVP Threshold	V_{HV} increasing	$V_{HV(OVP)}$	457	469	485	Vdc
HV Pin Voltage at which Line OVP is Reset	V_{HV} decreasing	$V_{HV(OVP)RST}$	430	443	465	Vdc
Blanking Time for Line OVP Reset		$T_{LOVP(blank)}$	210	340	470	ms
BROWN−OUT AND LINE SENSING						
Brown−Out ON Level (IC Start Pulsing)	V_{HV} increasing	$V_{HVBO(on)}$	101.5	108	114.5	Vdc
Brown−Out ON Level (IC Start Pulsing) Option 2	V_{HV} increasing	$V_{HVBO(on)2}$	129.7	138	146.3	Vdc
Brown−Out OFF Level (IC Stops Pulsing)	V_{HV} decreasing	$V_{HVBO(off)}$	92	99	106	Vdc
Brown−Out OFF Level (IC Stops Pulsing) Option 2	V_{HV} decreasing	$V_{HVBO(off)2}$	121	129	137	Vdc
HV Pin Voltage above which the Sampling of ZCD is Enabled Low Line	V_{HV} decreasing, low line	$V_{sampENLL}$	–	55	–	V
HV Pin Voltage above which the Sampling of ZCD is Enabled Highline	V_{HV} decreasing, highline	$V_{sampENHL}$	–	105	–	V
ZCD Sampling Enable Comparator Hysteresis	V_{HV} increasing	$V_{sampHYS}$	–	5	–	V
BO Comparators Delay		$t_{BO(delay)}$	–	30	–	μs
Brown−Out Blanking Time		$t_{BO(blank)}$	15	25	35	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Guaranteed by design.

chanhvinh.com

TYPICAL CHARACTERISTICS

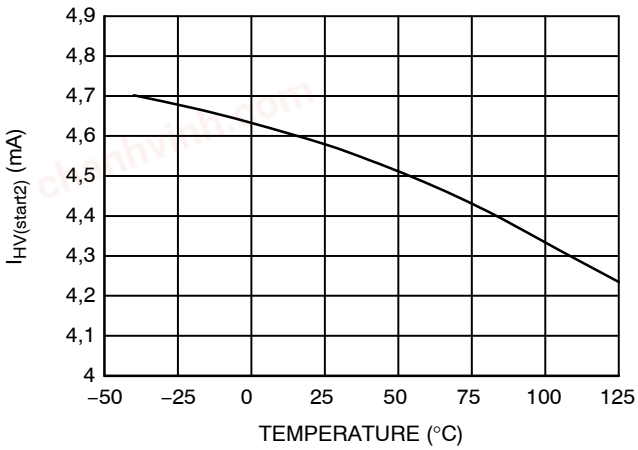


Figure 3. $I_{HV(start2)}$ vs. Temperature

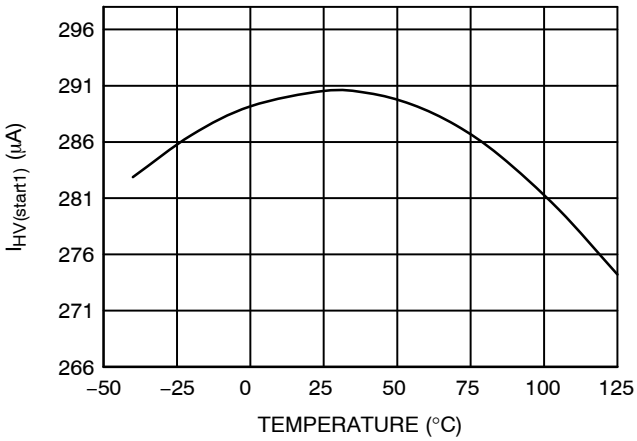


Figure 4. $I_{HV(start1)}$ vs. Temperature

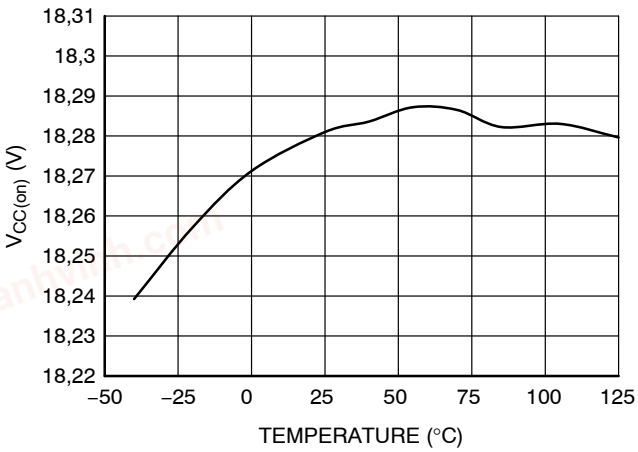


Figure 5. $V_{CC(on)}$ vs. Temperature

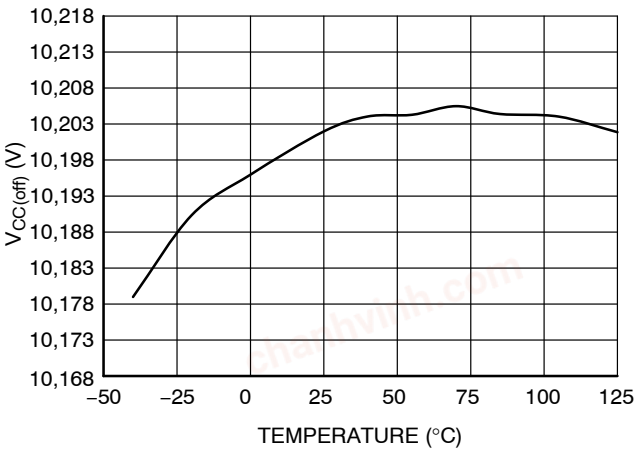


Figure 6. $V_{CC(off)}$ vs. Temperature

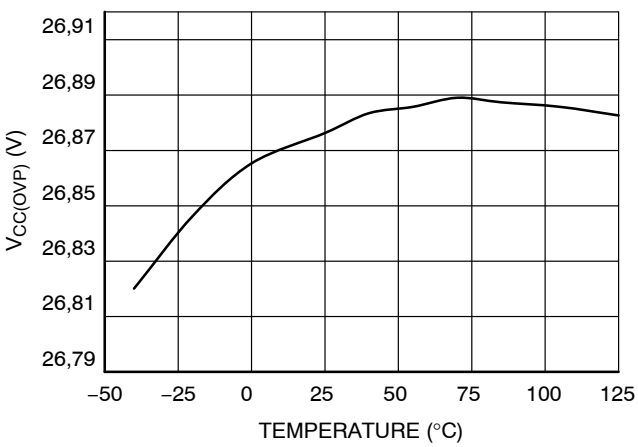


Figure 7. $V_{CC(OVP)}$ vs. Temperature

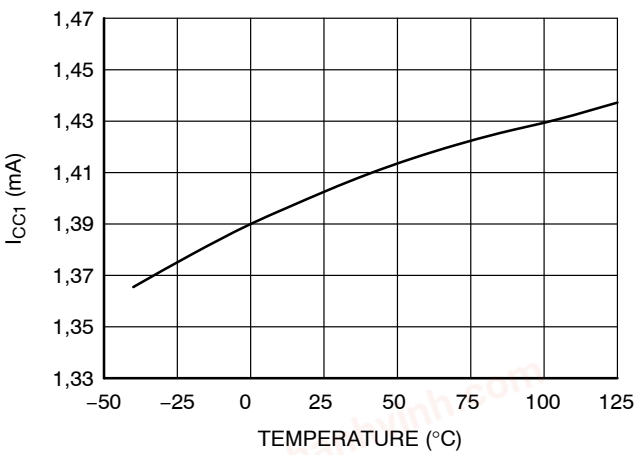


Figure 8. I_{CC1} vs. Temperature

chanhvinh.com

TYPICAL CHARACTERISTICS (continued)

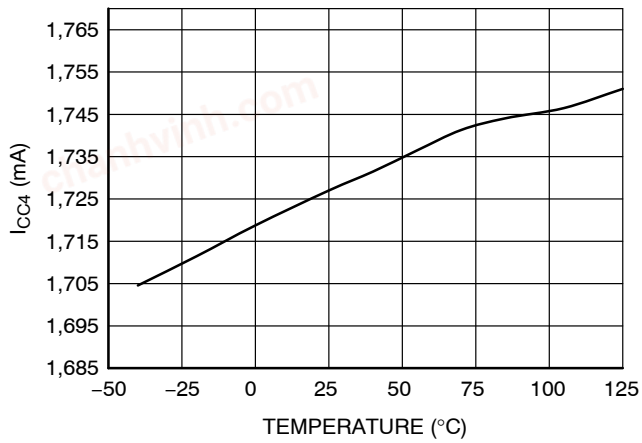


Figure 9. I_{CC4} vs. Temperature

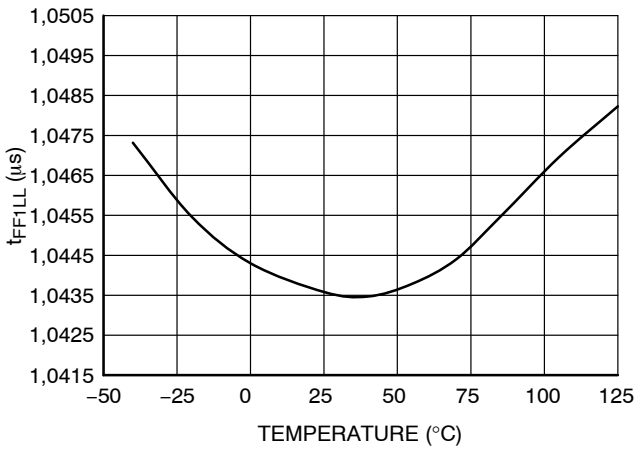


Figure 10. t_{FF1LL} vs. Temperature

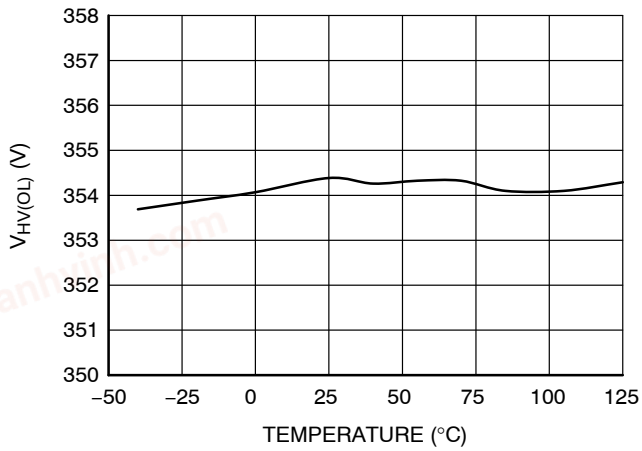


Figure 11. $V_{HV(OL)}$ vs. Temperature

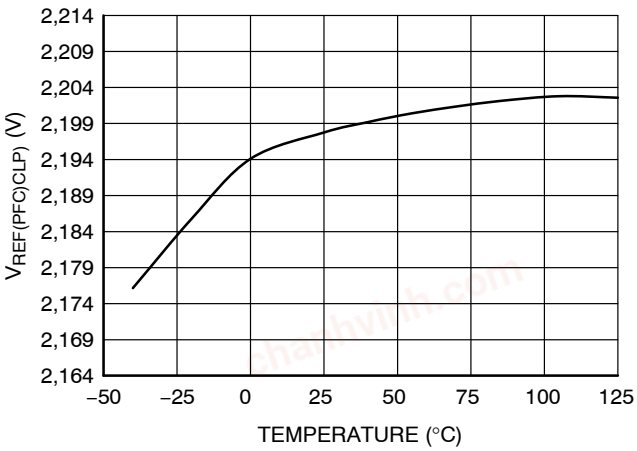


Figure 12. $V_{REF(PFC)CLP}$ vs. Temperature

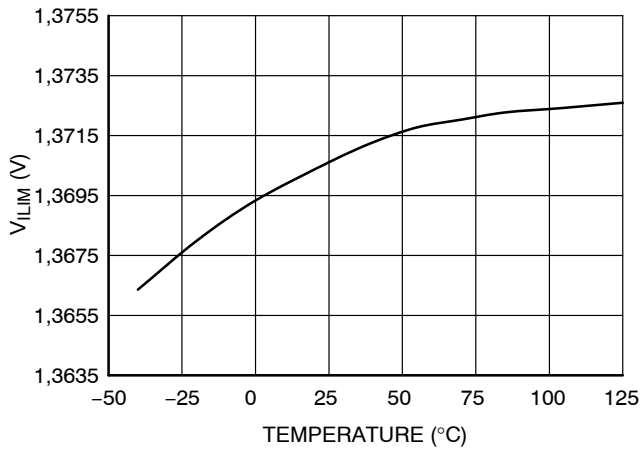


Figure 13. V_{ILIM} vs. Temperature

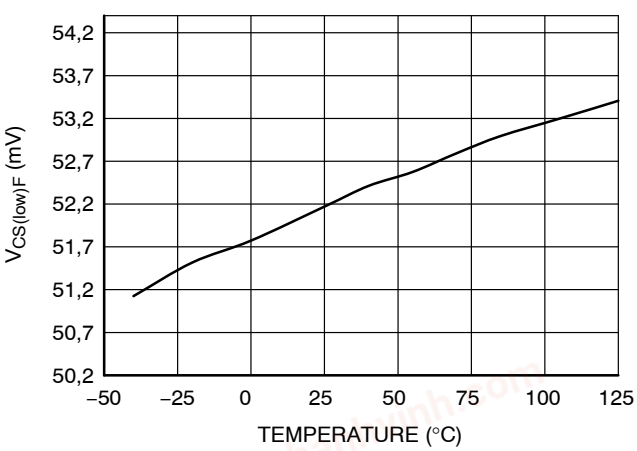


Figure 14. $V_{CS(low)F}$ vs. Temperature

chanhvinh.com

TYPICAL CHARACTERISTICS (continued)

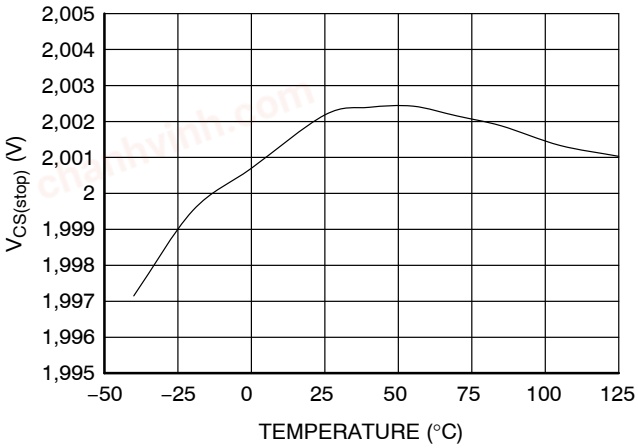


Figure 15. $V_{CS(stop)}$ vs. Temperature

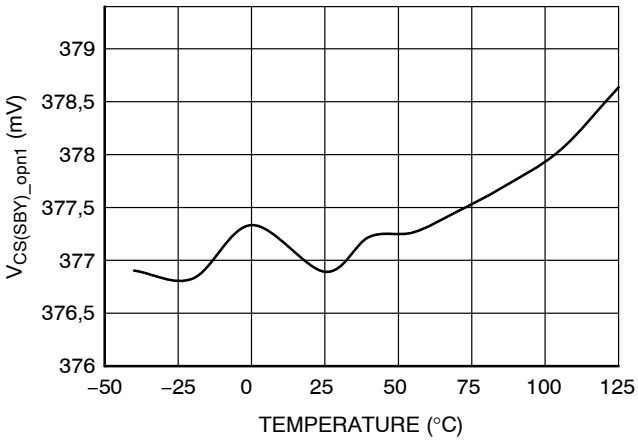


Figure 16. $V_{CS(SBY)_opn1}$ vs. Temperature

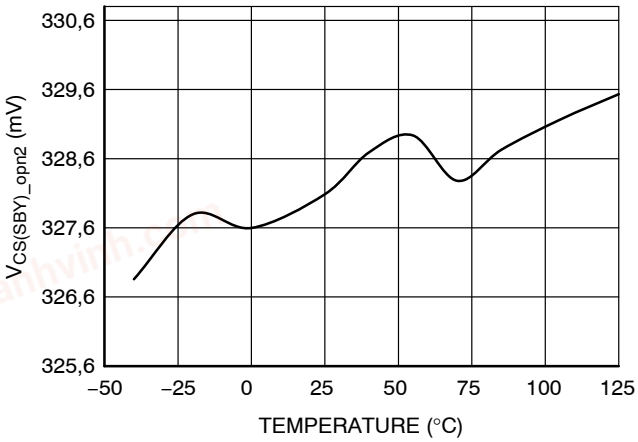


Figure 17. $V_{CS(SBY)_opn2}$ vs. Temperature

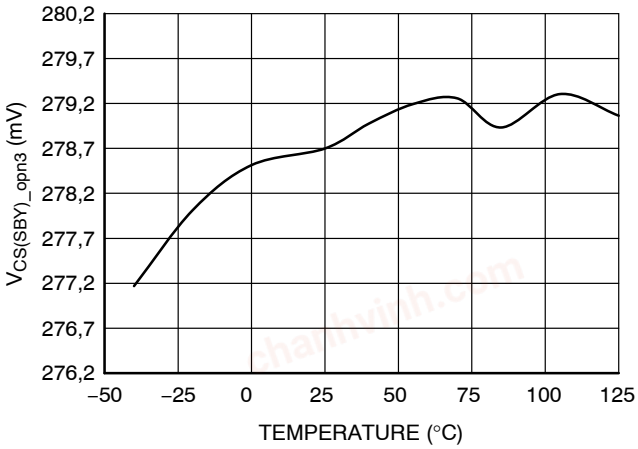


Figure 18. $V_{CS(SBY)_opn3}$ vs. Temperature

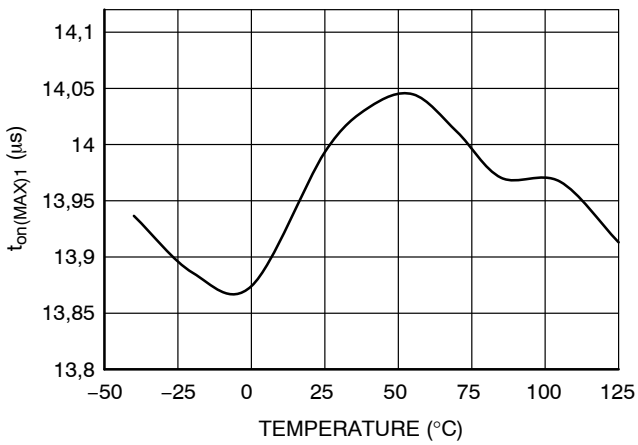


Figure 19. $t_{on(MAX)1}$ vs. Temperature

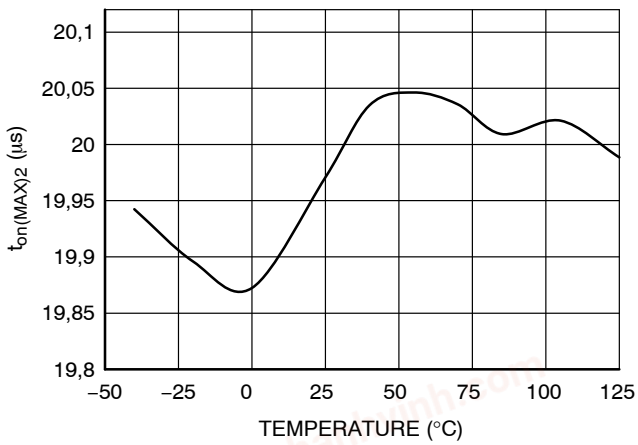


Figure 20. $t_{on(MAX)2}$ vs. Temperature

chanhvinh.com

TYPICAL CHARACTERISTICS (continued)

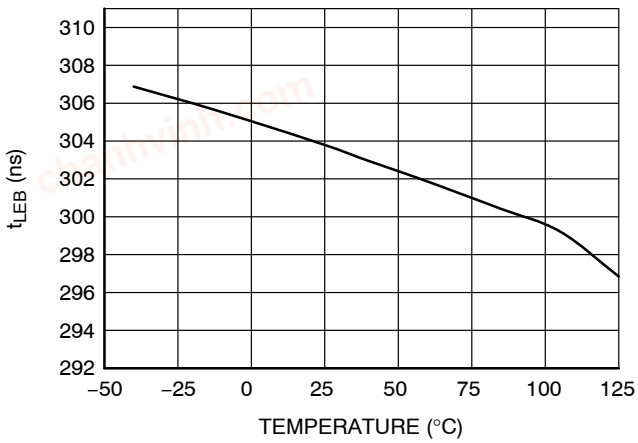


Figure 21. t_{LEB} vs. Temperature

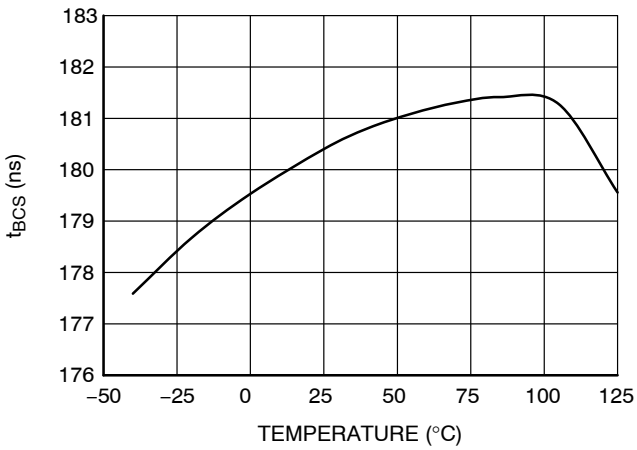


Figure 22. t_{BCS} vs. Temperature

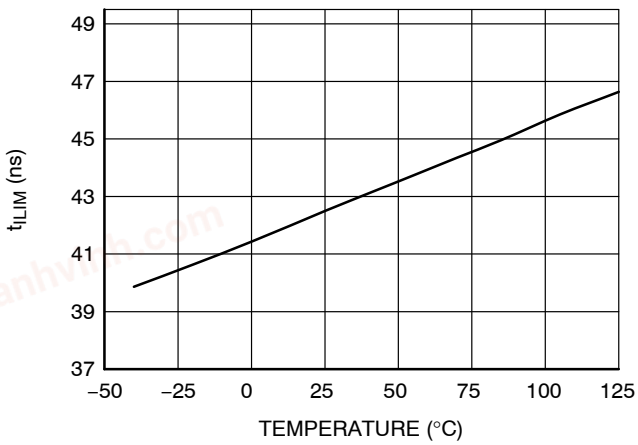


Figure 23. t_{ILIM} vs. Temperature

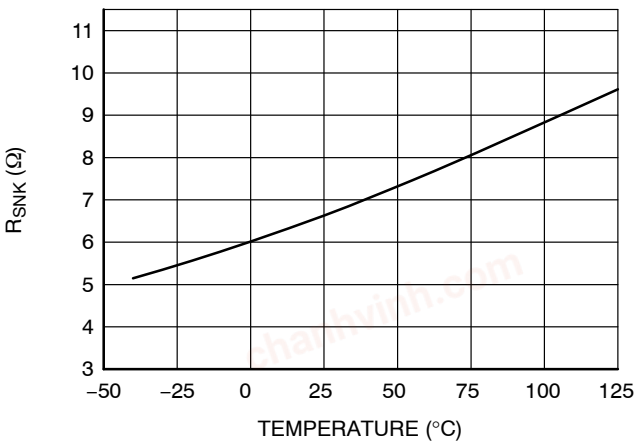


Figure 24. R_{SNK} vs. Temperature

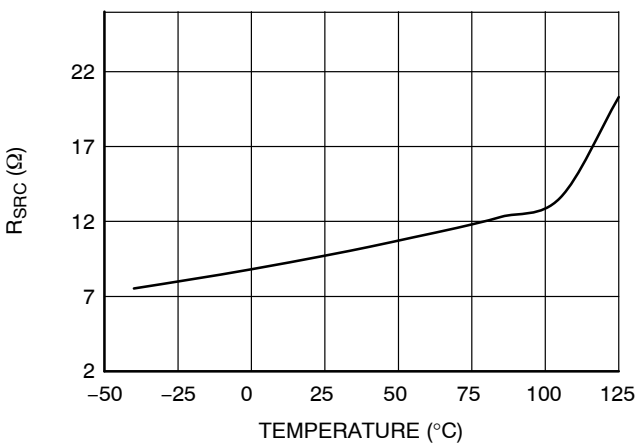


Figure 25. R_{SRC} vs. Temperature

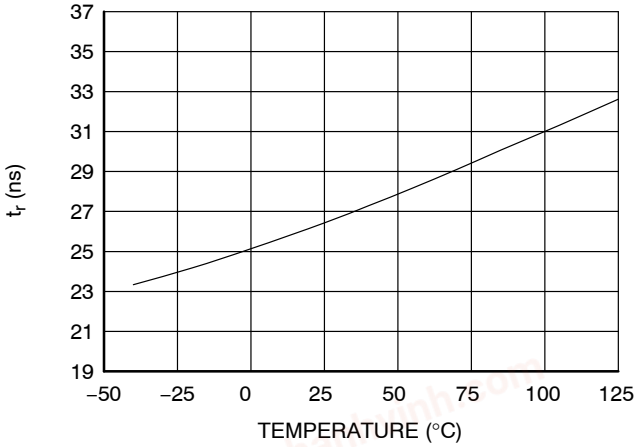


Figure 26. t_r vs. Temperature

chanhvinh.com

TYPICAL CHARACTERISTICS (continued)

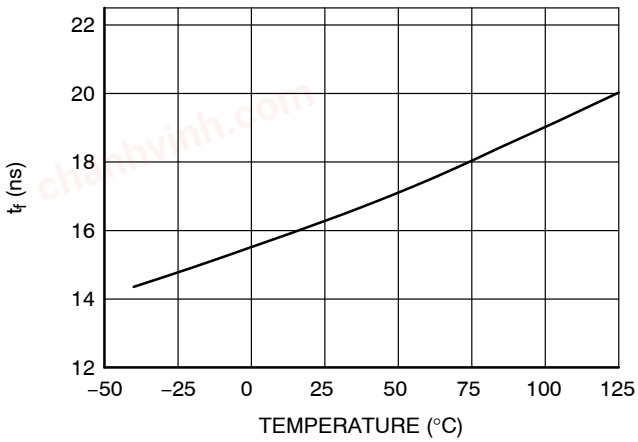


Figure 27. t_f vs. Temperature

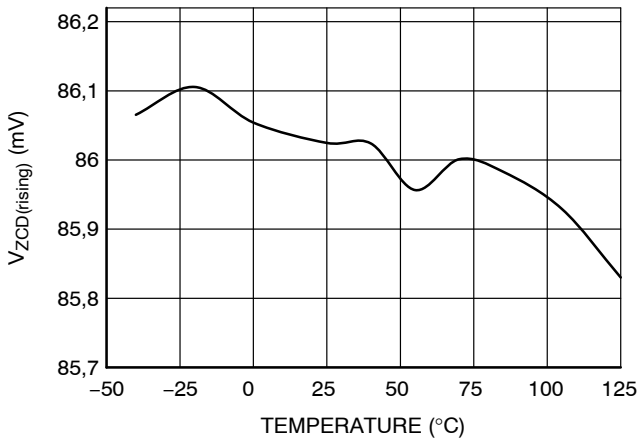


Figure 28. $V_{ZCD(rising)}$ vs. Temperature

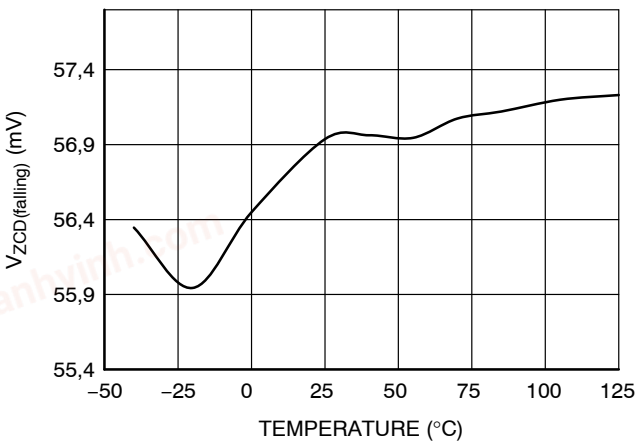


Figure 29. $V_{ZCD(falling)}$ vs. Temperature

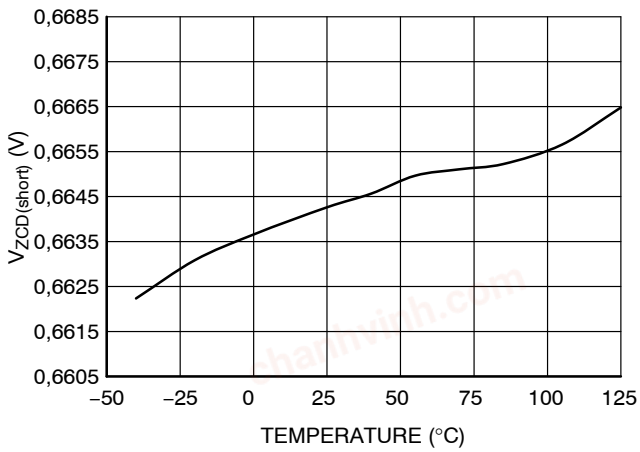


Figure 30. $V_{ZCD(short)}$ vs. Temperature

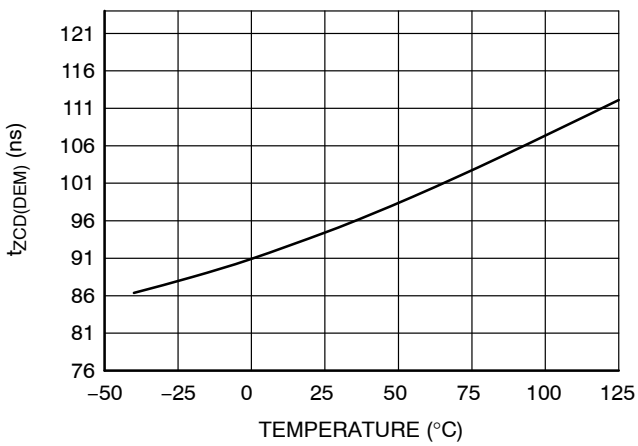


Figure 31. $t_{ZCD(DEM)}$ vs. Temperature

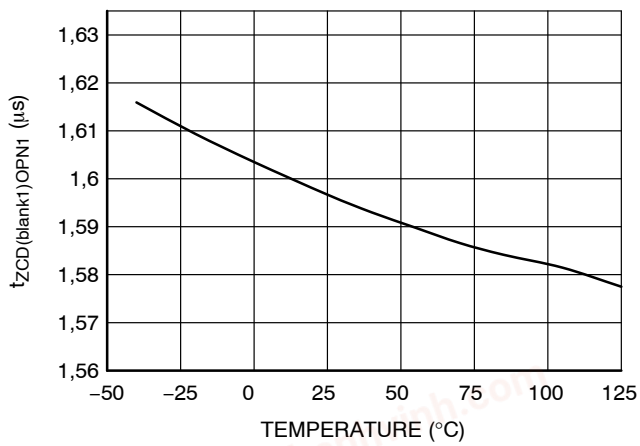


Figure 32. $t_{ZCD(blank1)OPN1}$ vs. Temperature

chanhvinh.com

TYPICAL CHARACTERISTICS (continued)

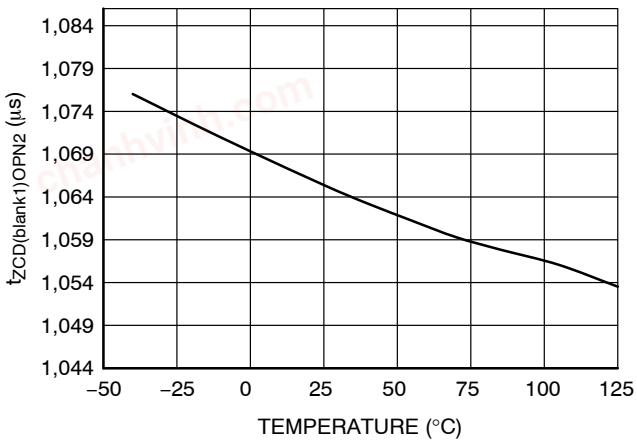


Figure 33. $t_{ZCD(blank1)OPN2}$ vs. Temperature

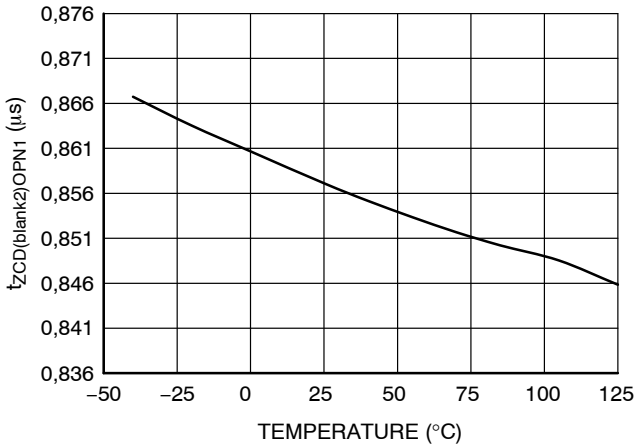


Figure 34. $t_{ZCD(blank1)OPN1}$ vs. Temperature

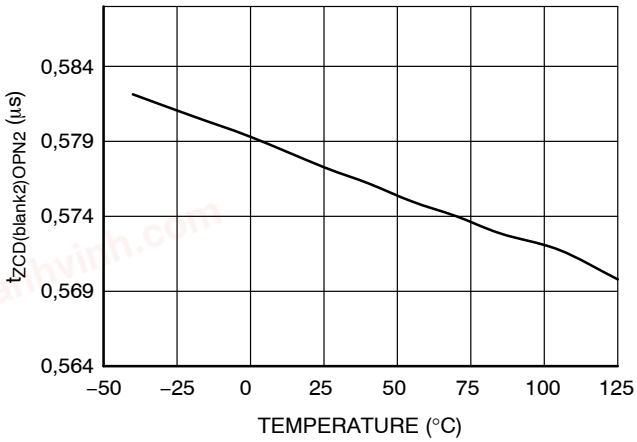


Figure 35. $t_{ZCD(blank2)OPN2}$ vs. Temperature

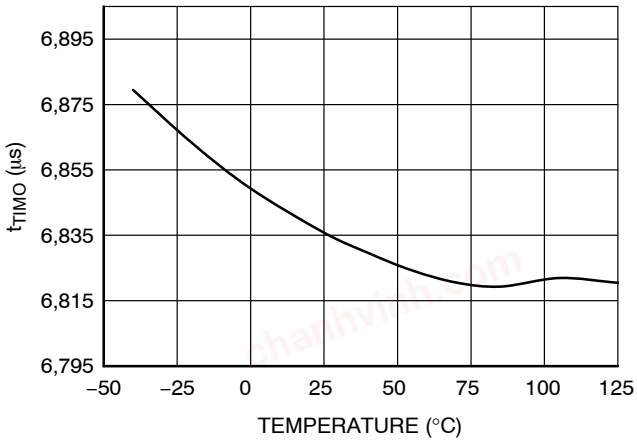


Figure 36. t_{TIMO} vs. Temperature

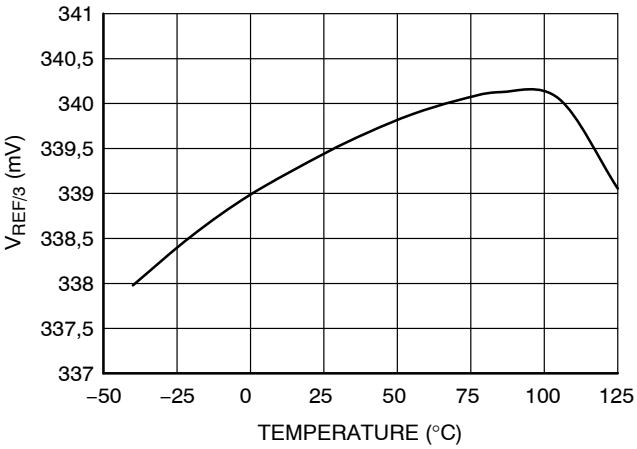


Figure 37. $V_{REF/3}$ vs. Temperature

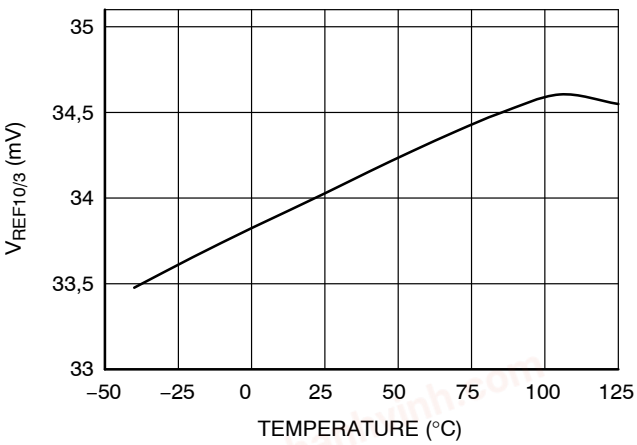


Figure 38. $V_{REF10/3}$ vs. Temperature

chanhvinh.com

TYPICAL CHARACTERISTICS (continued)

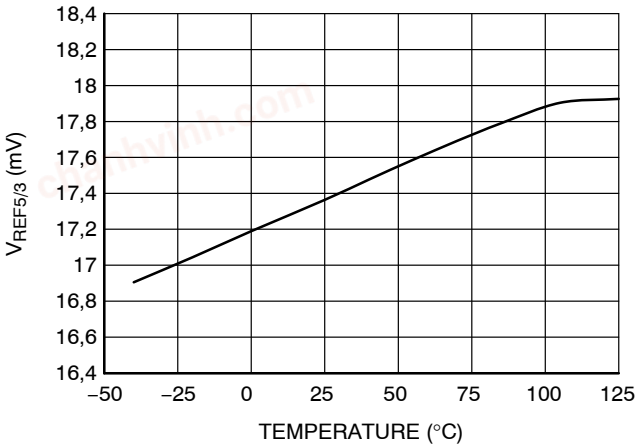


Figure 39. $V_{REF5/3}$ vs. Temperature

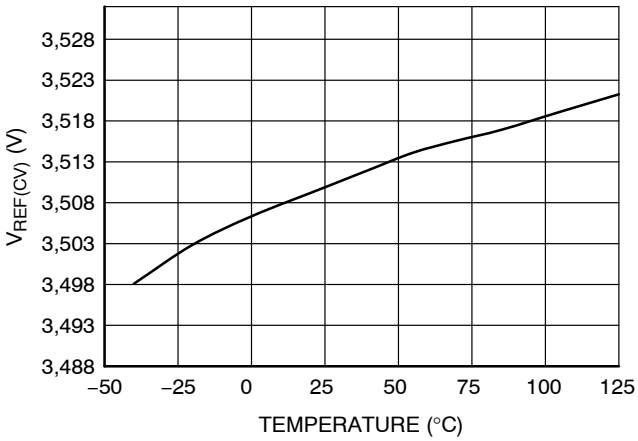


Figure 40. $V_{REF(CV)}$ vs. Temperature

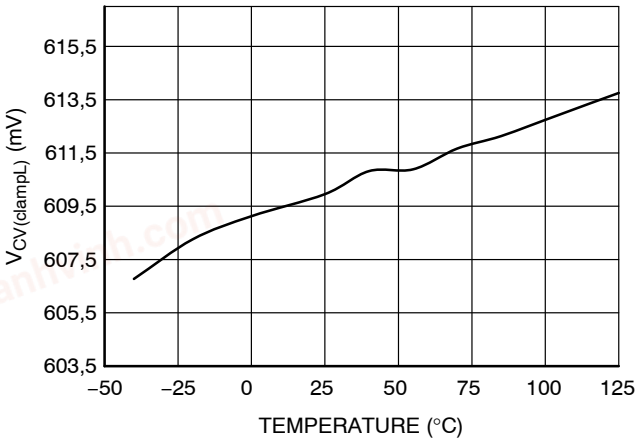


Figure 41. $V_{CV(clampL)}$ vs. Temperature

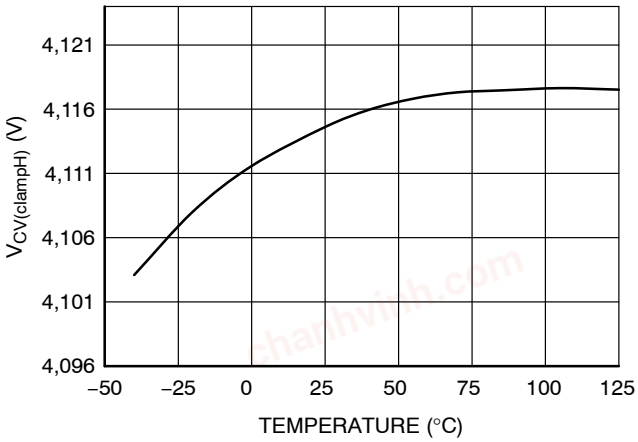


Figure 42. $V_{CV(clampH)}$ vs. Temperature

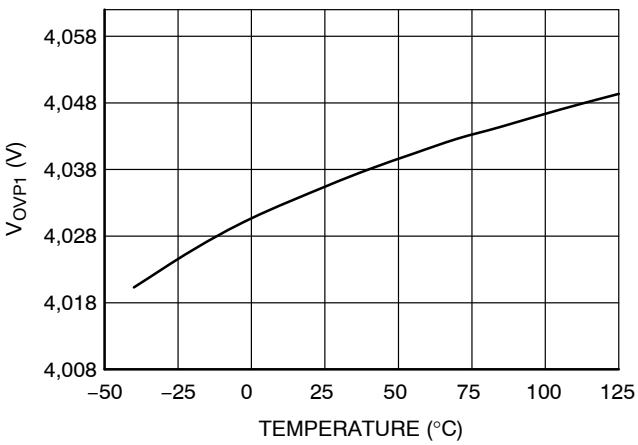


Figure 43. V_{OVP1} vs. Temperature

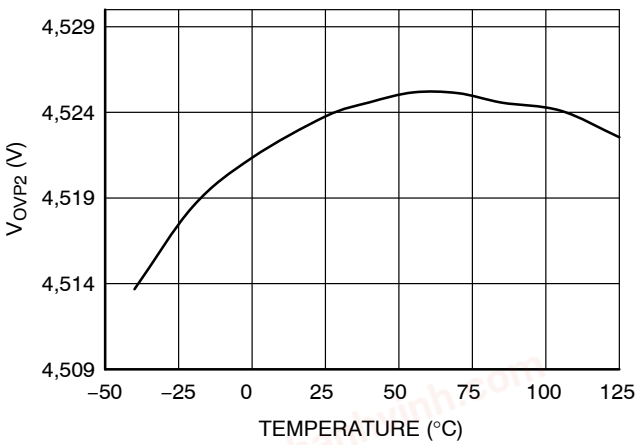


Figure 44. V_{OVP2} vs. Temperature

chanhvinh.com

TYPICAL CHARACTERISTICS (continued)

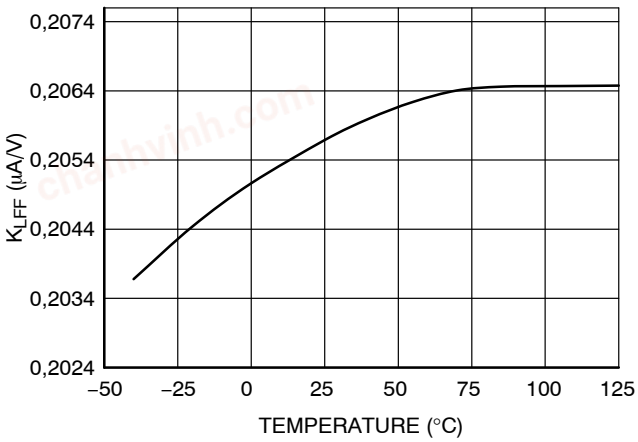


Figure 45. K_{LFF} vs. Temperature

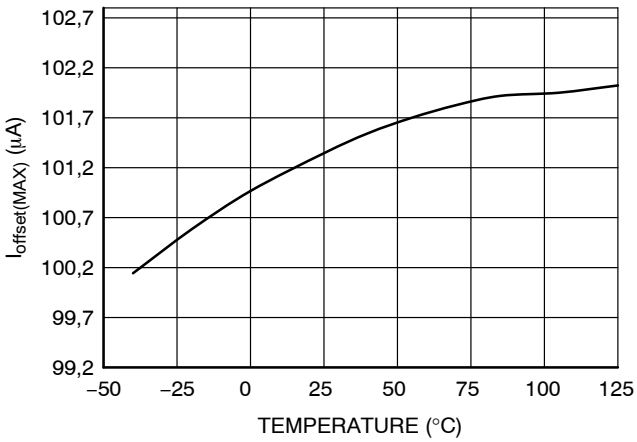


Figure 46. $I_{offset(MAX)}$ vs. Temperature

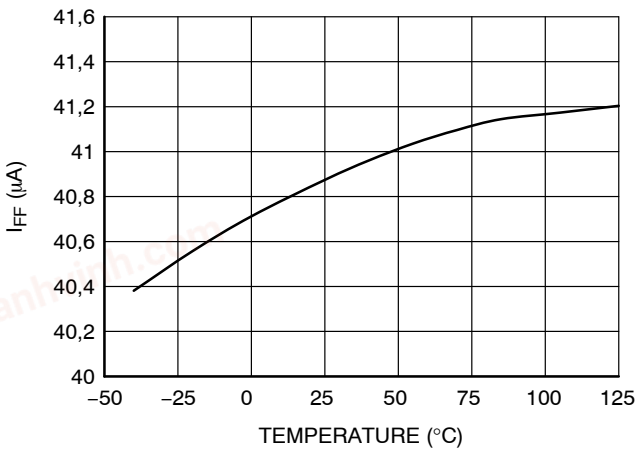


Figure 47. I_{FF} vs. Temperature

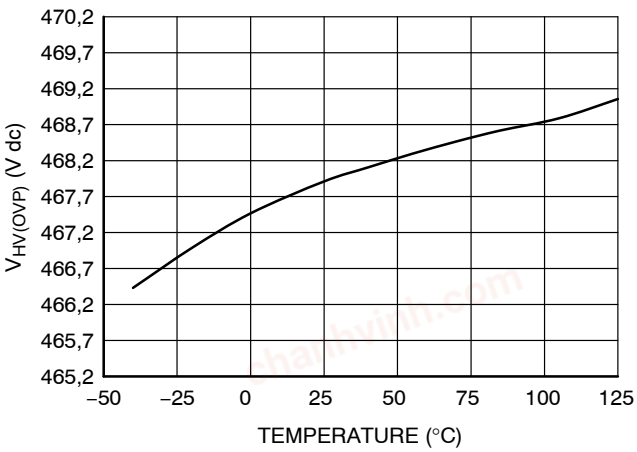


Figure 48. $V_{HV(OVP)}$ vs. Temperature

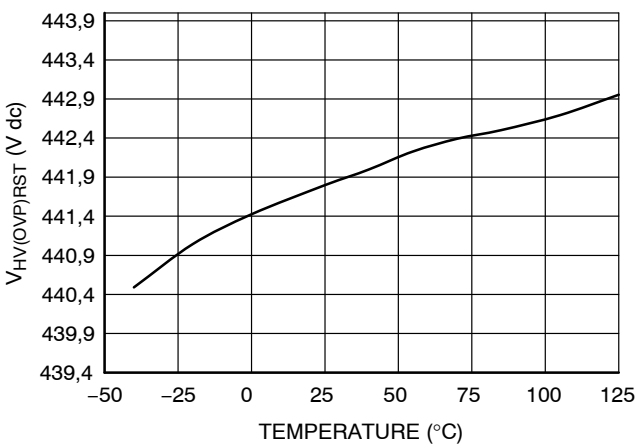


Figure 49. $V_{HV(OVP)RST}$ vs. Temperature

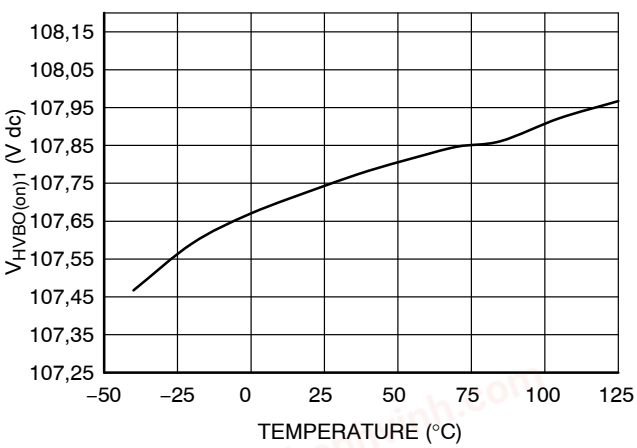


Figure 50. $V_{HVBO(on)1}$ vs. Temperature

chanhvinh.com

TYPICAL CHARACTERISTICS (continued)

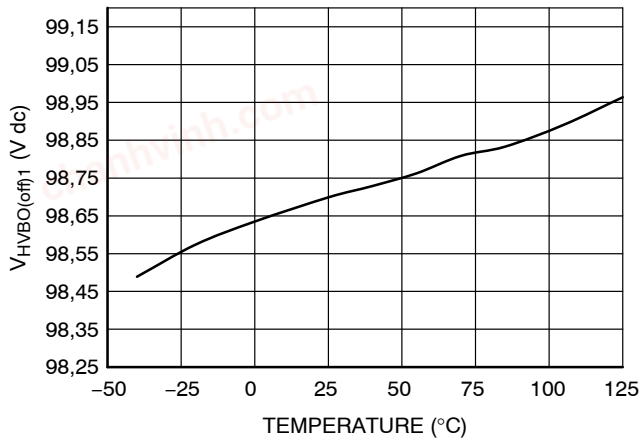


Figure 51. $V_{HVBO(off)1}$ vs. Temperature

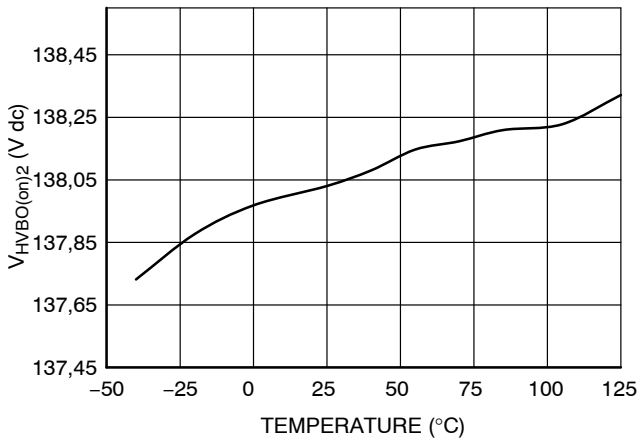


Figure 52. $V_{HVBO(on)2}$ vs. Temperature

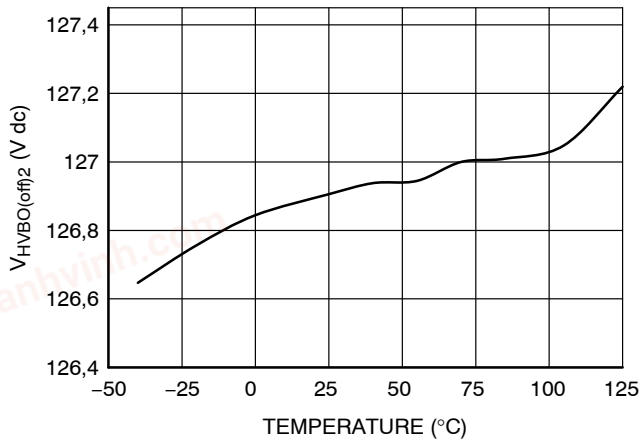


Figure 53. $V_{HVBO(off)2}$ vs. Temperature

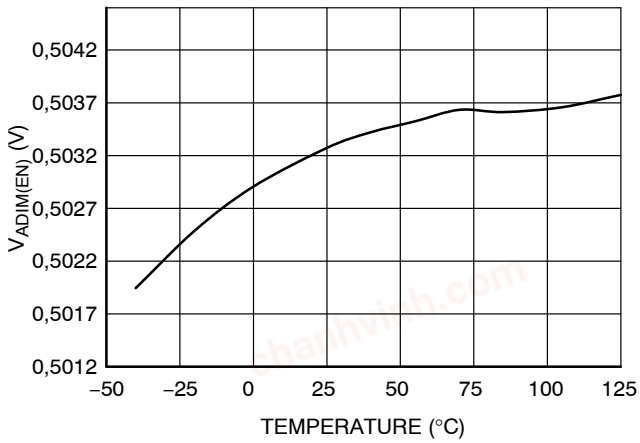


Figure 54. $V_{ADIM(EN)}$ vs. Temperature

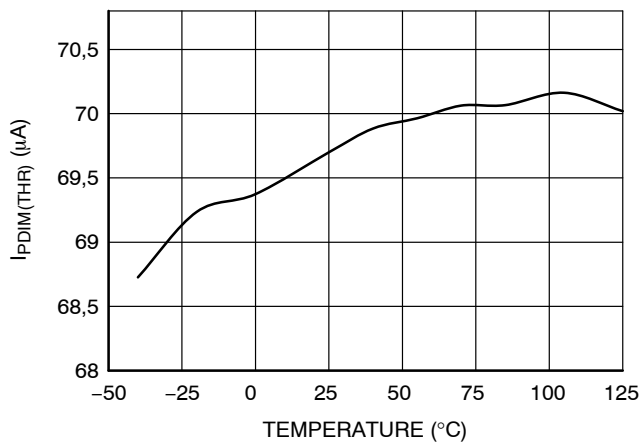


Figure 55. $I_{PDIM(THR)}$ vs. Temperature

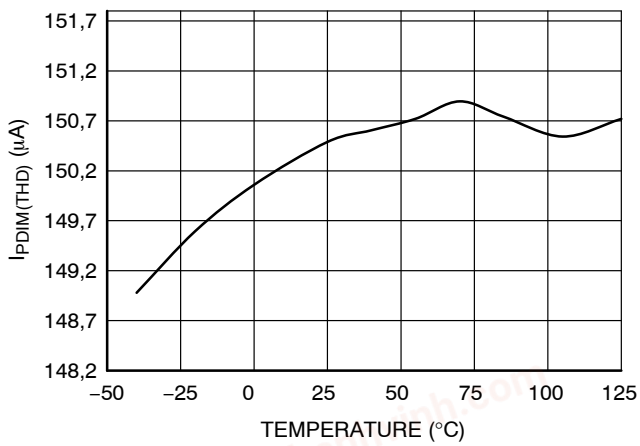


Figure 56. $I_{PDIM(THD)}$ vs. Temperature

chanhvinh.com

TYPICAL CHARACTERISTICS (continued)

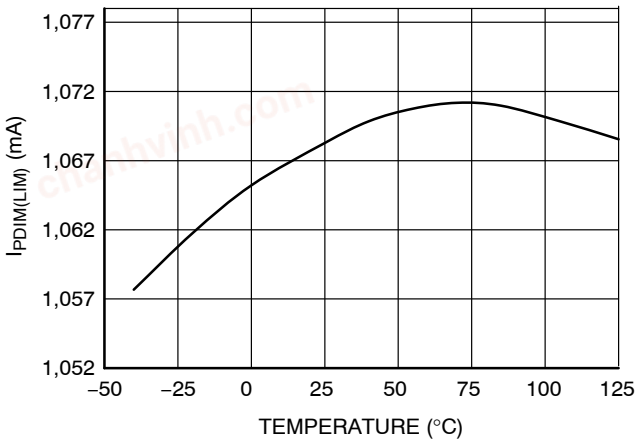


Figure 57. $I_{PDIM(LIM)}$ vs. Temperature

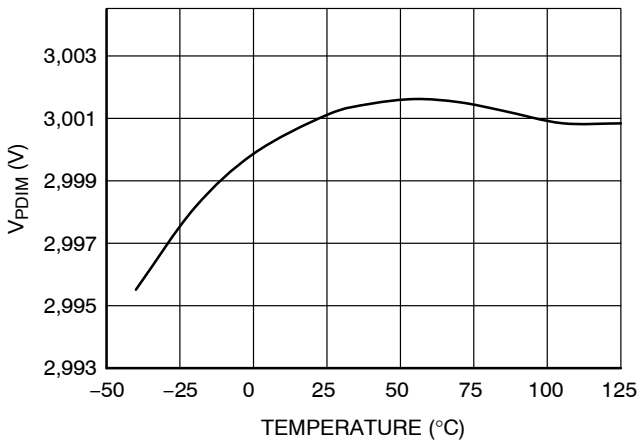


Figure 58. V_{PDIM} vs. Temperature

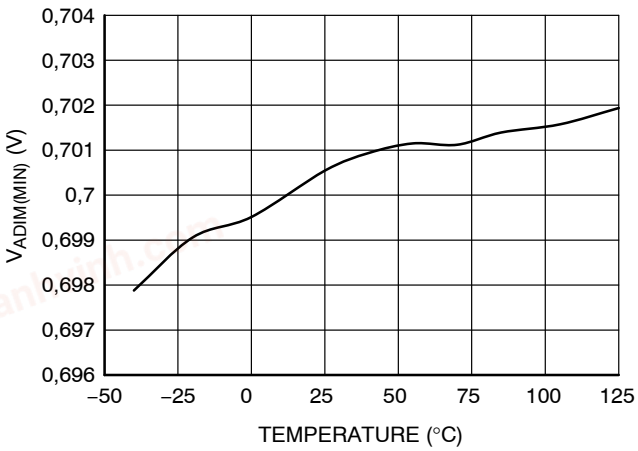


Figure 59. $V_{ADIM(MIN)}$ vs. Temperature

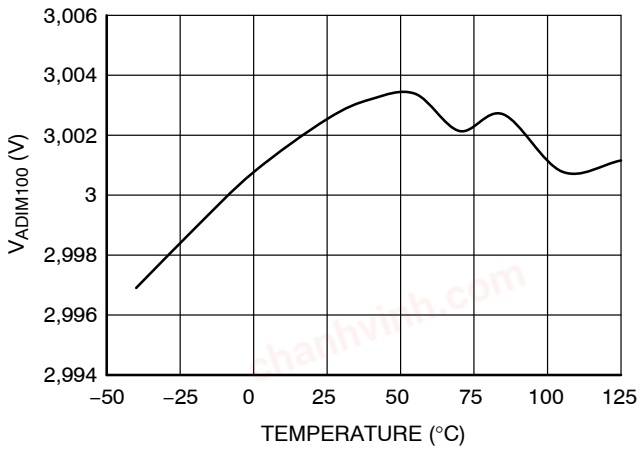


Figure 60. $V_{ADIM100}$ vs. Temperature

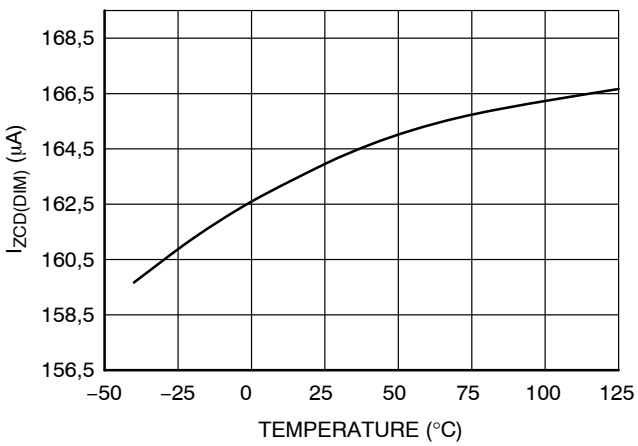


Figure 61. $I_{ZCD(DIM)}$ vs. Temperature

chanhvinh.com

Application Information

The NCL30486B implements a current−mode architecture operating in quasi−resonant mode. Thanks to proprietary circuitry, the controller is able to accurately regulate the secondary side current and voltage of the fly−back converter without using any opto−coupler or measuring directly the secondary side current or voltage. The controller provides near unity power factor correction

- *Quasi−Resonance Current−Mode Operation:* implementing quasi−resonance operation in peak current−mode control, the NCL30486B optimizes the efficiency by switching in the valley of the MOSFET drain−source voltage. Thanks to an internal algorithm control, the controller locks−out in a selected valley and remains locked until the input voltage or the output current set point significantly changes.
- *Primary Side Constant Current Control:* thanks to a proprietary circuit, the controller is able to take into account the effect of the leakage inductance of the transformer and allows an accurate control of the secondary side current regardless of the input voltage and output load variation.
- *Primary Side Constant Voltage Regulation:* By monitoring the auxiliary winding voltage, it is possible to regulate accurately the output voltage. The output voltage regulation is typically within ±2%.
- *Load Transient Compensation:* Since PFC has low loop bandwidth, abrupt changes in the load may cause excessive over or under−shoot. The slow Over Voltage Protection contains the output voltage when it tends to become excessive. In addition, the NCL30486B speeds up the constant voltage regulation loop when the output voltage goes below 80% or 85% of its regulation level.
- *Power Factor Correction:* A proprietary concept allows achieving high power factor correction and low THD while keeping accurate constant current and constant voltage control.
- *Line Feed−forward:* allows compensating the variation of the output current caused by the propagation delay.
- *V_{CC} Over Voltage Protection:* if the V_{CC} pin voltage exceeds an internal limit, the controller shuts down and waits 4 seconds before restarting pulsing.
- *Fast Over Voltage Protection:* If the voltage of ZCD pin exceeds 130% of its regulation level, the controller shuts down and waits 4 s before trying to restart.
- *Brown−Out:* the controller includes a brown−out circuit which safely stops the controller in case the input voltage is too low. The device will automatically restart if the line recovers.
- *Cycle−by−cycle Peak Current Limit:* when the current sense voltage exceeds the internal threshold V_{ILIM}, the MOSFET is turned off for the rest of the switching cycle.
- *Winding Short−Circuit Protection:* an additional comparator senses the CS signal and stops the controller if V_{CS} reaches 1.5 x V_{ILIM} (after a reduced LEB of t_{BCS}). This additional comparator is enabled only during the main LEB duration t_{LEB}, for noise immunity reason.
- *Output Under Voltage Protection:* If a too low voltage is applied on ZCD pin for 90 ms time interval, the controllers assume that the output or the ZCD pin is shorted to ground and shutdown. After waiting 4 seconds, the IC restarts switching.
- *Analog Dimming:* the ADIM pin is dedicated to analog dimming. There are several options for the minimum dimming level. Pulling the pin voltage lower than $V_{ADIM(EN)}$ disables the controller.
- *PWM Dimming:* the PDIM pin is dedicated to PWM dimming. The controller measures the duty ratio of a signal applied to the pin and reduces the output current accordingly. If this pin is left open, the controller delivers the maximum output current. If the pin is pulled down, the controller is disabled.
- *Thermal Shutdown:* an internal circuitry disables the gate drive when the junction temperature exceeds 150°C (typically). The circuit resumes operation once the temperature drops below approximately 100°C.
- *Standby Mode:* In order to decrease the power consumption of the SMPS if no load conditions, the controller features a standby mode, where its own consumption is decreased.
- *Dimming Standby Mode (dimCV Mode) Option:* by pulling ADIM or PDIM down, the controller goes in constant voltage mode with a reduced regulation setpoint.

POWER FACTOR AND CONSTANT CURRENT CONTROL

The NCL30486B embeds an analog/digital block to control the power factor and regulate the output current by monitoring the ZCD, CS and HV pin voltages (signals V_{ZCD}, V_{HV_DIV}, V_{CS}). This circuit generates the current setpoint signal and compares it to the current sense signal to turn the MOSFET off. The HV pin provides the sinusoidal reference necessary for shaping the input current. The obtained current reference is further modulated so that when averaged over a half line period, it is equal to the output current reference (V_{REFX}). The modulation and averaging process is made internally by a digital circuit. If the HV pin properly conveys the sinusoidal shape, power factor will be close to 1. Also, the Total Harmonic Distortion (THD) will be low especially if the output voltage ripple is small.

$$I_{OUT} = \frac{V_{REF}}{2N_{sp}R_{sense}} \quad \text{(eq. 1)}$$

Where:

- N_{sp} is the secondary to primary transformer turns ratio: $N_{sp} = N_S / N_P$
- R_{sense} is the current sense resistor
- V_{REFX} is the output current reference: $V_{REFX} = V_{REF}$ if no dimming

chanhvinh.com

The output current reference (V_{REFX}) is V_{REF} unless the constant voltage mode is activated or ADIM pin voltage is below $V_{ADIM(100)}$ or a PWM signal with a duty−cycle below 95% is applied on PDIM.

PRIMARY SIDE CONSTANT VOLTAGE CONTROL

The auxiliary winding voltage is sampled internally through the ZCD pin.

A precise internal voltage reference $V_{REF(CV)}$ sets the voltage target for the CV loop.

The sampled voltage is applied to the negative input of the constant voltage (CV) operational transconductance amplifier (OTA) and compared to V_{REFCV}.

A type 2 compensator is needed at the CV OTA output to stabilize the loop. The COMP pin voltage modify the the output current internal reference in order to regulate the output voltage.

When $V_{COMP} \geq 4$ V, $V_{REFX} = V_{REF}$.

When $V_{COMP} < 0.9$ V, $V_{REFX} = 0$ V.

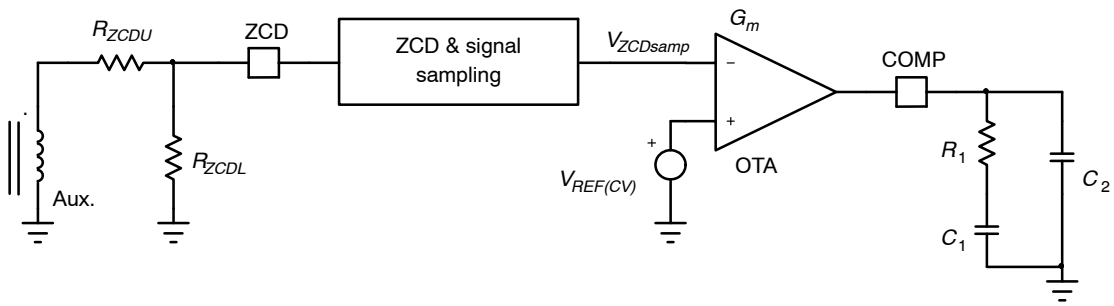


Figure 62. Constant Voltage Feedback Circuit

STARTUP PHASE (HV STARTUP)

It is generally requested that the LED driver starts to emit light in less than 1 s and possibly within 300 ms. It is challenging since the start−up consists of the time to charge the V_{CC} capacitor and that necessary to charge the output capacitor until sufficient current flows into the LED string. This second phase can be particularly long in dimming cases where the secondary current is a portion of the nominal one.

The NCL30486B features a high voltage startup circuit that allows charging VCC capacitor very fast.

When the power supply is first connected to the mains outlet, the internal current source is biased and charges up the V_{CC} capacitor. When the voltage on this V_{CC} capacitor reaches the $V_{CC(on)}$ level, the current source turns off. At this time, the controller is only supplied by the V_{CC} capacitor, and the auxiliary supply should take over before V_{CC} collapses below $V_{CC(off)}$.

The HV startup circuitry is made of two startup current levels, $I_{HV(start1)}$ and $I_{HV(start2)}$. This helps to protect the controller against short−circuit between V_{CC} and GND. At power−up, as long as V_{CC} is below $V_{CC(TH)}$, the source delivers $I_{HV(start1)}$ (around 300 μA typical). Then, when V_{CC} reaches $V_{CC(TH)}$, the source smoothly transitions to $I_{HV(start2)}$ and delivers its nominal value. As a result, in case of short−circuit between V_{CC} and GND occurring at high line (V_{in} = 305 V rms), the maximum power dissipation will be 431 x 300 μ = 130 mW instead of 1.5 W if there was only one startup current level.

To speed−up the output voltage rise, the following is implemented:

- The digital OTA output is increased until $V_{REF(PFC)}$ signal reaches V_{REFX}. Again, this is to speed−up the control signal rise to their steady state value.
- At the beginning of each operating phase of a V_{CC} cycle, the digital OTA output is set to 0. Actually, the digital OTA output is set to 0 in the case of a cold start−up or in the case of a start−up sequence following an operation interruption due to a fault. On the other hand, if the V_{CC} hiccups just because the system fails to start−up in one V_{CC} cycle, the digital OTA output is not reset to ease the second (or more) attempt. But, the digital OTA stops integrating if $V_{CC} < V_{CC(off)}$. The compensator output then restarts from its setpoint before the UVLO, thus avoiding any output current overshoot if a resistor is inserted in series with HV pin.
- If the load is shorted, the circuit will operate in hiccup mode with VCC oscillating between $V_{CC(off)}$ and $V_{CC(on)}$ until the output under voltage protection (UVP) trips. UVP is triggered if the ZCD pin voltage does not exceed $V_{ZCD(short)}$ within a 90 ms operation of time. This indicates that the ZCD pin is shorted to ground or that an excessive load prevents the output voltage from rising.

HV Startup Power Dissipation

At high line (305 V rms and above) the power dissipated by the HV startup in case of fault or when the controller is disabled with PDIM becomes high. Indeed, in case of fault, the NCL30486B is directly supplied by the HV rail. When the controller is disabled with PDIM, the optocoupler collector current is also supplied by the controller, since the NCL30486B allows directly connecting the optocoupler transistor to PDIM pin. Thus, the HV startup circuit also supplies the optocoupler transistor in case of faults. The current flowing through the HV startup will heat the controller. It is highly recommended adding enough copper around the controller to decrease the $R_{\theta JA}$ of the controller.

chanhvinh.com

Adding a minimum pad area of 215 mm^2 of 35 μm copper (1 oz) drops the $R_{\theta JA}$ to around 120°C/W (no air flow, $R_{\theta JA}$ measured at ADIM pin)

The PCB layout shown in Figure 63 is a layout example to achieve low $R_{\theta JA}$.

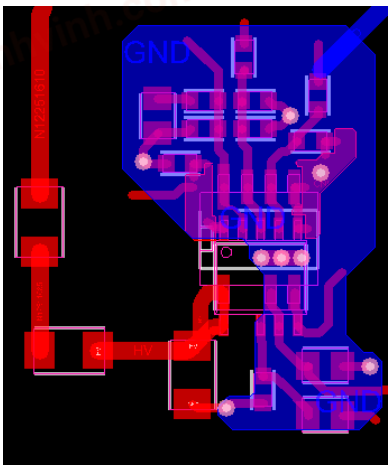


Figure 63. PCD Layout Example

The application note AND90120 gives more details about strategies to decrease the power dissipation of the HV startup circuit.

Cycle−by−Cycle Current Limit

When the current sense voltage exceeds the internal threshold V_{ILIM}, the MOSFET is turned off for the rest of the switching cycle.

Winding and Output Diode Short−Circuit Protection

In parallel to the cycle−by−cycle sensing of the CS pin, another comparator with a reduced LEB (t_{BCS}) and a threshold of ($V_{CS(stop)}$ = 140% x V_{ILIM}) monitors the CS pin to detect a winding or an output diode short circuit. The controller shuts down if it detects 4 consecutives pulses during which the CS pin voltage exceeds $V_{CS(stop)}$.

The controller goes into auto−recovery mode.

PWM Dimming

The NCL30486B has a dedicated pin for PWM dimming.

The controller directly measures the duty ratio of a PWM signal applied to PDIM.

Two counters with a high frequency clock are used for this purpose. A first counter measure the high state duration of the PWM signal (t_{on_PDIM}) and the second counter measures its period (T_{sw_PDIM}). A divider computes (t_{on_PDIM} / T_{sw_PDIM}) and the result is directly the output current setpoint (V_{REFX} set point). A filter is added after the digital divider to remove the ripple of the signal. A cascode configuration on PDIM pin allows decreasing the fall time of the signal.

Thanks to this circuit, the LED current is controlled in an analog way, even if a PWM signal is used for dimming. This allows having a good PF during dimming.

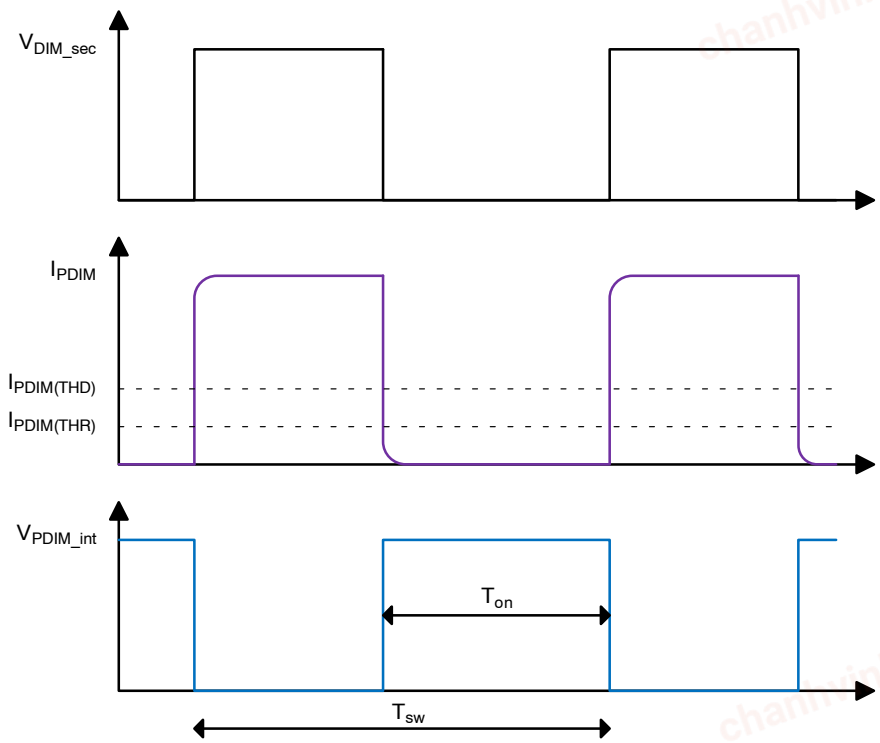


Figure 64. PDIM Internal Waveforms

chanhvinh.com

Practically, the controller extracts the duty−cycle by measuring the current inside PDIM pin which is directly the opto coupler collector current.

If PDIM pin is left open, the controller delivers 100% of I_{out}. If the pin is pulled down for longer than 25 ms, the controller is disabled.

If the PWM dimming signal is removed during dimming, the controller delivers 100% of I_{out}.

The NCL30486B set 100% of output current when the duty−cycle of the signal applied on PDIM is above 93%.

Analog Dimming

The pin ADIM pin allows implementing analog dimming of the LED light.

If the power supply designer applies an analog signal varying from $V_{DIM(EN)}$ to V_{DIM100} to the DIM pin, the output current will increase or decrease proportionally to the voltage applied. For V_{DIM} = V_{DIM100}, the power supply delivers the maximum output current (V_{REFX} = 1 V).

If a voltage lower than $V_{ADIM(MIN)}$ is applied to ADIM pin, the output current is clamped to the selected dimming clamp value (see Dimming clamp section below)

If a voltage lower than $V_{ADIM(EN)}$ is applied to the DIM pin, the DRV pulses are disabled for controllers without the dimming CV mode option.

The DIM pin is pulled up internally by a small current source or resistor. Thus, if the pin is left open, the controller is able to start.

NOTE:

- Interaction between ADIM and PDIM: if ADIM and PDIM are both used at the same time, the resulting dimming set point if a multiplication of V_{ADIM} and the duty−ratio of PDIM signal.
- During dimming, when the “Enable” signal is OK, the controller starts pulsing after first valley, even if a higher valley number is selected by V_{REFX}. This is to avoid too long startup time while dimming at low output current value. After ZCD voltage during DRV off time is higher than 0.65 V, the number of valley is selected by V_{REFX}.
- In order to minimize discrete output current variation caused by valley change in deep dimming, valley synchronization is removed when the dimming setpoint is below 15%.

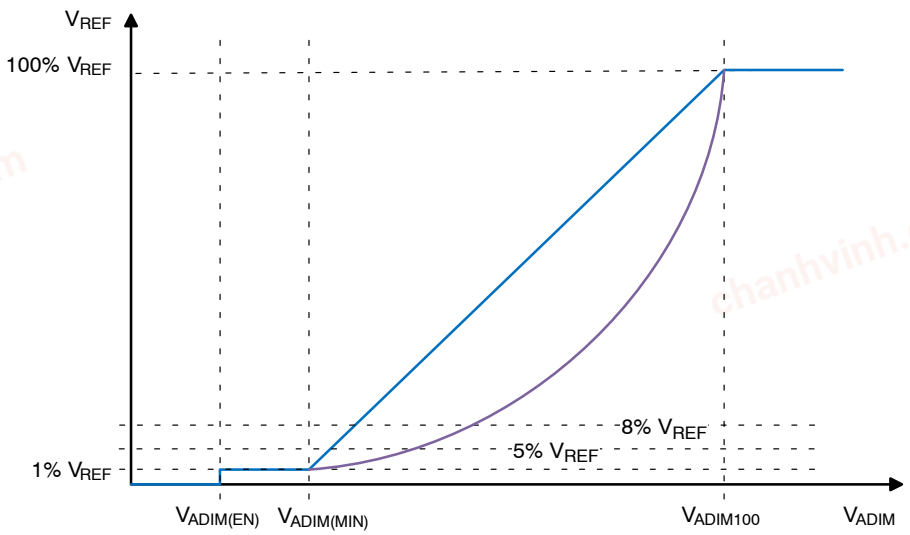


Figure 65. ADIM Pin Dimming Curves

chanhvinh.com

Dimming Clamp

For smart dimming applications, need to bias the secondary−side MCU. This can be achieved by clamping V_{REFX} when the dimming setpoint is small.

There are 4 options for the dimming clamp:

- No dimming clamp
- 1%
- 5%
- 8%

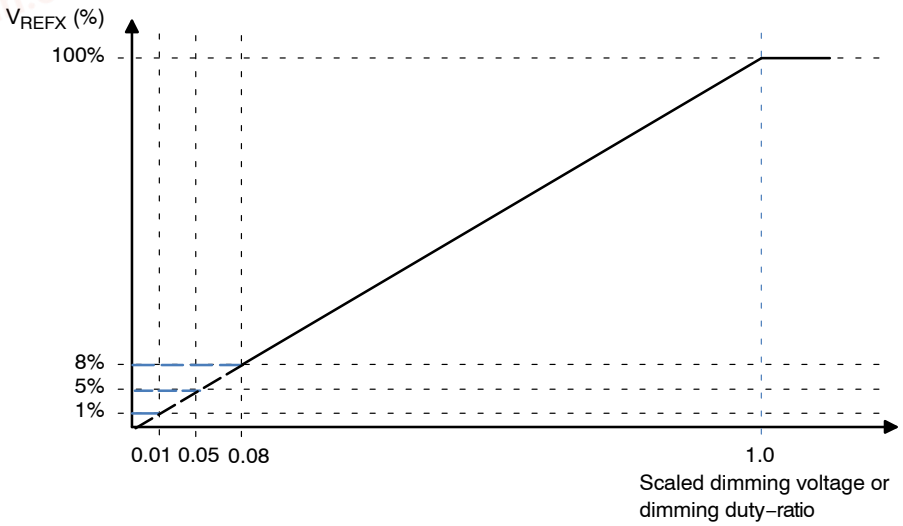


Figure 66. Dimming Clamp Options

Dimming Curves

By default, there is a linear relationship between the voltage applied on ADIM pin and V_{REFX} setpoint. In the same way, there is a linear relationship between the duty−ratio of the signal applied on PDIM and V_{REFX} setpoint.

An internal memory allows selecting a root square relationship between dimming and V_{REFX}.

The square like curve is based on CIE 1931 lightness formula.

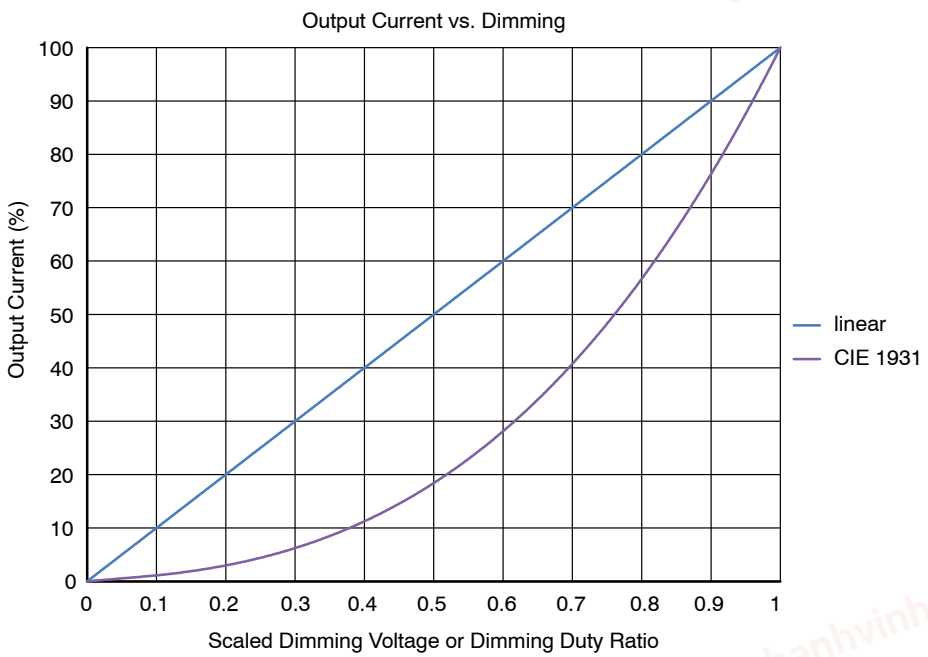


Figure 67. Dimming Curves

chanhvinh.com

Dimming Standby Mode (dimCV Mode)

The NCL30486B features an option to force constant voltage regulation by pulling ADIM or PDIM pin down. This can be useful to provide some energy to secondary side circuitry while the LED are turned off. In this mode, the regulation target is set lower than the regulation threshold is normal CV mode.

Concretely, when $V_{ADIM} < V_{ADIM(EN)}$ or when the internal PDIM signal on−time is below 10 μs during 20 ms, the "dimCVmode" signal becomes high and the $I_{ZCD(dim)}$ current source is applied to ZCD pin during the demagnetization time only (this is to allow correct valley detection). This current sources increases ZCD voltage and consequently a new regulation point is set for the CV loop.

The ZCD pin resistors set directly the regulation threshold in normal CV mode and in dimming CV mode.

$$R_{ZCDL} = \frac{V_{REF(CV)} (V_{auxCV1} - V_{auxCV2})}{I_{ZCD(dim)} (V_{auxCV1} - V_{REF(CV)})} \quad \text{(eq. 2)}$$

$$R_{ZCDU} = R_{ZCDL} \left(\frac{V_{auxCV1}}{V_{REF(CV)}} - 1 \right) \quad \text{(eq. 3)}$$

Where:

- R_{ZCDU} is the resistor from auxiliary winding to ZCD pin
- R_{ZCDL} is the resistor connected between ZCD and GND pins
- V_{auxCV1} is the auxiliary winding voltage corresponding to the nominal CV setpoint
- V_{auxCV2} is the auxiliary winding voltage corresponding to the CV setpoint in reduced CV mode: $V_{auxCV2} < V_{auxCV1}$

Valley Lockout

Quasi−Square wave resonant systems have a wide switching frequency excursion. The switching frequency increases when the output load decreases or when the input voltage increases. The switching frequency of such systems must be limited.

The NCL30486B changes valley as V_{REFX} decreases and as the input voltage increases and as the output current setpoint is varied during dimming. This limits the frequency excursion.

By default, when the output current is not dimmed, the controller operates in the first valley at low line and in the second valley at high line.

There is an option to have the valley thresholds incremented by 1 at high line for better I_{out} control at 305 V rms.

Table 1. VALLEY SELECTION

V_{REFX} Value at which the Controller Changes Valley (I_{out} Decreasing)	V_{HV_DIV} Voltage for Valley Change		V_{REFX} Value at which the Controller Changes Valley (I_{out} Increasing)
	0 −−LL−− 2.3 V	−−HL−− 5 V	
100%	1st	2nd (3rd)	100%
80%	2nd	3rd (4th)	90%
65%	3rd	4th (5th)	75%
50%	4th	5th (6th)	60%
35%	5th	6th (7th)	45%
25%	FF mode	FF mode	35%
0%			0%
I_{out} decreases	0 −−LL−− 2.3 V	−−HL−− 5 V	I_{out} increases
	Internal V_{HV_DIV} Voltage for Valley Change		

Zero Crossing Detection Block

The ZCD pin allows detecting when the drain−source voltage of the power MOSFET reaches a valley.

A valley is detected when the ZCD pin voltage crosses below the 55 mV internal threshold.

At startup or in case of extremely damped free oscillations, the ZCD comparator may not be able to detect the valleys. To avoid such a situation, NCL30486B features a Time−Out circuit that generates pulses if the voltage on ZCD pin stays below the 55 mV threshold for 6.5 μs.

The Time−out also acts as a substitute clock for the valley detection and simulates a missing valley in case of too damped free oscillations.

chanhvinh.com

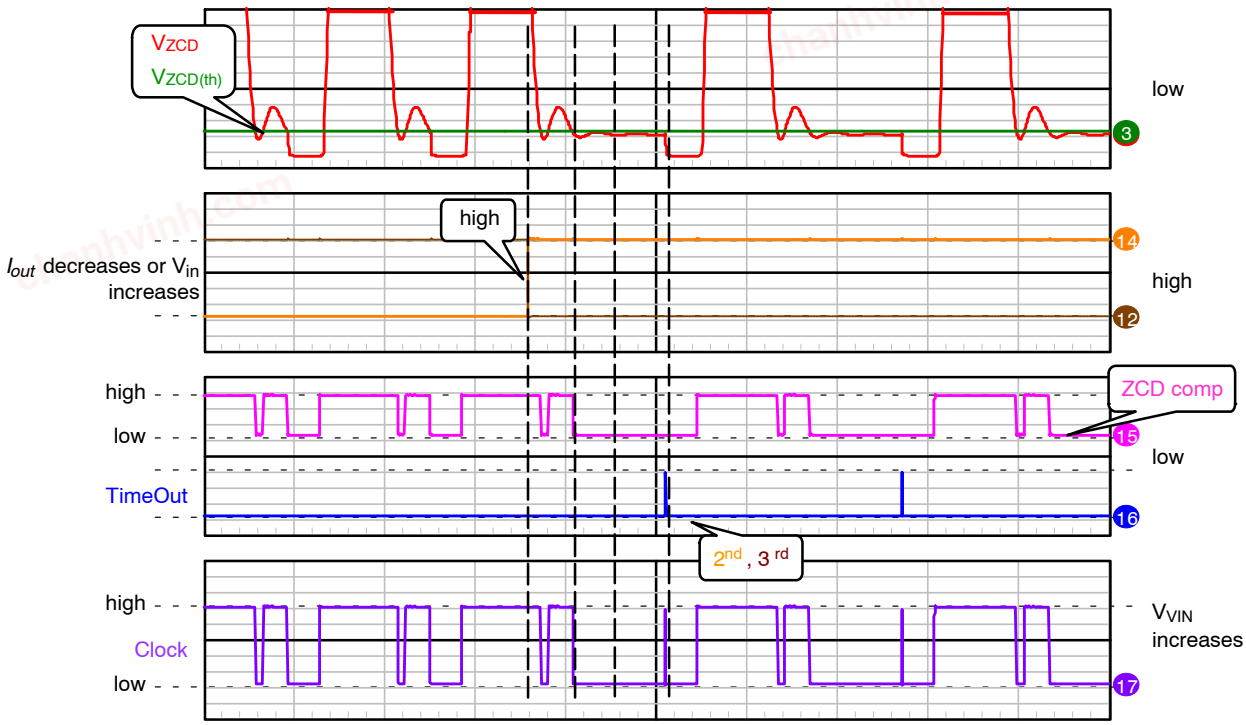


Figure 68. Valley Detection and Time−out Chronograms

If the ZCD pin or the auxiliary winding happen to be shorted the time−out function would normally make the controller keep switching and hence lead to improper regulation of the LED current.

The Under Voltage Protection (UVP) is implemented to avoid these scenarios: a secondary timer starts counting when the ZCD voltage is below the $V_{ZCD(short)}$ threshold. If this timer reaches 90 ms**,** the controller detects a fault and enters the auto−recovery fault mode.

Minimum Off−time at Startup

At startup, the output voltage reflected on the auxiliary winding is low. Thus, the voltage on the ZCD pin is very low and the ZCD comparator might be unable to detect the valleys. In this condition, setting the DRV latch with the 6.5−µs time−out leads to a continuous conduction mode operation (CCM).

To avoid CCM pulses during startup, a minimum off time (typ. 50 µs) is forced when $V_{ZCD} < V_{ZCD(short)}$ during 8 ms.

This minimum off time is also present when the controller restart after a fault, if $V_{ZCD} < V_{ZCD(short)}$.

ZCD Over Voltage Protection

Because of the power factor correction, it is necessary to set the crossover frequency of the CV loop very low (target 10 Hz, depending on power stage phase shift). Because the loop is slow, the output voltage can reach high value during startup or during an output load step. It is necessary to limit the output voltage excursion. For this, the NCL30486B features a slow OVP and a fast OVP on ZCD pin.

Slow OVP

If ZCD voltage exceeds V_{OVP1} for 4 consecutive switching cycles, the controller stops switching during 1.4 ms. The PFC loop is not reset. After 1.4 ms, the controller initiates a new DRV pulse to refresh ZCD sampling voltage. If V_{ZCD} is still too high ($V_{ZCD} > 115\%$ $V_{REF(CV)}$), the controller continues to switch with a 1.4 ms period. The controller resumes its normal operation when $V_{ZCD} < 105\%$ $V_{REF(CV)}$.

During slow OVP, the peak current setpoint is COMP pin voltage scaled down by a fixed ratio.

Fast OVP

If ZCD voltage exceeds $V_{ZCD(OVP2)}$ (130% of $V_{REF(CV)}$) for 4 consecutive switching cycles (slow OVP not triggered) or for 2 switching cycles if the slow OVP has already been triggered, the controller detects a fault and starts the auto−recovery fault mode (cf: Fault Management Section)

chanhvinh.com

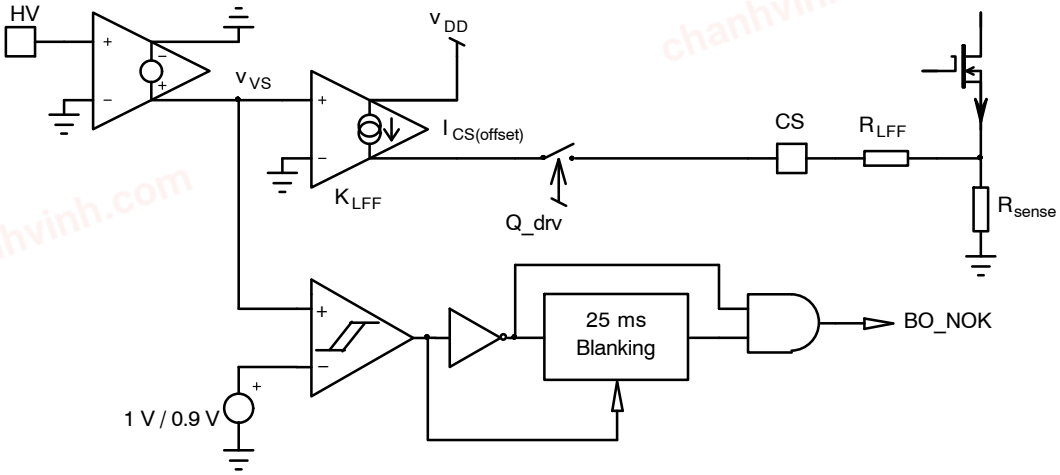


Figure 69. Line Feed−Forward and Brown−out Schematic

Line Feedforward

The line voltage is sensed by the HV pin and converted into a current. By adding an external resistor in series between the sense resistor and the CS pin, a voltage offset proportional to the line voltage is added to the CS signal. The offset is applied only during the MOSFET on−time in order to not influence the detection of the leakage inductance reset.

The offset is always applied even at light load in order to improve the current regulation at low output load.

Brown−out

In order to protect the supply against a very low input voltage, the controller features a brown−out circuit with a fixed ON/OFF threshold. The controller is allowed to start if a voltage higher than $V_{HVBO(on)}$ is applied to the HV pin and shuts−down if the HV pin voltage decreases and stays below $V_{HVBO(off)}$ for 25 ms typical.

An option with higher brown−out levels is also available (see ordering table and electricals parameters)

Line OVP

In order to protect the power supply in case of too high input voltage, the NCL30486B features a line over voltage protection. When the voltage on HV pin exceeds $V_{HV(OVP)}$ the controller stops switching; V_{CC} hiccups.

When V_{HV} becomes lower than $V_{HV(OVP)RST}$ for more than 340 ms, the controller initiates a clean startup sequence and re−starts switching.

chanhvinh.com

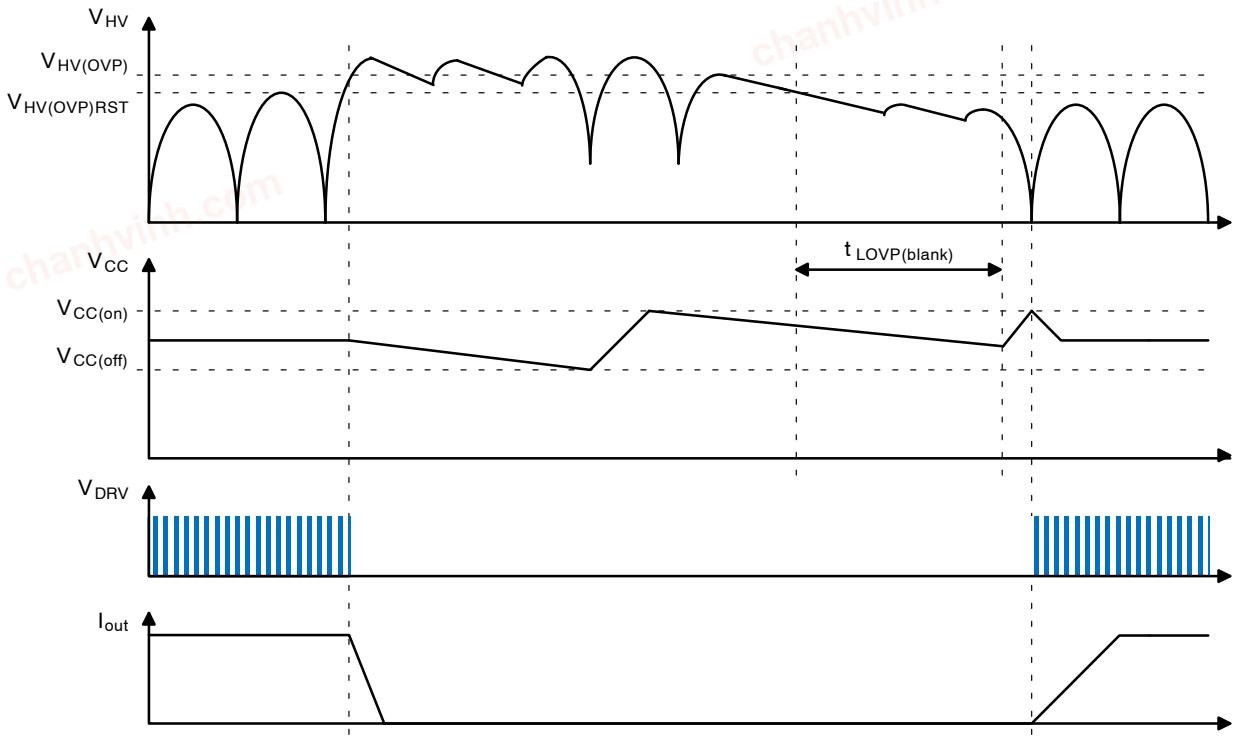


Figure 70. Line OVP Chronograms

Standby Mode

In order to decrease the power consumption of the converter when no output load is connected to its output, the NCL30486B versions features a standby mode.

In standby mode, the current consumption of the controller is reduced to I_{CC4} (1.7 mA typ.)

The peak current is frozen to a fixed value $V_{CS(STBY)}$ (27% or below of V_{ILIMIT}) and the controller adjust the switching frequency, more specifically the dead−time (DT) to keep the output voltage regulated (pink curve in Figure 71).

The regulation of V_{out} is based on COMP pin voltage varying between 700 mV to 913 mV.

Standby mode is entered if V_{COMP} < 895 mV, V_{COMP} decreasing and exit if V_{COMP} > 913 mV, V_{COMP} increasing. (See AND90120 for more details concerning the standby mode)

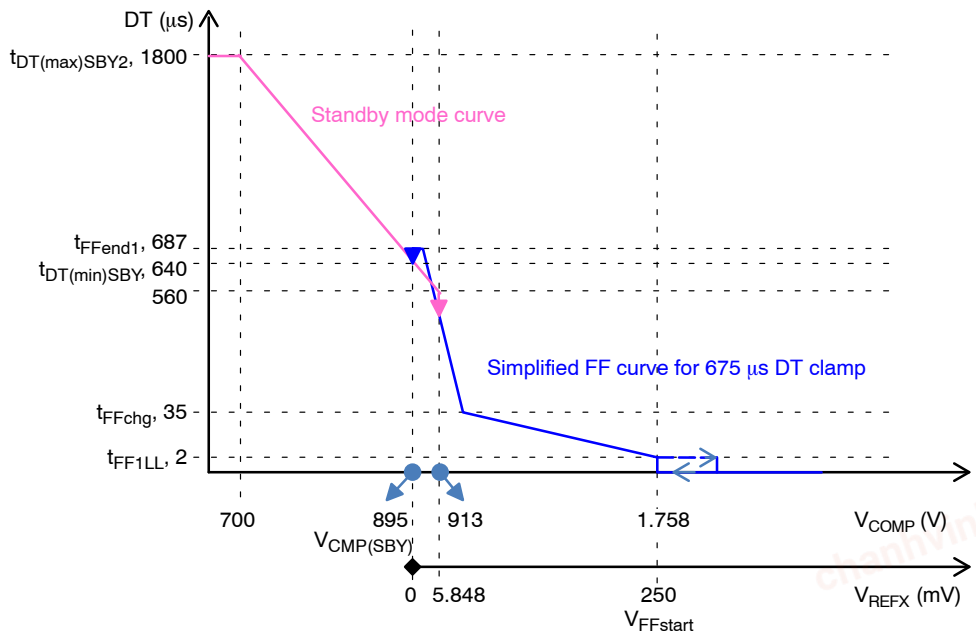


Figure 71. Dead−time Setpoint as a Function of V_{COMP}

chanhvinh.com

Variable Maximum On−time

Around line zero−crossing, the primary inductor slope is too low to reach the peak current setpoint imposed by the CC control. The DRV pulse is terminated by the max. on−time.

This creates sudden variation of the on−time and creates an input current spike (EMI filter inductance responds to rate of change of current).

Varying the maximum on−time with V_{REFX} helps decreasing this spike over the output load range. Figure 72 and Figure 73 shows the maximum on−time curve as a function of V_{REFX}.

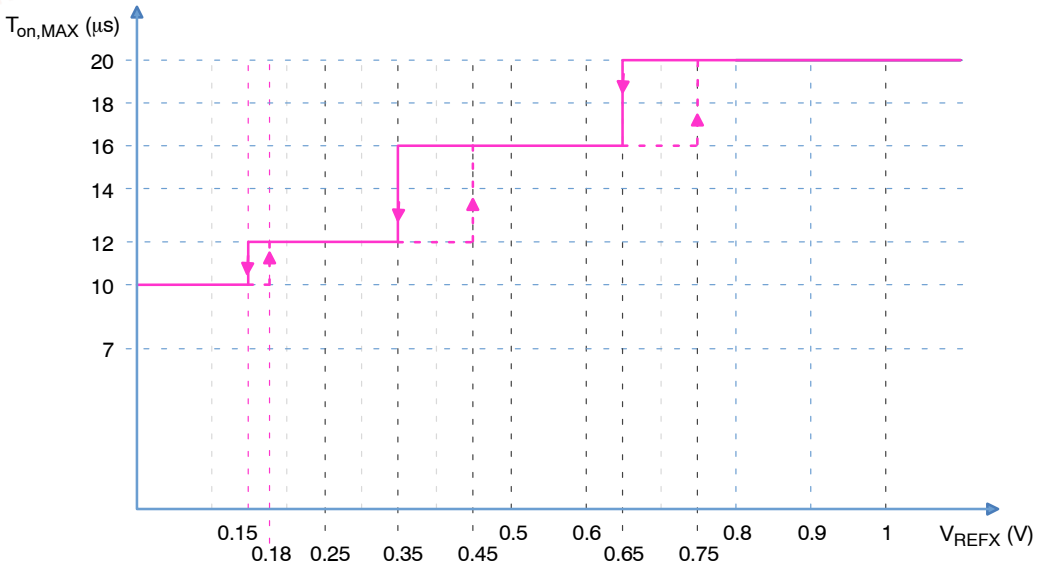


Figure 72. Variable Maximum On−time, 20−μs Option

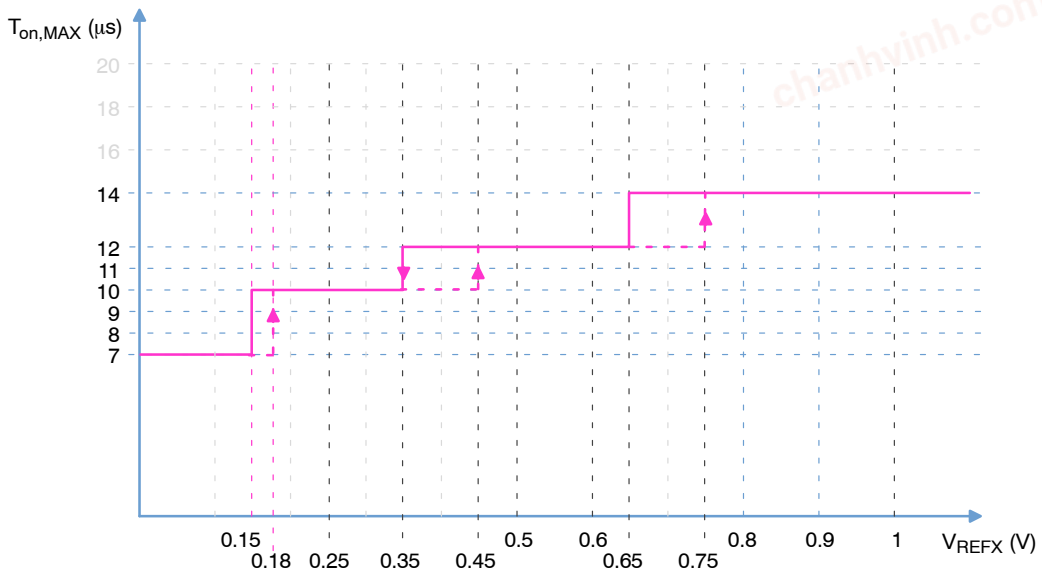


Figure 73. Variable Maximum On−time, 14−μs Option

chanhvinh.com

Protections

The circuit incorporates a large variety of protections to make the LED driver very rugged.

Among them, we can list:

- Fault of the GND connection
  If the GND pin is properly connected, the supply current drawn from the positive terminal of the V_{CC} capacitor, flows out of the GND pin to return to the negative terminal of the V_{CC} capacitor. If the GND pin is not connected, the circuit ESD diodes offer another return path. The accidental non connection of the GND pin can hence be detected by detecting that one of this ESD diode is conducting. Practically, the ESD diode of CS pin is monitored. If such a fault is detected for 200 μs, the circuit stops generating DRV pin.
- Output short circuit situation (Output Under Voltage Protection)
  Overload is detected by monitoring the ZCD pin voltage: if it remains below $V_{ZCD(short)}$ for 90 ms, an output short circuit is detected and the circuit stops generating pulses for 4 s. When this 4 s delay has elapsed, the circuit attempts to restart.
- ZCD pin incorrect connection:
  - If the ZCD pin grounded, the circuit will detect an output short circuit situation when 90 ms delay has elapsed.
  - A 200 kΩ resistor pulls down the ZCD pin so that the output short circuit detection trips if the ZCD pin is not connected (floating).
- Winding or Output Diode Short Circuit protection
  The circuit detects this failure when 4 consecutive DRV pulses occur within which the CS pin voltage exceeds ($V_{CS(stop)}$ = 140% x V_{ILIM}). In this case, the controller enters auto−recovery mode (4−s operation interruption between active bursts).
- V_{CC} Over Voltage Protection
  The circuit stops generating pulses if the V_{CC} exceeds $V_{CC(OVP)}$ and enters auto−recovery mode. This feature protects the circuit if output LEDs happen to be disconnected.
- ZCD fast OVP
  If ZCD voltage exceeds $V_{ZCD(OVP2)}$ for 4 consecutive switching cycles (slow OVP not triggered) or for 2 switching cycles if the slow OVP has already been triggered, the controller detects a fault and enters auto−recovery mode (4 s operation interruption between active bursts).
- Die Over Temperature (TSD)
  The circuit stops operating if the junction temperature (T_J) exceeds 150°C typically. The controller remains off until T_J goes below nearly 130°C.
- Brown−Out Protection (BO)
  The circuit prevents operation when the line voltage is too low to avoid an excessive stress of the LED driver. Operation resumes as soon as the line voltage is high enough and V_{CC} is higher than $V_{CC(on)}$.
- CS pin short to ground
  The CS pin is checked at start−up (cold start−up or after a brown−out event). A current source ($I_{cs(short)}$) is applied to the pin and no DRV pulse is generated until the CS pin exceeds $V_{cs(low)}$. $I_{cs(short)}$ and $V_{cs(low)}$ are 500 μA and 60 mV typically (V_{CS} rising). The typical minimum impedance to be placed on the CS pin for operation is then 120 Ω. In practice, it is recommended to place more than 250 Ω to take into account possible parametric deviations. Also, along the circuit operation, the CS pin could happen to be grounded. If it is grounded, the MOSFET conduction time is limited by the 20 μs maximum on−time. If such an event occurs, a new pin impedance test is made.
- Line overvoltage protection
  (see Line OVP section)

chanhvinh.com

ORDERING TABLE OPTION

OPN # NCL30486_ _	Dead−time Clamp			V_{REF}		Max. On−time		ZCD Blanking		Valley Transition from LL to HL		Standby Mode		Line Range Detector	
	250 μs	687 μs	1.4 ms	200 mV	333 mV	20 μs	14 μs	1 μs	1.5 μs	1st to 2nd	1st to 3rd	On	Off	On	Off
NCL30486B1	x				x		x	x		x		x		x	
NCL30486B2	x				x		x	x		x		x		x	

OPN # NCL30486_ _	Line OVP		Frozen Peak Current During Standby Mode $V_{CS(SBY)}$			Brown−out Levels		Dimming Clamp				Dimming Curve		dimCV Mode	
	On	Off	380 mV	330 mV	280 mV	On: 108 V Off: 98 V	On: 138 V Off: 129 V	0%	1%	5%	8%	Linear	Square	On	Off
NCL30486B1	x		x				x		x			x			x
NCL30486B2	x		x			x			x			x		x	

ORDERING INFORMATION

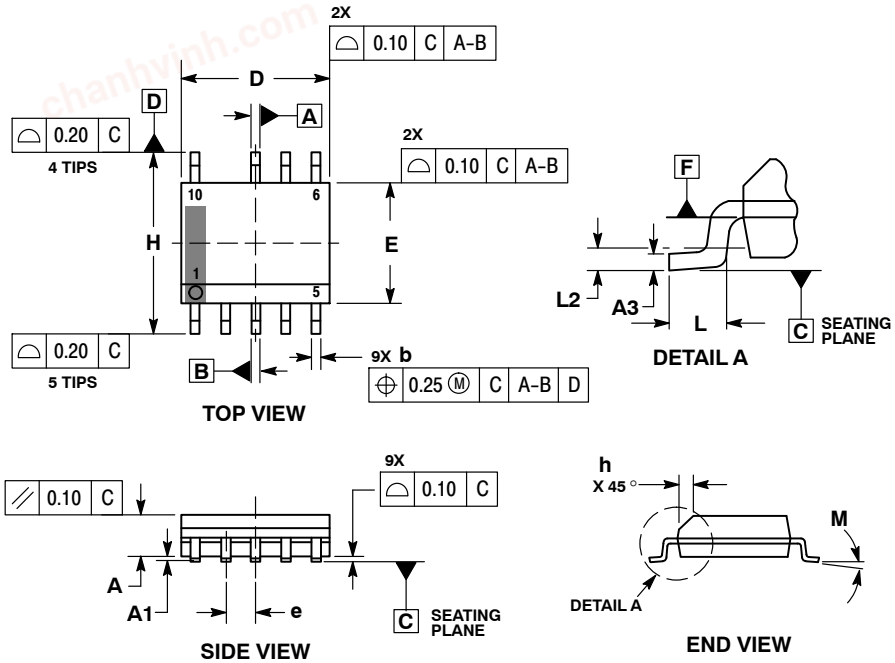
Device	Marking	Package Type	Shipping†
NCL30486B1	L30486B1	SOIC9 − P7 COMP VHV PBFH (Pb−Free)	2500 / Tape & Reel
NCL30486B2	L30486B2		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

chanhvinh.com

PACKAGE DIMENSIONS

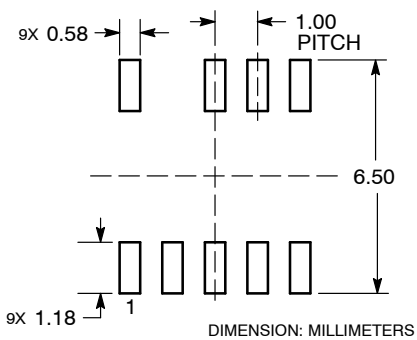
SOIC−9 NB
CASE 751BP
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF 'b' AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	1.25	1.75
A1	0.10	0.25
A3	0.17	0.25
b	0.31	0.51
D	4.80	5.00
E	3.80	4.00
e	1.00 BSC	
H	5.80	6.20
h	0.37 REF	
L	0.40	1.27
L2	0.25 BSC	
M	0°	8°

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

chanhvinh.com

NCL30486B

onsemi, ONSEMI., and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊