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DATA SHEET
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# High Speed Dual-Channel, Ceramic Digital Isolator

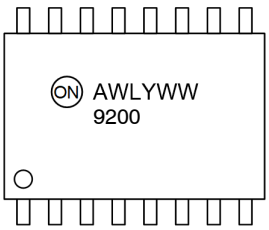
*Product Preview*

## NCID9200



SOIC16 W
CASE 751EN

### MARKING DIAGRAM




| | |
|---|---|
| A | = Assembly Location |
| WL | = Wafer Lot / Assembly Lot |
| Y | = Year |
| WW | = Work Week |
| 9200 | = Specific Device Code |

### ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

### Description

The NCID9200 is a galvanically isolated high−speed dual−channel digital isolator. This device supports isolated communications thereby allowing digital signals to communicate between systems without conducting ground loops or hazardous voltages.

It utilizes **onsemi**'s patented galvanic off−chip capacitor isolation technology and optimized IC design to achieve high insulation and high noise immunity, characterized by high common mode rejection and power supply rejection specifications. The thick ceramic substrate yields capacitors with ~25 times the thickness of thin film on−chip capacitors and coreless transformers. The result is a combination of the electrical performance benefits that digital isolators offer with the safety reliability of a >0.5 mm insulator barrier similar to what has historically been offered by optocouplers.

The device is housed in a 16−pin wide body small outline package.

### Features

- Off−Chip Capacitive Isolation to Achieve Reliable High Voltage Insulation
  - DTI (Distance Through Insulation): ≥ 0.5 mm
  - Maximum Working Insulation Voltage: 2000 $V_{peak}$
- 100 kV/μs Minimum Common Mode Rejection
- 8 mm Creepage and Clearance Distance to Achieve Reliable High Voltage Insulation
- Specifications Guaranteed Over 2.5 V to 5.5 V Supply Voltage and −40°C to 125°C Extended Temperature Range
- Over Temperature Detection
- NCIV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable (Pending)
- Safety and Regulatory Approvals
  - UL1577, 5000 VRMS for 1 Minute
  - DIN EN/IEC 60747−17 (Pending)

### Typical Applications

- Isolated PWM Control
- Industrial Fieldbus Communications
- Microprocessor System Interface (SPI, $I^2C$, etc.)
- Programmable Logic Control
- Isolated Data Acquisition System
- Voltage Level Translator

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## PIN CONFIGURATION

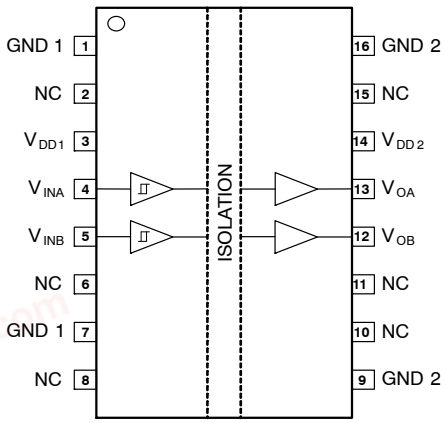



**Figure 1. Pin and Channel Configuration**

## BLOCK DIAGRAM

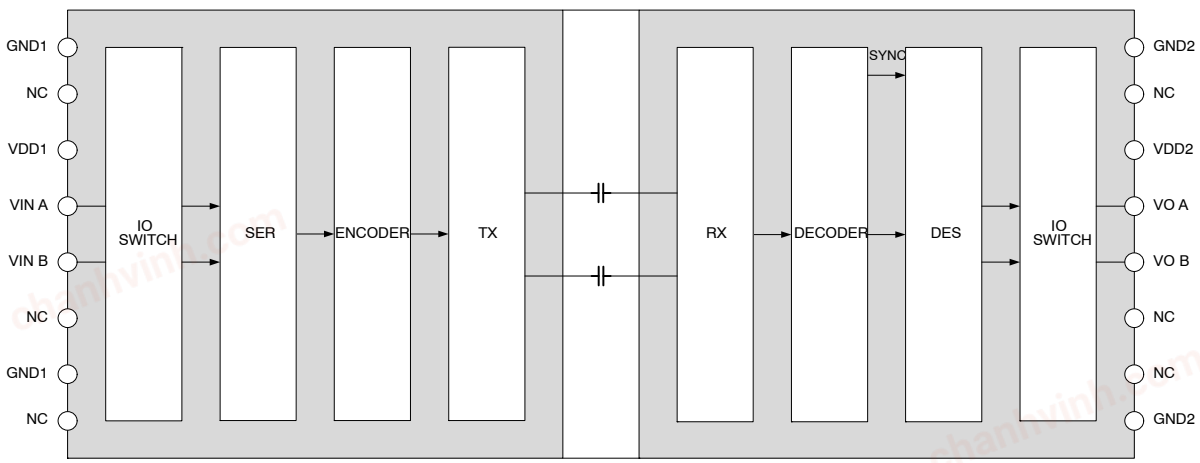



**Figure 2. Functional Block Diagram**

### PIN DEFINITIONS

| Pin No. | Name | Description |
|---|---|---|
| 1 | GND1 | Ground, Primary Side |
| 2 | NC | No Connect |
| 3 | $V_{DD1}$ | Power Supply, Primary Side |
| 4 | $V_{INA}$ | Input, Channel A |
| 5 | $V_{INB}$ | Input, Channel B |
| 6 | NC | No Connect |
| 7 | GND1 | Ground, Primary Side |
| 8 | NC | No Connect |
| 9 | GND2 | Ground, Secondary Side |
| 10 | NC | No Connect |
| 11 | NC | No Connect |
| 12 | $V_{OB}$ | Output, Channel B |
| 13 | $V_{OA}$ | Output, Channel A |
| 14 | $V_{DD2}$ | Power Supply, Secondary Side |
| 15 | NC | No Connect |
| 16 | GND2 | Ground, Secondary Side |

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## SPECIFICATIONS

**TRUTH TABLE** (Note 1)

| $V_{INX}$ | $V_{DDI}$ | $V_{DDO}$ | $V_{OX}$ | Comment |
|---|---|---|---|---|
| H | Power Up | Power Up | H | Normal Operation |
| L | Power Up | Power Up | L | Normal Operation |
| NC | Power Up | Power Up | L | Default Low |
| X | Power Down | Power Up | L | Default low; $V_{OX}$ return to normal operation when $V_{DDI}$ change to Power Up |
| X | Power Up | Power Down | Undetermined (Note 2) | $V_{OX}$ return to normal operation when $V_{DDO}$ change to Power Up |

1. $V_{INX}$ = Input signal of a given channel (A or B). $V_{OX}$ = Output signal of a given channel (A or B). $V_{DDI}$ = Input−side $V_{DD}$. $V_{DDO}$ = Output−side $V_{DD}$. X = Irrelevant. H = High level. L = Low level. NC = No Connection.
2. The outputs are in undetermined state when $V_{DDO} < V_{UVLO}$.

### SAFETY AND INSULATION RATINGS

As per DIN EN/IEC 60747−17 (pending), this digital isolator is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings must be ensured by means of protective circuits.

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | Installation Classifications per DIN VDE 0110/1.89 Table 1 Rated Mains Voltage | < 150 $V_{RMS}$ | – | I–IV | – | |
| | | < 300 $V_{RMS}$ | – | I–IV | – | |
| | | < 450 $V_{RMS}$ | – | I–IV | – | |
| | | < 600 $V_{RMS}$ | – | I–IV | – | |
| | | < 1000 $V_{RMS}$ | – | I–III | – | |
| | Climatic Classification | | – | 40/125/21 | – | |
| | Pollution Degree (DIN VDE 0110/1.89) | | – | 2 | – | |
| CTI | Comparative Tracking Index (DIN IEC 112/VDE 0303 Part 1) | | 600 | – | – | |
| $V_{PR}$ | Input−to−Output Test Voltage, Method b, $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with $t_m$ = 1 s, Partial Discharge < 5 pC | | 3750 | – | – | $V_{peak}$ |
| | Input−to−Output Test Voltage, Method a, $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test with $t_m$ = 10 s, Partial Discharge < 5 pC | | 3200 | – | – | $V_{peak}$ |
| $V_{IORM}$ | Maximum Working Insulation Voltage | | 2000 | – | – | $V_{peak}$ |
| $V_{IOTM}$ | Highest Allowable Over Voltage | | 8000 | – | – | $V_{peak}$ |
| $E_{CR}$ | External Creepage | | 8.0 | – | – | mm |
| $E_{CL}$ | External Clearance | | 8.0 | – | – | mm |
| DTI | Insulation Thickness | | 0.50 | – | – | mm |
| $T_{Case}$ | Safety Limit Values – Maximum Values in Failure; Case Temperature | | 150 | – | – | °C |
| $P_{S,INPUT}$ | Safety Limit Values – Maximum Values in Failure; Input Power | | 350 | – | – | mW |
| $P_{S,OUTPUT}$ | Safety Limit Values – Maximum Values in Failure; Output Power | | 350 | – | – | mW |
| $R_{IO}$ | Insulation Resistance at TS, $V_{IO}$ = 500 V | | $10^9$ | – | – | Ω |

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## ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise specified)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage Temperature | −55 to +150 | °C |
| $T_{OPR}$ | Operating Temperature | −40 to +125 | °C |
| $T_J$ | Junction Temperature | −40 to +150 | °C |
| $T_{SOL}$ | Lead Solder Temperature (Refer to Reflow Temperature Profile) | 260 for 10 s | °C |
| $V_{DD}$ | Supply Voltage ($V_{DDx}$) | −0.5 to 6 | V |
| V | Voltage ($V_{INx}$, $V_{Ox}$) | −0.5 to 6 | V |
| $I_O$ | Average Output Current | 10 | mA |
| PD | Power Dissipation | 210 | mW |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING RANGES

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_A$ | Ambient Operating Temperature | −40 | +125 | °C |
| $V_{DD1}$ $V_{DD2}$ | Supply Voltage (Notes 3, 4) | 2.5 | 5.5 | V |
| $V_{INH}$ | High Level Input Voltage | 0.7 × $V_{DDI}$ | $V_{DDI}$ | V |
| $V_{INL}$ | Low Level Input Voltage | 0 | 0.1 × $V_{DDI}$ | V |
| $V_{UVLO+}$ | Supply Voltage UVLO Rising Threshold | 2.2 | – | V |
| $V_{UVLO-}$ | Supply Voltage UVLO Falling Threshold | 2.0 | – | V |
| $UVLO_{HYS}$ | Supply Voltage UVLO Hysteresis | 0.1 | – | V |
| $I_{OH}$ | High Level Output Current | −2 | – | mA |
| $I_{OL}$ | Low Level Output Current | – | 2 | mA |
| DR | Signaling Rate | 0 | 20 | Mbps |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. During power up or down, ensure that both the input and output supply voltages reach the proper recommended operating voltages to avoid any momentary instability at the output state.
4. For reliable operation at recommended operating conditions, $V_{DD}$ supply pins require at least a pair of external bypass capacitors, placed within 2 mm from $V_{DD}$ pins 3 and 14 and GND pins 1 and 16. Recommended values are 0.1 μF and 1 μF.

## ISOLATION CHARACTERISTICS

Apply over all recommended conditions. All typical values are measured at $T_A$ = 25°C.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ISO}$ | Input−Output Isolation Voltage | $T_A$ = 25°C, Relative Humidity < 50%, t = 1.0 minute, $I_{I-O}$ ≤ 10 μA, 50 Hz (Notes 5, 6, 7) | 5000 | – | – | $V_{RMS}$ |
| $R_{ISO}$ | Isolation Resistance | $V_{I-O}$ = 500 V (Note 5) | – | $10^{11}$ | – | |
| $C_{ISO}$ | Isolation Capacitance | $V_{I-O}$ = 0 V, Frequency = 1.0 MHz (Note 5) | – | 1 | – | pF |

5. Device is considered a two−terminal device: pins 1 to 8 are shorted together and pins 9 to 16 are shorted together.
6. 5,000 $V_{RMS}$ for 1−minute duration is equivalent to 6,000 $V_{RMS}$ for 1−second duration.
7. The input−output isolation voltage is a dielectric voltage rating per UL1577. It should not be regarded as an input−output continuous voltage rating. For the continuous working voltage rating, refer to equipment−level safety specification or DIN EN/IEC 60747−17 Safety and Insulation Ratings Table on page 3.

## ELECTROSTATIC DISCHARGE RATINGS

| Symbol | Parameter | Conditions | Rating | Unit |
|---|---|---|---|---|
| HBM | Human Body Model | JS−001−2017; AEC−Q100−002−Rev E (Note 9) | ±3000 | V |
| CDM | Charged Device Model | JS−002−2018; AEC−Q100−011−Rev D (Note 10) | ±1250 | |
| ESDI | Contact Discharge | IEC 61000−4−2 Insulation Barrier Withstand Test (Note 8) | ±8000 | |
| | Air Discharge | | ±15000 | |

8. Device is considered a two−terminal device: pins 1 to 8 are shorted together and pins 9 to 16 are shorted together.
9. ESD Human Body Model for NCID9200 tested per JEDEC JS−001−2017 standard; NCIV9200 tested per AEC−Q100−002−Rev E standard.
10. ESD Charged Device Model for NCID9200 tested per JEDEC JS−002−2018 standard; NCIV9200 tested per AEC−Q100−011−Rev D standard.

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## ELECTRICAL CHARACTERISTICS

Apply over all recommended conditions, $T_A$ = −40°C to +125°C, $V_{DD1}$ = $V_{DD2}$ = 2.5 V to 5.5 V, unless otherwise specified. All typical values are measured at $T_A$ = 25°C.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | Figure |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High Level Output Voltage | $V_{DD}$ = 5 V, $I_{OH}$ = −4 mA | $V_{DDO}$ − 0.4 | $V_{DDO}$ − 0.1 | – | V | 7 |
| | | $V_{DD}$ = 3.3 V, $I_{OH}$ = −2 mA | | | | | |
| | | $V_{DD}$ = 2.5 V, $I_{OH}$ = −1 mA | | | | | |
| $V_{OL}$ | Low Level Output Voltage | $V_{DD}$ = 5 V, $I_{OL}$ = 4 mA | – | 0.1 | 0.4 | V | 8 |
| | | $V_{DD}$ = 3.3 V, $I_{OL}$ = 2 mA | | | | | |
| | | $V_{DD}$ = 2.5 V, $I_{OL}$ = 1 mA | | | | | |
| $V_{INT+}$ | Rising Input Voltage Threshold | | – | – | 0.7 × $V_{DDI}$ | V | |
| $V_{INT-}$ | Falling Input Voltage Threshold | | 0.1 × $V_{DDI}$ | – | – | V | |
| $V_{INT(HYS)}$ | Input Threshold Voltage Hysteresis | | 0.1 × $V_{DDI}$ | 0.2 × $V_{DDI}$ | – | V | |
| $I_{INH}$ | High Level Input Current | $V_{IH}$ = $V_{DDI}$ | – | – | 1 | μA | |
| $I_{INL}$ | Low Level Input Current | $V_{IL}$ = 0 V | −1 | – | – | μA | |
| CMTI | Common Mode Transient Immunity | $V_I$ = $V_{DDI}$ or 0 V, $V_{CM}$ = 1500 V | 100 | 150 | – | kV/μs | 10 |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = $V_{DDI}$/2 + 0.4 × sin (2πft), f = 1 MHz, $V_{DD}$ = 5 V | – | 2 | – | pF | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## SUPPLY CURRENT CHARACTERISTICS

Apply over all recommended conditions, $T_A$ = −40°C to +125°C unless otherwise specified. All typical values are measured at $T_A$ = 25°C.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | Figure |
|---|---|---|---|---|---|---|---|
| $I_{DD1}$ | DC Supply Current | $V_{DD}$ = 5 V, EN = 0/5 V, $V_{IN}$ = 0/5 V | – | 8.3 | 11.1 | mA | |
| $I_{DD2}$ | | | | 9.2 | 12.1 | | |
| $I_{DD1}$ | | $V_{DD}$ = 3.3 V, EN = 0/3.3 V, $V_{IN}$ = 0/3.3 V | | 8.2 | 10.8 | | |
| $I_{DD2}$ | | | | 9.1 | 11.8 | | |
| $I_{DD1}$ | | $V_{DD}$ = 2.5 V, EN = 0/2.5 V, $V_{IN}$ = 0/2.5 V | | 8.1 | 10.6 | | |
| $I_{DD2}$ | | | | 9.0 | 11.6 | | |
| $I_{DD1}$ | AC Supply Current 1 Mbps | $V_{DD}$ = 5 V, EN = 5 V, $C_L$ = 15 pF, $V_{IN}$ = 5 V Square Wave | – | 8.3 | 11.1 | mA | 3, 4 |
| $I_{DD2}$ | | | | 9.5 | 12.1 | | |
| $I_{DD1}$ | | $V_{DD}$ = 3.3 V, EN = 3.3 V, $C_L$ = 15 pF, $V_{IN}$ = 3.3 V Square Wave | | 8.2 | 10.8 | | |
| $I_{DD2}$ | | | | 9.2 | 11.8 | | |
| $I_{DD1}$ | | $V_{DD}$ = 2.5 V, EN = 2.5 V, $C_L$ = 15 pF, $V_{IN}$ = 2.5 V Square Wave | | 8.1 | 10.6 | | |
| $I_{DD2}$ | | | | 9.1 | 11.6 | | |
| $I_{DD1}$ | AC Supply Current 10 Mbps | $V_{DD}$ = 5 V, EN = 5 V, $C_L$ = 15 pF, $V_{IN}$ = 5 V Square Wave | – | 8.3 | 12.4 | mA | |
| $I_{DD2}$ | | | | 11.9 | 13.3 | | |
| $I_{DD1}$ | | $V_{DD}$ = 3.3 V, EN = 3.3 V, $C_L$ = 15 pF, $V_{IN}$ = 3.3 V Square Wave | | 8.2 | 11.4 | | |
| $I_{DD2}$ | | | | 10.5 | 12.5 | | |
| $I_{DD1}$ | | $V_{DD}$ = 2.5 V, EN = 2.5 V, $C_L$ = 15 pF, $V_{IN}$ = 2.5 V Square Wave | | 8.1 | 11.1 | | |
| $I_{DD2}$ | | | | 10.1 | 12.1 | | |

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**SUPPLY CURRENT CHARACTERISTICS** (continued)
Apply over all recommended conditions, $T_A$ = −40°C to +125°C unless otherwise specified. All typical values are measured at $T_A$ = 25°C.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | Figure |
|---|---|---|---|---|---|---|---|
| $I_{DD1}$ | AC Supply Current 20 Mbps | $V_{DD}$ = 5 V, EN = 5 V, $C_L$ = 15 pF, $V_{IN}$ = 5 V Square Wave | – | 8.3 | 13.6 | mA | 3, 4 |
| $I_{DD2}$ | | | | 14.2 | 15.2 | | |
| $I_{DD1}$ | | $V_{DD}$ = 3.3 V, EN = 3.3 V, $C_L$ = 15 pF, $V_{IN}$ = 3.3 V Square Wave | | 8.2 | 12.2 | | |
| $I_{DD2}$ | | | | 11.9 | 13.2 | | |
| $I_{DD1}$ | | $V_{DD}$ = 2.5 V, EN = 2.5 V, $C_L$ = 15 pF, $V_{IN}$ = 2.5 V Square Wave | | 8.1 | 11.6 | | |
| $I_{DD2}$ | | | | 11.1 | 12.7 | | |

**SWITCHING CHARACTERISTICS**
Apply over all recommended conditions, $T_A$ = −40°C to +125°C unless otherwise specified. All typical values are measured at $T_A$ = 25°C.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | Figure |
|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | Propagation Delay to Logic Low Output (Note 11) | $V_{DD}$ = 5 V, $V_{IN}$ Square Wave, $C_L$ = 15 pF | – | 95 | 140 | ns | 6, 9 |
| | | $V_{DD}$ = 3.3 V, $V_{IN}$ Square Wave, $C_L$ = 15 pF | | | | | |
| | | $V_{DD}$ = 2.5 V, $V_{IN}$ Square Wave, $C_L$ = 15 pF | | | | | |
| $t_{PLH}$ | Propagation Delay to Logic High Output (Note 12) | $V_{DD}$ = 5 V, $V_{IN}$ Square Wave, $C_L$ = 15 pF | – | 96 | 140 | ns | |
| | | $V_{DD}$ = 3.3 V, $V_{IN}$ Square Wave, $C_L$ = 15 pF | | | | | |
| | | $V_{DD}$ = 2.5 V, $V_{IN}$ Square Wave, $C_L$ = 15 pF | | | | | |
| PWD | Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (Note 13) | $V_{DD}$ = 5 V, $V_{IN}$ Square Wave, $C_L$ = 15 pF | – | 19 | 60 | ns | |
| | | $V_{DD}$ = 3.3 V, $V_{IN}$ Square Wave, $C_L$ = 15 pF | | | | | |
| | | $V_{DD}$ = 2.5 V, $V_{IN}$ Square Wave, $C_L$ = 15 pF | | | | | |
| $t_{PSK(PP)}$ | Propagation Delay Skew (Part to Part) (Note 14) | $V_{DD}$ = 5 V, $V_{IN}$ Square Wave, $C_L$ = 15 pF | −60 | – | 60 | ns | |
| | | $V_{DD}$ = 3.3 V, $V_{IN}$ Square Wave, $C_L$ = 15 pF | | | | | |
| | | $V_{DD}$ = 2.5 V, $V_{IN}$ Square Wave, $C_L$ = 15 pF | | | | | |
| $t_R$ | Output Rise Time (10% to 90%) | $V_{DD}$ = 5 V, $V_{IN}$ Square Wave, $C_L$ = 15 pF | – | 2.7 | – | ns | |
| | | $V_{DD}$ = 3.3 V, $V_{IN}$ Square Wave, $C_L$ = 15 pF | | | | | |
| | | $V_{DD}$ = 2.5 V, $V_{IN}$ Square Wave, $C_L$ = 15 pF | | | | | |
| $t_F$ | Output Fall Time (90% to 10%) | $V_{DD}$ = 5 V, $V_{IN}$ Square Wave, $C_L$ = 15 pF | – | 2.3 | – | ns | |
| | | $V_{DD}$ = 3.3 V, $V_{IN}$ Square Wave, $C_L$ = 15 pF | | | | | |
| | | $V_{DD}$ = 2.5 V, $V_{IN}$ Square Wave, $C_L$ = 15 pF | | | | | |

11. Propagation delay $t_{PHL}$ is measured from the 50% level of the falling edge of the input pulse to the 50% level of the falling edge of the $V_O$ signal.
12. Propagation delay $t_{PLH}$ is measured from the 50% level of the rising edge of the input pulse to the 50% level of the rising edge of the $V_O$ signal.
13. PWD is defined as $\lvert t_{PHL} - t_{PLH} \rvert$ for any given device.
14. Part−to−part propagation delay skew is the difference between the measured propagation delay times of a specified channel of any two parts at identical operating conditions and equal load.

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## TYPICAL PERFORMANCE CHARACTERISTICS

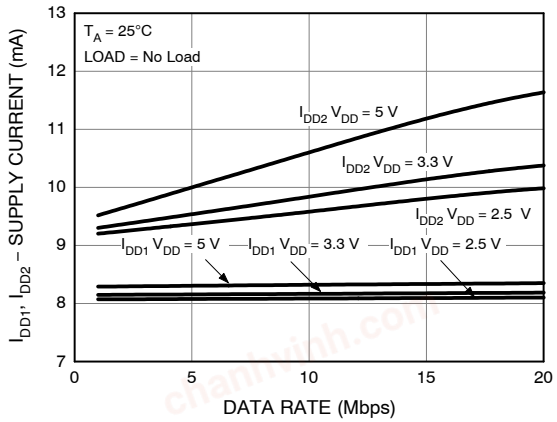



**Figure 3. Supply Current vs. Data Rate (No Load)**

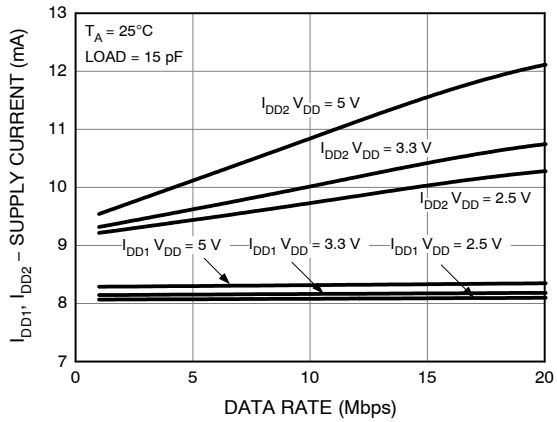



**Figure 4. Supply Current vs. Data Rate (Load = 15 pF)**

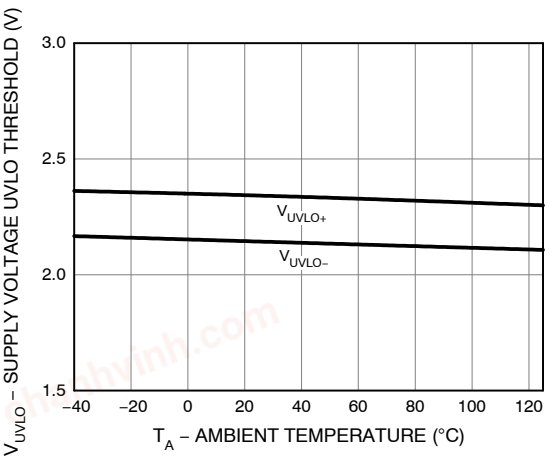



**Figure 5. Supply Voltage UVLO Threshold vs. Ambient Temperature**

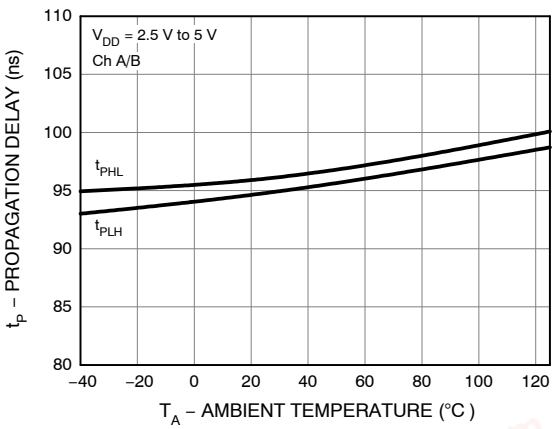



**Figure 6. Propagation Delay vs. Ambient Temperature**

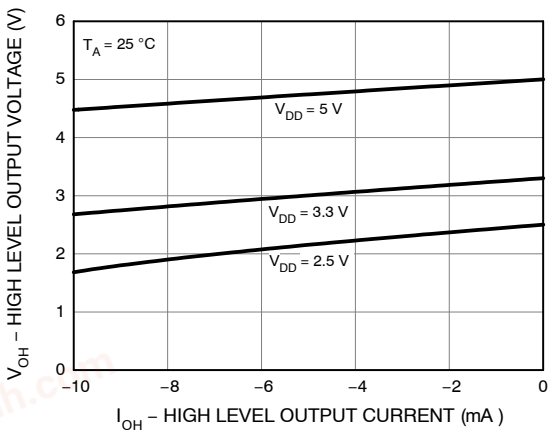



**Figure 7. High Level Output Voltage vs. Current**

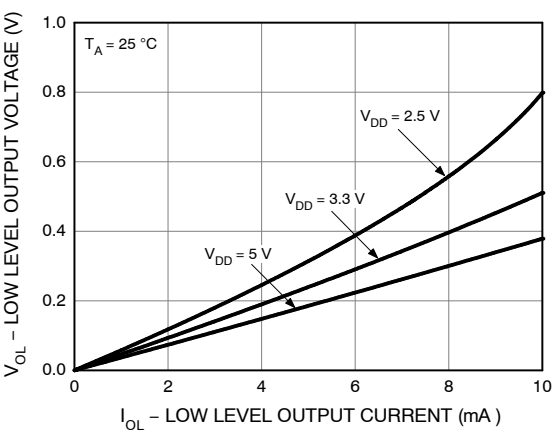



**Figure 8. Low Level Output Voltage vs. Current**

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## TEST CIRCUITS

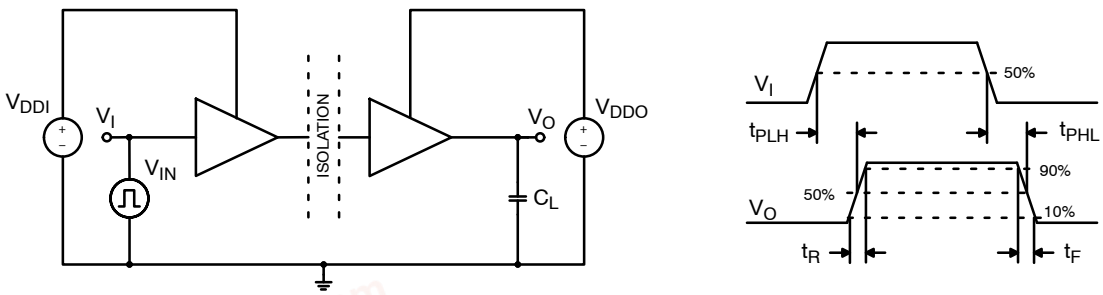
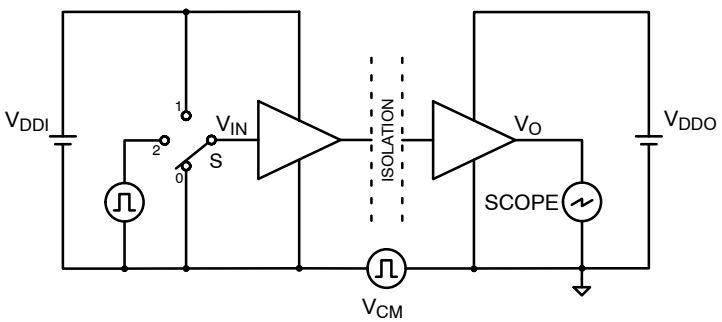



**Figure 9. $V_{IN}$ to $V_O$ Propagation Delay Test Circuit and Waveform**




S at 0, $V_O$ remain consistently low
S at 1, $V_O$ remain consistently high
S at 2, $V_O$ data same as $V_{IN}$ data

**Figure 10. Common Mode Transient Immunity Test Circuit**

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## APPLICATION INFORMATION

### Theory of Operation

NCID9200 is a dual−channel digital isolator. The chip to chip galvanic isolation are provided by a pair of off−chip capacitors. Digital circuits are used for processing signals through the 0.5 mm thick isolation barrier.

Pins are trimmed internally as input or output at IO Switch. Each direction of communication between two isolated circuits are achieved by implementing a pair of Serializer/Deserializer and Manchester Encoder/Decoder functional blocks as shown in Figure 11. The Serializer circuit converts the parallel data from the IO Switch into a serial (one bit) stream and the Manchester Encoder converts this data stream into coded data making it more robust, efficient and accurate for transmission. After encoding, all inputs signals are coded as $V_IT_X$ and transmitted across the isolation barrier via Transceiver.

The off−chip ceramic capacitors that serve both as the isolation barrier and as the medium of transmission for signal switching using On−Off keying (OOK) technique, are illustrated in the transceiver block diagram in Figure 12 and Figure 13. At the transmitter side, the $V_IT_X$ input logic state is modulated with a high frequency carrier signal. The resulting signal is amplified and transmitted to the isolation barrier. The receiver side detects the barrier signal and demodulates it using an envelope detection technique and output $V_OR_X$.

The output signal of the transceiver $V_OR_X$ will go to the Manchester Decoder. This decoder is used along with the receiver to recover the original data from the coded form and the Deserializer converts the serial stream back to the original, parallel data and redistributed back to the corresponding output pins. Both the Serializer/Deserializer and Manchester Encoder/Decoder are functional blocks on the transmitting and receiving chips.

$V_{OX}$ is at default state LOW when the power supply at the transmitter side is turned off or the input $V_{INX}$ is disconnected.

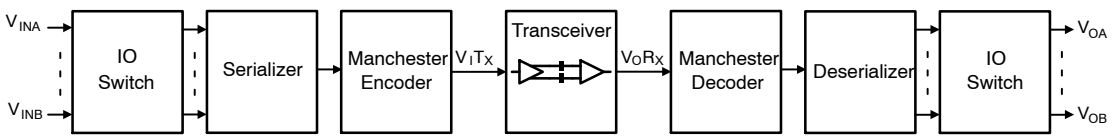



**Figure 11. Operational Block Diagram of Multi−Channels**

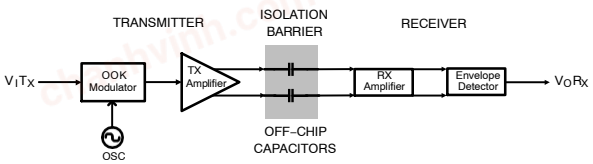



**Figure 12. Block Diagram of Transceiver**

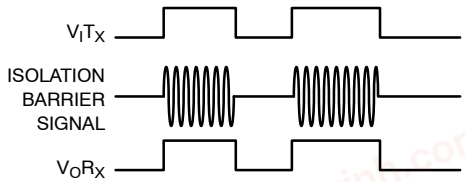



**Figure 13. On−Off Keying Modulation Signals**

### Layout Recommendation

Layout of the digital circuits relies on good suppression of unwanted noise and electromagnetic interference. It is recommended to use 4−layer FR4 PCB, with ground plane below the components, power plane below the ground plane, signal lines and power fill on top, and signal lines and ground fill at the bottom as shown in Figure 14. The alternating polarities of the layers creates interplane capacitances that aids the bypass capacitors required for reliable operation at digital switching rates.

In the layout with digital isolators, it is required that the isolated circuits have separate ground and power planes. The section below the device should be clear with no power, ground or signal traces. Maintain a gap equal to or greater than the specified minimum creepage clearance of the device package.

It is highly advised to connect at least a pair of low ESR supply bypass capacitors, placed within 2 mm from the power supply pins 3 and 14 and ground pins 1 and 16 as shown in Figure 15. Recommended values are 1 μF and 0.1 μF, respectively. Place them between the $V_{DD}$ pins of the device and the via to the power planes, with the higher frequency, lower value capacitor closer to the device pins. Directly connect the device ground pins 1 and 16 by via to their corresponding ground planes.

### Over Temperature Detection

NCID9200 has built−in Over Temperature Detection (OTD) feature that protects the IC from thermal damage. The output pins will automatically switch to default state when the ambient temperature exceeds the maximum junction temperature at threshold of approximately 160°C. The device will return to normal operation when the temperature decreases approximately 20°C below the OTD threshold.

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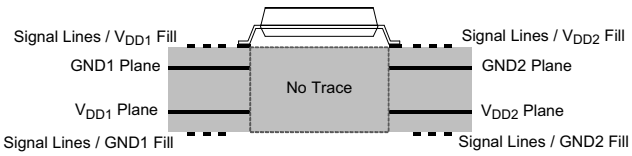



**Figure 14. 4−Layer PCB for Digital Isolator**

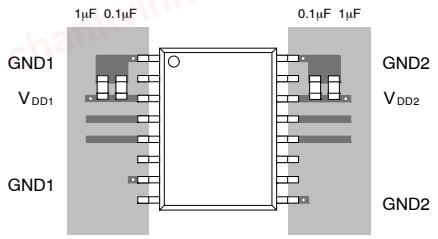



**Figure 15. Placement of Bypass Capacitors**

## ORDERING INFORMATION

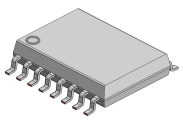
| Part Number | Grade | Package | Shipping† |
|---|---|---|---|
| NCID9200 | Industrial | SOIC16 W | 50 Units / Tube |
| NCID9200R2 | Industrial | SOIC16 W | 750 / Tape & Reel |
| NCIV9200* (pending) | Automotive | SOIC16 W | 50 Units / Tube |
| NCIV9200R2* (pending) | Automotive | SOIC16 W | 750 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCIV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

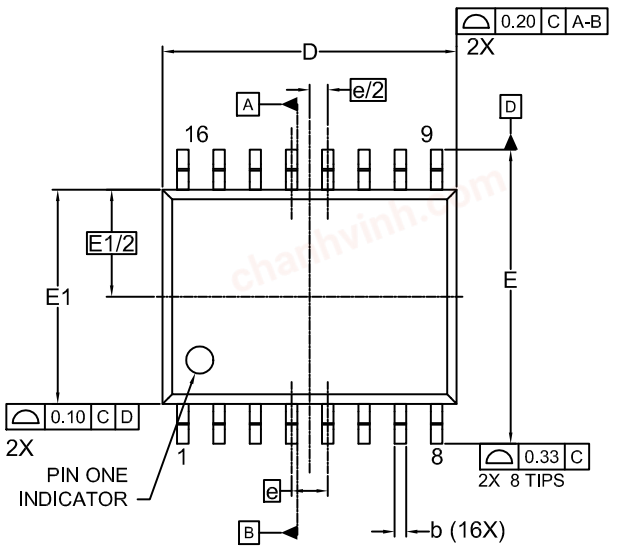
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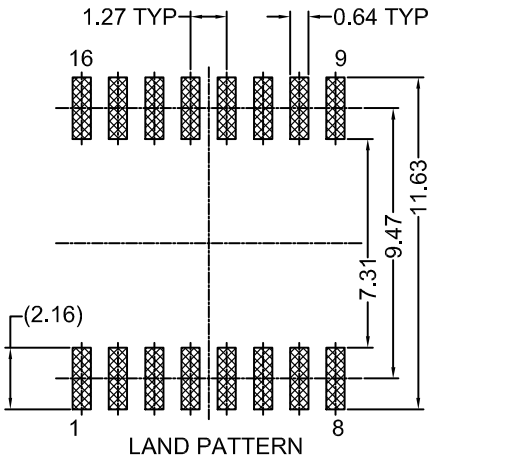
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS



**SOIC16 W**
CASE 751EN
ISSUE A

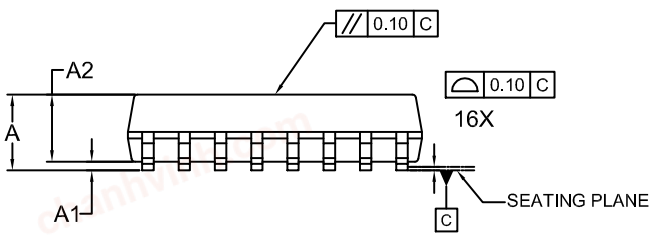
DATE 24 AUG 2021

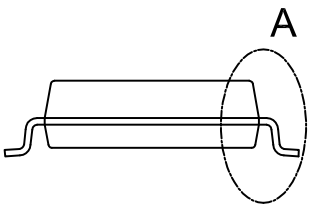


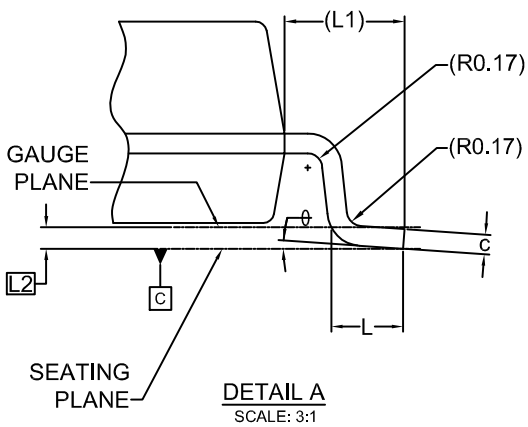




LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



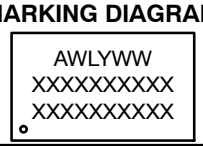

DETAIL A
SCALE: 3:1

| DIM | MILLIMETER | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | – | – | 3.00 |
| A1 | 0.15 | 0.30 | 0.45 |
| A2 | 2.25 | 2.35 | 2.45 |
| b | 0.31 | 0.41 | 0.51 |
| c | 0.19 | 0.22 | 0.25 |
| D | 10.20 | 10.30 | 10.40 |
| E | 10.10 | 10.30 | 10.50 |
| E1 | 7.40 | 7.50 | 7.60 |
| E1/2 | 3.75 BSC | | |
| e | 1.27 BSC | | |
| e/2 | 0.635 BSC | | |
| L | 0.40 | 0.84 | 1.27 |
| L1 | 1.42 REF | | |
| L2 | 0.25 BSC | | |
| θ | 0° | – | 8° |

NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING REFERS TO JEDEC MS-013, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS
D) DRAWING CONFORMS TO ASME Y14.5M-1994
E) LAND PATTERN STANDARD: SOIC127P1030X275-16N
F) DRAWING FILE NAME: MKT-M16FREV2
G) OPTOCOUPLER COMES IN WHITE MOLD BODY.

**GENERIC MARKING DIAGRAM***




XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **SOIC16 W** | **PAGE 1 OF 1** |

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