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Isolated High Current IGBT Gate Driver

NCD57080A, NCD57080B, NCD57080C

NCD57080A, NCD57080B and NCD57080C are high−current single channel IGBT gate drivers with 3.75 kVrms internal galvanic isolation, designed for high system efficiency and reliability in high power applications. The devices accept complementary inputs and depending on the pin configuration, offer options such as Active Miller Clamp (NCD57080A), negative power supply (NCD57080B) and separate high and low (OUTH and OUTL) driver outputs (NCD57080C) for system design convenience. NCD57080 (A/B/C) accommodate wide range of input bias voltage and signal levels from 3.3 V to 20 V. NCD57080 (A/B/C) are available in narrow−body SOIC−8 package.

Features

- High Peak Output Current (+6.5 A/−6.5 A)
- Low Clamp Voltage Drop Eliminates the Need of Negative Power Supply to Prevent Spurious Gate Turn−on (NCD57080A)
- Short Propagation Delays with Accurate Matching
- IGBT Gate Clamping during Short Circuit
- IGBT Gate Active Pull Down
- Tight UVLO Thresholds for Bias Flexibility
- Wide Bias Voltage Range including Negative V_{EE2} (NCD57080B)
- 3.3 V, 5 V, and 15 V Logic Input
- 3.75 kVrms Galvanic Isolation
- High Transient Immunity
- High Electromagnetic Immunity
- This Device is Pb−Free, Halogen Free/BFR Free and is RoHS Compliant

Typical Applications

- Motor Control
- Uninterruptible Power Supplies (UPS)
- Industrial Power Supplies
- HVAC

This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.

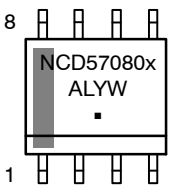
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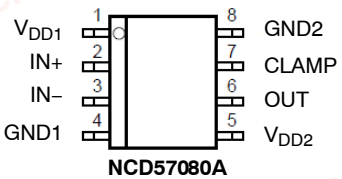
SOIC−8 NB
CASE 751−07

MARKING DIAGRAM

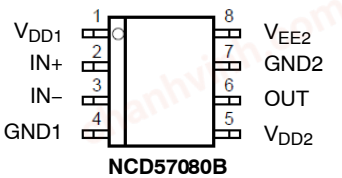


NCD57080	= Specific Device Code
x	= A/B/C
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

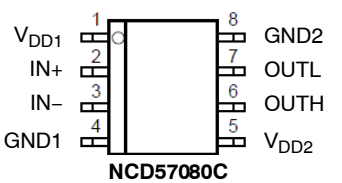
PIN CONNECTIONS



NCD57080A



NCD57080B



NCD57080C

ORDERING INFORMATION

See detailed ordering and shipping information on page 21 of this data sheet.

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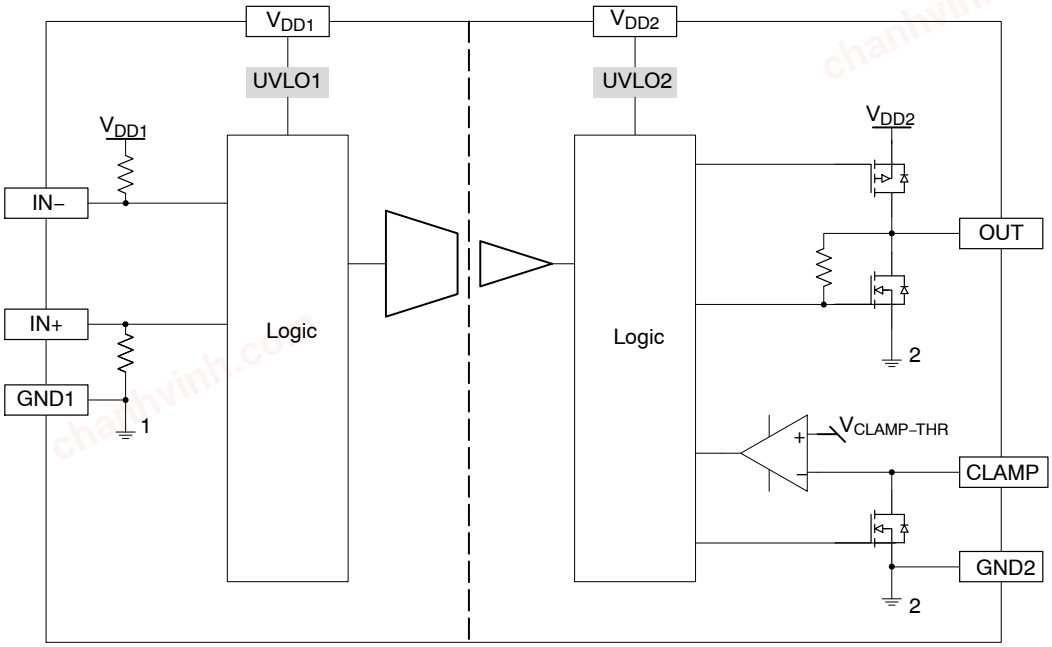


Figure 1. Simplified Block Diagram, NCD57080A

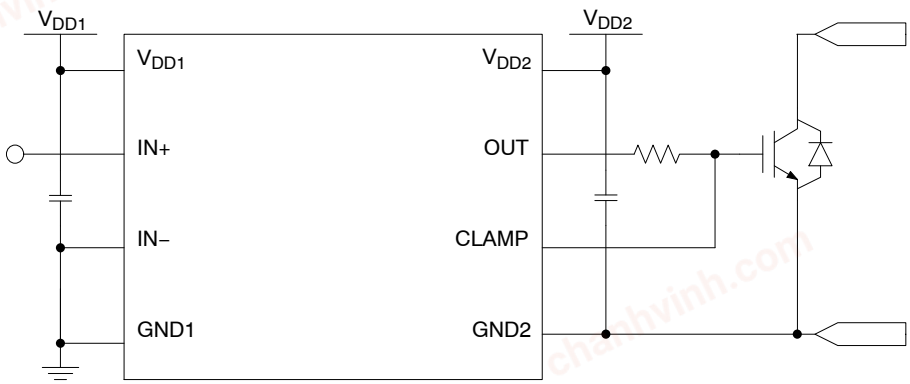


Figure 2. Simplified Application Schematic, NCD57080A

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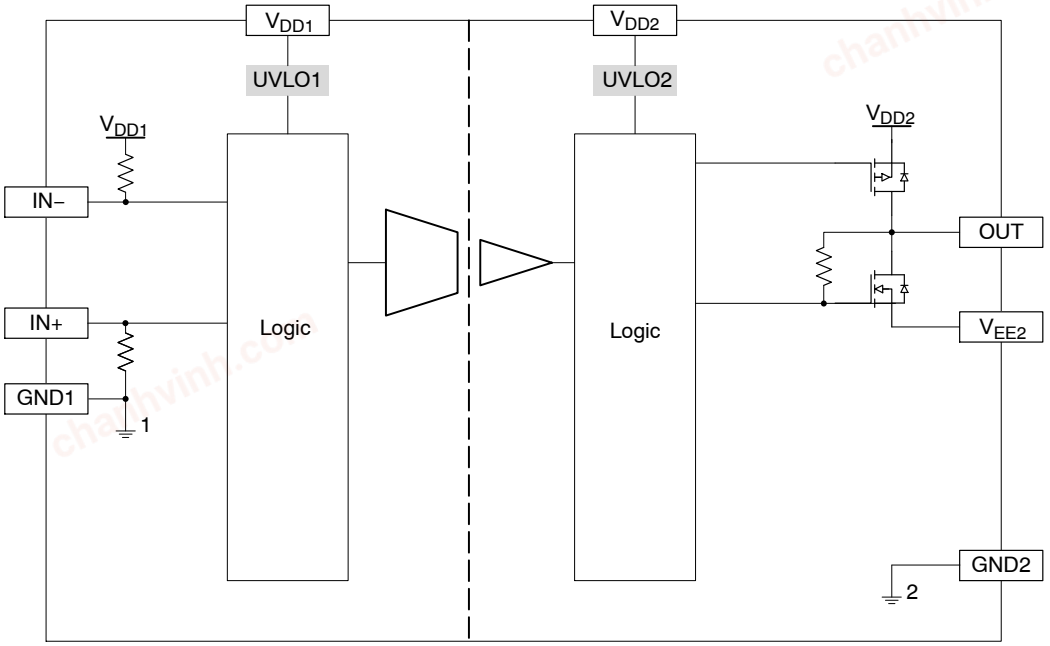


Figure 3. Simplified Block Diagram, NCD57080B

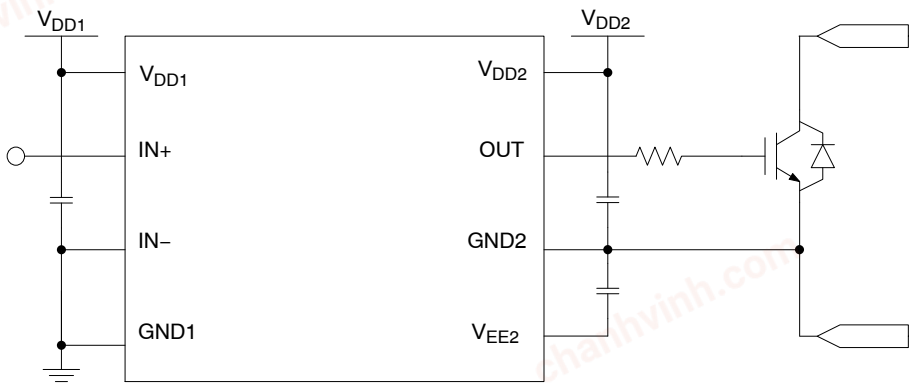


Figure 4. Simplified Application Schematic, NCD57080B

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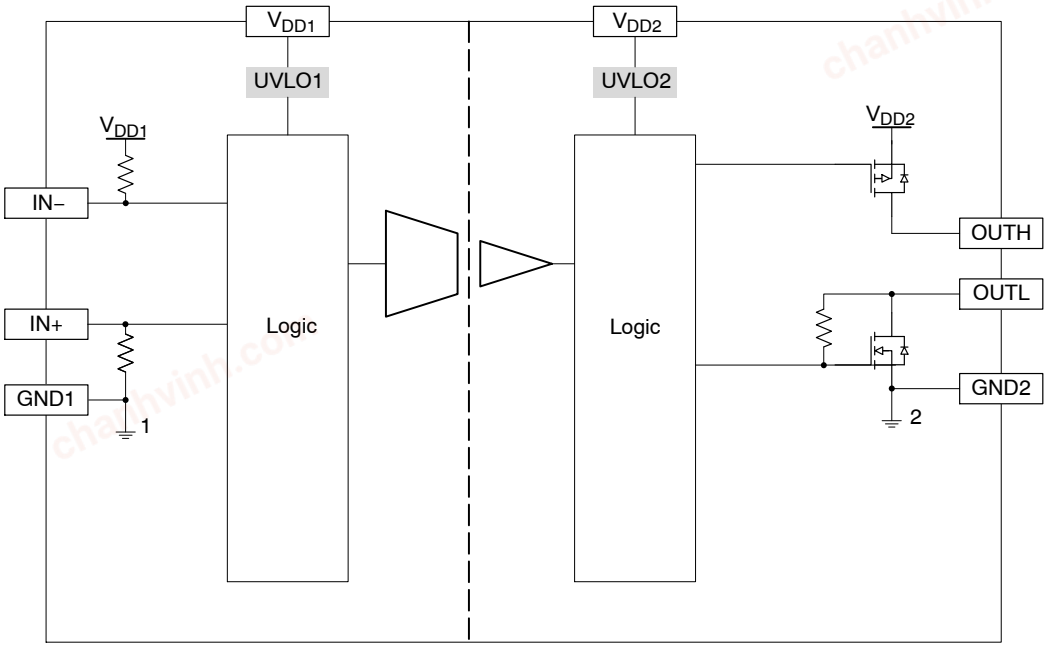


Figure 5. Simplified Block Diagram, NCD57080C

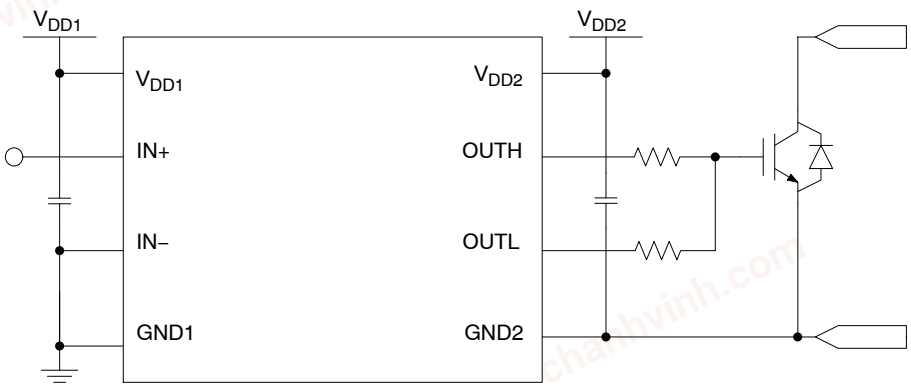


Figure 6. Simplified Application Schematic, NCD57080C

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Table 1. FUNCTION DESCRIPTION

Pin Name	No.	I/O	Description
V_{DD1}	1	Power	Input side power supply. A good quality bypassing capacitor is required from this pin to GND1 and should be placed close to the pins for best results. The under voltage lockout (UVLO) circuit enables the device to operate at power on when a typical supply voltage higher than $V_{UVLO1-OUT-ON}$ is present. Please see Figure 8 for more details.
IN+	2	I	Non inverted gate driver input. It is internally clamped to V_{DD1} and has a pull−down resistor of 50 kΩ to ensure that output is low in the absence of an input signal. A minimum positive or negative going pulse−width is required at IN+ before OUT or OUTH/OUTL responds.
IN−	3	I	Inverted gate driver input. It is internally clamped to V_{DD1} and has a pull−up resistor of 50 kΩ to ensure that output is low in the absence of an input signal. A minimum negative or positive going pulse−width is required at IN− before OUT or OUTH/OUTL responds.
GND1	4	Power	Input side ground reference.
V_{DD2}	5	Power	Output side positive power supply. The operating range for this pin is from UVLO2 to its maximum allowed value. A good quality bypassing capacitor is required from this pin to GND2 and should be placed close to the pins for best results.
GND2 (NCD57080A, NCD57080C)	8	Power	Output side gate drive reference connecting to IGBT emitter or FET source.
GND2 (NCD57080B)	7		
OUT (NCD57080A, NCD57080B)	6	O	Driver output that provides the appropriate drive voltage and source/sink current to the IGBT/FET gate. OUT is actively pulled low during start−up.
OUTH (NCD57080C)	6	O	Driver high output that provides the appropriate drive voltage and source current to the IGBT/FET gate.
OUTL (NCD57080C)	7	O	Driver low output that provides the appropriate drive voltage and sink current to the IGBT/FET gate. OUTL is actively pulled low during start−up.
CLAMP (NCD57080A)	7	O	Provides clamping for the IGBT/FET gate during the off period to protect it from parasitic turn−on. Its internal N FET is turned on when the voltage of this pin falls below $V_{CLAMP-THR}$. It is to be tied directly to IGBT/FET gate with minimum trace length for best results.
V_{EE2} (NCD57080B)	8	Power	Output side negative power supply. A good quality bypassing capacitor is required from this pin to GND2 and should be placed close to the pins for best results.

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Table 2. ABSOLUTE MAXIMUM RATINGS (Note 1) Over operating free−air temperature range unless otherwise noted.

Parameter	Symbol	Minimum	Maximum	Unit
Supply voltage, input side	V_{DD1}−GND1	−0.3	22	V
Positive Power Supply, output side	V_{DD2}−GND2	−0.3	32	V
Negative Power Supply, output side	V_{EE2}−GND2	−18	0.3	V
Differential Power Supply, output side (NCD57080B)	V_{DD2}−V_{EE2} (V_{MAX2})	0	36	V
Gate−driver output high voltage NCD57080A NCD57080B NCD57080C	 V_{OUT} − GND2 V_{OUT} − GND2 V_{OUTH} − GND2		V_{DD2} + 0.3	V
Gate−driver output low voltage NCD57080A NCD57080B NCD57080C	 V_{OUT} − GND2 V_{OUT} − V_{EE2} V_{OUTL} − GND2	−0.3		V
Gate−driver output sourcing current (maximum pulse width = 10 μs, maximum duty cycle = 0.2%, V_{DD2} = 15 V, V_{EE2} = 0 V)	I_{PK-SRC}		6.5	A
Gate−driver output sinking current (maximum pulse width = 10 μs, maximum duty cycle = 0.2%, V_{DD2} = 15 V, V_{EE2} = 0 V)	I_{PK-SNK}		6.5	A
Clamp sinking current (maximum pulse width = 10 μs, maximum duty cycle = 0.2%, V_{CLAMP} = 2.5 V)	$I_{PK-CLAMP}$		2.5	A
Maximum Short Circuit Clamping Time (I_{OUT_CLAMP} = 500 mA)	t_{CLP}		10	μs
Voltage at IN+, IN−	V_{LIM}−GND1	−0.3	V_{DD1} + 0.3	V
Clamp Voltage	V_{CLAMP}−GND2	−0.3	V_{DD2} + 0.3	V
Power Dissipation (SOIC−8 narrow package) with 4−layer board	PD		1315	mW
Input to Output Isolation Voltage	V_{ISO}	−1200	1200	V
Maximum Junction Temperature	T_J(max)	−40	150	°C
Storage Temperature Range	T_{STG}	−65	150	°C
ESD Capability, Human Body Model (Note 2)	ESDHBM		± 2	kV
ESD Capability, Charged Device Model (Note 2)	ESDCDM		± 2	kV
Moisture Sensitivity Level	MSL		1	−
Lead Temperature Soldering Reflow, Pb−Free (Note 3)	T_{SLD}		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114).
   ESD Charged Device Model tested per AEC−Q100−011 (EIA/JESD22−C101).
   Latchup Current Maximum Rating: ≤ 100 mA per JEDEC standard: JESD78, 25°C.
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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Table 3. THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Characteristics, SOIC−8 narrow body (Note 4) Thermal Resistance, Junction−to−Air (Note 5)	$R_{\theta JA}$	95 (4−layer board) 175 (1−layer board)	°C/W

4. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
5. Values based on copper area of 100 mm² (or 0.16 in²) of 1 oz copper thickness and FR4 PCB substrate.

Table 4. OPERATING RANGES (Note 6)

Parameter	Symbol	Min	Max	Unit
Supply voltage, input side	$V_{DD1-GND1}$	UVLO1	20	V
Positive Power Supply, output side	$V_{DD2-GND2}$	UVLO2	30	V
Negative Power Supply, output side (NCD57080B)	$V_{EE2-GND2}$	−15	0	V
Differential Power Supply, output side (NCD57080B)	$V_{DD2-VEE2}$ (V_{MAX2})	0	32	V
Low level input voltage at IN+, IN− (Note 7)	V_{IL}	0	0.3 x V_{DD1}	V
High level input voltage at IN+, IN− (Note 7)	V_{IH}	0.7 x V_{DD1}	V_{DD1}	V
Common Mode Transient Immunity	$\lvert dV_{ISO}/dt \rvert$	100		kV/μs
Ambient Temperature	T_A	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
7. Table values are valid for 3.3 V and 5 V V_{DD1}, for higher V_{DD1} voltages, the threshold values are maintained at the 5 V V_{DD1} levels.

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Table 5. ELECTRICAL CHARACTERISTICS V_{DD1} = 5 V, V_{DD2} = 15 V, (V_{EE2} = 0 V for NCD57080B).
For typical values T_A = 25°C, for min/max values, T_A is the operating ambient temperature range that applies, unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
VOLTAGE SUPPLY						
UVLO1 Output Enabled		$V_{UVLO1-OUT-ON}$			3.1	V
UVLO1 Output Disabled		$V_{UVLO1-OUT-OFF}$	2.4			V
UVLO1 Hysteresis		$V_{UVLO1-HYST}$	0.1			V
UVLO2 Output Enabled		$V_{UVLO2-OUT-ON}$	12.4	12.9	13.4	V
UVLO2 Output Disabled		$V_{UVLO2-OUT-OFF}$	11.5	12	12.5	V
UVLO2 Hysteresis		$V_{UVLO2-HYST}$		1		V
Input Supply Quiescent Current	IN+ = Low, IN− = Low, V_{DD1} = 3.3 V	$I_{DD1-0-3.3}$			2	mA
	IN+ = Low, IN− = Low	$I_{DD1-0-5}$			2	mA
	IN+ = Low, IN− = Low, V_{DD1} = 15 V	$I_{DD1-0-15}$			2	mA
	IN+ = High, IN− = Low	$I_{DD1-100-5}$			5.5	mA
Output Positive Supply Quiescent Current	IN+ = Low, IN− = Low, no load	I_{DD2-0}			2	mA
	IN+ = High, IN− = Low, no load	$I_{DD2-100}$			2	mA
Output Negative Supply Quiescent Current (NCD57080B)	IN+ = Low, IN− = Low, no load, V_{EE2} = −8 V	I_{EE2-0}			2	mA
	IN+ = High, IN− = Low, no load, V_{EE2} = −8 V	$I_{EE2-100}$			2	mA
LOGIC INPUT AND OUTPUT						
IN+, IN−, Low Input Voltage (Note 7)		V_{IL}			0.3 x V_{DD1}	V
IN+, IN−, High Input Voltage (Note 7)		V_{IH}	0.7 x V_{DD1}			V
Input Hysteresis Voltage (Note 7)		$V_{IN-HYST}$		0.15 x V_{DD1}		V
IN− Input Current	V_{IN-} = 0 V, V_{DD1} = 3.3 V	$I_{IN-L-3.3}$			100	μA
	V_{IN-} = 0 V	I_{IN-L-5}			100	μA
	V_{IN-} = 0 V, V_{DD1} = 15 V	$I_{IN-L-15}$			100	μA
	V_{IN-} = 0 V, V_{DD1} = 20 V	$I_{IN-L-20}$			100	μA
IN+ Input Current	V_{IN+} = V_{DD1} = 3.3 V	$I_{IN+H-3.3}$			100	μA
	V_{IN+} = V_{DD1} = 5 V	I_{IN+H-5}			100	μA
	V_{IN+} = V_{DD1} = 15 V	$I_{IN+H-15}$			100	μA
	V_{IN+} = V_{DD1} = 20 V	$I_{IN+H-20}$			100	μA
Input Pulse Width of IN+, IN− for Guaranteed No Response at Output		$t_{ON-MIN1}$			10	ns
Input Pulse Width of IN+, IN− for Guaranteed Response at Output		$t_{ON-MIN2}$	40			ns
DRIVER OUTPUT						
Output Low State (V_{OUT} − GND2 for NCD57080A) (V_{OUT} − V_{EE2} for NCD57080B) (V_{OUTL} − GND2 for NCD57080C)	I_{SINK} = 200 mA	V_{OUTL1}		0.15	0.3	V
	I_{SINK} = 1.0 A, T_A = 25°C	V_{OUTL2}			0.8	

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Table 5. ELECTRICAL CHARACTERISTICS V_{DD1} = 5 V, V_{DD2} = 15 V, (V_{EE2} = 0 V for NCD57080B).
For typical values T_A = 25°C, for min/max values, T_A is the operating ambient temperature range that applies, unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
DRIVER OUTPUT						
Output High State (V_{DD2} – V_{OUT} for NCD57080A) (V_{DD2} – V_{OUT} for NCD57080B) (V_{DD2} – V_{OUTL} for NCD57080C)	I_{SRC} = 200 mA	V_{OUTH1}		0.2	0.35	V
	I_{SRC} = 1.0 A, T_A = 25°C	V_{OUTH2}			1.0	
Peak Driver Current, Sink		$I_{PK-SNK1}$		6.5		A
Peak Driver Current, Source		$I_{PK-SRC1}$		6.5		A
MILLER CLAMP (NCD57080A)						
Clamp Voltage	I_{CLAMP} = 2.5 A, T_A = 25°C	V_{CLAMP}		2		V
	I_{CLAMP} = 2.5 A, T_A = –40°C to 125°C				3.5	
Clamp Activation Threshold		$V_{CLAMP-THR}$	1.5	2	2.5	V
IGBT SHORT CIRCUIT CLAMPING						
Clamping Voltage, Sourcing (V_{OUT} / V_{OUTH} – V_{DD2})	IN+ = Low, IN– = High, $I_{CLAMP-OUT/OUTH}$ = 500 mA, (pulse test, t_{CLPmax} = 10 μs)	$V_{CLAMP-OUTH}$		0.7	0.9	V
Clamping Voltage, Sinking (V_{OUTL} – V_{DD2})	IN+ = High, IN– = Low, $I_{CLAMP-OUTL}$ = 500 mA, (pulse test, t_{CLPmax} = 10 μs)	$V_{CLAMP-OUTL}$		0.8	1.5	V
Clamping Voltage, Clamp (V_{CLAMP} – V_{DD2}) (NCD57080A)	IN+ = High, IN– = Low, $I_{CLAMP-CLAMP}$ = 500 mA (pulse test, t_{CLPmax} = 10 μs)	$V_{CLAMP-CLAMP}$		1.1	1.7	V
DYNAMIC CHARACTERISTIC						
IN+, IN– to Output High Propagation Delay	C_{LOAD} = 10 nF V_{IH} to 10% of output change Pulse Width > 150 ns.					
	V_{DD1} = V_{IN+} = 3.3V, V_{IN-} = 0 V	$t_{PD-ON-3.3}$	40	60	90	ns
	V_{DD1} = V_{IN+} = 5 V, V_{IN-} = 0 V	$t_{PD-ON-5}$	40	60	90	ns
	V_{DD1} = V_{IN+} = 15 V, V_{IN-} = 0 V	$t_{PD-ON-15}$	40	60	90	ns
	V_{DD1} = V_{IN+} = 20 V, V_{IN-} = 0 V	$t_{PD-ON-20}$	40	60	90	ns
IN+, IN– to Output Low Propagation Delay	C_{LOAD} = 10 nF V_{IH} to 10% of output change Pulse Width > 150 ns.					
	V_{DD1} = V_{IN+} = 3.3 V, V_{IN-} = 0 V	$t_{PD-OFF-3.3}$	40	60	90	ns
	V_{DD1} = V_{IN+} = 5 V, V_{IN-} = 0 V	$t_{PD-OFF-5}$	40	60	90	ns
	V_{DD1} = V_{IN+} = 15 V, V_{IN-} = 0 V	$t_{PD-OFF-15}$	40	60	90	ns
	V_{DD1} = V_{IN+} = 20 V, V_{IN-} = 0 V	$t_{PD-OFF-20}$	40	60	90	ns
Propagation Delay Distortion (= t_{PD-ON} – t_{PD-OFF})	T_A = 25°C, PW > 150 ns	$t_{DISTORT}$		–6		ns
	T_A = –40°C to 125°C, PW > 150 ns		–25		25	ns
Prop Delay Distortion between Parts	PW > 150 ns	$t_{DISTORT_TOT}$	–30	0	30	ns
Rise Time (see Fig. 3)	C_{LOAD} = 1 nF, 10% to 90% of Output Change			13		ns
Fall Time (see Fig. 3)	C_{LOAD} = 1 nF, 90% to 10% of Output Change			13		ns
UVLO1 Fall Delay		t_{UVF1}		1500		ns

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Table 5. ELECTRICAL CHARACTERISTICS V_{DD1} = 5 V, V_{DD2} = 15 V, (V_{EE2} = 0 V for NCD57080B).
For typical values T_A = 25°C, for min/max values, T_A is the operating ambient temperature range that applies, unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTIC						
UVLO1 Rise Delay		t_{UVR1}		770		ns
UVLO2 Fall Delay		t_{UVF2}		1000		ns
UVLO2 Rise Delay		t_{UVR2}		1000		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
8. Values based on design and/or characterization.

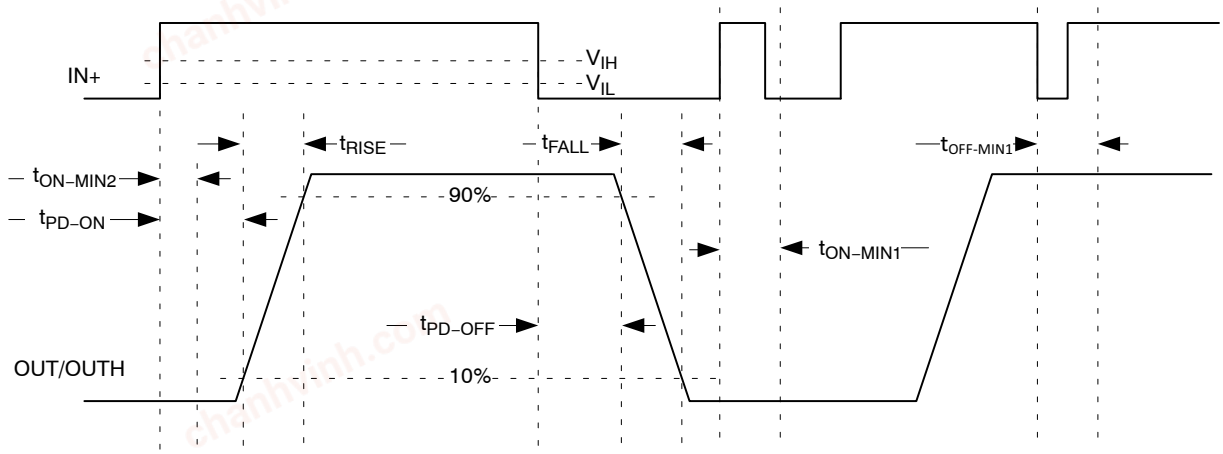


Figure 7. Propagation Delay, Rise and Fall time

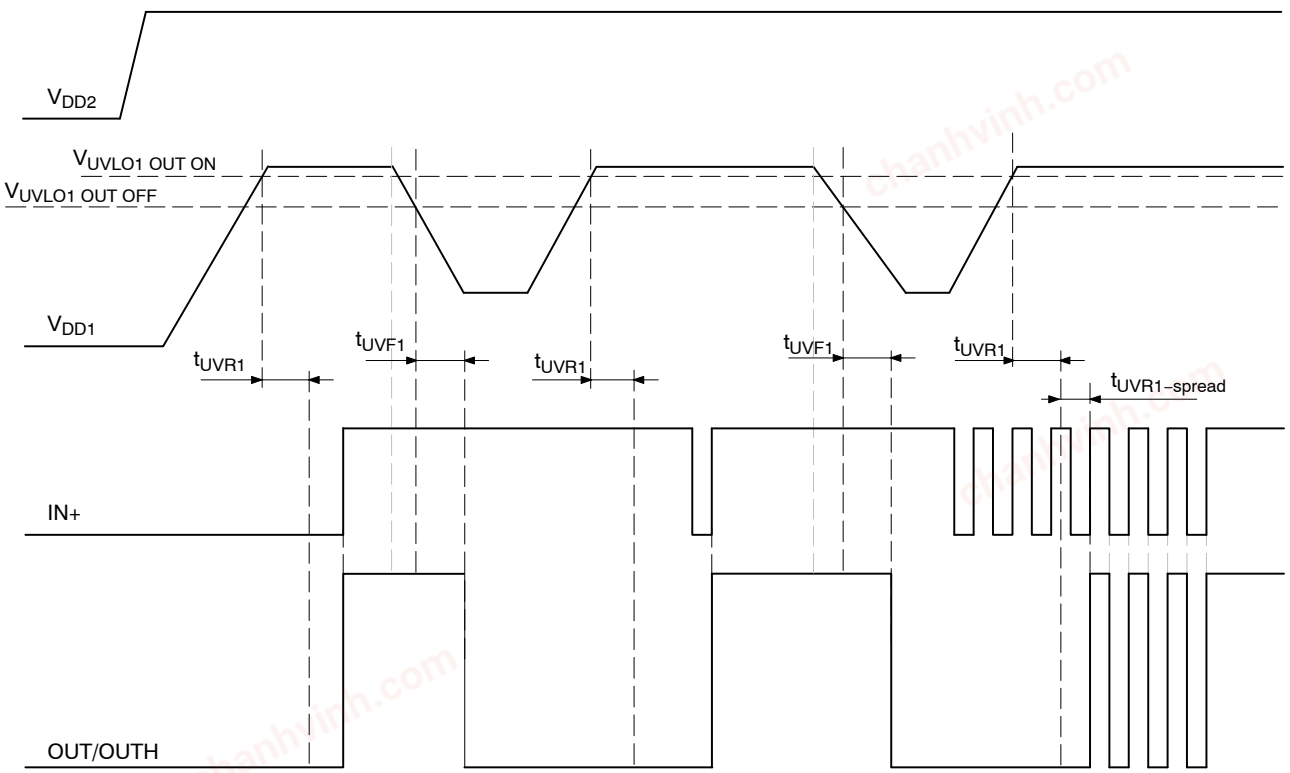


Figure 8A. UVLO1 and Associated Timing Waveforms

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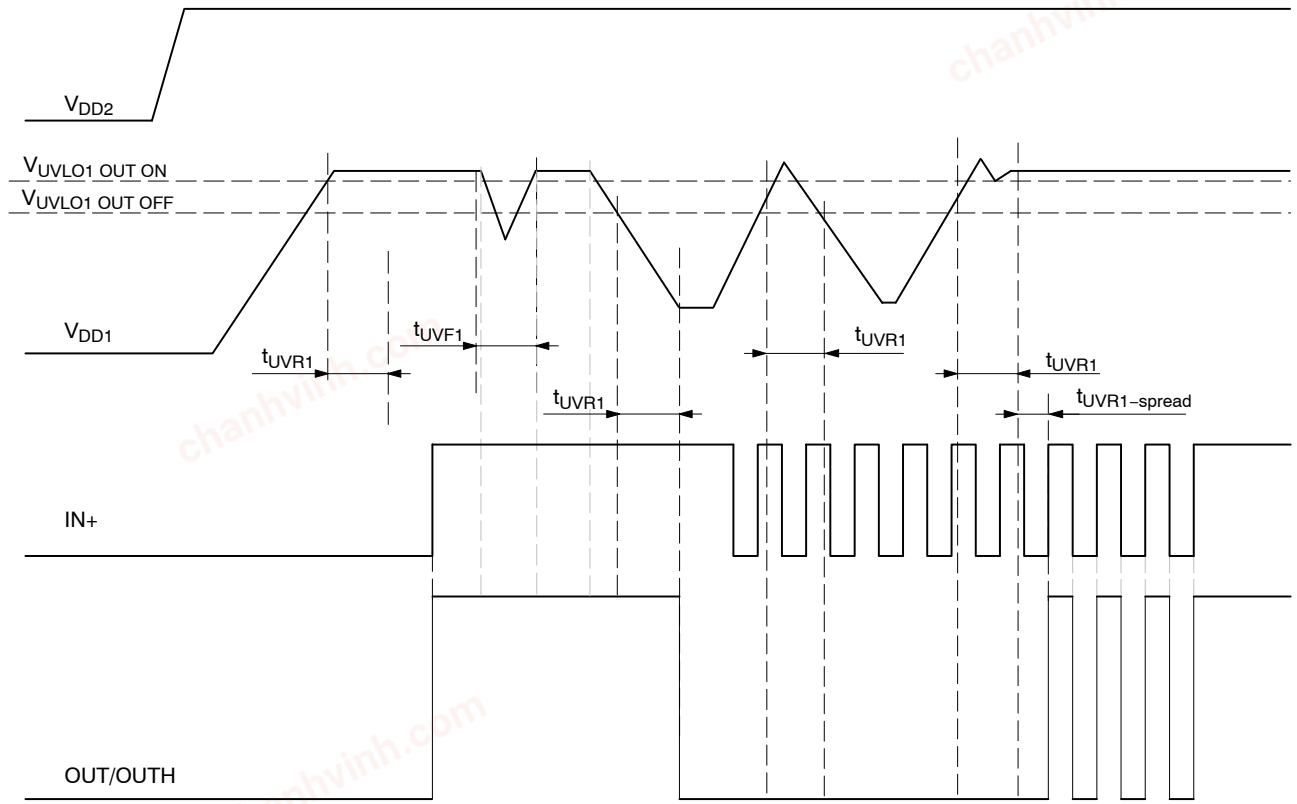


Figure 8B. UVLO1 Waveforms Depicting V_{DD1} Glitch Filtering

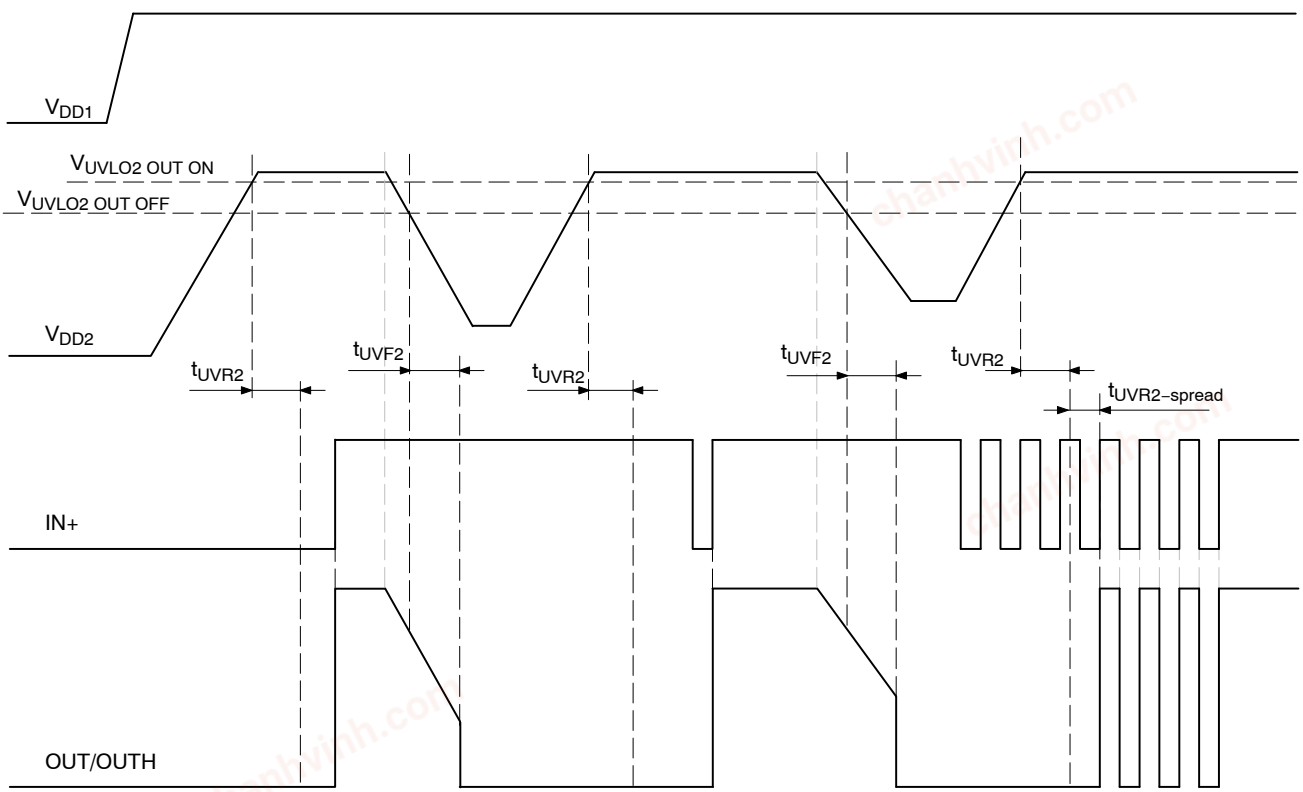


Figure 8C. UVLO2 and Associated Timing Waveforms

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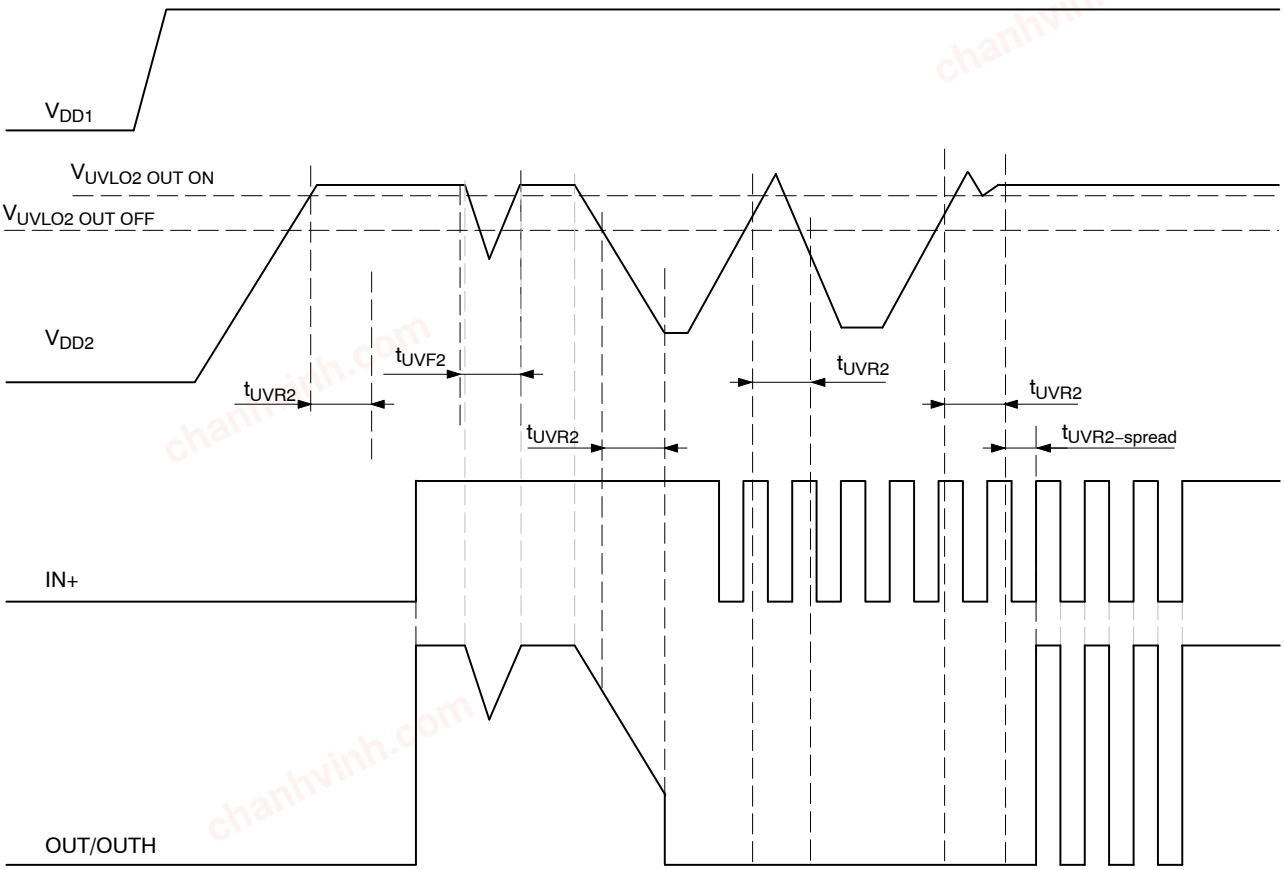


Figure 8D. UVLO2 Waveforms Depicting V_{DD2} Glitch Filtering

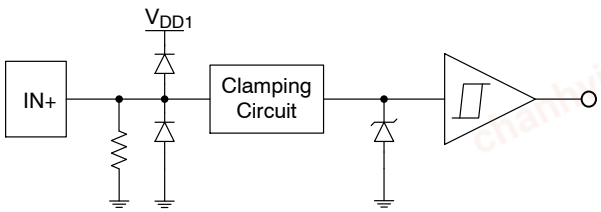


Figure 9. Input Pin Structure

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TYPICAL CHARACTERISTICS

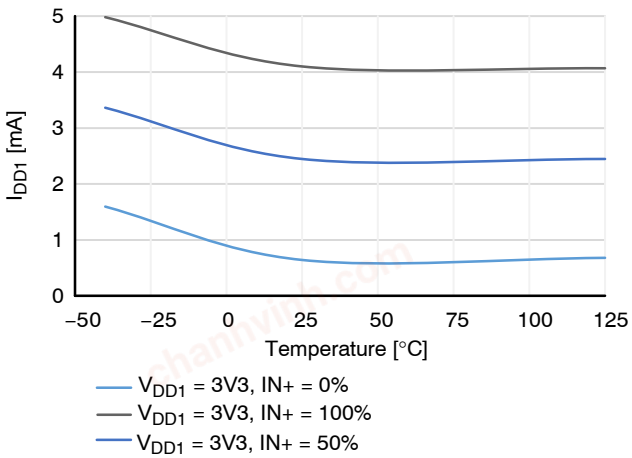


Figure 10. I_{DD1} Supply Current V_{DD1} = 3.3 V

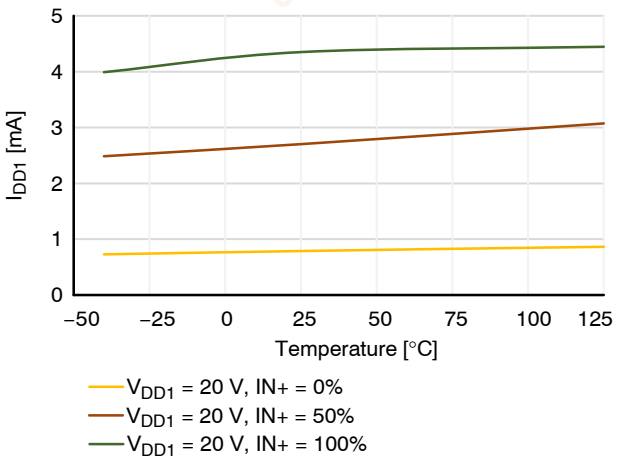


Figure 11. I_{DD1} Supply Current V_{DD1} = 20 V

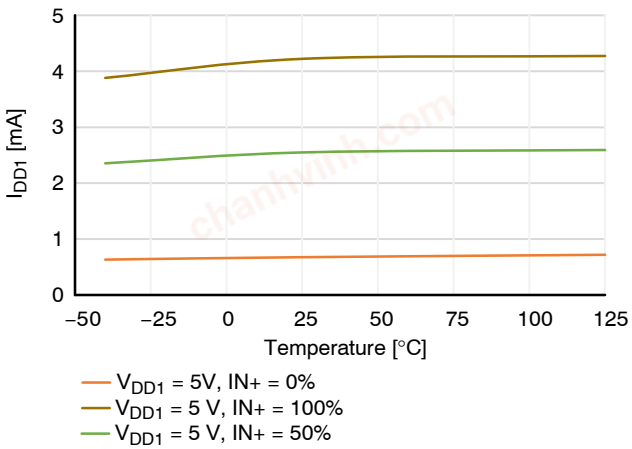


Figure 12. I_{DD1} Supply Current V_{DD1} = 5 V

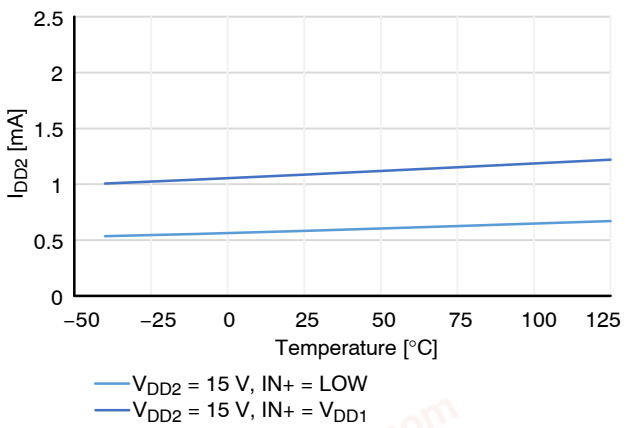


Figure 13. I_{DD2} Supply Current V_{DD2} = 15 V

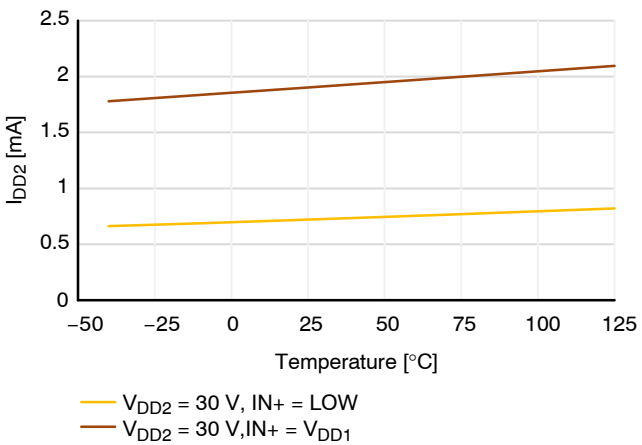


Figure 14. I_{DD2} Supply Current V_{DD2} = 30 V

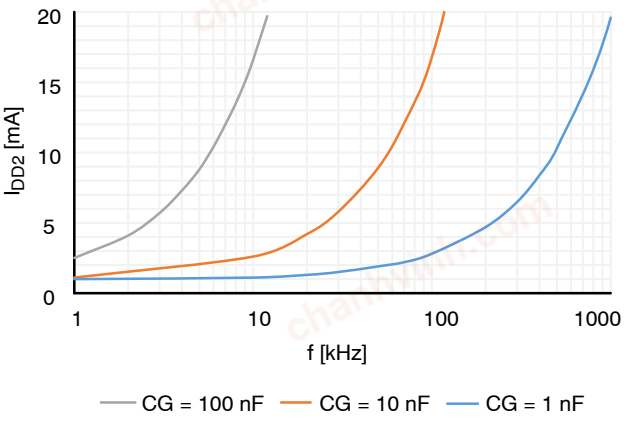


Figure 14a. I_{DD2} vs. Switching Frequency

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TYPICAL CHARACTERISTICS (continued)

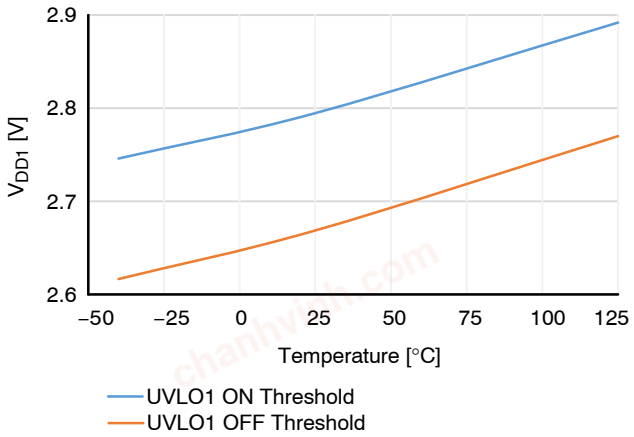


Figure 15. UVLO1 Threshold Voltage

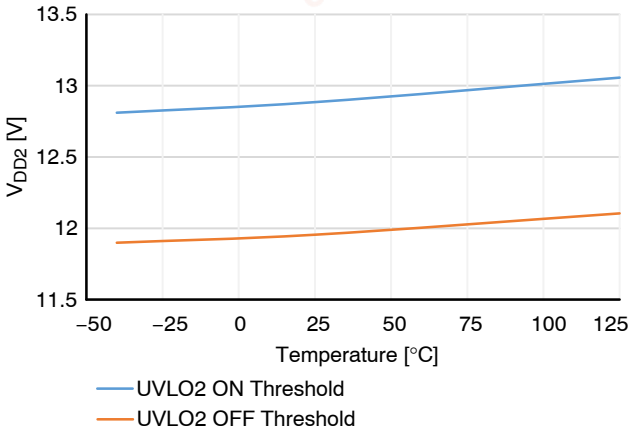


Figure 16. UVLO2 Threshold Voltage

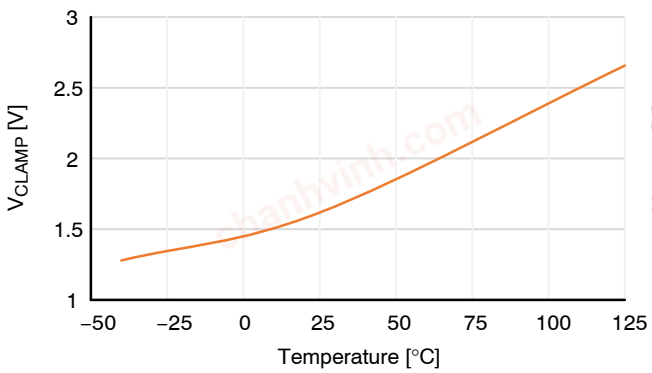


Figure 17a. Miller Clamp Voltage (2.5 A)

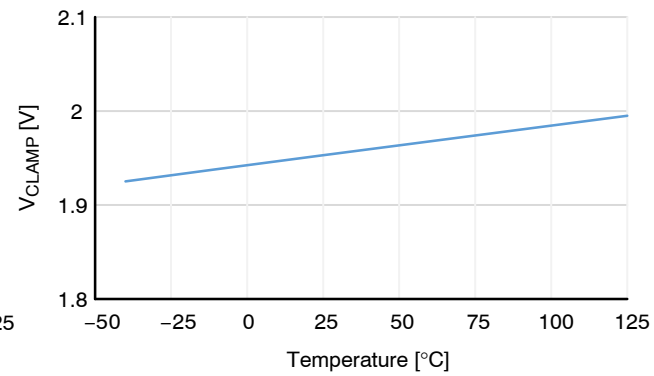


Figure 17b. Miller Clamp Activation Voltage Threshold

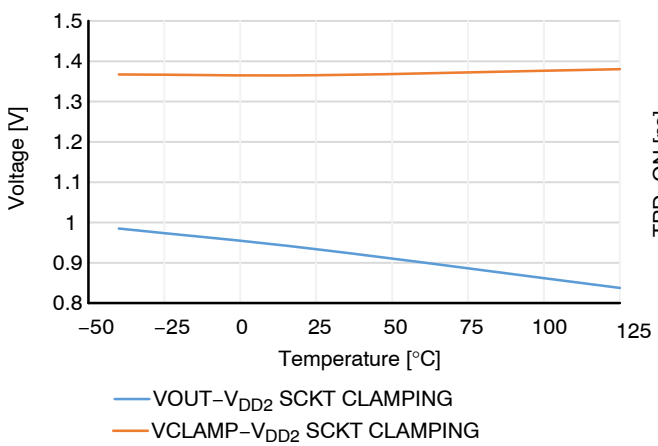


Figure 18. IGBT Short Circuit CLAMP Voltage Drop

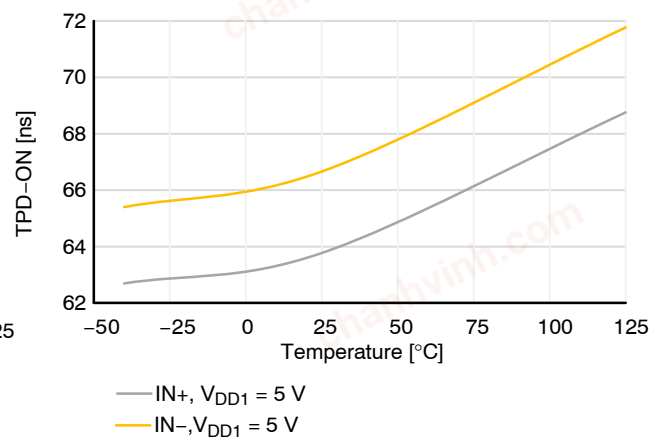


Figure 19. Propagation Delay Turn−on

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TYPICAL CHARACTERISTICS (continued)

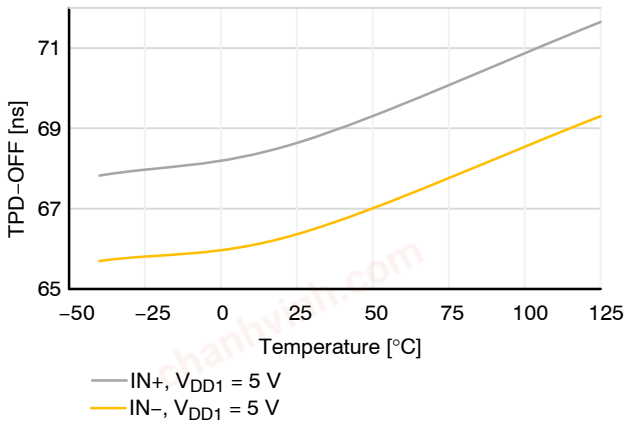


Figure 20. Propagation Delay Turn−off

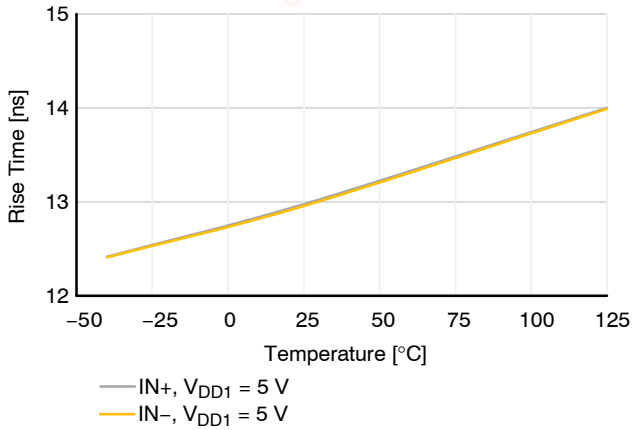


Figure 21. Rise Time

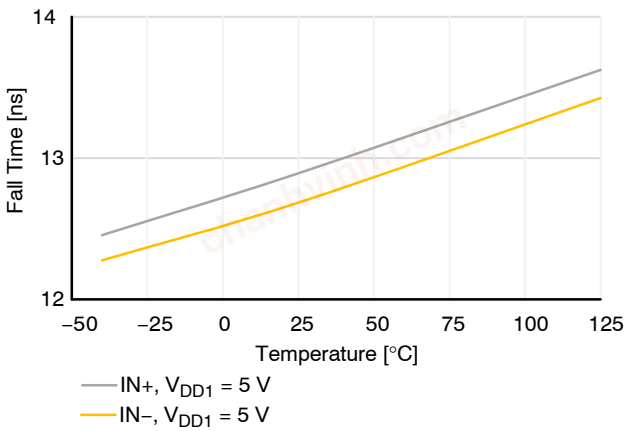


Figure 22. Fall Time

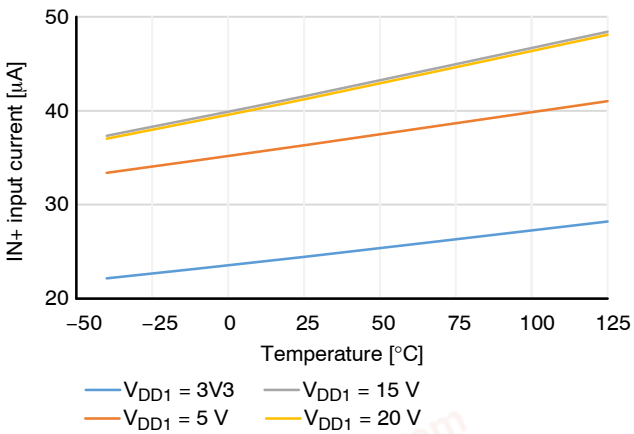


Figure 23. Input Current – Positive Input

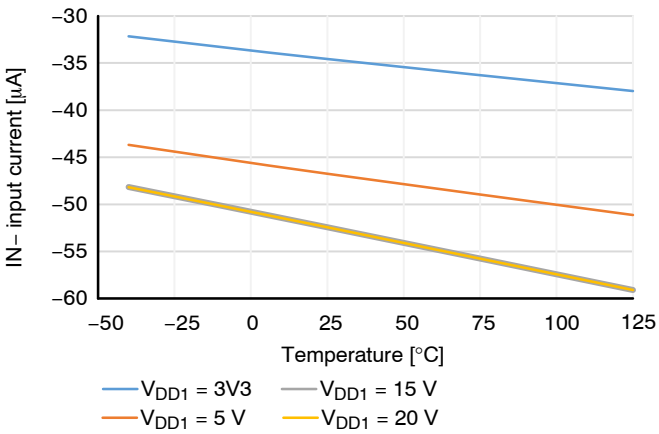


Figure 24. Input Current – Negative Input

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Under Voltage Lockout (Refer to Figure 8A/8B/8C/8D)

UVLO ensures correct switching of IGBT connected to the driver output.

- The IGBT is turned−off and the output is disabled, if the supply V_{DD1} drops below $V_{UVLO1-OUT-OFF}$ or V_{DD2} drops below $V_{UVLO2-OUT-OFF}$.
- The driver output does not follow the input signal on IN+ or IN− until the V_{DDX} rises above the $V_{UVLOX-OUT-ON}$ and the input signal rising edge is applied to the IN+ or IN−
- V_{EE2} is not monitored (NCD57080B)

With high loading gate capacitances over 10 nF it is important to follow the decoupling capacitor routing guidelines as shown on Figure 32. The decoupling capacitor value should be at least 10 μF. Also gate resistor of minimal value of 2 Ω has to be used in order to avoid interference of the high di/dt with internal circuitry (e.g. UVLO2).

After the power−on of the driver there has to be a rising edge applied to the IN+ or falling edge to the IN− in order for the output to start following the inputs. This serves as a protection against producing partial pulses at the output if the V_{DD1} or V_{DD2} is applied in the middle of the input PWM pulse.

If the V_{DD2} rises over $V_{UVLO-OUT-ON}$ level the PWM will appear on the output after $t_{UVR2} + t_{UVR2-spread}$. The $t_{UVR2-spread}$ time is variable and is defined as a time from end of t_{UVR2} to first rising edge on IN+ input. If the V_{DD2} is starting from 0 V the time until PWM is at the output of the driver is longer than $t_{UVR2} + t_{UVR2-spread}$. This is caused by start up time of internal circuits of the driver.

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ACTIVE MILER CLAMP PROTECTION (CLAMP)

NCD57080B supports bipolar power supply to prevent unintentional turning on.

For operation with bipolar supplies, the IGBT is turned off with a negative voltage through OUT with respect to its emitter. This prevents the IGBT from unintentionally turning on because of current induced from its collector to its gate due to Miller effect. Typical values for bipolar operation are V_{DD2} = 15 V and V_{EE2} = −5 V with respect to GND2.

NCD57080A supports unipolar power supply with active Miller clamp.

For operation with unipolar supply, typically, V_{DD2} = 15 V with respect to GND2, and V_{EE2} = GND2. In this case, the IGBT can turn on due to additional charge from IGBT Miller capacitance caused by a high voltage slew rate transition on the IGBT collector. To prevent IGBT to turn on, the CLAMP pin is connected directly to IGBT gate and Miller current is sinked through a low impedance CLAMP transistor. When the IGBT is turned−off and the gate voltage transitions below V_{CLAMP}, the CLAMP output is activated

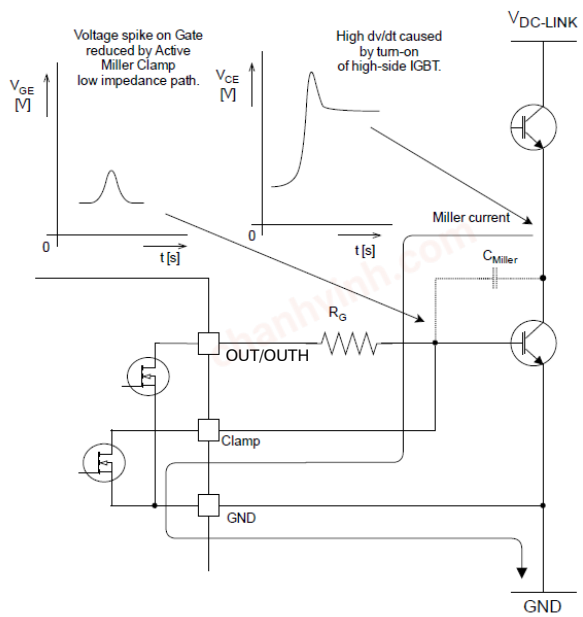


Figure 25. Current Path with Miler Clamp Protection

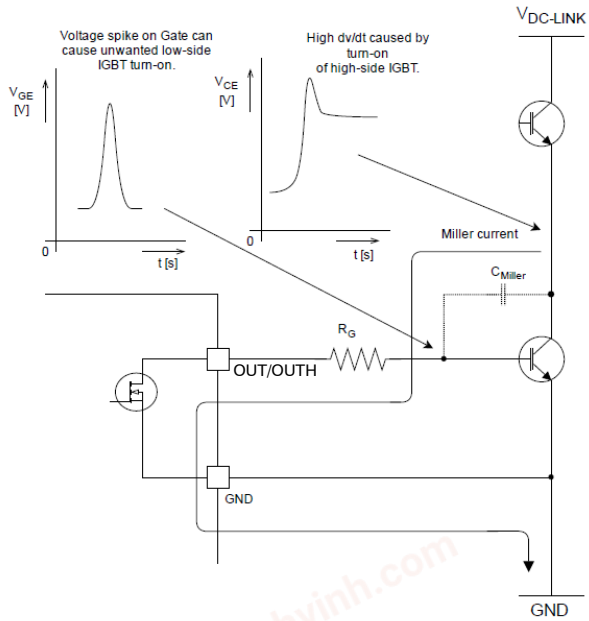


Figure 26. Current Path without Miler Clamp Protection

Non−inverting and Inverting Input Pin (IN+, IN−)

NCD57080x has two possible input modes to control IGBT. Both inputs have defined minimum input pulse width to filter occasional glitches.

- Non−inverting input IN+ controls the driver output while inverting input IN− is set to LOW
- Inverting input IN− controls the driver output while non−inverting input IN+ is set to HIGH

WARNING: When the application uses an independent or separate power supply for the control unit and the input side of the driver, all inputs should be protected by a serial resistor (In case of a power failure of the driver, the driver may be damaged due to overloading of the input protection circuits)

Power Supply (V_{DD1}, V_{DD2}, V_{EE2})

NCD57080A and NCD57080C are designed to support unipolar power supply.

NCD57080B is designed to support bipolar power supply. For reliable high output current delivery suitable external power capacitors are required. Parallel combination of 100 nF + 4.7 μF ceramic capacitors is optimal for a wide range of applications using IGBT. For reliable driving of IGBT modules (containing several parallel IGBTs) a higher capacity is required (typically 100 nF + 10 μF). Capacitors should be as close as possible to the driver's power pins.

- In bipolar power supply the driver is typically supplied with a positive voltage of 15 V at V_{DD2} and negative voltage −5 V at V_{EE2} (Figure 27). Negative power supply prevents a dynamic turn on through the internal IGBT input capacitance
- In Unipolar power supply the driver is typically supplied with a positive voltage of 15 V at V_{DD2}. Dynamic turn on through the internal IGBT input capacitance could be prevented by Active Miler Clamp function (NCD57080A). CLAMP output should be directly connected to IGBT gate (Figure 25)

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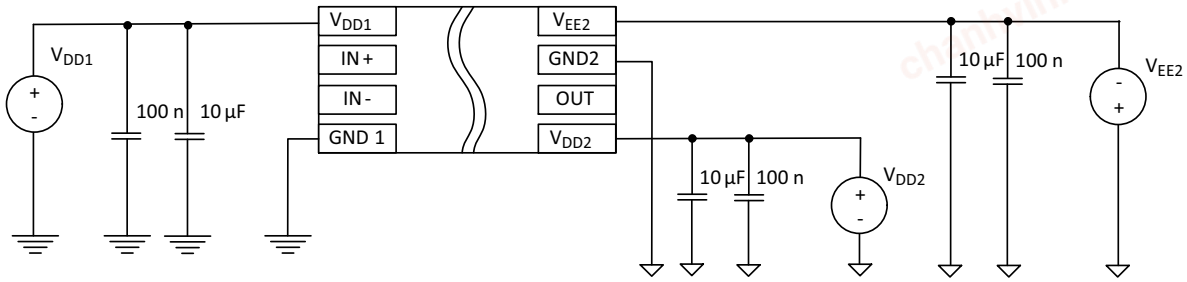


Figure 27. Bipolar Power Supply NCD57080B

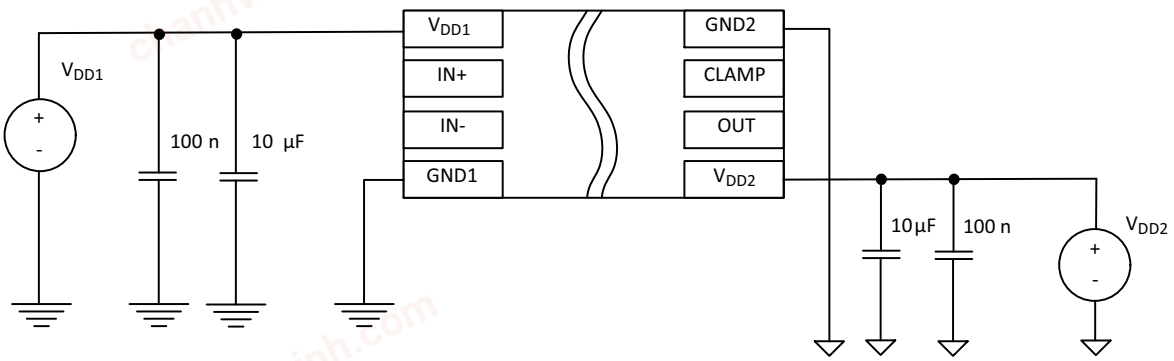


Figure 28. Unipolar Power Supply NCD57080A

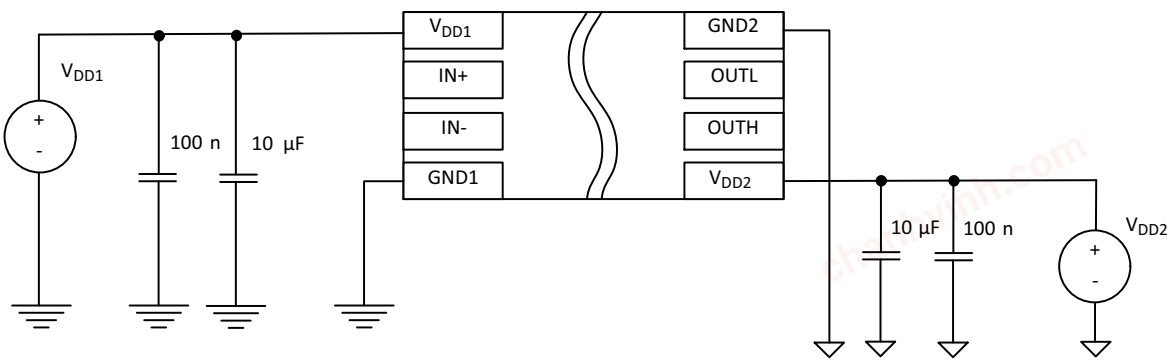


Figure 29. Suggested Bypassing Scheme for NCD57080x

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Common Mode Transient Immunity (CMTI)

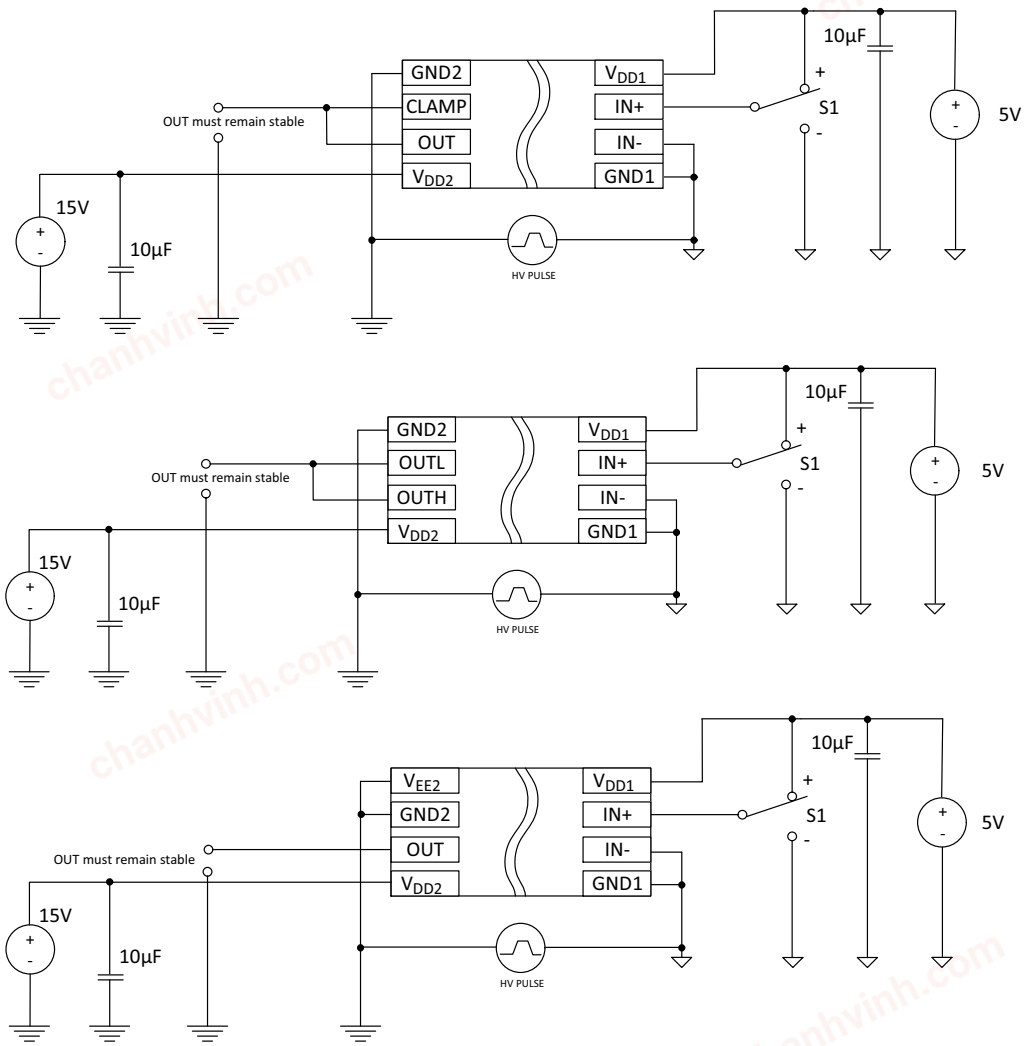


Figure 30. Common−Mode Transient Immunity Test Circuit

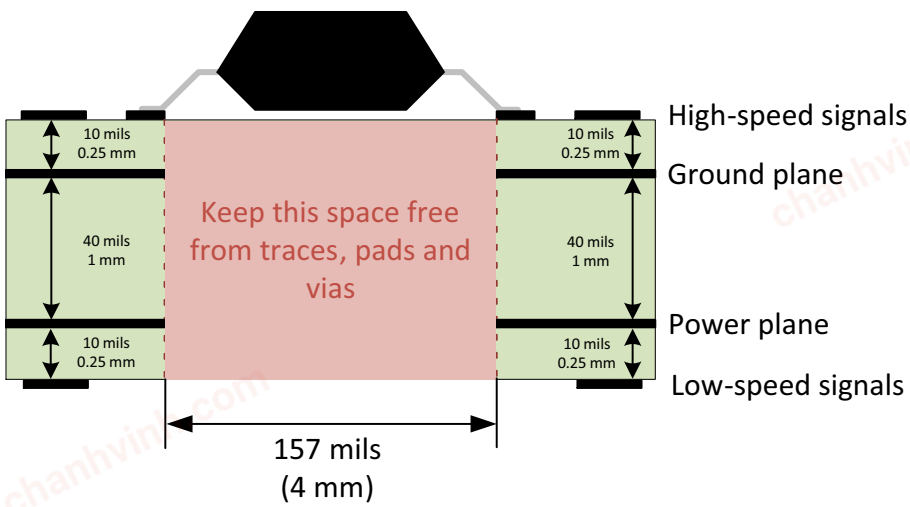


Figure 31. Recommended Layer Stack

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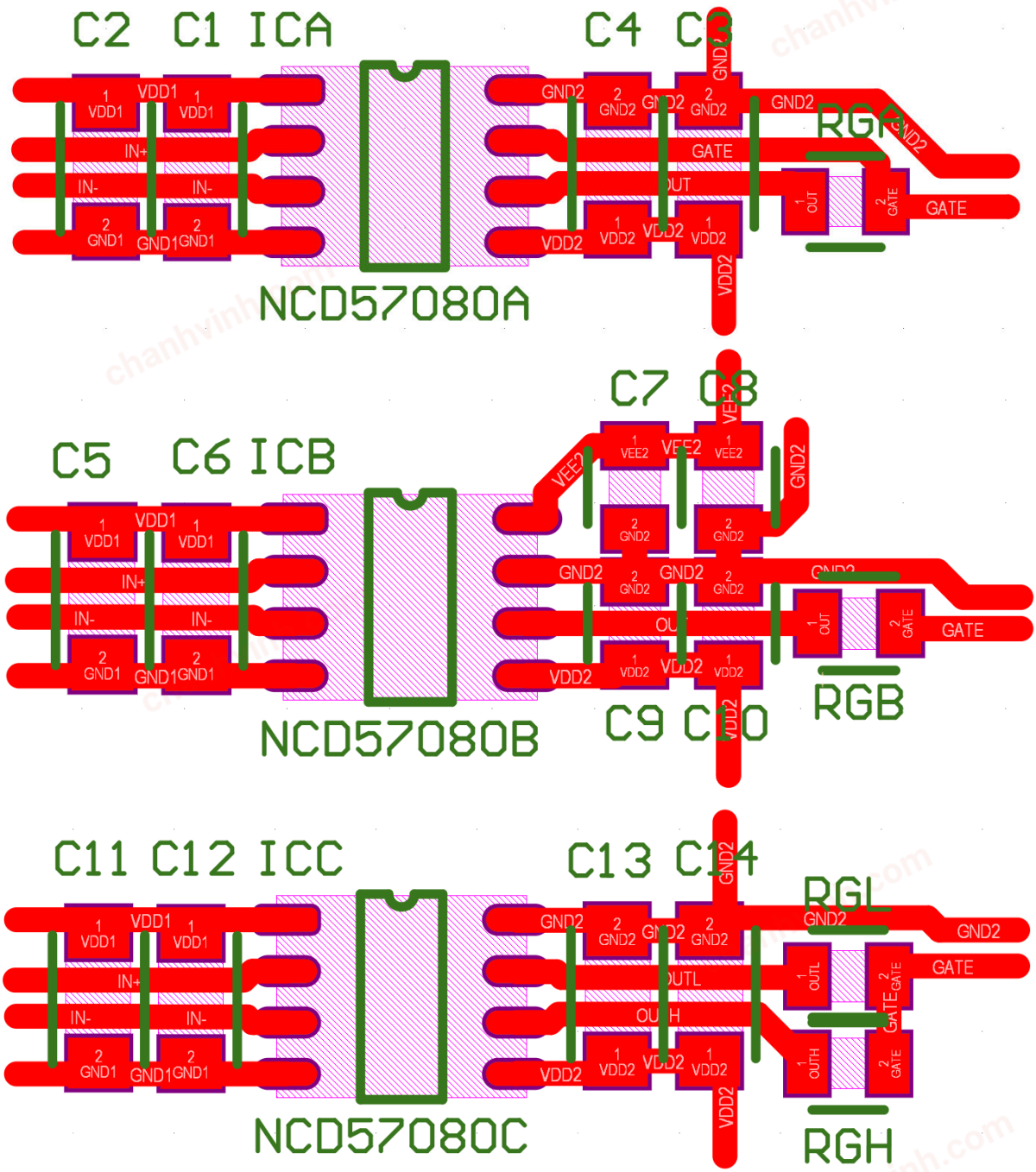


Figure 32. Recommended Layout

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ORDERING INFORMATION

Device	Package	Shipping†
NCD57080ADR2G	SOIC−8 Narrow Body, (Pb−Free)	2500 / Tape & Reel
NCD57080BDR2G (In Development)	SOIC−8 Narrow Body, (Pb−Free)	2500 / Tape & Reel
NCD57080CDR2G	SOIC−8 Narrow Body, (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

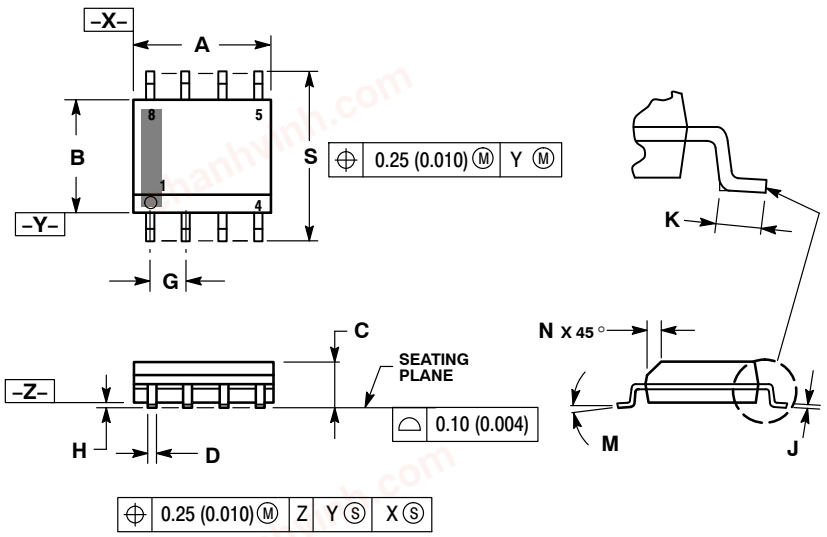
ON Semiconductor®



SCALE 1:1

SOIC–8 NB
CASE 751–07
ISSUE AK

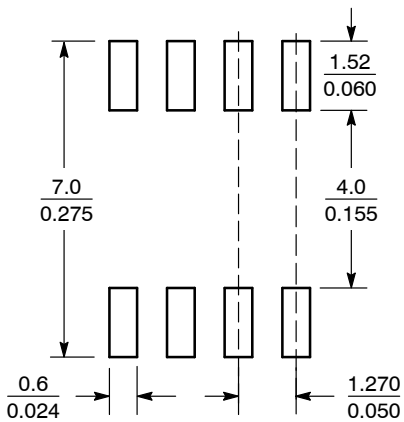
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751–01 THRU 751–06 ARE OBSOLETE. NEW STANDARD IS 751–07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

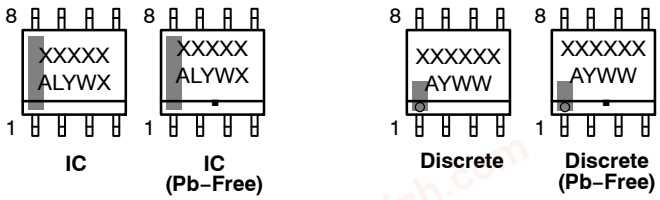
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb–Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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