chanhvinh.com

# NCD57001

# Isolated High Current IGBT Gate Driver

NCD57001 is a high−current single channel IGBT driver with internal galvanic isolation, designed for high system efficiency and reliability in high power applications. Its features include complementary inputs, open drain FAULT and Ready outputs, active Miller clamp, accurate UVLOs, DESAT protection, and soft turn−off at DESAT. NCD57001 accommodates both 5 V and 3.3 V signals on the input side and wide bias voltage range on the driver side including negative voltage capability. NCD57001 provides > 5 kVrms (UL1577 rating) galvanic isolation and > 1200 $V_{iorm}$ (working voltage) capabilities. NCD57001 is available in the wide−body SOIC−16 package with guaranteed 8 mm creepage distance between input and output to fulfill reinforced safety insulation requirements.

### Features

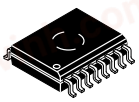
- High Current Output (+4/−6 A) at IGBT Miller Plateau Voltages
- Low Output Impedance for Enhanced IGBT Driving
- Short Propagation Delays with Accurate Matching
- Active Miller Clamp to Prevent Spurious Gate Turn−on
- DESAT Protection with Programmable Delay
- Negative Voltage (Down to −9 V) Capability for DESAT
- Soft Turn Off During IGBT Short Circuit
- IGBT Gate Clamping During Short Circuit
- IGBT Gate Active Pull Down
- Tight UVLO Thresholds for Bias Flexibility
- Wide Bias Voltage Range including Negative VEE2
- 3.3 V to 5 V Input Supply Voltage
- Designed for AEC−Q100 Certification
- 5000 V Galvanic Isolation (to meet UL1577 Requirements)
- 1200 V Working Voltage (per VDE0884−10 Requirements)
- High Transient Immunity
- High Electromagnetic Immunity
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

### Typical Applications

- Solar Inverters
- Motor Control
- Uninterruptible Power Supplies (UPS)
- Industrial Power Supplies
- Welding

**ON Semiconductor®**

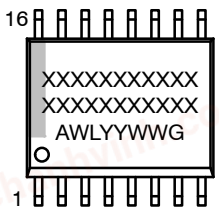
www.onsemi.com



1

**SOIC−16 WB**
**CASE 751G−03**

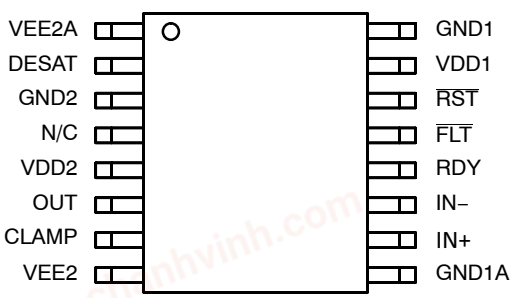
### MARKING DIAGRAM




| | |
|---|---|
| XXXXX | = Specific Device Code |
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

### PIN ASSIGNMENT




### ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

© Semiconductor Components Industries, LLC, 2018

chanhvinh.com



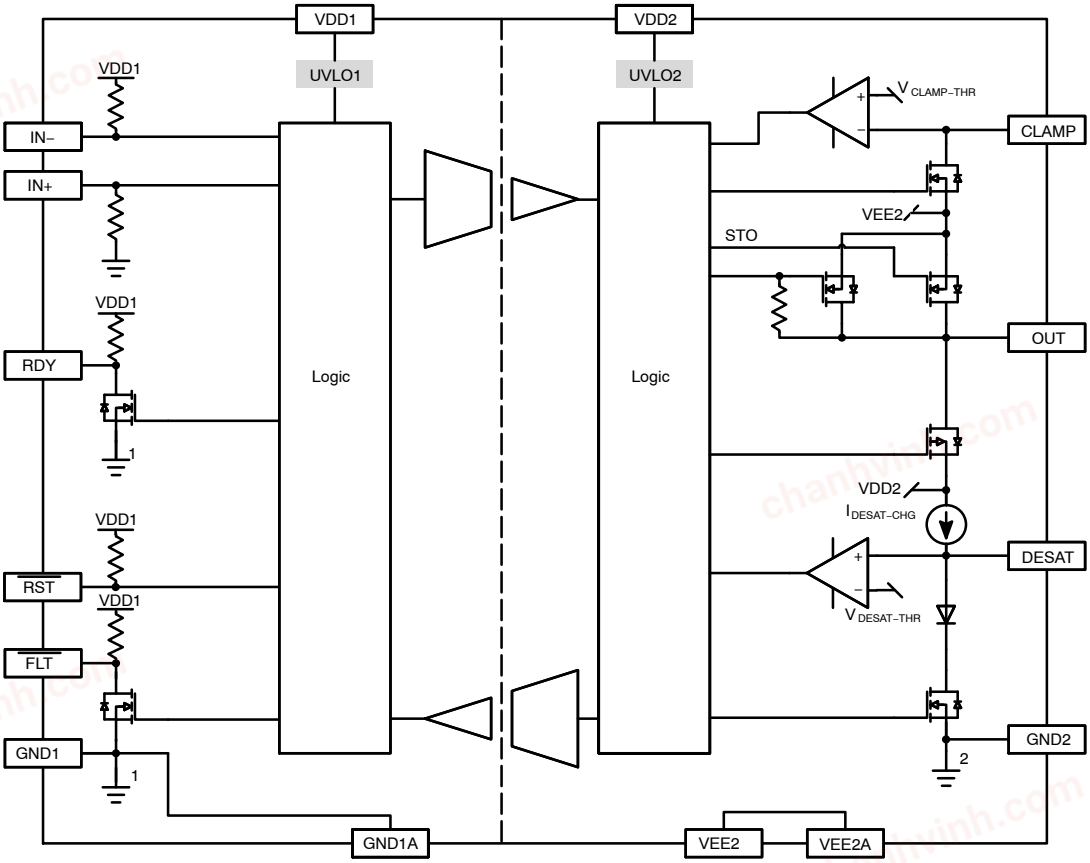



**Figure 1. Simplified Block Diagram**

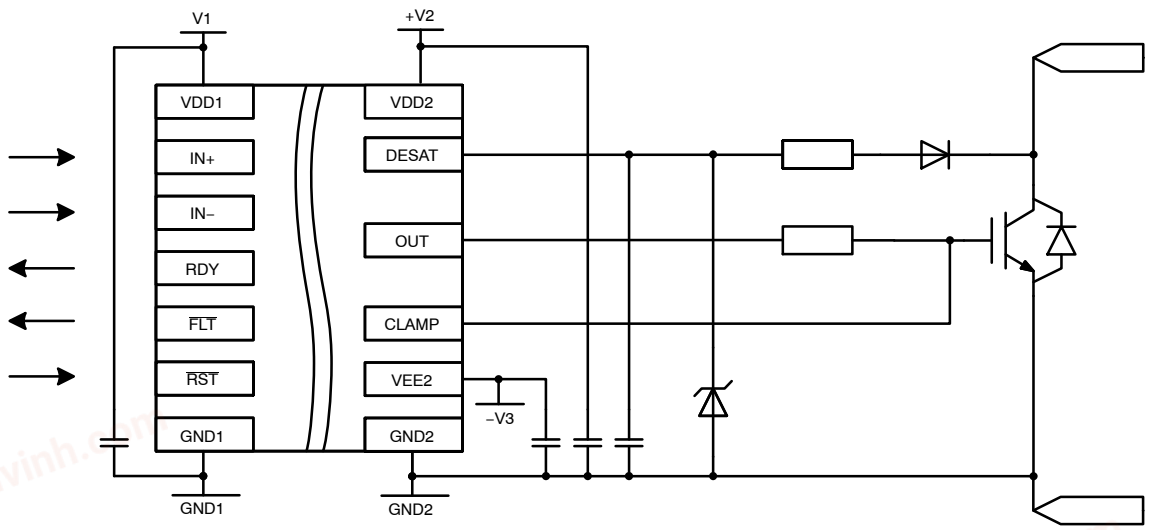



**Figure 2. Simplified Application Schematics**

chanhvinh.com



## PIN DESCRIPTION

| Pin Name | No. | I/O | Description |
|---|---|---|---|
| $V_{EE2A}$ | 1 | Power | Output side negative power supply. A good quality bypassing capacitor is required from these pins to GND2 and should be placed close to the pins for best results. Connect it to GND2 for unipolar supply application. |
| $V_{EE2}$ | 8 | | |
| DESAT | 2 | I/O | Input for detecting the desaturation of IGBT due to a short circuit condition. An internal constant current source $I_{DESAT-CHG}$ charging an external capacitor connected to this pin allows a programmable blanking delay every ON cycle before DESAT fault is processed, thus preventing false triggering. When the DESAT voltage goes up and reaches $V_{DESAT-THR}$, the output is driven low. Further, the /FLT output is activated, please refer to Figure 5 on page 9.<br><br>A 5 μs mute time apply to IN+ and IN− once DESAT occurs. |
| GND2 | 3 | Power | Output side gate drive reference connecting to IGBT emitter or FET source. |
| N/C | 4 | – | Not connected. |
| $V_{DD2}$ | 5 | Power | Output side positive power supply. The operating range for this pin is from UVLO2 to its maximum allowed value. A good quality bypassing capacitor is required from this pin to GND2 and should be placed close to the pins for best results. |
| OUT | 6 | O | Driver output that provides the appropriate drive voltage and source/sink current to the IGBT/FET gate. OUT is actively pulled low during start−up and under Fault conditions. |
| CLAMP | 7 | I/O | Provides clamping for the IGBT/FET gate during the off period to protect it from parasitic turn−on. Its internal N FET is turned on when the voltage of this pin falls below $V_{EE2}$ + $V_{CLAMP-THR}$. It is to be tied directly to IGBT/FET gate with minimum trace length for best results. |
| GND1 | 9 | Power | Input side ground reference. |
| | 16 | | |
| IN+ | 10 | I | Non inverted gate driver input. It is internally clamped to $V_{DD1}$ and has a pull−down resistor of 50 kΩ to ensure that output is low in the absence of an input signal. A minimum positive going pulse−width is required at IN+ before OUT responds. |
| IN− | 11 | I | Inverted gate driver input. It is internally clamped to $V_{DD1}$ and has a pull−up resistor of 50 kΩ to ensure that output is low in the absence of an input signal. A minimum negative going pulse−width is required at IN− before OUT responds. |
| RDY | 12 | O | Power good indication output, active high when $V_{DD2}$ is good. There is an internal 50 kΩ pull−up resistor connected to this pin. Multiple of them from different drivers can be ”OR”ed together. If a low RDY event is triggered by UVLO2, the maximum low duration for RDY is 200 ns. OUT remains low when RDY is low. Short time delay may apply. See Figure 4 on page 8 for details. |
| /FLT | 13 | O | Fault output (active low) that allows communication to the main controller that the driver has encountered a desaturation condition and has deactivated the output. |
| /RST | 14 | I | Reset input with an internal 50 kΩ pull−up resistor, active low to reset fault latch. |
| $V_{DD1}$ | 15 | Power | Input side power supply (3.3 V to 5 V). |

chanhvinh.com



**ABSOLUTE MAXIMUM RATINGS** (Over operating free−air temperature range unless otherwise noted) (Note 1)

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $V_{DD1}$−GND1 | Supply voltage, input side | −0.3 | 6 | V |
| $V_{DD2}$−GND2 | Positive Power Supply, output side | −0.3 | 25 | V |
| $V_{EE2}$−GND2 | Negative Power Supply, output side | −10 | 0.3 | V |
| $V_{DD2}$−$V_{EE2}$ ($V_{MAX2}$) | Differential Power Supply, output side | 0 | 25 | V |
| $V_{OUT}$ | Gate−driver output voltage | $V_{EE2}$ − 0.3 | $V_{DD2}$ + 0.3 | V |
| $I_{PK-SRC}$ | Gate−driver output sourcing current (maximum pulse width = 10 μs, maximum duty cycle = 0.2%, $V_{MAX2}$ = 20 V) | − | 7.8 | A |
| $I_{PK-SNK}$ | Gate−driver output sinking current (maximum pulse width = 10 μs, maximum duty cycle = 0.2%, $V_{MAX2}$ = 20 V) | − | 7.1 | A |
| $I_{PK-CLAMP}$ | Clamp sinking current (maximum pulse width = 10 μs, maximum duty cycle = 0.2%, $V_{CLAMP}$ = 3 V) | − | 2.5 | A |
| $t_{CLP}$ | Maximum Short Circuit Clamping Time ($I_{OUT_CLAMP}$ = 500 mA) | − | 10 | μs |
| $V_{LIM}$−GND1 | Voltage at IN+, IN−, /RST, /FLT, RDY | −0.3 | $V_{DD1}$ + 0.3 | V |
| $I_{LIM}$−GND1 | Output current of /FLT, RDY | − | 10 | mA |
| $V_{DESAT}$−GND2 | Desat Voltage (Note 2) | −9 | $V_{DD2}$ + 0.3 | V |
| $V_{CLAMP}$−GND2 | Clamp Voltage | $V_{EE2}$ − 0.3 | $V_{DD2}$ + 0.3 | V |
| $P_D$ | Power Dissipation (Note 3) | − | 1400 | mW |
| $V_{ISO}$ | Input to Output Isolation Voltage | −1200 | 1200 | V |
| $T_{J(max)}$ | Maximum Junction Temperature | −40 | 150 | °C |
| $T_{STG}$ | Storage Temperature Range | −65 | 150 | °C |
| $ESD_{HBM}$ | ESD Capability, Human Body Model (Note 4) | − | ±2 | kV |
| $ESD_{CDM}$ | ESD Capability, Charged Device Model (Note 4) | − | ±2 | kV |
| MSL | Moisture Sensitivity Level | − | 2 | − |
| $T_{SLD}$ | Lead Temperature Soldering Reflow, Pb−Free Versions (Note 5) | − | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. The minimum value is verified by characterization with a single pulse of 100 mA for 100 μs.
3. The value is estimated for ambient temperature 25°C and junction temperature 150°C, 650 $mm^2$, 1 oz copper, 2 surface layers and 2 internal power plane layers. Power dissipation is affected by the PCB design and ambient temperature.
4. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Charged Device Model tested per AEC−Q100−011 (EIA/JESD22−C101)
   Latchup Current Maximum Rating: ≤100 mA per JEDEC standard: JESD78, 25°C
5. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**THERMAL CHARACTERISTICS**

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction−to−Air | 100 $mm^2$, 1 oz Copper, 1 Surface Layer | 150 | °C/W |
| | | 650 $mm^2$, 1 oz Copper, 2 Surface Layers and 2 Internal Power Plane Layers | 84 | |

chanhvinh.com



**OPERATING RANGES** (Note 6)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD1}$–GND1 | Supply voltage, input side | UVLO1 | 5.5 | V |
| $V_{DD2}$–GND2 | Positive Power Supply, output side | UVLO2 | 24 | V |
| $V_{EE2}$–GND2 | Negative Power Supply, output side | −10 | 0 | V |
| $V_{DD2}$–$V_{EE2}$ ($V_{MAX2}$) | Differential Power Supply, output side | 0 | 24 | V |
| $V_{IL}$ | Low level input voltage at IN+, IN−, /RST | 0 | 0.3 X $V_{DD1}$ | V |
| $V_{IH}$ | High level input voltage at IN+, IN−, /RST | 0.7 X $V_{DD1}$ | $V_{DD1}$ | V |
| $\|dV_{ISO}/dt\|$ | Common Mode Transient Immunity (1500 V) | 100 | – | kV/μs |
| $T_A$ | Ambient Temperature | −40 | 125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

**ELECTRICAL CHARACTERISTICS** ($V_{DD1}$ = 5 V, $V_{DD2}$ = 15 V, $V_{EE2}$ = −8 V. For typical values $T_A$ = 25°C, for min/max values, $T_A$ is the operating ambient temperature range that applies, unless otherwise noted)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VOLTAGE SUPPLY** | | | | | | |
| $V_{UVLO1-OUT-ON}$ | UVLO1 Output Enabled | | – | – | 3 | V |
| $V_{UVLO1-OUT-OFF}$ | UVLO1 Output Disabled | | 2.4 | – | – | V |
| $V_{UVLO1-HYST}$ | UVLO1 Hysteresis | | 0.125 | – | – | V |
| $V_{UVLO2-OUT-ON}$ | UVLO2 Output Enabled | | 13.2 | 13.5 | 13.8 | V |
| $V_{UVLO2-OUT-OFF}$ | UVLO2 Output Disabled | | 12.2 | 12.5 | 12.8 | V |
| $V_{UVLO2-HYST}$ | UVLO2 Hysteresis | | – | 1 | | V |
| $I_{DD1-0}$ | Input Supply Quiescent Current Output Low | IN+ = Low, IN− = Low<br>RDY = High, /FLT = High | – | 1 | 2 | mA |
| $I_{DD1-100}$ | Input Supply Quiescent Current Output High | IN+ = High, IN− = Low<br>RDY = High, /FLT = High | – | 4.8 | 6 | mA |
| $I_{DD2-0}$ | Output Positive Supply Quiescent Current, Output Low | IN+ = Low, IN− = Low<br>RDY = High, /FLT = High, no load | – | 3.3 | 4 | mA |
| $I_{DD2-100}$ | Output Positive Supply Quiescent Current, Output High | IN+ = High, IN− = Low<br>RDY = High, /FLT = High, no load | – | 3.6 | 6 | mA |
| $I_{EE2-0}$ | Output Negative Supply Quiescent Current, Output Low | IN+ = High, IN− = Low, no load | – | 0.4 | 2 | mA |
| $I_{EE2-100}$ | Output Negative Supply Quiescent Current, Output High | IN+ = High, IN− = Low, no load | – | 0.2 | 2 | mA |
| **LOGIC INPUT AND OUTPUT** | | | | | | |
| $V_{IL}$ | IN+, IN−, /RST Low Input Voltage | | – | – | 0.3 x $V_{DD1}$ | V |
| $V_{IH}$ | IN+, IN−, /RST High Input Voltage | | 0.7 x $V_{DD1}$ | – | – | V |
| $V_{IN-HYST}$ | Input Hysteresis Voltage | | – | 0.15 x $V_{DD1}$ | – | V |
| $I_{IN-L}$, $I_{RST-L}$ | IN−, /RST Input Current (50 kΩ pull−up resistor) | $V_{IN-}$/$V_{RST}$ = 0 V | – | −100 | – | μA |
| $I_{IN+H}$ | IN+ Input Current (50 kΩ pull−down resistor) | $V_{IN+}$ = 5 V | – | 100 | – | μA |

chanhvinh.com



**ELECTRICAL CHARACTERISTICS** ($V_{DD1}$ = 5 V, $V_{DD2}$ = 15 V, $V_{EE2}$ = −8 V. For typical values $T_A$ = 25°C, for min/max values, $T_A$ is the operating ambient temperature range that applies, unless otherwise noted) (continued)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **LOGIC INPUT AND OUTPUT** | | | | | | |
| $I_{RDY-L}$, $I_{FLT-L}$ | RDY, /FLT Pull−up Current (50 kΩ pull−up resistor) | $V_{RDY}/V_{FLT}$ = Low | – | 100 | – | μA |
| $V_{RDY-L}$, $V_{FLT-L}$ | RDY, /FLT Low Level Output Voltage | $I_{RDY}/I_{FLT}$ = 5 mA | – | – | 0.3 | V |
| $t_{MIN1}$ | Input Pulse Width of IN+, IN− for No Response at Output | | – | – | 10 | ns |
| $t_{MIN2}$ | Input Pulse Width of IN+, IN− for Guaranteed Response at Output | | 40 | – | – | ns |
| $t_{RST-MIN}$ | Pulse Width of /RST for Resetting /FLT | | 800 | – | – | ns |
| **DRIVER OUTPUT** | | | | | | |
| $V_{OUTL1}$ | Output Low State ($V_{OUT}$ − $V_{EE2}$) | $I_{SINK}$ = 200 mA | – | 0.1 | 0.2 | V |
| $V_{OUTL3}$ | | $I_{SINK}$ = 1.0 A, $T_A$ = 25°C | – | 0.5 | 0.8 | |
| $V_{OUTH1}$ | Output High State ($V_{DD2}$ − $V_{OUT}$) | $I_{SRC}$ = 200 mA | – | 0.3 | 0.5 | V |
| $V_{OUTH3}$ | | $I_{SRC}$ = 1.0 A, $T_A$ = 25°C | – | 0.8 | 1 | |
| $I_{PK-SNK1}$ | Peak Driver Current, Sink (Note 7) | $V_{OUT}$ = 7.9 V | – | 7.1 | – | A |
| $I_{PK-SRC1}$ | Peak Driver Current, Source (Note 7) | $V_{OUT}$ = −5 V | – | 7.8 | – | A |
| **MILLER CLAMP** | | | | | | |
| $V_{CLAMP}$ | Clamp Voltage ($V_{CLAMP}$ − $V_{EE2}$) | $I_{CLAMP}$ = 2.5 A, $T_A$ = 25°C | – | 1.3 | 1.7 | V |
| | | $I_{CLAMP}$ = 2.5 A, $T_A$ = −40°C to 125°C | – | – | 3 | |
| $V_{CLAMP-THR}$ | Clamp Activation Threshold ($V_{CLAMP}$ − $V_{EE2}$) | | 1.5 | 2 | 2.5 | V |
| **IGBT SHORT CIRCUIT CLAMPING** | | | | | | |
| $V_{CLAMP-OUT}$ | Clamping Voltage, ($V_{OUT}$ − $V_{DD2}$) | IN+ = Low, IN− = High, $I_{OUT}$ = 500 mA (pulse test, $t_{CLPmax}$ = 10 μs) | – | 0.9 | 1.1 | V |
| $V_{CLAMP-CLAMP}$ | Clamping Voltage, Clamp ($V_{CLAMP}$ − $V_{DD2}$) | IN+ = High, IN− = Low, $I_{CLAMP-CLAMP}$ = 500 mA (pulse test, $t_{CLPmax}$ = 10 μs) | – | 1.4 | 1.6 | V |
| **DESAT PROTECTION** | | | | | | |
| $V_{DESAT-THR}$ | DESAT Threshold Voltage | | 8.5 | 9 | 9.5 | V |
| $V_{DESAT-NEG}$ | DESAT Negative Voltage | $I_{DESAT}$ = 1.5 mA | – | −8 | – | V |
| $I_{DESAT-CHG}$ | Blanking Charge Current | $V_{DESAT}$ = 7 V | 0.45 | 0.5 | 0.6 | mA |
| $I_{DESAT-DIS}$ | Blanking Discharge Current | | – | 50 | – | mA |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $t_{PD-ON}$ | IN+, IN− to Output High Propagation Delay | $C_{LOAD}$ = 10 nF $V_{IH}$ to 10% of output change for PW > 150 ns. OUT and CLAMP pins are connected together | 40 | 60 | 90 | ns |
| $t_{PD-OFF}$ | IN+, IN− to Output Low Propagation Delay | $C_{LOAD}$ = 10 nF $V_{IL}$ to 90% of output change for PW > 150 ns. OUT and CLAMP pins are connected together | 40 | 66 | 90 | ns |
| $t_{DISTORT}$ | Propagation Delay Distortion (= $t_{PD-ON}$ − $t_{PD-OFF}$) | $T_A$ = 25°C, PW > 150 ns | −15 | −6 | 15 | ns |
| | | $T_A$ = −40°C to 125°C, PW > 150 ns | −25 | – | 25 | |
| $t_{DISTORT_TOT}$ | Prop Delay Distortion between Parts | PW > 150 ns | −30 | 0 | 30 | ns |

chanhvinh.com



**ELECTRICAL CHARACTERISTICS** ($V_{DD1}$ = 5 V, $V_{DD2}$ = 15 V, $V_{EE2}$ = −8 V. For typical values $T_A$ = 25°C, for min/max values, $T_A$ is the operating ambient temperature range that applies, unless otherwise noted) (continued)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $t_{RISE}$ | Rise Time (see Fig. 3) (Note 7) | $C_{LOAD}$ = 1 nF, 10% to 90% of Output Change | – | 10 | – | ns |
| $t_{FALL}$ | Fall Time (see Fig. 3) (Note 7) | $C_{LOAD}$ = 1 nF, 90% to 10% of Output Change | – | 15 | – | ns |
| $t_{LEB}$ | DESAT Leading Edge Blanking Time (See Fig. 5) | | – | 450 | – | ns |
| $t_{FILTER}$ | DESAT Threshold Filtering Time (see Fig. 5) | | – | 320 | – | ns |
| $t_{STO}$ | Soft Turn Off Time (see Fig. 5) | $C_{LOAD}$ = 10 nF, $R_G$ = 10 Ω. $V_{EE2}$ = 0 V | – | 1.8 | – | μs |
| | | $C_{LOAD}$ = 10 nF, $R_G$ = 10 Ω | – | 2.6 | – | |
| $t_{FLT}$ | Delay after $t_{FILTER}$ to /FLT | | – | 450 | – | ns |
| $t_{RST}$ | /RST Rise to /FLT Rise Delay | | – | 23 | – | ns |
| $t_{RDY1O}$ | RDY High to Output High Delays (see Fig. 4) | | – | 55 | – | ns |
| $t_{RDY2O}$ | | | | | | |
| $t_{RDY1F}$ | $V_{UVLO2-OUT-OFF}$ to RDY Low Delays (see Fig. 4) | | – | 8 | – | μs |
| $t_{RDY2F}$ | | | | | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Values based on design and/or characterization.

## ORDERING INFORMATION

| Device | Package Type | Shipping† |
|---|---|---|
| NCD57001DWR2G | SOIC−16 Wide Body (Pb−Free) | 1,000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

chanhvinh.com



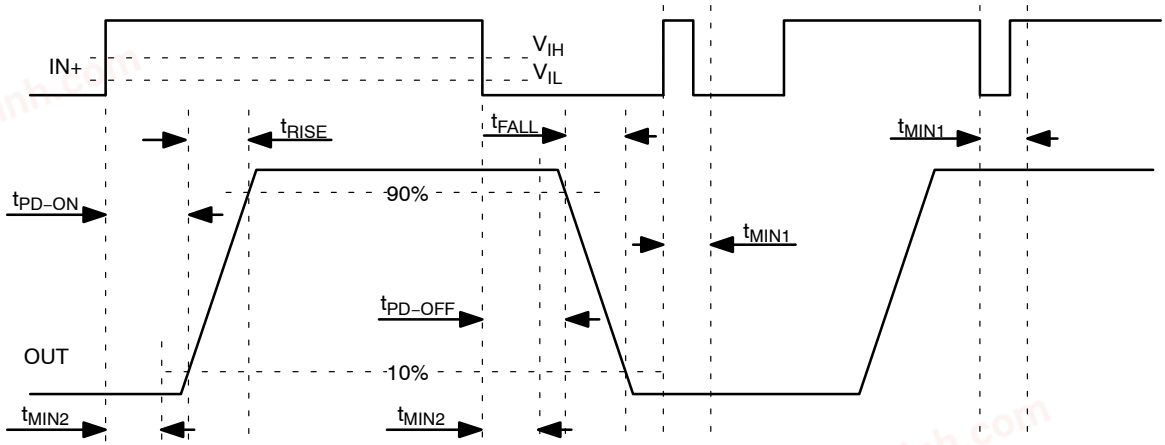



**Figure 3. Propagation Delay, Rise and Fall Time**

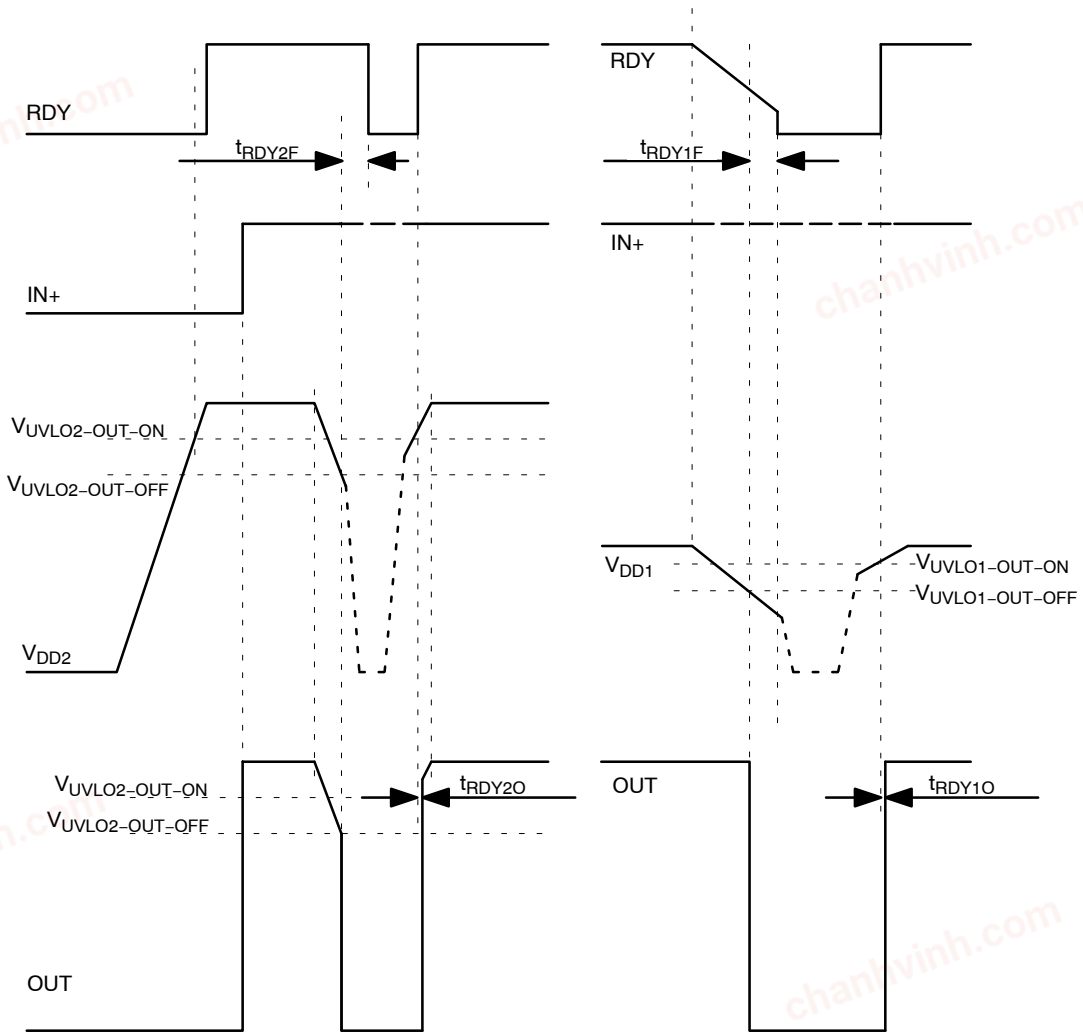



**Figure 4. UVLO Waveform**

chanhvinh.com



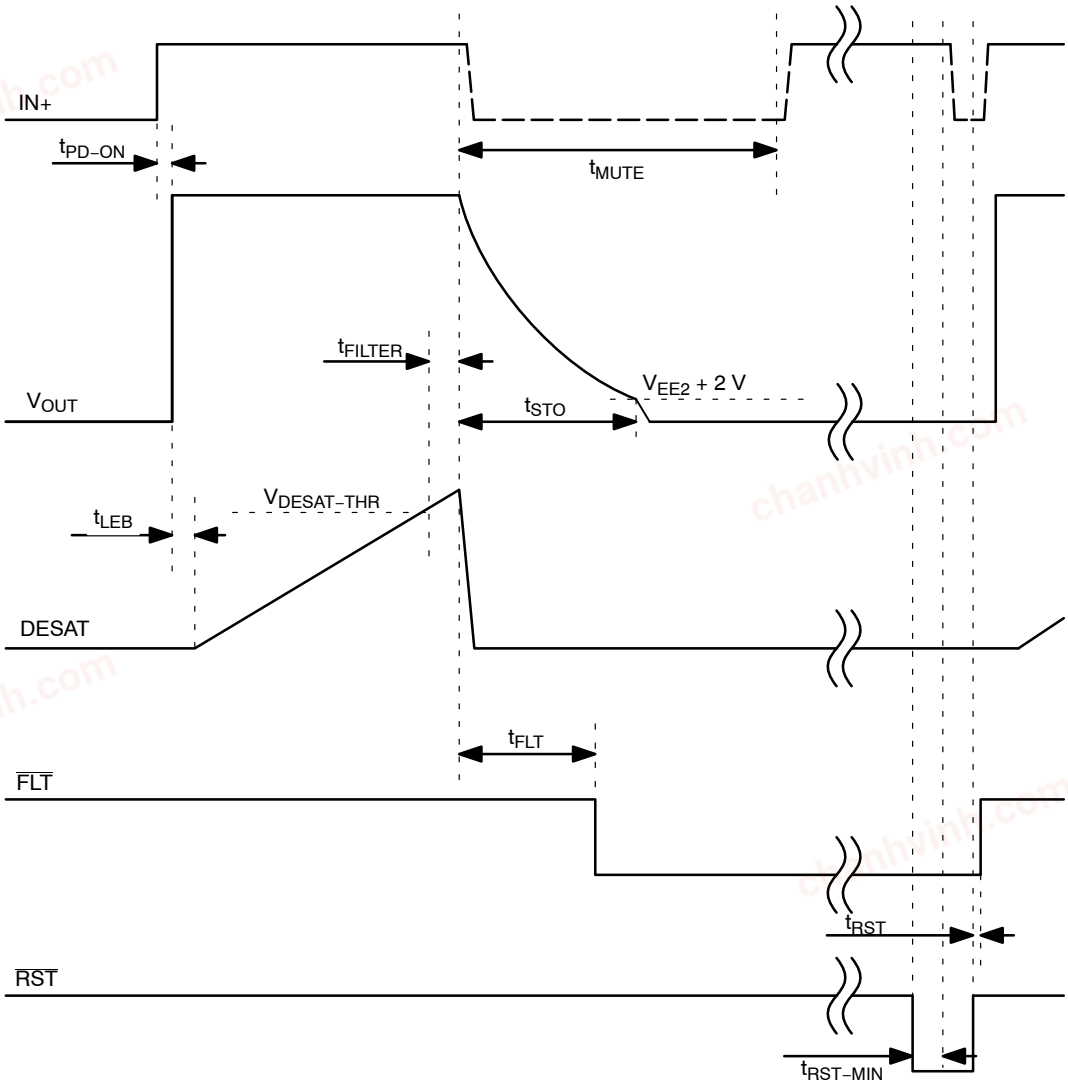



**Figure 5. DESAT Response Waveform**

chanhvinh.com



## TYPICAL CHARACTERISTICS

(Conditions for the following figures are the same as stated for ELECTRICAL CHARACTERISTICS Table unless otherwise noted. Typical and/or average values are used.)

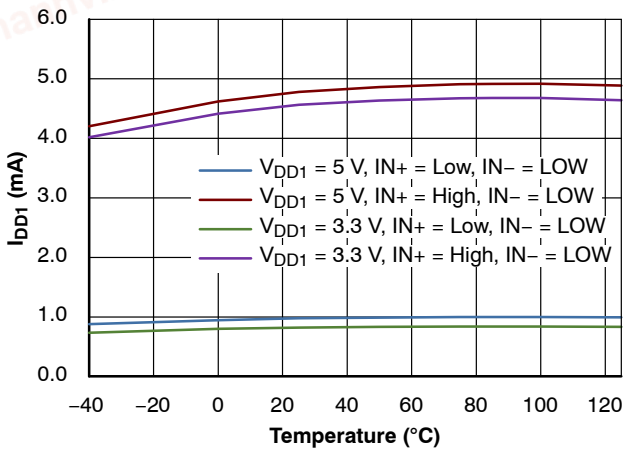



**Figure 6. $V_{DD1}$ Supply Current**

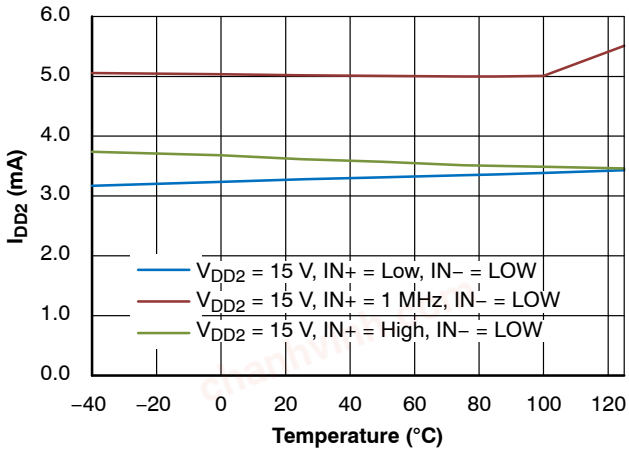



**Figure 7. $V_{DD2}$ Supply Current**

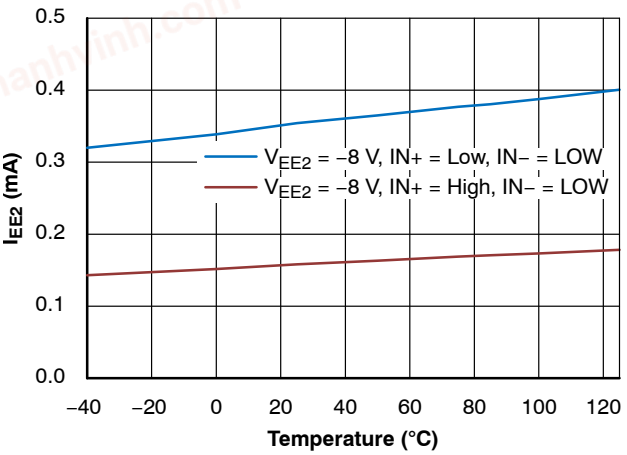



**Figure 8. $V_{EE2}$ Supply Current**

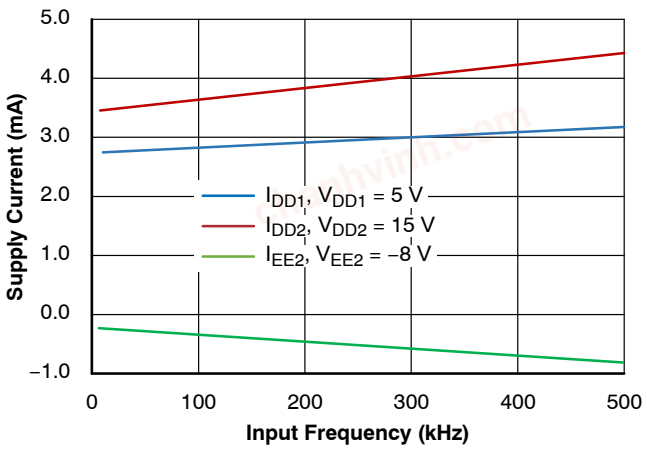



**Figure 9. Supply Current vs Frequency**

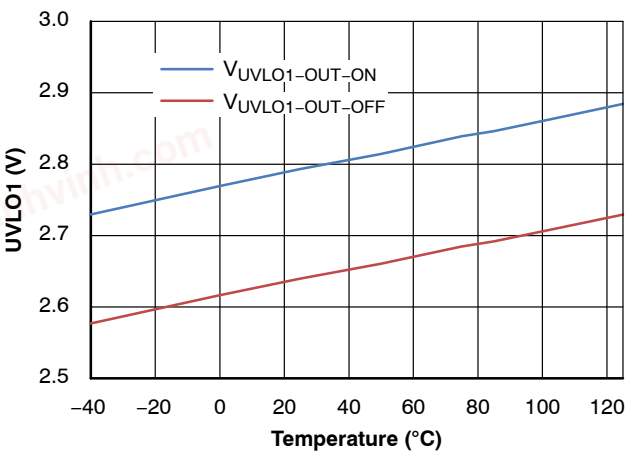



**Figure 10. UVLO1 Threshold Voltage**

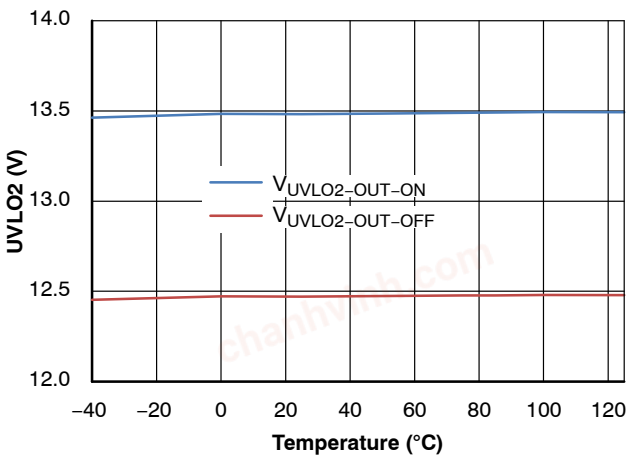



**Figure 11. UVLO2 Threshold Voltage**

chanhvinh.com



## TYPICAL CHARACTERISTICS

(Conditions for the following figures are the same as stated for ELECTRICAL CHARACTERISTICS Table unless otherwise noted. Typical and/or average values are used.) (continued)

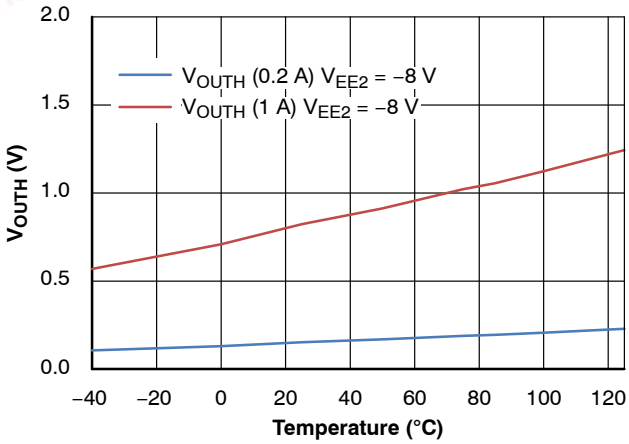



**Figure 12. Output Voltage Drop, Sourcing**

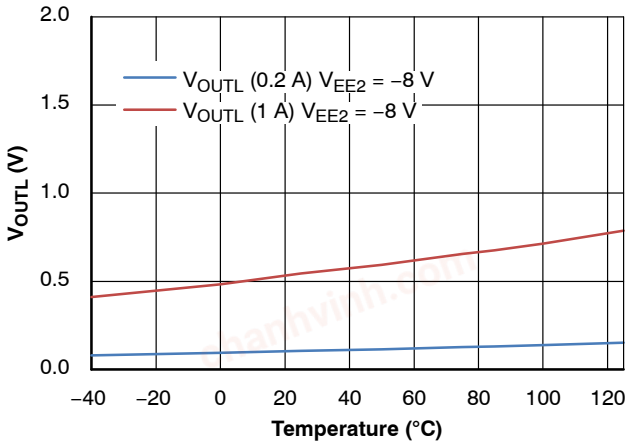



**Figure 13. Output Voltage Drop, Sinking**

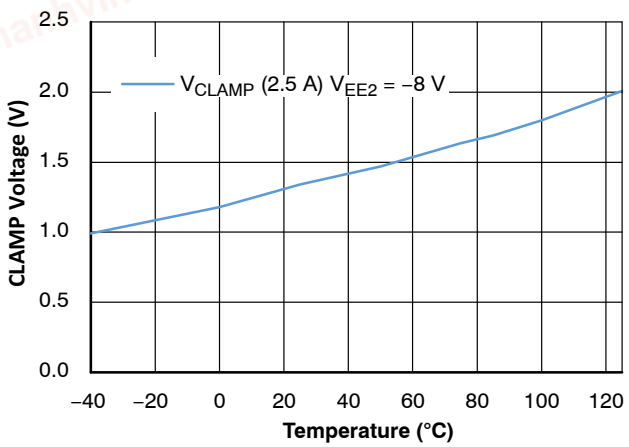



**Figure 14. CLAMP Voltage Drop**

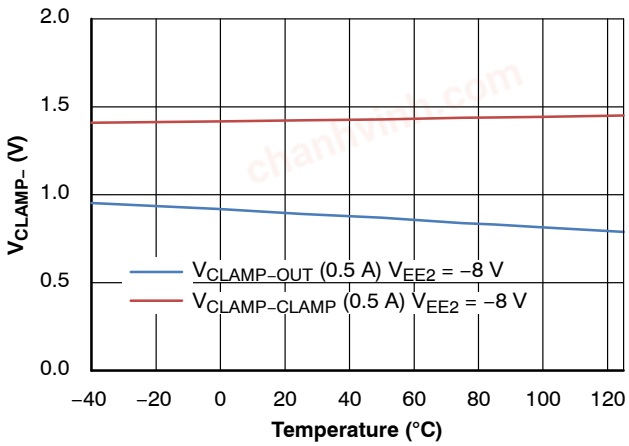



**Figure 15. IGBT Short Circuit Clamp Voltage Drop**

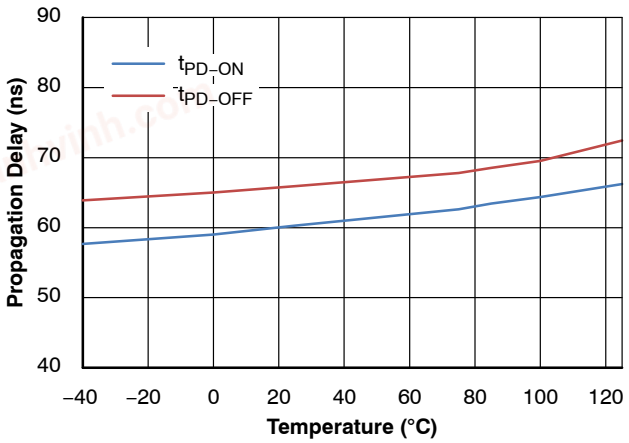



**Figure 16. Propagation Delay**

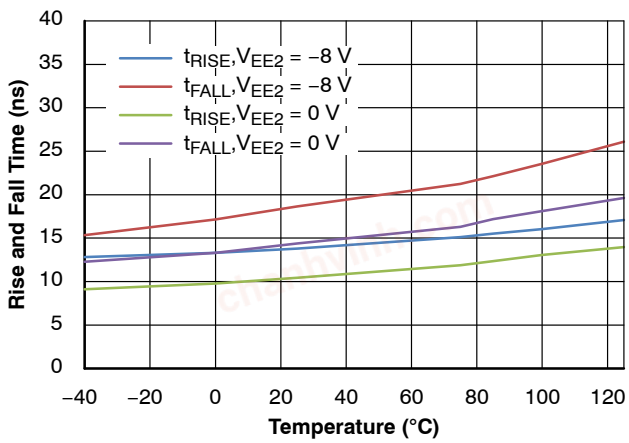



**Figure 17. Rise and Fall Time**

chanhvinh.com



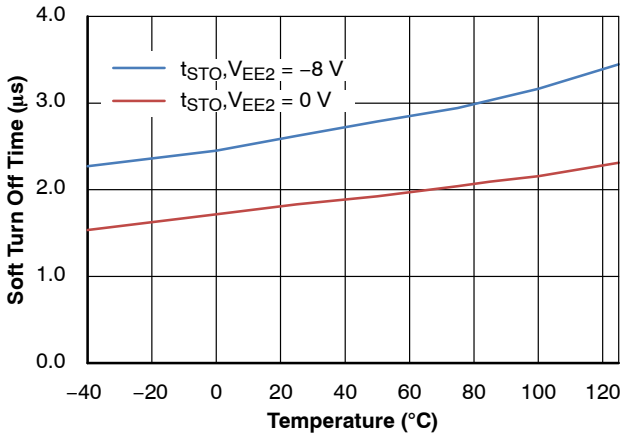


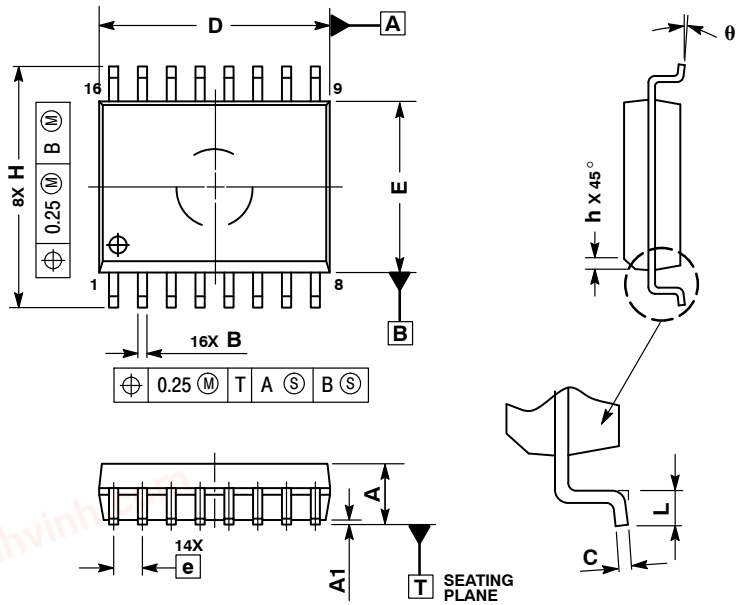

**Figure 18. Soft Turn Off Time**

chanhvinh.com

# NCD57001

## PACKAGE DIMENSIONS

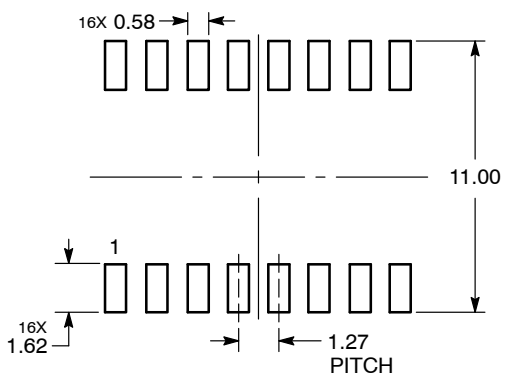
**SOIC−16 WB**
CASE 751G−03
ISSUE D




NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 10.15 | 10.45 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| q | 0 ° | 7 ° |

## SOLDERING FOOTPRINT




DIMENSIONS: MILLIMETERS

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT**:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
**Phone**: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
**Fax**: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
**Email**: orderlit@onsemi.com

**N. American Technical Support**: 800−282−9855 Toll Free USA/Canada
**Europe, Middle East and Africa Technical Support:**
Phone: 421 33 790 2910

**ON Semiconductor Website**: **www.onsemi.com**

**Order Literature**: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative