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Product Overview

MC74HC125A: Quad Non-inverting Buffer, 3-State

For complete documentation, see the data sheet.

High-Performance Silicon-Gate CMOS

The MC74HC125A and MC74HC126A are identical in pinout to the LS125 and LS126. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC125A and HC126A noninverting buffers are designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The devices have four separate output enables that are active-low (HC125A) or active-high (HC126A).

Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 <FONT FACE=SYMBOL>m</FONT>A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- Pb-Free Packages are Available

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Part Electrical Specifications

Product	Compliance	Status	Channels	Output	V_{CC} Min (V)	V_{CC} Max (V)	t_{pd} Max (ns)	I_O Max (mA)	Package Type
MC74HC125ADG	Pb-free Halide free	Active	4	3-State	2	6	24	6	SOIC-14
MC74HC125ADR2G	Pb-free Halide free	Active	4	3-State	2	6	24	6	SOIC-14
MC74HC125ADTG	Pb-free Halide free	Active	4	3-State	2	6	24	6	TSSOP-14
MC74HC125ADTR2G	Pb-free Halide free	Active	4	3-State	2	6	24	6	TSSOP-14
NLV74HC125ADG	AEC Qualified PPAP Capable Pb-free Halide free	Active	4	3-State	2	6	24	6	SOIC-14
NLV74HC125ADR2G	AEC Qualified PPAP Capable Pb-free Halide free	Active	4	3-State	2	6	24	6	SOIC-14
NLV74HC125ADTG	AEC Qualified PPAP Capable Pb-free Halide free	Active	4	3-State	2	6	24	6	TSSOP-14
NLV74HC125ADTR2G	AEC Qualified PPAP Capable Pb-free Halide free	Active	4	3-State	2	6	24	6	TSSOP-14
NLVHC125ADTR2G	AEC Qualified PPAP Capable Pb-free Halide free	Active	4	3-State	2	6	24	6	TSSOP-14

For more information please contact your local sales support at www.onsemi.com.

Created on: 6/18/2019

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