chanhvinh.com

FAIRCHILD SEMICONDUCTOR®

February 2006

FDS8884

N-Channel PowerTrench® MOSFET

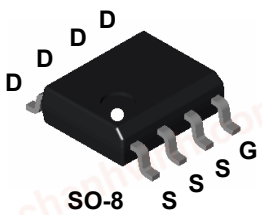
30V, 8.5A, 23mΩ

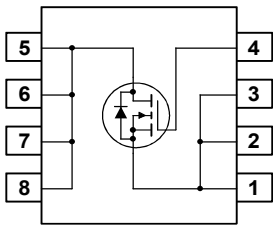
General Descriptions

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$ and fast switching speed.

Features

- Max $r_{DS(on)}$ = 23mΩ at V_{GS} = 10V, I_D = 8.5A
- Max $r_{DS(on)}$ = 30mΩ at V_{GS} = 4.5V, I_D = 7.5A
- Low gate charge
- 100% R_G Tested
- RoHS Compliant





MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DS}	Drain to Source Voltage		30	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current Continuous	(Note 1a)	8.5	A
	Pulsed		40	A
E_{AS}	Single Pulse Avalanche Energy	(Note 2)	32	mJ
P_D	Power dissipation		2.5	W
	Derate above 25°C		20	mW/°C
T_J, T_{STG}	Operating and Storage Temperature		-55 to 150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Case	(Note 1)	25	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS8884	FDS8884	SO-8	330mm	12mm	2500 units

©2006 Fairchild Semiconductor Corporation

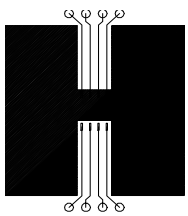
chanhvinh.com

Electrical Characteristics T_J = 25°C unless otherwise noted

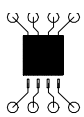
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		23		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24V, V_{GS} = 0V			1	μA
		V_{DS} = 24V, V_{GS} = 0V, T_J = 125°C			250	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V			±100	nA
On Characteristics (Note 3)						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	1.2	1.7	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		-4.9		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10V, I_D = 8.5A,		19	23	mΩ
		V_{GS} = 4.5V , I_D = 7.5A,		23	30	mΩ
		V_{GS} = 10V, I_D = 8.5A, T_J = 125°C		26	32	mΩ
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz		475	635	pF
C_{oss}	Output Capacitance			100	135	pF
C_{rss}	Reverse Transfer Capacitance			65	100	pF
R_G	Gate Resistance	f = 1MHz		0.9	1.6	Ω
Switching Characteristics (Note 3)						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15V, I_D = 8.5A, V_{GS} = 10V, R_{GS} = 33Ω		5	10	ns
t_r	Rise Time			9	18	ns
$t_{d(off)}$	Turn-Off Delay Time			42	68	ns
t_f	Fall Time			21	34	ns
Q_g	Total Gate Charge	V_{DS} = 15V, V_{GS} = 10V, I_D = 8.5A		9.2	13	nC
Q_g	Total Gate Charge	V_{DS} = 15V, V_{GS} = 5V, I_D = 8.5A		5.0	7	nC
Q_{gs}	Gate to Source Gate Charge			1.5		nC
Q_{gd}	Gate to Drain Charge			2.0		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 8.5A		0.9	1.25	V
		I_{SD} = 2.1A		0.8	1.0	V
t_{rr}	Reverse Recovery Time	I_F = 8.5A, di/dt = 100A/μs			33	ns
Q_{rr}	Reverse Recovery Charge				20	nC

Notes:

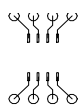
1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1 in2 pad of 2 oz copper



b) 105°C/W when mounted on a .04 in^2 pad of 2 oz copper



c) 125°C/W when mounted on a minimun pad

Scale 1 : 1 on letter size paper

2: Starting T_J = 25°C, L = 1mH, I_{AS} = 8A, V_{DD} = 27V, V_{GS} = 10V.

3: Pulse Test:Pulse Width <300μS, Duty Cycle <2%.

chanhvinh.com

Typical Characteristics T_J = 25°C unless otherwise noted

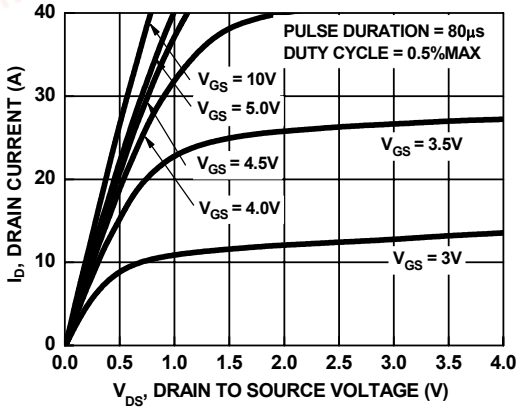


Figure 1. On Region Characteristics

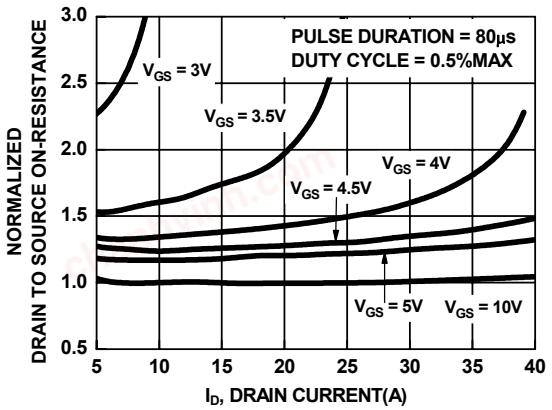


Figure 2. Normalized On-Resistance vs Drain current and Gate Voltage

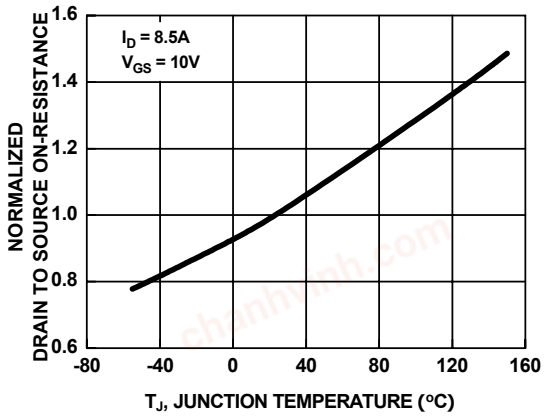


Figure 3. Normalized On Resistance vs Junction Temperature

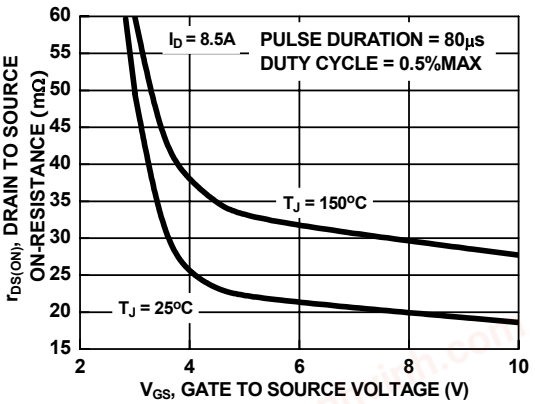


Figure 4. On-Resistance vs Gate to Source Voltage

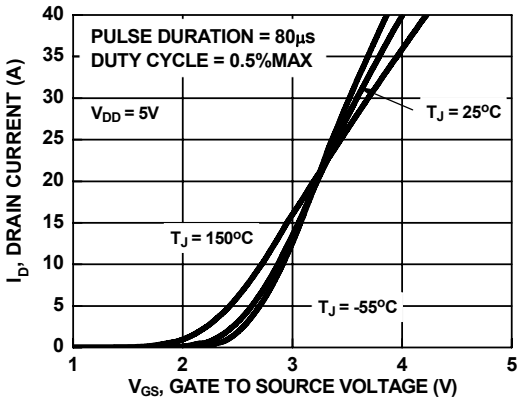


Figure 5. Transfer Characteristics

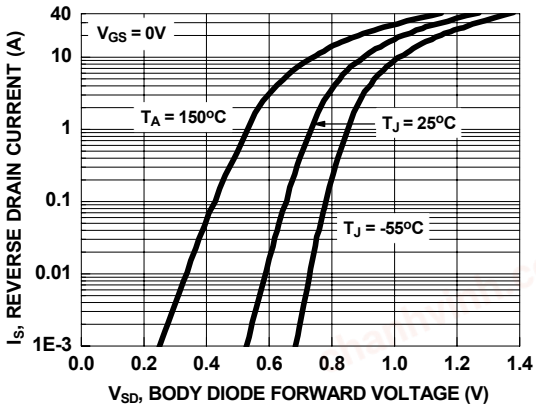


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

chanhvinh.com

Typical Characteristics T_J = 25°C unless otherwise noted

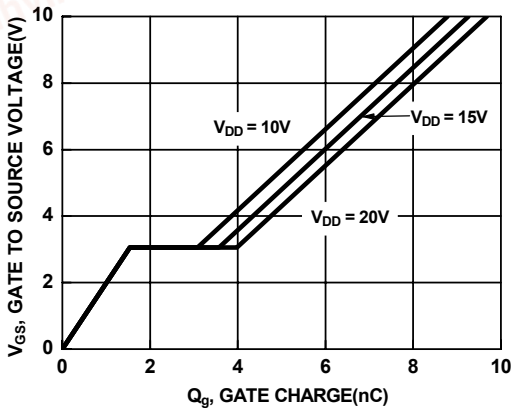


Figure 7. Gate Charge Characteristics

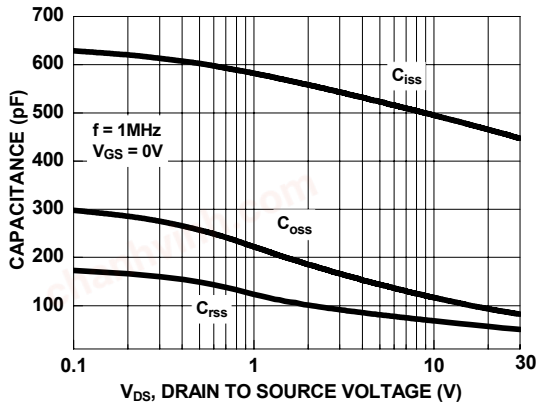


Figure 8. Capacitance vs Drain to Source Voltage

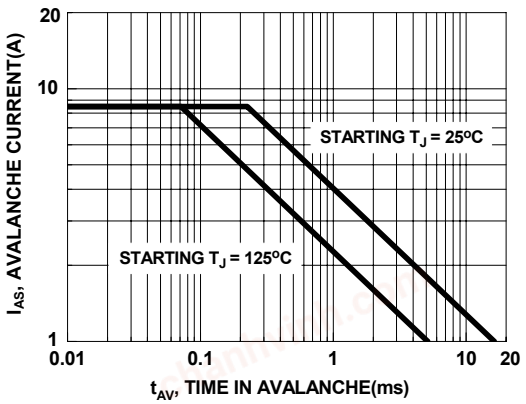


Figure 9. Unclamped Inductive Switching Capability

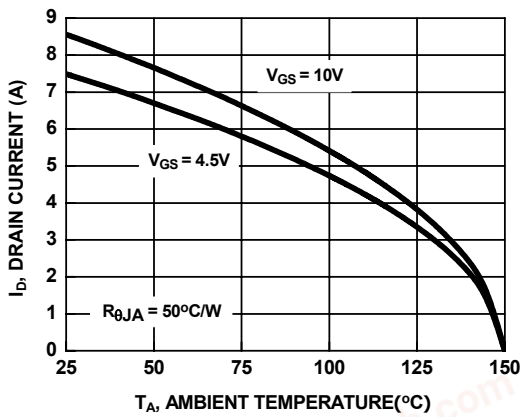


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

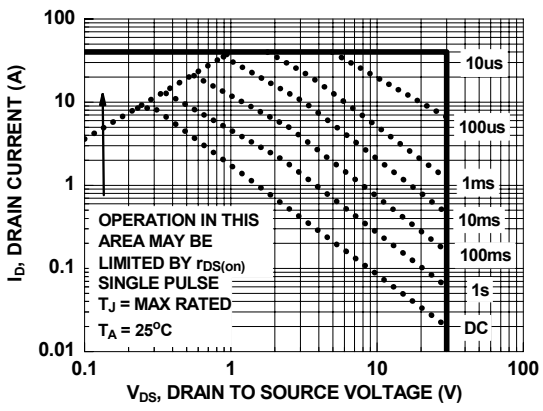


Figure 11. Forward Bias Safe Operating Area

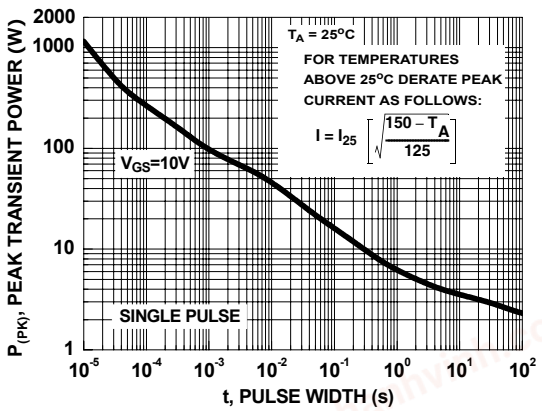


Figure 12. Single Pulse Maximum Power Dissipation

chanhvinh.com

Typical Characteristics T_J = 25°C unless otherwise noted

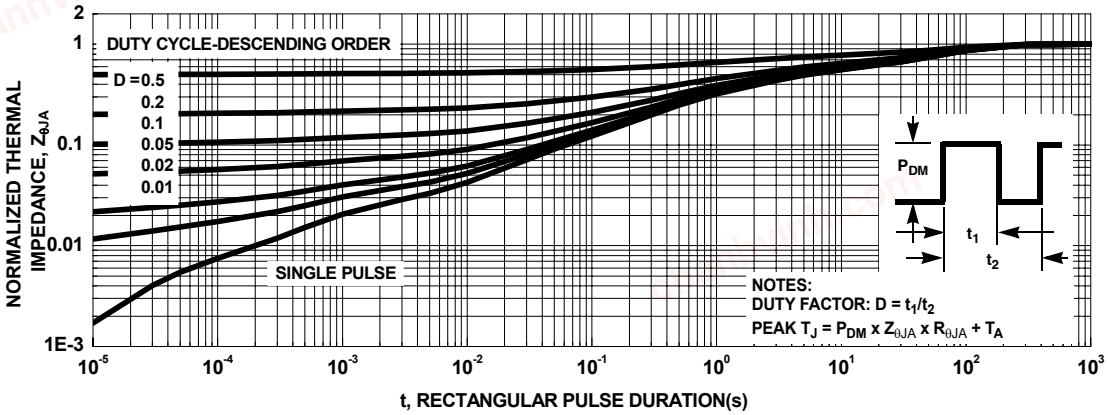


Figure 13. Transient Thermal Response Curve

chanhvinh.com

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FAST®	ISOPLANAR™	PowerSaver™	SuperSOT™-6
ActiveArray™	FASTr™	LittleFET™	PowerTrench®	SuperSOT™-8
Bottomless™	FPS™	MICROCOUPLER™	QFET®	SyncFET™
Build it Now™	FRFET™	MicroFET™	QS™	TCM™
CoolFET™	GlobalOptoisolator™	MicroPak™	QT Optoelectronics™	TinyLogic®
CROSSVOLT™	GTO™	MICROWIRE™	Quiet Series™	TINYOPTO™
DOME™	HiSeC™	MSX™	RapidConfigure™	TruTranslation™
EcoSPARK™	I^2C™	MSXPro™	RapidConnect™	UHC™
E^2CMOS™	*i-Lo*™	OCX™	µSerDes™	UltraFET®
EnSigna™	ImpliedDisconnect™	OCXPro™	ScalarPump™	UniFET™
FACT™	IntelliMAX™	OPTOLOGIC®	SILENT SWITCHER®	VCX™
FACT Quiet Series™		OPTOPLANAR™	SMART START™	Wire™
		PACMAN™	SPM™	
Across the board. Around the world.™		POP™	Stealth™	
The Power Franchise®		Power247™	SuperFET™	
Programmable Active Droop™		PowerEdge™	SuperSOT™-3	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. I18