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March 2016

FDP51N25 / FDPF51N25

N-Channel UniFET™ MOSFET

250 V, 51 A, 60 mΩ

Features

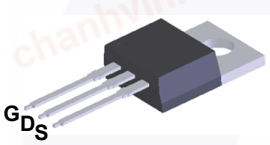
- $R_{DS(on)}$ = 48 mΩ(Typ.) @ V_{GS} = 10 V, I_D = 25.5 A
- Low Gate Charge (Typ. 55 nC)
- Low C_{rss} (Typ. 63 pF)

Applications

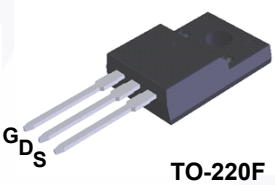
- PDP TV
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

Description

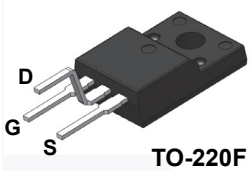
UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



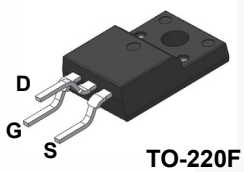
TO-220



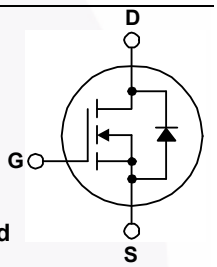
TO-220F



TO-220F
Y-formed



TO-220F
LG-formed



Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FDP51N25	FDPF51N25 FDPF51N25YDTU FDPF51N25RDTU	Unit
V_{DSS}	Drain-Source Voltage		250		V
I_D	Drain Current	- Continuous (T_C = 25°C) - Continuous (T_C = 100°C)	51 30	51* 30*	A A
I_{DM}	Drain Current	- Pulsed (Note 1)	204	204*	A
V_{GSS}	Gate-Source voltage		±30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		1111		mJ
I_{AR}	Avalanche Current (Note 1)		51		A
E_{AR}	Repetitive Avalanche Energy (Note 1)		32		mJ
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=0.3sec; T_C = 25°C)		N/A	2500	V
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5		V/ns
P_D	Power Dissipation	(T_C = 25°C) - Derate Above 25°C	320 3.7	38 0.3	W W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150		°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300		°C

*Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	FDP51N25	FDPF51N25 FDPF51N25YDTU FDPF51N25RDTU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.39	3.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	62.5	°C/W

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Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP51N25	FDP51N25	TO-220	Tube	N/A	N/A	50 units
FDPF51N25	FDPF51N25	TO-220F	Tube	N/A	N/A	50 units
FDPF51N25YDTU	FDPF51N25	TO-220F (Y-formed)	Tube	N/A	N/A	50 units
FDPF51N25RDTU	FDPF51N25	TO-220F (LG-formed)	Tube	N/A	N/A	50 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA, T_J = 25 °C	250	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.25	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 250 V, V_{GS} = 0 V V_{DS} = 200 V, T_C = 125°C	-- --	-- --	1 10	μA μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 25.5 A	--	0.048	0.060	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 25.5 A	--	43	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	--	2620	3410	pF
C_{oss}	Output Capacitance		--	530	690	pF
C_{rss}	Reverse Transfer Capacitance		--	63	90	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 125 V, I_D = 51 A, V_{GS} = 10 V, R_G = 25 Ω	--	62	135	ns
t_r	Turn-On Rise Time		--	465	940	ns
$t_{d(off)}$	Turn-Off Delay Time		--	98	205	ns
t_f	Turn-Off Fall Time	(Note 4)	--	130	270	ns
Q_g	Total Gate Charge	V_{DS} = 200 V, I_D = 51 A, V_{GS} = 10 V	--	55	70	nC
Q_{gs}	Gate-Source Charge		--	16	--	nC
Q_{gd}	Gate-Drain Charge	(Note 4)	--	27	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	51	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	204	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 51 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 51 A, dI_F/dt =100 A/μs	--	178	--	ns
Q_{rr}	Reverse Recovery Charge		--	4.0	--	μC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. L = 0.68 mH, I_{AS} = 51 A, V_{DD} = 50 V, R_G = 25 Ω starting T_J = 25°C.
3. $I_{SD} \le$ 51 A, di/dt ≤ 200 A/μs, $V_{DD} \le BV_{DSS}$, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristics.

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Typical Performance Characteristics

Figure 1. On-Region Characteristics

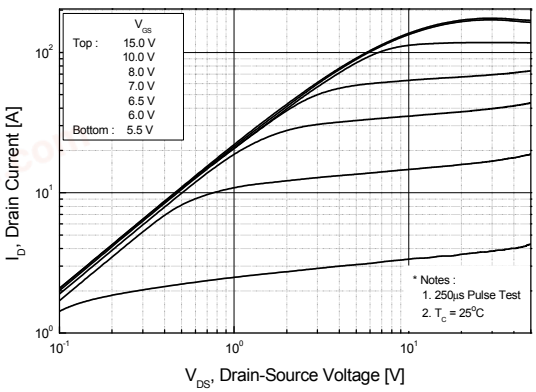


Figure 2. Transfer Characteristics

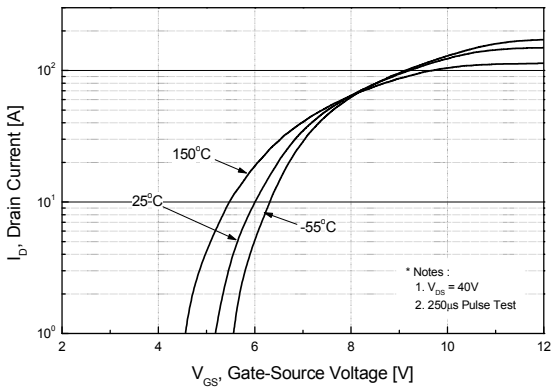


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

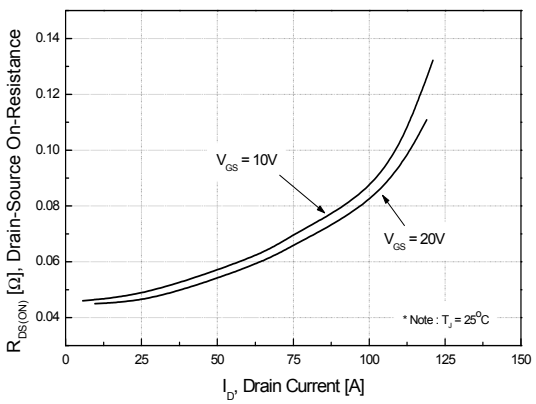


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

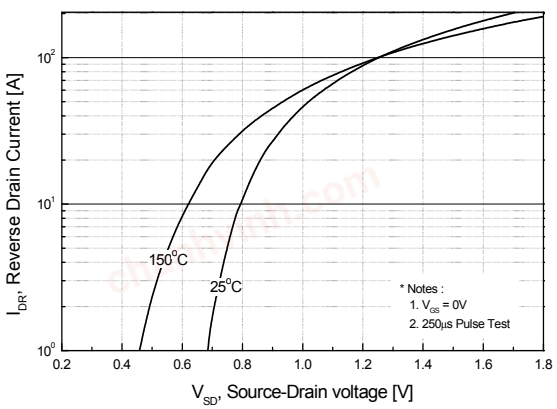


Figure 5. Capacitance Characteristics

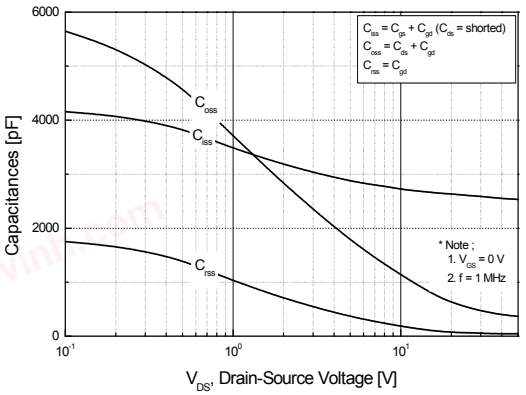
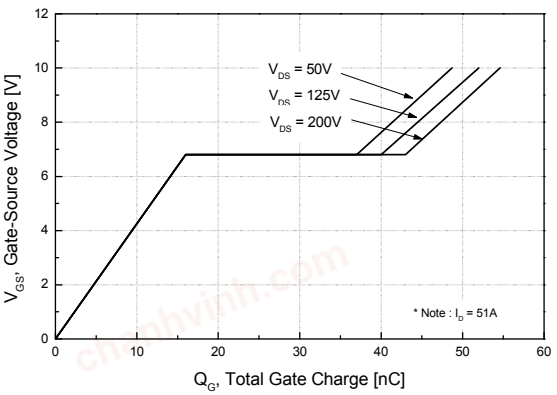


Figure 6. Gate Charge Characteristics



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Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

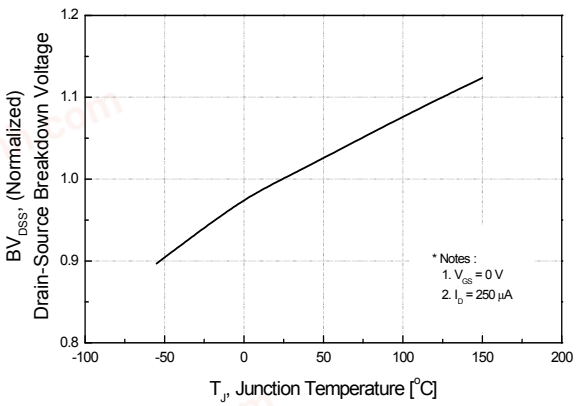


Figure 8. On-Resistance Variation vs. Temperature

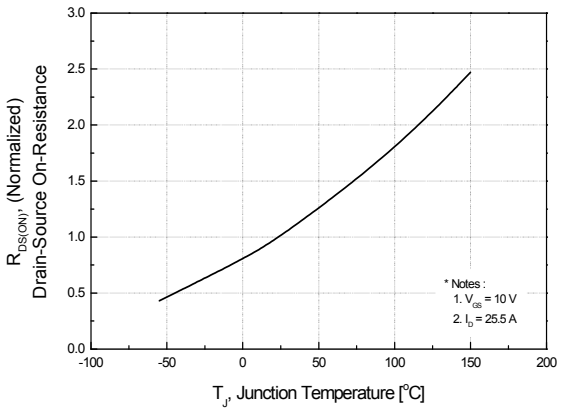


Figure 9-1. Maximum Safe Operating Area for FDP51N25

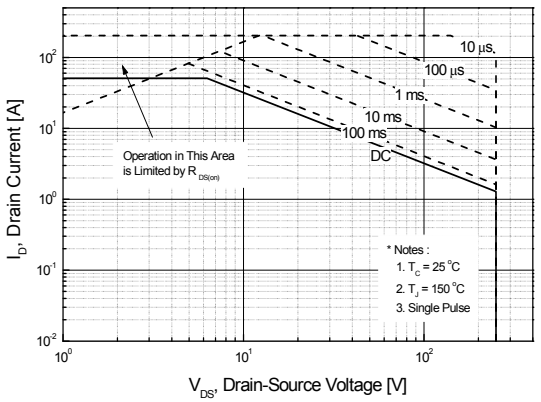


Figure 9-2. Maximum Safe Operating Area for FDPF51N25 / FDPF51N25YDTU

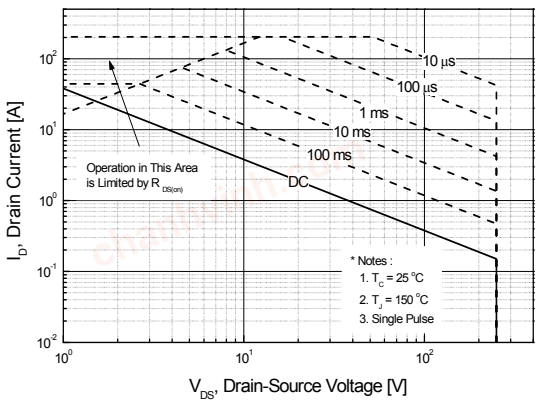
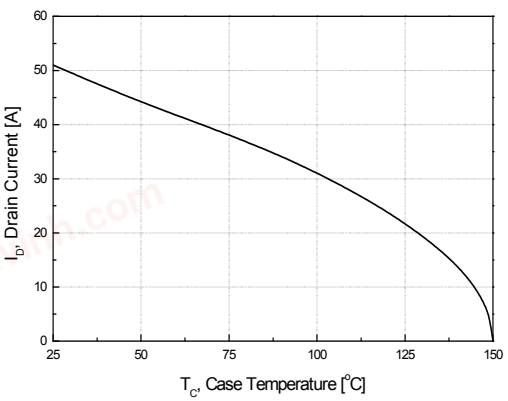


Figure 10. Maximum Drain Current vs. Case Temperature



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Typical Performance Characteristics (Continued)

Figure 11-1. Transient Thermal Response Curve for FDP51N25

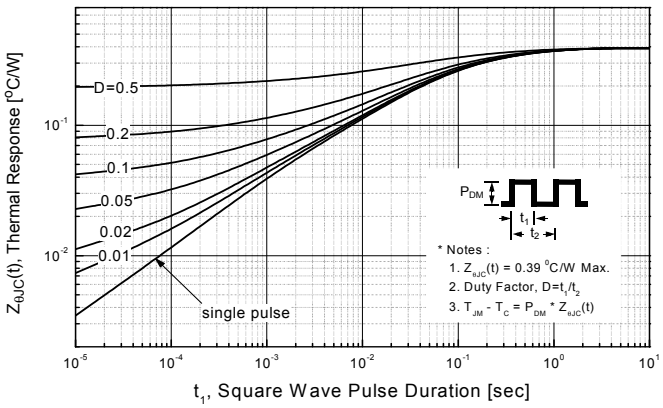
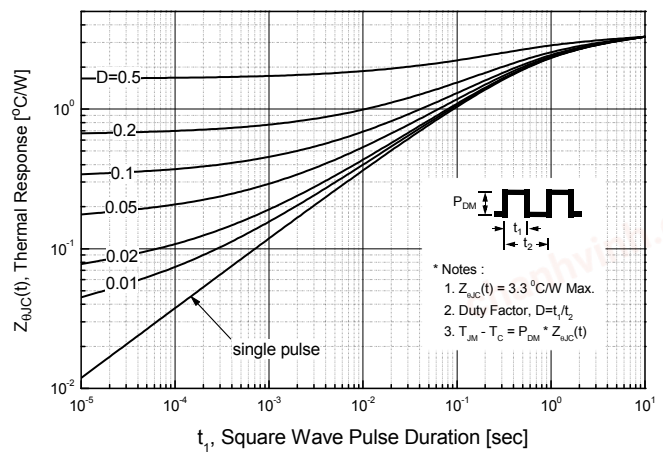


Figure 11-2. Transient Thermal Response Curve for FDPF51N25 / FDPF51N25YDTU



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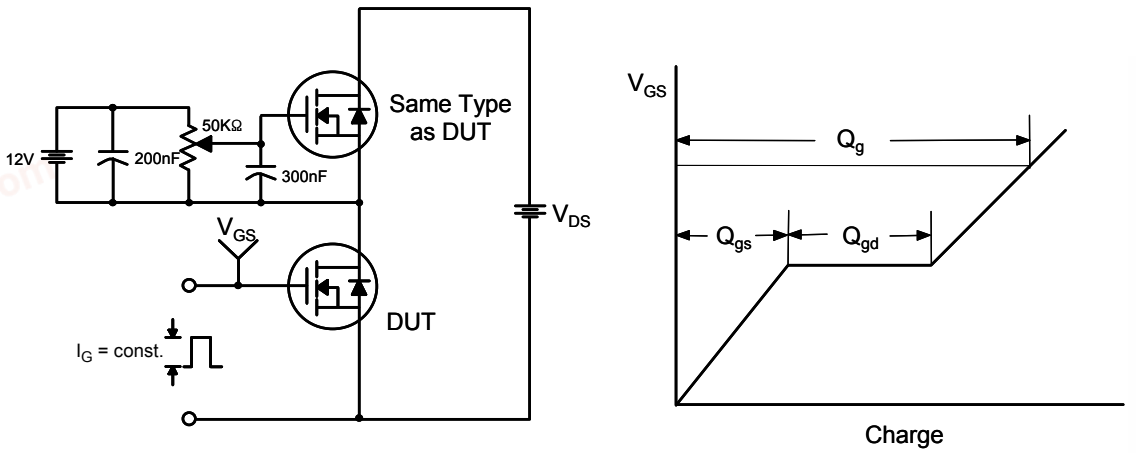


Figure 12. Gate Charge Test Circuit & Waveform

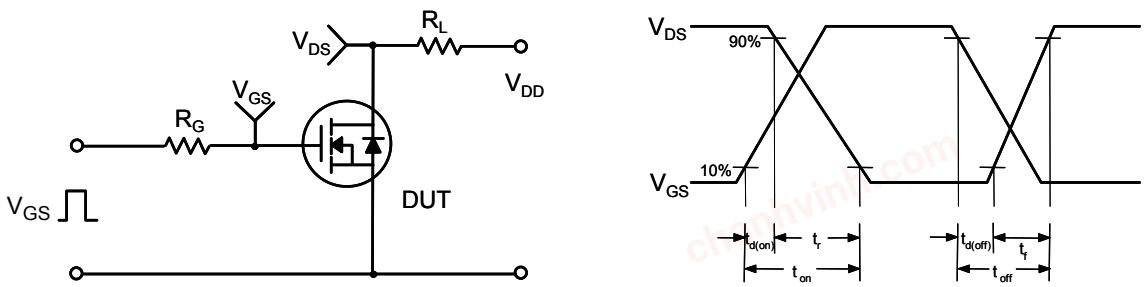


Figure 13. Resistive Switching Test Circuit & Waveforms

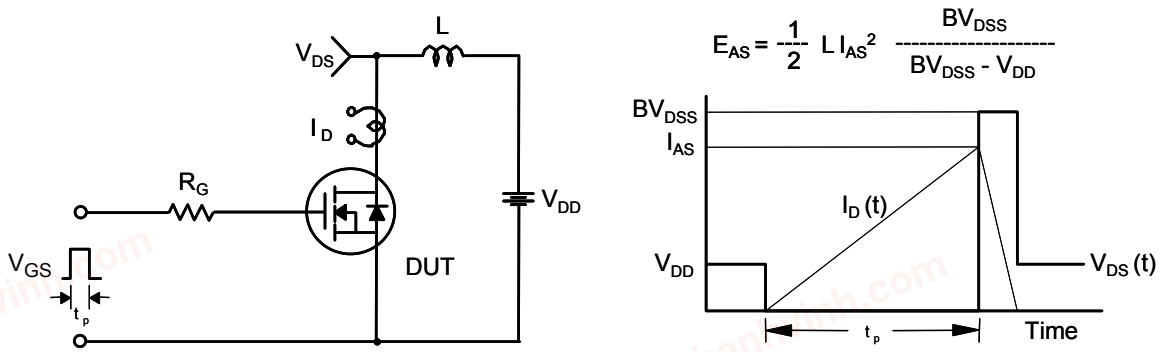


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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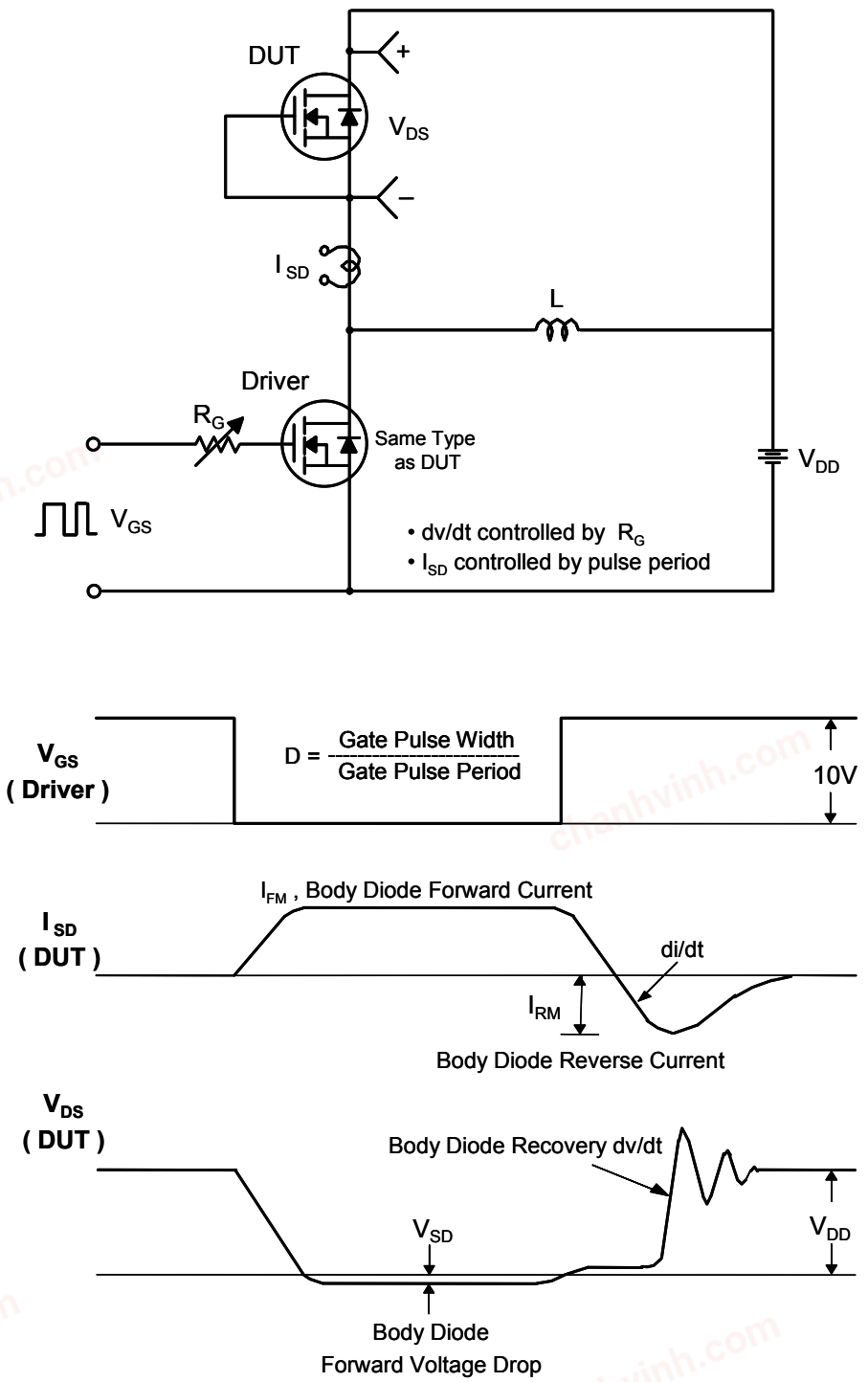


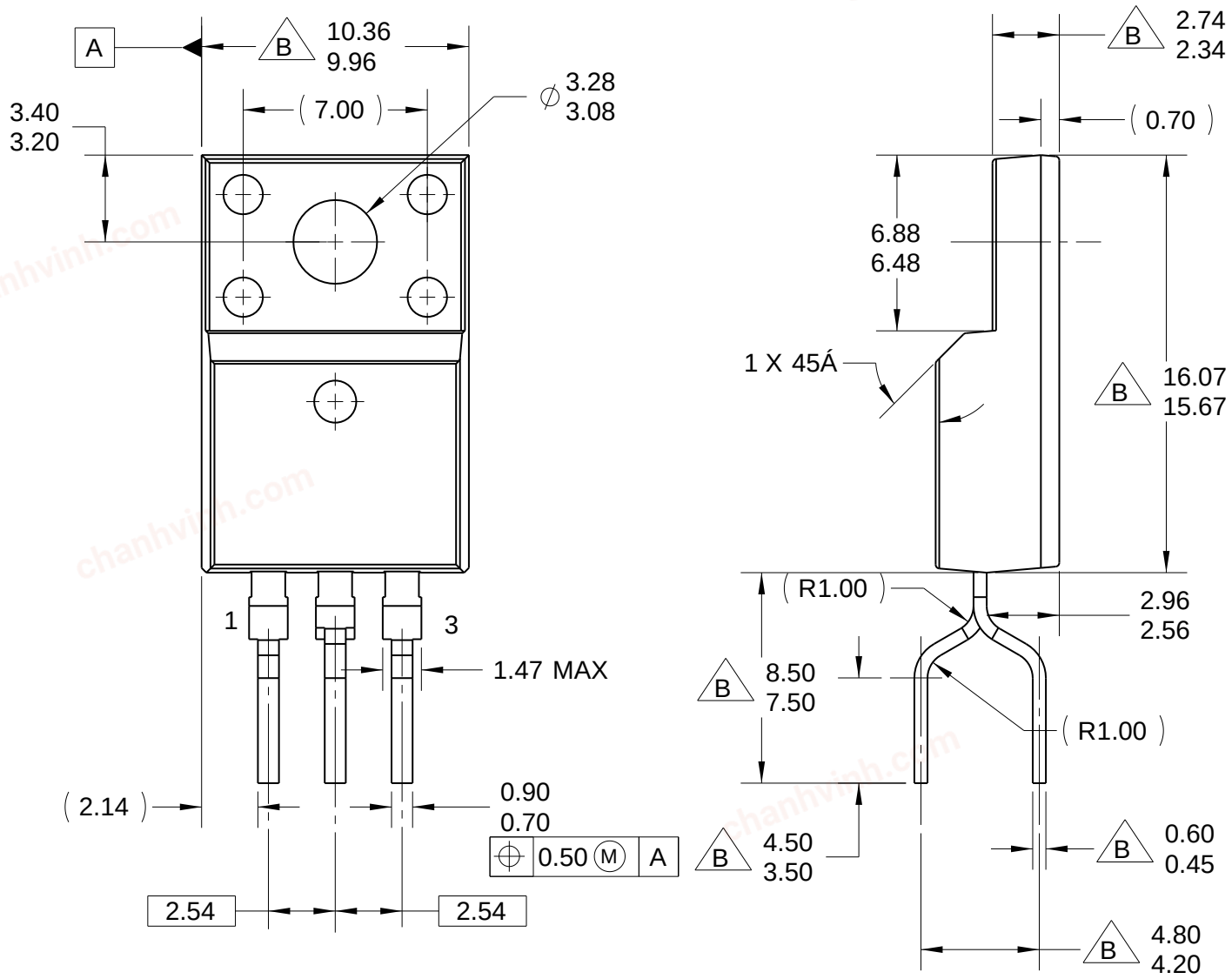
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

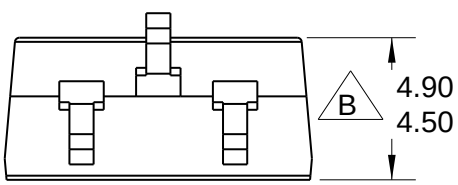
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REVISIONS

NBR	DESCRIPTION	DATE	BY/APP'D
1	RELEASED TO DCC	04JUN08	SDLEE/ SUZHOU





NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
B DOES NOT COMPLY EIAJ STD. VALUE.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
F. DRAWING FILE NAME: TO220N03REV1

APPROVALS	DATE
DRAWN: BOBOY MALDO	04JUN08
CHECKED: SD LEE	
APPROVED: BY HUANG	
APPROVED: HOWARD ALLEN	

PROJECTION [MM] INCH

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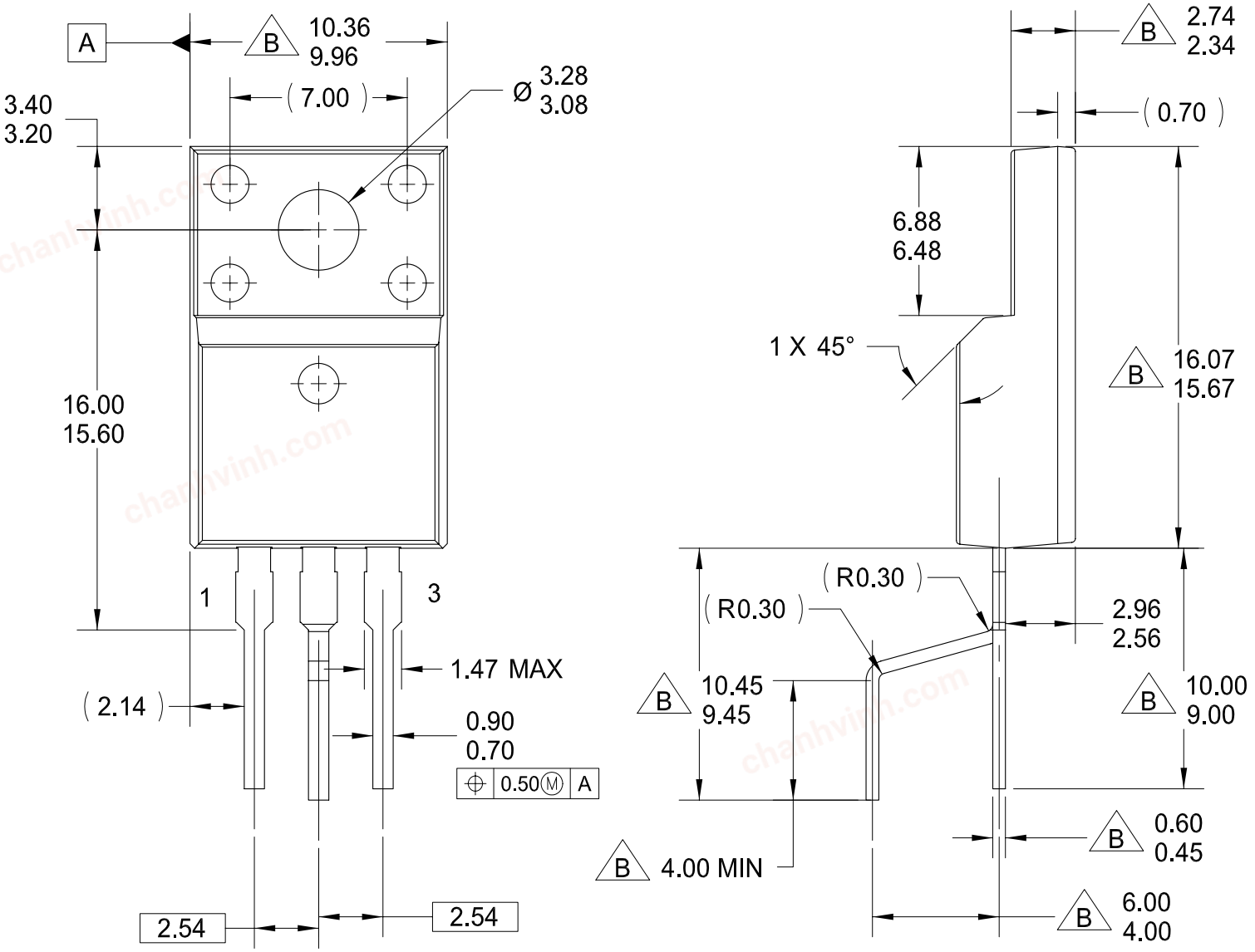
TO220, MOLDED, 3LD, FULL PACK, EIAJ SC91, LG FORM

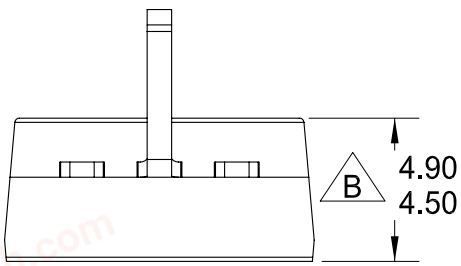
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FORMERLY: N/A

SHEET : 1 OF 1

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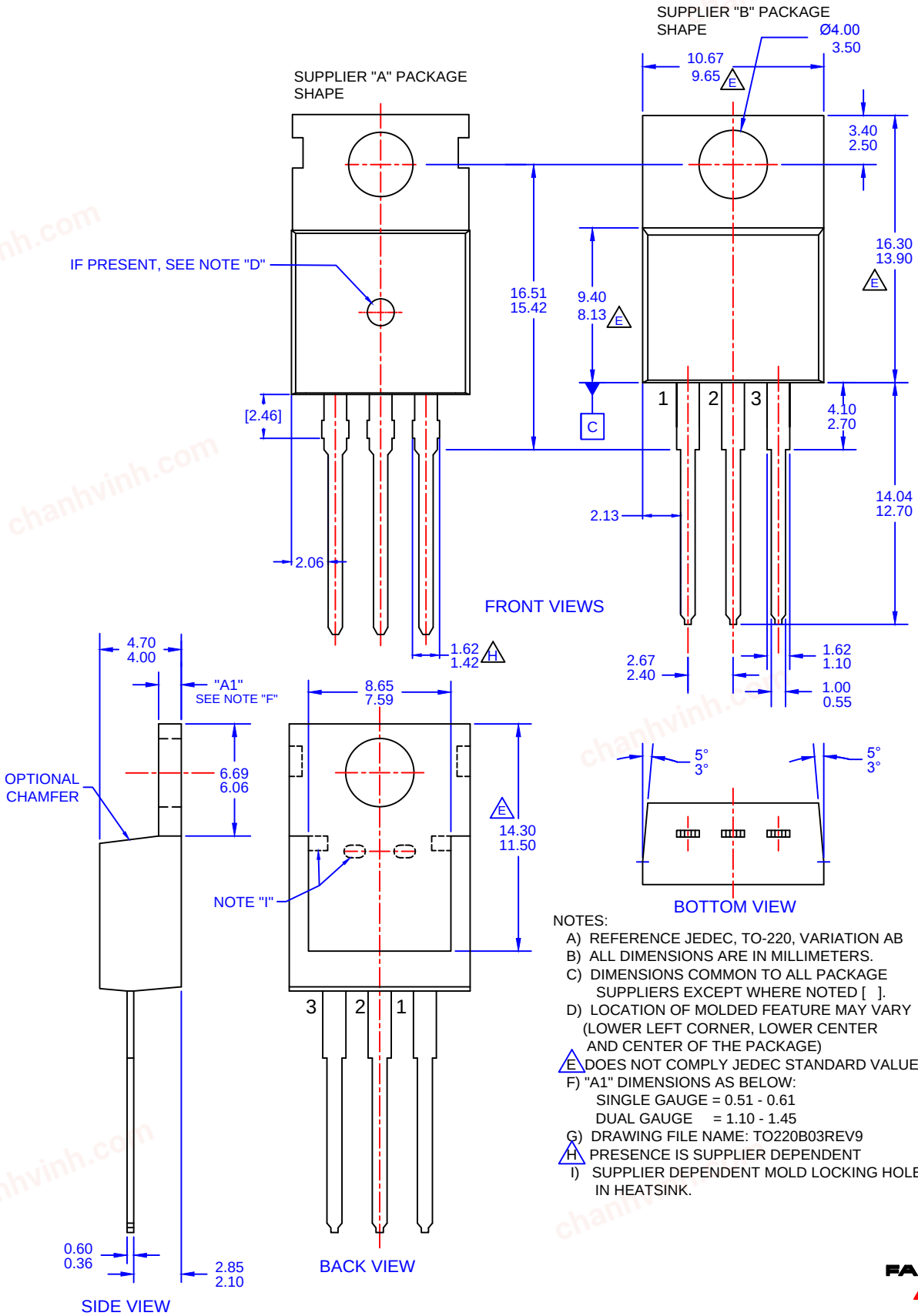




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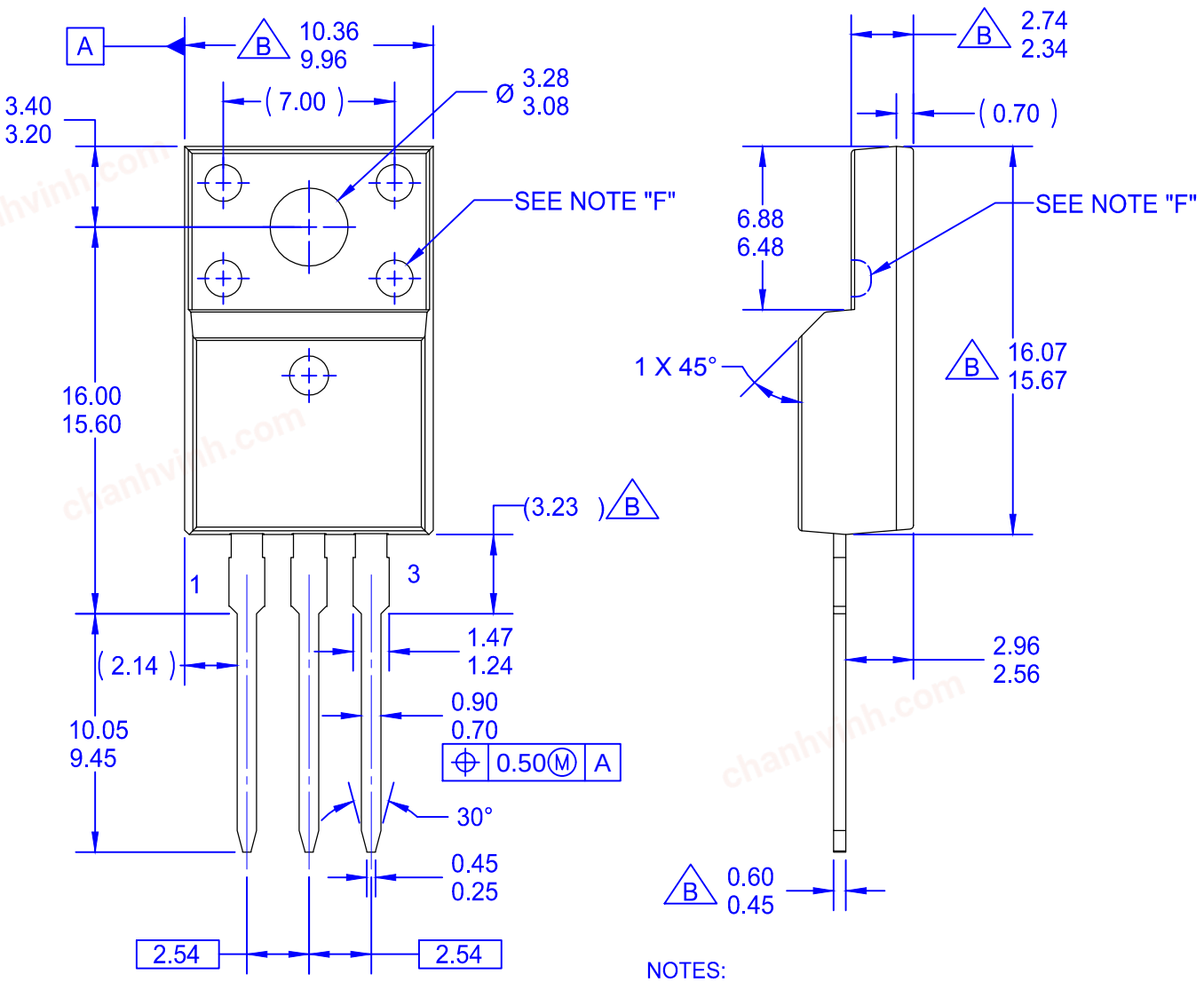


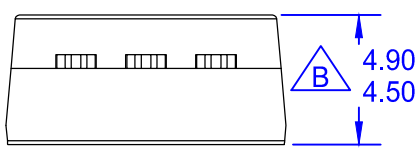
NOTES:

A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E) DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
G) DRAWING FILE NAME: TO220B03REV9
H) PRESENCE IS SUPPLIER DEPENDENT
I) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
F. OPTION 1 - WITH SUPPORT PIN HOLE.
OPTION 2 - NO SUPPORT PIN HOLE.
G. DRAWING FILE NAME: TO220M03REV4

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SuperSOT™-6
SuperSOT™-8
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TinyPWM™
TinyWire™
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µSerDes™
SerDes™
UHC®
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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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