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FAIRCHILD SEMICONDUCTOR®

February 2007

FDMS2672
N-Channel UltraFET Trench MOSFET
200V, 20A, 77mΩ

Features

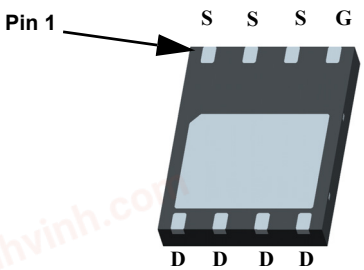
- Max $r_{DS(on)}$ = 77mΩ at V_{GS} = 10V, I_D = 3.7A
- Max $r_{DS(on)}$ = 88mΩ at V_{GS} = 6V, I_D = 3.5A
- Low Miller Charge
- RoHS Compliant

General Description

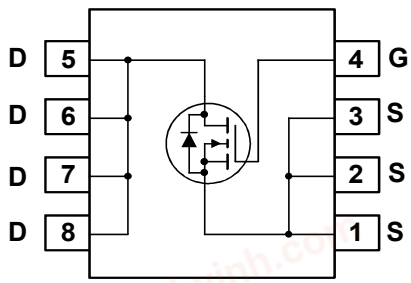
UltraFET devices combine characteristics that enable benchmark efficiency in power conversion applications. Optimized for $r_{DS(on)}$, low ESR, low total and Miller gate charge, these devices are ideal for high frequency DC to DC converters.

Application

- DC - DC Conversion



Power 56 (Bottom view)



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			200	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous (Silicon limited)	T_C = 25°C		20	A
	-Continuous	T_A = 25°C	(Note 1a)	3.7	
	-Pulsed			20	
P_D	Power Dissipation	T_C = 25°C		78	W
	Power Dissipation	T_A = 25°C	(Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS2672	FDMS2672	Power 56	13”	12mm	3000 units

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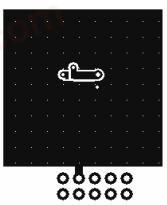
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Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	200			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		210		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 160V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	2	3.1	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		-10		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10V, I_D = 3.7A		64	77	mΩ
		V_{GS} = 6V, I_D = 3.5A		69	88	
		V_{GS} = 10V, I_D = 3.7A T_J = 125°C		129	156	
g_{FS}	Forward Transconductance	V_{DS} = 10V, I_D = 3.7A		14		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 100V, V_{GS} = 0V, f = 1MHz		1740	2315	pF
C_{oss}	Output Capacitance			95	125	pF
C_{rss}	Reverse Transfer Capacitance			30	45	pF
R_g	Gate Resistance	f = 1MHz		0.9		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 100V, I_D = 3.7A V_{GS} = 10V, R_{GEN} = 6Ω		22	34	ns
t_r	Rise Time			11	22	ns
$t_{d(off)}$	Turn-Off Delay Time			36	57	ns
t_f	Fall Time			10	20	ns
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0V to 10V, V_{DD} = 100V, I_D = 3.7A		30	42	nC
Q_{gs}	Gate to Source Gate Charge			7		nC
Q_{gd}	Gate to Drain “Miller” Charge			8		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 3.7A (Note 2)		0.8	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 3.7A, di/dt = 100A/μs		70	105	ns
Q_{rr}	Reverse Recovery Charge			238	357	nC

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 125°C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

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Typical Characteristics T_J = 25°C unless otherwise noted

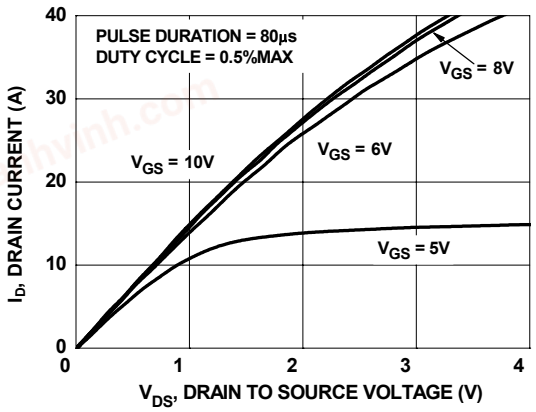


Figure 1. On Region Characteristics

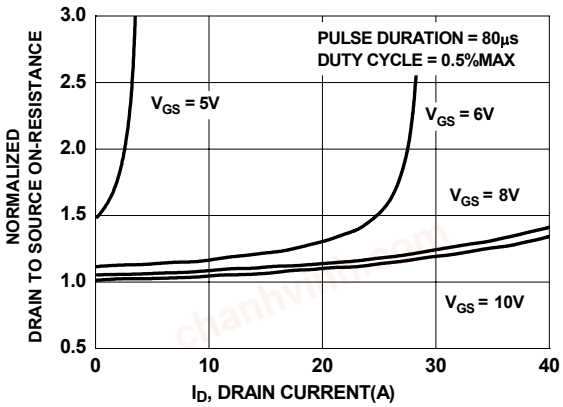


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

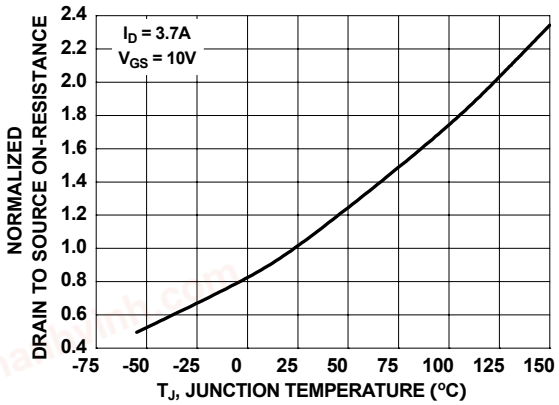


Figure 3. Normalized On Resistance vs Junction Temperature

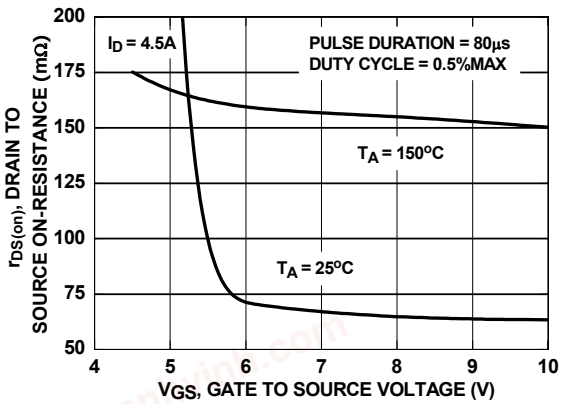


Figure 4. On-Resistance vs Gate to Source Voltage

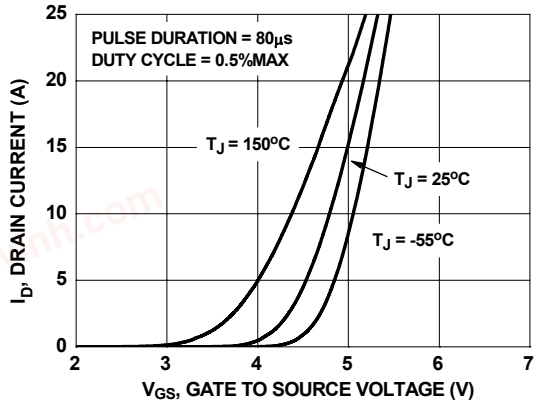


Figure 5. Transfer Characteristics

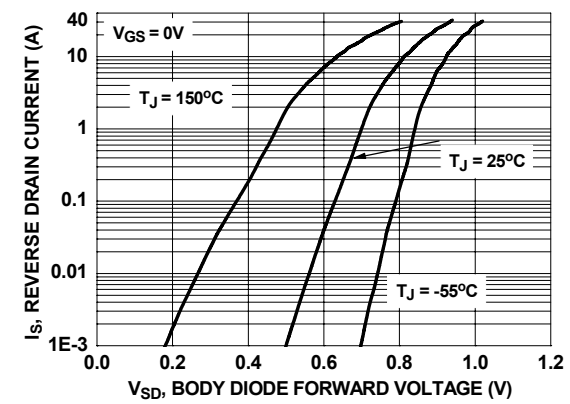


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

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Typical Characteristics T_J = 25°C unless otherwise noted

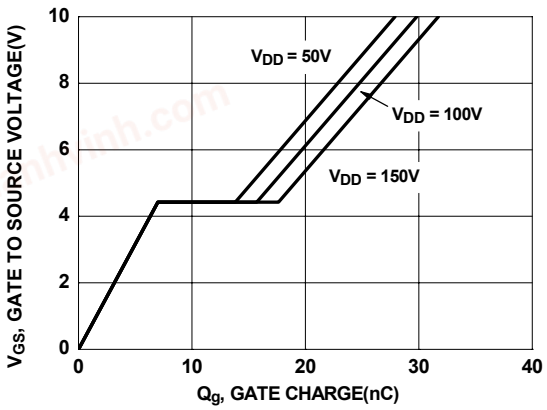


Figure 7. Gate Charge Characteristics

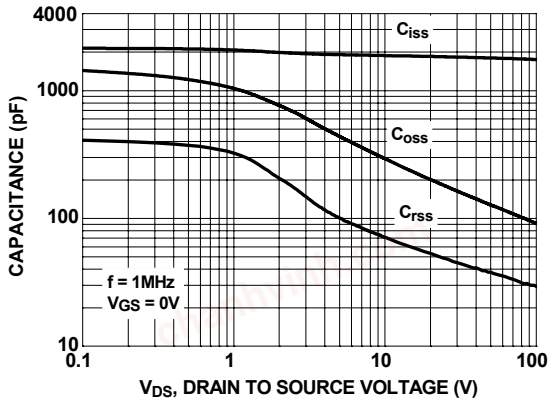


Figure 8. Capacitance vs Drain to Source Voltage

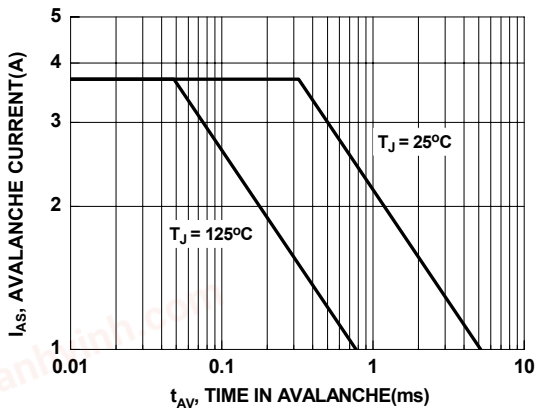


Figure 9. Unclamped Inductive Switching Capability

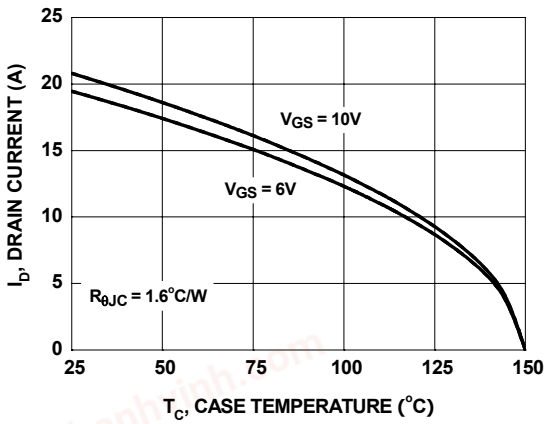


Figure 10. Maximum Continuous Drain Current vs Case Temperature

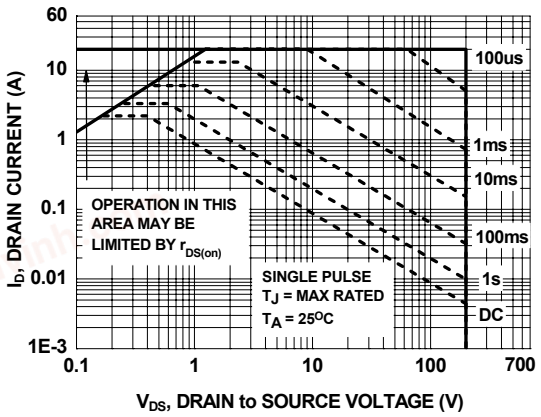


Figure 11. Forward Bias Safe Operating Area

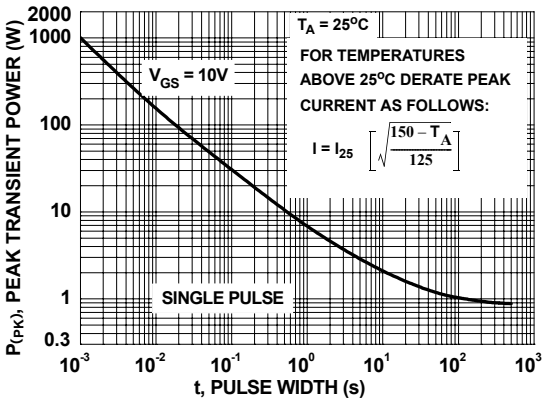


Figure 12. Single Pulse Maximum Power Dissipation

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Typical Characteristics T_J = 25°C unless otherwise noted

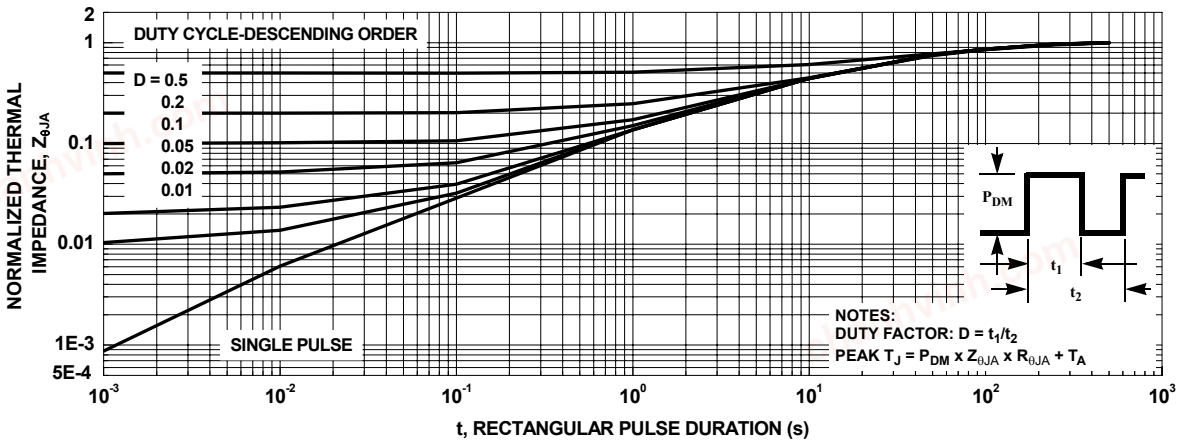
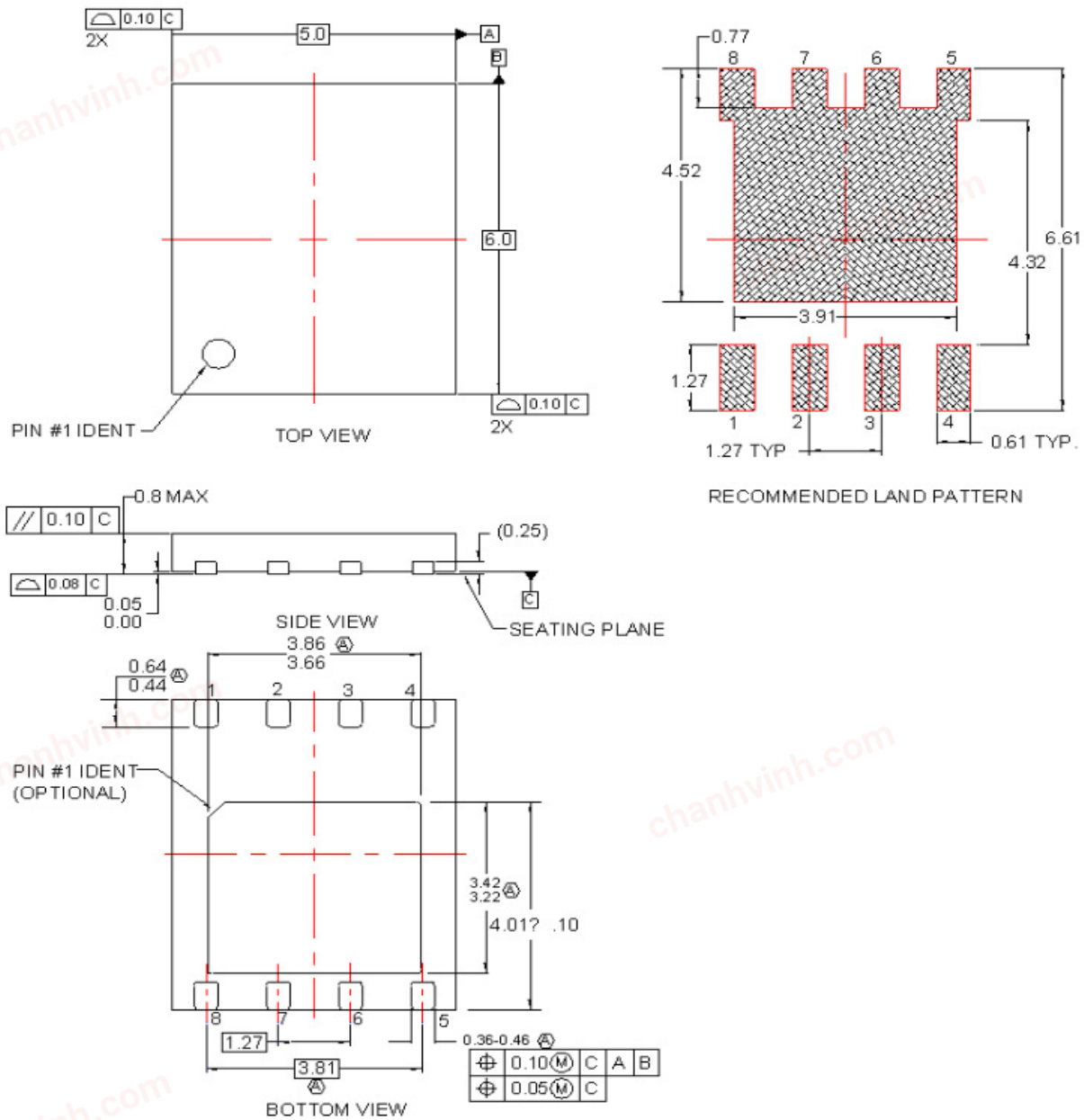


Figure 13. Transient Thermal Response Curve

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NOTES:

A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229. DATED 11/2001.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

D. TERMINALS 5,6,7 AND 8 ARE TIED TO THE EXPOSED PADDLE

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