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FAIRCHILD SEMICONDUCTOR®

October 2013

FDME905PT

P-Channel PowerTrench® MOSFET

-12 V, -8 A, 22 mΩ

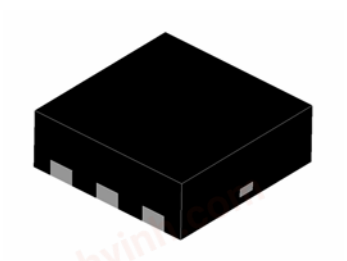
Features

- Max $r_{DS(on)}$ = 22 mΩ at V_{GS} = -4.5 V, I_D = -8 A
- Max $r_{DS(on)}$ = 26 mΩ at V_{GS} = -2.5 V, I_D = -7.3 A
- Max $r_{DS(on)}$ = 97 mΩ at V_{GS} = -1.8 V, I_D = -3.8 A
- Low profile: 0.55 mm maximum in the new package MicroFET 1.6x1.6 **Thin**
- Free from halogenated compounds and antimony oxides
- RoHS Compliant

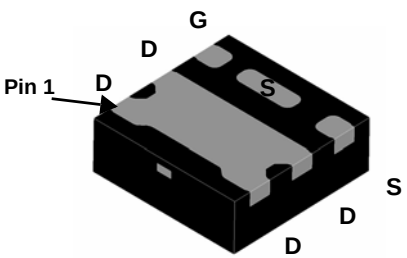
General Description

This device is designed specifically for battery charging or load switching in cellular handset and other ultraportable applications. It features a MOSFET with low on-state resistance.

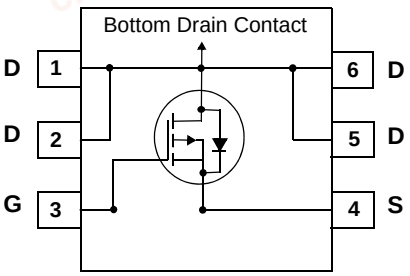
The MicroFET 1.6x1.6 **Thin** package offers exceptional thermal performance for its physical size and is well suited to switching and linear mode applications.



TOP



BOTTOM



MicroFET 1.6x1.6 Thin

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			-12	V
V_{GS}	Gate to Source Voltage			±8	V
I_D	Drain Current -Continuous	T_A = 25 °C	(Note 1a)	-8	A
	-Pulsed			-30	
P_D	Power Dissipation	T_A = 25 °C	(Note 1a)	2.1	W
	Power Dissipation	T_A = 25 °C	(Note 1b)	0.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		4.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	60	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	175	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
E95	FDME905PT	MicroFET 1.6x1.6 **Thin**	7 ”	8 mm	5000 units

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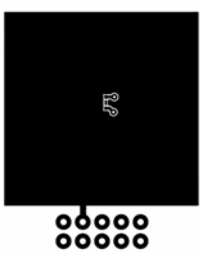
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Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250 μA, V_{GS} = 0 V	-12			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		-8.7		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -9.6 V, V_{GS} = 0 V			-1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250 μA	-0.4	-0.7	-1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		2.5		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = -4.5 V, I_D = -8 A		18	22	mΩ
		V_{GS} = -2.5 V, I_D = -7.3 A		22	26	
		V_{GS} = -1.8 V, I_D = -3.8 A		28	97	
		V_{GS} = -4.5 V, I_D = -8 A, T_J = 125 °C		23	32	
g_{FS}	Forward Transconductance	V_{DS} = -5 V, I_D = -8 A		38		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -6 V, V_{GS} = 0 V, f = 1 MHz		1740	2315	pF
C_{oss}	Output Capacitance			350	525	pF
C_{rss}	Reverse Transfer Capacitance			311	465	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -6 V, I_D = -8 A, V_{GS} = -4.5 V, R_{GEN} = 6 Ω		9.5	19	ns
t_r	Rise Time			8	16	ns
$t_{d(off)}$	Turn-Off Delay Time			90	144	ns
t_f	Fall Time			42	67	ns
Q_g	Total Gate Charge	V_{DD} = -6 V, I_D = -8 A, V_{GS} = -4.5 V		14	20	nC
Q_{gs}	Gate to Source Gate Charge			2.4		nC
Q_{gd}	Gate to Drain “Miller” Charge			3		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = -8 A (Note 2)		-0.8	-1.2	V
		V_{GS} = 0 V, I_S = -1.8 A (Note 2)		-0.7	-1.2	
t_{rr}	Reverse Recovery Time	I_F = -8 A, di/dt = 100 A/μs		17	31	ns
Q_{rr}	Reverse Recovery Charge			4.5	10	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 60 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 175 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.

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Typical Characteristics T_J = 25 °C unless otherwise noted

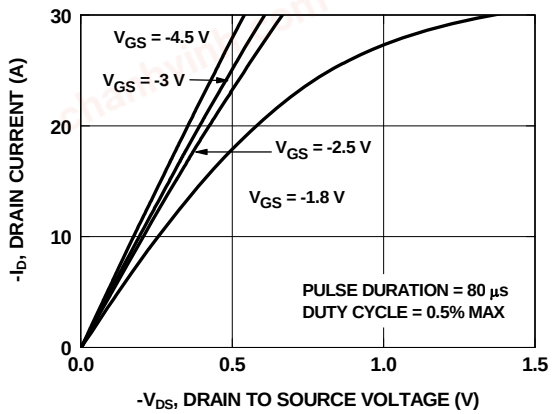


Figure 1. On-Region Characteristics

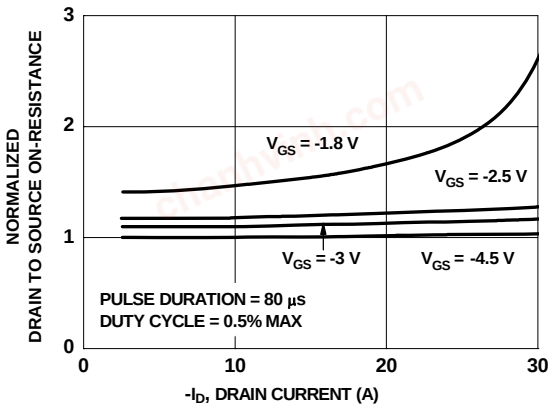


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

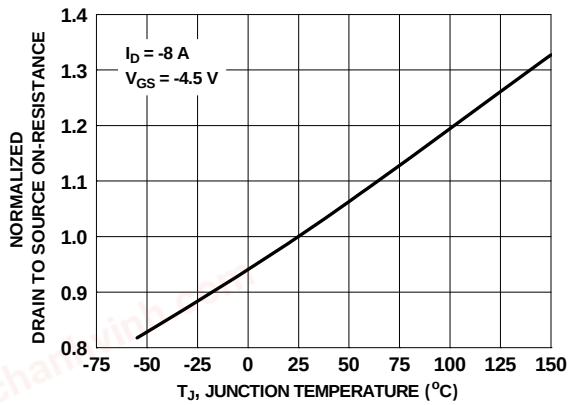


Figure 3. Normalized On-Resistance vs Junction Temperature

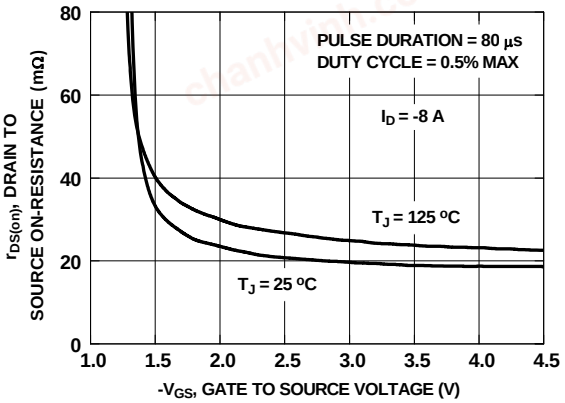


Figure 4. On-Resistance vs Gate to Source Voltage

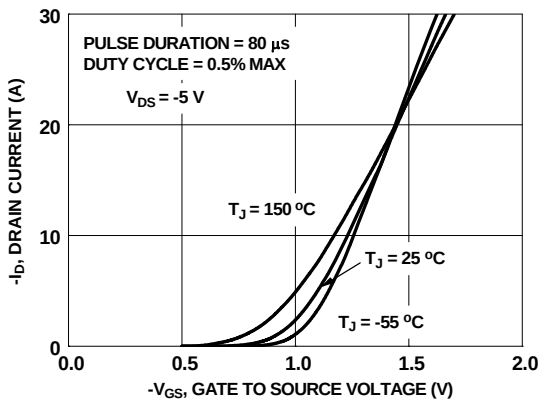


Figure 5. Transfer Characteristics

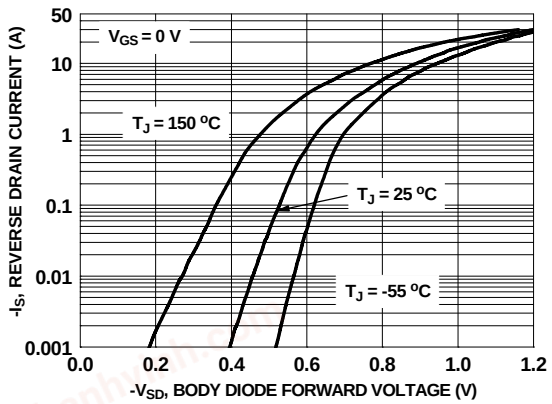


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

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Typical Characteristics T_J = 25 °C unless otherwise noted

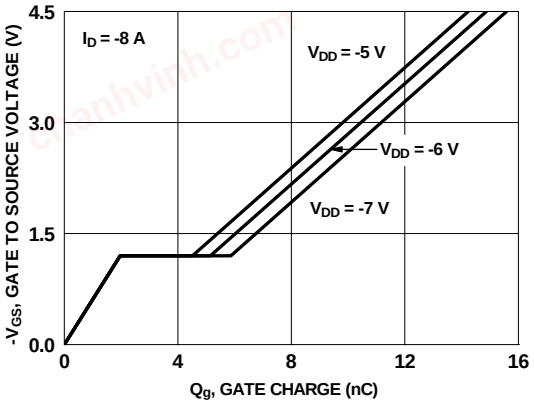


Figure 7. Gate Charge Characteristics

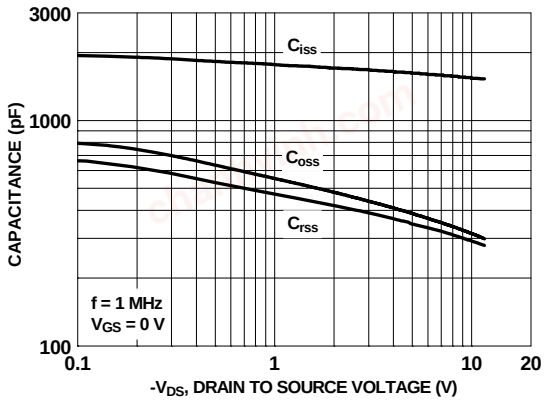


Figure 8. Capacitance vs Drain to Source Voltage

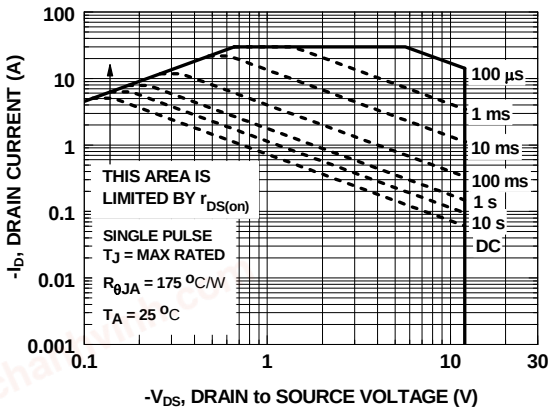


Figure 9. Forward Bias Safe Operating Area

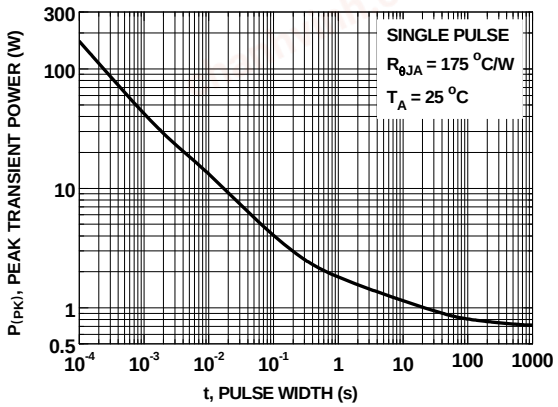


Figure 10. Single Pulse Maximum Power Dissipation

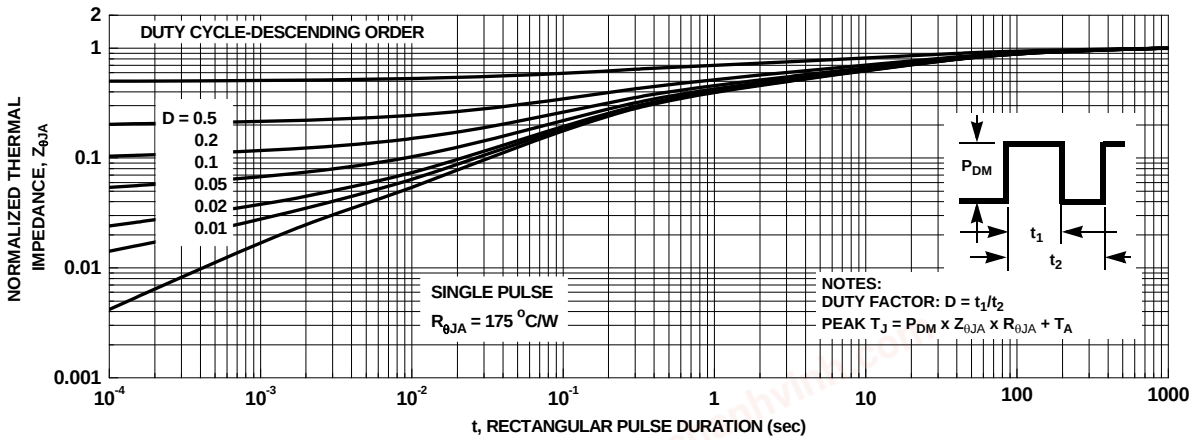
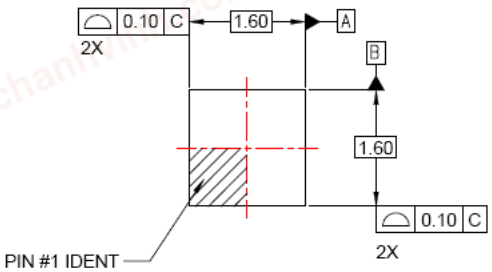


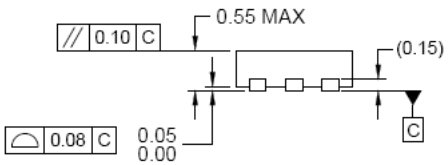
Figure 11. Junction-to-Ambient Transient Thermal Response Curve

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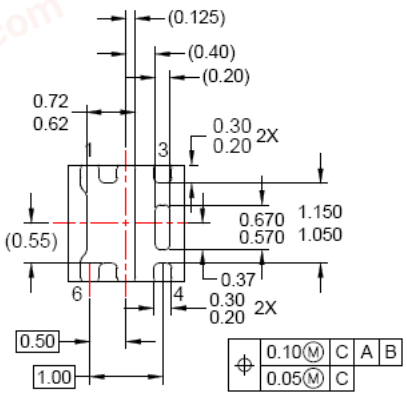
Dimensional Outline and Pad Layout

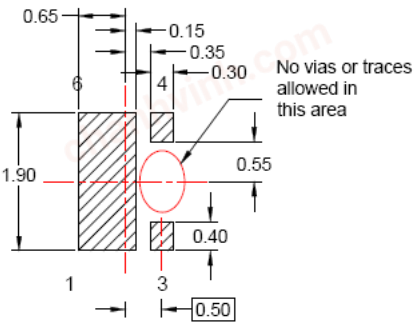


TOP VIEW

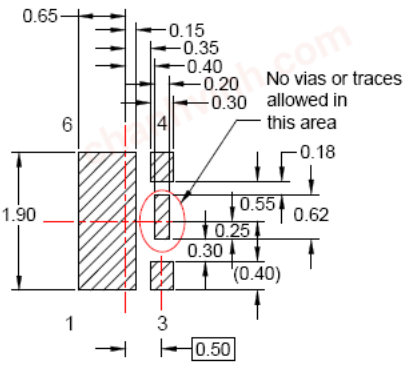


SIDE VIEW





RECOMMENDED LAND PATTERN OPT 1



RECOMMENDED LAND PATTERN OPT 2

NOTES:

A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

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