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PXN012-100QS

N-channel 100 V, 12 mOhm, standard level Trench MOSFET in MLPAK33

21 September 2023 Product data sheet

1. General description

General purpose MOSFET for standard applications, 50 A, standard level N-channel enhancement mode Power MOSFET in MLPAK33 package.

2. Features and benefits

- Standard level compatibility
- Trench MOSFET technology
- Thermally efficient package in a small form factor (3.3 mm x 3.3 mm footprint)

3. Applications

- Secondary side synchronous rectification
- DC-to-DC converters
- Home appliance
- Motor drive
- Load switching
- LED lighting

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C		-	-	100	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	-	50	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	58	W
T_j	junction temperature			-55	-	150	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A; T_j = 25 °C; Fig. 9		-	10.6	12	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 10 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 11; Fig. 12		-	5.5	-	nC
$Q_{G(tot)}$	total gate charge			-	22	-	nC
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 23.2 A; V_{sup} ≤ 100 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	[1]	-	-	53.8	mJ

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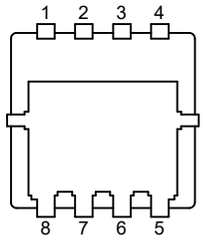
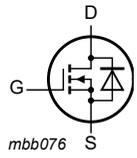
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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Source-drain diode							
Q_r	recovered charge	I_S = 10 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V; T_j = 25 °C; Fig. 15	[2]	-	27	-	nC

[1] Protected by 100% test
[2] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 MLPAK33 (SOT8002-1)	
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PXN012-100QS	MLPAK33	plastic thermal enhanced surface mounted package; mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-1

7. Marking

Table 4. Marking codes

Type number	Marking code
PXN012-100QS	7AN

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C		-	100	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	58	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	50	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	32	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	201	A
T_{stg}	storage temperature			-55	150	°C

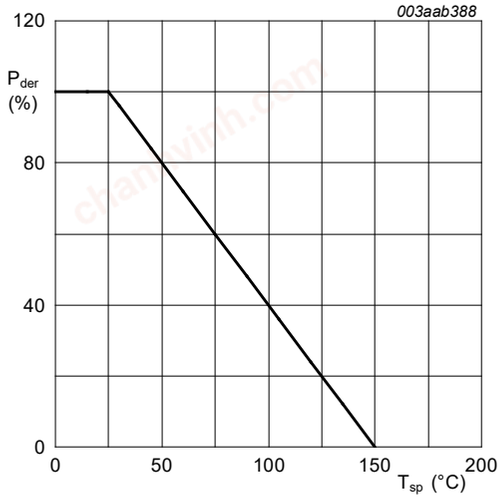
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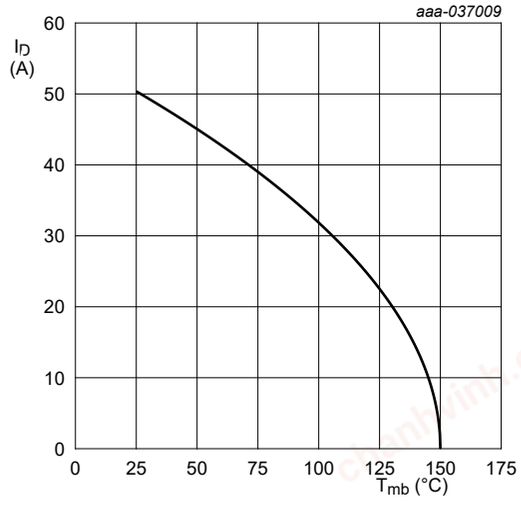
Symbol	Parameter	Conditions		Min	Max	Unit
T_j	junction temperature			-55	150	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	48	A
I_{SM}	peak source current	pulsed; $t_p \leq$ 10 µs; T_{mb} = 25 °C		-	201	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 23.2 A; $V_{sup} \leq$ 100 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	[1]	-	53.8	mJ
I_{AS}	non-repetitive avalanche current	$T_{j(init)}$ = 25 °C	[1]	-	23.2	A

[1] Protected by 100% test



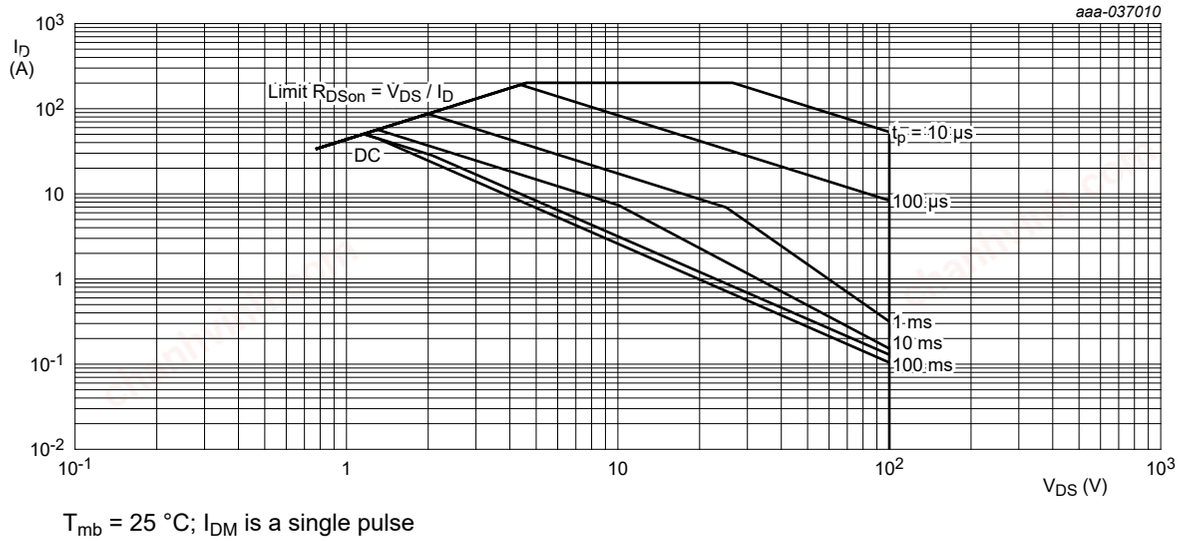
$$P_{der} = \frac{P_{tot}}{P_{tot(25\,°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



$V_{GS} \geq$ 10 V

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

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9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	1.79	2.15	K/W

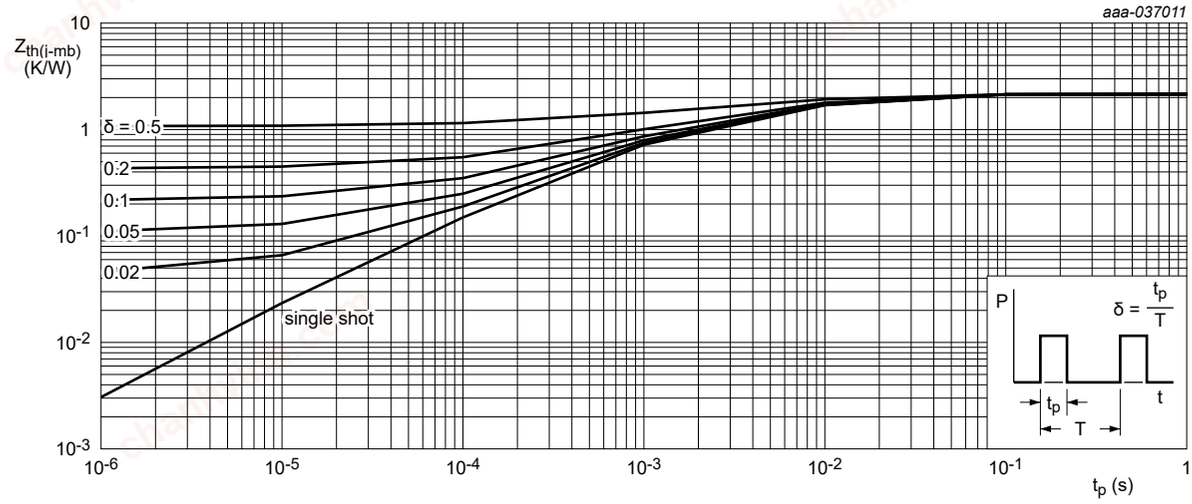


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		100	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		-	100	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 0.25 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 8		2	3	4	V
		I_D = 0.25 mA; V_{DS}=V_{GS}; T_j = 150 °C		-	1.8	-	V
		I_D = 0.25 mA; V_{DS}=V_{GS}; T_j = -55 °C		-	3.6	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T_j ≤ 150 °C		-	-9.2	-	mV/K
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C		-	0.01	1	µA
		V_{DS} = 100 V; V_{GS} = 0 V; T_j = 150 °C		-	9	-	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A; T_j = 25 °C; Fig. 9		-	10.6	12	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 150 °C; Fig. 10		-	-	23	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		-	1	-	Ω

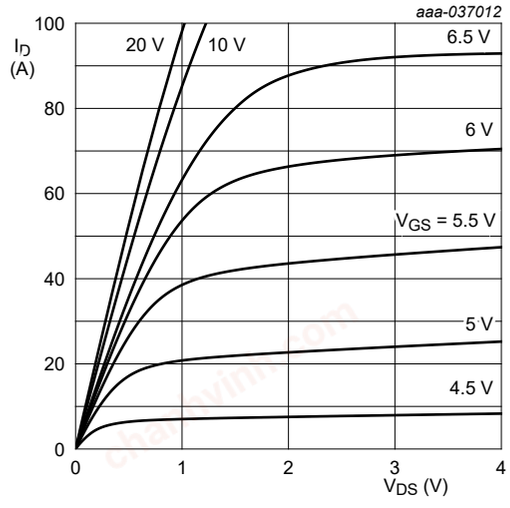
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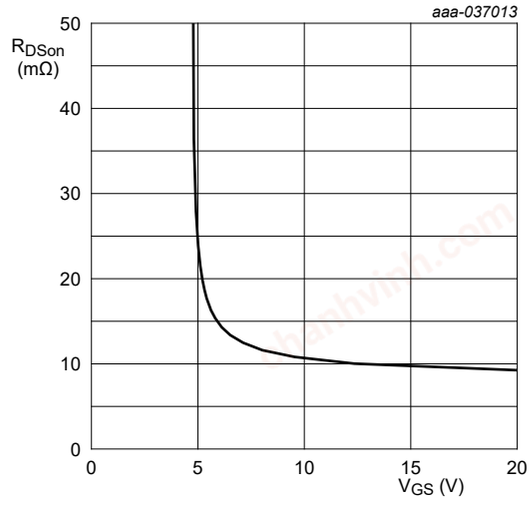
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 10 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 11; Fig. 12		-	22	-	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V; T_j = 25 °C		-	11	-	nC
Q_{GS}	gate-source charge	I_D = 10 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 11; Fig. 12		-	6	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	3.8	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	2.1	-	nC
Q_{GD}	gate-drain charge			-	5.5	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 10 A; V_{DS} = 50 V; T_j = 25 °C; Fig. 11; Fig. 12		-	4.6	-	V
C_{iss}	input capacitance	V_{DS} = 50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 13		-	1313	-	pF
C_{oss}	output capacitance			-	456	-	pF
C_{rss}	reverse transfer capacitance			-	16	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 50 V; R_L = 5 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	6.7	-	ns
t_r	rise time			-	5.8	-	ns
$t_{d(off)}$	turn-off delay time			-	14	-	ns
t_f	fall time			-	9.7	-	ns
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz; T_j = 25 °C		-	35	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 10 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 14		-	0.83	1.2	V
t_{rr}	reverse recovery time	I_S = 10 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V; T_j = 25 °C; Fig. 15		-	33	-	ns
Q_r	recovered charge		[1]	-	27	-	nC

[1] includes capacitive recovery



T_j = 25 °C

Fig. 5. Output characteristics; drain current as a function of drain-source voltage; typical values



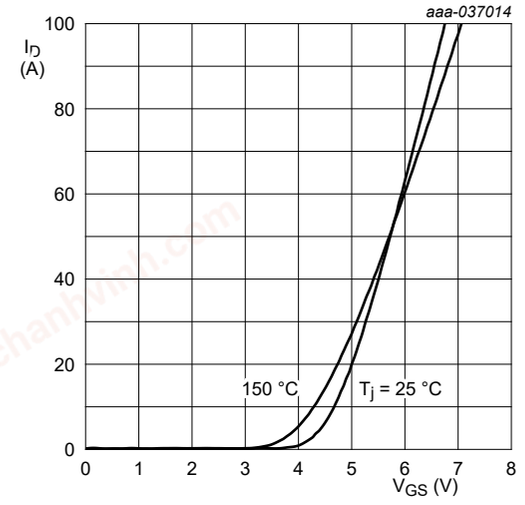
T_j = 25 °C; I_D = 10 A

Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

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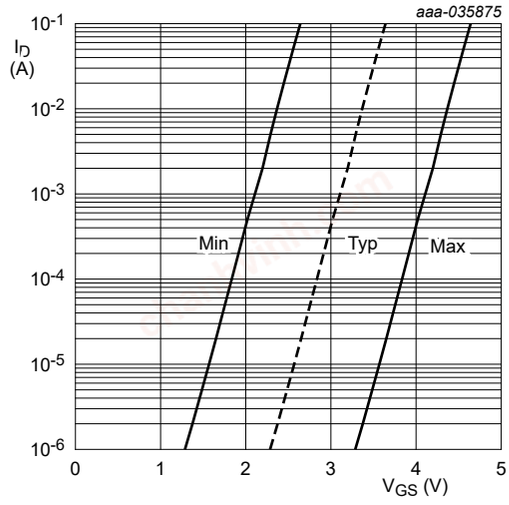
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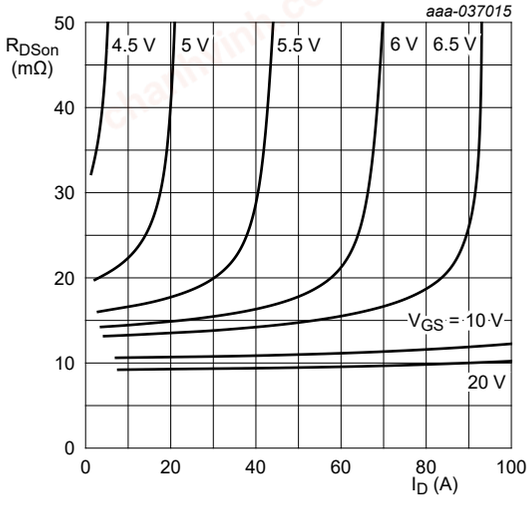
V_{DS} = 8 V

Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values



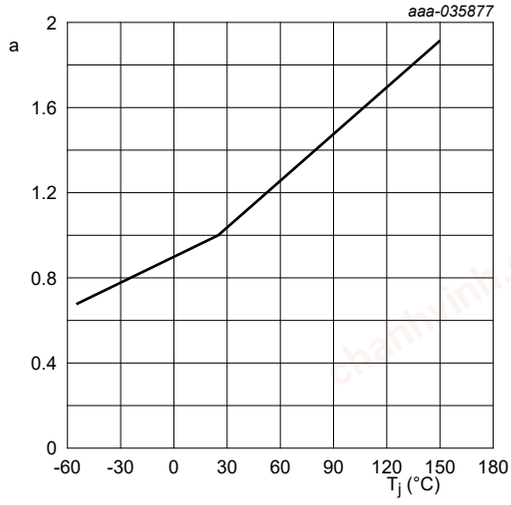
T_j = 25 °C; V_{DS} = 5 V

Fig. 8. Sub-threshold drain current as a function of gate-source voltage



T_j = 25 °C

Fig. 9. Drain-source on-state resistance as a function of drain current; typical values



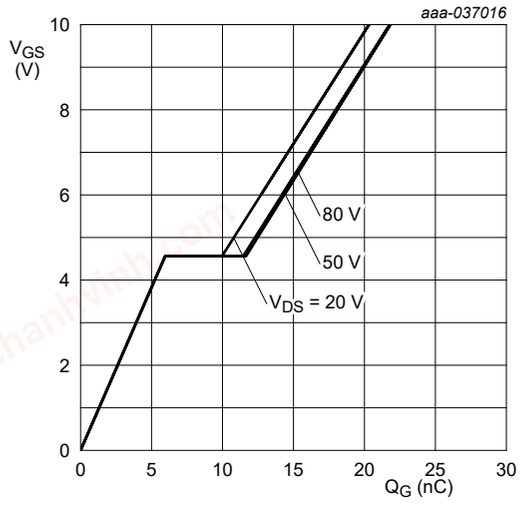
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

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T_j = 25 °C; I_D = 10 A

Fig. 11. Gate-source voltage as a function of gate charge; typical values

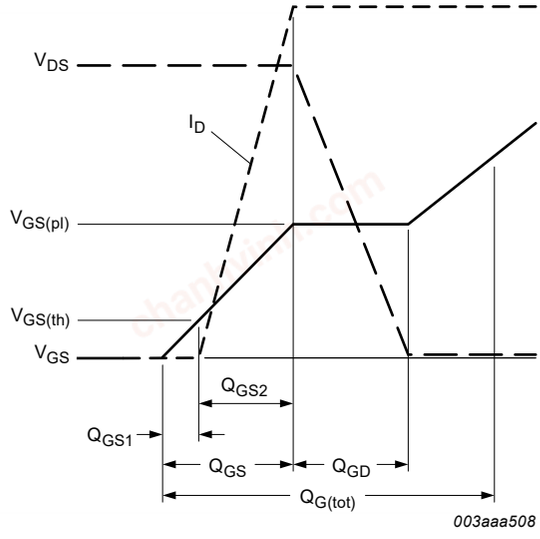
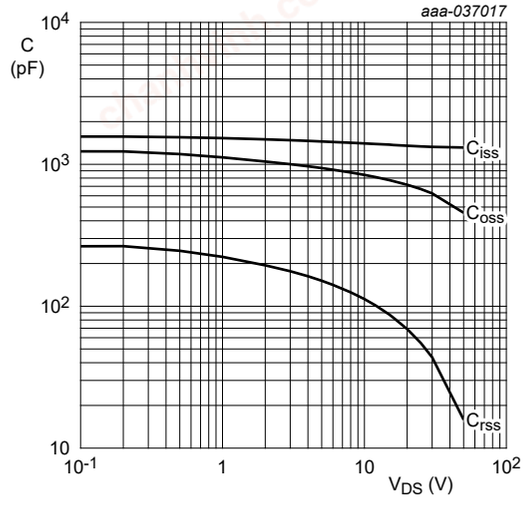
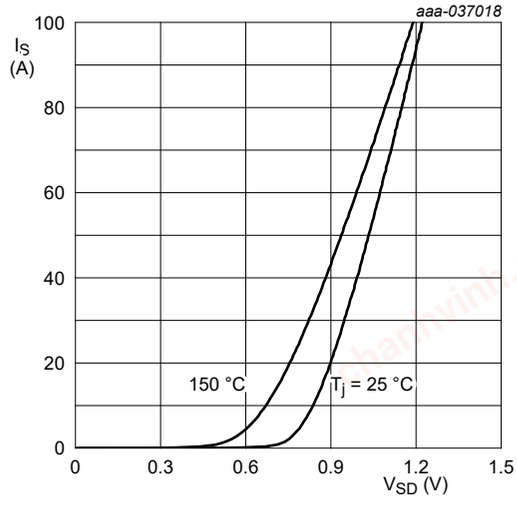


Fig. 12. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{GS} = 0 V

Fig. 14. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

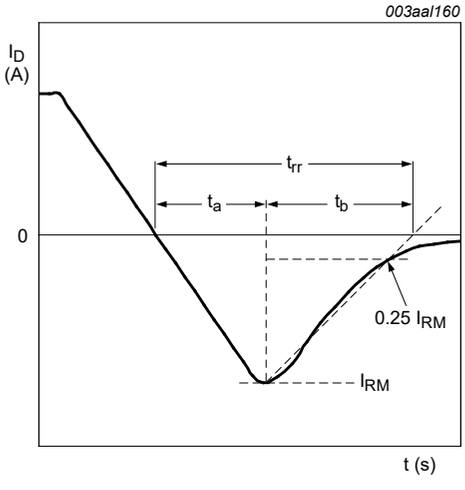


Fig. 15. Reverse recovery timing definition

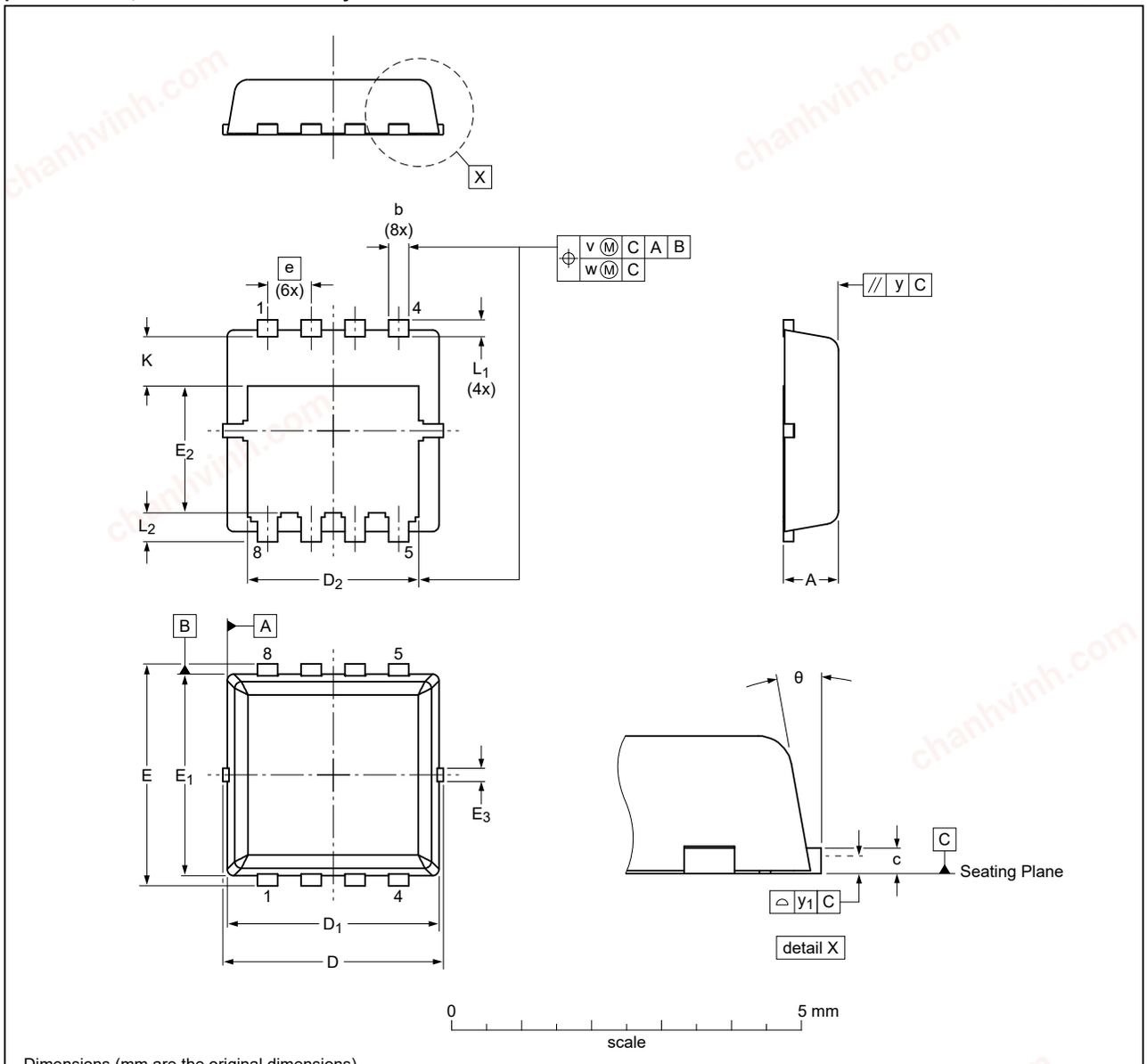
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11. Package outline

MLPAK33: plastic thermal enhanced surface mounted package; mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body **SOT8002-1**



Dimensions (mm are the original dimensions)

Unit		A	b	c	D	D_1	D_2	e	E	E_1	E_2	E_3	K	L_1	L_2	θ	y	y_1	v	w
mm	max	0.90	0.35	0.18	3.50	3.25	2.65	0.65	3.50	3.10	1.99	0.25	0.65 (ref)	0.40	0.58	12°	0.05	0.05	0.1	0.05
	nom	0.80	0.30	0.15	3.30	3.15	2.55		3.30	3.00	1.89	0.20		0.25	0.43	10°				
	min	0.70	0.25	0.12	3.10	3.05	2.45		3.10	2.90	1.79	0.15		0.10	0.28	8°				

sot8002-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	EIAJ			
SOT8002-1						~~20-01-19~~ 23-05-17

Fig. 16. Package outline MLPAK33 (SOT8002-1)

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12. Soldering

Footprint information for reflow soldering of MLPAK33 package **SOT8002-1**

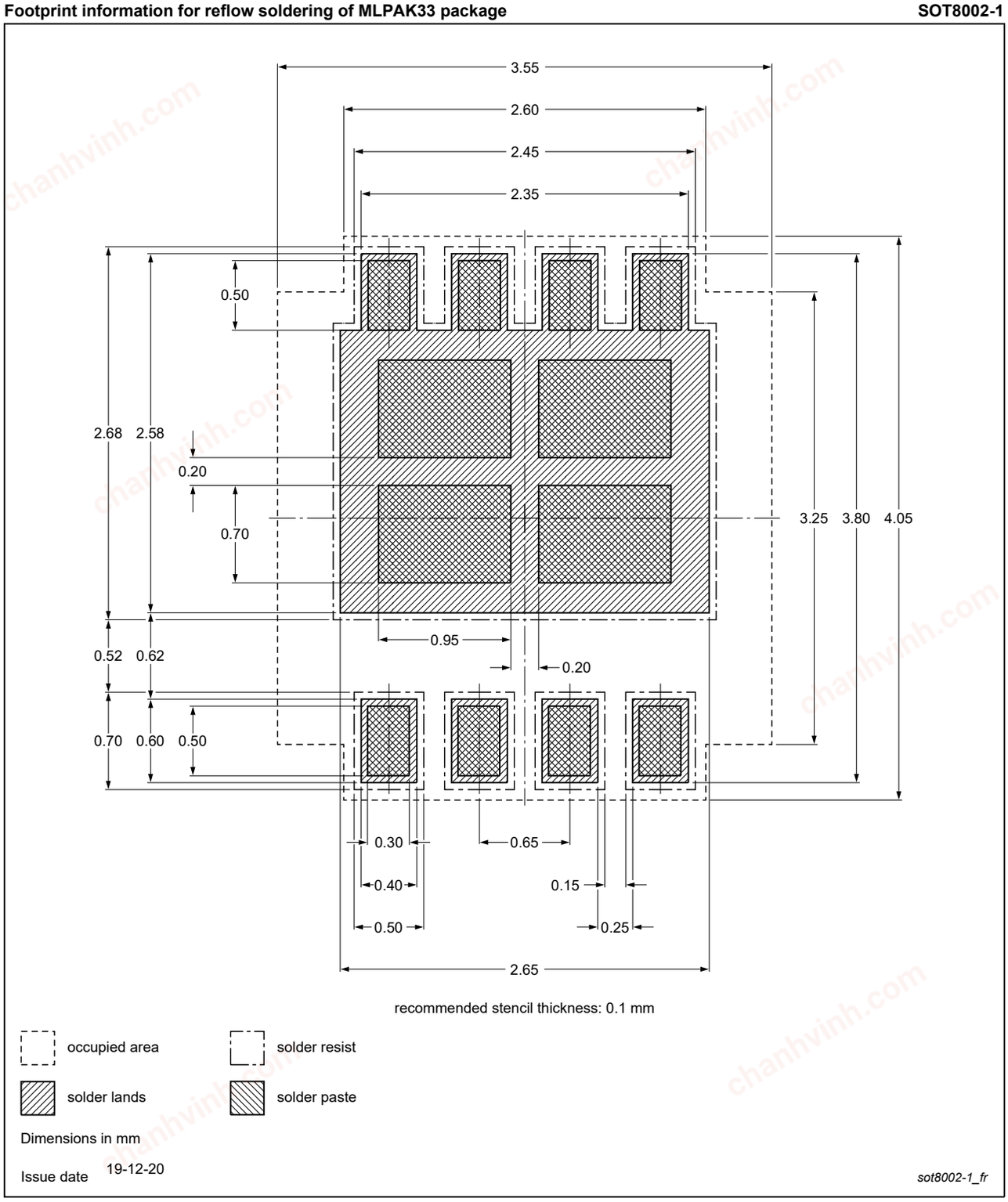


Fig. 17. Reflow soldering footprint for MLPAK33 (SOT8002-1)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Contents

1. General description....1
2. Features and benefits....1
3. Applications....1
4. Quick reference data....1
5. Pinning information....2
6. Ordering information....2
7. Marking....2
8. Limiting values....2
9. Thermal characteristics....4
10. Characteristics....4
11. Package outline....8
12. Soldering....9
13. Legal information....10

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Date of release: 21 September 2023