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NXT4556

SIM card interface level translator

Rev. 2 — 15 June 2022 Product data sheet

1. General description

The NXT4556 device is built for interfacing a SIM card with a single low-voltage host side interface. The NXT4556 has three level translators to convert the data, RST and CLK signals between a SIM card and a host microcontroller. A high speed level translation capable of supporting class-B, class-C SIM cards. V_{CC_SIM} power-down initiates a shutdown sequence on SIM card pins in accordance with ISO-7816-3.

The NXT4556 is compliant with all ETSI, IMT-2000 and ISO-7816 SIM/Smart card interface requirements.

2. Features and benefits

- Support SIM cards and eSIM with supply voltages 1.62 V to 3.3 V
- Host micro-controller operating voltage range: 1.08 V to 1.98 V
- Automatic level translation of I/O, RST and CLK between SIM card and host side interface with capacitance isolation
- Incorporates shutdown feature for the SIM card signals according to ISO-7816-3
- High $V_{dis(UVLO_AC)}$ switching level, arranging quick shut down when V_{CC_SIM} powers down
- Integrated pull-up resistors; no external resistor required
- Integrated EMI Filters suppresses higher harmonics of digital I/O's
- Low current shutdown mode < 1 µA
- Supports clock speed beyond 5 MHz clock
- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 exceeds 2 kV
  - CDM ANSI/ESDA/JEDEC JS-002 exceeds 1 kV
  - IEC61000-4-2 level 4, contact and air discharge on all SIM card-side pins exceeds 8 kV and 15 kV
- Available in 9-pin wafer level chip-scale package (WLCSP); 9 bumps; 1.06 mm x 1.06 mm x 0.43 mm body; 0.35 mm pitch

3. Applications

- NXT4556 can be used with a range of SIM card attached devices including:
  - Mobile and personal phones
  - Wireless modems
  - SIM card terminals

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4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NXT4556UP	-40 °C to +85 °C	WLCSP9	wafer level chip-scale package; 9 bumps; 1.06 × 1.06 × 0.43 mm body	SOT8027-1

5. Marking

Table 2. Marking

Type number	Marking code[1]
NXT4556UP	z6

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

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6. Functional diagram

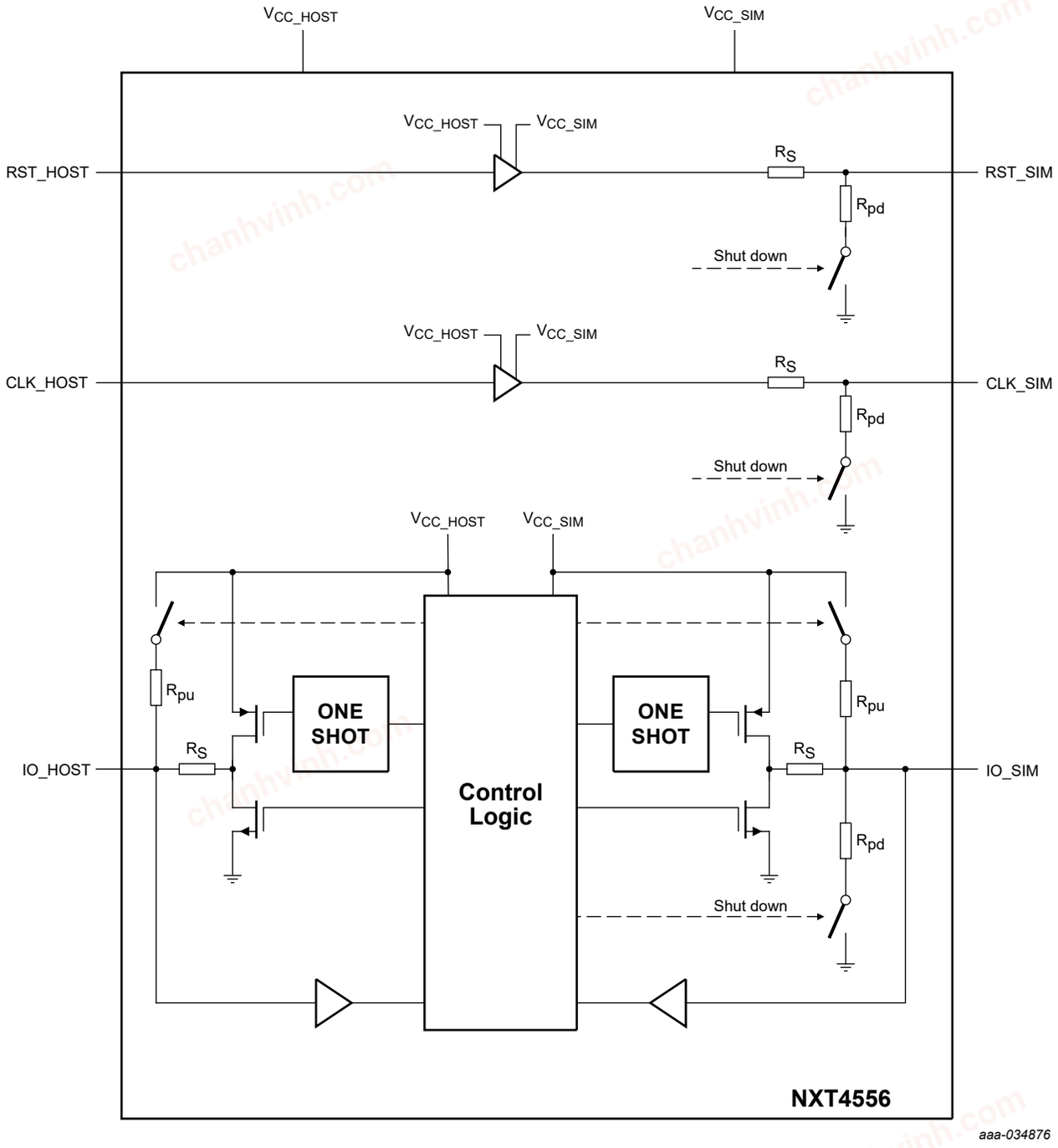


Fig. 1. Functional diagram

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7. Pinning information

7.1. Pinning

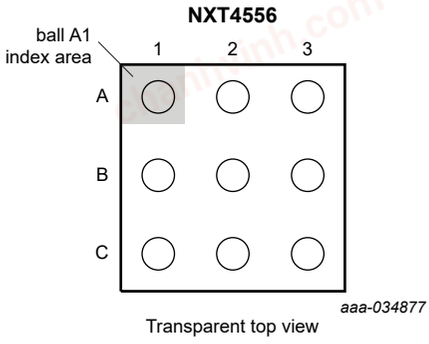


Fig. 2. Bump configuration for SOT8027-1 (WLCSP9)

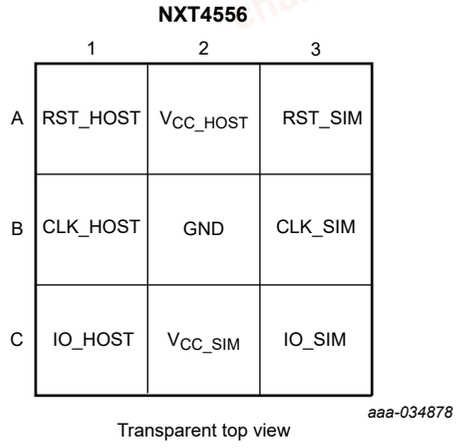


Fig. 3. Bump mapping for SOT8027-1 (WLCSP9)

7.2. Pin description

Table 3. Pin description

Symbol	Bump	Type	Description
RST_HOST	A1	I	Reset input from host controller.
V_{CC_HOST}	A2	power	Supply voltage for the host controller side input/output pins (CLK_HOST, RST_HOST, IO_HOST). This pin should be bypassed with a 0.1 µF ceramic capacitor close to the pin.
RST_SIM	A3	O	Reset output pin for the SIM card.
CLK_HOST	B1	I	Clock input from host controller.
GND	B2	ground	Ground for the SIM card and host controller. Proper grounding and bypassing are required to meet ESD specifications.
CLK_SIM	B3	O	Clock output pin for the SIM card.
IO_HOST	C1	I/O	Host controller bidirectional data input/output. This pin can be driven from push-pull as well as open-drain drivers.
V_{CC_SIM}	C2	power	Supply voltage for the SIM CARD side input/output pins. This input voltage ranges from 1.62 V to 3.3 V. This pin should be bypassed with a 0.1 µF ceramic capacitor close to the pin.
IO_SIM	C3	I/O	SIM card bidirectional data input/output. The SIM card output must be on an open-drain driver.

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8. Functional description

8.1. Functional behavior

The functional diagram of the NTX4556 is shown in Fig. 1.

The upper part of Fig. 1 shows the RST and CLK channels which are uni-directional level shifters from the host to the SIM card side.

The bottom part shows the architecture of the bidirectional I/O channel. Both on IO_HOST and IO_SIM a resistor R_{pu} pulls up the I/O node. On both sides an output stage is present that consists of a PMOST and an NMOST device. Each output stage drives the output through a series resistor R_S. Input stages sense the I/O nodes and pass LOW/HIGH information to the control logic that controls the translator outputs and several pull-up and pull-down resistors.

The NXT4556 I/O channel does not require a dedicated input signal to control the direction of data flow from IO_HOST to IO_SIM or from IO_SIM to IO_HOST. Change in driving direction is possible when both sides are at HIGH state. The control logic recognizes the I/O node with the first falling edge and grants control over the opposite I/O node. When for example the IO_HOST is turned LOW, the control circuit will turn on the NMOST on the IO_SIM side, pulling LOW IO_SIM. The IO_SIM pin is then an output only, until IO_HOST is turned HIGH and the translator has turned IO_SIM HIGH again.

The PMOST devices are used to actively turn high the outputs. Each PMOST is driven by a one-shot circuit that generates a pulse. For example: Assuming HOST to SIM communication, when the IO_HOST is turned HIGH, it will activate the one shot circuit on the IO_SIM side. A pulse starts, arranging a fast LOW to HIGH transition on IO_SIM. When the pulse has finished, the PMOST is released. At that stage, the system returns to a standard open drain state whereby the pull resistors keep the I/O nodes HIGH.

At the same time, at a LOW to HIGH transition, the one shot on the input side is activated as well. In an open drain application, this creates a typical input LOW to HIGH waveform. Fig. 4 shows an example of a LOW to HIGH transition in an open drain application.

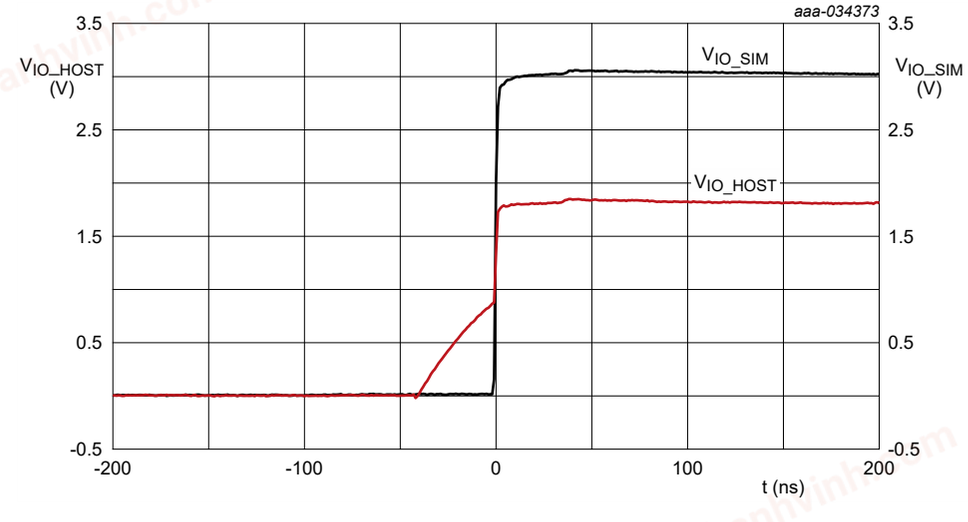


Fig. 4. LOW to HIGH transition for IO_HOST to IO_SIM communication

Looking at the input signal, the first part of the LOW to HIGH transition is an exponential curve caused by the I/O node capacitance being charged via the pull-up resistor. The second part starts when the input signal crosses the input switching level. The rising edge is accelerated dramatically by the PMOST that is turned on by the one shot on the input side.

In case of a communication error or some other unforeseen incident that may drive both connected sides of the drivers at the same time, the internal logic automatically prevents stuck-at situation. This ensures that both I/Os will return to HIGH level once released from being driven LOW.

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In shut down mode, the control circuit disables all output stages. Additionally, in shut down mode, the pull-up resistor on IO_SIM side is disabled, and all pull-down resistors R_{pd} on SIM side are enabled, pulling LOW the pins on the SIM side. The shut down sequence is explained in more detail in Section 8.3.

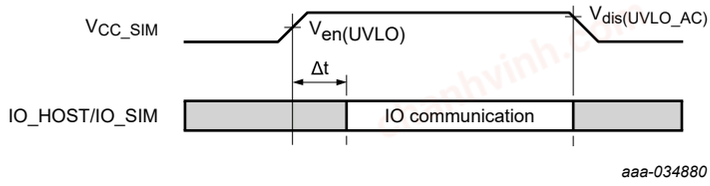
8.2. Window of I/O communication

When the translator is in operating mode, I/O communication can take place through the I/O channel. Communication can take place in both directions IO_HOST ↔ IO_SIM. Additionally, during operating mode, the RST_HOST and CLK_HOST signals are passed to RST_SIM and CLK_SIM respectively.

The translator is active when V_{CC_HOST} and V_{CC_SIM} are at a proper level. Fig. 5 shows how V_{CC_SIM} controls the translator mode. V_{CC_HOST} is assumed to be default present and is not shown in the waveform.

When V_{CC_SIM} has turned HIGH, I/O communication can commence after a certain amount of time: $\Delta t > 300$ ns.

It is assumed that during the power up sequence, the nodes of IO_HOST and and IO_SIM are not pulled down by the host controller and the SIM card. The translator has integrated pull-up resistors and will turn HIGH both IO_HOST and IO_SIM. The pull-up resistors R_{pu} are pointed out in Fig. 1.



Δt > 300 ns

Fig. 5. Timing window for I/O communication

When V_{CC_SIM} drops below $V_{dis(UVLO)}$, the translator turns to shutdown mode. Section 8.3 illustrates the shutdown sequence in more detail.

8.3. Shutdown sequence

The ISO 7816-3 specification specifies the shutdown sequence for the SIM card signals to ensure that the card is properly disabled for power savings. Also, during hot swap, the orderly shutdown of these signals helps to avoid any improper write and corruption of data.

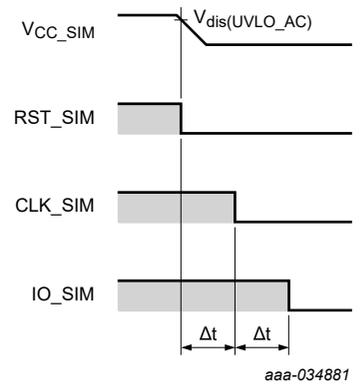
When V_{CC_SIM} drops below $V_{dis(UVLO_AC)}$, the shutdown sequence is initiated. Fig. 6 illustrates the shutdown sequence initiated by V_{CC_SIM} being powered down.

The shut down sequence starts by pulling down the RST_SIM output. Once RST_SIM is turned LOW, CLK_SIM and IO_SIM are pulled LOW sequentially, one-by-one. Internal pull-down resistors on the SIM pins are used to pull the SIM channels LOW. The internal pull-down resistors, R_{pd}, that pull down the three pins on the SIM side are shown in Fig. 1. The shutdown sequence is completed in a few microseconds. The interval time (Δt), is typically 4 µs.

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Δt = 4 µs (typical)

The shaded areas indicate that the signals are HIGH or LOW.

Fig. 6. Shutdown sequence for RST_SIM, CLK_SIM and IO_SIM of NXT4556 SIM card translator

8.4. UVLO

When V_{CC_SIM} drops below $V_{dis(UVLO_AC)}$, the translator goes to shut down mode. This is illustrated in Fig. 5. The switching level $V_{dis(UVLO_AC)}$ has a high value of approximately 86 %xV_{CC_SIM}. The circuitry uses an AC detection mechanism that operates accurately with a falling slope that is typical in the SIM card application. Next to this AC detection, a standard UVLO detection is in place that has no condition with respect to the slope of the rising or falling V_{CC_SIM}. For the standard UVLO, the parameters $V_{en(UVLO)}$ and $V_{dis(UVLO)}$ are involved which have lower values than $V_{dis(UVLO_AC)}$. When V_{CC_SIM} is powered up, the translator is enabled when V_{CC_SIM} crosses $V_{en(UVLO)}$. This is illustrated in Fig. 5.

8.5. EMI filter

All output driver stages of I/O, RST and CLK channels are equipped with EMI filters to reduce interference towards sensitive mobile communication.

8.6. ESD protection

The device has robust ESD protections on all SIM card pins. The architecture prevents any stress for the host: the voltage translator discharges any stress to supply ground.

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9. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	SIM card side; IEC 61000-4-2; level 4; contact discharge	-	±8	kV
		SIM card side; IEC 61000-4-2; level 4; air discharge	-	±15	kV
		all other pins; IEC 61000-4-2; level 4	-	±2	kV
		all other pins; HBM [1]	-	±2	kV
		all other pins; CDM [2]	-	±1	kV
V_{CC_HOST}	supply voltage		GND - 0.5	4.6	V
V_{CC_SIM}	SIM card supply voltage		GND - 0.5	4.6	V
V_I	input voltage	CLK_HOST; input signal voltage, HOST side	GND - 0.5	4.6	V
		RST_HOST; input signal voltage, HOST side	GND - 0.5	4.6	V
		IO_HOST; input signal voltage, HOST side	GND - 0.5	4.6	V
		CLK_SIM; input signal voltage, SIM side	GND - 0.5	4.6	V
		RST_SIM; input signal voltage, SIM side	GND - 0.5	4.6	V
		IO_SIM; input signal voltage, SIM side	GND - 0.5	4.6	V
T_{stg}	storage temperature		-55	+125	°C

[1] Human Body Model (HBM) according to JESD22-A-A114.
[2] Charged-Device Model (CDM) according to JESD22-C101.

10. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC_HOST}	supply voltage	[1]	1.08	-	1.98 V	V
V_{CC_SIM}	card side supply voltage	[1]	1.62	-	3.3	V
V_I	input voltage	HOST side	-0.3	-	V_{CC_HOST} + 0.3	V
		SIM side	-0.3	-	V_{CC_SIM} + 0.3	V
T_{amb}	ambient temperature		-40	+25	+85	°C

[1] $V_{CC_SIM} \geq V_{CC_HOST}$

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11. Electrical characteristics

Table 6. Electrical characteristics

1.08 V ≤ V_{CC_HOST} ≤ 1.98 V; 1.62 V ≤ V_{CC_SIM} ≤ 3.3 V; GND = 0 V; unless otherwise specified.

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
I_{CC_HOST}	supply current	operating mode; f_{clk} = 1 MHz; IO_HOST = IO_SIM = HIGH [2]	-	5	10	µA
		shutdown mode; IO_HOST = HIGH [3]	-	-	1	µA
I_{CC_SIM}	card side supply current	operating mode; IO_HOST = IO_SIM = HIGH; CLK_HOST = RST_HOST = LOW [2]	-	2	8	µA
$V_{en(UVLO)}$	undervoltage lockout enable voltage	V_{CC_SIM} rising; V_{CC_HOST} = 1.8 V	0.85	1.2	1.6	V
$V_{dis(UVLO)}$	undervoltage lockout disable voltage	V_{CC_SIM} falling; V_{CC_HOST} = 1.8 V	0.65	1.0	1.3	V
$V_{dis(UVLO_AC)}$	undervoltage lockout disable voltage	V_{CC_SIM} falling;				
		-dV/dt = 0.9 V/ms to 9 V/ms; V_{CC_SIM} = 1.8 V	-	1.55	-	V
		-dV/dt = 1.5 V/ms to 15 V/ms; V_{CC_SIM} = 3.0 V	-	2.58	-	V
		-dV/dt = 0.9 V/ms to 9 V/ms; V_{CC_SIM} = 1.71 V to 1.89 V	-	$0.86V_{CC_SIM}$	-	V
		-dV/dt = 1.5 V/ms to 15 V/ms; V_{CC_SIM} = 2.85 V to 3.15 V	-	$0.86V_{CC_SIM}$	-	V

[1] Typical values measured at 25 °C.
[2] Internal pull-up resistance active on IO_HOST and IO_SIM
[3] Internal pull-up resistance active on IO_HOST

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Table 7. Static characteristics

1.08 V ≤ V_{CC_HOST} ≤ 1.98 V; 1.62 V ≤ V_{CC_SIM} ≤ 3.3 V; GND = 0 V; unless otherwise specified.

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
Level shifter						
V_{IH}	HIGH-level input voltage	RST_HOST, CLK_HOST [2]	$0.65V_{CC_HOST}$	-	V_{CC_HOST} + 0.3	V
		IO_HOST	$0.5V_{CC_HOST}$	-	V_{CC_HOST} + 0.3	V
		IO_SIM [2]	$0.5V_{CC_SIM}$	-	V_{CC_SIM} + 0.3	V
V_{IL}	LOW-level input voltage	RST_HOST, CLK_HOST [2]	-0.3	-	$0.35V_{CC_HOST}$	V
		IO_HOST [2]	-0.3	-	$0.3V_{CC_HOST}$	V
		IO_SIM [2]	-0.3	-	$0.25V_{CC_SIM}$	V
R_{pu}	pull-up resistance	IO_SIM connected to V_{CC_SIM}	3.3	5.3	7.3	kΩ
		IO_HOST connected to V_{CC_HOST}	2.8	4.3	6	kΩ
V_{OH}	HIGH-level output voltage	RST_SIM, CLK_SIM; I_{OH} = -1 mA	$0.85V_{CC_SIM}$	-	V_{CC_SIM}+0.3	V
		IO_SIM; I_{OH} = -10 µA	$0.85V_{CC_SIM}$	-	V_{CC_SIM}+0.3	V
		IO_HOST; I_{OH} = -10 µA	$0.85V_{CC_HOST}$	-	V_{CC_HOST}+0.3	V
V_{OL}	LOW-level output voltage	RST_SIM, CLK_SIM; I_{OL} = 1 mA	-	50	200	mV
		IO_SIM; I_{OL} = 1 mA	-	50	300	mV
		IO_HOST; I_{OL} = 1 mA	-	50	300	mV
R_{pd}	pull-down resistance	CLK_SIM, RST_SIM, IO_SIM	-	400	-	Ω
EMI filter						
R_S	series resistance	IO_SIM	-	44	-	Ω
		RST_SIM	-	44	-	Ω
		CLK_SIM	-	44	-	Ω
C_{io}	input/output capacitance	IO_SIM	-	10	-	pF
		RST_SIM	-	10	-	pF
		CLK_SIM	-	10	-	pF

[1] Typical values measured at 25 °C.
[2] V_{IL}, V_{IH} depend on the individual supply voltage per interface.

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Table 8. Dynamic characteristics

Push-pull: test circuit see Fig. 8; C_L = 50 pF.
Open-drain: test circuit see Fig. 9; C_{IO_HOST} = 10 pF; C_{IO_SIM} = 30 pF.
For waveform see Fig. 7.

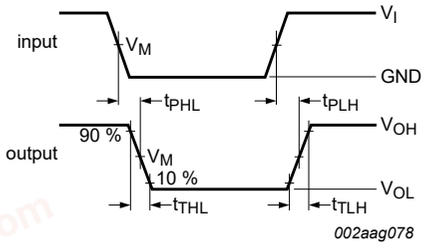
Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C;						Unit
			V_{CC_SIM} = 1.8 V ± 0.18 V			V_{CC_SIM} = 3.0 V ± 0.3 V			
			Min	Typ[1]	Max	Min	Typ[1]	Max	
V_{CC_HOST} = 1.2 V ± 0.12 V									
t_{pd}	propagation delay	I/O channel; push-pull [2]	-	12	20	-	12	20	ns
		I/O channel; open-drain	-	15	25	-	15	25	ns
		CLK and RST channels; push-pull	-	12	20	-	12	20	ns
t_t	transition time	IO_HOST; push-pull [3]	-	-	10	-	-	10	ns
		IO_SIM; RST_SIM; CLK_SIM; push-pull	-	-	10	-	-	10	ns
t_{sk}	skew time	between channels IO_SIM and CLK_SIM; push-pull	-	2	-	-	2	-	ns
f_{clock}	clock frequency	CLK channel; push-pull [4]	-	-	25	-	-	25	MHz
f_{data}	data rate	I/O channel; push-pull [4]	-	-	5	-	-	5	Mbps
		I/O channel; open-drain; see Fig. 9 [4]	-	-	800	-	-	800	kbps
V_{CC_HOST} = 1.8 V ± 0.18 V									
t_{pd}	propagation delay	I/O channel; push-pull [2]	-	7	12	-	7	12	ns
		I/O channel; open-drain	-	8	15	-	8	15	ns
		CLK and RST channels; push-pull	-	7	12	-	7	12	ns
t_t	transition time	IO_HOST; push-pull [3]	-	-	10	-	-	10	ns
		IO_SIM; RST_SIM; CLK_SIM; push-pull	-	-	10	-	-	10	ns
t_{sk}	skew time	between channels IO_SIM and CLK_SIM; push-pull	-	2	-	-	2	-	ns
f_{clock}	clock frequency	CLK channel; push-pull [4]	-	-	25	-	-	25	MHz
f_{data}	data rate	I/O channel; push-pull [4]	-	-	5	-	-	5	Mbps
		I/O channel; open-drain; see Fig. 9 [4]	-	-	800	-	-	800	kbps

[1] Typical values measured at 25 °C.
[2] t_{pd} is the same as t_{PHL} and t_{PLH}.
[3] t_t is the same as t_{THL} and t_{TLH}.
[4] Criteria: duty cycle between 40% and 60%; Voltage swing between 10% V_{CCI} and 90% V_{CCI}.

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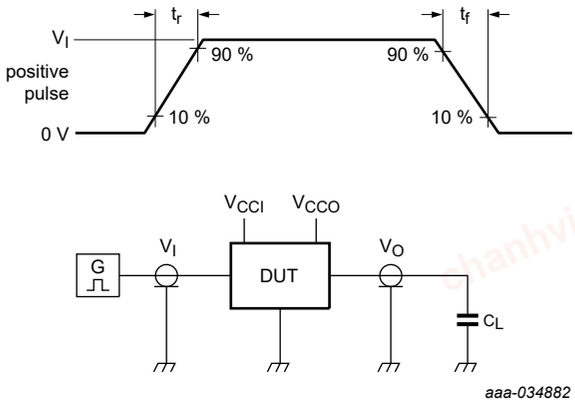
11.1. Waveforms and test circuits



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. Data input to data output propagation delay times



Test data is given in Table 9.

All input pulses are supplied by generators having the following characteristics:

PRR ≤ 10 MHz; Z_O = 50 Ω; t_r, t_f ≤ 2.5 ns.

C_L = Load capacitance including jig and probe capacitance.

V_{CCI} is the supply voltage associated with the input.

V_{CCO} is the supply voltage associated with the output.

Fig. 8. Test circuit for measuring switching times for push-pull drive

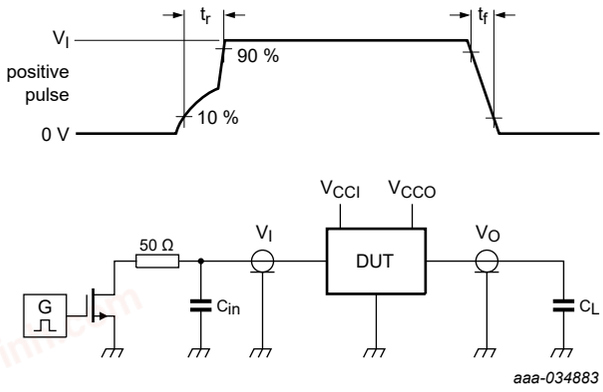
Table 9. Test data for push-pull drive

Supply voltage		Direction	Input		Output	Load
V_{CC_HOST}	V_{CC_SIM}		V_I	V_M	V_M	C_L
1.08 V to 1.98 V	1.62 V to 3.3 V	host side to SIM card side	V_{CC_HOST}	$0.5V_{CC_HOST}$	$0.5V_{CC_SIM}$	50 pF
1.08 V to 1.98 V	1.62 V to 3.3 V	SIM card side to host side	V_{CC_SIM}	$0.5V_{CC_SIM}$	$0.5V_{CC_HOST}$	50 pF

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Test data is given in Table 10.
Pulse generator (G) has the following characteristics: PRR ≤ 10 MHz; Z_O = 50 Ω; t_r, t_f ≤ 2.5 ns.
C_L = Load capacitance including jig and probe capacitance.
V_{CCI} is the supply voltage associated with the input.
V_{CCO} is the supply voltage associated with the output.
Rise time on input pin strongly depends on source impedance, internal pull-up resistor and load capacitance (C_{in}).

Fig. 9. Test circuit for measuring switching times for open drain drive

Table 10. Test data for open drain drive

Supply voltage		Direction	Input		Output	Load	
V_{CC_HOST}	V_{CC_SIM}		V_I	V_M	V_M	C_{in}	C_L
1.08 V to 1.98 V	1.62 V to 3.3 V	host side to SIM card side	V_{CC_HOST}	$0.6V_{CC_HOST}$	$0.6V_{CC_SIM}$	10 pF	30 pF
1.08 V to 1.98 V	1.62 V to 3.3 V	SIM card side to host side	V_{CC_SIM}	$0.5V_{CC_SIM}$	$0.5V_{CC_HOST}$	30 pF	10 pF

12. Application information

The application circuit for the NXT4556, which shows the typical interface with a SIM card, is shown in Fig. 10. Supply decoupling capacitors (100 nF) are recommended and should be placed close to the translator product.

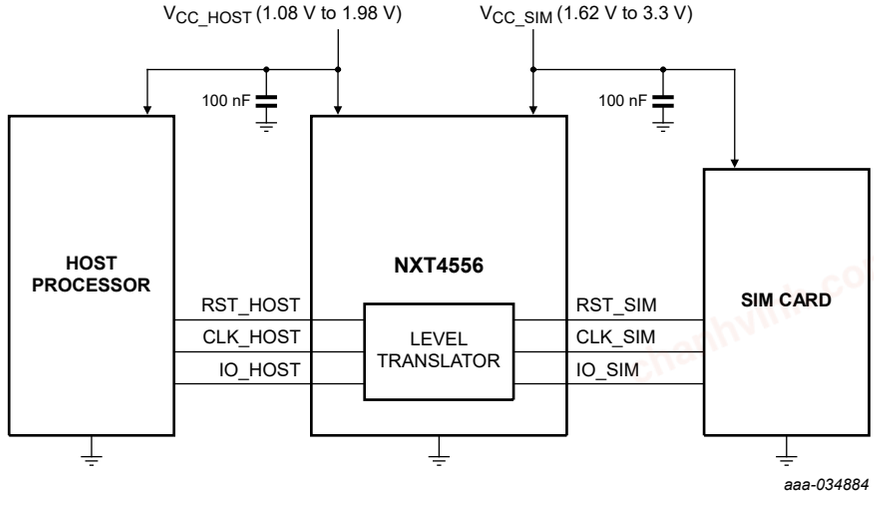


Fig. 10. NXT4556 application circuit interfacing with typical SIM card

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13. Design and assembly recommendations

13.1. PCB design guidelines

For optimum performance, use a Non-Solder Mask PCB Design (NSMD), also known as a copper-definied design, incorporating laser-drilled micro-vias connecting the ground pads to a buried ground-plane layer. This results in the lowest possible ground inductance and provides the best high frequency and ESD performance. For this case, refer to Table 11 for the recommended PCB design parameters.

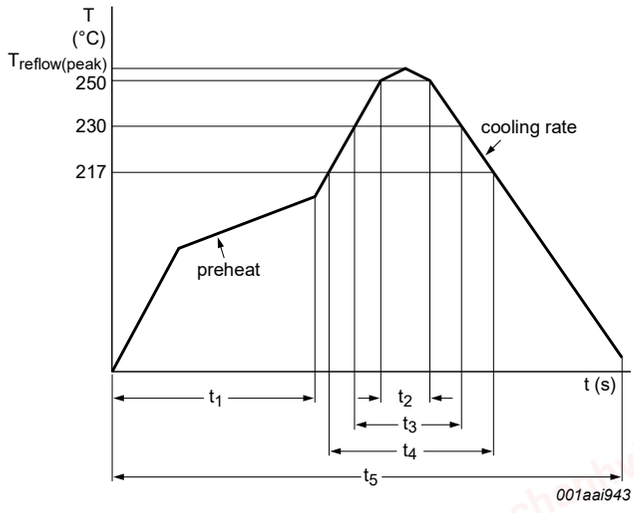
Table 11. Recommended PCB design parameters

Parameter	Value or specification
PCB Cu pad shape	circular
PCB Cu pad diameter	200 µm
PCB solder resist diameter	270 µm
WLCSP pad diameter (UBM)	200 µm

13.2. PCB assembly guidelines for Pb-free soldering

Table 12. Assembly recommendations

Parameter	Value or specification
PCB stencil shape	circular
PCB stencil aperture diameter	200 µm
PCB stencil thickness	80 µm
Solder paste material	$SnAg_4Cu$ (Cu 0.5%) (SAC405)
Solder reflow profile	see Fig. 11



The device can withstand at least three reflows with this profile.

Fig. 11. Pb-free solder reflow profile

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Table 13. Reflow soldering process characteristics

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{reflow(peak)}$	peak reflow temperature		230	-	260	°C
t_1	time 1	soak time	60	-	180	s
t_2	time 2	time during T ≥ 250 °C	-	-	30	s
t_3	time 3	time during T ≥ 230 °C	10	-	50	s
t_4	time 4	time during T ≥ 217 °C	30	-	150	s
t_5	time 5		-	-	540	s
dT/dt	rate of change of temperature	cooling rate	-	-	-6	°C/s
		preheat	2.5	-	4.0	°C/s

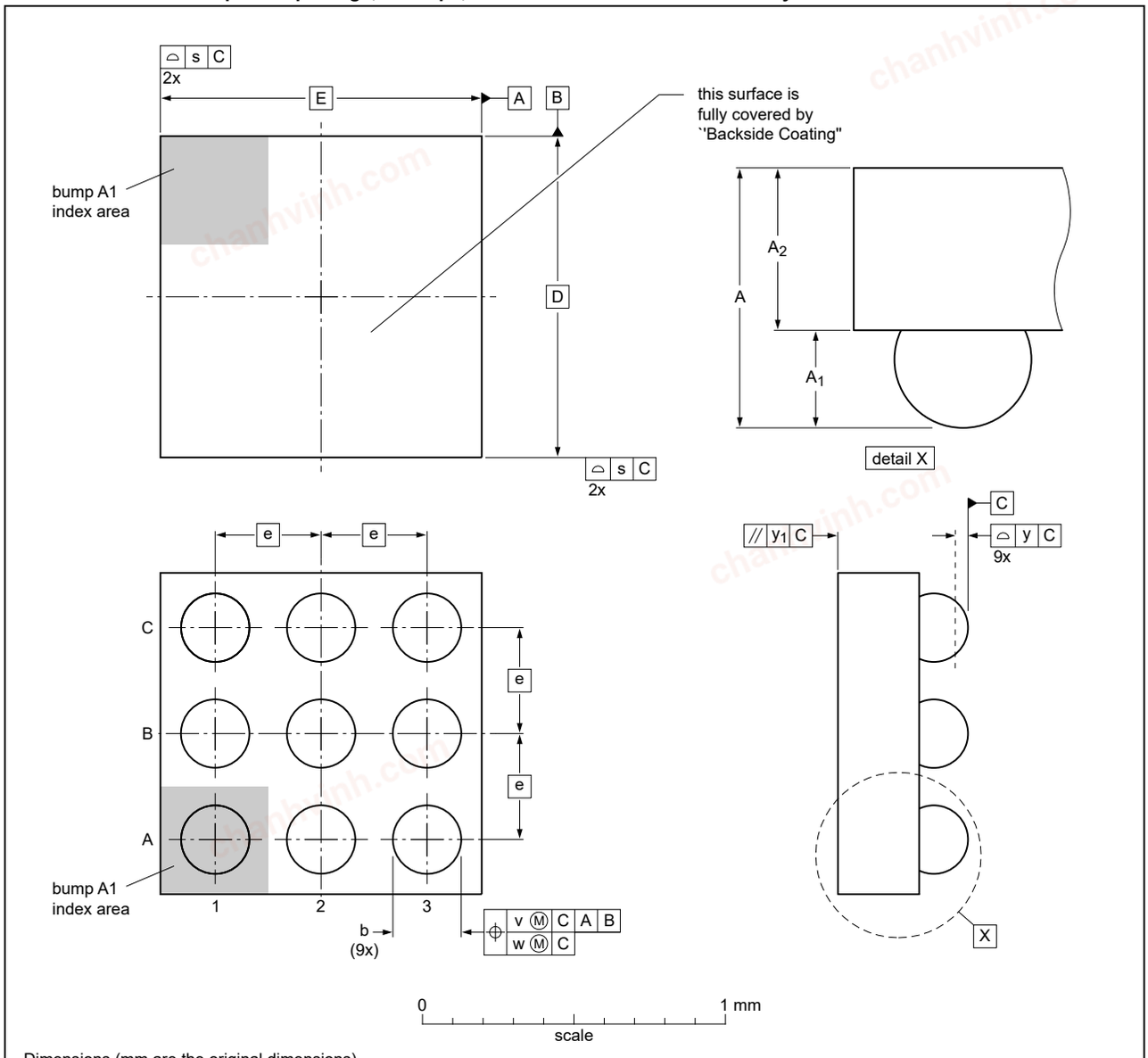
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14. Package outline

WLCSP9: wafer level chip-scale package; 9 bumps; 1.06 mm x 1.06 mm x 0.43 mm body **SOT8027-1**



Dimensions (mm are the original dimensions)

Unit	A	A_1	A_2	b	D	E	e	s	v	w	y	y_1
max	0.468	0.183	0.285	0.245								
mm nom	0.430	0.163	0.267	0.225	1.06	1.06	0.35	0.025	0.015	0.05	0.05	0.06
min	0.392	0.143	0.249	0.205								

Note
1. Dimension A includes backside coating thickness.

sot8027-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8027-1						~~21-06-11~~ 21-06-16

Fig. 12. Package outline SOT8027-1 (WLCSP16)

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15. Abbreviations

Table 14. Abbreviations

Acronym	Description
CDM	Charged-Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board
SIM	Subscriber Identification Module

16. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NXT4556 v.2	20220615	Product data sheet	-	NXT4556 v.1
Modifications:	• Table 3 corrected (errata). • Fig. 4 corrected (errata). • Fig. 10 corrected (errata).			
NXT4556 v.1	20220502	Product data sheet	-	-

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Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Contents

1. General description....1
2. Features and benefits....1
3. Applications....1
4. Ordering information....2
5. Marking....2
6. Functional diagram....3
7. Pinning information....4
7.1. Pinning....4
7.2. Pin description....4
8. Functional description....5
8.1. Functional behavior....5
8.2. Window of I/O communication....6
8.3. Shutdown sequence....6
8.4. UVLO....7
8.5. **EMI filter**....7
8.6. ESD protection....7
9. Limiting values....8
10. Recommended operating conditions....8
11. Electrical characteristics....9
11.1. Waveforms and test circuits....12
12. Application information....13
13. Design and assembly recommendations....14
13.1. PCB design guidelines....14
13.2. PCB assembly guidelines for Pb-free soldering....14
14. Package outline....16
15. Abbreviations....17
16. Revision history....17
17. Legal information....18

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