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USB3340

Enhanced Single Supply Hi-Speed USB ULPI Transceiver

PRODUCT FEATURES

Datasheet

- USB-IF Battery Charging 1.2 Specification Compliant
- Link Power Management (LPM) Specification Compliant
- Integrated ESD protection circuits
  - — Up to ±25kV IEC Air Discharge without external devices
- Over-Voltage Protection circuit (OVP) protects the VBUS pin from continuous DC voltages up to 30V
- Integrated USB Switch
  - — Allows single USB port of connection by providing switching function for:
    - – Battery charging
    - – Stereo and mono/mic audio
    - – USB Full-Speed/Low-Speed data
- RapidCharge Anywhere™ Provides:
  - — 3-times the charging current through a USB port over traditional solutions
  - — USB-IF Battery Charging 1.2 compliance to any portable device
  - — Charging current up to 1.5Amps via compatible USB host or dedicated charger
  - — Dedicated Charging Port (DCP), Charging (CDP) & Standard (SDP) Downstream Port support
- flexPWR® Technology
  - — Extremely low current design ideal for battery powered applications
  - — “Sleep” mode tri-states all ULPI pins and places the part in a low current state
  - — 1.8V to 3.3V IO Voltage
- Single Power Supply Operation
  - — Integrated 1.8V regulator
  - — Integrated 3.3V regulator
    - – 100mV dropout voltage
- PHYBoost
  - — Programmable USB transceiver drive strength for recovering signal integrity
- VariSense™
  - — Programmable USB receiver sensitivity
- “Wrapper-less” design for optimal timing performance and design ease
  - — Low Latency Hi-Speed Receiver (43 Hi-Speed clocks Max) allows use of legacy UTMI Links with a ULPI bridge
- External Reference Clock operation available
  - — ULPI Clock Input Mode (60MHz sourced by Link)
  - — 0 to 3.6V input drive tolerant
  - — Able to accept “noisy” clock sources as reference to internal, low-jitter PLL
  - — Crystal support available
- Smart detection circuits allow identification of USB charger, headset, or data cable insertion
- Includes full support for the optional On-The-Go (OTG) protocol detailed in the On-The-Go Supplement Revision 2.0 specification
- Supports the OTG Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- UART mode for non-USB serial data transfers
- Internal 5V cable short-circuit protection of ID, DP and DM lines to VBUS or ground
- Industrial Operating Temperature -40°C to +85°C
- 32 pin, QFN RoHS Compliant package (5 x 5 x 0.90 mm height)

Applications

The USB3340 is the solution of choice for any application where a Hi-Speed USB connection is desired and when board space, power, and interface pins must be minimized.

- Cell Phones
- PDAs
- MP3 Players
- GPS Personal Navigation
- Scanners
- External Hard Drives
- Digital Still and Video Cameras
- Portable Media Players
- Entertainment Devices
- Printers
- Set Top Boxes
- Video Record/Playback Systems
- IP and Video Phones
- Gaming Consoles

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Enhanced Single Supply Hi-Speed USB ULPI Transceiver

Datasheet

Order Number(s):

ORDER NUMBER	REFCLK FREQUENCY (Note 0.1)	PACKAGE TYPE	REEL SIZE
USB3340-EZK-TR	Selectable See Table 5.2	32 Pin, QFN RoHS Compliant Package (tape and reel)	4,000 pieces

Note 0.1 All versions support ULPI Clock In Mode (60MHz input at REFCLK)

This product meets the halogen maximum concentration values per IEC61249-2-21

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0.1 Reference Documents

UTMI+ Low Pin Interface (ULPI) Specification, Revision 1.1

Universal Serial Bus Specification, Revision 2.0

On-The-Go Supplement to the USB2.0 Specification, Revision 1.3

On-The-Go Supplement to the USB2.0 Specification, Revision 2.0

USB Battery Charging Specification, Revision 1.2

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Chapter 1 General Description

Microchip's USB3340 is a Hi-Speed USB 2.0 Transceiver that provides a physical layer (PHY) solution well-suited for portable electronic devices. Both commercial and industrial temperature applications are supported.

Several advanced features make the USB3340 the transceiver of choice by reducing both eBOM part count and printed circuit board (PCB) area. Outstanding ESD robustness eliminates the need for external ESD protection devices in typical applications. The internal Over-Voltage Protection circuit (OVP) protects the USB3340 from voltages up to 30V on the **VBUS** pin. By using a reference clock from the Link, the USB3340 removes the cost of a dedicated crystal reference from the design. The USB3340 includes integrated 3.3V and 1.8V regulators, making it possible to operate the device from a single power supply.

The USB3340 is optimized for use in portable applications where a low operating current and standby currents are essential. The USB3340 operates from a single supply and includes integrated regulators for its supplies. The USB3340 also supports the USB Link Power Management protocol (LPM) to further reduce USB operating currents.

The USB3340 also includes RapidCharge Anywhere™ which supports USB-IF Battery Charging 1.2 for any portable device. RapidCharge Anywhere™ provides three times the charging current through a USB port over traditional solutions which translate up to 1.5Amps via compatible USB host or dedicated charger. In addition, this provides a complete USB charging ecosystem between device and host ports such as Dedicated Charging Port (DCP), Charging (CDP) and Standard (SDP) Downstream Ports. Section 5.9 describes this is further detail.

The USB3340 meets all of the electrical requirements for a Hi-Speed USB Host, Device, or an On-the-Go (OTG) transceiver. In addition to the supporting USB signaling, the USB3340 also provides USB UART mode and, in versions with the integrated USB switch, USB Audio mode.

USB3340 uses the industry standard UTMI+ Low Pin Interface (ULPI) to connect the USB transceiver to the Link. ULPI uses a method of in-band signaling and status byte transfers between the Link and PHY to facilitate a USB session with only twelve pins.

The USB3340 uses "wrapper-less" technology to implement the ULPI interface. This "wrapper-less" technology allows the PHY to achieve a low latency transmit and receive time. Microchip's low latency transceiver allows an existing UTMI Link to be reused by adding a UTMI to ULPI bridge. By adding a bridge to the ASIC the existing and proven UTMI Link IP can be reused.

The integrated USB switch enables a single USB port of connection.

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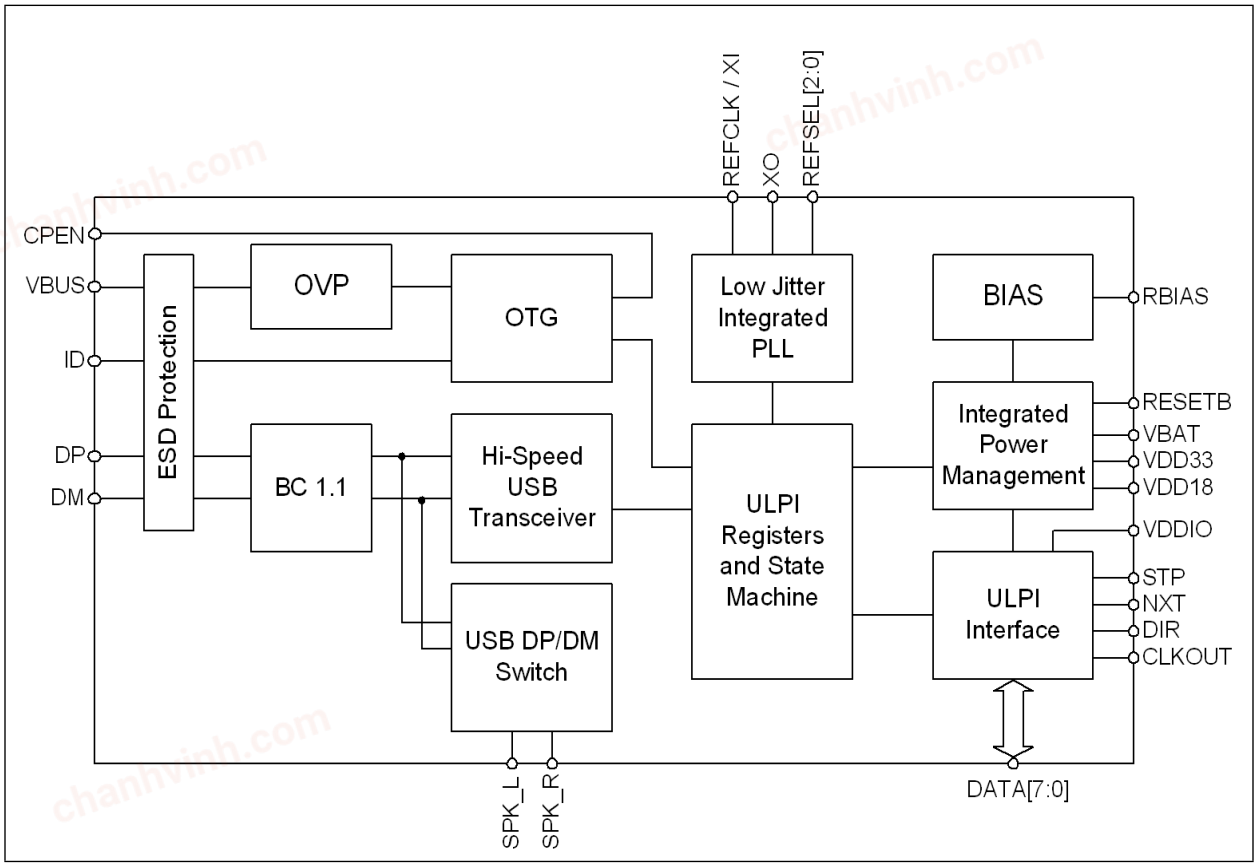


Figure 1.1 Block Diagram USB3340

In USB audio mode, a switch connects the **DP** pin to the **SPK_R** pin, and another switch connects he **DM** pin to the **SPK_L** pin. These switches are shown in the lower left-hand corner of .The USB3340 can be configured to enter USB audio mode as described in Section 6.7.2. In addition, these switches are on when the **RESETB** pin of the USB3340 is asserted. The USB audio mode enables audio signaling from a single USB port of connection, and the switches may also be used to connect Full Speed USB from another transceiver to the USB connector.

The USB3340 includes an integrated 3.3V LDO regulator that is used to generate 3.3V from power applied to the **VBAT** pin. The voltage on the **VBAT** pin can range from 3.0 to 5.5V. The regulator dropout voltage is less than 100mV which allows the PHY to continue USB signaling when the voltage on **VBAT** drops to 3.0V. The USB transceiver will continue to operate at lower voltages, although some parameters may be outside the limits of the USB specifications. The **VBAT** and **VDD33** pins should *never* be connected together.

In USB UART mode, the USB3340 **DP** and **DM** pins are redefined to enable pass-through of asynchronous serial data. The USB3340 will enter UART mode when programmed, as described in Section 6.7.1.

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Chapter 2 Pin Locations and Definitions

2.1 USB3340 Pin Locations and Descriptions

2.1.1 USB3340 Pin Diagram and Pin Definitions

The illustration below is viewed from the top of the package.

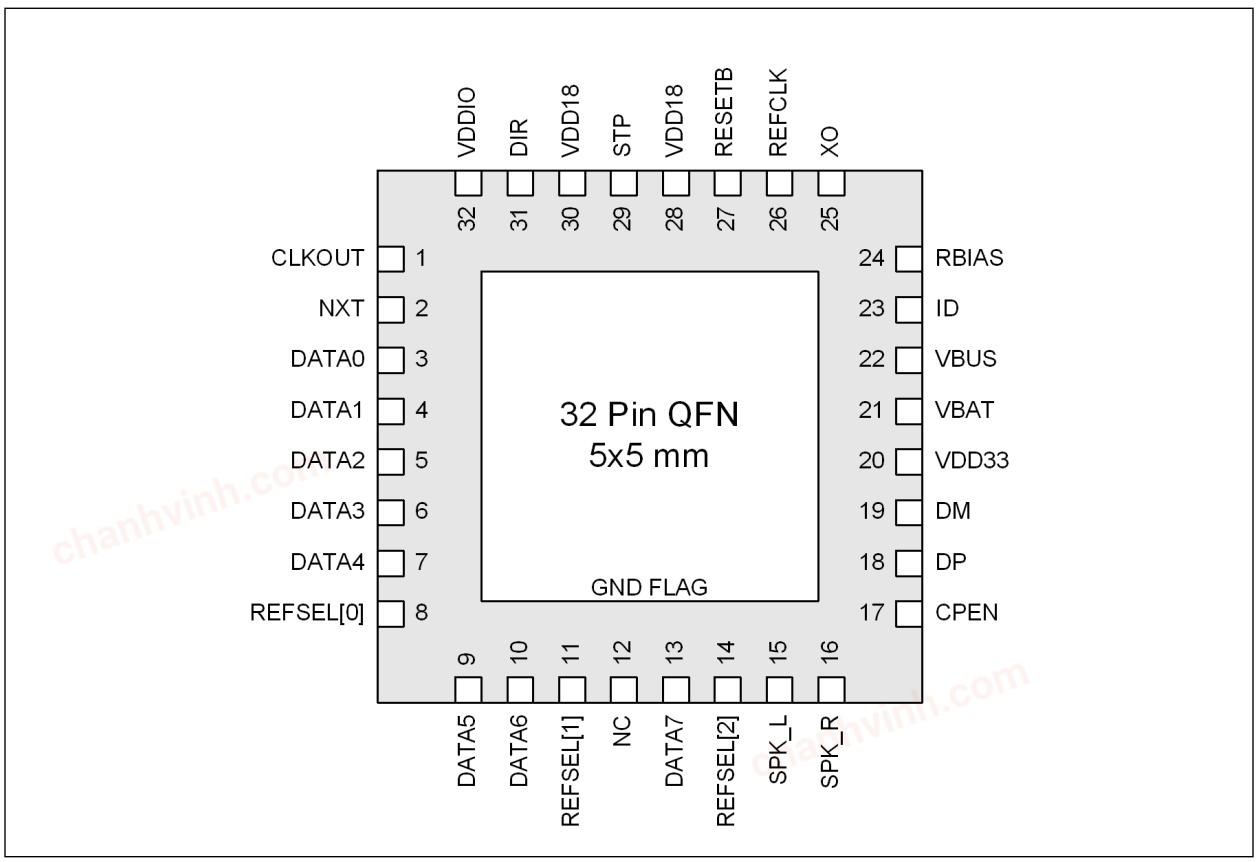


Figure 2.1 USB3340 Pin Locations - Top View

The following table details the pin definitions for the figure above.

Table 2.1 USB3340 Pin Descriptions

PIN	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
1	**CLKOUT**	Output, CMOS	N/A	**ULPI Clock Out Mode:** 60MHz ULPI clock output. All ULPI signals are driven synchronous to the rising edge of this clock. **ULPI Clock In Mode:** Connect this pin to **VDDIO** to configure 60MHz ULPI Clock IN mode as described in Section 5.5.1.
2	**NXT**	Output, CMOS	High	The PHY asserts **NXT** to throttle the data. When the Link is sending data to the PHY, **NXT** indicates when the current byte has been accepted by the PHY.

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Table 2.1 USB3340 Pin Descriptions (continued)

PIN	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
3	**DATA[0]**	I/O, CMOS	N/A	ULPI bi-directional data bus. **DATA[0]** is the LSB.
4	**DATA[1]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
5	**DATA[2]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
6	**DATA[3]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
7	**DATA[4]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
8	**REFSEL[0]**	Input	N/A	Used to select xtal/reference frequency. This pad is connected to **VDDIO** or **GND**.
9	**DATA[5]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
10	**DATA[6]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
11	**REFSEL[1]**	Input	N/A	Used to select xtal/reference frequency. This pad is connected to **VDDIO** or **GND**.
12	**NC**	N/A	N/A	No connect. Leave pin floating.
13	**DATA[7]**	I/O, CMOS	N/A	ULPI bi-directional data bus. **DATA[7]** is the MSB.
14	**REFSEL[2]**	Input	N/A	Used to select xtal/reference frequency. This pad is connected to **VDDIO** or **GND**.
15	**SPK_L**	I/O, Analog	N/A	USB switch in/out for **DM** signals.
16	**SPK_R**	I/O, Analog	N/A	USB switch in/out for **DP** signals.
17	**CPEN**	Output, CMOS	High	External 5 volt supply enable. This pin is used to enable the external Vbus power supply. The **CPEN** pin is low on POR. This pad uses VDD33 logic level.
18	**DP**	I/O, Analog	N/A	D+ pin of the USB cable.
19	**DM**	I/O, Analog	N/A	D- pin of the USB cable.
20	**VDD33**	Power	N/A	3.3V Regulator Output. A 1.0uF (<1 ohm ESR) bypass capacitor to ground is required for regulator stability. The bypass capacitor should be placed as close as possible to the USB3340.
21	**VBAT**	Power	N/A	Regulator input. The regulator supply can be from 5.5V to 3.0V.
22	**VBUS**	I/O, Analog	N/A	This pin is used for the VBUS comparator inputs and for VBUS pulsing during session request protocol. An external resistor, R_{VBUS}, is required between this pin and the USB connector.

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Table 2.1 USB3340 Pin Descriptions (continued)

PIN	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
23	ID	Input, Analog	N/A	For device applications the **ID** pin is connected to **VDD33**. For Host applications **ID** is grounded. For OTG applications the **ID** pin is connected to the USB connector.
24	RBIAS	Analog, CMOS	N/A	Bias Resistor pin. This pin requires an 8.06kΩ (±1%) resistor to ground, placed as close as possible to the USB3340. Nominal voltage during ULPI operation is 0.8V.
25	XO	Output, Analog	N/A	Crystal pin. If using an external clock on XI this pin should be floated.
26	REFCLK	Input, CMOS	N/A	**ULPI Clock Out Mode:** Model-specific reference clock or XI (crystal in) pin. See on page 2. **ULPI Clock In Mode:** 60MHz ULPI clock input.
27	RESETB	Input, CMOS,	Low	When low, the part is suspended and the 3.3V and 1.8V regulators are disabled. When high, the USB3340 will operate as a normal ULPI device, as described in Section 5.6.2. The state of this pin may be changed asynchronously to the clock signals. When asserted for a minimum of 1 microsecond and then de-asserted, the ULPI registers are reset to their default state and all internal state machines are reset.
28	VDD18	Power	N/A	1.8V Regulator Output. A 1.0uF (<1 ohm ESR) bypass capacitor to ground is required for regulator stability. The bypass capacitor should be placed as close as possible to the USB3340. Pin 28 and Pin 30 must be tied together. Only one bypass capacitor is required between Pin 28 and Pin 30.
29	STP	Input, CMOS	High	The Link asserts **STP** for one clock cycle to stop the data stream currently on the bus. If the Link is sending data to the PHY, **STP** indicates the last byte of data was on the bus in the previous cycle.
30	VDD18	Power	N/A	1.8V Regulator Output. A 1.0uF (<1 ohm ESR) bypass capacitor to ground is required for regulator stability. The bypass capacitor should be placed as close as possible to the USB3340. Pin 28 and Pin 30 must be tied together. Only one bypass capacitor is required between Pin 28 and Pin 30.
31	DIR	Output, CMOS	N/A	Controls the direction of the data bus. When the PHY has data to transfer to the Link, it drives **DIR** high to take ownership of the bus. When the PHY has no data to transfer it drives **DIR** low and monitors the bus for commands from the Link.
32	VDDIO	Power	N/A	ULPI interface supply voltage. When RESETB is low and VDDIO is powered on, ULPI pins will tri-state.
FLAG	GND	Ground	N/A	Ground.

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Chapter 3 Limiting Values

3.1 Absolute Maximum Ratings

Table 3.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VBUS, **VBAT**, **ID**, **DP**, **DM**, **SPK_L**, and **SPK_R** voltage to **GND**	V_{MAX_5V}	Voltage measured at pin. **VBUS** tolerant to 30V with external R_{VBUS}.	-0.5		+6.0	V
Maximum **VDD18** voltage to Ground	V_{MAX_18V}		-0.5		2.5	V
Maximum **VDD33** voltage to Ground	V_{MAX_33V}		-0.5		4.0	V
Maximum **VDDIO** voltage to Ground	V_{MAX_IOV}		-0.5		4.0	V
Maximum I/O voltage to Ground	V_{MAX_IN}		-0.5		V_{DDIO} + 0.7	
Operating Temperature	T_{MAX_OP}		-40		85	C
Storage Temperature	T_{MAX_STG}		-55		150	C

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.2 Recommended Operating Conditions

Table 3.2 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VBAT to **GND**	V_{BAT}		3.0		5.5	V
VDD33 to **GND**	V_{DD33}		3.0	3.3	3.6	V
VDD18 to **GND**	V_{DD18}		1.6	1.8	2.0	V
VDDIO to **GND**	V_{DDIO}		1.6	1.8-3.3	3.6	V
Input Voltage on Digital Pins (**RESETB**, **STP**, **DIR**, **NXT**, **DATA[7:0]**)	V_I		0.0		V_{DDIO}	V
Voltage on Analog I/O Pins (**DP**, **DM**, **ID**, **CPEN**, **SPK_L**, **SPK_R**)	$V_{I(I/O)}$		0.0		V_{DD33}	V
VBUS to **GND**	V_{VMAX}		0.0		5.5	V
Ambient Temperature	T_A		-40		85	C

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Chapter 4 Electrical Characteristics

The following conditions are assumed unless otherwise specified:

V_{DD33} = 3.0 to 3.6V; VDD18 = 1.6 to 2.0V; V_{SS} = 0V; T_A = -40C to +85C

4.1 Operating Current

Table 4.1 Operating Current

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Synchronous Mode Current (Default Configuration)	$I_{VBAT(SYNC)}$	USB Idle	18	22	24	mA
	$I_{VIO(SYNC)}$		1	2	5	mA
Synchronous Mode Current (HS USB operation)	$I_{VBAT(HS)}$	Active USB Transfer	33	35	37	mA
	$I_{VIO(HS)}$		5	6	14	mA
Synchronous Mode Current (FS/LS USB operation)	$I_{VBAT(FS)}$	Active USB Transfer	25	28.5	30	mA
	$I_{VIO(FS)}$		4	5	13	mA
Serial Mode Current (FS/LS USB) Note 4.1	$I_{VBAT(FS_S)}$		7	8	9	mA
	$I_{VIO(FS_S)}$		0	0.1	0.7	mA
USB UART Current Note 4.1	$I_{VBAT(UART)}$		7	8	9	mA
	$I_{VIO(UART)}$		0	0.1	0.7	mA
Low Power Mode Note 4.2 Note 4.3	$I_{VBAT(SUSPEND)}$	V_{VBAT} = 4.2V V_{VDDIO} = 1.8V	29	32	83	uA
	$I_{VIO(SUSPEND)}$		0	0	2	uA
RESET Mode Note 4.3	$I_{VBAT(RSTB)}$	**RESETB** = 0 V_{VBAT} = 4.2V V_{VDDIO} = 1.8V	0.1	1	12	uA
	$I_{VIO(RSTB)}$		0	0	7	uA

Note 4.1 *ClockSuspendM* bit = 0.

Note 4.2 SessEnd, VbusVld, and IdFloat comparators disabled. **STP** Interface protection disabled.

Note 4.3 REFCLK is OFF

4.2 Clock Specifications

The model number for each frequency of REFCLK is provided in on page 2.

Table 4.2 Clock Specifications

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Suspend Recovery Time	T_{START}	LPM Enable = 0	1.0	1.1	1.2	ms
	T_{START_LPM}	LPM Enable = 1	125		150	uS

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Table 4.2 Clock Specifications (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PHY Preparation Time 60MHz **REFCLK**	T_{PREP}	LPM Enable = 0	1.0	1.1	1.2	ms
	T_{PREP_LPM}	LPM Enable = 1	125		150	uS
CLKOUT Duty Cycle	DC_{CLKOUT}	**ULPI Clock Input Mode**	45		55	%
REFCLK Duty Cycle	DC_{REFCLK}		20		80	%
REFCLK Frequency Accuracy	F_{REFCLK}		-500		+500	PPM

Note: T_{START} and T_{PREP} are measured from the time when **REFCLK** and **RESETB** are both valid to when the USB3340 de-asserts **DIR**.

Note: The USB3340 uses the *AutoResume* feature, Section 6.4.1.4, to allow a host start-up time of less than 1ms.

4.3 ULPI Interface Timing

Table 4.3 ULPI Interface Timing

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
60MHz ULPI Output Clock Note 4.4					
Setup time (**STP**, data in)	T_{SC}, T_{SD}	Model-specific **REFCLK**	5.0		ns
Hold time (**STP**, data in)	T_{HC}, T_{HD}	Model-specific **REFCLK**	0.0		ns
Output delay (control out, 8-bit data out)	T_{DC}, T_{DD}	Model-specific **REFCLK**	1.5	6	ns
60MHz ULPI Input Clock					
Setup time (**STP**, data in)	T_{SC}, T_{SD}	60MHz **REFCLK**	3		ns
Hold time (**STP**, data in)	T_{HC}, T_{HD}	60MHz **REFCLK**	0		ns
Output delay (control out, 8-bit data out)	T_{DC}, T_{DD}	60Mhz **REFCLK**	0.5	6.0	ns

Note: C_{Load} = 10pF.

Note 4.4 **REFCLK** does not need to be aligned in any way to the ULPI signals.

4.4 Digital IO Pins

Table 4.4 Digital IO Characteristics: RESETB, CPEN, STP, DIR, NXT, DATA[7:0], and REFCLK Pins

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low-Level Input Voltage	V_{IL}		V_{SS}		0.8	V
High-Level Input Voltage	V_{IH}		0.68 * V_{DDIO}		V_{DDIO}	V
High-Level Input Voltage **REFCLK** and **RESETB**	V_{IH_REF}		0.68 * V_{DDIO}		V_{DD33}	V
Low-Level Output Voltage	V_{OL}	I_{OL} = 8mA			0.4	V

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Table 4.4 Digital IO Characteristics: RESETB, CPEN, STP, DIR, NXT, DATA[7:0], and REFCLK Pins (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High-Level Output Voltage	V_{OH}	I_{OH} = -8mA	V_{DDIO}-0.4			V
High-Level Output Voltage **CPEN**	V_{OH}	I_{OH} = -8mA	V_{DD33} - 0.4			V
Output rise time	T_{IORISE}	C_{LOAD} = 10pF		1.19		nS
Output fall time	T_{IOFALL}	C_{LOAD} = 10pF		1.56		nS
Input Leakage Current	I_{LI}				±10	uA
Pin Capacitance	Cpin				4	pF
STP pull-up resistance	R_{STP}	InterfaceProtectDisable = 0	55	67	80	kΩ
DATA[7:0] pull-down resistance	R_{DATA_PD}	ULPI Synchronous Mode	55	67	77	kΩ
CLKOUT External Drive	V_{IH_ED}	At start-up or following reset			0.4 * V_{DDIO}	V

4.5 DC Characteristics: Analog I/O Pins

Table 4.5 DC Characteristics: Analog I/O Pins (DP/DM)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LS/FS FUNCTIONALITY						
Input levels						
Differential Receiver Input Sensitivity	V_{DIFS}	| V(DP) - V(DM) |	0.2			V
Differential Receiver Common-Mode Voltage	V_{CMFS}		0.8		2.5	V
Single-Ended Receiver Low Level Input Voltage	V_{ILSE}	Note 4.6			0.8	V
Single-Ended Receiver High Level Input Voltage	V_{IHSE}	Note 4.6	2.0			V
Single-Ended Receiver Hysteresis	V_{HYSSE}		0.050		0.150	V
Output Levels						
Low Level Output Voltage	V_{FSOL}	Pull-up resistor on DP; R_L = 1.5kΩ to V_{DD33}			0.3	V
High Level Output Voltage	V_{FSOH}	Pull-down resistor on DP, DM; Note 4.6 R_L = 15kΩ to GND	2.8		3.6	V
Termination						
Driver Output Impedance for HS	Z_{HSDRV}	Steady state drive	40.5	45	49.5	Ω

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Table 4.5 DC Characteristics: Analog I/O Pins (DP/DM) (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Impedance	Z_{INP}	RX, RPU, RPD disabled	1.0			MΩ
Pull-up Resistor Impedance	R_{PU}	Bus Idle, Note 4.5	0.900	1.24	1.575	kΩ
Pull-up Resistor Impedance	R_{PU}	Device Receiving, Note 4.5	1.425	2.26	3.09	kΩ
Pull-dn Resistor Impedance	R_{PD}	Note 4.5	14.25	16.9	20	kΩ
HS FUNCTIONALITY						
Input levels						
HS Differential Input Sensitivity	V_{DIHS}	| V(DP) - V(DM) |	100			mV
HS Data Signaling Common Mode Voltage Range	V_{CMHS}		-50		500	mV
HS Squelch Detection Threshold (Differential)	V_{HSSQ}	*VariSense[1:0]* = 00b Note 4.7	100		150	mV
HS Disconnect Threshold	V_{HSDSC}		525		625	mV
Output Levels						
High Speed Low Level Output Voltage (DP/DM referenced to GND)	V_{HSOL}	45Ω load	-10		10	mV
High Speed High Level Output Voltage (DP/DM referenced to GND)	V_{HSOH}	45Ω load	360		440	mV
High Speed IDLE Level Output Voltage (DP/DM referenced to GND)	V_{OLHS}	45Ω load	-10		10	mV
Chirp-J Output Voltage (Differential)	V_{CHIRPJ}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	700		1100	mV
Chirp-K Output Voltage (Differential)	V_{CHIRPK}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	-900		-500	mV
Leakage Current						
OFF-State Leakage Current	I_{LZ}				±10	uA
Port Capacitance						
Transceiver Input Capacitance	C_{IN}	Pin to GND		5	10	pF

Note 4.5 The resistor value follows the 27% Resistor ECN published by the USB-IF.

Note 4.6 The values shown are valid when the *USB RegOutput* bits in the USB IO & Power Management register are set to the default value.

Note 4.7 An automatic waiver up to 200mV is granted to accommodate system-level elements such as measurement/test fixtures, captive cables, EMI components, and ESD suppression. This parameter can be tuned using VariSense technology, as defined in Section 7.1.3.1of Chapter 7.

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4.6 Dynamic Characteristics: Analog I/O Pins

Table 4.6 Dynamic Characteristics: Analog I/O Pins (DP/DM)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FS Output Driver Timing						
FS Rise Time	T_{FR}	C_L = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
FS Fall Time	T_{FF}	C_L = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
Output Signal Crossover Voltage	V_{CRS}	Excluding the first transition from IDLE state	1.3		2.0	V
Differential Rise/Fall Time Matching	T_{FRFM}	Excluding the first transition from IDLE state	90		111.1	%
LS Output Driver Timing						
LS Rise Time	T_{LR}	C_L = 50-600pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	75		300	ns
LS Fall Time	T_{LF}	C_L = 50-600pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	75		300	ns
Differential Rise/Fall Time Matching	T_{LRFM}	Excluding the first transition from IDLE state	80		125	%
HS Output Driver Timing						
Differential Rise Time	T_{HSR}		500			ps
Differential Fall Time	T_{HSF}		500			ps
Driver Waveform Requirements		Eye pattern of Template 1 in USB 2.0 specification				
High Speed Mode Timing						
Receiver Waveform Requirements		Eye pattern of Template 4 in USB 2.0 specification				
Data Source Jitter and Receiver Jitter Tolerance		Eye pattern of Template 4 in USB 2.0 specification				

4.7 VBUS Electrical Characteristics

Table 4.7 VBUS Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SessEnd trip point	$V_{SessEnd}$		0.2	0.5	0.8	V
SessVld trip point	$V_{SessVld}$		0.8	1.4	2.0	V
VbusVld trip point	$V_{VbusVld}$		4.4	4.58	4.75	V
VBUS Pull-Up	R_{VPU}	**VBUS** to **VDD33** Note 4.8 (*ChargeVbus* = 1)	1.29	1.34	1.45	kΩ

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Table 4.7 VBUS Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VBUS Pull-down	R_{VPD}	**VBUS** to **GND** Note 4.8 (*DisChargeVbus* = 1)	1.55	1.7	1.85	kΩ
VBUS Impedance	R_{VB}	**VBUS** to **GND**	40	75	100	kΩ
A-Device Impedance to ground	R_{IdGnd}	Maximum Impedance to ground on **ID** pin			100	kΩ

Note 4.8 The R_{VPD} and R_{VPU} values include the required 1kΩ external R_{VBUS} resistor.

4.8 ID Electrical Characteristics

Table 4.8 ID Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ID Ground Trip Point	V_{IdGnd}		0.4	0.7	0.9	V
ID Float Trip Point	$V_{IdFloat}$		1.6	2.2	2.5	V
ID pull-up resistance	R_{ID}	IdPullup = 1	80	100	120	kΩ
ID weak pull-up resistance	R_{IDW}	IdPullup = 0	1			MΩ
ID pull-dn resistance	R_{IDPD}	IdGndDrv = 1			1000	Ω

4.9 USB Audio Switch Characteristics

Table 4.9 USB Audio Switch Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum “ON” Resistance	R_{ON_Min}	$0 < V_{switch} < V_{DD33}$	2.7	5	5.8	Ω
Maximum “ON” Resistance	R_{ON_Max}	$0 < V_{switch} < V_{DD33}$	4.5	7	13	Ω
Minimum “OFF” Resistance	R_{OFF_Min}	$0 < V_{switch} < V_{DD33}$	1			MΩ

4.10 USB Charger Detection Characteristics

Table 4.10 USB Charger Detection Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Source Voltage	V_{DAT_SRC}	$I_{DAT_SRC} < 250uA$	0.5		0.7	V
Data Detect Voltage	V_{DAT_REF}		0.25		0.4	V
Data Source Current	I_{DAT_SRC}		250			uA
Data Sink Current	I_{DAT_SINK}		50		150	uA

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Table 4.10 USB Charger Detection Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Connect Current	I_{DP_SRC}		7		13	uA
Weak Pull-up Resistor Impedance	R_{CD}	Configured by bits 4 and 5 in USB IO & Power Management register.	128	170	212	kΩ

4.11 Regulator Output Voltages and Capacitor Requirement

Table 4.11 Regulator Output Voltages and Capacitor Requirement

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Regulator Output Voltage	V_{DD33}	5.5V > **VBAT** > 3.0V	2.8	3.3	3.6	V
		USB UART Mode & UART RegOutput[1:0] = 01 6V > VBAT > 3.0V	2.7	3.0	3.3	V
		USB UART Mode & UART RegOutput[1:0] = 10 6V > VBAT > 3.0V	2.47	2.75	3.03	V
		USB UART Mode & UART RegOutput[1:0] = 11 6V > VBAT > 3.0V	2.25	2.5	2.75	V
Regulator Bypass Capacitor	C_{OUT33}		1.0			uF
Bypass Capacitor ESR	C_{ESR33}				1	Ω
Regulator Output Voltage	V_{DD18}	3.6V > **VDD33** > 2.25V	1.6	1.8	2.0	V
Regulator Bypass Capacitor	C_{OUT18}		1.0			uF
Bypass Capacitor ESR	C_{ESR18}				1	Ω

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4.12 Piezoelectric Resonator for Internal Oscillator

The internal oscillator may be used with an external quartz crystal or ceramic resonator as described in Section 5.4. See Table 4.12 for the recommended crystal specifications.

Table 4.12 USB3340 Quartz Crystal Specifications

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS	NOTES
Crystal Cut	AT, typ					
Crystal Oscillation Mode	Fundamental Mode					
Crystal Calibration Mode	Parallel Resonant Mode					
Frequency	F_{fund}	-	See on page 2	-	MHz	
Total Allowable PPM Budget		-	-	±500	PPM	Note 4.9
Shunt Capacitance	C_O	-	7 typ	-	pF	
Load Capacitance	C_L	-	20 typ	-	pF	
Drive Level	P_W	0.1	-	-	mW	
Equivalent Series Resistance	R_1	-	-	30	Ohm	
USB3340 **REFCLK** Pin Capacitance		-	3 typ	-	pF	Note 4.10
USB3340 **XO** Pin Capacitance		-	3 typ	-	pF	Note 4.10

Note 4.9 The required bit rate accuracy for Hi-Speed USB applications is ±500 ppm as provided in the USB 2.0 Specification. This takes into account the effect of voltage, temperature, aging, etc.

Note 4.10 This number includes the pad, the bond wire and the lead frame. Printed Circuit Board (PCB) capacitance is not included in this value. The PCB capacitance value and the capacitance value of the **XO** and **REFCLK** pins are required to accurately calculate the value of the two external load capacitors.

4.13 ESD and Latch-Up Performance

Table 4.13 ESD and Latch-Up Performance

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	COMMENTS
ESD PERFORMANCE						
Note 4.11 Note 4.12	Human Body Model			±8	kV	Device
System	EN/IEC 61000-4-2 Contact Discharge			±25	kV	3rd party system test
System	EN/IEC 61000-4-2 Air-gap Discharge			±25	kV	3rd party system test
LATCH-UP PERFORMANCE						
All Pins	EIA/JESD 78, Class II		150		mA	

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Note 4.11 **REFCLK**, **XO**, **ID, RESETB**, **SPK_L** and **SPK_R** pins: ±5kV Human Body Model.

Note 4.12 The **REFSEL[2:0]** pins only tested to ±2kV Human Body Model.

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Chapter 5 Architecture Overview

The USB3340 consists of the blocks shown in the diagram below.

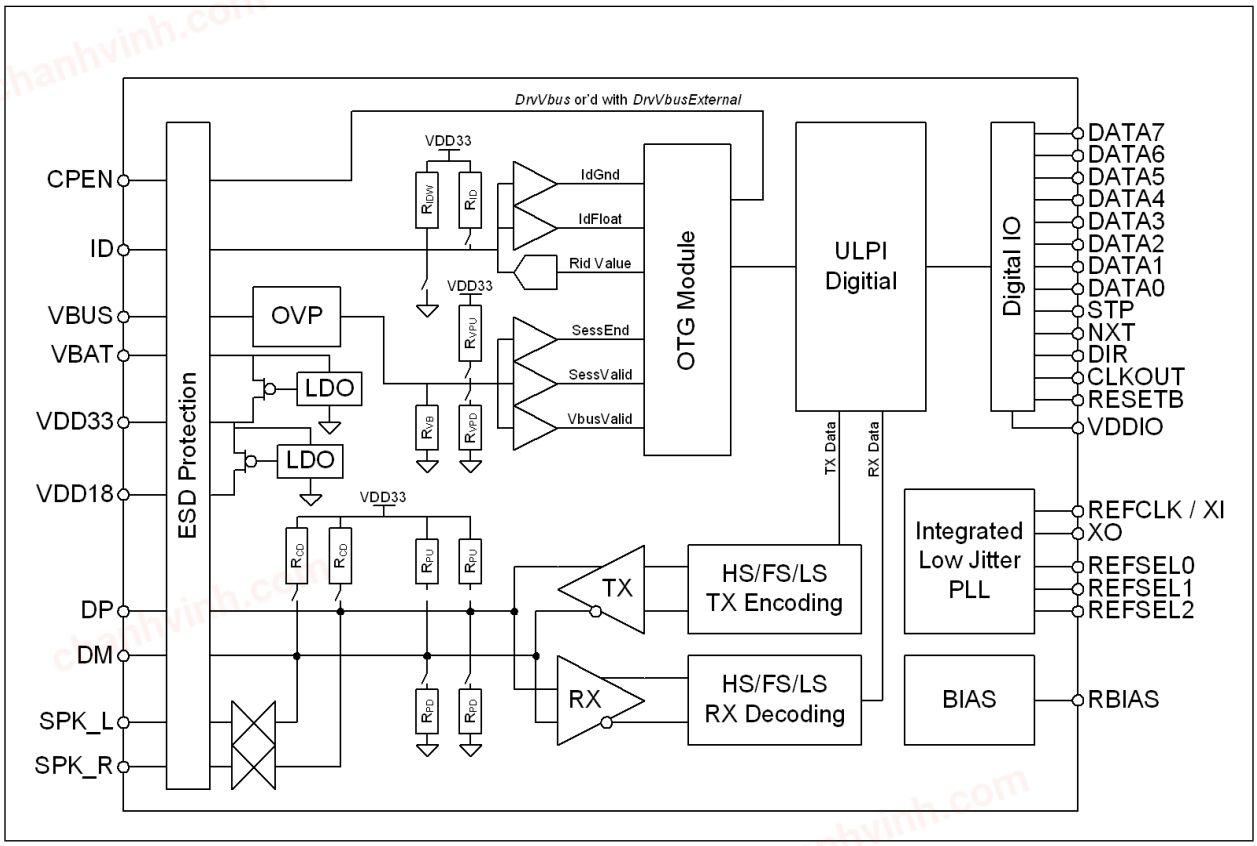


Figure 5.1 USB3340 System Diagram

5.1 ULPI Digital Operation and Interface

This section of the USB3340 is covered in detail in Chapter 6, ULPI Operation.

5.2 USB 2.0 Hi-Speed Transceiver

The blocks in the lower left-hand corner of interface to the DP/DM pins.

5.2.1 USB Transceiver

The USB3340 transceiver includes a Universal Serial Bus Specification Rev 2.0 compliant receiver and transmitter. The DP/DM signals in the USB cable connect directly to the receivers and transmitters.

The receiver consists of receivers for HS and FS/LS mode. Depending on the mode, the selected receiver provides the serial data stream through the multiplexer to the RX Logic block. For HS mode support, the HS RX block contains a squelch circuit to insure that noise is not interpreted as data. The RX block also includes a single-ended receiver on each of the data lines to determine the correct FS linestate.

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Data from the Link is encoded, bit stuffed, serialized and transmitted onto the USB cable by the transmitter. Separate differential FS/LS and HS transmitters are included to support all modes.

The USB3340 TX block meets the HS signalling level requirements in the USB 2.0 Specification when the PCB traces from the **DP** and **DM** pins to the USB connector are correctly designed. In some systems the proper 90 ohm differential impedance can not be maintained and it may be desirable to compensate for loss by adjusting the HS transmitter amplitude and this HS squelch threshold. The *PHYBoost* bits in the HS Compensation Register may be configured to adjust the HS transmitter amplitude at the **DP** and **DM** pins. The *VariSense* bits in the HS Compensation Register can also be used to lower the squelch threshold to compensate for losses on the PCB.

To ensure proper operation of the USB transceiver the settings of Table 5.1 must be followed.

5.2.2 Termination Resistors

The USB3340 transceiver fully integrates all of the USB termination resistors on both **DP** and **DM**. This includes 1.5kΩ pull-up resistors, 15kΩ pull-down resistors and the 45Ω High Speed termination resistors. These resistors require no tuning or trimming by the Link. The state of the resistors is determined by the operating mode of the transceiver when operating in synchronous mode.

The *XcvrSelect[1:0]*, *TermSelect* and *OpMode[1:0]* bits in the Function Control register, and the *DpPulldown* and *DmPulldown* bits in the OTG Control register control the configuration of the termination resistors. All possible valid resistor combinations are shown in Table 5.1, and operation is guaranteed in only the configurations shown. If a ULPI Register Setting is configured that does not match a setting in the table, the transceiver operation is not guaranteed and the settings in the last row of Table 5.1 will be used.

- RPU_DP_EN activates the 1.5kΩ DP pull-up resistor
- RPU_DM_EN activates the 1.5kΩ DM pull-up resistor
- RPD_DP_EN activates the 15kΩ DP pull-down resistor
- RPD_DM_EN activates the 15kΩ DM pull-down resistor
- HSTERM_EN activates the 45Ω DP and DM High Speed termination resistors

Table 5.1 DP/DM Termination vs. Signaling Mode

SIGNALING MODE	ULPI REGISTER SETTINGS					USB3340 TERMINATION RESISTOR SETTINGS				
	XcvrSelect[1:0]	*TermSelect*	*OpMode[1:0]*	*DpPulldown*	*DmPulldown*	RPU_DP_EN	RPU_DM_EN	RPD_DP_EN	RPD_DM_EN	HSTERM_EN
General Settings										
Tri-State Drivers, Note 5.1	XXb	Xb	01b	Xb	Xb	0b	0b	0b	0b	0b
Power-up or VBUS < $V_{SESSEND}$	01b	0b	00b	1b	1b	0b	0b	1b	1b	0b
Host Settings										
Host Chirp	00b	0b	10b	1b	1b	0b	0b	1b	1b	1b
Host High Speed	00b	0b	00b	1b	1b	0b	0b	1b	1b	1b
Host Full Speed	X1b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host HS/FS Suspend	01b	1b	00b	1b	1b	0b	0b	1b	1b	0b

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Table 5.1 DP/DM Termination vs. Signaling Mode (continued)

SIGNALING MODE	ULPI REGISTER SETTINGS					USB3340 TERMINATION RESISTOR SETTINGS				
	XcvrSelect[1:0]	*TermSelect*	*OpMode[1:0]*	*DpPulldown*	*DmPulldown*	RPU_DP_EN	RPU_DM_EN	RPD_DP_EN	RPD_DM_EN	HSTERM_EN
Host HS/FS Resume	01b	1b	10b	1b	1b	0b	0b	1b	1b	0b
Host Low Speed	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host LS Suspend	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host LS Resume	10b	1b	10b	1b	1b	0b	0b	1b	1b	0b
Host Test J/Test_K	00b	0b	10b	1b	1b	0b	0b	1b	1b	1b
Peripheral Settings										
Peripheral Chirp	00b	1b	10b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS	00b	0b	00b	0b	0b	0b	0b	0b	0b	1b
Peripheral FS	01b	1b	00b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Suspend	01b	1b	00b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Resume	01b	1b	10b	0b	0b	1b	0b	0b	0b	0b
Peripheral LS	10b	1b	00b	0b	0b	0b	1b	0b	0b	0b
Peripheral LS Suspend	10b	1b	00b	0b	0b	0b	1b	0b	0b	0b
Peripheral LS Resume	10b	1b	10b	0b	0b	0b	1b	0b	0b	0b
Peripheral Test J/Test K	00b	0b	10b	0b	0b	0b	0b	0b	0b	1b
OTG device, Peripheral Chirp	00b	1b	10b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS	00b	0b	00b	0b	1b	0b	0b	0b	1b	1b
OTG device, Peripheral FS	01b	1b	00b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS/FS Suspend	01b	1b	00b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS/FS Resume	01b	1b	10b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral Test J/Test K	00b	0b	10b	0b	1b	0b	0b	0b	1b	1b
Charger Detection										
Connect Detect	01b	0b	00b	0b	1b	0b	0b	0b	1b	0b
Any combination not defined above, Note 5.2						0b	0b	1b	1b	0b

Note: This is equivalent to Table 40, Section 4.4 of the ULPI 1.1 specification.

Note: USB3340 does not support operation as an upstream hub port. See Chapter 6.4.1.3.

Note 5.1 When **RESETB** = 0 The HS termination will tri-state the USB drivers

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Note 5.2 The transceiver operation is not guaranteed in a combination that is not defined.

The USB3340 uses the 27% resistor ECN resistor tolerances. The resistor values are shown in Table 4.5.

5.3 Bias Generator

This block consists of an internal bandgap reference circuit used for generating the driver current and the biasing of the analog circuits. This block requires an external 8.06KΩ, 1% tolerance, reference resistor connected from **RBIAS** to ground. This resistor should be placed as close as possible to the USB3340 to minimize the trace length. The nominal voltage at **RBIAS** is 0.8V +/- 10% and therefore the resistor will dissipate approximately 80µW of power.

5.4 Crystal Reference Support

The USB3340 provide support for a 26MHz crystal to provide the reference frequency required by the device in place of a clock oscillator. The crystal should be connected to the REFCLK/XI and XO pins as shown in Figure 8.2. If a 26MHz clock oscillator is used in place of a crystal, it should be driven into the REFCLK/XI pin, and the XO pin should be left floating.

Proper care should be taken to ensure that a crystal is selected with appropriate power dissipation characteristics.

5.5 Integrated Low Jitter PLL

The USB3340 uses an integrated low jitter phase locked loop (PLL) to provide a clean 480MHz clock required for HS USB signal quality. This clock is used by the PHY during both transmit and receive. The USB3340 PLL requires an accurate frequency reference to be driven on the **REFCLK** pin.

5.5.1 REFCLK Frequency Selection

The USB3340 PLL is designed to operate in one of two reference clock modes. In the first mode, the 60MHz ULPI clock is driven on the **REFCLK** pin. In the second mode a reference clock is driven on the **REFCLK** pin. The Link is driving the ULPI clock, in the first mode, and this is referred to as **ULPI Clock Input Mode**. In the second mode, the USB3340 generates the ULPI clock, and this is referred to as **ULPI Clock Output Mode**.

During start-up, the USB3340 monitors the **CLKOUT** pin. If a connection to **VDDIO** is detected, the USB3340 is configured for a 60MHz ULPI reference clock driven on the **REFCLK** pin. Section 5.5.1.1 and Section 5.5.1.2 describe how to configure the USB3340 for either ULPI Clock Input Mode or ULPI Clock Output Mode.

5.5.1.1 ULPI Clock Input Mode (60MHz REFCLK Mode)

When using ULPI Clock Input Mode, the Link must supply the 60MHz ULPI clock to the USB3340. In this mode the 60MHz ULPI Clock is connected to the **REFCLK** pin, and the **CLKOUT** pin is tied high to **VDDIO**.

After the PLL has locked to the correct frequency, the USB3340 will de-assert **DIR** and the Link can begin using the ULPI interface. The USB3340 is guaranteed to start the clock within the time specified in Table 4.2. For Host applications, the ULPI *AutoResume* bit should be enabled. This is described in Section 6.4.1.4.

For the USB3340, the REF pins should be tied to ground.

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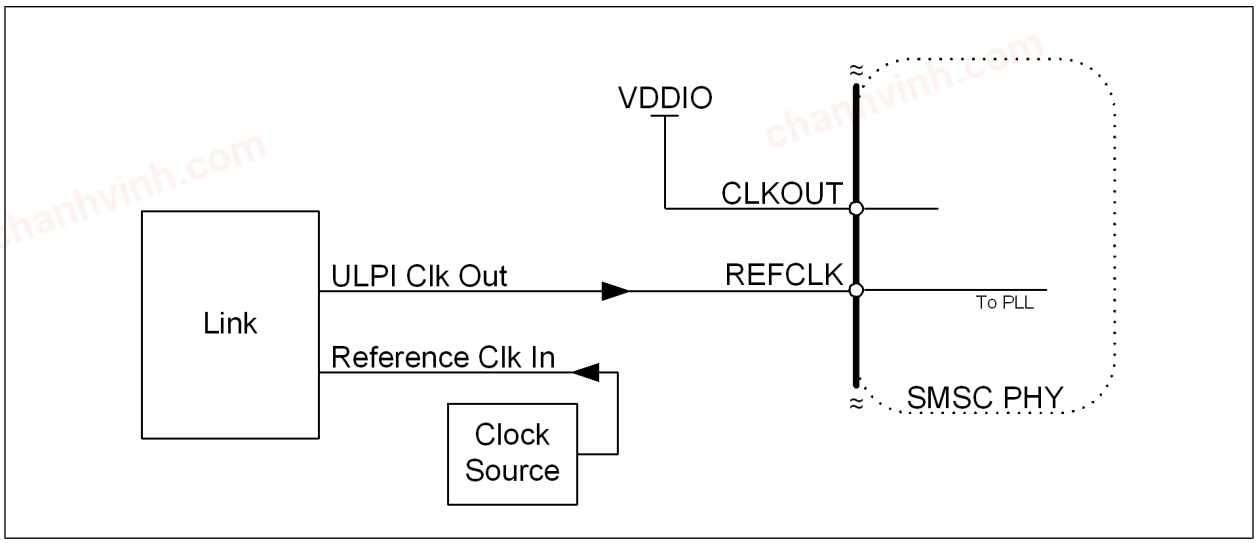


Figure 5.2 Configuring the USB3340 for ULPI Clock Input Mode (60 MHz)

5.5.1.2 ULPI Clock Output Mode

When using ULPI Clock Output Mode, the USB3340 generates the 60MHz ULPI clock used by the Link. In this mode, the **REFCLK** pin must be driven with the model-specific frequency, and the **CLKOUT** pin sources the 60MHz ULPI clock to the Link. When using ULPI Clock Output Mode, the system must not drive the **CLKOUT** pin following POR or hardware reset with a voltage that exceeds the value of V_{IH_ED} provided in Table 4.3. An example of ULPI Clock Output Mode is shown in Figure 8.1

After the PLL has locked to the correct frequency, the USB3340 generates the 60MHz ULPI clock on the **CLKOUT** pin, and de-asserts **DIR** to indicate that the PLL is locked. The USB3340 is guaranteed to start the clock within the time specified in Table 4.2, and it will be accurate to within ±500ppm. For Host applications the ULPI *AutoResume* bit should be enabled. This is described in Section 6.4.1.4.

When using ULPI Clock Output Mode, the edges of the reference clock do not need to be aligned in any way to the ULPI interface signals. There is no need to align the phase of the **REFCLK** and the **CLKOUT**.

For the USB3340, the reference clock frequency required is determined by the settings of the REFSEL[2:0] pins. The pins should either be connected to **VDDIO** or **GND**. The reference frequency use is shown in Table 5.2.

Table 5.2 REF[2:0] vs. Required Frequency at REFCLK

REFSEL[2:0]	REFCLK FREQUENCY
000	52 MHz
001	38.4 MHz
010	12 MHz
011	27 MHz

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Table 5.2 REF[2:0] vs. Required Frequency at REFCLK

REFSEL[2:0]	REFCLK FREQUENCY
100	13 MHz
101	19.2 MHz
110	26 MHz
111	24 MHz

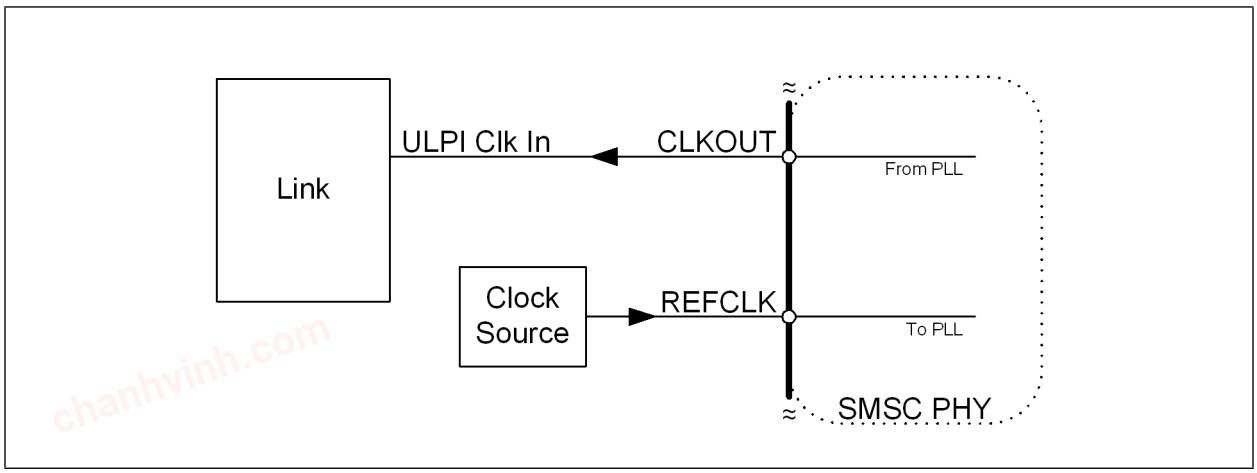


Figure 5.3 Configuring the USB3340 for ULPI Clock Output Mode

5.5.2 REFCLK Amplitude

The reference clock should be connected to the **REFCLK** pin as shown in the application diagrams, Figure 8.1. The **REFCLK** pin is designed to be driven with a square wave from 0V to **VDDIO**, but can be driven with a square wave from 0V to as high as 3.6V. The USB3340 uses only the positive edge of the **REFCLK**.

If a digital reference is not available, the **REFCLK** pin can be driven by an analog sine wave that is AC coupled into the **REFCLK** pin. If using an analog clock the DC bias should be set at the mid-point of the **VDD18** supply using a bias circuit as shown in Figure 5.4. The amplitude must be greater than 300mV peak to peak. The component values provided in Figure 5.4 are for example only. The actual values should be selected to satisfy system requirements.

The **REFCLK** amplitude must comply with the signal amplitudes shown in Table 4.4 and the duty cycle in Table 4.2.

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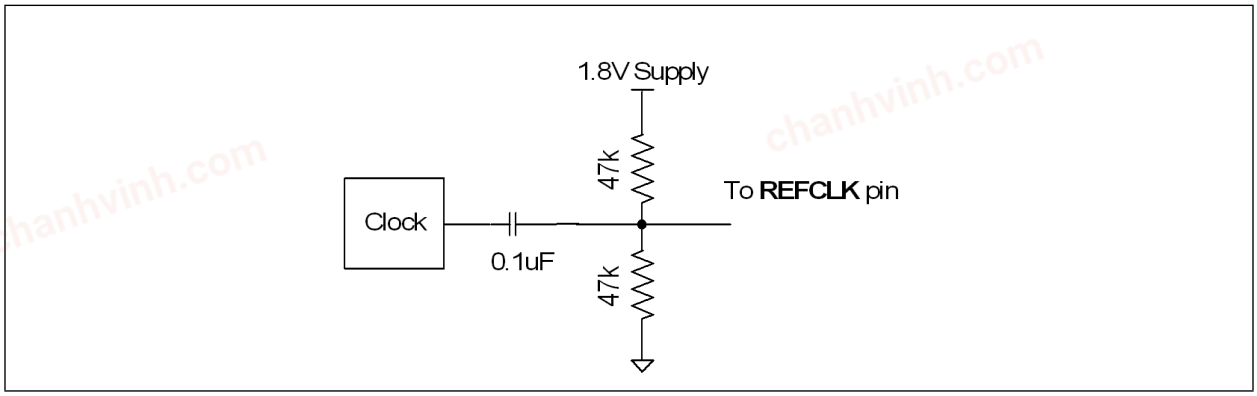


Figure 5.4 Example of Circuit Used to Shift a Reference Clock Common-mode Voltage Level

5.5.3 REFCLK Jitter

The USB3340 is tolerant to jitter on the reference clock. The **REFCLK** jitter should be limited to a peak to peak jitter of less than 1nS over a 10uS time interval. If this level of jitter is exceeded when configured for either ULPI Clock Input Mode or ULPI Clock Output Mode, the USB3340 High Speed eye diagram may be degraded.

The frequency accuracy of the REFCLK must meet the +/- 500ppm requirement as shown in Table 4.2.

5.5.4 REFCLK Enable/Disable

The **REFCLK** should be enabled when the **RESETB** pin is brought high. The ULPI interface will start running after the time specified in Table 4.2. If the reference clock enable is delayed relative to the **RESETB** pin, the ULPI interface will start operation delayed by the same amount. The reference clock can be run at anytime the **RESETB** pin is low without causing the USB3340 to start-up or draw current.

When the USB3340 is placed in Low Power Mode or Carkit Mode, the reference clock can be stopped after the final ULPI register write is complete. The **STP** pin is asserted to bring the USB3340 out of Low Power Mode. The reference clock should be started at the same time **STP** is asserted to minimize the USB3340 start-up time.

If the reference clock is stopped while in ULPI Synchronous mode the PLL will come out of lock and the frequency of oscillation will decrease to the minimum allowed by the PLL design. If the reference clock is stopped during a USB session, the session may drop.

5.6 Internal Regulators and POR

The USB3340 includes integrated power management functions, including a Low-Dropout regulator that can be used to generate the 3.3V USB supply, an integrated 1.8V regulator, and a POR generator described in Section 5.6.2.

5.6.1 Integrated Low Dropout Regulators

The USB3340 includes two integrated linear regulators. Power sourced at the **VBAT** pin is regulated to 3.3V and 1.8V output on the **VDD33** and **VDD18** pins. To ensure stability, both regulators require an external bypass capacitor as specified in Table 4.11 placed as close to the pin as possible.

The USB3340 regulators are designed to generate the 3.3 Volt and 1.8 Volt supplies for the USB3340 only. Using the regulators to provide current for other circuits is not recommended and Microchip does not guarantee USB performance or regulator stability.

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During USB UART mode the 3.3V regulator output voltage can be changed to allow the USB3340 to work with UARTs operating at different operating voltages. The 3.3V regulator output is configured to the voltages shown in Table 4.11 with the *UART RegOutput[1:0]* bits in the USB IO & Power Management register.

The regulators are enabled by the **RESETB** pin. When **RESETB** pin is low both regulators are disabled and the regulator outputs are pulled low by weak pull-down. The **RESETB** pin must be brought high to enable the regulators.

For peripheral-only or host-only bus-powered applications, the input to **VBAT** may be derived from the VBUS pin of the USB connector. In this configuration, the supply must be capable of withstanding any transient voltage present at the VBUS pin of the USB connector. Microchip does not recommend connecting the **VBAT** pin to the VBUS terminal of the USB connector.

5.6.2 Power On Reset (POR)

The USB3340 provides a POR circuit that generates an internal reset pulse after the **VDD18** supply is stable. After the internal POR goes high the USB3340 will release from reset and begin normal ULPI operation as described in Section 5.3.

The ULPI registers will power up in their default state summarized in Table 7.1 when the 1.8V supply comes up. Cycling the **RESETB** pin can also be used to reset the ULPI registers to their default state (and reset all internal state machines) by bringing the pin low for a minimum of 1 microsecond and then high. It is not necessary to wait for the **VDD33** and **VDD18** pins to discharge to 0 volts to reset the part.

The **RESETB** pin must be pulled high to enable the 3.3V and 1.8V regulators. A pull-down resistor is not present on the **RESETB** pin and therefore the system should drive the **RESETB** pin to the desired state at all times. If the system does not need to place the USB3340 into reset mode the **RESETB** pin can be connected to a supply between 1.8V and 3.3V.

5.6.3 Recommended Power Supply Sequence

For USB operation, the USB3340 requires a valid voltage on the **VBAT** and **VDDIO** pins. The **VDD33** and **VDD18** regulators are automatically enabled when the **RESETB** pin is brought high. Table 5.3 presents the power supply configurations in more detail.

The **RESETB** pin can be held low until the **VBAT** supply is stable. If the Link is not ready to interface the USB3340, the Link may choose to hold the **RESETB** pin low until it is ready to control the ULPI interface.

Table 5.3 Operating Mode vs. Power Supply Configuration

VBAT	VDDIO	RESETB	OPERATING MODES AVAILABLE
0	0	0	Powered Off
1	X	0	RESET Mode. (Note 5.3)
1	1	1	Full USB operation as described in Chapter 6.

Note 5.3 **VDDIO** must be present for ULPI pins to tri-state.

5.6.4 Start-Up

The power on default state of the USB3340 is ULPI Synchronous mode. The USB3340 requires the following conditions to begin operation: the power supplies must be stable, the **REFCLK** must be present and the **RESETB** pin must be high. After these conditions are met, the USB3340 will begin ULPI operation that is described in Chapter 6.

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Figure 5.5 below shows a timing diagram to illustrate the start-up of the USB3340. At T0, the supplies are stable and the USB3340 is held in reset mode. At T1, the Link drives **RESETB** high after the **REFCLK** has started. The **RESETB** pin may be brought high asynchronously to **REFCLK**. Once, the 3.3V and 1.8V internal supplies become stable the USB3340 will apply the 15Kohm pull downs to the data bus and assert **DIR** until the internal PLL has locked. After the PLL has locked, the USB3340 will check that the Link has de-asserted **STP** and at T2 it will de-assert **DIR** and begin ULPI operation.

The ULPI bus will be available as shown in Figure 5.5 in the time defined as T_{START} given in Table 4.2. If the **REFCLK** signal starts after the **RESETB** pin is brought high, then time T0 will begin when **REFCLK** starts. T_{START} also assumes that the Link has de-asserted **STP**. If the Link has held **STP** high the USB3340 will hold **DIR** high until **STP** is de-asserted. When the LINK de-asserts **STP**, it must be ready drive the ULPI data bus to idle (00h) for a minimum of one clock cycle after **DIR** de-asserts.

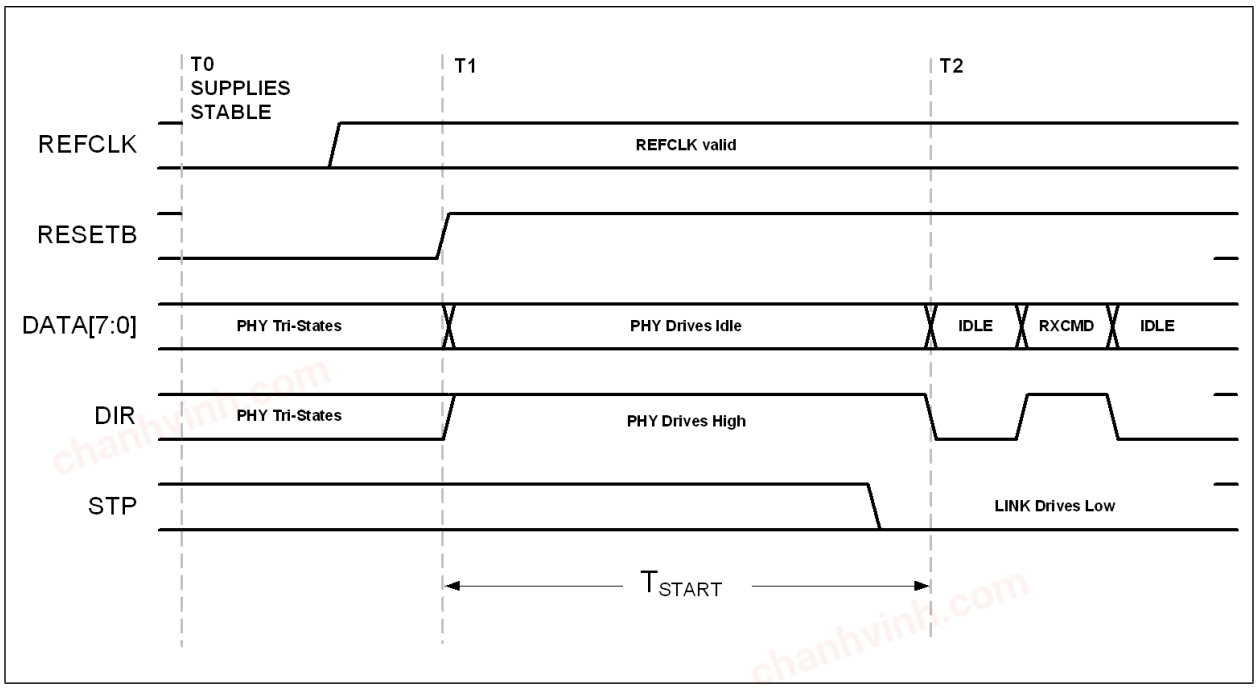


Figure 5.5 ULPI Start-up Timing

5.7 USB On-The-Go (OTG)

The USB3340 provides support for the USB OTG protocol. OTG allows the USB3340 to be dynamically configured as a host or peripheral depending on the type of cable inserted into the Micro-AB receptacle. When the Micro-A plug of a cable is inserted into the Micro-AB receptacle, the USB device becomes the A-device. When a Micro-B plug is inserted, the device becomes the B-device. The OTG A-device behaves similar to a Host while the B-device behaves similar to a peripheral. The differences are covered in the “On-The-Go Supplement to the USB 2.0 Specification”. In applications where only USB Host or USB Peripheral is required, the OTG Module is unused.

5.7.1 ID Resistor Detection

The ID pin of the USB connector is monitored by the **ID** pin of the USB3340 to detect the attachment of different types of USB devices and cables. For device only applications that do not use the ID signal the **ID** pin should be connected to **VDD33**. The block diagram of the ID detection circuitry is shown in Figure 5.6 and the related parameters are given in Table 4.8.

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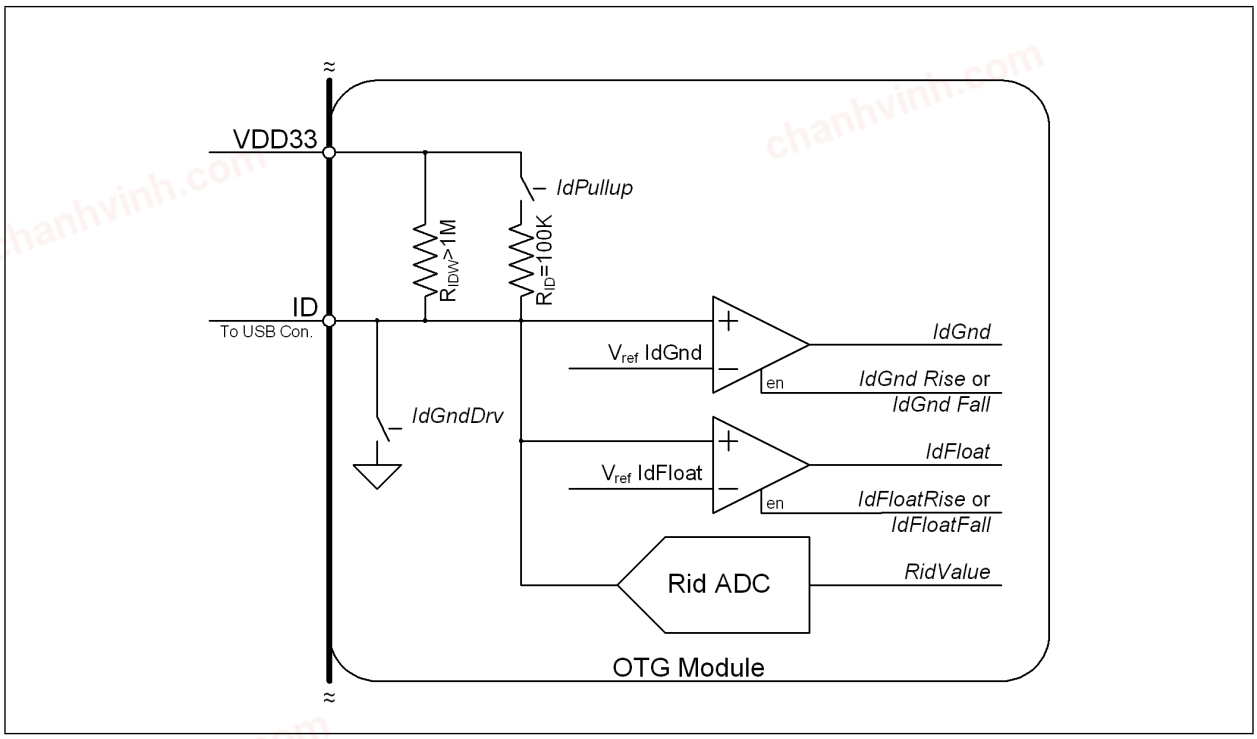


Figure 5.6 USB3340 ID Resistor Detection Circuitry

5.7.1.1 USB OTG Operation

The USB3340 can detect **ID** grounded and **ID** floating to determine if an A or B cable has been inserted. The A plug will ground the **ID** pin while the B plug will float the **ID** pin. These are the only two valid states allowed in the OTG Protocol.

To monitor the status of the **ID** pin, the Link activates the *IdPullup* bit in the OTG Control register, waits 50mS and then reads the status of the *IdGnd* bit in the USB Interrupt Status register. If an A cable has been inserted the *IdGnd* bit will read 0. If a B cable is inserted, the **ID** pin is floating and the *IdGnd* bit will read 1.

The USB3340 provides an integrated weak pull-up resistor on the **ID** pin, R_{IDW}. This resistor is present to keep the **ID** pin in a known state when the *IdPullup* bit is disabled and the **ID** pin is floated. In addition to keeping the **ID** pin in a known state, it enables the USB3340 to generate an interrupt to inform the link when a cable with a resistor to ground has been attached to the **ID** pin. The weak pull-up is small enough that the largest valid RID resistor pulls the **ID** pin low and causes the IdGnd comparator to go low.

After the link has detected an **ID** pin state change, the RID converter can be used to determine the resistor value as described in Section 5.7.1.2.

5.7.1.2 Measuring ID Resistance to Ground

The Link can use the integrated resistance measurement capabilities of the USB3340 to determine the value of an ID resistance to ground. The following table details the valid values of resistance to ground that the USB3340 can detect.

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Table 5.4 Valid Values of ID Resistance to Ground

ID RESISTANCE TO GROUND	RID VALUE
Ground	000
75Ω +/-1%	001
102kΩ +/-1%	010
200kΩ+/-1%	011
Floating	101

Note: IdPullUp = 0

The ID resistance to ground can be read while the USB3340 is in Synchronous Mode. When a resistor to ground is attached to the **ID** pin, the state of the IdGnd comparator will change. After the Link has detected **ID** transition to ground, it can use the methods described in Section 6.8 to operate the Rid converter.

5.7.1.3 Using IdFloat Comparator (not recommended)

Note: The ULPI specification details a method to detect a 102kΩ resistance to ground using the IdFloat comparator. This method can only detect 0ohms, 102kΩ, and floating terminations of the **ID** pin. Due to this limitation it is recommended to use the RID Converter as described in Section 5.7.1.2.

The **ID** pin can be either grounded, floated, or connected to ground with a 102kΩ external resistor. To detect the 102K resistor, set the *idPullup* bit in the OTG Control register, causing the USB3340 to apply the 100K internal pull-up connected between the **ID** pin and VDD33. Set the *idFloatRise* and *idFloatFall* bits in the Carkit Interrupt Enable register to enable the IdFloat comparator to generate an RXCMD to the Link when the state of the IdFloat changes. As described in Figure 6.3, the alt_int bit of the RXCMD will be set. The values of IdGnd and IdFloat are shown for the three types cables that can attach to the USB Connector in Table 5.5.

Table 5.5 IdGnd and IdFloat vs. ID Resistance to Ground

ID RESISTANCE	IDGND	IDFLOAT
Float	1	1
102K	1	0
GND	0	0

Note: The ULPI register bits *IdPullUp*, *IdFloatRise,* and *IdFloatFall* should be enabled.

To save current when an A Plug is inserted, the internal 102kΩ pull-up resistor can be disabled by clearing the *IdPullUp* bit in the OTG Control register and the *IdFloatRise* and *IdFloatFall* bits in both the USB Interrupt Enable Rising and USB Interrupt Enable Falling registers. If the cable is removed the weak R_{IDW} will pull the **ID** pin high.

The *IdGnd* value can be read using the ULPI USB Interrupt Status register, bit 4. In host mode, it can be set to generate an interrupt when *IdGnd* changes by setting the appropriate bits in the USB Interrupt Enable Rising and USB Interrupt Enable Falling registers. The *IdFloat* value can be read by reading the ULPI Carkit Interrupt Status register bit 0.

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Note: The IdGnd switch has been provided to ground the **ID** pin for future applications.

5.7.2 VBUS Monitoring and VBUS Pulsing

The USB3340 includes all of the VBUS comparators required for OTG. The VBUSVld, SessVld, and SessEnd comparators shown in Figure 5.7 are fully integrated into the USB3340. These comparators are used to monitor changes in the VBUS voltage, and the state of each comparator can be read from the USB Interrupt Status register.

The VbusVld comparator is used by the Link, when configured as an A device, to ensure that the VBUS voltage on the cable is valid. The SessVld comparator is used by the Link when configured as both an A or B device to indicate a session is requested or valid. Finally the SessEnd comparator is used by the B-device to indicate a USB session has ended.

Also included in the VBUS Monitor and Pulsing block are the resistors used for VBUS pulsing in SRP. The resistors used for VBUS pulsing include a pull-down to ground and a pull-up to **VDD33**.

In some applications, voltages much greater than 5.5V may be present at the VBUS pin of the USB connector. The USB3340 includes an over voltage protection circuit that protects the **VBUS** pin of the USB3340 from excessive voltages as shown in Figure 5.7.

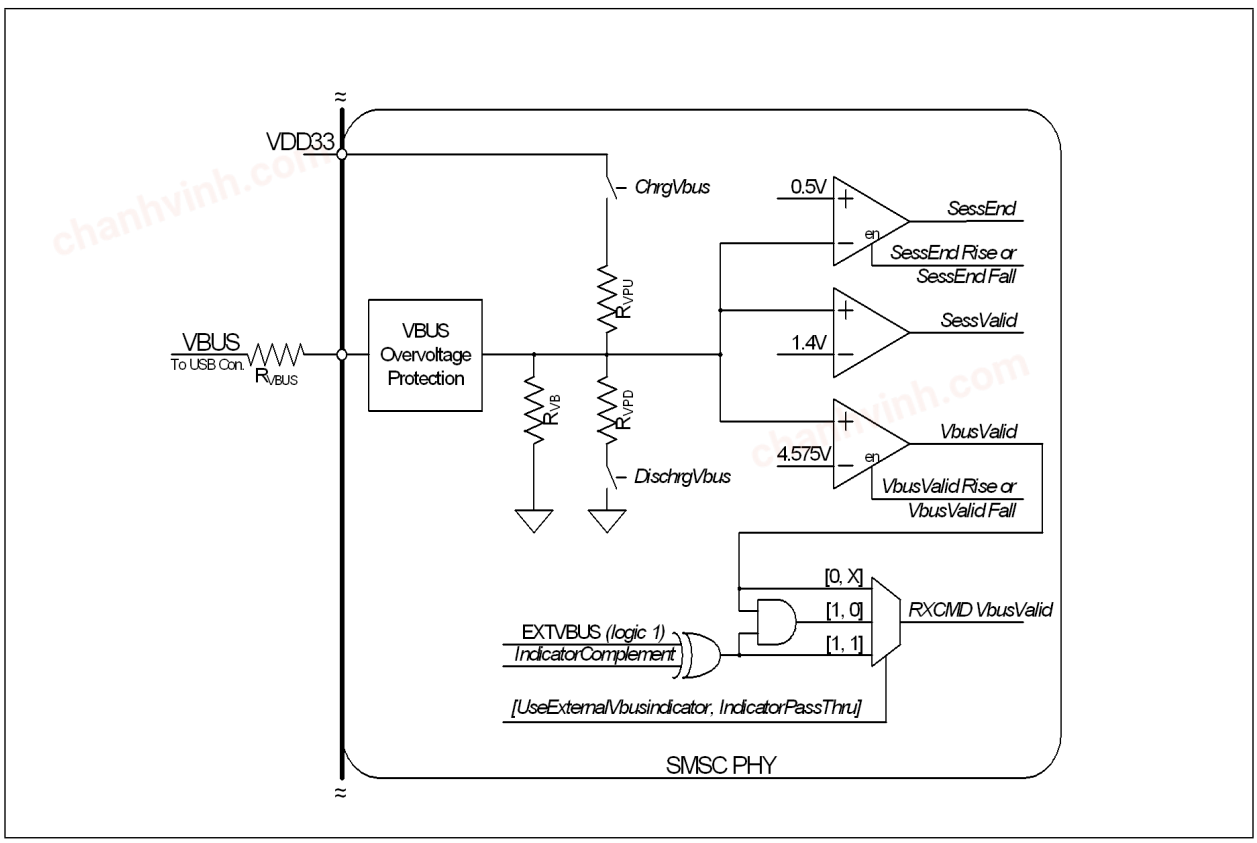


Figure 5.7 USB3340 OTG VBUS Block

5.7.2.1 SessEnd Comparator

The SessEnd comparator is used during the Session Request Protocol (SRP). The comparator is used by the B-device to detect when a USB session has ended and it is safe to start Vbus Pulsing to request a USB session from the A-device. When VBUS goes below the threshold in Table 4.7, the USB session is considered to be ended, and SessEnd will transition from 0 to 1. The SessEnd comparator can be

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disabled by clearing this bit in both the USB Interrupt Enable Rising and USB Interrupt Enable Falling registers. When disabled, the SessEnd bit in the USB Interrupt Status register will read 0.

The SessEnd Comparator is only used when configured as an OTG device. If the USB3340 is used as a Host or Device only the SessEnd Comparator should be disabled, using the method described above.

5.7.2.2 SessVld Comparator

The SessVld comparator is used when the PHY is configured as both an A and B device. When configured as an A device, the SessVld is used to detect Session Request protocol (SRP). When configured as a B device, SessVld is used to detect the presence of VBUS. The SessVld comparator output can also be read from the USB Interrupt Status register. The SessVld comparator will also generate an RX CMD, as detailed in Section 6.3.1, anytime the comparator changes state. The SessVld interrupts can be disabled by clearing this bit in both the USB Interrupt Enable Rising and USB Interrupt Enable Falling registers. When the interrupts are disabled, the SessVld comparator is still operational and will generate RX CMD's. The SessVld comparator trip point is detailed in Table 4.8.

Note: The OTG Supplement specifies a voltage range for A-Device Session Valid and B-Device Session Valid comparator. The USB3340 PHY combines the two comparators into one and uses the narrower threshold range.

5.7.2.3 VbusVld Comparator

The VbusVld comparator is only used when the USB3340 is configured as a host that can supply less than 100mA VBUS current. In the USB protocol, the A-device supplies the VBUS voltage and is responsible to ensure it remains within a specified voltage range. The VbusVld comparator can be disabled by clearing this bit in both the USB Interrupt Enable Rising and USB Interrupt Enable Falling registers. When disabled, bit 1 of the USB Interrupt Status register will return a 0. The VbusVld comparator threshold values are detailed in Table 4.8.

If the USB3340 is used as a Device only the VbusValid Comparator should be disabled, using the method described above.

The USB3340 includes the external VbusVld indicator logic as detailed in the ULPI Specification. The external VbusVld indicator is tied to a logic one. The decoding of this logic is shown in Table 5.6 below. By default this logic is disabled.

Table 5.6 External VBUS Indicator Logic

TYPICAL APPLICATION	USE EXTERNAL VBUS INDICATOR	INDICATOR PASS THRU	INDICATOR COMPLEMENT	RXCMD VBUS VALID ENCODING SOURCE
OTG Device	0	X	X	Internal VbusVld comparator (Default)
	1	1	0	Fixed 1
	1	1	1	Fixed 0
	1	0	0	Internal VbusVld comparator.
	1	0	1	Fixed 0
Standard Host	1	1	0	Fixed 1
	1	1	1	Fixed 0

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Table 5.6 External VBUS Indicator Logic

TYPICAL APPLICATION	USE EXTERNAL VBUS INDICATOR	INDICATOR PASS THRU	INDICATOR COMPLEMENT	RXCMD VBUS VALID ENCODING SOURCE
Standard Peripheral	0	X	X	Internal VbusVld comparator. This information should not be used by the Link. (Note 5.4)

Note 5.4 A peripheral should not use VbusVld to begin operation. The peripheral should use SessVld to detect the presence of VBUS on the USB connector. VbusVld should only be used for USB Host and OTG A-device applications.

5.7.2.4 VBUS Pulsing with Pull-up and Pull-down Resistors

In addition to the internal VBUS comparators, the USB3340 also includes the integrated VBUS pull-up and pull-down resistors used for VBUS Pulsing during OTG Session Request Protocol. To discharge the VBUS voltage so that a Session Request can begin, the USB3340 provides a pull-down resistor from **VBUS** to **GND**. This resistor is controlled by the *DischargeVbus* bit 3 of the OTG Control register. The pull-up resistor is connected between VBUS and VDD33. This resistor is used to pull VBUS above 2.1 volts so that the A-Device knows that a USB session has been requested. The state of the pull-up resistor is controlled by the bit 4 *ChargeVbus* of the OTG Control register. The Pull-Up and Pull-Down resistor values are detailed in Table 4.8.

The internal VBUS Pull-up and Pull-down resistors are designed to include the R_{VBUS} external resistor in series. This external resistor is used by the VBUS Over voltage protection described below.

5.7.2.5 VBUS Input Impedance

The OTG Supplement requires an A-Device that supports Session Request Protocol to have a VBUS input impedance less than 100kΩ and greater the 40kΩ to ground. The USB3340 provides a 75kΩ resistance to ground, R_{VB}. The R_{VB} resistor tolerance is detailed in Table 4.8.

5.7.2.6 VBUS Over Voltage Protection (OVP)

The USB3340 provides an integrated over voltage protection circuit to protect the **VBUS** pin from excessive voltages that may be present at the USB connector. The over voltage protection circuit works with an external resistor (R_{VBUS}) by drawing current across the resistor to reduce the voltage at the **VBUS** pin.

When voltage at the **VBUS** pin exceeds 5.5V, the Over voltage Protection block will sink current to ground until VBUS is below 5.5V. The current drops the excess voltage across R_{VBUS} and protects the USB3340 **VBUS** pin. The required R_{VBUS} value is dependent on the operating mode of the USB3340 as shown in Table 5.7.

Table 5.7 Required R_{VBUS} Resistor Value

OPERATING MODE	R_{VBUS}
Device only	20kΩ ±5%
OTG Host Capable of less than 100mA of current on VBUS	1kΩ ±5%
Host or OTG Host capable of >100mA UseExternalVbusIndicator = 1	20kΩ ±5%

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The Over voltage Protection circuit is designed to protect the USB3340 from continuous voltages up to 30V on the R_{VBUS} resistor.

The R_{VBUS} resistor must be sized to handle the power dissipated across the resistor. The resistor power can be found using the equation below:

$$P_{RVBUS} = \frac{(Vprotect - 5.0)^2}{R_{VBUS}}$$

Where:

- Vprotect is the VBUS protection required.
- R_{VBUS} is the resistor value, 1kΩ or 20kΩ.
- P_{RVBUS} is the required power rating of R_{VBUS}.

For example, protecting a peripheral or device only application to 15V would require a 20kΩ R_{VBUS} resistor with a power rating of 0.05W. To protect an OTG product to 15V would require a 1kΩ R_{VBUS} resistor with a power rating of 0.1W.

5.7.3 Driving External VBUS

The USB3340 monitors VBUS as described in VBUS Monitoring and VBUS Pulsing. The USB3340 does not provide an external output for the *DrvVbusExternal* ULPI register. For OTG and Host applications, the external VBUS supply or power switch must be controlled by the Link.

The USB3340 monitors VBUS as described in VBUS Monitoring and VBUS Pulsing. For OTG and Host applications, the system is required to source 5 volts on VBUS. The USB3340 fully supports VBUS power control using an external VBUS switch as shown in Figure 8.3. The USB3340 provides an active high control signal, **CPEN**, that is dedicated to controlling the Vbus supply when configured as an A-Device.

CPEN is asserted by setting the *DrvVbus* or *DrvVbusExternal* bit of the OTG Control register. To be compatible with Link designs that support both internal and external Vbus supplies the *DrvVbus* and *DrvVbusExternal* bits in the OTG Control Register are or'd together. This enables the Link to set either bit to access the external Vbus enable (**CPEN**). This logic is shown in Figure 5.8. *DrvVbus* and *DrvVbusExternal* are set to 0 on Power On Reset (POR) as shown in Section 7.1.1.7.

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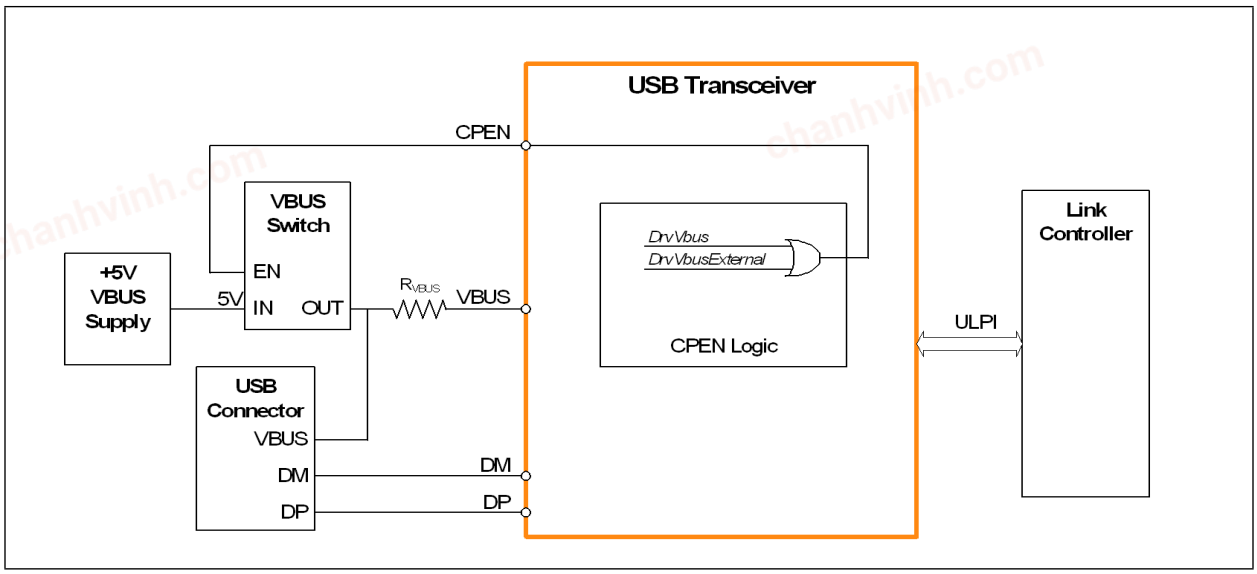


Figure 5.8 USB3340 Drives Control Signal (CPEN) to External Vbus Switch

5.8 USB UART Support

The USB3340 provides support for the USB UART interface as detailed in the ULPI specification and the former CEA-936A specification. The USB3340 can be placed in UART Mode using the method described in Section 6.7, and the regulator output will automatically switch to the value configured by the *UART RegOutput bits in the* USB IO & Power Management register. While in UART mode, the Linestate signals cannot be monitored on the DATA[0] and DATA[1] pins.

5.9 USB Charger Detection Support

The following blocks allow the USB3340 to detect when a Battery Charger, Charging Host Port, or a USB Host is attached to the USB connector. The USB3340 can also be configured to appear as a Charging Host Port, all according to the USB-IF Battery Charging 1.2 specification. The charger detection circuitry should be disabled during USB operation.

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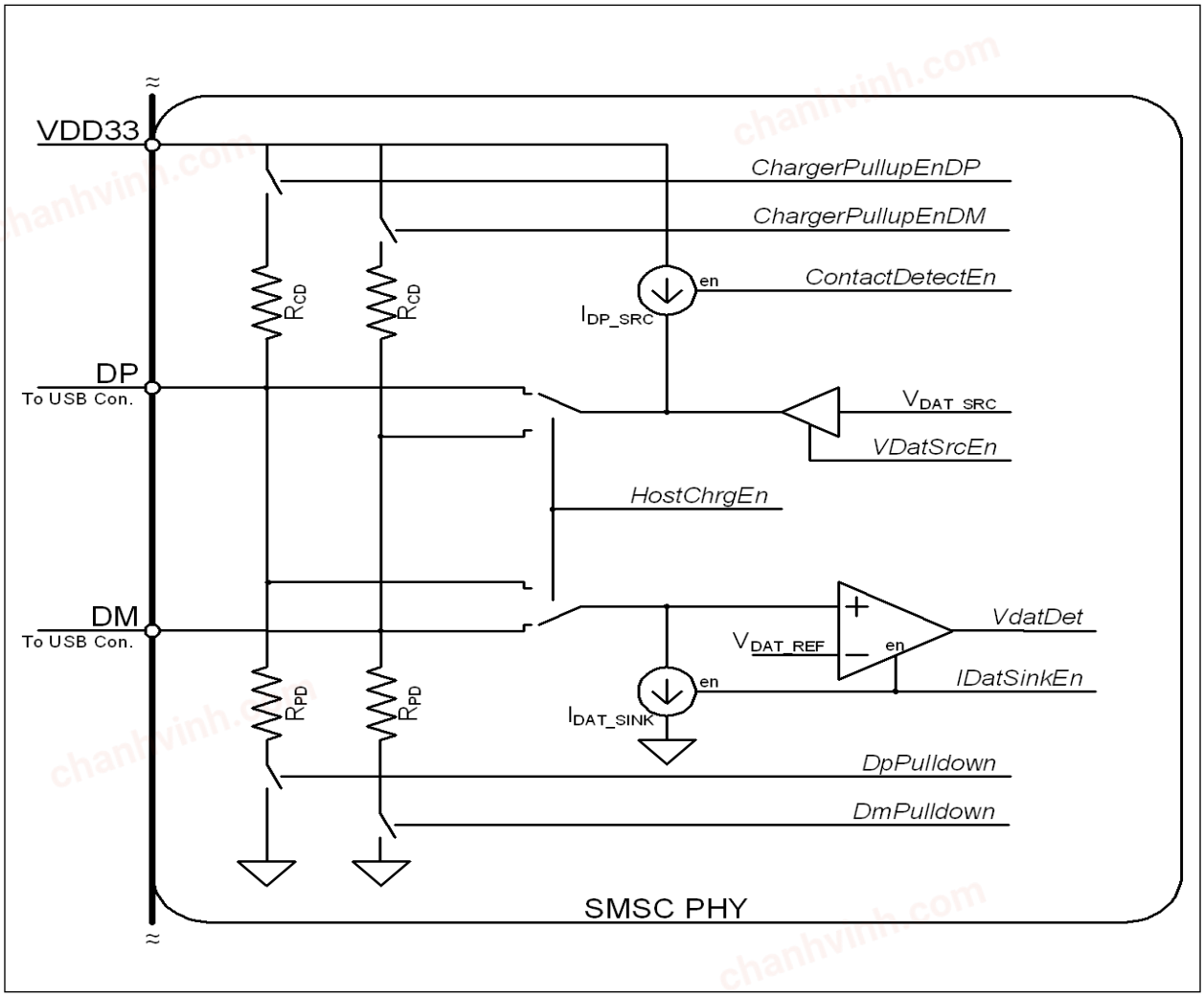


Figure 5.9 USB Charger Detection Block Diagram

Note: The *italic names* in the Figure 5.9 correspond to bits in the ULPI register set.

The charger detection circuitry runs from the **VDD33** supply and requires that the **VDD33** supply to be present to run the charger detection circuitry. The **VDD33** supply is present anytime the **RESETB** pin is pulled high and **VBAT** is present. The charger detection circuits are fully functional while in Low Power Mode (*Suspendm* = 0). The status of the *VdatDet* can be relayed back to the Link through the ULPI interrupts in both Synchronous mode and Low Power Mode.

5.9.1 Active Analog Charger Detection (USB-IF Battery Charging 1.2)

The USB3340 includes the active analog charger detection specified in the USB-IF Battery Charging Specification. The additional analog circuitry will allow the USB3340 to:

1. Detect a Dedicated Charging Port (DCP) with the DP and DM pins shorted together.
2. Detect a Standard Downstream Port (SDP) which has no battery charging circuitry.
3. Detect a Charging Downstream Port (CDP) which activly supplies voltage to the DM pin when connected to a USB-IF BC 1.2 compatible device.
4. Behave as a Charging Downstream Port by enabling the voltage source on the DM pin.

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The charger detection circuitry is shown in Figure 5.9.

The *VdatDet* output is qualified with the Linestate[1:0] value. If the Linestate is not equal to 00 the *VdatDet* signal will not assert.

The proper detection process flows through different modes of detection and uses the linestate and VdatDet signals values to determine the connection. Table 5.8 describes the bit values that need to be set to enter each mode.

Table 5.8 USB Charger Setting vs. Modes

CHARGER DETECTION MODES	VDATSRCEN	IDATSINKEN	CONTACTDETEN	HOSTCHRGEN	DPPULLDOWN	DMPULLDOWN
Device Connect Detect (The Connect Detect setting in Table 5.1 must be followed)	0	0	1	0	0	1
Device Charger Detection	1	1	0	0	0	0
Device Enhanced Charger Detection	1	1	0	1	0	0
Device USB Operation	0	0	0	0	0	0
Charging Host Port, no charging device attached and SE0 (*VdatDet* = 0)	0	1	0	1	1	1
Charging Host Port, charging device attached (*VdatDe*t = 1)	1	1	0	1	1	1
Charging Host Port USB Operation	0	0	0	1	1	1

5.9.1.1 Example Charger Detection Flow - Dedicated Charging Port

The USB-IF Battery Charging 1.2 specification describes in detail the flow for each charger type, but below is an example of the flow used to detect a Dedicated Charger (DCP).

1. Device detects Vbus voltage is present from RXCMD, (SESS_VLD is 1)
2. Device enters the *Device Connect Detect* mode.
   If the linestate still equals 10 after a specified timeout, the charger is an unknown charger and there will be no attempted USB enumeration.
   If the linestate equals 00 or 11, the device will go to the next mode:
3. Device enters *Device Charger Detection* mode.
   If the VdatDet bit is 0 then the host is a Standard Downstream Port (SDP) and the device will draw the standard 500mA of current and enter the *Device USB Operation* mode.
   If the VdatDet bit is 1 then the host is a charger that can supply at least 1.5A of current, the device will go to the next mode.
4. Device enters *Device Enhanced Charger Detection* mode.
   If the VdatDet bit is 0 then the device is connected to a Charging Downstream Port (CDP) and the device will enter the *Device USB Operation* mode.
   If the VdatDet bit is 1 then the device is connected to a Dedicated Charding Port (DCP) and the device will not try to enumerate.
5. The charger detection is complete.

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5.9.2 Resistive Charger Detection

Note: The Resistive Charger Detection has been superseded by the Active Analog Charger Detection (USB-IF Battery Charging 1.2) detailed above. It is recommended that new designs use the Active Analog Charger Detection (USB-IF Battery Charging 1.2).

To support the detection and identification of different types of USB chargers the USB3340 provides integrated pull-up resistors, R_{CD}, on both **DP** and **DM**. These pull-up resistors along with the single ended receivers can be used to determine the type of USB charger attached. Reference information on implementing charger detection is provided in Section 8.2.

Table 5.9 USB Weak Pull-up Enable

RESETB	DP PULLUP ENABLE	DM PULLUP ENABLE
0	0	0
1	*ChargerPullupEnableDP*	*ChargerPullupEnableDM*

Note: *ChargerPullupEnableDP* and *ChargerPullupEnableDM* are enabled in the USB IO & Power Management register.

5.10 USB Audio Support

Note: The USB3340 supports “USB Digital Audio” through the USB protocol in ULPI and USB Serial modes described in Section 6.

The USB3340 provides two low resistance analog switches that allow analog audio to be multiplexed over the DP and DM terminals of the USB connector. The audio switches are shown in . The electrical characteristics of the USB Audio Switches are provided in Table 4.10.

During normal USB operation the switches are off. When USB Audio is desired the switches can be turned “on” by enabling the *SpkLeftEn, SpkRightEn,* or *MicEn* bits in the Carkit Control register as described in Section 6.7.2. These bits are disabled by default.

The **RESETB** pin must be high when using the analog switches so that the **VDD33** supply is present. If the **VDD33** supply is applied externally and **RESETB** is held low the switches will be off.

In addition to USB Audio support the switches could also be used to multiplex a second Full Speed USB transceiver to the USB connector. The signal quality will be degraded slightly due to the “on” resistance of the switches. The USB3340 single-ended receivers described in Section 5.2.1 are enabled while in synchronous mode and are disabled when Carkit Mode is entered.

The USB3340 does not provide the DC bias for the audio signals. The **SPK_R** and **SPK_L** pins should be biased to 1.65V when audio signals are routed through the USB3340. This DC bias is necessary to prevent the audio signal from swinging below ground and being clipped by ESD Diodes.

When the system is not using the USB Audio switches, the **SPK_R** and **SPK_L** switches should be disabled.

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Chapter 6 ULPI Operation

6.1 ULPI Introduction

The USB3340 uses the industry standard ULPI digital interface for communication between the transceiver and Link (device controller). The ULPI interface is designed to reduce the number of pins required to connect a discrete USB transceiver to an ASIC or digital controller. For example, a full UTMI+ Level 3 OTG interface requires 54 signals while a ULPI interface requires only 12 signals.

The ULPI interface is documented completely in the “UTMI+ Low Pin Interface (ULPI) Specification Revision 1.1”. The following sections describe the operating modes of the USB3340 digital interface.

Figure 6.1 illustrates the block diagram of the ULPI digital functions. It should be noted that this USB3340 does not use a “ULPI wrapper” around a UTMI+ PHY core as the ULPI specification implies.

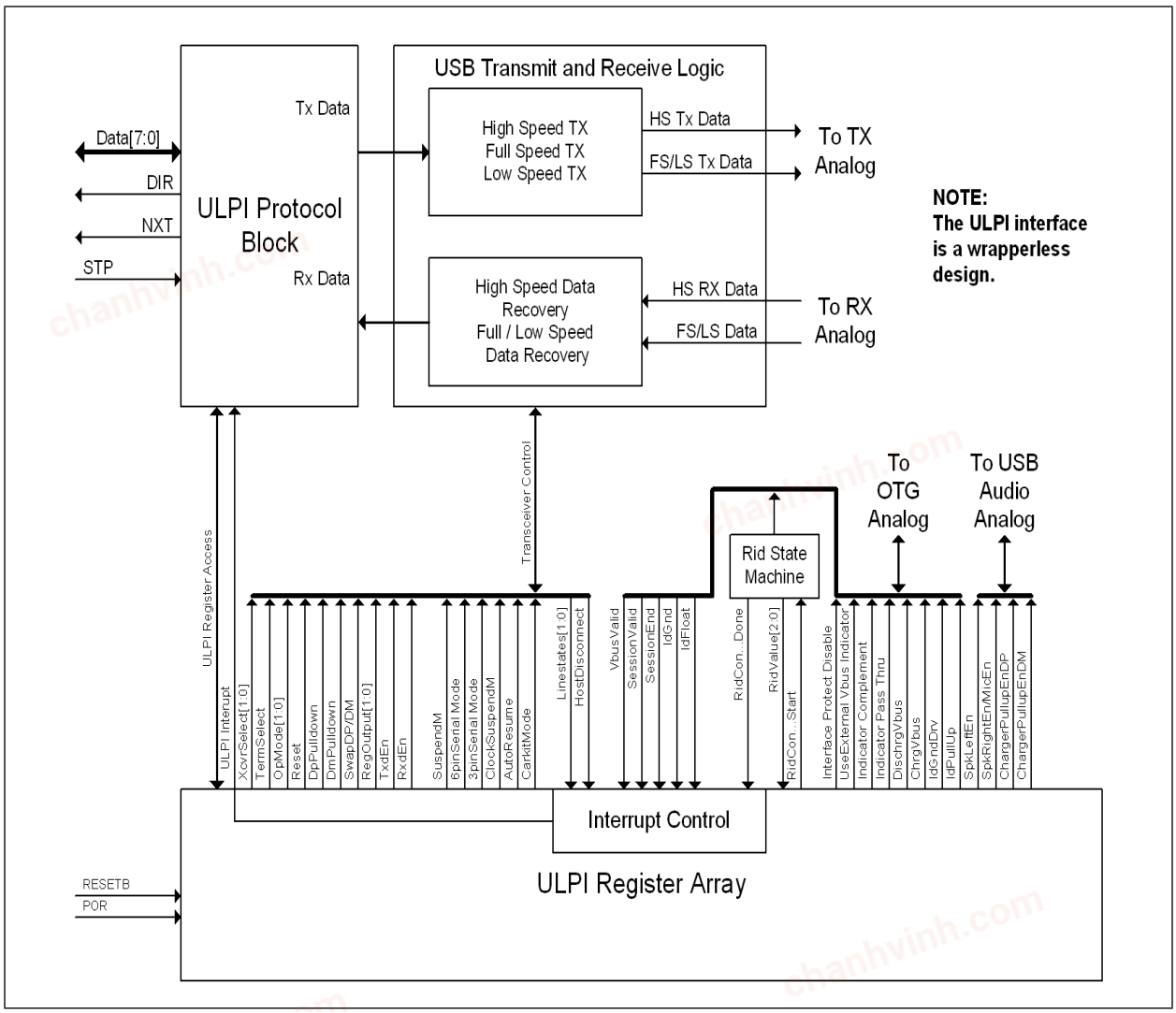


Figure 6.1 ULPI Digital Block Diagram

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The advantage of a “wrapper-less” architecture is that the USB3340 has a lower USB latency than a design which must first register signals into the PHY’s wrapper before the transfer to the transceiver core. A low latency PHY allows a wrapper around a UTMI Link to be used and still make the required USB turn-around timing required by the USB 2.0 specification.

RxEndDelay maximum allowed by the UTMI+/ULPI for 8-bit data is 63 Hi-Speed clocks. USB3340 uses a low latency Hi-Speed receiver path to lower the RxEndDelay to 43 Hi-Speed clocks. This low latency design gives the Link more cycles to make decisions and reduces the Link complexity. This is the result of the “wrapper less” architecture of the USB3340. This low RxEndDelay should allow legacy UTMI Links to use a “wrapper” to convert the UTMI+ interface to a ULPI interface.

In Figure 6.1, a single ULPI Protocol Block decodes the ULPI 8-bit bi-directional bus when the Link addresses the PHY. The Link must use the **DIR** output to determine direction of the ULPI data bus. The USB3340 is the “bus arbitrator”. The ULPI Protocol Block will route data/commands to the transmitter or the ULPI register array.

6.1.1 ULPI Interface Signals

The UTMI+ Low Pin Interface (ULPI) uses a 12-pin interface to connect a USB Transceiver to an external Link. The reduction of external pins, relative to UTMI+, is accomplished implementing the relatively static configuration pins (i.e. xcvrselect[1:0], termselect, opmode[1:0], and DpPullDown DmPulldown) as an internal register array.

An 8-bit bi-directional data bus clocked at 60MHz allows the Link to access this internal register array and transfer USB packets to and from the PHY. The remaining 3 pins function to control the data flow and arbitrate the data bus.

Direction of the 8-bit data bus is controlled by the **DIR** output from the PHY. Another output, **NXT**, is used to control data flow into and out of the device. Finally, **STP**, which is in input to the PHY, terminates transfers and is used to start up and resume from Low Power Mode.

The ULPI Interface signals are described below in Table 6.1.

Table 6.1 ULPI Interface Signals

SIGNAL	DIRECTION	DESCRIPTION
CLK	I/O	60MHz ULPI clock. All ULPI signals are driven synchronous to the rising edge of this clock. This clock can be either driven by the PHY or the Link as described in Section 5.5.1
DATA[7:0]	I/O	8-bit bi-directional data bus. Bus ownership is determined by DIR. The Link and PHY initiate data transfers by driving a non-zero pattern onto the data bus. ULPI defines interface timing for a single-edge data transfers with respect to rising edge of the ULPI clock.
DIR	OUT	Controls the direction of the data bus. When the PHY has data to transfer to the Link, it drives **DIR** high to take ownership of the bus. When the PHY has no data to transfer it drives **DIR** low and monitors the bus for commands from the Link. The PHY will pull **DIR** high whenever the interface cannot accept data from the Link, such as during PLL start-up.
STP	IN	The Link asserts **STP** for one clock cycle to stop the data stream currently on the bus. If the Link is sending data to the PHY, **STP** indicates the last byte of data was on the bus in the previous cycle.
NXT	OUT	The PHY asserts **NXT** to throttle the data. When the Link is sending data to the PHY, **NXT** indicates when the current byte has been accepted by the PHY. The Link places the next byte on the data bus in the following clock cycle.

USB3340 implements a Single Data Rate (SDR) ULPI interface with all data transfers happening on the rising edge of the 60MHz ULPI Clock while operating in Synchronous Mode. The direction of the

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data bus is determined by the state of **DIR**. When **DIR** is high, the PHY is driving **DATA[7:0]**. When **DIR** is low, the Link is driving **DATA[7:0]**.

Each time DIR changes, a “turn-around” cycle occurs where neither the Link nor PHY drive the data bus for one clock cycle. During the “turn-around“cycle, the state of **DATA[7:0]** is unknown and the PHY will not read the data bus.

Because USB uses a bit-stuffing encoding, some means of allowing the PHY to throttle the USB transmit data is needed. The ULPI signal **NXT** is used to request the next byte to be placed on the data bus by the Link.

The ULPI interface supports the two basic modes of operation: Synchronous Mode and Asynchronous Mode. Asynchronous Mode includes Low Power Mode, the Serial Modes, and Carkit Mode. In Synchronous Mode, all signals change synchronously with the 60MHz ULPI clock. In asynchronous modes the clock is off and the ULPI bus is redefined to bring out the signals required for that particular mode of operations. The description of synchronous Mode is described in the following sections while the descriptions of the asynchronous modes are described in Section 6.5, Section 6.6, and Section 6.7.

6.1.2 ULPI Interface Timing in Synchronous Mode

The control and data timing relationships are given in Figure 6.2 and Table 4.3. All timing is relative to the rising clock edge of the 60MHz ULPI Clock.

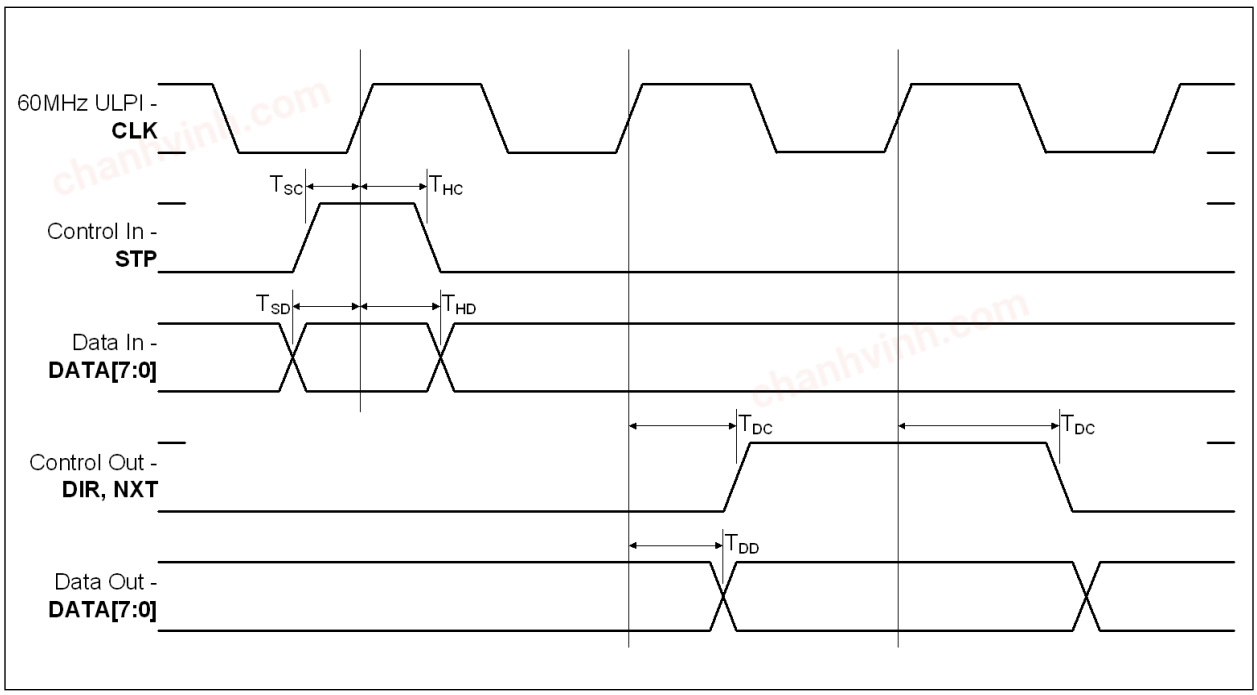


Figure 6.2 ULPI Single Data Rate Timing Diagram in Synchronous Mode

6.2 ULPI Register Access

The following section details the steps required to access registers through the ULPI interface. At any time **DIR** is low the Link may access the ULPI registers set using the Transmit Command byte. The ULPI registers retain their contents when the PHY is in Low Power Mode, Full Speed/Low Speed Serial Mode, or Carkit Mode.

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6.2.1 Transmit Command Byte (TX CMD)

A command from the Link begins a ULPI transfer from the Link to the USB3340. Before reading a ULPI register, the Link must wait until **DIR** is low, and then send a Transmit Command Byte (TX CMD) byte. The TX CMD byte informs the USB3340 of the type of data being sent. The TX CMD is followed by a data transfer to or from the USB3340. Table 6.2 gives the TX command byte (TX CMD) encoding for the USB3340. The upper two bits of the TX CMD instruct the PHY as to what type of packet the Link is transmitting.

Table 6.2 ULPI TX CMD Byte Encoding

COMMAND NAME	CMD BITS[7:6]	CMD BITS[5:0]	COMMAND DESCRIPTION
Idle	00b	000000b	ULPI Idle
Transmit	01b	000000b	USB Transmit Packet with No Packet Identifier (NOPID)
		00XXXXb	USB Transmit Packet Identifier (PID) where DATA[3:0] is equal to the 4-bit PID. $P_3P_2P_1P_0$ where P_3 is the MSB.
Register Write	10b	XXXXXXb	Immediate Register Write Command where: **DATA[5:0]** = 6-bit register address
		101111b	Extended Register Write Command where the 8-bit register address is available on the next cycle.
Register Read	11b	XXXXXXb	Immediate Register Read Command where: **DATA[5:0]** = 6-bit register address
		101111b	Extended Register Read Command where the 8-bit register address is available on the next cycle.

6.2.2 ULPI Register Write

A ULPI register write operation is given in Figure 6.3. The TX command with a register write **DATA[7:6]** = 10b is driven by the Link at T0. The register address is encoded into **DATA[5:0]** of the TX CMD byte.

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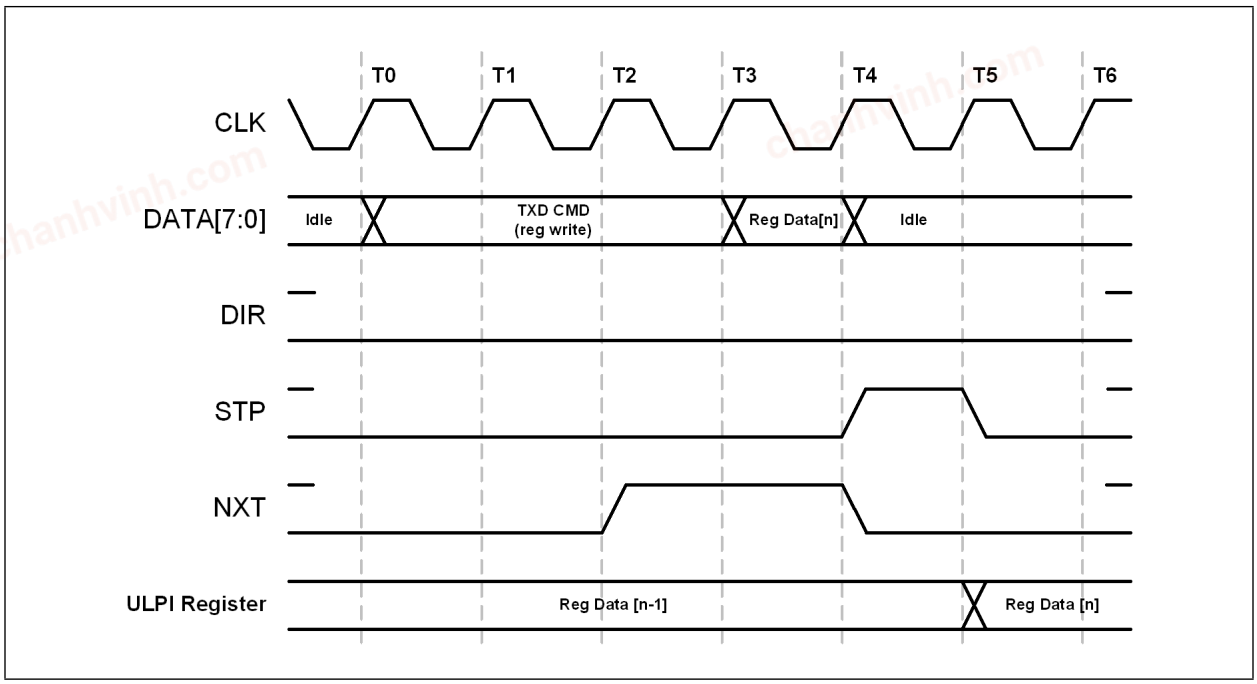


Figure 6.3 ULPI Register Write in Synchronous Mode

To write a register, the Link will wait until **DIR** is low, and at T0, drive the TX CMD on the data bus. At T2 the PHY will drive **NXT** high. On the next rising clock edge, T3, the Link will write the register data. At T4, the PHY will accept the register data and drive **NXT** low. The Link will drive an Idle on the bus and drive **STP** high to signal the end of the data packet. Finally, at T5, the PHY will latch the data into the register and the Link will pull **STP** low.

NXT is used to throttle when the Link drives the register data on the bus. **DIR** is low throughout this transaction since the PHY is receiving data from the Link. **STP** is used to end the transaction and data is registered after the de-assertion of **STP**. After the write operation completes, the Link must drive a ULPI Idle (00h) on the data bus. If the databus is not driven to idle the USB3340 may decode the non-zero bus value as an RX Command.

A ULPI extended register write operation is shown in Figure 6.4. To write an extended register, the Link will wait until **DIR** is low, and at T0, drive the TX CMD on the data bus. At T2 the PHY will drive **NXT** high. On the next clock T3 the Link will drive the extended address. On the next rising clock edge, T4, the Link will write the register data. At T5, the PHY will accept the register data and drive **NXT** low. The Link will drive an Idle on the bus and drive **STP** high to signal the end of the data packet. At T5, the PHY will latch the data into the register. Finally, at T6, the Link will drive **STP** low.

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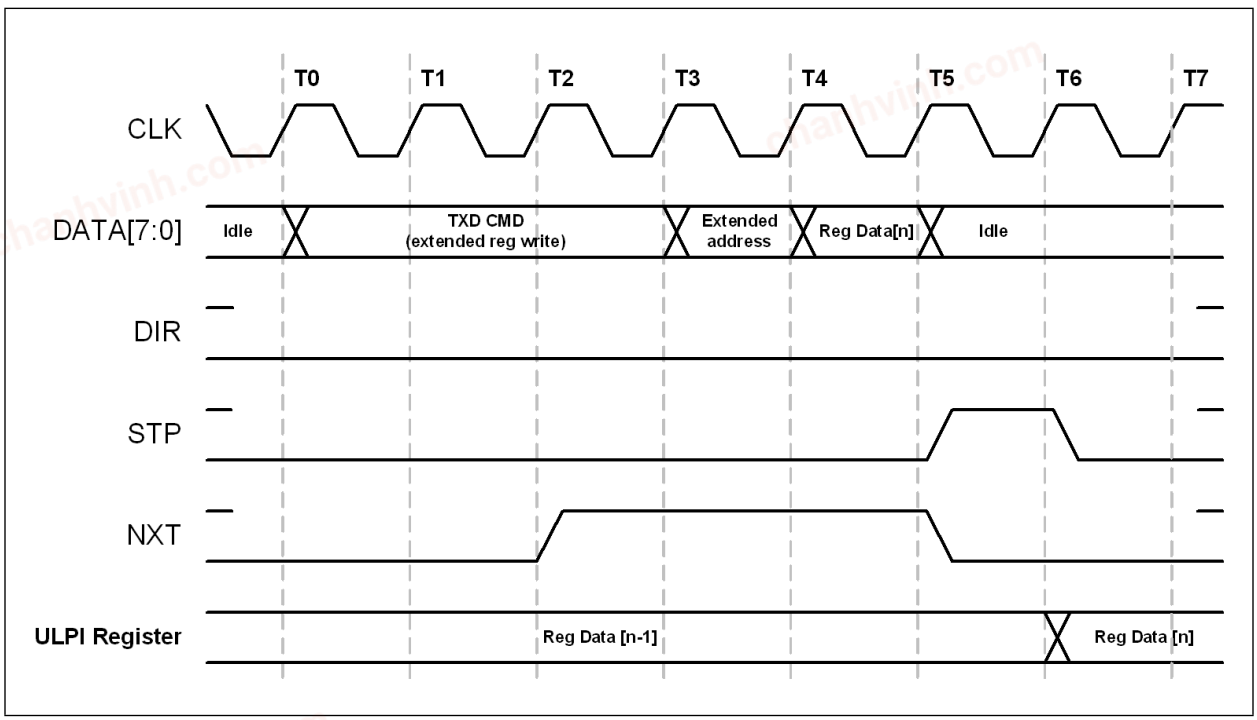


Figure 6.4 ULPI Extended Register Write in Synchronous Mode

6.2.3 ULPI Register Read

A ULPI register read operation is given in Figure 6.5. The Link drives a TX CMD byte with **DATA[7:6]** = 11h for a register read. **DATA[5:0]** of the ULPI TX command bye contain the register address.

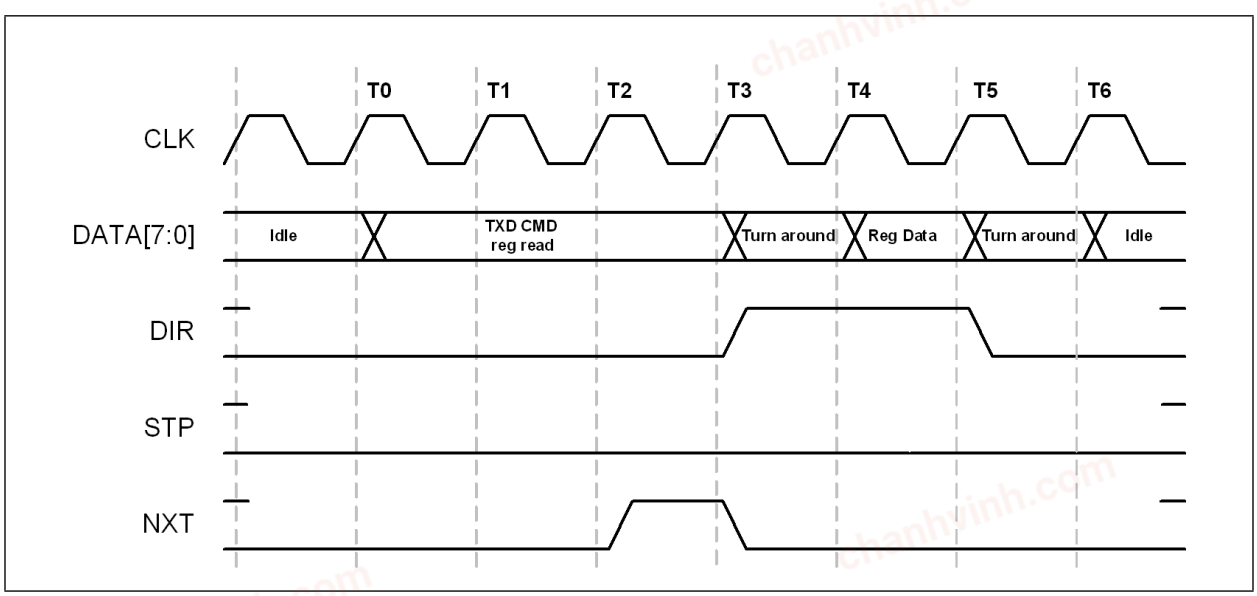


Figure 6.5 ULPI Register Read in Synchronous Mode

At T0, the Link will place the TX CMD on the data bus. At T2, the PHY will bring **NXT** high, signaling the Link it is ready to accept the data transfer. At T3, the PHY reads the TX CMD, determines it is a

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register read, and asserts **DIR** to gain control of the bus. The PHY will also de-assert **NXT**. At T4, the bus ownership has transferred back to the PHY and the PHY drives the requested register onto the data bus. At T5, the Link will read the data bus and the PHY will drop **DIR** low returning control of the bus back to the Link. After the turn around cycle, the Link must drive a ULPI Idle command at T6.

A ULPI extended register read operation is shown in Figure 6.6.To read an extended register, the Link writes the TX CMD with the address set to 2Fh. At T2, the PHY will assert **NXT**, signaling the Link it is ready to accept the extended address. At T3, the Link places the extended register address on the bus. At T4, the PHY reads the extended address, and asserts **DIR** to gain control of the bus. The PHY will also de-assert **NXT**. At T5, the bus ownership has transferred back to the PHY and the PHY drives the requested register onto the data bus. At T6, the Link will read the data bus and the PHY will de-assert **DIR** returning control of the bus back to the Link. After the turn around cycle, the Link must drive a ULPI Idle command at T6.

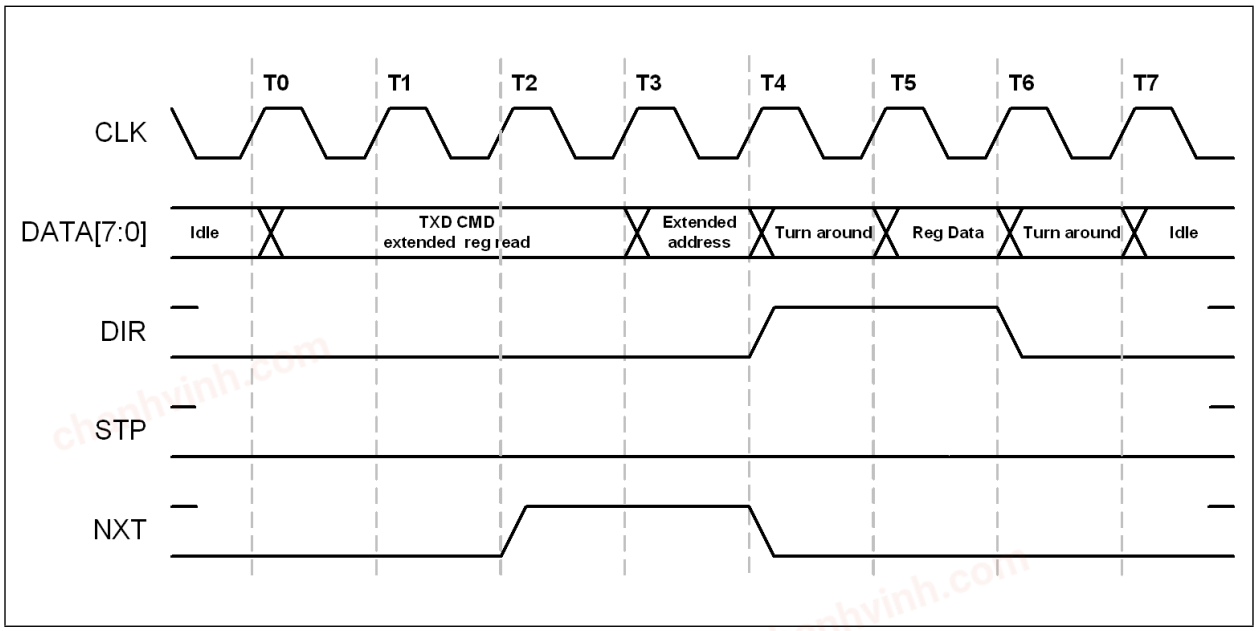


Figure 6.6 ULPI Extended Register Read in Synchronous Mode

6.3 USB3340 Receiver

The following section describes how the USB3340 uses the ULPI interface to receive USB signaling and transfer status information to the Link. This information is communicated to the Link using RX Commands to relay bus status and received USB packets.

6.3.1 ULPI Receive Command (RX CMD)

The ULPI Link needs information which was provided by the following pins in a UTMI implementation: linestate[1:0], rxactive, rxvalid, rxerror, and VbusValid. When implementing the OTG functions, the **VBUS** and **ID** pin states must also be transferred to the Link. ULPI defines a Receive Command Byte (RXCMD) that contains this information.

An RXCMD can be sent a any time the bus is idle. The RXCMD is initiated when the USB3340 asserts **DIR** to take control of the bus. The timing of RXCMD is shown in the figure below. The USB3340 can send single or back to back RXCMD's as required. The Encoding of the RXCMD byte is given in the Table 6.3.

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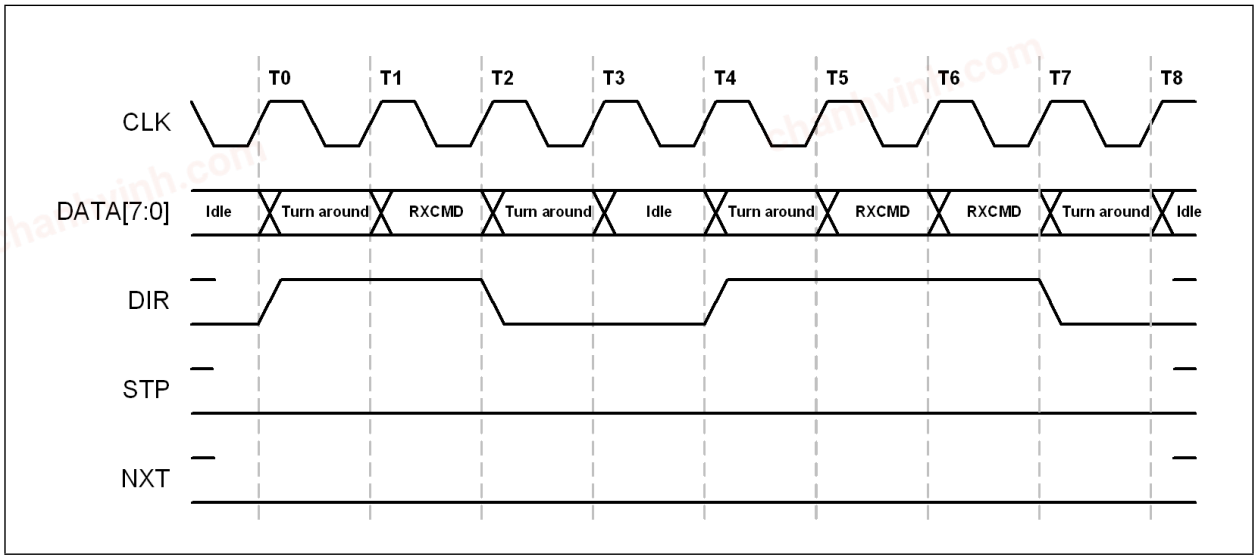


Figure 6.7 ULPI RXCMD Timing

Transfer of the RXCMD byte occurs in Synchronous Mode when the PHY has control of the bus. The ULPI Protocol Block shown in Figure 6.1 determines when to send an RXCMD. A RXCMD will occur:

- When a linestate change occurs.
- When VBUS or ID comparators change state.
- During a USB receive when **NXT** is low.
- After the USB3340 deasserts **DIR** and **STP** is low during start-up
- After the USB3340 exits Low Power Mode, Serial Modes, or Carkit Mode after detecting that the Link has de-asserted **STP**, and **DIR** is low.

When a USB Receive is occurring, RXCMD's are sent whenever **NXT** = 0 and **DIR** = 1. During a USB Transmit, the RXCMD's are returned to the Link after **STP** is asserted.

If an RXCMD event occurs during a Hi-Speed USB transmit, the RXCMD is blocked until **STP** de-asserts at the end of the transmit. The RXCMD contains the status that is current at the time the RXCMD is sent.

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Table 6.3 ULPI RX CMD Encoding

DATA[7:0]	NAME	DESCRIPTION AND VALUE				
[1:0]	Linestate	UTMI Linestate Signals. See Section 6.3.1.1				
[3:2]	Encoded VBUS State	**ENCODED VBUS VOLTAGE STATES**				
		VALUE	**VBUS VOLTAGE**	**SESSEND**	**SESSVLD**	**$VBUSVLD_2$**
		00	$V_{VBUS} < V_{SESS_END}$	1	0	0
		01	$V_{SESS_END} < V_{VBUS} < V_{SESS_VLD}$	0	0	0
		10	$V_{SESS_VLD} < V_{VBUS} < V_{VBUS_VLD}$	X	1	0
		11	$V_{VBUS_VLD} < V_{VBUS}$	X	X	1
[5:4]	Rx Event Encoding	**ENCODED UTMI EVENT SIGNALS**				
		VALUE	**RXACTIVE**	**RXERROR**	**HOSTDISCONNECT**	
		00	0	0	0	
		01	1	0	0	
		11	1	1	0	
		10	X	X	1	
[6]	State of **ID** pin	Set to the logic state of the **ID** pin. A logic low indicates an A device. A logic high indicates a B device.				
[7]	alt_int	Asserted when a non-USB interrupt occurs. This bit is set when an unmasked event occurs on any bit in the Carkit Interrupt Latch register. The Link must read the Carkit Interrupt Latch register to determine the source of the interrupt. Section 6.8 describes how an interrupt can be generated when the *RidConversionDone* bit is set.				

Notes:

1. An ‘X’ is a do not care and can be either a logic 0 or 1.
2. The value of VbusValid is defined in Table 5.6.

6.3.1.1 Definition of Linestate

The Linestate information is used to relay information back to the Link on the current status of the USB data lines, **DP** and **DM**. The definition of Linestate changes as the USB3340 transitions between LS/FS mode, HS mode, and HS Chirp.

6.3.1.1.1 LS/FS LINESTATE DEFINITIONS

In LS and FS operating modes the Linestate is defined by the outputs of the LS/FS Single Ended Receivers (SE RX). The logic thresholds for single ended receivers, V_{ILSE} and V_{ILSE} are shown in Table 4.5.

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Table 6.4 USB Linestate Decoding in FS and LS Mode

LINESTATE[1:0]		DP SE RX	DM SE RX	STATE
00	SE0	0	0	USB Reset
01	J (FS idle)	1	0	J State
10	K (LS Idle)	0	1	K State
11	SE1	1	1	SE1

Low Speed uses the same Linestate decoding threshold as Full Speed. Low Speed re-defines the Idle state as an inversion of the Full Speed idle to account for the inversion which occurs in the hub repeater path. Linestates are decoded exactly as in Table 6.4 with the idle as a K state.

6.3.1.1.2 HS LINESTATE DEFINITION

In HS mode the data transmission is too fast for Linestate to be transmitted with each transition in the data packet. In HS operation the Linestate is redefined to indicate activity on the USB interface. The Linestate will signal the assertion and de-assertion of squelch in HS mode.

Table 6.5 USB Linestate Decoding in HS Mode

LINESTATE[1:0]		DP SE RX	DM SE RX	STATE
00	SE0	0	0	HS Squelch asserted
01	J	1	0	HS Squelch de-asserted
10	K	0	1	Invalid State
11	SE1	1	1	Invalid State

6.3.1.1.3 HS CHIRP LINESTATE DEFINITION

There is also a third use of Linestate in HS Chirp where when the Host and Peripheral negotiate the from FS mode to HS mode. While the transitions from K to J or SE0 are communicated to the Link through the Linestate information.

Table 6.6 USB Linestate Decoding in HS Chirp Mode

LINESTATE[1:0]		DP SE RX	DM SE RX	STATE
00	SE0	0	0	HS Squelch asserted
01	J	1	0	HS Squelch de-asserted & HS differential Receiver = 1
10	K	0	1	HS Squelch de-asserted & HS differential Receiver = 0
11	SE1	1	1	Invalid State

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6.3.2 USB Receiver

The USB3340 ULPI receiver fully supports HS, FS, and LS transmit operations. In all three modes the receiver detects the start of packet and synchronizes to the incoming data packet. In the ULPI protocol, a received packet has the priority and will immediately follow register reads and RXCMD transfers. Figure 6.8 shows a basic USB packet received by the USB3340 over the ULPI interface.

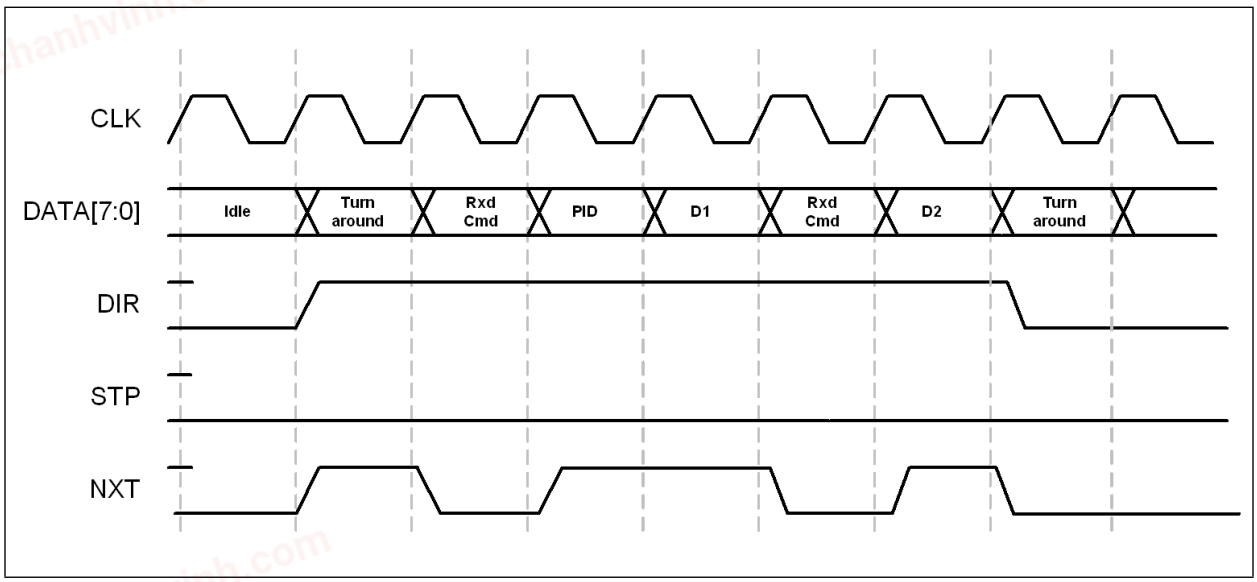


Figure 6.8 ULPI Receive in Synchronous Mode

In Figure 6.8 the PHY asserts **DIR** to take control of the data bus from the Link. The assertion of **DIR** and **NXT** in the same cycle contains additional information that Rxactive has been asserted. When **NXT** is de-asserted and **DIR** is asserted, the RXCMD data is transferred to the Link. After the last byte of the USB receive packet is transferred to the PHY, the linestate will return to idle.

The ULPI Full Speed receiver operates according to the UTMI / ULPI specification. In the Full Speed case, the **NXT** signal will assert only when the Data bus has a valid received data byte. When **NXT** is low with **DIR** high, the RXCMD is driven on the data bus.

In Full Speed, the USB3340 will not issue a Rxactive de-assertion in the RXCMD until the DP/DM linestate transitions to idle. This prevents the Link from violating the two Full Speed bit times minimum turn around time.

6.3.2.1 Disconnect Detection

A Hi-Speed host must detect a disconnect by sampling the transmitter outputs during the long EOP transmitted during a SOF packet. The USB3340 only looks for a Hi-Speed disconnect during the long EOP where the period is long enough for the disconnect reflection to return to the host PHY. When a Hi-Speed disconnect occurs, the USB3340 will return a RXCMD and set the host disconnect bit in the USB Interrupt Status register.

When in FS or LS modes, the Link is expected to handle all disconnect detection.

6.3.2.2 Link Power Management (LPM) Token Receive

The USB3340 is fully capable of receiving the Extended PID in the LPM token. When the LPM 0000b PID is received, this information is passed to the Link as a normal receive packet. If the Link chooses to enter LPM suspend, the procedure detailed in 6.5.3 can be followed.

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6.4 USB3340 Transmitter

The USB3340 ULPI transmitter fully supports HS, FS, and LS transmit operations. Figure 6.1 shows the Hi-Speed, Full Speed, and Low Speed transmitter block controlled by ULPI Protocol Block. Encoding of the USB packet follows the bit-stuffing and NRZI outlined in the USB 2.0 specification. Many of these functions are reused between the HS and FS/LS transmitters. When using the USB3340, Table 5.1 should always be used as a guideline on how to configure for various modes of operation. The transmitter decodes the inputs of *XcvrSelect[1:0]*, *TermSelect*, *OpMode[1:0]*, *DpPulldown,* and *DmPulldown* to determine what operation is expected. Users must strictly adhere to the modes of operation given in Table 5.1.

Several important functions for a device and host are designed into the transmitter blocks.

The USB3340 transmitter will transmit a 32-bit long Hi-Speed sync before every Hi-Speed packet. In Full and Low Speed modes a 8-bit sync is transmitted.

When the device or host needs to chirp for Hi-Speed port negotiation, the *OpMode* = 10 setting will turn off the bit-stuffing and NRZI encoding in the transmitter. At the end of a chirp, the USB3340 *OpMode* register bits should be changed only after the RXCMD linestate encoding indicates that the transmitter has completed transmitting. Should the opmode be switched to normal bit-stuffing and NRZI encoding before the transmit pipeline is empty, the remaining data in the pipeline may be transmitted in an bit-stuff encoding format.

Please refer to the ULPI specification for a detailed discussion of USB reset and HS chirp.

6.4.1 USB3340 Host Features

The USB3340 can also support USB Host operation and includes the following features that are required for Host operation.

6.4.1.1 Hi-Speed Long EOP

When operating as a Hi-Speed host, the USB3340 will automatically generate a 40 bit long End of Packet (EOP) after a SOF PID (A5h). The USB3340 determines when to send the 40-bit long EOP by decoding the ULPI TX CMD bits [3:0] for the SOF. The 40-bit long EOP is only transmitted when the *DpPulldown* and *DmPulldown* bits in the OTG Control register are asserted. The Hi-Speed 40-bit long EOP is used to detect a disconnect in mode.

In device mode, the USB3340 will not send a long EOP after a SOF PID.

6.4.1.2 Low Speed Keep-Alive

Low Speed keep alive is supported by the USB3340. When in Low Speed mode, the USB3340 will send out two Low Speed bit times of SE0 when a SOF PID is received.

6.4.1.3 UTMI+ Level 3

Pre-amble is supported for UTMI+ Level 3 compatibility. When *XcvrSelect* is set to (11b) in host mode, (*DpPulldown* and *DmPulldown* both asserted) the USB3340 will pre-pend a Full Speed pre-amble before the Low Speed packet. Full Speed rise and fall times are used in this mode. The pre-amble consists of the following: Full Speed sync, the encoded pre-PID (C3h) and then Full Speed idle (DP=1 and DM = 0). A Low Speed packet follows with a sync, data and a LS EOP.

The USB3340 will only support UTMI+ Level 3 as a host. The USB3340 does not support UTMI+ Level 3 as a peripheral. A UTMI+ Level 3 peripheral is an upstream hub port. The USB3340 will not decode a pre-amble packet intended for a LS device when the USB3340 is configured as the upstream port of a FS hub, *XcvrSelect* = 11b, *DpPulldown* = 0b, *DmPulldown* =0b.

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6.4.1.4 Host Resume K

Resume K generation is supported by the USB3340. At the end of a USB Suspend the PHY will drive a K back to the downstream device. When the USB3340 exits from Low Power Mode, when operating as a host, it will automatically transmit a Resume K on DP/DM. The transmitters will end the K with SE0 for two Low Speed bit times. If the USB3340 was operating in Hi-Speed mode before the suspend, the host must change to Hi-Speed mode before the SE0 ends. SE0 is two Low Speed bit times which is about 1.2 us. For more details please see sections 7.1.77 and 7.9 of the USB Specification.

In device mode, the resume K will not append an SE0, but release the bus to the correct idle state, depending upon the operational mode as shown in Table 5.1.

The ULPI specification includes a detailed discussion of the resume sequence and the order of operations required. To support Host start-up of less than 1mS the USB3340 implements the ULPI *AutoResume* bit in the Interface Control register. The default *AutoResume* state is 0 and this bit should be enabled for Host applications.

6.4.1.5 No SYNC and EOP Generation (*OpMode* = 11)

UTMI+ defines O*pMode* = 11 where no sync and EOP generation occurs in Hi-Speed operation. This is an option to the ULPI specification and not implemented in the USB3340.

6.4.2 Typical USB Transmit with ULPI

Figure 6.9 shows a typical USB transmit sequence. A transmit sequence starts by the Link sending a TX CMD where **DATA[7:6]** = 01b, **DATA[5:4]** = 00b, and **Data[3:0]** = PID. The TX CMD with the PID is followed by transmit data.

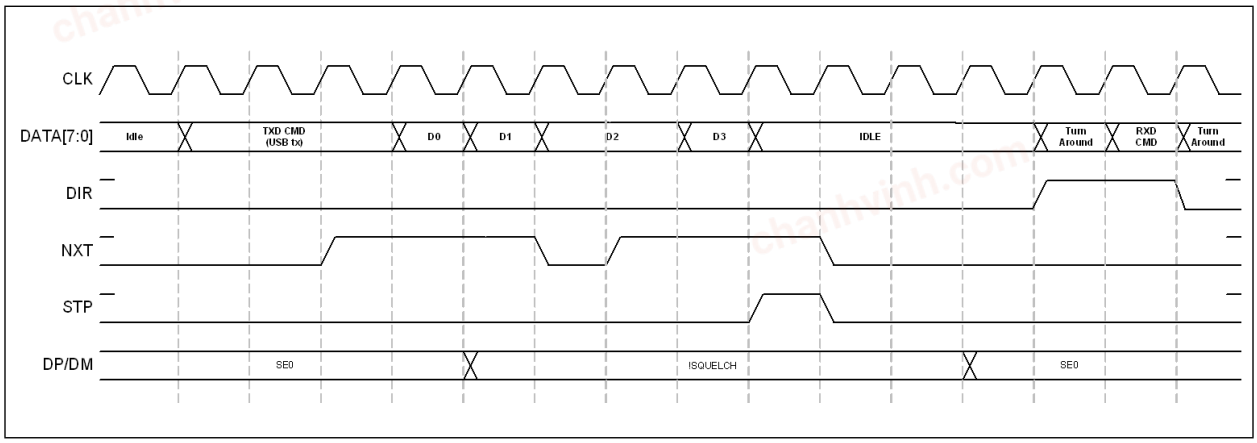


Figure 6.9 ULPI Transmit in Synchronous Mode

During transmit the PHY will use **NXT** to control the rate of data flow into the PHY. If the USB3340 pipeline is full or bit-stuffing causes the data pipeline to overfill **NXT** is de-asserted and the Link will hold the value on Data until **NXT** is asserted. The USB Transmit ends when the Link asserts **STP** while **NXT** is asserted.

Note: The Link cannot assert **STP** with **NXT** de-asserted since the USB3340 is expecting to fetch another byte from the Link.

After the USB3340 completes transmitting, the **DP** and **DM** lines return to idle and a RXCMD is returned to the Link so the inter-packet timers may be updated by linestate.

While operating in Full Speed or Low Speed, an End-of-Packet (EOP) is defined as SE0 for approximately two bit times, followed by J for one bit time. The transceiver drives a J state for one bit time following the SE0 to complete the EOP. The Link must wait for one bit time following line state

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indication of the SE0 to J transition to allow the transceiver to complete the one bit time J state. All bit times are relative to the speed of transmission.

In the case of Full Speed or Low Speed, after **STP** is asserted each FS/LS bit transition will generate a RXCMD since the bit times are relatively slow.

6.4.2.1 Link Power Management Token Transmit

A Host Link can send a LPM command using the USB3340. When sending the LPM token the normal transmit method is not used. Sending a LPM token requires the USB3340 to send a 0000b or 'F0' PID. When the ULPI specification was defined the 'F0' PID was not defined. The ULPI specification used the "Reserved" 'F0' PID to signal chirp and resume signaling while using *OpMode* 10b. While in *OpMode* 00b the USB3340 is able to generate the 'F0' PID as shown below.

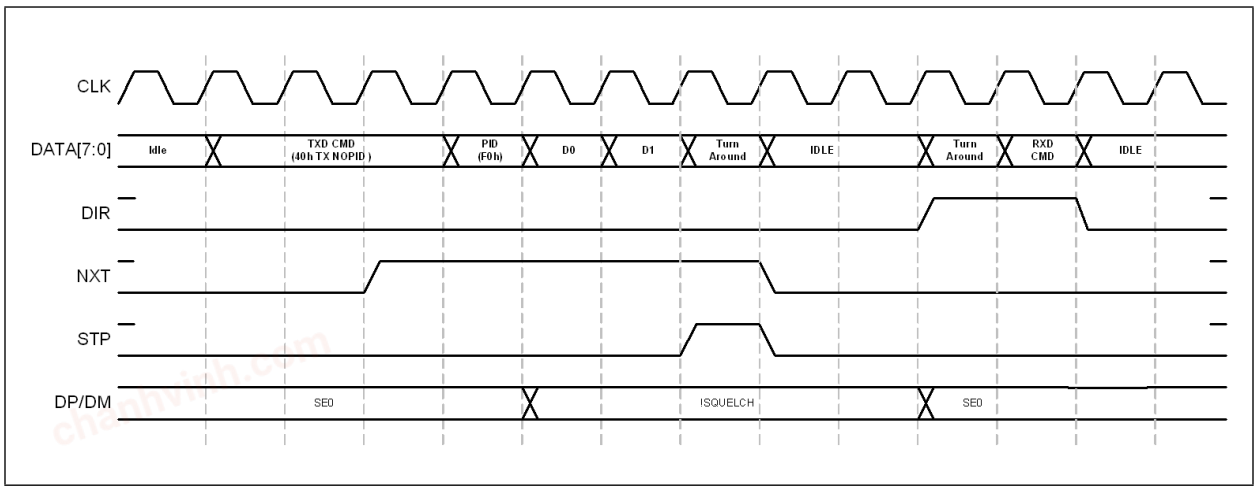


Figure 6.10 LPM Token Transmit

To send the 'F0' PID, the link will be required to use the TX CMD with NOPID to initiate the transmit and then follow up the TX CMD with the 'F0' PID. The data bytes follow as in a normal transmit, in *OpMode* 00b. The key difference is in that the link will have to send the PID the same as it would send a data packet. The USB3340 is able to recognize the LPM transmit and correctly send the PID information.

6.5 Low Power Mode

Low Power Mode is a power down state to save current when the USB session is suspended. The Link controls when the PHY is placed into or out of Low Power Mode. In Low Power Mode all of the circuits are powered down except the interface pins, Full Speed receiver, VBUS comparators, and IdGnd comparator. The VBUS and ID comparators can optionally be powered down to save current as shown in Section 6.5.5.

Before entering Low Power Mode, the USB3340 must be configured to set the desired state of the USB transceiver. The *XcvrSelect[1:0]*, *TermSelect* and *OpMode[1:0]* bits in the Function Control register, and the *DpPulldown* and *DmPulldown* bits in the OTG Control register control the configuration as shown in Table 5.1. The **DP** and **DM** pins are configured to a high impedance state by configuring *OpMode[1:0]* = 01 as shown in the programming example in Table 6.8. Pull-down resistors with a value of approximately 2MΩ are present on the **DP** and **DM** pins to avoid false linestate indications that could result if the pins were allowed to float.

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6.5.1 Entering Low Power/Suspend Mode

To enter Low Power Mode, the Link will write a 0 or clear the *SuspendM* bit in the Function Control register. After this write is complete, the PHY will assert **DIR** high and after a minimum of five rising edges of **CLKOUT**, drive the clock low. After the clock is stopped, the PHY will enter a low power state to conserve current. Placing the PHY in Suspend Mode is not related to USB Suspend. To clarify this point, USB Suspend is initiated when a USB host stops data transmissions and enters Full-Speed mode with 15KΩ pull-down resistors on **DP** and **DM**. The suspended device goes to Full-Speed mode with a pull-up on **DP**. Both the host and device remain in this state until one of them drives **DM** high (this is called a resume).

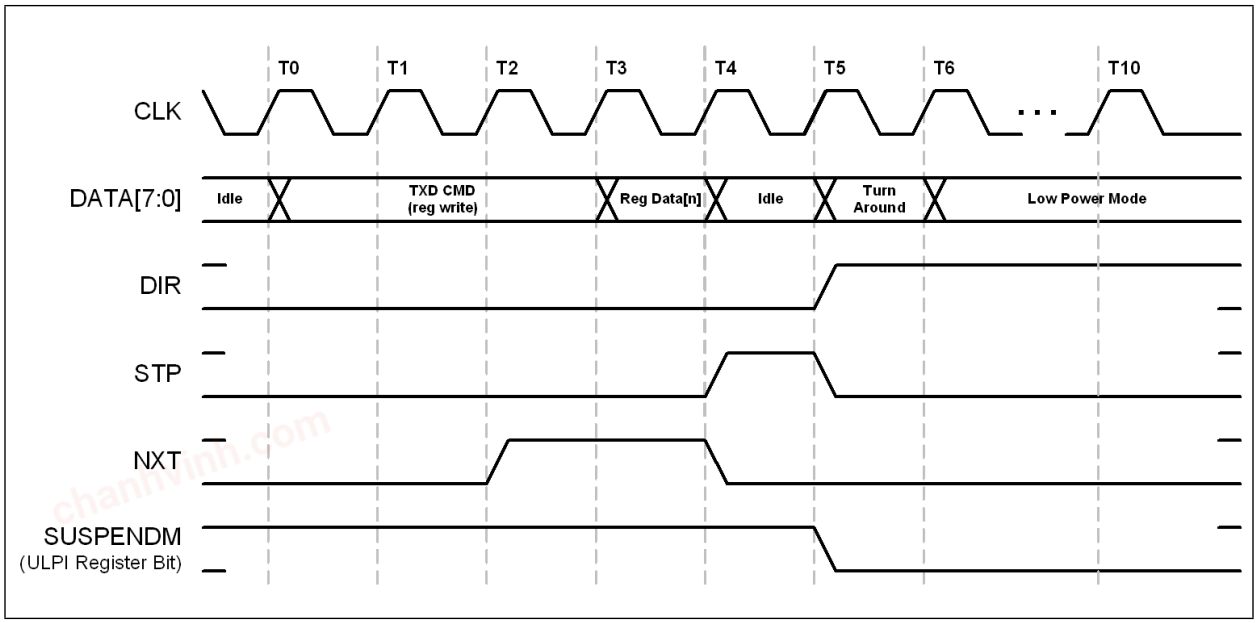


Figure 6.11 Entering Low Power Mode from Synchronous Mode

While in Low Power Mode, the Data interface is redefined so that the Link can monitor Linestate and the VBUS voltage. In Low Power Mode **DATA[3:0]** are redefined as shown in Table 6.7. Linestate[1:0] is the combinational output of the Single-Ended Receivers. The “int” or interrupt signal indicates an unmasked interrupt has occurred. When an unmasked interrupt or linestate change has occurred, the Link is notified and can determine if it should wake-up the PHY.

Table 6.7 Interface Signal Mapping During Low Power Mode

SIGNAL	MAPS TO	DIRECTION	DESCRIPTION
linestate[0]	**DATA[0]**	OUT	Combinatorial LineState[0] driven directly by the Full-Speed single ended receiver. Note 6.1
linestate[1]	**DATA[1]**	OUT	Combinatorial LineState[1] driven directly by the Full-Speed single ended receiver. Note 6.1
reserved	**DATA[2]**	OUT	Driven Low
int	**DATA[3]**	OUT	Active high interrupt indication. Must be asserted whenever any unmasked interrupt occurs.
reserved	**DATA[7:4]**	OUT	Driven Low

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Note 6.1 LineState: These signals reflect the current state of the Full-Speed single ended receivers. LineState[0] directly reflects the current state of **DP**. LineState[1] directly reflects the current state of **DM**. When **DP=DM**=0 this is called "Single Ended Zero" (SE0). When **DP=DM**=1, this is called "Single Ended One" (SE1).

An unmasked interrupt can be caused by the following comparators changing state: VbusVld, SessVld, SessEnd, and IdGnd. If any of these signals change state during Low Power Mode and the bits are enabled in either the USB Interrupt Enable Rising or USB Interrupt Enable Falling registers, **DATA[3]** will assert. During Low Power Mode, the VbusVld and SessEnd comparators can have their interrupts masked to lower the suspend current as described in Section 6.5.5.

While in Low Power Mode, the Data bus is driven asynchronously because all of the PHY clocks are stopped during Low Power Mode.

6.5.2 Exiting Low Power Mode

To exit Low Power Mode, the Link will assert **STP**. Upon the assertion of **STP**, the USB3340 will begin its start-up procedure. After the PHY start-up is complete, the PHY will start the clock on **CLKOUT** and de-assert **DIR**. After **DIR** has been de-asserted, the Link can de-assert **STP** when ready and start operating in Synchronous Mode. The PHY will automatically set the *SuspendM* bit to a 1 in the Function Control register.

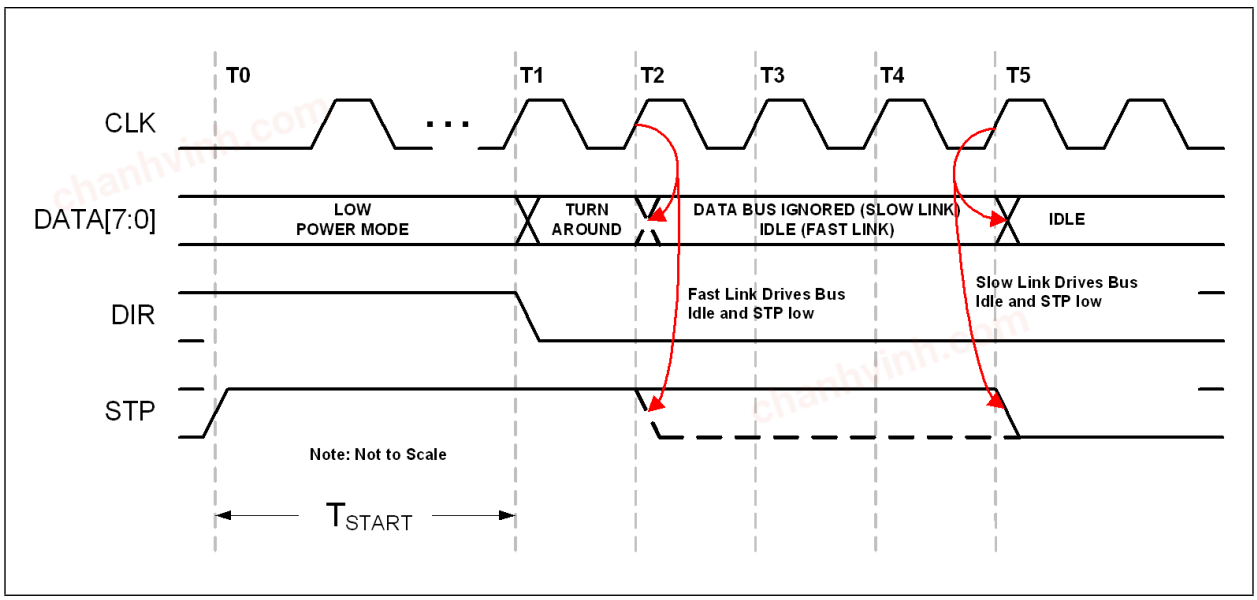


Figure 6.12 Exiting Low Power Mode

The value for T_{START} is given in Table 4.2.

Should the Link de-assert **STP** before **DIR** is de-asserted, the USB3340 will detect this as a false resume request and return to Low Power Mode. This is detailed in Section 3.9.4 of the UTMI+ Low Pin Interface (ULPI) Specification Revision 1.1.

6.5.3 Link Power Management (LPM)

When the USB3340 is operating with a Link capable of Link Power Management, the Link will place the USB3340 in and out of suspend rapidly to conserve power. The USB3340 provides a fast suspend recovery that allows the USB3340 to meet the suspend recovery time detailed in the Link Power Management ECN to the USB 2.0 specification.

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When the Link places the USB3340 into suspend during Link Power Management, the *LPM Enable* bit of the HS Compensation Register must be set to 1. This allows the USB3340 to start-up in the time specified in Table 4.2.

6.5.4 Interface Protection

ULPI protocol assumes that both the Link and PHY will keep the ULPI data bus driven by either the Link when **DIR** is low or the PHY when **DIR** is high. The only exception is when **DIR** has changed state and a turn around cycle occurs for 1 clock period.

In the design of a USB system, there can be cases where the Link may not be driving the ULPI bus to a known state while **DIR** is low. Two examples where this can happen is because of a slow Link start-up or a hardware reset.

6.5.4.1 Start up Protection

Upon start-up, when the PHY de-asserts **DIR**, the Link must be ready to receive commands and drive Idle on the data bus. If the Link is not ready to receive commands or drive Idle, it must assert **STP** before **DIR** is de-asserted. The Link can then de-assert **STP** when it has completed its start-up. If the Link doesn't assert **STP** before it can receive commands, the **PHY** may interpret the data bus state as a TX CMD and transmit invalid data onto the **USB** bus, or make invalid register writes.

When the USB3340 sends a RXCMD the Link is required to drive the data bus back to idle at the end of the turn around cycle. If the Link does not drive the databus to idle the USB3340 may take the information on the data bus as a TXCMD and transmit data on **DP** and **DM** until the Link asserts stop. If the **ID** pin is floated the last RXCMD from the USB3340 will remain on the bus after **DIR** is de-asserted and the USB3340 will take this in as a TXCMD.

A Link should be designed to have the default POR state of the **STP** output high and the data bus tri-stated. The USB3340 has weak pull-downs on the data bus to prevent these inputs from floating when not driven. These resistors are only used to prevent the ULPI interface from floating during events when the link ULPI pins may be tri-stated. The strength of the pull down resistors can be found in Table 4.4. The pull downs are not strong enough to pull the data bus low after a ULPI RXCMD, the Link must drive the data bus to idle after **DIR** is de-asserted.

In some cases, a Link may be software configured and not have control of its **STP** pin until after the PHY has started. In this case, the USB3340 has in internal pull-up on the **STP** input pad which will pull **STP** high while the Link's **STP** output is tri-stated. The **STP** pull-up resistor is enabled on POR and can be disabled by setting the *InterfaceProtectDisable* bit 7 of the Interface Control register.

The **STP** pull-up resistor will pull-up the Link's **STP** input high until the Link configures and drives **STP** high. After the Link completes its start-up, **STP** can be synchronously driven low.

A Link design which drives **STP** high during POR can disable the pull-up resistor on **STP** by setting *InterfaceProtectDisable* bit to 1. A motivation for this is to reduce the suspend current. In Low Power Mode, **STP** is held low, which would draw current through the pull-up resistor on **STP**.

6.5.4.2 Warm Reset

Designers should also consider the case of a warm restart of a Link with a PHY in Low Power Mode. After the PHY enters Low Power Mode, **DIR** is asserted and the clock is stopped. The USB3340 looks for **STP** to be asserted to re-start the clock and then resume normal synchronous operation.

Should the USB3340 be suspended in Low Power Mode, and the Link receives a hardware reset, the PHY must be able to recover from Low Power Mode and start its clock. If the Link asserts **STP** on reset, the PHY will exit Low Power Mode and start its clock.

If the Link does not assert **STP** on reset, the interface protection pull-up can be used. When the Link is reset, its **STP** output will tri-state and the pull-up resistor will pull **STP** high, signaling the PHY to restart its clock.

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6.5.5 Minimizing Current in Low Power Mode

In order to minimize the suspend current in Low Power Mode, the VBUS and ID comparators can be disabled to reduce suspend current. In Low Power Mode, the VbusVld and SessEnd comparators are not needed and can be disabled by clearing the associated bits in both the USB Interrupt Enable Rising and USB Interrupt Enable Falling registers. By disabling the interrupt in BOTH the rise and fall registers, the SessEnd and VbusVld comparators are turned off. The *IdFloatRise* and *IdFloatFall* bits in Carkit Interrupt Enable register should also be disabled if they were set. When exiting Low Power Mode, the Link should immediately re-enable the VbusVld and SessEnd comparators if host or OTG functionality is required.

In addition to disabling the OTG comparators in Low Power Mode, the Link may choose to disable the Interface Protect Circuit. By setting the *InterfaceProtectDisable* bit high in the Interface Control register, the Link can disable the pull-up resistor on **STP**. When **RESETB** is low the Interface Protect Circuit will be disabled.

6.6 Full Speed/Low Speed Serial Modes

The USB3340 includes two serial modes to support legacy Links which use either the 3pin or 6pin serial format. To enter either serial mode, the Link will need to write a 1 to the *6-pin FsLsSerialMode* or the *3-pin FsLsSerialMode* bits in the Interface control register. Serial Mode may be used to conserve power when attached to a device that is not capable of operating in Hi-Speed.

The serial modes are entered in the same manner as the entry into Low Power Mode. The Link writes the Interface Control register bit for the specific serial mode. The USB3340 will assert **DIR** and shut off the clock after at least five clock cycles. Then the data bus goes to the format of the serial mode selected. Before entering Serial Mode the Link must set the ULPI transceiver to the appropriate mode as defined in Table 5.1.

In ULPI Clock Output Mode, the PHY will shut off the 60MHz clock to conserve power. Should the Link need the 60MHz clock to continue during the serial mode of operation, the *ClockSuspendM* bit[3] of the Interface Control Register should be set before entering a serial mode. If set, the 60 MHz clock will be present during serial modes.

In serial mode, interrupts are possible from unmasked sources. The state of each interrupt source is sampled prior to the assertion of **DIR** and this is compared against the asynchronous level from interrupt source.

Exiting the serial modes is the same as exiting Low Power Mode. The Link must assert **STP** to signal the PHY to exit serial mode. When the PHY can accept a command, **DIR** is de-asserted and the PHY will wait until the Link de-asserts **STP** to resume synchronous ULPI operation. The **RESETB** pin can also be pulsed low to reset the USB3340 and return it to Synchronous Mode.

6.6.0.1 3-Pin FS/LS Serial Mode

Three pin serial mode utilizes the data bus pins for the serial functions shown in Table 6.8.

Table 6.8 Pin Definitions in 3 pin Serial Mode

SIGNAL	CONNECTED TO	DIRECTION	DESCRIPTION
tx_enable	**DATA[0]**	IN	Active High transmit enable.
data	**DATA[1]**	I/O	TX differential data on DP/DM when tx_enable is high. RX differential data from DP/DM when tx_enable is low.
SE0	**DATA[2]**	I/O	TX SE0 on DP/DM when tx_enable is high. RX SE0_b from DP/DM when tx_enable is low.

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Table 6.8 Pin Definitions in 3 pin Serial Mode (continued)

SIGNAL	CONNECTED TO	DIRECTION	DESCRIPTION
interrupt	**DATA[3]**	OUT	Asserted when any unmasked interrupt occurs. Active high.
Reserved	**DATA[7:4]**	OUT	Driven Low.

6.6.0.2 6-Pin FS/LS Serial Mode

Six pin serial mode utilizes the data bus pins for the serial functions shown in Table 6.9.

Table 6.9 Pin Definitions in 6 pin Serial Mode

SIGNAL	CONNECTED TO	DIRECTION	DESCRIPTION
tx_enable	**DATA[0]**	IN	Active High transmit enable.
tx_data	**DATA[1]**	IN	Tx differential data on DP/DM when tx_enable is high.
tx_se0	**DATA[2]**	IN	Tx SE0 on DP/DM when tx_enable is high.
interrupt	**DATA[3]**	OUT	Asserted when any unmasked interrupt occurs. Active high.
rx_dp	**DATA[4]**	OUT	Single ended receive data on DP.
rx_dm	**DATA[5]**	OUT	Single ended receive data on DM.
rx_rcv	**DATA[6]**	OUT	Differential receive data from DP and DM.
Reserved	**DATA[7]**	OUT	Driven Low.

6.7 Carkit Mode

The USB3340 includes Carkit Mode to support a USB UART and USB Audio Mode.

By entering Carkit Mode, the USB3340 current drain is minimized. The internal PLL is disabled and the 60MHz ULPI **CLKOUT** will be stopped to conserve power by default. The Link may configure the 60MHz clock to continue by setting the *ClockSuspendM* bit of the Interface Control register before entering Carkit Mode. If set, the 60 MHz clock will continue during the Carkit Mode of operation.

In Carkit Mode, interrupts are possible if they have been enabled in the Carkit Interrupt Enable register. The state of each interrupt source is sampled prior to the assertion of **DIR** and this is compared against the asynchronous level from interrupt source. In Carkit Mode, the Linestate signals are not available per the ULPI specification.

The ULPI interface is redefined to the following when Carkit Mode is entered.

Table 6.10 Pin Definitions in Carkit Mode

SIGNAL	CONNECTED TO	DIRECTION	DESCRIPTION
txd	**DATA[0]**	IN	UART TXD signal that is routed to the **DM** pin if the *TxdEn* is set in the Carkit Control register.
rxd	**DATA[1]**	OUT	UART RXD signal that is routed to the **DP** pin if the *RxdEn* bit is set in the Carkit Control register.

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Table 6.10 Pin Definitions in Carkit Mode (continued)

SIGNAL	CONNECTED TO	DIRECTION	DESCRIPTION
reserved	**DATA[2]**	OUT	Driven Low (*CarkitDataMC = 0, default)*
		IN	Tri-state *(CarkitDataMC = 1)*
int	**DATA[3]**	OUT	Asserted when any unmasked interrupt occurs. Active high.
reserved	**DATA[4:7]**	OUT	Driven Low.

Exiting Carkit Mode is the same as exiting Low Power Mode as described in Section 6.5.2. The Link must assert **STP** to signal the PHY to exit serial mode. When the PHY can accept a command, **DIR** is de-asserted and the PHY will wait until the Link de-asserts **STP** to resume synchronous ULPI operation. The **RESETB** pin can also be pulsed low to reset the USB3340 and return it to Synchronous Mode.

6.7.1 Entering USB UART Mode

The USB3340 can be placed into UART Mode by first setting the *TxdEn* and *RxdEn* bits in the Carkit Control register. Then the Link can set the *CarkitMode* bit in the Interface Control register. The *TxdEn* and *RxdEn* bits must be written before the *CarkitMode* bit.

Table 6.11 ULPI Register Programming Example to Enter UART Mode

R/W	ADDRESS (HEX)	VALUE (HEX)	DESCRIPTION	RESULT
W	04	49	Configure Non-Driving mode Select FS transmit edge rates	*OpMode*=01 *XcvrSelect*=01
W	39	00	Set regulator to 3.3V	*UART RegOutput*=00
W	19	0C	Enable UART connections	*RxdEn*=1 *TxdEn*=1
W	07	04	Enable carkit mode	*CarkitMode*=1

After the *CarkitMode* bit is set, the ULPI interface will become redefined as described in Table 6.10, and the USB3340 will transmit data through the **DATA[0]** to **DM** of the USB connector and receive data on **DP** and pass the information the Link on **DATA[1]**.

When entering UART mode, the regulator output will automatically switch to the value configured by the *UART RegOutput bits in the* USB IO & Power Management register and the R_{CD} pull-up resistors will be applied internally to **DP** and **DM**. This will hold the UART in its default operating state.

While in UART mode, the transmit edge rates can be set to either the Full Speed USB or Low Speed USB edge rates by using the *XcvrSelect[1:0]* bits in the Function Control register.

6.7.2 USB Audio Mode

When the USB3340 is powered in Synchronous Mode, the Audio switches can be enabled by asserting the *SpkLeftEn*, or *SpkRightEn* bits in the Carkit Control register. After the register write is complete, the USB3340 will immediately enable or disable the audio switch. Then the Link can set the *CarkitMode* bit in the Interface Control register. The *SpkLeftEn*, or *SpkRightEn* bits must be written before the *CarkitMode* bit.

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Table 6.12 ULPI Register Programming Example to Enter Audio Mode

R/W	ADDRESS (HEX)	VALUE (HEX)	DESCRIPTION	RESULT
W	04	48	Configure Non-Driving mode	*OpMode*=01
W	19	30	Enable Audio connections	*SpkrRightEn*=1, *SpkrLeftEn*=1
W	07	04	Enable carkit mode	*CarkitMode*=1

After the *CarkitMode* bit is set, the ULPI interface will become redefined as described in Table 6.10.

6.8 RID Converter Operation

The RID converter is designed to read the value of the ID resistance to ground and report back its value through the ULPI interface.

When a resistor to ground is applied to the **ID** pin the state of the IdGnd comparator will change from a 1 to a 0 as described in Section 5.7.1. If the USB3340 is in ULPI mode, an RXCMD will be generated with bit 6 low. If the USB3340 is in Low Power Mode (or one of the other non-ULPI modes), the DATA[3] interrupt signal will go high.

After the USB3340 has detected the change of state on the **ID** pin, the RID converter can be used to determine the value of ID resistance. To start a ID resistance measurement, the *RidConversionStart* bit is set in the Vendor Rid Conversion register.

The Link can use one of two methods to determine when the RID Conversion is complete. One method is polling the *RidConversionStart* bit as described in Section 7.1.3.4. The preferred method is to set the *RidIntEn* bit in the Vendor Rid Conversion register. When *RidIntEn* is set, an RXCMD will be generated after the RID conversion is complete. As described in Table 6.3, the alt_int bit of the RXCMD will be set.

After the RID Conversion is complete, the Link can read *RidValue* from the Vendor Rid Conversion register.

6.8.1 Headset Audio Mode

This mode is designed to allow a user to view the status of several signals while using an analog Audio headset with a USB connector. This mode is provided as an alternate mode to the CarKit Mode defined in Chapter 6.7. In the CarKit mode the Link is unable to view the source of the interrupt on **ID**. For the Link to view the interrupt on **ID** the PHY must be returned to synchronous mode so the interrupt can be read. This will force the audio switches to be deactivated during the PHY start-up which may glitch the audio signals. In addition the Link can not change the resistance on the **ID** pin without starting up the PHY to access the ULPI registers.

The Headset Audio Mode is entered by writing to the Headset Audio Mode register, and allows the Link access to the state of the **VBUS** and **ID** pins during audio without having to break the audio connection. The Headset Audio mode also allows for the Link to change the resistance on the **ID** pin to change the audio device attached from mono to stereo.

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Table 6.13 Pin Definitions in Headset Audio Mode

SIGNAL	CONNECTED TO	DIRECTION	DESCRIPTION
SessVld	**DATA[0]**	OUT	Output of SessVld comparator
VbusVld	**DATA[1]**	OUT	Output of VbusVld Comparator (interrupt must be enabled)
IdGndDrv	**DATA[2]**	IN	Drives **ID** pin to ground when asserted 0b: Not connected 1b: Connects **ID** to ground.
	DATA[3]	OUT	Driven low
IdGround	**DATA[4]**	OUT	Asserted when the **ID** pin is grounded. 0b: **ID** pin is grounded 1b: **ID** pin is floating
IdFloat	**DATA[5]**	OUT	Asserted when the **ID** pin is floating. *IdPullup* or *Id_pullup330* must be enabled. *IdFloatRise* and *IdFloatFall* must be enabled.
IdPullup330	**DATA[6]**	IN	When enabled a 330kΩ pullup is applied to the **ID** pin. This bit will also change the trip point of the IdGnd comparator to the value shown in Table 4.8. 0b: Disables the pull-up resistor 1b: Enables the pull-up resistor
IdPullup	**DATA[7]**	IN	Connects the 100kΩ pull-up resistor from the **ID** pin to **VDD3.3** 0b: Disables the pull-up resistor 1b: Enables the pull-up resistor

Exiting Headset Audio Mode is the same as exiting Low Power Mode as described in Section 6.5.2. The **RESETB** pin can also be pulsed low to reset the USB3340 and return to Synchronous Mode.

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Chapter 7 ULPI Register Map

7.1 ULPI Register Array

The USB3340 PHY implements all of the ULPI registers detailed in the ULPI revision 1.1 specification. The complete USB3340 ULPI register set is shown in Table 7.1. All registers are 8 bits. This table also includes the default state of each register upon POR or de-assertion of **RESETB**, as described in Section 5.6.2. The RESET bit in the Function Control Register does not reset the bits of the ULPI register array. The Link should not read or write to any registers not listed in this table.

The USB3340 supports extended register access. The immediate register set (00-3Fh) can be accessed through either a immediate address or an extended register address.

Table 7.1 ULPI Register Map

REGISTER NAME	DEFAULT STATE	ADDRESS (6BIT)			
		READ	WRITE	SET	CLEAR
Vendor ID Low	24h	00h	-	-	-
Vendor ID High	04h	01h	-	-	-
Product ID Low	09h	02h	-	-	-
Product ID High	00h	03h	-	-	-
Function Control	41h	04-06h	04h	05h	06h
Interface Control	00h	07-09h	07h	08h	09h
OTG Control	06h	0A-0Ch	0Ah	0Bh	0Ch
USB Interrupt Enable Rising	1Fh	0D-0Fh	0Dh	0Eh	0Fh
USB Interrupt Enable Falling	1Fh	10-12h	10h	11h	12h
USB Interrupt Status (Note 7.1)	00h	13h	-	-	-
USB Interrupt Latch	00h	14h	-	-	-
Debug	00h	15h	-	-	-
Scratch Register	00h	16-18h	16h	17h	18h
Carkit Control	00h	19-1Bh	19h	1Ah	1Bh
Reserved	00h	1Ch			
Carkit Interrupt Enable	00h	1D-1Fh	1Dh	1Eh	1Fh
Carkit Interrupt Status	00h	20h	-	-	-
Carkit Interrupt Latch	00h	21h	-	-	-
Reserved	00h	22-30h			
HS Compensation Register	00h	31h	31h	-	-
USB-IF Charger Detection	00h	32h	32h	-	-
Headset Audio Mode	00	33	33	-	-

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Table 7.1 ULPI Register Map (continued)

REGISTER NAME	DEFAULT STATE	ADDRESS (6BIT)			
		READ	WRITE	SET	CLEAR
Reserved	00h	34-35h			
Vendor Rid Conversion	00h	36-38h	36h	37h	38h
USB IO & Power Management	04h	39-3Bh	39h	3Ah	3Bh
Reserved	00h	3C-3Fh			

Note 7.1 Dynamically updates to reflect current status of interrupt sources.

7.1.1 ULPI Register Set

The following registers are used for the ULPI interface.

7.1.1.1 Vendor ID Low

Address = 00h (read only)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
Vendor ID Low	7:0	rd	24h	Microchip Vendor ID

7.1.1.2 Vendor ID High

Address = 01h (read only)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
Vendor ID High	7:0	rd	04h	Microchip Vendor ID

7.1.1.3 Product ID Low

Address = 02h (read only)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
Product ID Low	7:0	rd	09h	Microchip Product ID

7.1.1.4 Product ID High

Address = 03h (read only)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
Product ID High	7:0	rd	00h	Microchip Product ID

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7.1.1.5 Function Control

Address = 04-06h (read), 04h (write), 05h (set), 06h (clear)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
XcvrSelect[1:0]	1:0	rd/w/s/c	01b	Selects the required transceiver speed. 00b: Enables HS transceiver 01b: Enables FS transceiver 10b: Enables LS transceiver 11b: Enables FS transceiver for LS packets (FS preamble automatically pre-pended)
TermSelect	2	rd/w/s/c	0b	Controls the DP and DM termination depending on *XcvrSelect*, *OpMode*, *DpPulldown*, and *DmPulldown*. The DP and DM termination is detailed in Table 5.1.
OpMode	4:3	rd/w/s/c	00b	Selects the required bit encoding style during transmit. 00b: Normal Operation 01b: Non-Driving 10b: Disable bit-stuff and NRZI encoding 11b: Reserved
Reset	5	rd/w/s/c	0b	Active high transceiver reset. This reset does not reset the ULPI interface or register set. Automatically clears after reset is complete.
SuspendM	6	rd/w/s/c	1b	Active low PHY suspend. When cleared the PHY will enter Low Power Mode as detailed in 6.5. Automatically set when exiting Low Power Mode.
LPM Enable	7	rd/w/s/c	0b	When enabled the PLL start-up time is shortened to allow fast start-up for LPM. The reduced PLL start-up time is achieved by bypassing the VCO process compensation which was done on initial start-up.

7.1.1.6 Interface Control

Address = 07-09h (read), 07h (write), 08h (set), 09h (clear)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
6-pin FsLsSerialMode	0	rd/w/s/c	0b	When asserted the ULPI interface is redefined to the 6-pin Serial Mode. The PHY will automatically clear this bit when exiting serial mode.
3-pin FsLsSerialMode	1	rd/w/s/c	0b	When asserted the ULPI interface is redefined to the 3-pin Serial Mode. The PHY will automatically clear this bit when exiting serial mode.
CarkitMode	2	rd/w/s/c	0b	When asserted the ULPI interface is redefined to the Carkit interface. The PHY will automatically clear this bit when exiting Carkit Mode.

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FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
ClockSuspendM	3	rd/w/s/c	0b	Enables Link to turn on 60MHz CLKOUT in Serial Mode or Carkit Mode. 0b: Disable clock in serial or Carkit Mode. 1b: Enable clock in serial or Carkit Mode.
AutoResume	4	rd/w/s/c	0b	Only applicable in Host mode. Enables the PHY to automatically transmit resume signaling. This function is detailed in Section 6.4.1.4.
IndicatorComplement	5	rd/w/s/c	0b	Inverts the EXTVBUS signal. This function is detailed in Section 5.7.2. **Note:** The EXTVBUS signal is always high on the USB3340.
IndicatorPassThru	6	rd/w/s/c	0b	Disables and'ing the internal VBUS comparator with the EXTVBUS signal when asserted. This function is detailed in Section 5.7.2. **Note:** The EXTVBUS signal is always high on the USB3340.
InterfaceProtectDisable	7	rd/w/s/c	0b	Used to disable the integrated **STP** pull-up resistor used for interface protection. This function is detailed in Section 6.5.4.

7.1.1.7 OTG Control

Address = 0A-0Ch (read), 0Ah (write), 0Bh (set), 0Ch (clear)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
IdPullup	0	rd/w/s/c	0b	Connects a 100kΩ pull-up resistor from the **ID** pin to **VDD33** 0b: Disables the pull-up resistor 1b: Enables the pull-up resistor
DpPulldown	1	rd/w/s/c	1b	Enables the 15k Ohm pull-down resistor on **DP**. 0b: Pull-down resistor not connected 1b: Pull-down resistor connected
DmPulldown	2	rd/w/s/c	1b	Enables the 15k Ohm pull-down resistor on **DM**. 0b: Pull-down resistor not connected 1b: Pull-down resistor connected
DischrgVbus	3	rd/w/s/c	0b	This bit is only used during SRP. Connects a resistor from VBUS to ground to discharge **VBUS**. 0b: disconnect resistor from **VBUS** to ground 1b: connect resistor from **VBUS** to ground
ChrgVbus	4	rd/w/s/c	0b	This bit is only used during SRP. Connects a resistor from **VBUS** to **VDD33** to charge **VBUS** above the SessValid threshold. 0b: disconnect resistor from **VBUS** to **VDD33** 1b: connect resistor from **VBUS** to **VDD33**
DrvVbus	5	rd/w/s/c	0b	Enables external 5 volt supply to drive 5 volts on VBUS. This signal is or'ed with *DrvVbusExternal*. 0b: Do not drive Vbus, **CPEN** driven low. 1b: Drive Vbus, **CPEN** driven high.

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FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
DrvVbusExternal	6	rd/w/s/c	0b	Enables external 5 volt supply to drive 5 volts on VBUS. This signal is or'ed with *DrvVbus*. 0b: Do not drive Vbus, **CPEN** driven low. 1b: Drive Vbus, **CPEN** driven high.
UseExternalVbus Indicator	7	rd/w/s/c	0b	Tells the PHY to use an external VBUS over-current or voltage indicator. This function is detailed in Section 5.7.2. 0b: Use the internal VbusValid comparator 1b: Use the EXTVBUS input as for VbusValid signal. **Note:** The EXTVBUS signal is always high on the USB3340.

7.1.1.8 USB Interrupt Enable Rising

Address = 0D-0Fh (read), 0Dh (write), 0Eh (set), 0Fh (clear)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
HostDisconnect Rise	0	rd/w/s/c	1b	Generate an interrupt event notification when Hostdisconnect changes from low to high. Applicable only in host mode.
VbusValid Rise	1	rd/w/s/c	1b	Generate an interrupt event notification when Vbusvalid changes from low to high.
SessValid Rise	2	rd/w/s/c	1b	Generate an interrupt event notification when SessValid changes from low to high.
SessEnd Rise	3	rd/w/s/c	1b	Generate an interrupt event notification when SessEnd changes from low to high.
IdGnd Rise	4	rd/w/s/c	1b	Generate an interrupt event notification when IdGnd changes from low to high.
Reserved	7:5	rd	0h	Read only, 0.

7.1.1.9 USB Interrupt Enable Falling

Address = 10-12h (read), 10h (write), 11h (set), 12h (clear)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
HostDisconnect Fall	0	rd/w/s/c	1b	Generate an interrupt event notification when Hostdisconnect changes from high to low. Applicable only in host mode.
VbusValid Fall	1	rd/w/s/c	1b	Generate an interrupt event notification when Vbusvalid changes from high to low.
SessValid Fall	2	rd/w/s/c	1b	Generate an interrupt event notification when SessValid changes from high to low.
SessEnd Fall	3	rd/w/s/c	1b	Generate an interrupt event notification when SessEnd changes from high to low.

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FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
IdGnd Fall	4	rd/w/s/c	1b	Generate an interrupt event notification when IdGnd changes from high to low.
Reserved	7:5	rd	0h	Read only, 0.

7.1.1.10 USB Interrupt Status

Address = 13h (read only)

This register dynamically updates to reflect current status of interrupt sources.

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
HostDisconnect	0	rd (read only)	0b	Current value of the UTMI+ HS Hostdisconnect output. Applicable only in host mode.
VbusValid	1		0b	Current value of the UTMI+ Vbusvalid output. If *VbusValid Rise* and *VbusValid Fall* are set this register will read 0.
SessValid	2		0b	Current value of the UTMI+ SessValid output. This register will always read the current status of the Session Valid comparator regardless of the *SessValid Rise* and *SessValid Fall* settings.
SessEnd	3		0b	Current value of the UTMI+ SessEnd output. If *SessEnd Rise* and *SessEnd Fall* are set this register will read 0.
IdGnd	4		0b	Current value of the UTMI+ IdGnd output.
Reserved	7:5		0h	Read only, 0.

Note: The default value is only valid after POR. When the register is read it will match the current status of the comparators at the moment the register is read.

7.1.1.11 USB Interrupt Latch

Address = 14h (read only with auto clear)

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FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
HostDisconnect Latch	0	rd (Note 7.2)	0b	Set to 1b by the PHY when an unmasked event occurs on Hostdisconnect. Cleared when this register is read. Applicable only in host mode.
VbusValid Latch	1		0b	Set to 1b by the PHY when an unmasked event occurs on VbusValid. Cleared when this register is read.
SessValid Latch	2		0b	Set to 1b by the PHY when an unmasked event occurs on SessValid. Cleared when this register is read.
SessEnd Latch	3		0b	Set to 1b by the PHY when an unmasked event occurs on SessEnd. Cleared when this register is read.
IdGnd Latch	4		0b	Set to 1b by the PHY when an unmasked event occurs on IdGnd. Cleared when this register is read.
Reserved	7:5	rd	0h	Read only, 0.

Note 7.2 rd: Read Only with auto clear.

7.1.1.12 Debug

Address = 15h (read only)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
Linestate[1:0]	1:0	rd	00b	Contains the current value of Linestate[1:0].
Reserved	7:2	rd	000000b	Read only, 0.

7.1.1.13 Scratch Register

Address = 16-18h (read), 16h (write), 17h (set), 18h (clear)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
Scratch	7:0	rd/w/s/c	00h	Empty register byte for testing purposes. Software can read, write, set, and clear this register and the PHY functionality will not be affected.

7.1.2 Carkit Control Registers

The following registers are used to set-up and enable the USB UART and USB Audio functions.

7.1.2.1 Carkit Control

Address = 19-1Bh (read), 19h (write), 1Ah (set), 1Bh (clear)

This register is used to program the USB3340 into and out of the Carkit Mode. When entering the UART mode the Link must first set the desired *TxdEn* and the *RxdEn* bits and then transition to Carkit

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Mode by setting the *CarkitMode* bit in the Interface Control Register. When *RxdEn* is not set then the **DATA[1]** pin is held to a logic high.

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
CarkitPwr	0	rd	0b	Read only, 0.
IdGndDrv	1	rd/w/s/c	0b	Drives **ID** pin to ground
TxdEn	2	rd/w/s/c	0b	Connects UART TXD (**DATA[0]**) to **DM**
RxdEn	3	rd/w/s/c	0b	Connects UART RXD (**DATA[1]**) to **DP**
SpkLeftEn	4	rd/w/s/c	0b	Connects **DM** pin to **SPK_L** pin
SpkRightEn	5	rd/w/s/c	0b	Connects **DP** pin to **SPK_R** pin. See Note below.
MicEn	6	rd/w/s/c	0b	Connects **DP** pin to **SPK_R** pin. See Note below.
CarkitDataMC	7	rd/w/s/c	0b	When set the UPLI DATA[2] pin is changed from a driven 0 to tri-state, when carkit mode is entered.

Note: If *SpkRightEn* or *MicEn* are asserted the **DP** pin will be connected to **SPK_R**. To disconnect the **DP** pin from the **SPK_R** pin both *SpkrRightEn* and *MicEn* must be set to de-asserted.

If using USB UART mode, the UART data will appear at the **SPK_L** and **SPK_R** pins if the corresponding *SpkLeftEn*, *SpkRightEn*, or *MicEn* switches are enabled.

If using USB Audio the *TxdEn* and *RxdEn* bits should not be set when the *SpkLeftEn*, *SpkRightEn*, or *MicEn* switches are enabled. The USB single-ended receivers described in Section 5.2.1 are disabled when either *SpkLeftEn*, *SpkRightEn*, or *MicEn* are set.

7.1.2.2 Carkit Interrupt Enable

Address = 1D-1Fh (read), 1Dh (write), 1Eh (set), 1Fh (clear)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
IdFloatRise	0	rd/w/s/c	0b	When enabled an interrupt will be generated on the alt_int of the RXCMD byte when the **ID** pin transitions from non-floating to floating. The *IdPullup* bit in the OTG Control register should be set.
IdFloatFall	1	rd/w/s/c	0b	When enabled an interrupt will be generated on the alt_int of the RXCMD byte when the **ID** pin transitions from floating to non-floating. The *IdPullup* bit in the OTG Control register should be set.
VdatDetIntEn	2	rd/w/s/c	0b	When enabled an interrupt will be generated on the alt_int of the RXCMD byte when the V_{DAT_DET} Comparator changes state.
CarDpRise	3	rd	0b	Not Implemented. Reads as 0b.
CarDpFall	4	rd	0b	Not Implemented. Reads as 0b.

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FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
RidIntEn	5	rd/w/s/c	0b	When enabled an interrupt will be generated on the alt_int of the RXCMD byte when *RidConversionDone* bit is asserted. **Note:** This register bit is or'ed with the *RidIntEn* bit of the Vendor Rid Conversion register described in Section 7.1.3.4.
Reserved	6	rd/w/s/c	0b	Read only, 0.
Reserved	7	rd	0b	Read only, 0.

7.1.2.3 Carkit Interrupt Status

Address = 20h (read only)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
IdFloat	0	rd	0b	Asserted when the **ID** pin is floating. *IdPullup* must be enabled.
VdatDet	1	rd	0b	V_{DAT_DET} Comparator output 0b: No voltage is detected on **DP** 1b: Voltage detected on **DP**, *IdatSinkEn* must be set to 1. **Note:** *VdatDet* can also be read from the USB-IF Charger Detection register described in Section 7.1.3.3.
CarDp	2	rd	0b	Not Implemented. Reads as 0b.
RidValue	5:3	rd	000b	Conversion value of Rid resistor 000: 0 ohms 001: 75 ohms 010: 102K ohms 011: 200K ohms 100: Reserved 101: ID floating 111: Error **Note:** *RidValue* can also be read from the Vendor Rid Conversion register described in Section 7.1.3.4.
RidConversionDone	6	rd	0b	Automatically asserted by the USB3340 when the Rid Conversion is finished. The conversion will take 282uS. This bit will auto clear when the *RidValue* is read from the Rid Conversion Register. Reading the *RidValue* from the Carkit Interrupt Status register will not clear either *RidConversionDone* status bit. **Note:** *RidConversionDone* can also be read from the Vendor Rid Conversion register described in Section 7.1.3.4.
Reserved	7	rd	0b	Read only, 0.

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7.1.2.4 Carkit Interrupt Latch

Address = 21h (read only with auto-clear)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
IdFloat Latch	0	rd (Note 7.3)	0b	Asserted if the state of the **ID** pin changes from non-floating to floating while the *IdFloatRise* bit is enabled or if the state of the **ID** pin changes from floating to non-floating while the *IdFloatFall* bit is enabled.
VdatDet Latch	1	rd	0b	If *VdatDetIntEn* is set and the *VdatDet* bit changes state, this bit will be asserted.
CarDp Latch	2	rd	0b	Not Implemented. Reads as 0b.
RidConversionLatch	3	rd (Note 7.3)	0b	If *RidIntEn* is set and the state of the *RidConversionDone* bit changes from a 0 to 1 this bit will be asserted.
Reserved	7:4	rd	0000b	Read only, 0.

Note 7.3 rd: Read Only with auto clear

7.1.3 Vendor Register Access

The vendor specific registers include the range from 30h to 3Fh. These can be accessed by the ULPI immediate register read / write.

7.1.3.1 HS Compensation Register

Address = 31h (read / write)

The USB3340 is designed to meet the USB specifications and requirements when the DP and DM signals are properly designed on the PCB. The DP and DM trace impedance should be 45ohm single ended and 90ohm differential. In cases where the DP and DM traces are not able to meet these requirements the HS Compensation register can be used to compensate for the losses in signal amplitude.

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
VariSense	1:0	rd/w	00b	Used to lower the threshold of the squelch detector. 00: 100% (default) 01: 83% 10: 66.7% 11: 50%
Reserved	2	rd	0b	Read only, 0.
Reserved	3	rd	0b	Read only, 0.

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FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
PHYBoost	6:4	rd/w	000b	Used to change the output voltage of the Hi-Speed transmitter 000: Nominal 001: +3.7% 010: +7.4% 011: +11.0% 100: +14.7% 101: +18.3% 110: +22.0% 111: +25.7%
Reserved	7	rd	0b	Read only, 0.

7.1.3.2 USB-IF Charger Detection

Address = 32h (read / write)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
VDatSrcEn	0	rd/w	0	V_{DAT_SRC} voltage enable 0b: Disabled 1b: Enabled
IDatSinkEn	1	rd/w	0	I_{DAT_SINK} current sink and V_{DAT_DET} comparator enable 0b: Disabled, V_{DAT_DET} = 0. 1b: Enabled
ContactDetectEn	2	rd/w	0	I_{DP_SRC} Enable 0b: Disabled 1b: Enabled
HostChrgEn	3	rd/w	0	Enable Charging Host Port Mode. 0b: Portable Device 1b: Charging Host Port. When the charging host port bit is set the connections of V_{DAT_SRC}, I_{DAT_SINK}, I_{DP_SRC}, and V_{DAT_DET} are reversed between **DP** and **DM**.
VdatDet	4	rd	0	V_{DAT_DET} Comparator output. *IdatSinkEn* must be set to 1 to enable the comparator. 0b: No voltage is detected on **DP** or *Linestate[1:0]* is not equal to 00b. 1b: Voltage detected on **DP**, and *Linestate[1:0]* = 00b. **Note:** *VdatDet* can also be read from the Carkit Interrupt Status register described in Section 7.1.2.3.
Reserved	5-7	rd		Read only, 0.

Note: The charger detection should be turned off before beginning USB operation. USB-IF Charger Detection Bits 2:0 should be set to 000b.

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7.1.3.3 Headset Audio Mode

Address = 33h (read / write)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
HeadsetAudioEn	3:0	rd/w	0000b	When this field is set to a value of '1010', the Headset Audio Mode is enabled as described in Section 6.8.1.
Reserved	7:4	rd	0h	Read only, 0.

7.1.3.4 Vendor Rid Conversion

Address = 36-38h (read), 36h (write), 37h (set), 38h (clear)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
RidValue	2:0	rd/w	000b	Conversion value of Rid resistor 000: 0 ohms 001: 75 ohms 010: 100K ohms 011: 200K ohms 100: 440K ohms 101: ID floating 111: Error **Note:** *RidValue* can also be read from the Carkit Interrupt Status Register.
RidConversionDone	3	rd (Note 7.4)	0b	Automatically asserted by the USB3340 when the Rid Conversion is finished. The conversion will take 282uS. This bit will auto clear when the *RidValue* is read from the Rid Conversion Register. Reading the *RidValue* from the Carkit Interrupt Status Register will not clear either *RidConversionDone* status bit. **Note:** *RidConversionDone* can also be read from the Carkit Interrupt Status Register.
RidConversionStart	4	rd/w/s/c	0b	When this bit is asserted either through a register write or set, the Rid converter will read the value of the ID resistor. When the conversion is complete this bit will auto clear.
Reserved	5	rd/w/s/c	0b	This bit must remain at 0.
RidIntEn	6	rd/w/s/c	0b	When enabled an interrupt will be generated on the alt_int of the RXCMD byte when *RidConversionDone* bit is asserted. **Note:** This register bit is or'ed with the *RidIntEn* bit of the Carkit Interrupt Status register.
Reserved	7	rd	0b	Read only, 0.

Note 7.4 rd: Read Only with auto clear.

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7.1.3.5 USB IO & Power Management

Address = 39-3Bh (read), 39h (write), 3Ah (set), 3Bh (clear)

FIELD NAME	BIT	ACCESS	DEFAULT	DESCRIPTION
Reserved	0	rd/w/s/c	0b	Read only, 0.
SwapDP/DM	1	rd/w/s/c	0b	When asserted, the **DP** and **DM** pins of the USB transceiver are swapped. This bit can be used to prevent crossing the DP/DM traces on the board. In UART mode, it swaps the routing to the **DP** and **DM** pins. In USB Audio Mode, it does not affect the **SPK_L** and **SPK_R** pins.
UART RegOutput	3:2	rd/w/s/c	01b	Controls the output voltage of the **VBAT** to **VDD33** regulator in UART mode. When the PHY is switched from USB mode to UART mode regulator output will automatically change to the value specified in this register when *TxdEn* is asserted. 00: 3.3V 01: 3.0V (default) 10: 2.75V 11: 2.5V **Note:** When in USB Audio Mode the regulator will remain at 3.3V. When using this register it is recommended that the Link exit UART mode by using the **RESETB** pin.
ChargerPullupEnDP	4	rd/w/s/c	0b	Enables the R_{CD} Pull-up resistor on the **DP** pin. (The pull-up is automatically enabled in UART mode)
ChargerPullupEnDM	5	rd/w/s/c	0b	Enables the R_{CD} Pull-up resistor on the **DM** pin. (The pull-up is automatically enabled in UART mode)
USB RegOutput	7:6	rd/w/s/c	00b	Controls the output voltage of the **VBAT** to **VDD33** regulator in USB mode. When the PHY is in Synchronous Mode, Serial Mode, or Low Power Mode, the regulator output will be the value specified in this register. 00: 3.3V (default) 01: 3.0V 10: 2.75V 11: 2.5V

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Chapter 8 Application Notes

8.1 Application Diagram

The USB3340 requires few external components as shown in the application diagrams. The USB 2.0 Specification restricts the voltage at the VBUS pin to a maximum value of 5.25V. In some applications, the voltage will exceed this limit, so the USB3340 provides an integrated over voltage protection circuit. The over voltage protection circuit works with an external resistor (R_{VBUS}) to lower the voltage at the **VBUS** pin.

Table 8.1 Component Values in Application Diagrams

REFERENCE DESIGNATOR	VALUE	DESCRIPTION	NOTES
C_{OUT}	See Table 4.11	Bypass capacitor to ground (<1Ω ESR) for regulator stability.	Place as close as possible to the PHY.
C_{VBUS}	See Table 8.2	Capacitor to ground required by the USB Specification. Microchip recommends <1Ω ESR.	Place near the USB connector.
C_{BYP}	System dependent.	Bypass capacitor to ground. Typical values used are 0.1 or 0.01 µF.	Place as close as possible to the PHY.
C_{DC_LOAD}	System dependent.	The USB connector housing may be AC-coupled to the device ground.	Industry convention is to ground only the host side of the cable shield.
R_{VBUS}	1kΩ or 20kΩ	Series resistor to work with internal over voltage protection.	See Section 5.7.2.6 for information regarding power dissipation.
R_{BIAS}	8.06kΩ (±1%)	Series resistor to establish reference voltage.	See Section 5.3 for information regarding power dissipation.

Table 8.2 Capacitance Values at VBUS of USB Connector

MODE	MIN VALUE	MAX VALUE
Host	120µF	
Device	1µF	10µF
OTG	1µF	6.5µF

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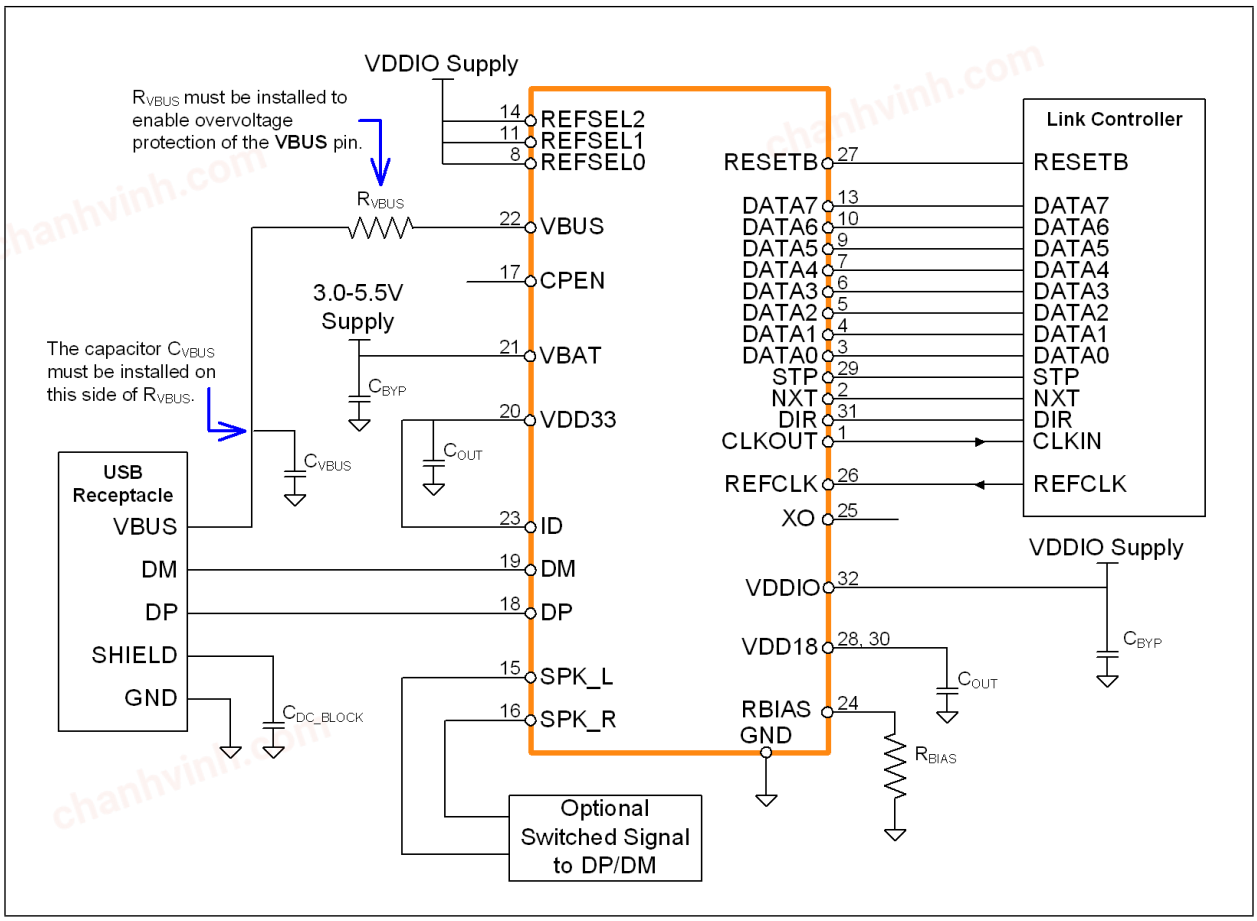


Figure 8.1 USB3340 Application Diagram (Device configured for ULPI Clock Output Mode, 24MHz)

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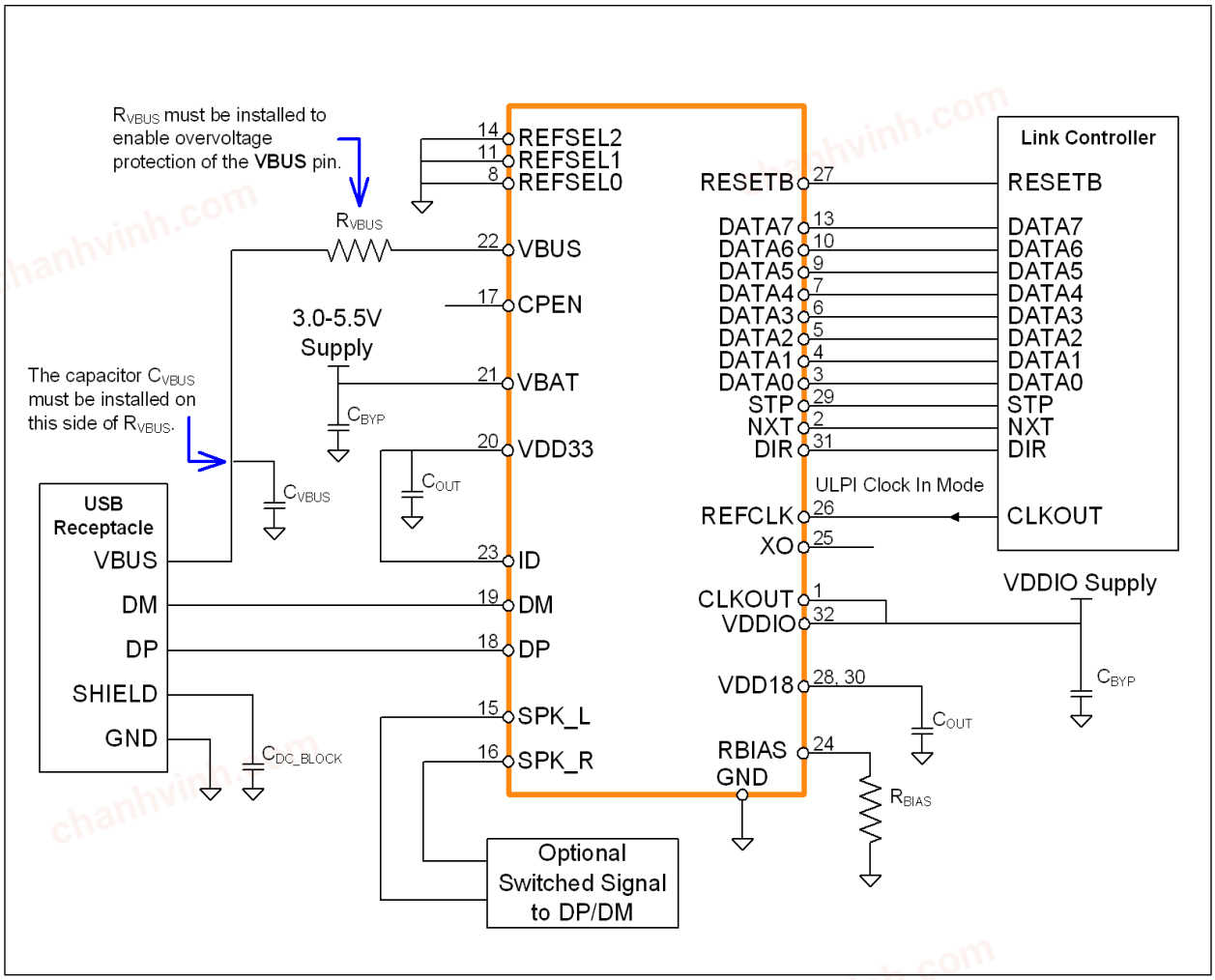


Figure 8.2 USB3340 Application Diagram (Device configured for ULPI Clock Input Mode, 60MHz)

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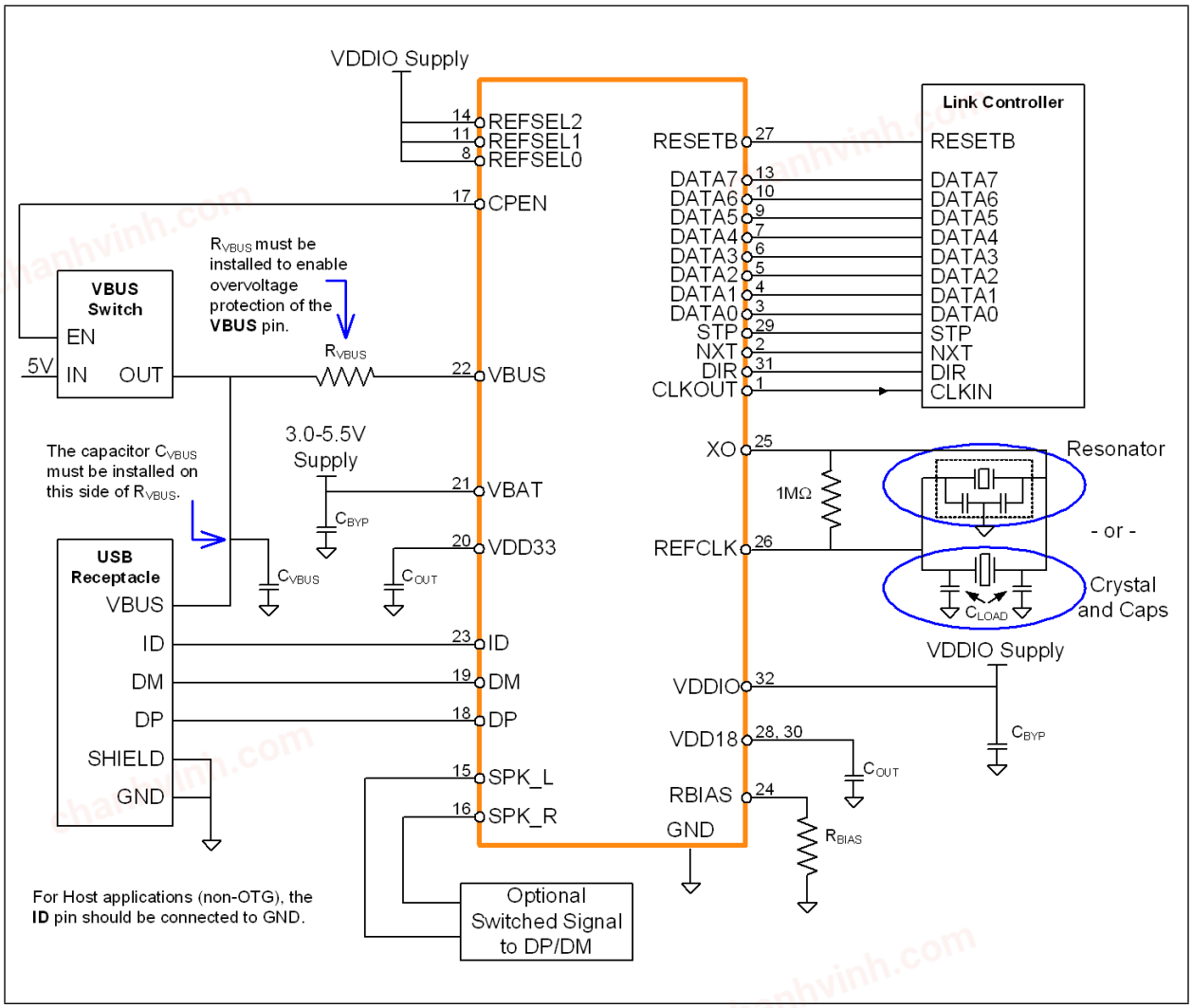


Figure 8.3 USB3340 Application Diagram (Host or OTG configured for ULPI Clock Output Mode, 24MHz)

8.2 USB Charger Detection

The USB3340 provides the hardware described in the USB Battery Charging Specification. Microchip provides an Application Note which describes how to use the USB3340 in a battery charging application.

8.3 Reference Designs

Microchip has generated reference designs for connecting the USB3340 to SoCs with a ULPI port. Please contact the Microchip sales office for more details.

8.4 ESD Performance

The USB3340 is protected from ESD strikes. By eliminating the requirement for external ESD protection devices, board space is conserved, and the board manufacturer is enabled to reduce cost. The advanced ESD structures integrated into the USB3340 protect the device whether or not it is powered up.

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8.4.1 Human Body Model (HBM) Performance

HBM testing verifies the ability to withstand the ESD strikes like those that occur during handling and manufacturing, and is done without power applied to the IC. To pass the test, the device must have no change in operation or performance due to the event. The USB3340 HBM performance is detailed in Table 4.13.

8.4.2 EN/IEC 61000-4-2 Performance

The EN/IEC 61000-4-2 ESD specification is an international standard that addresses system-level immunity to ESD strikes while the end equipment is operational. In contrast, the HBM ESD tests are performed at the device level with the device powered down.

Microchip contracts with Independent laboratories to test the USB3340 to EN/IEC 61000-4-2 in a working system. Reports are available upon request. Please contact your Microchip representative, and request information on 3rd party ESD test results. The reports show that systems designed with the USB3340 can safely provide the ESD performance shown in Table 4.13 without additional board level protection.

In addition to defining the ESD tests, EN/IEC 61000-4-2 also categorizes the impact to equipment operation when the strike occurs (ESD Result Classification). The USB3340 maintains an ESD Result Classification 1 or 2 when subjected to an EN/IEC 61000-4-2 (level 4) ESD strike.

Both air discharge and contact discharge test techniques for applying stress conditions are defined by the EN/IEC 61000-4-2 ESD document.

8.4.2.1 Air Discharge

To perform this test, a charged electrode is moved close to the system being tested until a spark is generated. This test is difficult to reproduce because the discharge is influenced by such factors as humidity, the speed of approach of the electrode, and construction of the test equipment.

8.4.2.2 Contact Discharge

The uncharged electrode first contacts the USB connector to prepare this test, and then the probe tip is energized. This yields more repeatable results, and is the preferred test method. The independent test laboratories contracted by Microchip provide test results for both types of discharge methods.

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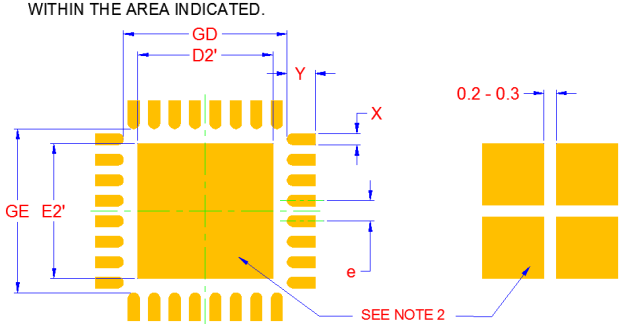
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Chapter 9 Package Outline

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging.

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.70	0.85	1.00	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
A2	-	0.65	0.90	-	MOLD CAP THICKNESS
D/E	4.90	5.00	5.10	-	X/Y BODY SIZE
D1/E1	4.55	4.75	4.95	-	X/Y MOLD CAP SIZE
D2/E2	3.20	3.30	3.40	-	X/Y EXPOSED PAD SIZE
L	0.30	0.40	0.50	-	TERMINAL LENGTH
b	0.18	0.25	0.30	2	TERMINAL WIDTH
k	0.35	0.45	-	-	TERMINAL TO ePAD CLEARANCE
e	0.50 BSC			-	TERMINAL PITCH

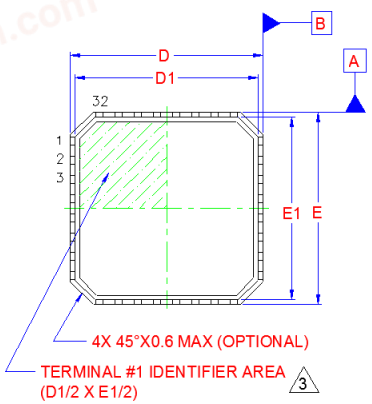
NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.



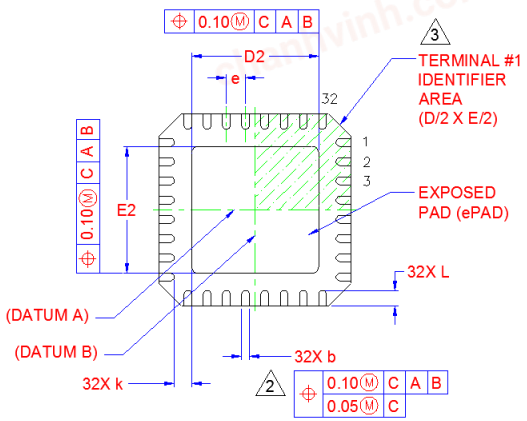
LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	4.00	-	4.10
D2'/E2'	3.10	-	3.30
X	-	0.24	0.28
Y	-	0.69	0.75
e		0.50	

NOTES:
1. THE USER MAY MODIFY THE PCB LAND PATTERN DESIGN AND DIMENSIONS BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY
2. EXPOSED SOLDERABLE COPPER AREA OF THE CENTER PAD CAN BE EITHER SOLID OR SEGMENTED
3. MAXIMUM THERMAL AND ELECTRICAL PACKAGE PERFORMANCE IS ACHIEVED WHEN AN ARRAY OF SOLID VIAS IS INCORPORATED IN THE CENTER LAND PATTERN

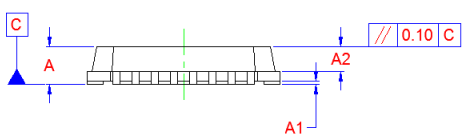
PCB LAND PATTERN



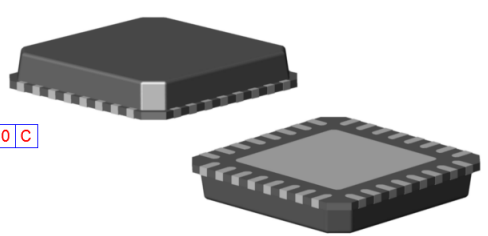
TOP VIEW



BOTTOM VIEW



SIDE VIEW



3-D VIEWS

Figure 9.1 USB3340 32-pin QFN, 5x5mm Body, 0.5mm Pitch

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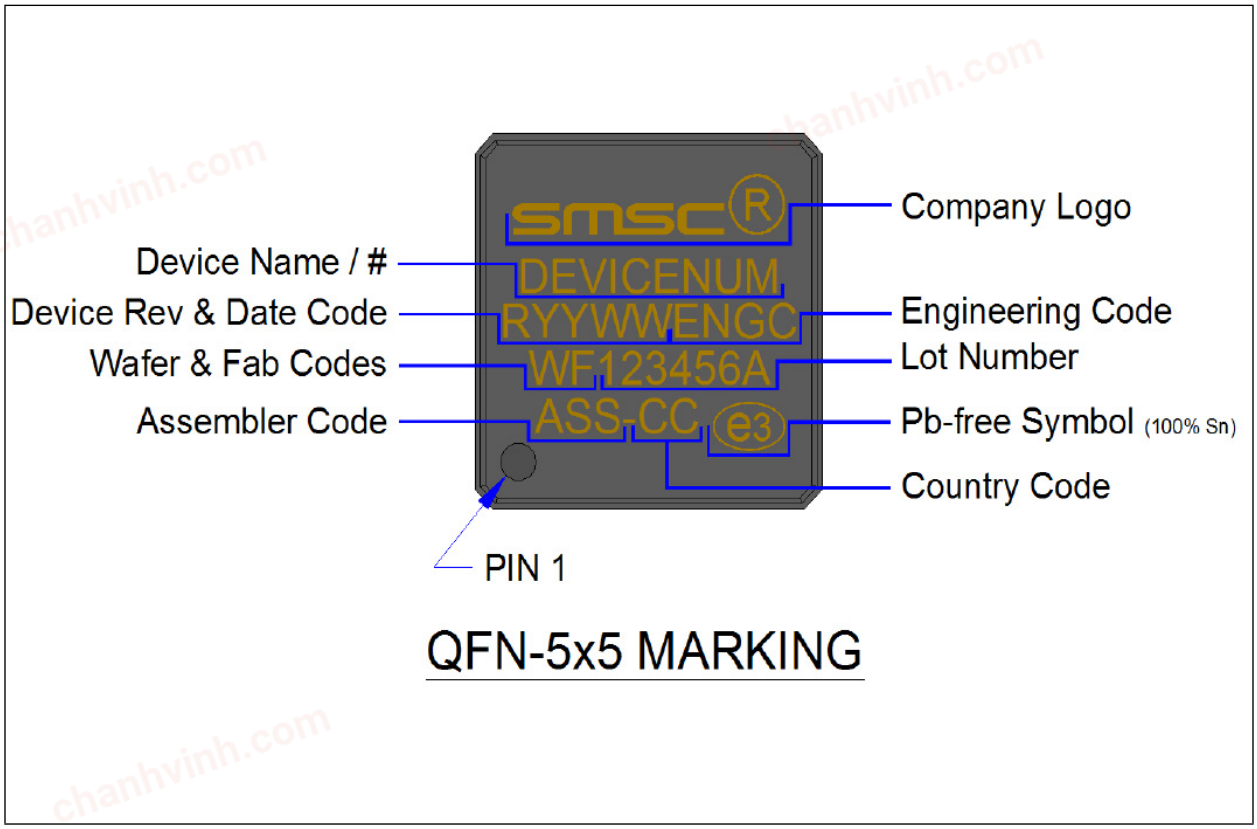


Figure 9.3 32QFN, 5x5 Package Marking

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Chapter 10 Datasheet Revision History

Table 10.1 Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
REV A (02-18-14)	REV A replaces previous SMSC version Rev. 1.1 (08-15-11). Document is Microchip branded; mention of SMSC removed, mention of “lead-free” removed, SMSC and vendor logos removed. Tape & Reel diagrams removed.	
Rev. 1.1 (08-15-11)	Table 3.1, Table 3.2	Removed requirement that VDD18 be active while VDDIO is active.
	Table 2.1	Modified VDDIO Description
	Table 4.1	Updated power specifications
	Table 4.4	Changed CPEN VOH specification.
	Section 7.1.3.1	Removed “and LPM” from section title.
	Figure 5.2	Removed connection to VDD18.
	Throughout Document	Updated support for Battery Charging v1.2.
	Throughout Document	Various editorial improvements.
Rev. 1.0 (01-20-11)	Initial datasheet release	

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