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USB3250

Hi-Speed USB Device Transceiver with UTMI Interface

PRODUCT FEATURES

Datasheet

- USB-IF "Hi-Speed" certified to USB 2.0 electrical specification
- Interface compliant with the UTMI specification (60MHz 8-bit unidirectional interface or 30MHz 16-bit bidirectional interface)
- Supports 480Mbps High Speed (HS) and 12Mbps Full Speed (FS) serial data transmission rates
- Integrated 45Ω and 1.5kΩ termination resistors reduce external component count
- Internal short circuit protection of DP and DM lines
- On-chip oscillator operates with low cost 12MHz crystal
- Robust and low power digital clock and data recovery circuit
- SYNC and EOP generation on transmit packets and detection on receive packets
- NRZI encoding and decoding
- Bit stuffing and unstuffing with error detection
- Supports the USB suspend state, HS detection, HS Chirp, Reset and Resume
- Support for all test modes defined in the USB 2.0 specification
- Draws 72mA (185mW) maximum current consumption in HS mode - ideal for bus powered functions
- On-die decoupling capacitance and isolation for immunity to digital switching noise
- Available in a 56-pin QFN package
- Full industrial operating temperature range from -40°C to +85°C (ambient)

Applications

The Universal Serial Bus (USB) is the preferred interface to connect Hi-Speed PC peripherals.

- Digital Still and Video Cameras
- MP3 Players
- External Hard Drives
- Scanners
- Entertainment Devices
- Printers
- Test and Measurement Systems
- POS Terminals
- Set Top Boxes

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Hi-Speed USB Device Transceiver with UTMI Interface

Datasheet

Ordering Information:

- USB3250-ABZJ for 56 pin, QFN lead-free RoHS compliant package, 8 x 8 x 0.85mm

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.

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Chapter 1 General Description

The USB3250 provides the Physical Layer (PHY) interface to a USB 2.0 Device Controller. The IC is available in a 56 pin QFN.

The USB3250 is a USB 2.0 physical layer transceiver (PHY) integrated circuit. SMSC's proprietary technology results in low power dissipation, which is ideal for building a bus powered USB 2.0 peripheral. The PHY can be configured for either an 8-bit unidirectional or a 16-bit bidirectional parallel interface, which complies with the USB Transceiver Macrocell Interface (UTMI) specification. It supports 480Mbps transfer rate, while remaining backward compatible with USB 1.1 legacy protocol at 12Mbps.

All required termination for the USB 2.0 Transceiver is internal. Internal 5.25V short circuit protection of DP and DM lines is provided for USB compliance.

While transmitting data, the PHY serializes data and generates SYNC and EOP fields. It also performs needed bit stuffing and NRZI encoding. Likewise, while receiving data, the PHY de-serializes incoming data, stripping SYNC and EOP fields and performs bit un-stuffing and NRZI decoding.

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Chapter 2 Functional Block Diagram

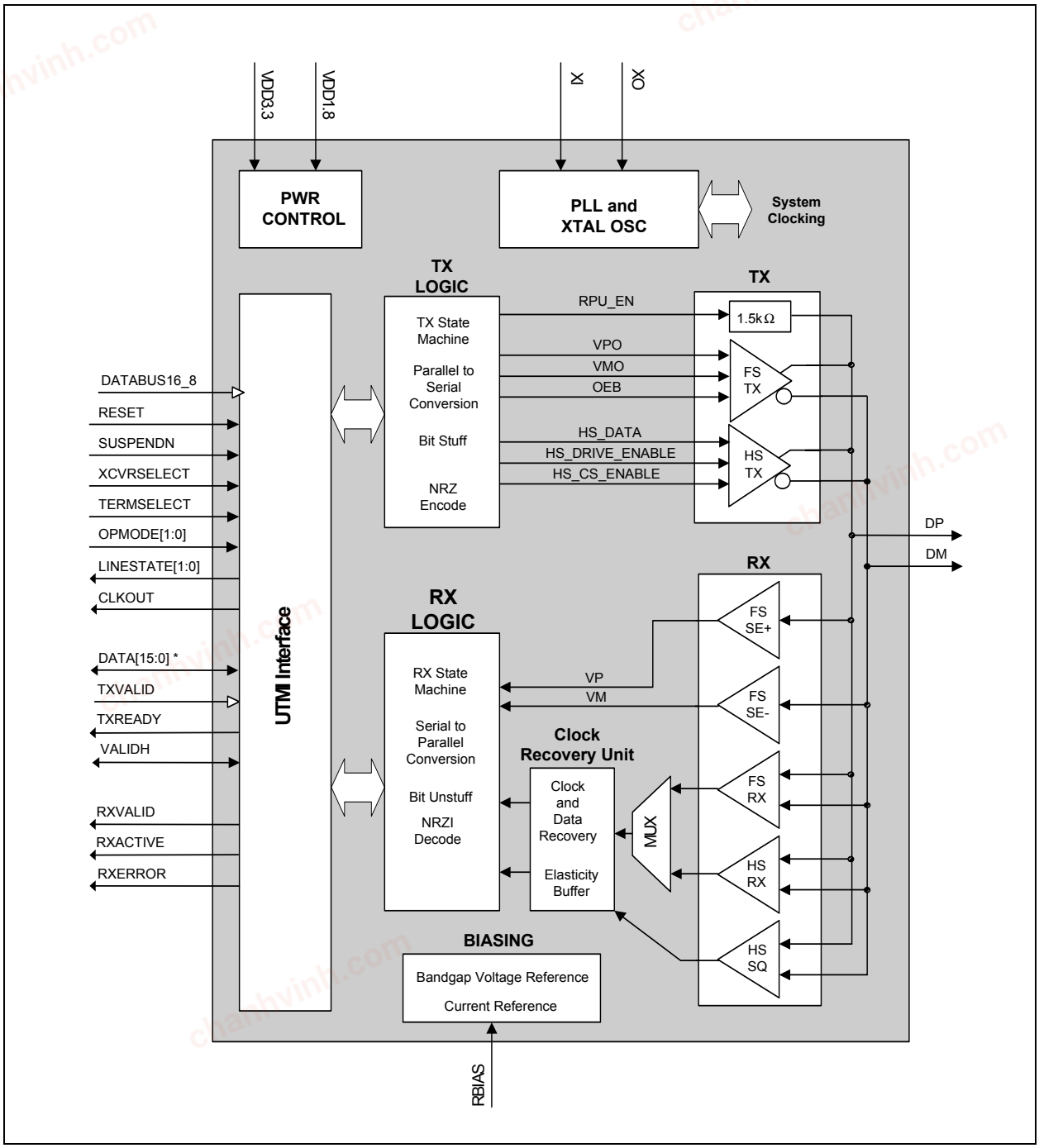


Figure 2.1 Block Diagram

Note: See Section 7.1, "Modes of Operation," on page 22 for a description of the digital interface.

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Chapter 3 Pin Configuration

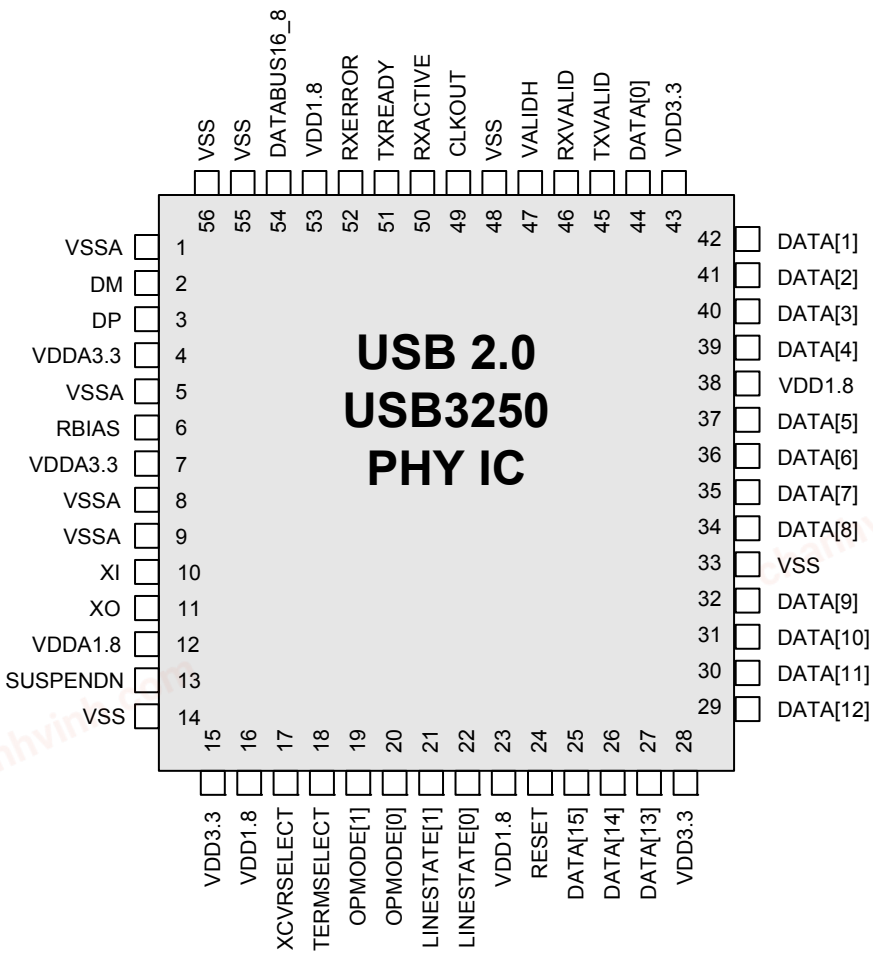


Figure 3.1 56 Pin USB3250 Pin Configuration (Top View)

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Chapter 4 Interface Signal Definition

Table 4.1 System Interface Signals

NAME	DIRECTION	ACTIVE LEVEL	DESCRIPTION
RESET	Input	High	**Reset.** Reset all state machines. After coming out of reset, must wait 5 rising edges of clock before asserting TXValid for transmit. Assertion of Reset: May be asynchronous to CLKOUT. De-assertion of Reset: Must be synchronous to CLKOUT unless RESET is asserted longer than two periods of CLKOUT.
XCVRSELECT	Input	N/A	**Transceiver Select.** This signal selects between the FS and HS transceivers: 0: HS transceiver enabled 1: FS transceiver enabled.
TERMSELECT	Input	N/A	**Termination Select.** This signal selects between the FS and HS terminations: 0: HS termination enabled 1: FS termination enabled
SUSPENDN	Input	Low	**Suspend.** Places the transceiver in a mode that draws minimal power from supplies. Shuts down all blocks not necessary for Suspend/Resume operation. While suspended, TERMSELECT must always be in FS mode to ensure that the 1.5k Ω pull-up on DP remains powered. 0: Transceiver circuitry drawing suspend current 1: Transceiver circuitry drawing normal current
CLKOUT	Output	Rising Edge	**System Clock.** This output is used for clocking receive and transmit parallel data at 60MHz (8-bit mode) or 30MHz (16-bit mode). When in 8-bit mode, this specification refers to CLKOUT as CLK60. When in 16-bit mode, CLKOUT is referred to as CLK30.
OPMODE[1:0]	Input	N/A	**Operational Mode.** These signals select between the various operational modes: [1] [0] Description 0 0 0: Normal Operation 0 1 1: Non-driving (all terminations removed) 1 0 2: Disable bit stuffing and NRZI encoding 1 1 3: Reserved
LINESTATE[1:0]	Output	N/A	**Line State.** These signals reflect the current state of the USB data bus in FS mode, with [0] reflecting the state of DP and [1] reflecting the state of DM. When the device is suspended or resuming from a suspended state, the signals are combinatorial. Otherwise, the signals are synchronized to CLKOUT. [1] [0] Description 0 0 0: SE0 0 1 1: J State 1 0 2: K State 1 1 3: SE1
DATABUS16_8	Input	N/A	**Databus Select.** Selects between 8-bit and 16-bit data transfers. 0: 8-bit data path enabled. VALIDH is undefined. CLKOUT = 60MHz. 1: 16-bit data path enabled. CLKOUT = 30MHz.

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Table 4.2 Data Interface Signals

<table>
<tr><th>NAME</th><th>DIRECTION</th><th>ACTIVE LEVEL</th><th>DESCRIPTION</th></tr>
<tr><td rowspan="11">DATA[15:0]</td><td rowspan="11">Bidir</td><td rowspan="11">N/A</td><td colspan="4">DATA BUS. 16-BIT BIDIRECTIONAL MODE.</td></tr>
<tr><td>TXVALID</td><td>RXVALID</td><td>VALIDH</td><td>DATA[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>X</td><td>Not used</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>DATA[7:0] output is valid for receive
VALIDH is an output</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DATA[15:0] output is valid for receive
VALIDH is an output</td></tr>
<tr><td>1</td><td>X</td><td>0</td><td>DATA[7:0] input is valid for transmit
VALIDH is an input</td></tr>
<tr><td>1</td><td>X</td><td>1</td><td>DATA[15:0] input is valid for transmit
VALIDH is an input</td></tr>
<tr><td colspan="4">DATA BUS. 8-BIT UNIDIRECTIONAL MODE.</td></tr>
<tr><td>TXVALID</td><td>RXVALID</td><td colspan="2">DATA[15:0]</td></tr>
<tr><td>0</td><td>0</td><td colspan="2">Not used</td></tr>
<tr><td>0</td><td>1</td><td colspan="2">DATA[15:8] output is valid for receive</td></tr>
<tr><td>1</td><td>X</td><td colspan="2">DATA[7:0] input is valid for transmit</td></tr>
<tr><td>TXVALID</td><td>Input</td><td>High</td><td colspan="4">Transmit Valid. Indicates that the TXDATA bus is valid for transmit. The assertion of TXVALID initiates the transmission of SYNC on the USB bus. The negation of TXVALID initiates EOP on the USB.

Control inputs (OPMODE[1:0], TERMSELECT,XCVRSELECT) must not be changed on the de-assertion or assertion of TXVALID. The PHY must be in a quiescent state when these inputs are changed.</td></tr>
<tr><td>TXREADY</td><td>Output</td><td>High</td><td colspan="4">Transmit Data Ready. If TXVALID is asserted, the SIE must always have data available for clocking into the TX Holding Register on the rising edge of CLKOUT. TXREADY is an acknowledgement to the SIE that the transceiver has clocked the data from the bus and is ready for the next transfer on the bus. If TXVALID is negated, TXREADY can be ignored by the SIE.</td></tr>
<tr><td>VALIDH</td><td>Bidir</td><td>N/A</td><td colspan="4">Transmit/Receive High Data Bit Valid (used in 16-bit mode only). When TXVALID = 1, the 16-bit data bus direction is changed to inputs, and VALIDH is an input. If VALIDH is asserted, DATA[15:0] is valid for transmission. If deasserted, only DATA[7:0] is valid for transmission. The DATA bus is driven by the SIE.

When TXVALID = 0 and RXVALID = 1, the 16-bit data bus direction is changed to outputs, and VALIDH is an output. If VALIDH is asserted, the DATA[15:0] outputs are valid for receive. If deasserted, only DATA[7:0] is valid for receive. The DATA bus is read by the SIE.</td></tr>
<tr><td>RXVALID</td><td>Output</td><td>High</td><td colspan="4">Receive Data Valid. Indicates that the RXDATA bus has received valid data. The Receive Data Holding Register is full and ready to be unloaded. The SIE is expected to latch the RXDATA bus on the rising edge of CLKOUT.</td></tr>
</table>

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Table 4.2 Data Interface Signals (continued)

NAME	DIRECTION	ACTIVE LEVEL	DESCRIPTION
RXACTIVE	Output	High	**Receive Active.** Indicates that the receive state machine has detected Start of Packet and is active.
RXERROR	Output	High	**Receive Error.** 0: Indicates no error. 1: Indicates a receive error has been detected. This output is clocked with the same timing as the RXDATA lines and can occur at anytime during a transfer.

Table 4.3 USB I/O Signals

NAME	DIRECTION	ACTIVE LEVEL	DESCRIPTION
DP	I/O	N/A	**USB Positive Data Pin**.
DM	I/O	N/A	**USB Negative Data Pin**.

Table 4.4 Biasing and Clock Oscillator Signals

NAME	DIRECTION	ACTIVE LEVEL	DESCRIPTION
RBIAS	Input	N/A	**External 1% bias resistor**. Requires a 12KΩ resistor to ground. Used for setting HS transmit current level and on-chip termination impedance.
XI/XO	Input	N/A	**External crystal**. 12MHz crystal connected from XI to XO.

Table 4.5 Power and Ground Signals

NAME	DIRECTION	ACTIVE LEVEL	DESCRIPTION
VDD3.3	N/A	N/A	**3.3V Digital Supply**. Powers digital pads. See Note 4.1
VDD1.8	N/A	N/A	**1.8V Digital Supply**. Powers digital core.
VSS	N/A	N/A	**Digital Ground**. See Note 4.2
VDDA3.3	N/A	N/A	**3.3V Analog Supply**. Powers analog I/O and 3.3V analog circuitry.
VDDA1.8	N/A	N/A	**1.8V Analog Supply**. Powers 1.8V analog circuitry. See Note 4.1
VSSA	N/A	N/A	**Analog Ground**. See Note 4.2

Note 4.1 A Ferrite Bead (with DC resistance <.5 Ohms) is recommended for filtering between both the VDD3.3 and VDDA3.3 supplies and the VDD1.8 and VDDA1.8 Supplies. See Figure 8.9 Application Diagram for 56-pin QFN Packageon page 44.

Note 4.2 All VSS and VSSA are bonded to the exposed pad under the IC in the package. The exposed pad must be connected to solid GND plane on printed circuit board.

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Chapter 5 Limiting Values

Table 5.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
1.8V Supply Voltage (VDD1.8 and VDDA1.8)	$V_{DD1.8}$		-0.5		TBD	V
3.3V Supply Voltage (VDD3.3 and VDDA3.3)	$V_{DD3.3}$		-0.5		4.6	V
Input Voltage	V_I		-0.5		4.6	V
Storage Temperature	T_{STG}		-40		+125	°C
[1] Equivalent to discharging a 100pF capacitor via a 1.5kΩ resistor (HBM).						

Note: In accordance with the Absolute Maximum Rating System (IEC 60134

Table 5.2 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
1.8V Supply Voltage (VDD1.8 and VDDA1.8)	$V_{DD1.8}$		1.6	1.8	2.0	V
3.3V Supply Voltage (VDD3.3 and VDDA3.3)	$V_{DD3.3}$		3.0	3.3	3.6	V
Input Voltage on Digital Pins	V_I		0.0		$V_{DD3.3}$	V
Input Voltage on Analog I/O Pins (DP, DM)	$V_{I(I/O)}$		0.0		$V_{DD3.3}$	V
Ambient Temperature	T_A		-40		+85	°C

Table 5.3 Recommended External Clock Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
System Clock Frequency		XO driven by the external clock; and no connection at XI		12 (+/- 100ppm) Note 5.1		MHz
System Clock Duty Cycle		XO driven by the external clock; and no connection at XI	45	50	55	%

Note 5.1 The USB 2.0 Specification requires a frequency accuracy of +/-500ppm. For applications using a quartz crystal, SMSC recommends that it be specified with an accuracy of +/-100ppm. Resonators that are specified to meet the +/-500ppm accuracy have also been used successfully with the USB3250.

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Chapter 6 Electrical Characteristics

Table 6.1 Electrical Characteristics: Supply Pins

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FS TRANSMIT	Total Power	$P_{TOT(FSTX)}$	FS transmitting at 12Mb/s; 50pF load on DP and DM		86	115	mW
	VDD3.3 Power	$P_{3.3V(FSTX)}$			57	76	mW
	VDD1.8 Power	$P_{1.8V(FSTX)}$			29	39	mW
FS RECEIVE	Total Power	$P_{TOT(FSRX)}$	FS receiving at 12Mb/s		75	115	mW
	VDD3.3 Power	$P_{3.3V(FSRX)}$			46	76	mW
	VDD1.8 Power	$P_{1.8V(FSRX)}$			29	39	mW
HS TRANSMIT	Total Power	$P_{TOT(HSTX)}$	HS transmitting into a 45Ω load		158	185	mW
	VDD3.3 Power	$P_{3.3V\ (HSTX)}$			110	130	mW
	VDD1.8 Power	$P_{1.8V\ (HSTX)}$			48	55	mW
HS RECEIVE	Total Power	$P_{TOT(HSRX)}$	HS receiving at 480Mb/s		155	185	mW
	VDD3.3 Power	$P_{3.3V\ (HSRX)}$			107	130	mW
	VDD1.8 Power	$P_{1.8V\ (HSRX)}$			48	55	mW
SUSPEND MODE 1	Total Current	$I_{DD(SUSP1)}$	15kΩ pull-down and 1.5kΩ pull-up resistor on pin DP not connected.		123	240	uA
	VDD3.3 Current	$I_{3.3V\ (SUSP1)}$			68	120	uA
	VDD1.8 Current	$I_{1.8V\ (SUSP1)}$			55	120	uA
SUSPEND MODE 2	Total Current	$I_{DD(SUSP2)}$	15kΩ pull-down and 1.5kΩ pull-up resistor on pin DP connected.		323	460	uA
	VDD3.3 Current	$I_{3.3V\ (SUSP2)}$			268	340	uA
	VDD1.8 Current	$I_{1.8V\ (SUSP2)}$			55	120	uA
($V_{DD1.8}$ =1.6 to 2.0V; $V_{DD3.3}$ =3.0 to 3.6V; V_{SS} = 0V; T_A = -40 °C to +85°C; unless otherwise specified.)							

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Table 6.2 DC Electrical Characteristics: Logic Pins

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low-Level Input Voltage	V_{IL}		V_{SS}		0.8	V
High-Level Input Voltage	V_{IH}		2.0		$V_{DD3.3}$	V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA	$V_{DD3.3}$ - 0.5			V
Input Leakage Current	I_{LI}				± 1	uA
Pin Capacitance	C_{pin}				4	pF
($V_{DD1.8}$ =1.6 to 2.0V; $V_{DD3.3}$ =3.0 to 3.6V; V_{SS} = 0V; T_A = -40 °C to +85°C; unless otherwise specified. Pins Data[15:0] and VALIDH have passive pull-down elements.)						

Table 6.3 DC Electrical Characteristics: Analog I/O Pins (DP/DM)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FS FUNCTIONALITY						
INPUT LEVELS						
Differential Receiver Input Sensitivity	V_{DIFS}	| V(DP) - V(DM) |	0.2			V
Differential Receiver Common-Mode Voltage	V_{CMFS}		0.8		2.5	V
Single-Ended Receiver Low Level Input Voltage	V_{ILSE}				0.8	V
Single-Ended Receiver High Level Input Voltage	V_{IHSE}		2.0			V
Single-Ended Receiver Hysteresis	V_{HYSSE}		0.050		0.150	V
OUTPUT LEVELS						
Low Level Output Voltage	V_{FSOL}	Pull-up resistor on DP; R_L = 1.5kΩ to $V_{DD3.3}$			0.3	V
High Level Output Voltage	V_{FSOH}	Pull-down resistor on DP, DM; R_L = 15kΩ to GND	2.8		3.6	V
TERMINATION						
Driver Output Impedance for HS and FS	Z_{HSDRV}	Steady state drive (See Figure 6.1)	40.5	45	49.5	Ω
Input Impedance	Z_{INP}	TX, RPU disabled	10			MΩ
Pull-up Resistor Impedance	Z_{PU}		1.425		1.575	KΩ
Termination Voltage For Pull-up Resistor On Pin DP	V_{TERM}		3.0		3.6	V
HS FUNCTIONALITY						
INPUT LEVELS						
HS Differential Input Sensitivity	V_{DIHS}	| V(DP) - V(DM) |	100			mV
($V_{DD1.8}$ =1.6 to 2.0V; $V_{DD3.3}$ =3.0 to 3.6V; V_{SS} = 0V; T_A = -40 °C to +85°C; unless otherwise specified.)						

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Table 6.3 DC Electrical Characteristics: Analog I/O Pins (DP/DM) (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HS Data Signaling Common Mode Voltage Range	V_{CMHS}		-50		500	mV
HS Squelch Detection Threshold (Differential)	V_{HSSQ}	Squelch Threshold			100	mV
		Unsquelch Threshold	150			mV
OUTPUT LEVELS						
High Speed Low Level Output Voltage (DP/DM referenced to GND)	V_{HSOL}	45Ω load	-10		10	mV
High Speed High Level Output Voltage (DP/DM referenced to GND)	V_{HSOH}	45Ω load	360		440	mV
High Speed IDLE Level Output Voltage (DP/DM referenced to GND)	V_{OLHS}	45Ω load	-10		10	mV
Chirp-J Output Voltage (Differential)	V_{CHIRPJ}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	700		1100	mV
Chirp-K Output Voltage (Differential)	V_{CHIRPK}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	-900		-500	mV
LEAKAGE CURRENT						
OFF-State Leakage Current	I_{LZ}				± 1	uA
PORT CAPACITANCE						
Transceiver Input Capacitance	C_{IN}	Pin to GND		5	10	pF
($V_{DD1.8}$ =1.6 to 2.0V; $V_{DD3.3}$ =3.0 to 3.6V; V_{SS} = 0V; T_A = -40 °C to +85°C; unless otherwise specified.)						

Table 6.4 Dynamic Characteristics: Analog I/O Pins (DP/DM)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FS OUTPUT DRIVER TIMING						
Rise Time	T_{FSR}	CL = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
Fall Time	T_{FFF}	CL = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
Output Signal Crossover Voltage	V_{CRS}	Excluding the first transition from IDLE state	1.3		2.0	V
Differential Rise/Fall Time Matching	F_{RFM}	Excluding the first transition from IDLE state	90		111.1	%
($V_{DD1.8}$ =1.6 to 2.0V; $V_{DD3.3}$ =3.0 to 3.6V; V_{SS} = 0V; T_A = -40 °C to +85°C; unless otherwise specified.)						

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Table 6.4 Dynamic Characteristics: Analog I/O Pins (DP/DM)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HS OUTPUT DRIVER TIMING						
Differential Rise Time	T_{HSR}		500			ps
Differential Fall Time	T_{HSF}		500			ps
Driver Waveform Requirements		Eye pattern of Template 1 in USB 2.0 specification			See Figure 6.2	
HIGH SPEED MODE TIMING						
Receiver Waveform Requirements		Eye pattern of Template 4 in USB 2.0 specification			See Figure 6.2	
Data Source Jitter and Receiver Jitter Tolerance		Eye pattern of Template 4 in USB 2.0 specification			See Figure 6.2	
($V_{DD1.8}$ =1.6 to 2.0V; $V_{DD3.3}$ =3.0 to 3.6V; V_{SS} = 0V; T_A = -40 ^oC to +85^oC; unless otherwise specified.)						

Table 6.5 Dynamic Characteristics: Digital UTMI Pins

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UTMI TIMING						
RXDATA[7:0]	T_{PD}	Propagation delay from CLKOUT to signal CL = 10pF		2	4	ns
RXVALID				2	4	
RXACTIVE				2	4	
RXERROR				2	4	
LINESTATE[1:0]				2	4	
TXREADY				2	4	
TXDATA[7:0]	T_{SU}	Setup time from signal to CLKOUT	4			ns
TXVALID			4			
OPMODE[1:0]			4			
XCVRSELECT			4			
TERMSELECT			4			
SUSPENDN			4			
TXDATA[7:0]	T_H	Hold time from CLKOUT to signal	0			ns
TXVALID			0			
OPMODE[1:0]			0			
XCVRSELECT			0			
TERMSELECT			0			
SUSPENDN			0			
($V_{DD1.8}$ =1.6 to 2.0V; $V_{DD3.3}$ =3.0 to 3.6V; V_{SS} = 0V; T_A = -40 ^oC to +85^oC; unless otherwise specified.)						

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6.1 Driver Characteristics of Full-Speed Drivers in Hi-Speed Capable Transceivers

The USB transceiver uses a differential output driver to drive the USB data signal onto the USB cable. Figure 6.1 shows the V/I characteristics for a full-speed driver which is part of a Hi-Speed capable transceiver. The normalized V/I curve for the driver must fall entirely inside the shaded region. The V/I region is bounded by the minimum driver impedance above (40.5 Ohm) and the maximum driver impedance below (49.5 Ohm). The output voltage must be within 10mV of ground when no current is flowing in or out of the pin.

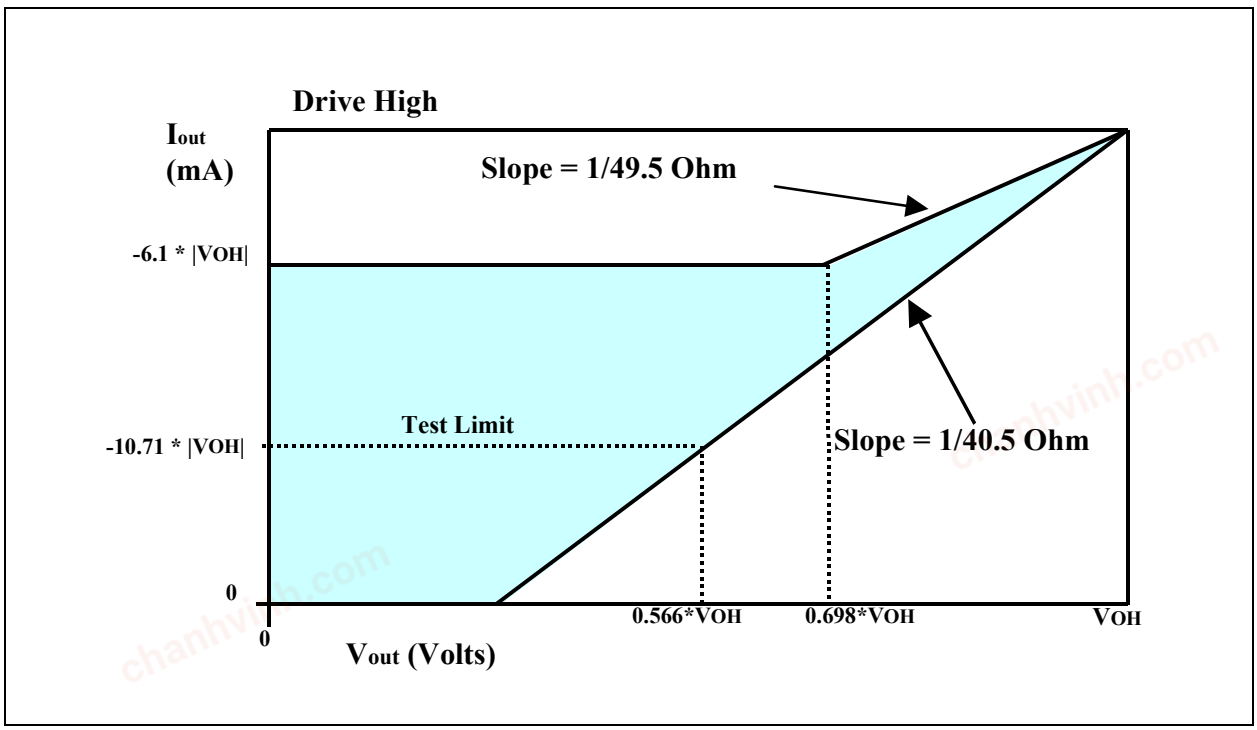


Figure 6.1 Full-Speed Driver VOH/IOH Characteristics for Hi-Speed Capable Transceiver

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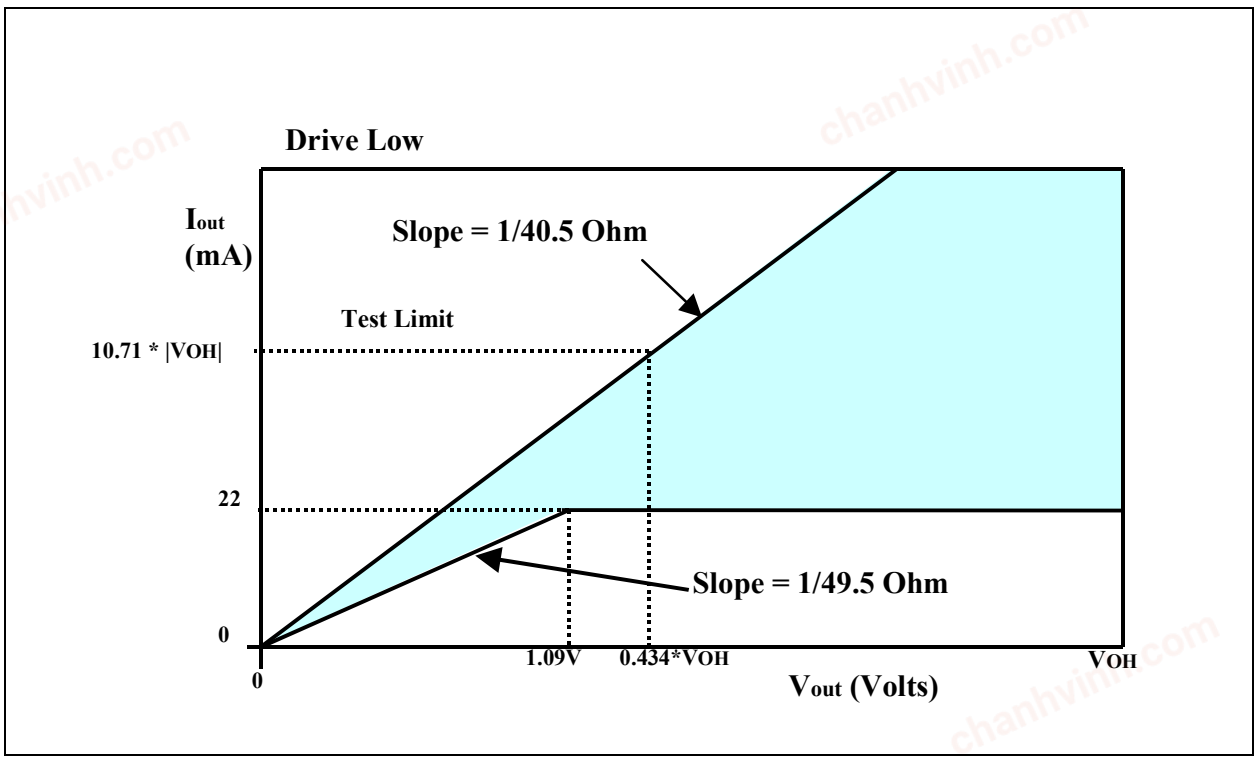


Figure 6.2 Full-Speed Driver VOL/IOL Characteristics for Hi-Speed Capable Transceiver

6.2 Hi-Speed Signaling Eye Patterns

Hi-Speed USB signals are characterized using eye patterns. For measuring the eye patterns 4 points have been defined (see Figure 6.3). The Universal Serial Bus Specification Rev.2.0 defines the eye patterns in several 'templates'. The two templates that are relevant to the PHY are shown below.

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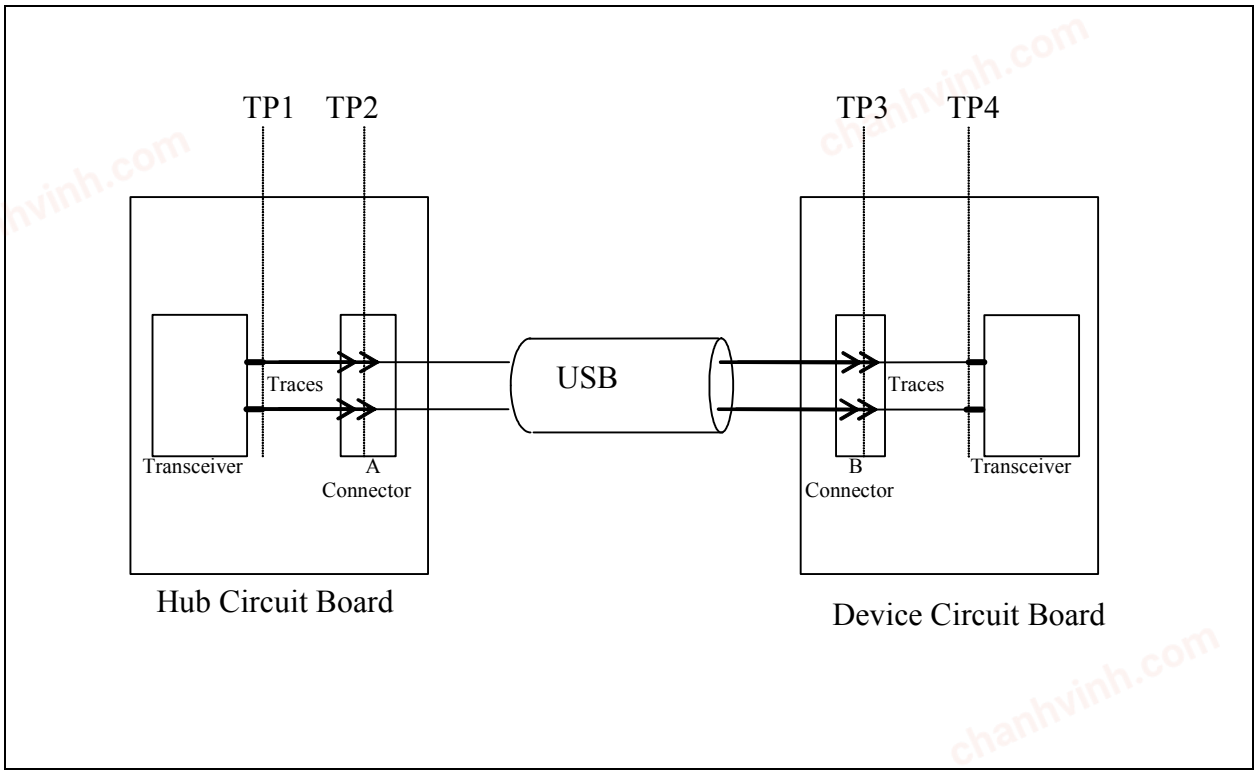


Figure 6.3 Eye Pattern Measurement Planes

The eye pattern in Figure 6.4 defines the transmit waveform requirements for a hub (measured at TP2 of Figure 6.3) or a device without a captive cable (measured at TP3 of Figure 6.3). The corresponding signal levels and timings are given in Table 6.6. Time is specified as a percentage of the unit interval (UI), which represents the nominal bit duration for a 480 Mbit/s transmission rate.

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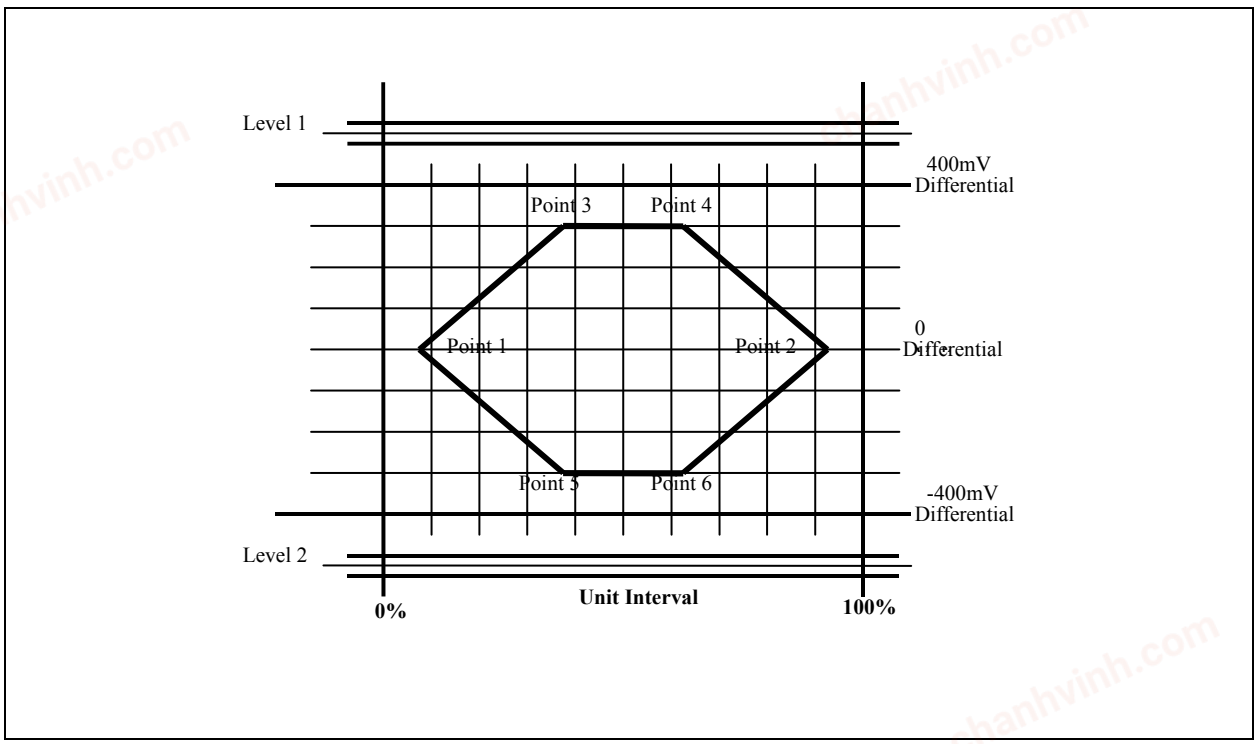


Figure 6.4 Eye Pattern for Transmit Waveform and Eye Pattern Definition

Table 6.6 Eye Pattern for Transmit Waveform and Eye Pattern Definition

	VOLTAGE LEVEL (D+, D-)	TIME (% OF UNIT INTERVAL)
Level 1	525mV in UI following a transition, 475mV in all others	N/A
Level 2	-525mV in UI following a transition, -475mV in all others	N/A
Point 1	0V	7.5% UI
Point 2	0V	92.5% UI
Point 3	300mV	37.5% UI
Point 4	300mV	62.5% UI
Point 5	-300mV	37.5% UI
Point 6	-300mV	62.5% UI

The eye pattern in Figure 6.5 defines the receiver sensitivity requirements for a hub (signal applied at test point TP2 of Figure 6.3) or a device without a captive cable (signal applied at test point TP3 of Figure 6.3). The corresponding signal levels and timings are given in Table 6.7. Timings are given as a percentage of the unit interval (UI), which represents the nominal bit duration for a 480 Mbit/s transmission rate.

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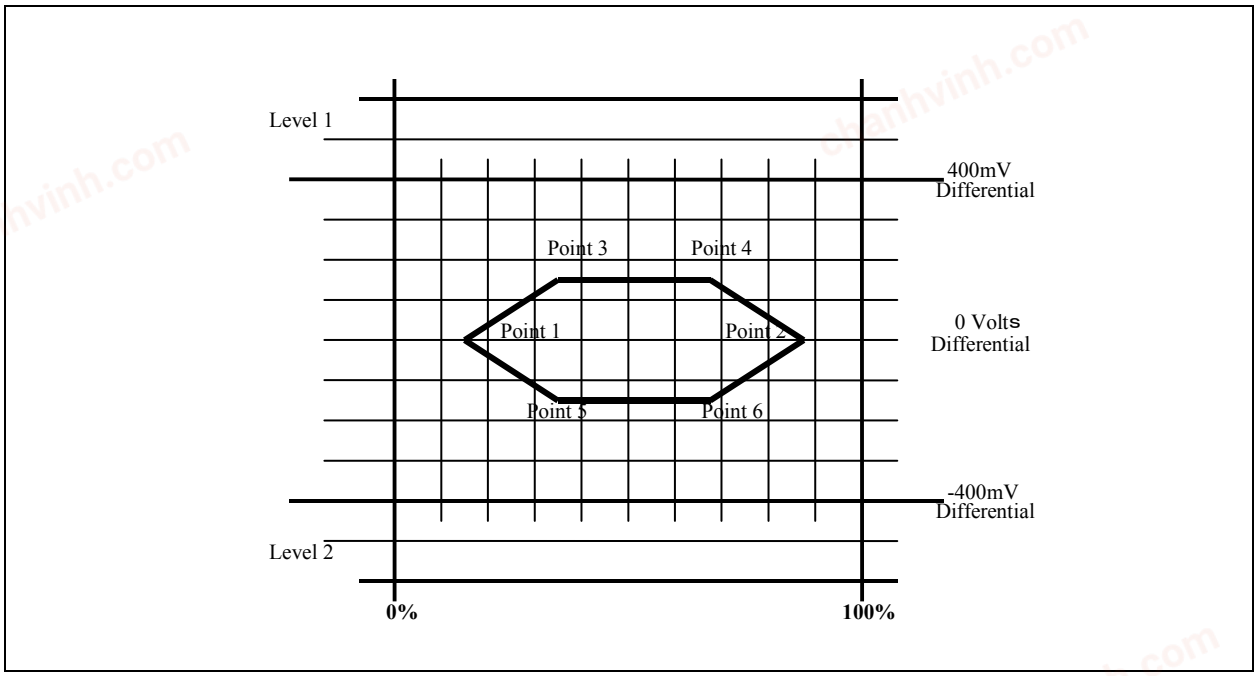


Figure 6.5 Eye Pattern for Receive Waveform and Eye Pattern Definition

Table 6.7 Eye Pattern for Receive Waveform and Eye Pattern Definition

	VOLTAGE LEVEL (D+, D-)	TIME (% OF UNIT INTERVAL)
Level 1	575mV	N/A
Level 2	-575mV	N/A
Point 1	0V	15% UI
Point 2	0V	85% UI
Point 3	150mV	35% UI
Point 4	150mV	65% UI
Point 5	-150mV	35% UI
Point 6	-150mV	65% UI

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Chapter 7 Functional Overview

Figure 2.1 Block Diagramon page 7 shows the functional block diagram of the USB3250. Each of the functions is described in detail below.

7.1 Modes of Operation

The USB3250 supports two modes of operation. See Figure 7.1 for a block diagram of the digital interface.

- 8-bit unidirectional mode. Selected when DATABUS16_8 = 0. CLKOUT runs at 60MHz. The 8-bit transmit data bus uses the lower 8 bits of the DATA bus (ie, TXDATA[7:0] = DATA[7:0]). The 8-bit receive data bus uses the upper 8 bits of the DATA bus (ie, RXDATA[7:0] = DATA[15:8]).
- 16-bit bidirectional mode. Selected when DATABUS16_8 = 1. CLKOUT runs at 30MHz. An additional signal (VALIDH) is used to identify whether the high byte of the respective 16-bit data word is valid. The full 16-bit DATA bus is used for transmit and receive operations. If TXVALID is asserted, then the DATA[15:0] bus accepts transmit data from the SIE. If TXVALID is deasserted, then the DATA[15:0] bus presents received data to the SIE. VALIDH is undefined when DATABUS16_8 = 0 (8-bit mode).

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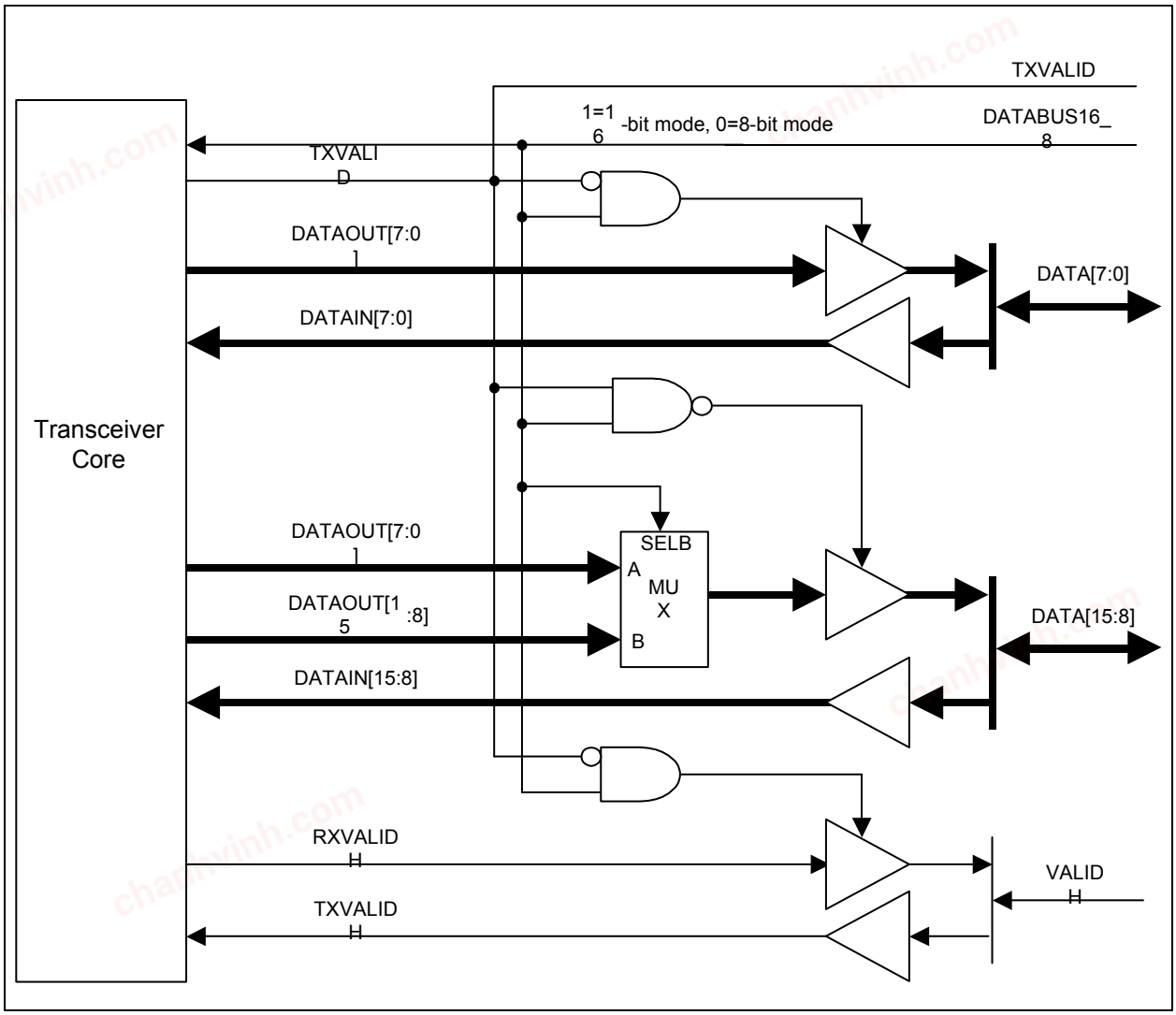


Figure 7.1 Bidirectional 16-bit interface

7.2 System Clocking

This block connects to either an external 12MHz crystal or an external clock source and generates a 480MHz multi-phase clock. The clock is used in the CRC block to over-sample the incoming received data, resynchronize the transmit data, and is divided down to a 30MHz or 60MHz version (CLKOUT) which acts as the system byte clock. The PLL block also outputs a clock valid signal to the other parts of the transceiver when the clock signal is stable. All UTMI signals are synchronized to the CLKOUT output. The behavior of the CLKOUT is as follows:

- Produce the first CLKOUT transition no later than 5.6ms after negation of SUSPENDN. The CLKOUT signal frequency error is less than 10% at this time.
- The CLKOUT signal will fully meet the required accuracy of ±500ppm no later than 1.4ms after the first transition of CLKOUT.

In HS mode there is one CLKOUT cycle per byte time. The frequency of CLKOUT does not change when the Macrocell is switched between HS to FS modes. In FS mode (8-bit mode) there are 5 CLK60 cycles per FS bit time, typically 40 CLK60 cycles per FS byte time. If a received byte contains a stuffed bit then the byte boundary can be stretched to 45 CLK60 cycles, and two stuffed bits would result in a 50 CLK60 cycles.

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Figure 7.2 shows the relationship between CLK60 and the transmit data transfer signals in FS mode. TXREADY is only asserted for one CLK60 per byte time to signal the SIE that the data on the TXDATA lines has been read by the Macrocell. The SIE may hold the data on the TXDATA lines for the duration of the byte time. Transitions of TXVALID must meet the defined setup and hold times relative to CLK60.

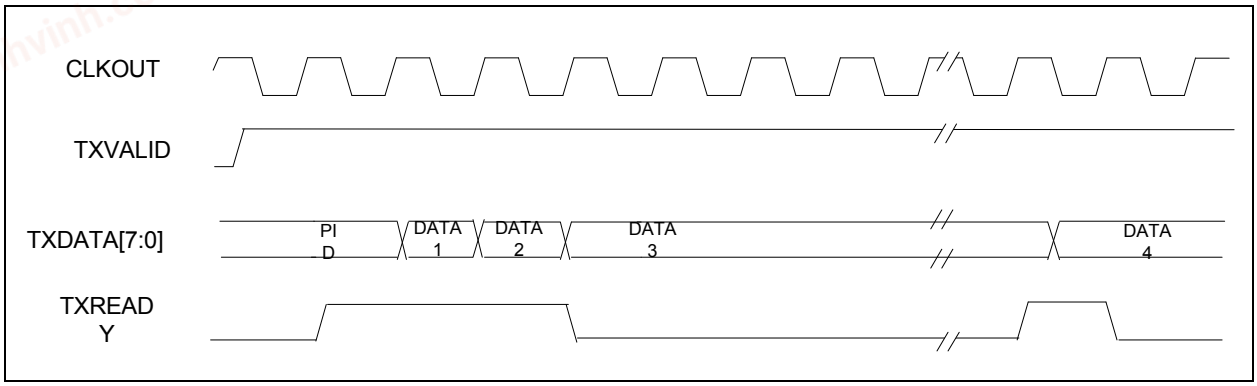


Figure 7.2 FS CLK Relationship to Transmit Data and Control Signals (8-bit mode)

Figure 7.3 shows the relationship between CLK60 and the receive data control signals in FS mode. RXACTIVE "frames" a packet, transitioning only at the beginning and end of a packet. However transitions of RXVALID may take place any time 8 bits of data are available. Figure 7.3 also shows how RXVALID is only asserted for one CLKOUT cycle per byte time even though the data may be presented for the full byte time. The XCVRSELECT signal determines whether the HS or FS timing relationship is applied to the data and control signals.

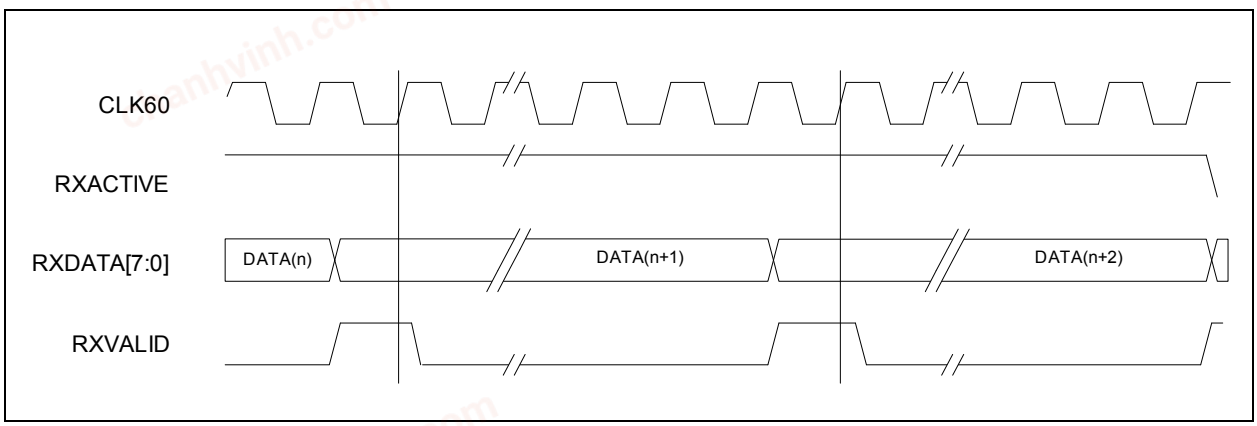


Figure 7.3 FS CLK Relationship to Receive Data and Control Signals (8-bit mode)

7.3 Clock and Data Recovery Circuit

This block consists of the Clock and Data Recovery Circuit and the Elasticity Buffer. The Elasticity Buffer is used to compensate for differences between the transmitting and receiving clock domains. The USB 2.0 specification defines a maximum clock error of ±1000ppm of drift.

7.4 TX Logic

This block receives parallel data bytes placed on the DATA bus and performs the necessary transmit operations. These operations include parallel to serial conversion, bit stuffing and NRZI encoding. Upon valid assertion of the proper TX control lines by the SIE and TX State Machine, the TX LOGIC

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block will synchronously shift, at either the FS or HS rate, the data to the FS/HS TX block to be transmitted on the USB cable. Data transmit timing is shown in Figure 7.4.

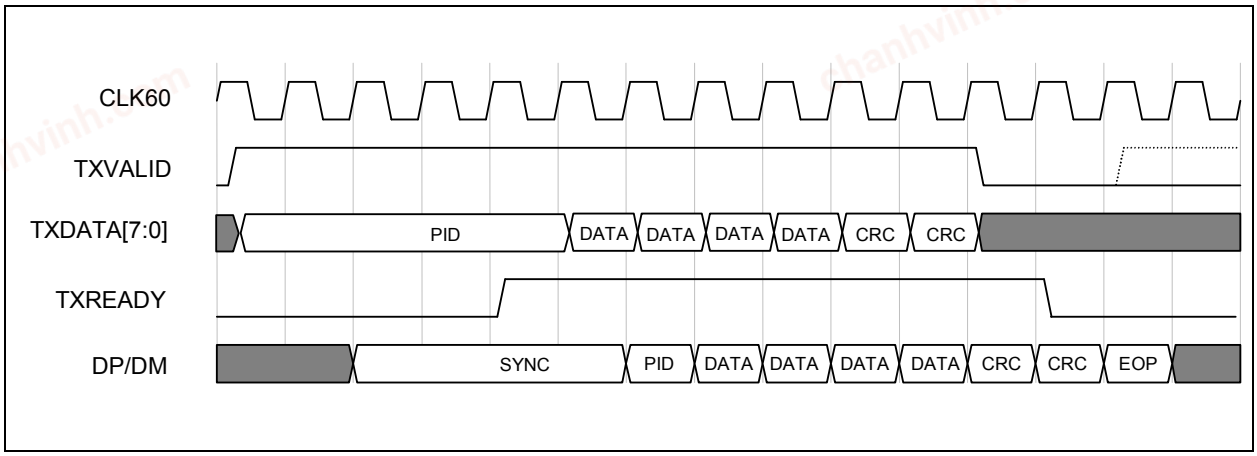


Figure 7.4 Transmit Timing for a Data Packet (8-bit mode)

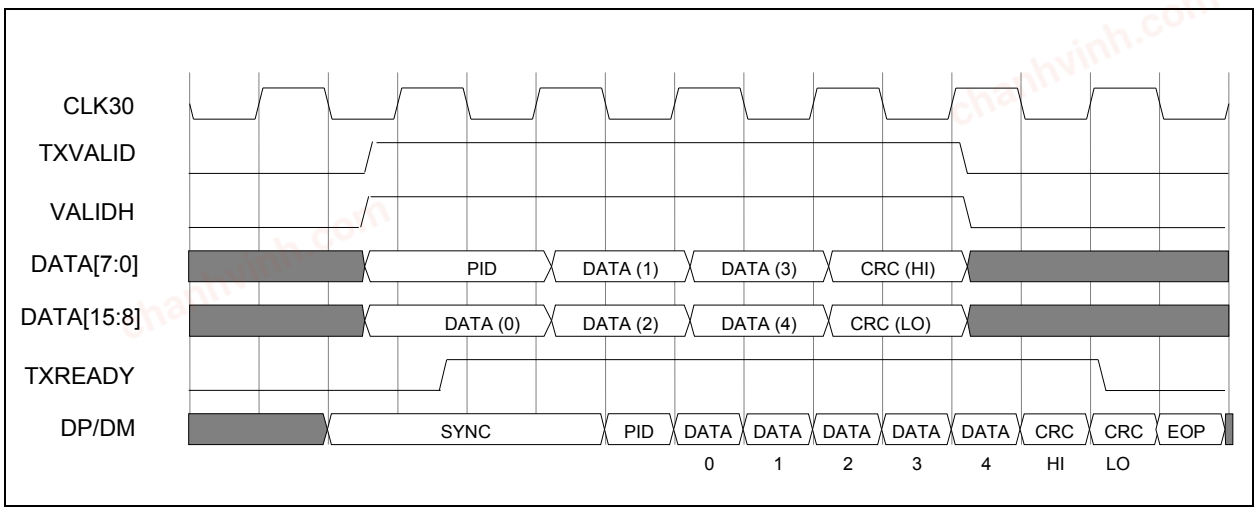


Figure 7.5 Transmit Timing for 16-bit Data, Even Byte Count

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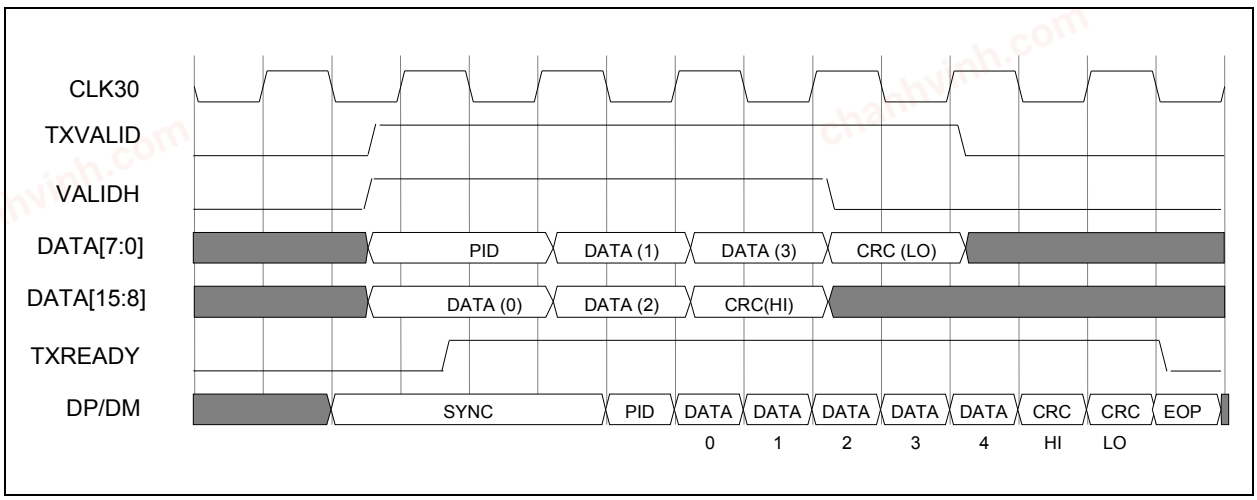


Figure 7.6 Transmit Timing for 16-bit Data, Odd Byte Count

The behavior of the Transmit State Machine is described below.

- Asserting a RESET forces the transmit state machine into the Reset state which negates TXREADY. When RESET is negated the transmit state machine will enter a wait state.
- The SIE asserts TXVALID to begin a transmission.
- After the SIE asserts TXVALID it can assume that the transmission has started when it detects TXREADY has been asserted.
- The SIE must assume that the PHY has consumed a data byte if TXREADY and TXVALID are asserted on the rising edge of CLKOUT.
- The SIE must have valid packet information (PID) asserted on the TXDATA bus coincident with the assertion of TXVALID.
- TXREADY is sampled by the SIE on the rising edge of CLKOUT.
- The SIE negates TXVALID to complete a packet. Once negated, the transmit logic will never reassert TXREADY until after the EOP has been generated. (TXREADY will not re-assert until TXVALID asserts again).
- The PHY is ready to transmit another packet immediately, however the SIE must conform to the minimum inter-packet delays identified in the USB 2.0 specification.

7.5 RX Logic

This block receives serial data from the CRC block and processes it to be transferred to the SIE on the RXDATA bus. The processing involved includes NRZI decoding, bit unstuffing, and serial to parallel conversion. Upon valid assertion of the proper RX control lines by the RX State Machine, the RX Logic block will provide bytes to the RXDATA bus as shown in the figures below. The behavior of the Receive State Machine is described below.

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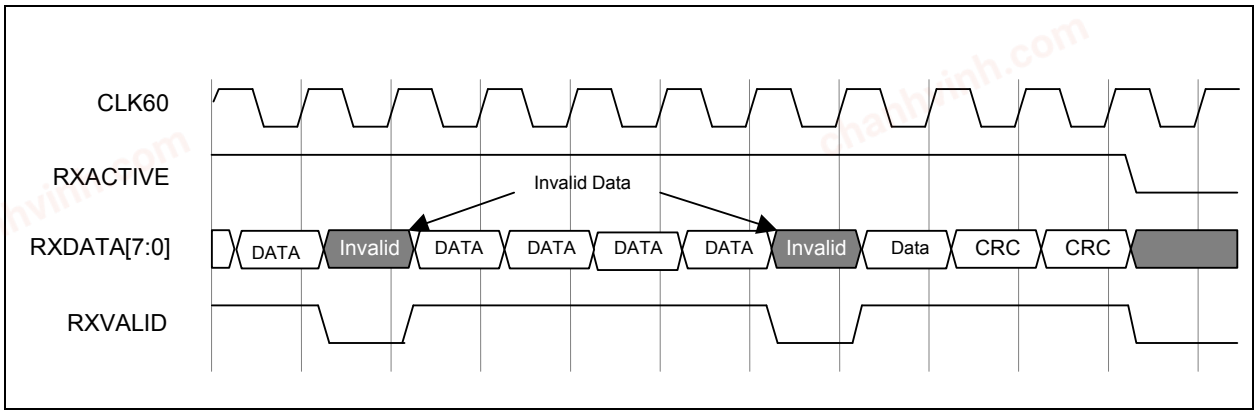


Figure 7.7 Receive Timing for Data with Unstuffed Bits (8-bit mode)

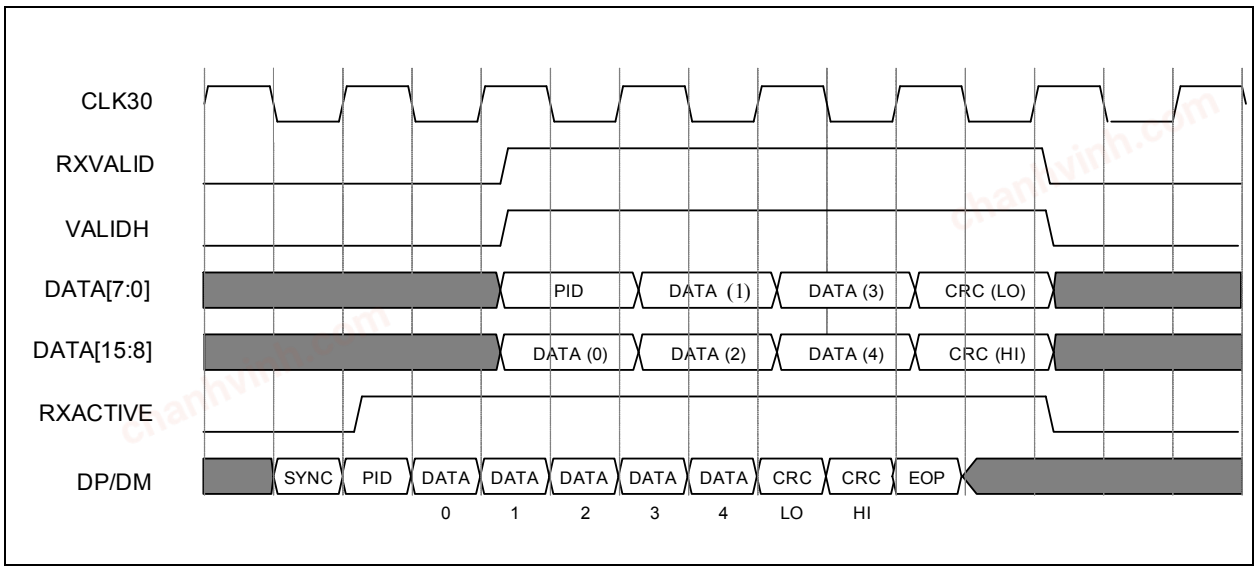


Figure 7.8 Receive Timing for 16-bit Data, Even Byte Count

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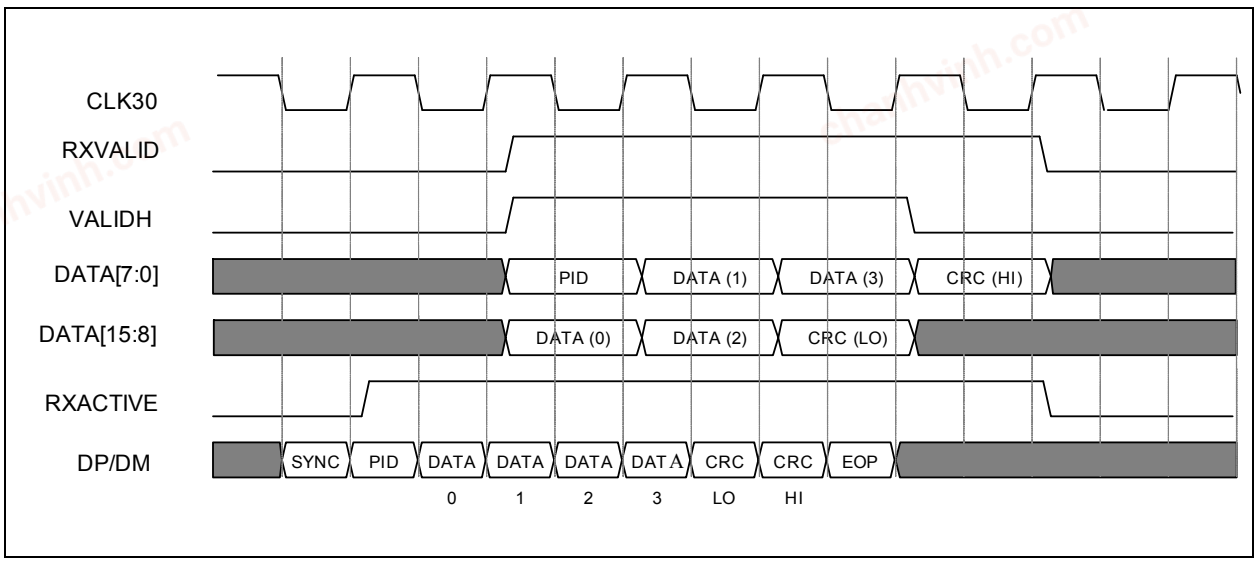


Figure 7.9 Receive Timing for 16-bit Data, Odd Byte Count

The assertion of RESET will force the Receive State Machine into the Reset state. The Reset state deasserts RXACTIVE and RXVALID. When the RESET signal is deasserted the Receive State Machine enters the RX Wait state and starts looking for a SYNC pattern on the USB. When a SYNC pattern is detected the state machine will enter the Strip SYNC state and assert RXACTIVE. The length of the received Hi-Speed SYNC pattern varies and can be up to 32 bits long or as short as 12 bits long when at the end of five hubs. As a result, the state machine may remain in the Strip SYNC state for several byte times before capturing the first byte of data and entering the RX Data state.

After valid serial data is received, the state machine enters the RX Data state, where the data is loaded into the RX Holding Register on the rising edge of CLKOUT and RXVALID is asserted. The SIE must clock the data off the RXDATA bus on the next rising edge of CLKOUT. If OPMODE = Normal, then stuffed bits are stripped from the data stream. Each time 8 stuffed bits are accumulated the state machine will enter the RX Data Wait state, negating RXVALID thus skipping a byte time.

When the EOP is detected the state machine will enter the Strip EOP state and negate RXACTIVE and RXVALID. After the EOP has been stripped the Receive State Machine will reenter the RX Wait state and begin looking for the next packet.

The behavior of the Receive State Machine is described below:

- RXACTIVE and RXREADY are sampled on the rising edge of CLKOUT.
- In the RX Wait state the receiver is always looking for SYNC.
- The USB3250 asserts RXACTIVE when SYNC is detected (Strip SYNC state).
- The USB3250 negates RXACTIVE when an EOP is detected and the elasticity buffer is empty (Strip EOP state).
- When RXACTIVE is asserted, RXVALID will be asserted if the RX Holding Register is full.
- RXVALID will be negated if the RX Holding Register was not loaded during the previous byte time. This will occur if 8 stuffed bits have been accumulated.
- The SIE must be ready to consume a data byte if RXACTIVE and RXVALID are asserted (RX Data state).
- Figure 7.10 shows the timing relationship between the received data (DP/DM), RXVALID, RXACTIVE, RXERROR and RXDATA signals.

Note 7.1 The USB 2.0 Transceiver does NOT decode Packet ID's (PIDs). They are passed to the SIE for decoding.

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Note 7.2 Figure 7.10, Figure 7.11 and Figure 7.12 are timing examples of a HS/FS Macrocell when it is in HS mode. When a HS/FS Macrocell is in FS Mode (8-bit mode) there are approximately 40 CLK60 cycles every byte time. The Receive State Machine assumes that the SIE captures the data on the RXDATA bus if RXACTIVE and RXVALID are asserted. In FS mode, RXVALID will only be asserted for one CLK60 per byte time.

Note 7.3 Figure 7.10, Figure 7.11 and Figure 7.12 the SYNC pattern on DP/DM is shown as one byte long. The SYNC pattern received by a device can vary in length. These figures assume that all but the last 12 bits have been consumed by the hubs between the device and the host controller.

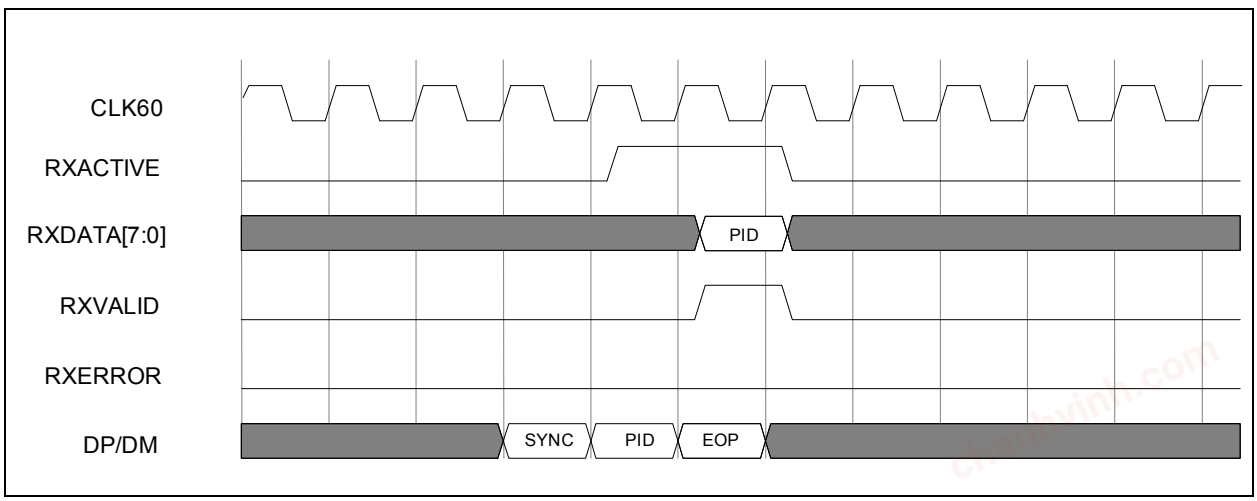


Figure 7.10 Receive Timing for Data (with CRC-16 in 8-bit mode)

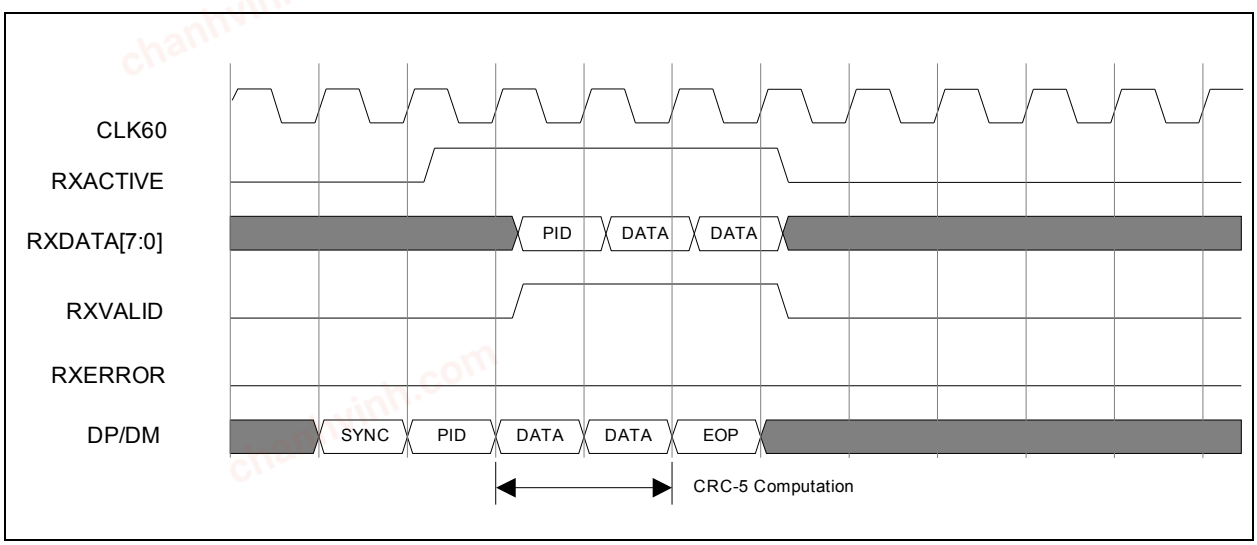


Figure 7.11 Receive Timing for Setup Packet (8-bit mode)

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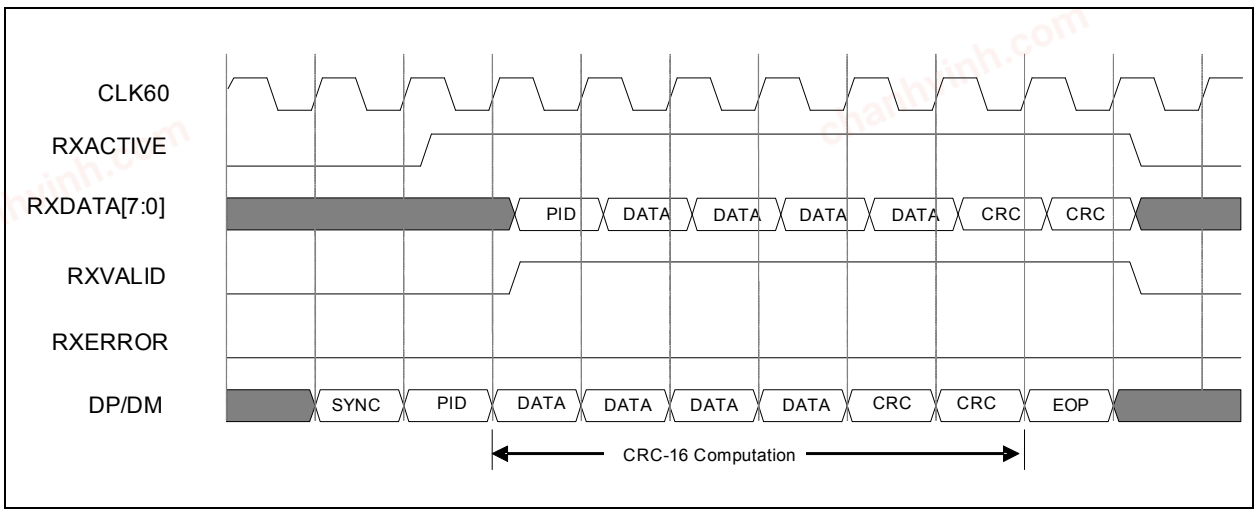


Figure 7.12 Receive Timing for Data Packet with CRC-16 (8-bit mode)

7.6 FS/HS RX

The receivers connect directly to the USB cable. The block contains a separate differential receiver for HS and FS mode. Depending on the mode, the selected receiver provides the serial data stream through the multiplexer to the RX Logic block. The FS mode section of the FS/HS RX block also consists of a single-ended receiver on each of the data lines to determine the correct FS LINESTATE. For HS mode support, the FS/HS RX block contains a squelch circuit to insure that noise is never interpreted as data.

7.7 FS/HS TX

The transmitters connect directly to the USB cable. The block contains a separate differential FS and HS transmitter which receive encoded, bitstuffed, serialized data from the TX Logic block and transmit it on the USB cable. The FS/HS TX block also contains circuitry that either enables or disables the pull-up resistor on the D+ line.

7.8 Biasing

This block consists of an internal bandgap reference circuit used for generating the driver current and the biasing of the analog circuits. This block requires an external precision resistor (12kΩ +/- 1% from the RBIAS pin to analog ground).

7.9 Power Control

This is the block that receives and distributes all the power for the transceiver. This block is also responsible for handling ESD protection.

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Chapter 8 Application Notes

The following sections consist of select functional explanations to aid in implementing the PHY into a system. For complete description and specifications consult the USB 2.0 Transceiver Macrocell Interface Specification and Universal Serial Bus Specification Revision 2.0.

8.1 Linestate

The voltage thresholds that the LINESTATE[1:0] signals use to reflect the state of DP and DM depend on the state of XCVRSELECT. LINESTATE[1:0] uses HS thresholds when the HS transceiver is enabled (XCVRSELECT = 0) and FS thresholds when the FS transceiver is enabled (XCVRSELECT = 1). There is not a concept of variable single-ended thresholds in the USB 2.0 specification for HS mode.

The HS receiver is used to detect Chirp J or K, where the output of the HS receiver is always qualified with the Squelch signal. If squelched, the output of the HS receiver is ignored. In the USB3250, as an alternative to using variable thresholds for the single-ended receivers, the following approach is used.

Table 8.1 Linestate States

	STATE OF DP/DM LINES			
LINESTATE[1:0]		**FULL SPEED XCVRSELECT =1 TERMSELECT=1**	**HIGH SPEED XCVRSELECT =0 TERMSELECT=0**	**CHIRP MODE XCVRSELECT =0 TERMSELECT=1**
LS[1]	**LS[0]**			
0	0	SE0	Squelch	Squelch
0	1	J	!Squelch	!Squelch & HS Differential Receiver Output
1	0	K	Invalid	!Squelch & !HS Differential Receiver Output
1	1	SE1	Invalid	Invalid

In HS mode, 3ms of no USB activity (IDLE state) signals a reset. The SIE monitors LINESTATE[1:0] for the IDLE state. To minimize transitions on LINESTATE[1:0] while in HS mode, the presence of !Squelch is used to force LINESTATE[1:0] to a J state.

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8.2 OPMODES

The OPMODE[1:0] pins allow control of the operating modes.

Table 8.2 Operational Modes

MODE[1:0]	STATE#	STATE NAME	DESCRIPTION
00	0	Normal Operation	Transceiver operates with normal USB data encoding and decoding
01	1	Non-Driving	Allows the transceiver logic to support a soft disconnect feature which tri-states both the HS and FS transmitters, and removes any termination from the USB making it appear to an upstream port that the device has been disconnected from the bus
10	2	Disable Bit Stuffing and NRZI encoding	Disables bitstuffing and NRZI encoding logic so that 1's loaded from the TXDATA bus become 'J's on the DP/DM and 0's become 'K's
11	3	Reserved	N/A

The OPMODE[1:0] signals are normally changed only when the transmitter and the receiver are quiescent, i.e. when entering a test mode or for a device initiated resume.

When using OPMODE[1:0] = 10 (state 2), OPMODES are set, and then 5 60MHz clocks later, TXVALID is asserted. In this case, the SYNC and EOP patterns are not transmitted.

The only exception to this is when OPMODE[1:0] is set to state 2 while TXVALID has been asserted (the transceiver is transmitting a packet), in order to flag a transmission error. In this case, the PHY has already transmitted the SYNC pattern so upon negation of TXVALID the EOP must also be transmitted to properly terminate the packet. Changing the OPMODE[1:0] signals under all other conditions, while the transceiver is transmitting or receiving data will generate undefined results.

Under no circumstances should the device controller change OPMODE while the DP/DM lines are still transmitting or unpredictable changes on DP/DM are likely to occur. The same applies for TERMSELECT and XCVRSELECT.

8.3 Test Mode Support

Table 8.3 USB 2.0 Test Mode to Macrocell Mapping

USB 2.0 TEST MODES	USB3250 SETUP		
	OPERATIONAL MODE	SIE TRANSMITTED DATA	XCVRSELECT & TERMSELECT
SE0_NAK	Normal	No transmit	HS
J	Disable	All '1's	HS
K	Disable	All '0's	HS
Test_Packet	Normal	Test Packet data	HS

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8.4 SE0 Handling

For FS operation, IDLE is a J state on the bus. SE0 is used as part of the EOP or to indicate reset. When asserted in an EOP, SE0 is never asserted for more than 2 bit times. The assertion of SE0 for more than 2.5us is interpreted as a reset by the device operating in FS mode.

For HS operation, IDLE is a SE0 state on the bus. SE0 is also used to reset a HS device. A HS device cannot use the 2.5us assertion of SE0 (as defined for FS operation) to indicate reset since the bus is often in this state between packets. If no bus activity (IDLE) is detected for more than 3ms, a HS device must determine whether the downstream facing port is signaling a suspend or a reset. The following section details how this determination is made. If a reset is signaled, the HS device will then initiate the HS Detection Handshake protocol.

8.5 Reset Detection

If a device in HS mode detects bus inactivity for more than 3ms (T1), it reverts to FS mode. This enables the FS pull-up on the DP line in an attempt to assert a continuous FS J state on the bus. The SIE must then check LINESTATE for the SE0 condition. If SE0 is asserted at time T2, then the upstream port is forcing the reset state to the device (i.e., a Driven SE0). The device will then initiate the HS detection handshake protocol.

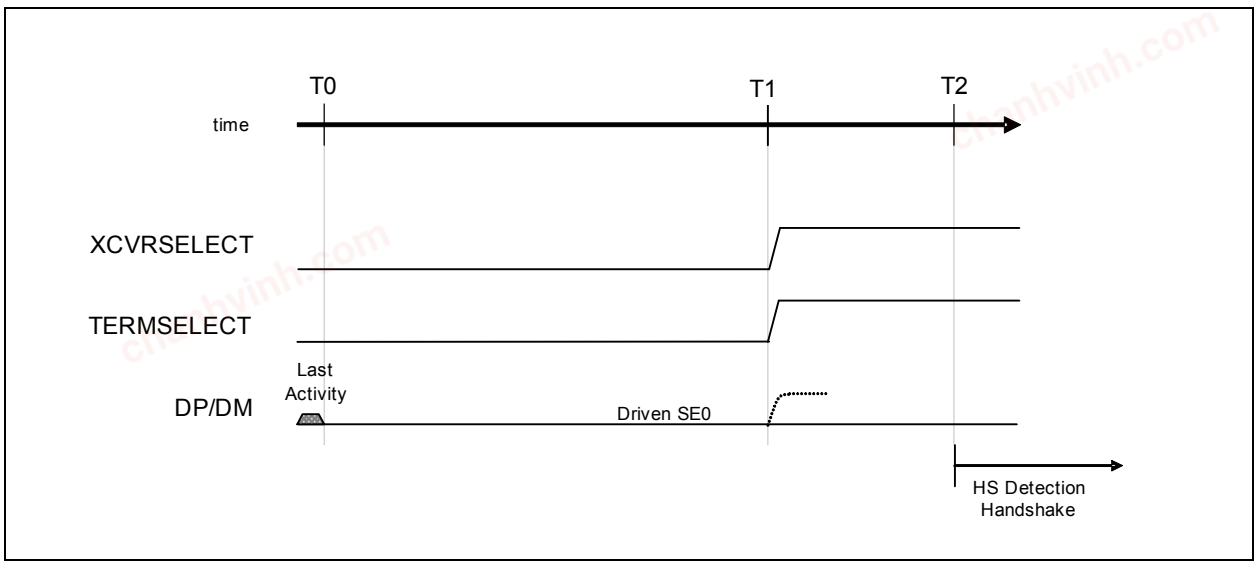


Figure 8.1 Reset Timing Behavior (HS Mode)

Table 8.4 Reset Timing Values (HS Mode)

TIMING PARAMETER	DESCRIPTION	VALUE
HS Reset T0	Bus activity ceases, signaling either a reset or a SUSPEND.	0 (reference)
T1	Earliest time at which the device may place itself in FS mode after bus activity stops.	HS Reset T0 + 3. 0ms < T1 < HS Reset T0 + 3.125ms
T2	SIE samples LINESTATE. If LINESTATE = SE0, then the SE0 on the bus is due to a Reset state. The device now enters the HS Detection Handshake protocol.	T1 + 100µs < T2 < T1 + 875µs

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8.6 Suspend Detection

If a HS device detects SE0 asserted on the bus for more than 3ms (T1), it reverts to FS mode. This enables the FS pull-up on the DP line in an attempt to assert a continuous FS J state on the bus. The SIE must then check LINESTATE for the J condition. If J is asserted at time T2, then the upstream port is asserting a soft SE0 and the USB is in a J state indicating a suspend condition. By time T4 the device must be fully suspended.

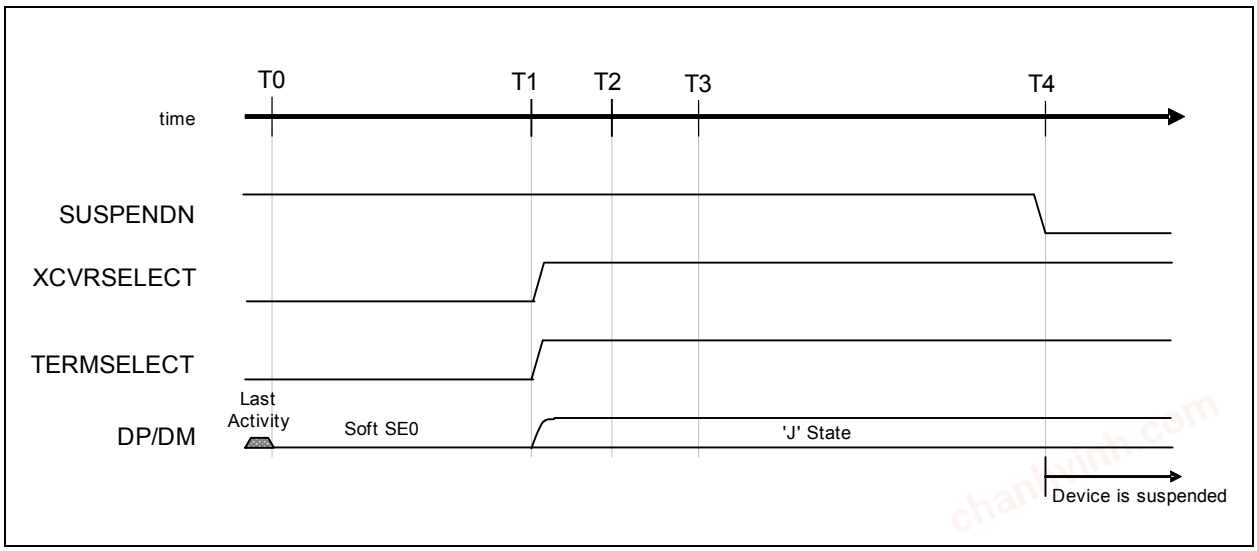


Figure 8.2 Suspend Timing Behavior (HS Mode)

Table 8.5 Suspend Timing Values (HS Mode)

TIMING PARAMETER	DESCRIPTION	VALUE
HS Reset T0	End of last bus activity, signaling either a reset or a SUSPEND.	0 (reference)
T1	The time at which the device must place itself in FS mode after bus activity stops.	HS Reset T0 + 3. 0ms < T1 < HS Reset T0 + 3.125ms
T2	SIE samples LINESTATE. If LINESTATE = 'J', then the initial SE0 on the bus (T0 - T1) had been due to a Suspend state and the SIE remains in HS mode.	T1 + 100 µs < T2 < T1 + 875µs
T3	The earliest time where a device can issue Resume signaling.	HS Reset T0 + 5ms
T4	The latest time that a device must actually be suspended, drawing no more than the suspend current from the bus.	HS Reset T0 + 10ms

8.7 HS Detection Handshake

The High Speed Detection Handshake process is entered from one of three states: suspend, active FS or active HS. The downstream facing port asserting an SE0 state on the bus initiates the HS Detection Handshake. Depending on the initial state, an SE0 condition can be asserted from 0 to 4 ms before initiating the HS Detection Handshake. These states are described in the USB 2.0 specification.

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There are three ways in which a device may enter the HS Handshake Detection process:

1. If the device is suspended and it detects an SE0 state on the bus it may immediately enter the HS handshake detection process.
2. If the device is in FS mode and an SE0 state is detected for more than 2.5µs. it may enter the HS handshake detection process.
3. If the device is in HS mode and an SE0 state is detected for more than 3.0ms. it may enter the HS handshake detection process. In HS mode, a device must first determine whether the SE0 state is signaling a suspend or a reset condition. To do this the device reverts to FS mode by placing XCVRSELECT and TERMSELECT into FS mode. The device must not wait more than 3.125ms before the reversion to FS mode. After reverting to FS mode, no less than 100µs and no more than 875µs later the SIE must check the LINESTATE signals. If a J state is detected the device will enter a suspend state. If an SE0 state is detected, then the device will enter the HS Handshake detection process.

In each case, the assertion of the SE0 state on the bus initiates the reset. The minimum reset interval is 10ms. Depending on the previous mode that the bus was in, the delay between the initial assertion of the SE0 state and entering the HS Handshake detection can be from 0 to 4ms.

This transceiver design pushes as much of the responsibility for timing events on to the SIE as possible, and the SIE requires a stable CLKOUT signal to perform accurate timing. In case 2 and 3 above, CLKOUT has been running and is stable, however in case 1 the PHY is reset from a suspend state, and the internal oscillator and clocks of the transceiver are assumed to be powered down. A device has up to 6ms after the release of SUSPENDN to assert a minimum of a 1ms Chirp K.

8.8 HS Detection Handshake - FS Downstream Facing Port

Upon entering the HS Detection process (T0) XCVRSELECT and TERMSELECT are in FS mode. The DP pull-up is asserted and the HS terminations are disabled. The SIE then sets OPMODE to Disable Bit Stuffing and NRZI encoding, XCVRSELECT to HS mode, and begins the transmission of all 0's data, which asserts a HS K (chirp) on the bus (T1). The device chirp must last at least 1.0ms, and must end no later than 7.0ms after HS Reset T0. At time T1 the device begins listening for a chirp sequence from the host port.

If the downstream facing port is not HS capable, then the HS K asserted by the device is ignored and the alternating sequence of HS Chirp K's and J's is not generated. If no chirps are detected (T4) by the device, it will enter FS mode by returning XCVRSELECT to FS mode.

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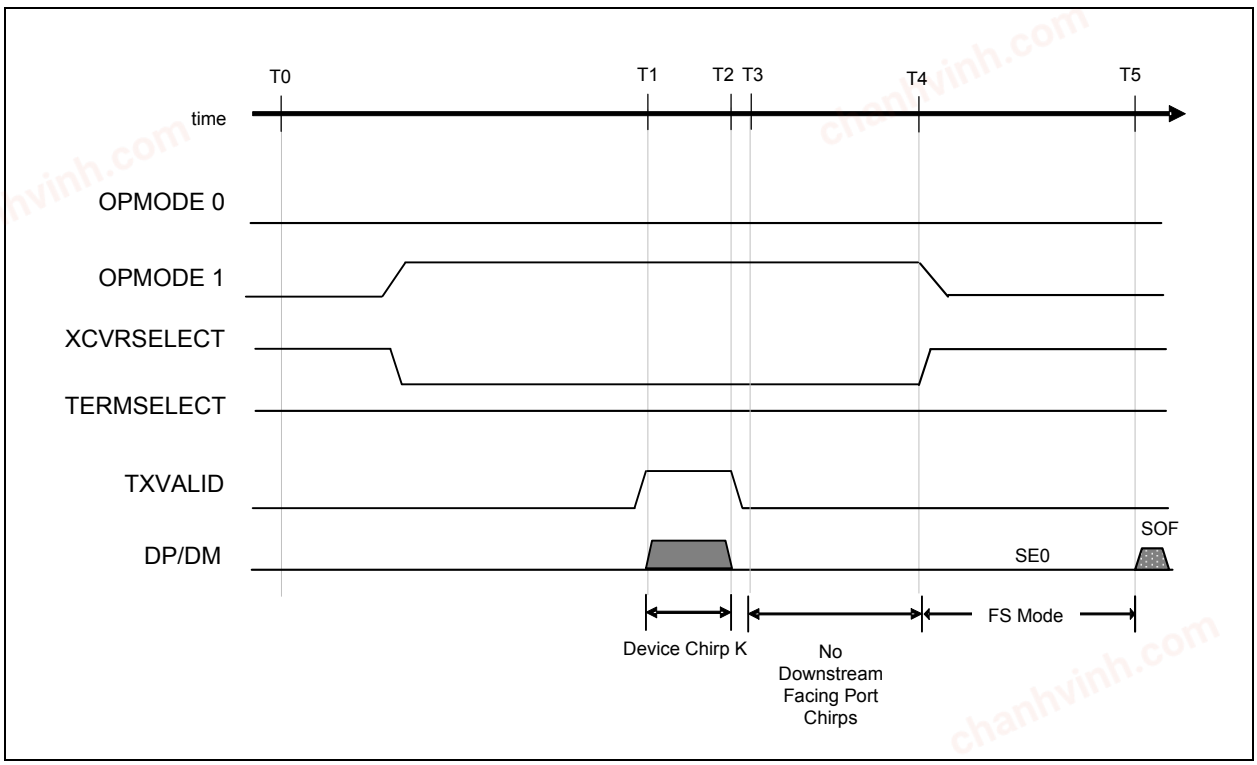


Figure 8.3 HS Detection Handshake Timing Behavior (FS Mode)

Table 8.6 HS Detection Handshake Timing Values (FS Mode)

TIMING PARAMETER	DESCRIPTION	VALUE
T0	HS Handshake begins. DP pull-up enabled, HS terminations disabled. The XCVRSELECT and OPMODE inputs are then set for HS with bitstuffing disabled, and TXVALID is asserted at least 5 60MHz clocks later.	0 (reference)
T1	Device enables HS Transceiver and asserts Chirp K on the bus.	T0 < T1 < HS Reset T0 + 6.0ms
T2	Device removes Chirp K from the bus. 1ms minimum width.	T1 + 1.0 ms < T2 < HS Reset T0 + 7.0ms
T3	Earliest time when downstream facing port may assert Chirp KJ sequence on the bus.	T2 < T3 < T2+100µs
T4	Chirp not detected by the device. Device reverts to FS default state and waits for end of reset.	T2 + 1.0ms < T4 < T2 + 2.5ms
T5	Earliest time at which host port may end reset	HS Reset T0 + 10ms

Note 8.1 T0 may occur to 4ms after HS Reset T0.

Note 8.2 The SIE must assert the Chirp K for 66000 CLK60 cycles to ensure a 1ms minimum duration.

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8.9 HS Detection Handshake - HS Downstream Facing Port

Upon entering the HS Detection process (T0) XCVRSELECT and TERMSELECT are in FS mode. The DP pull-up is asserted and the HS terminations are disabled. The SIE then sets OPMODE to Disable Bit Stuffing and NRZI encoding, XCVRSELECT to HS mode, and begins the transmission of all 0's data, which asserts a HS K (chirp) on the bus (T1). The device chirp must last at least 1.0ms, and must end no later than 7.0ms after HS Reset T0. At time T1 the device begins listening for a chirp sequence from the downstream facing port. If the downstream facing port is HS capable then it will begin generating an alternating sequence of Chirp K's and Chirp J's (T3) after the termination of the chirp from the device (T2). After the device sees the valid chirp sequence Chirp K-J-K-J-K-J (T6), it will enter HS mode by setting TERMSELECT to HS mode (T7).

Figure 8.4 provides a state diagram for Chirp K-J-K-J-K-J validation. Prior to the end of reset (T9) the device port must terminate the sequence of Chirp K's and Chirp J's (T8) and assert SE0 (T8-T9). Note that the sequence of Chirp K's and Chirp J's constitutes bus activity.

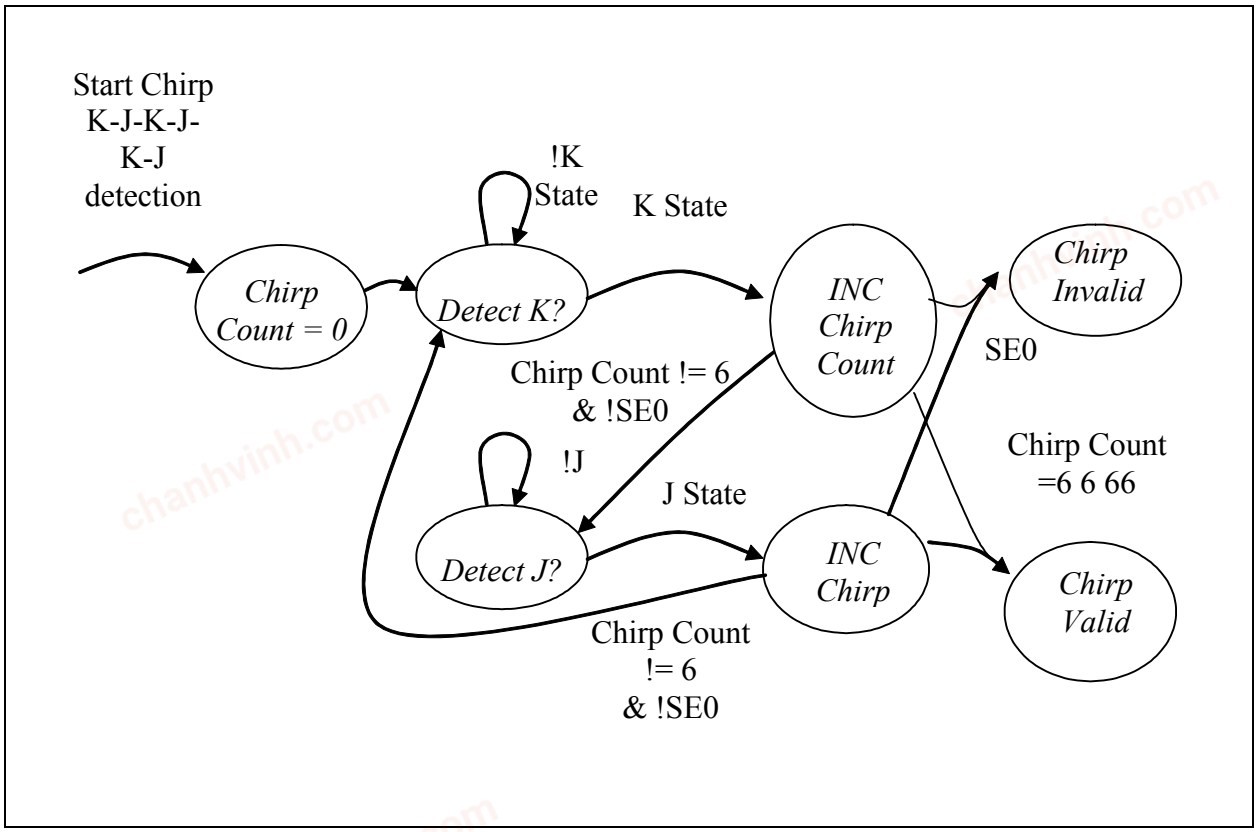


Figure 8.4 Chirp K-J-K-J-K-J Sequence Detection State Diagram

The Chirp K-J-K-J-K-J sequence occurs too slow to propagate through the serial data path, therefore LINESTATE signal transitions must be used by the SIE to step through the Chirp K-J-K-J-K-J state diagram, where "K State" is equivalent to LINESTATE = K State and "J State" is equivalent to LINESTATE = J State. The SIE must employ a counter (Chirp Count) to count the number of Chirp K and Chirp J states. Note that LINESTATE does not filter the bus signals so the requirement that a bus state must be "continuously asserted for 2.5µs" must be verified by the SIE sampling the LINESTATE signals.

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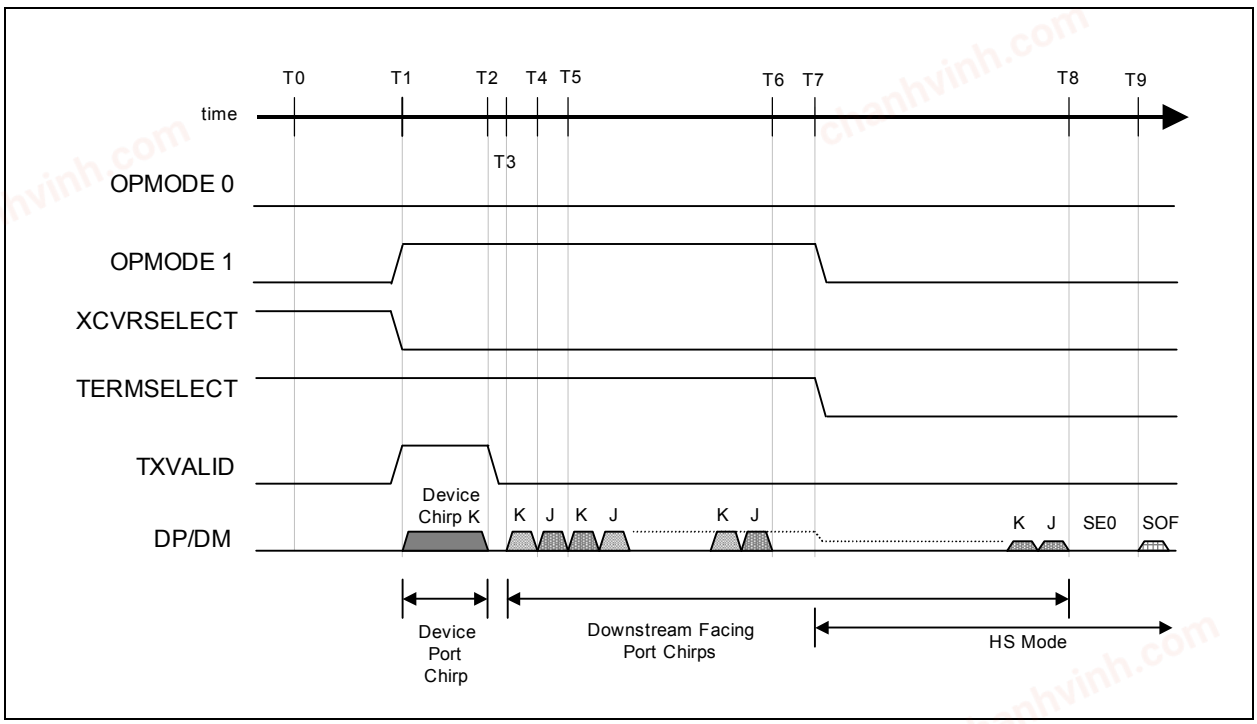


Figure 8.5 HS Detection Handshake Timing Behavior (HS Mode)

Table 8.7 Reset Timing Values

TIMING PARAMETER	DESCRIPTION	VALUE
T0	HS Handshake begins. DP pull-up enabled, HS terminations disabled.	0 (reference)
T1	Device asserts Chirp K on the bus.	T0 < T1 < HS Reset T0 + 6.0ms
T2	Device removes Chirp K from the bus. 1 ms minimum width.	T0 + 1.0ms < T2 < HS Reset T0 + 7.0ms
T3	Downstream facing port asserts Chirp K on the bus.	T2 < T3 < T2+100µs
T4	Downstream facing port toggles Chirp K to Chirp J on the bus.	T3 + 40µs < T4 < T3 + 60µs
T5	Downstream facing port toggles Chirp J to Chirp K on the bus.	T4 + 40µs < T5 < T4 + 60µs
T6	Device detects downstream port chirp.	T6
T7	Chirp detected by the device. Device removes DP pull-up and asserts HS terminations, reverts to HS default state and waits for end of reset.	T6 < T7 < T6 + 500µs
T8	Terminate host port Chirp K-J sequence (Repeating T4 and T5)	T9 - 500µs < T8 < T9 - 100µs

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Table 8.7 Reset Timing Values (continued)

TIMING PARAMETER	DESCRIPTION	VALUE
T9	The earliest time at which host port may end reset. The latest time, at which the device may remove the DP pull-up and assert the HS terminations, reverts to HS default state.	HS Reset T0 + 10ms

Note 8.3 T0 may be up to 4ms after HS Reset T0.

Note 8.4 The SIE must use LINESTATE to detect the downstream port chirp sequence.

Note 8.5 Due to the assertion of the HS termination on the host port and FS termination on the device port, between T1 and T7 the signaling levels on the bus are higher than HS signaling levels and are less than FS signaling levels.

8.10 HS Detection Handshake - Suspend Timing

If reset is entered from a suspended state, the internal oscillator and clocks of the transceiver are assumed to be powered down. Figure 8.6 shows how CLK60 is used to control the duration of the chirp generated by the device.

When reset is entered from a suspended state (J to SE0 transition reported by LINESTATE), SUSPENDN is combinatorially negated at time T0 by the SIE. It takes approximately 5 milliseconds for the transceiver's oscillator to stabilize. The device does not generate any transitions of the CLK60 signal until it is "usable" (where "usable" is defined as stable to within ±10% of the nominal frequency and the duty cycle accuracy 50±5%).

The first transition of CLK60 occurs at T1. The SIE then sets OPMODE to Disable Bit Stuffing and NRZI encoding, XCVRSELECT to HS mode, and must assert a Chirp K for 66000 CLK60 cycles to ensure a 1ms minimum duration. If CLK60 is 10% fast (66MHz) then Chirp K will be 1.0ms. If CLK60 is 10% slow (54 MHz) then Chirp K will be 1.2ms. The 5.6ms requirement for the first CLK60 transition after SUSPENDN, ensures enough time to assert a 1ms Chirp K and still complete before T3. Once the Chirp K is completed (T3) the SIE can begin looking for host chirps and use CLK60 to time the process. At this time, the device follows the same protocol as in section 8.9 for completion of the High Speed Handshake.

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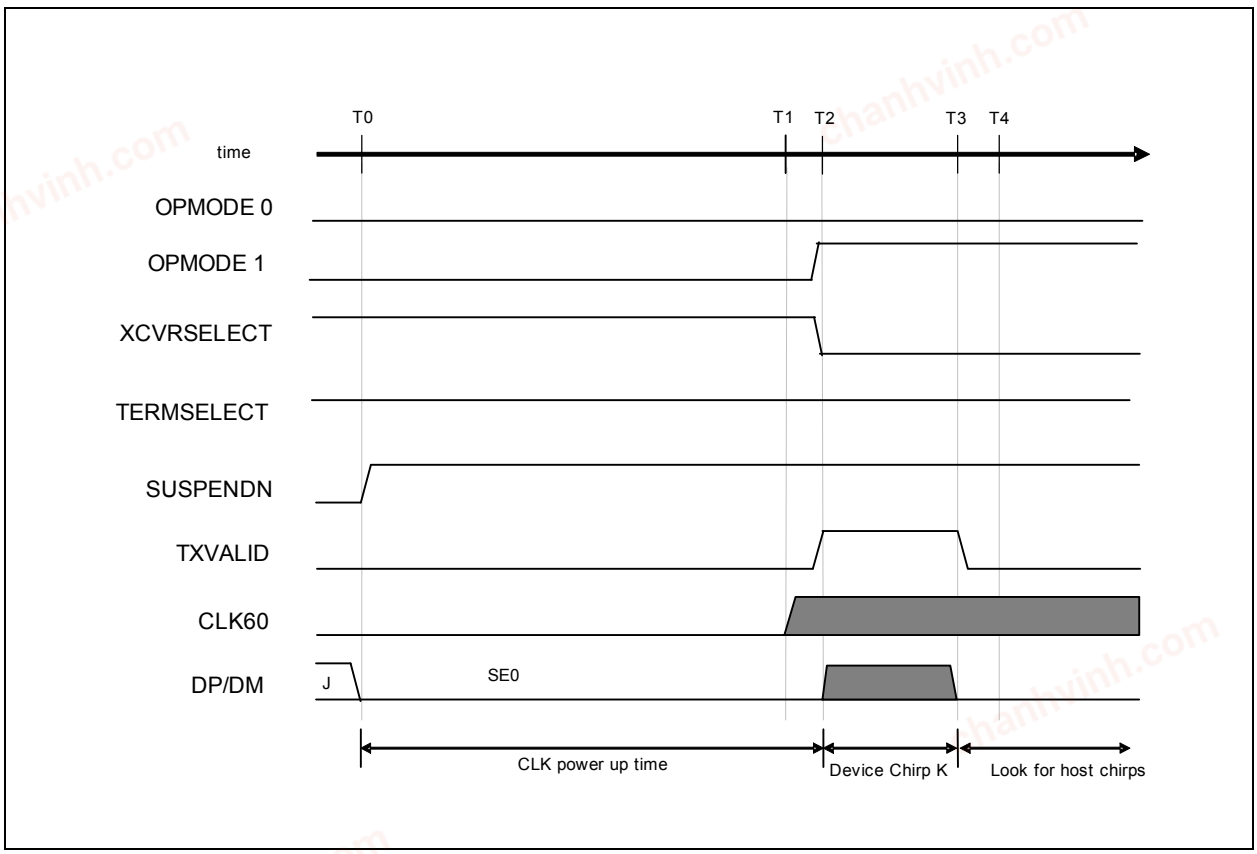


Figure 8.6 HS Detection Handshake Timing Behavior from Suspend

To detect the assertion of the downstream Chirp K's and Chirp J's for 2.5us {TFILT}, the SIE must see the appropriate LINESTATE signals asserted continuously for 165 CLK60 cycles.

Table 8.8 HS Detection Handshake Timing Values from Suspend

TIMING PARAMETER	DESCRIPTION	VALUE
T0	While in suspend state an SE0 is detected on the USB. HS Handshake begins. D+ pull-up enabled, HS terminations disabled, SUSPENDN negated.	0 (HS Reset T0)
T1	First transition of CLKOUT. CLKOUT "Usable" (frequency accurate to ±10%, duty cycle accurate to 50±5).	T0 < T1 < T0 + 5.6ms
T2	Device asserts Chirp K on the bus.	T1 < T2 < T0 + 5.8ms
T3	Device removes Chirp K from the bus. (1 ms minimum width) and begins looking for host chirps.	T2 + 1.0 ms < T3 < T0 + 7.0 ms
T4	CLK "Nominal" (CLKOUT is frequency accurate to ±500 ppm, duty cycle accurate to 50±5).	T1 < T3 < T0 + 20.0ms

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8.11 Assertion of Resume

In this case, an event internal to the device initiates the resume process. A device with remote wake-up capability must wait for at least 5ms after the bus is in the idle state before sending the remote wake-up resume signaling. This allows the hubs to get into their suspend state and prepare for propagating resume signaling.

The device has 10ms where it can draw a non-suspend current before it must drive resume signaling. At the beginning of this period the SIE may negate SUSPENDN, allowing the transceiver (and its oscillator) to power up and stabilize.

Figure 8.7 illustrates the behavior of a device returning to HS mode after being suspended. At T4, a device that was previously in FS mode would maintain TERMSELECT and XCVRSELECT high.

To generate resume signaling (FS 'K') the device is placed in the "Disable Bit Stuffing and NRZI encoding" Operational Mode (OPMODE [1:0] = 10), TERMSELECT and XCVRSELECT must be in FS mode, TXVALID asserted, and all 0's data is presented on the TXDATA bus for at least 1ms (T1 - T2).

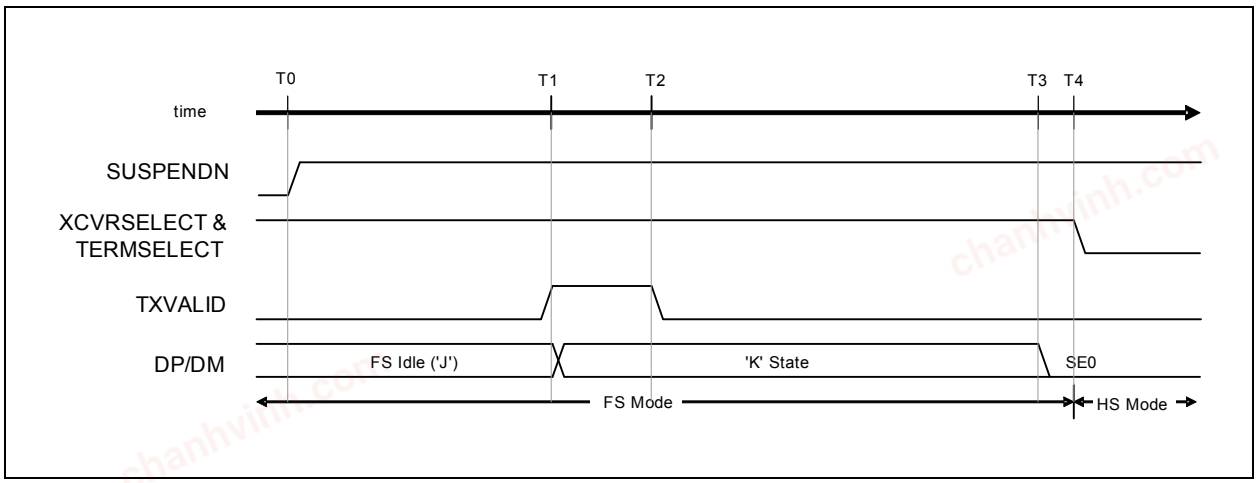


Figure 8.7 Resume Timing Behavior (HS Mode)

Table 8.9 Resume Timing Values (HS Mode)

TIMING PARAMETER	DESCRIPTION	VALUE
T0	Internal device event initiating the resume process	0 (reference)
T1	Device asserts FS 'K' on the bus to signal resume request to downstream port	T0 < T1 < T0 + 10ms.
T2	The device releases FS 'K' on the bus. However by this time the 'K' state is held by downstream port.	T1 + 1.0ms < T2 < T1 + 15ms
T3	Downstream port asserts SE0.	T1 + 20ms
T4	Latest time at which a device, which was previously in HS mode, must restore HS mode after bus activity stops.	T3 + 1.33µs {2 Low-speed bit times}

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8.12 Detection of Resume

Resume signaling always takes place in FS mode (TERMSELECT and XCVRSELECT = FS enabled), so the behavior for a HS device is identical to that if a FS device. The SIE uses the LINESTATE signals to determine when the USB transitions from the 'J' to the 'K' state and finally to the terminating FS EOP (SE0 for 1.25us-1.5µs.).

The resume signaling (FS 'K') will be asserted for at least 20ms. At the beginning of this period the SIE may negate SUSPENDN, allowing the transceiver (and its oscillator) to power up and stabilize.

The FS EOP condition is relatively short. SIEs that simply look for an SE0 condition to exit suspend mode do not necessarily give the transceiver's clock generator enough time to stabilize. It is recommended that all SIE implementations key off the 'J' to 'K' transition for exiting suspend mode (SUSPENDN = 1). And within 1.25µs after the transition to the SE0 state (low-speed EOP) the SIE must enable normal operation, i.e. enter HS or FS mode depending on the mode the device was in when it was suspended.

If the device was in FS mode: then the SIE leaves the FS terminations enabled. After the SE0 expires, the downstream port will assert a J state for one low-speed bit time, and the bus will enter a FS Idle state (maintained by the FS terminations).

If the device was in HS mode: then the SIE must switch to the FS terminations before the SE0 expires (< 1.25µs). After the SE0 expires, the bus will then enter a HS IDLE state (maintained by the HS terminations).

8.13 HS Device Attach

Figure 8.8 demonstrates the timing of the PHY control signals during a device attach event. When a HS device is attached to an upstream port, power is asserted to the device and the device sets XCVRSELECT and TERMSELECT to FS mode (time T1).

V_{BUS} is the +5V power available on the USB cable. Device Reset in Figure 8.8 indicates that VBUS is within normal operational range as defined in the USB 2.0 specification. The assertion of Device Reset (T0) by the upstream port will initialize the device. By monitoring LINESTATE, the SIE state machine knows to set the XCVRSELECT and TERMSELECT signals to FS mode (T1).

The standard FS technique of using a pull-up resistor on DP to signal the attach of a FS device is employed. The SIE must then check the LINESTATE signals for SE0. If LINESTATE = SE0 is asserted at time T2 then the upstream port is forcing the reset state to the device (i.e. Driven SE0). The device will then reset itself before initiating the HS Detection Handshake protocol.

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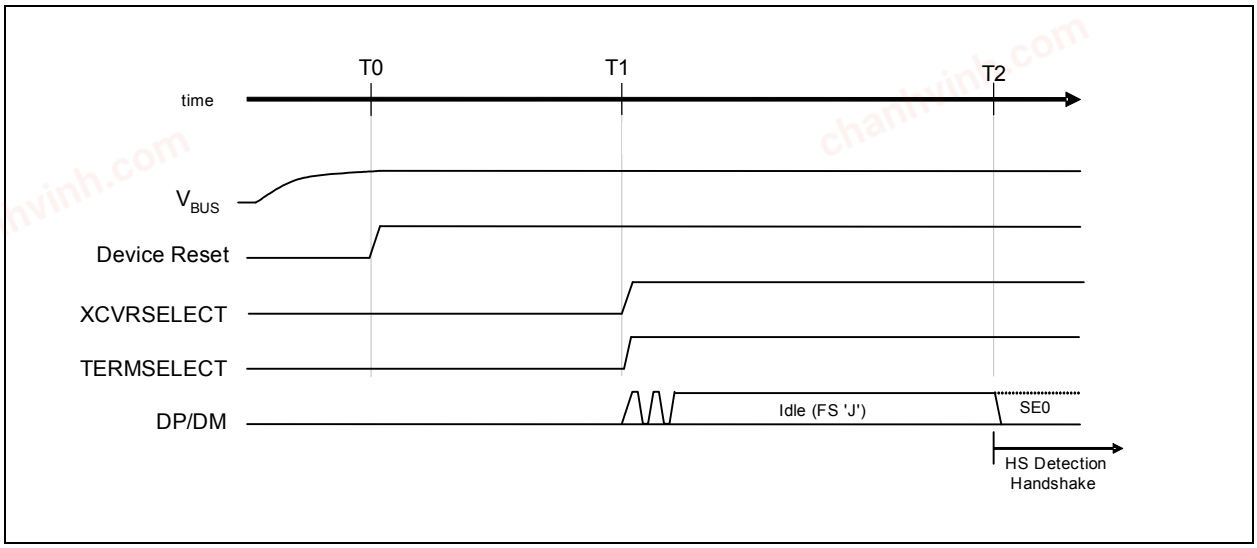


Figure 8.8 Device Attach Behavior

Table 8.10 Attach and Reset Timing Values

TIMING PARAMETER	DESCRIPTION	VALUE
T0	Vbus Valid.	0 (reference)
T1	Maximum time from Vbus valid to when the device must signal attach.	T0 + 100ms < T1
T2 (HS Reset T0)	Debounce interval. The device now enters the HS Detection Handshake protocol.	T1 + 100ms < T2

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8.14 Application Diagrams

The bypass capacitors shown Figure 8.9 for the voltage regulator are typical values. The actual values will be dictated by the regulator used in the end application. Please refer to the layout application note for recommendations regarding critical component placement.

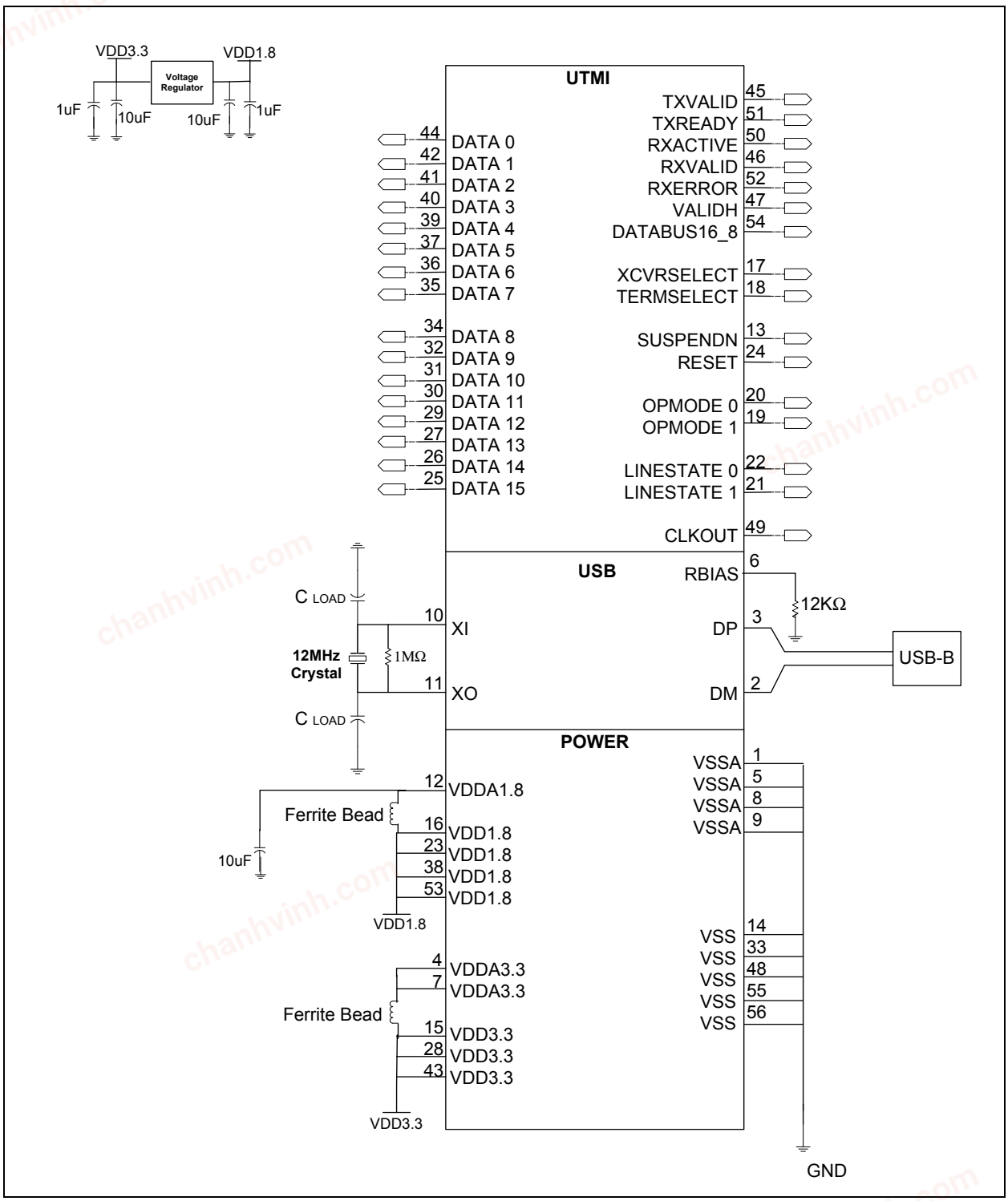
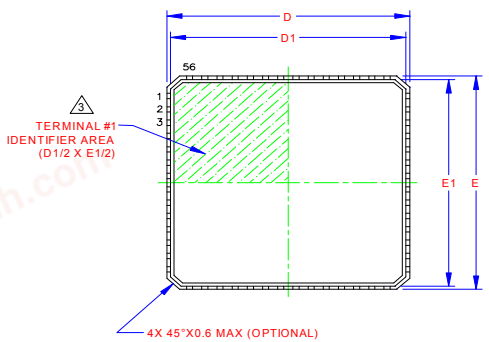


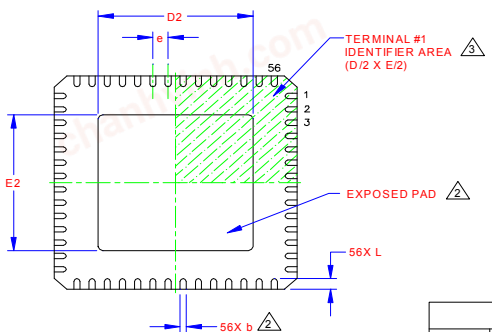
Figure 8.9 Application Diagram for 56-pin QFN Package

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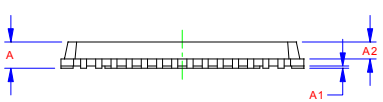
Chapter 9 Package Outline



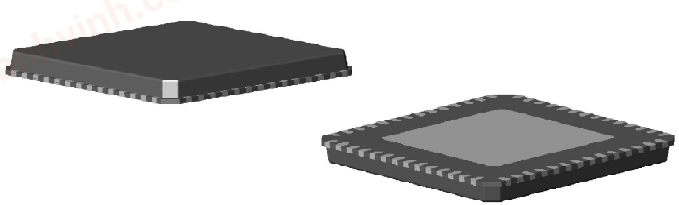
TOP VIEW



BOTTOM VIEW



SIDE VIEW



3-D VIEWS

REVISION HISTORY			
REVISION	DESCRIPTION	DATE	RELEASED BY
A	INITIAL RELEASE	2/07/04	S.K.ILIEV
B	REMOVE "PRELIMINARY" NOTE	10/7/04	S.K.ILIEV
C	L(MAX) FROM 0.55 TO 0.50. ADDED D2/E2 VARIATIONS TABLE	7/2/05	S.K.ILIEV

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.70	–	1.00	–	OVERALL PKG HEIGHT
A1	0	0.02	0.05	–	STANDOFF
A2	–	–	0.90	–	MOLD THICKNESS
D/E	7.85	8.00	8.15	–	"X"/"Y" BODY SIZE
D1/E1	7.55	–	7.95	–	"X"/"Y" MOLD SIZE
D2/E2	SEE VARIATIONS			–	"X"/"Y" EXPOSED PAD SIZE
L	0.30	–	0.50	–	TERMINAL LENGTH
b	0.18	0.25	0.30	2	TERMINAL WIDTH
e	0.50 BSC			–	TERMINAL PITCH

D2 / E2 VARIATIONS				
MIN	NOM	MAX	NOTE	CATALOG PART
4.15	4.30	4.45	–	USB3250, USB3500 & EMC2700

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETER.
2. POSITION TOLERANCE OF EACH TERMINAL AND EXPOSED PAD IS ± 0.05mm AT MAXIMUM MATERIAL CONDITION. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS AND TOLERANCES ARE:
DECIMAL X.X ±0.1, X.XX ±0.05, X.XXX ±0.025 ANGULAR ±1°
DIM AND TOL PER ASME Y14.5M - 1994
MATERIAL -
FINISH -
PRINT WITH "SCALE TO FIT" DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

	NAME	DATE
DRAWN	S.K.ILIEV	2/06/04
CHECKED	S.K.ILIEV	2/07/04
APPROVED	S.K.ILIEV	2/07/04

80 ARKAY DRIVE
HAUPPAUGE, NY 11788
USA

SMSC SUCCESS BY DESIGN

TITLE: PACKAGE OUTLINE
56 TERMINAL QFN, 8x8mm BODY, 0.5mm PITCH

DWG NUMBER: MO-56-QFN-8x8 REV: C
SCALE: 1:1 STD COMPLIANCE: JEDEC: MO-220 SHEET: 1 OF 1