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USB224x

Ultra Fast USB 2.0 Multi-Format, SD/MMC, and MS Flash Media Controllers

PRODUCT FEATURES

Datasheet

General Description

The SMSC USB224x is a USB 2.0 compliant, Hi-Speed bulk only[1] mass storage class peripheral controller intended for reading and writing to popular flash media from the xD-Picture Card™ (xD)[2], Memory Stick® (MS), Secure Digital (SD), and MultiMediaCard™ (MMC) families.

The SMSC USB224x is a fully integrated, single chip solution capable of ultra high performance operation. Average sustained transfer rates exceeding 35 MB/s are possible if the media and host can support those rates. The USB2244/44i includes provisions to read/write secure media formats.

General Features

- Low pin count 36-pin QFN (6x6 mm) lead-free RoHS compliant package
- USB2240/40i/41/41i
  - Targeted for applications in which single or "combo" media sockets are used
- Hardware-controlled data flow architecture for all self-mapped media
- Pipelined hardware support for access to non-self-mapped media
- Order number with “i” denote the products that support the industrial temperature range of -40ºC to 85ºC
- Support included for secure media format on a licensed, customized basis
  - USB2244/44i: SD Secure
  - USB2242/42i: Sony MagicGate™

Hardware Features

- Single chip flash media controller with
  - USB2240/40i/41/4i: multiplexed interface for use with “combo” card sockets
  - USB2242/42i: MS flash media reader/writer
  - USB2244/44i: SD/MMC flash media reader/writer
- SDIO and MMC Streaming Mode support
- Extended configuration options
  - xD player mode operation
  - Socket switch polarities, etc.
- Media Activity LED
- GPIO configuration and polarity
  - Up to 8 GPIOs for special function use
  - One GPIO with up to 200 mA drive
- On board 24 MHz crystal driver circuit
- Optional external 24 MHz clock input[3]
- Internal card power FET
  - 200 mA
  - "Fold-back" short circuit protection
- 8051 8-bit microprocessor
  - 60 MHz - single cycle execution
  - 64 KB ROM | 14 KB RAM
- Supports a single external 3.3 V supply source; internal regulators provide 1.8 V internal core voltage for additional bill of materials and power savings
- Optimized pinout improves signal routing which eases implementation for improved signal integrity

Flash Media Specification Compliance

- Secure Digital 2.0
  - HS-SD, SDHC
  - TransFlash™ and reduced form factor media
- MultiMediaCard 4.2
  - 1/4/8-bit MMC
- Memory Stick Formats
  - MS 1.43, Pro 1.02, Duo 1.10
  - Pro-HG Duo 1.01
    - MS, MS Duo, HS-MS, MS Pro-HG, MS Pro
- xD-Picture Card 1.2

Software Features

- Customizable vendor specific data
- Optimized for low latency interrupt handling
- Reduced memory footprint

Applications

- Flash media card reader/writers
- Desktop and mobile PCs
- Printers
- Consumer A/V and media players/viewers
- Compatible with
  - Microsoft® Vista™ and Vista ReadyBoost™
  - Windows® XP, ME, 2K SP4
  - Apple Mac OSx®
  - Linux Mass Storage Class Drivers

1.Bulk only is not applicable to USB2240/40i/41/41i.
2.xD-Picture Card is not applicable to USB2241/41i.

3.Only applicable to USB2240/40i/41/41i.

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Order Numbers:

ORDER NUMBERS	LEAD-FREE ROHS COMPLIANT PACKAGE TYPE / SIZE	SD/MMC	xD	MS/ MS PRO/ MS PRO-HG	OPERATING TEMPERATURE
USB2240-AEZG-XX	36 QFN 6 x 6 x 0.5 mm	✓	✓	✓	0ºC to 70ºC
USB2240i-AEZG-XX		✓	✓	✓	-40ºC to 85ºC
USB2241-AEZG-XX		✓		✓	0ºC to 70ºC
USB2241i-AEZG-XX		✓		✓	-40ºC to 85ºC
USB2242-AEZG-XX				✓	0ºC to 70ºC
USB2242i-AEZG-XX				✓	-40ºC to 85ºC
USB2244-AEZG-XX		✓			0ºC to 70ºC
USB2244i-AEZG-XX		✓			-40ºC to 85ºC

“XX” in the order number indicates the internal ROM firmware revision level.
Please contact your SMSC sales representative for more information.

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.

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Chapter 1 Overview

The SMSC USB224x is a flash media card reader solution fully compliant with the USB 2.0 specification. All required resistors on the USB ports are integrated into the device. This includes all series termination resistors on D+ and D– pins and all required pull-down and pull-up resistors. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

Hardware Features

- Single chip flash media controller in low pin count 36-pin QFN, lead-free RoHS compliant package
- Commercial temperature products support 0°C to +70°C: USB2240/41, USB2242 and USB2244
- Industrial temperature products support -40°C to +85°C: USB2240i/41i, USB2242i and USB2244i
- Up to 8 GPIOs
  - Configuration and polarity for special function use such as LED indicators, button inputs, and power control to memory devices
  - The number of actual GPIOs depends on the implementation configuration used
- One GPIO available with up to 200 mA drive and “fold-back” short circuit protection
- 8051 8-bit microprocessor
  - 60 MHz - single cycle execution
  - 64 KB ROM |14 KB RAM
- Supports a single external 3.3 V supply source; internal regulators provide 1.8 V internal core voltage for additional bill of materials and power savings

Compliance with the following flash media card specifications:

- Secure Digital 2.0
  - HS-SD and SDHC
  - TransFlash™ and reduced form factor media
- MultiMediaCard 4.2
  - 1/4/8 bit MMC
- Memory Stick 1.43
- Memory Stick Pro Format 1.02
- Memory Stick Pro-HG Duo Format 1.01
  - Memory Stick, MS Duo, HS-MS, MS Pro-HG, MS Pro
- Memory Stick Duo 1.10
- xD-Picture Card 1.2

Software Features

- If the OEM is using an external EEPROM, the following features are available:
  - Customizable vendor, product, language, and device ID’s
  - 12-hex digits maximum for the serial number string
  - 28-character manufacturer ID and product strings for the flash media reader/writer
  - LED blink interval or duration

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Chapter 2 Acronyms

ATA: Advanced Technology Attachment

FET: Field Effect Transistor

LUN: Logical Unit Number

MMC: MultiMediaCard[1]

MSC: Memory Stick Controller[2]

PLL: Phase-Locked Loop

QFN: Quad Flat No leads

RoHS: Restriction of Hazardous Substances Directive

RXD: Received eXchange Data

SDIO: Secure Digital Input/Output

SDC: Secure Digital Controller

SIE: Serial Interface Engine

TXD: Transmit eXchange Data

UART: Universal Asynchronous Receiver-Transmitter

UCHAR: Unsigned Character

UINT: Unsigned Integer

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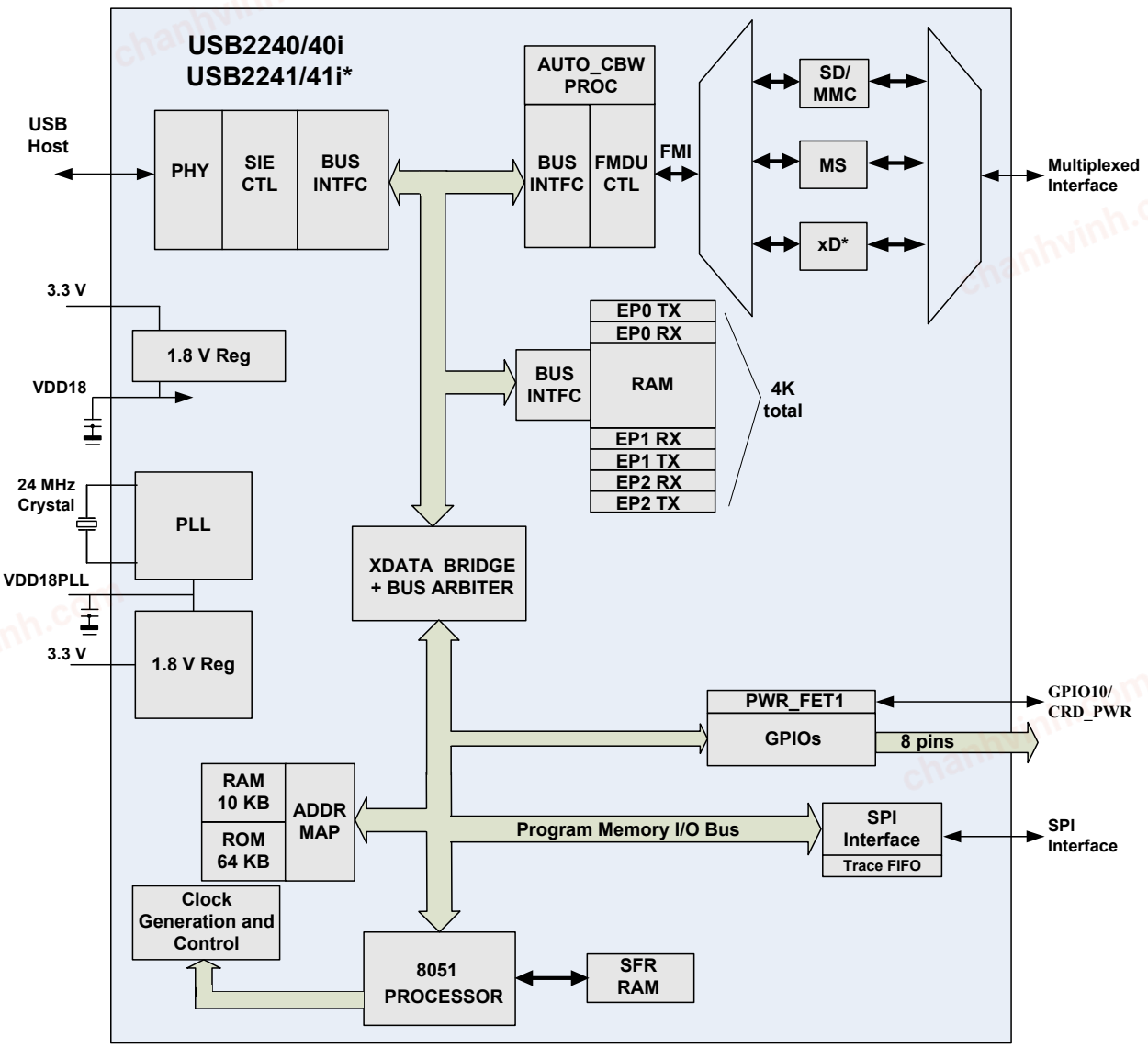
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1.MMC, SDIO, and SDC are not applicable to USB2242/42i.
2.Not applicable to USB2244/44i.

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Chapter 3 Block Diagrams



NOTE: xD-Picture Card is not applicable to USB2241/41i.

Figure 3.1 USB2240/40i/41/41i Block Diagram

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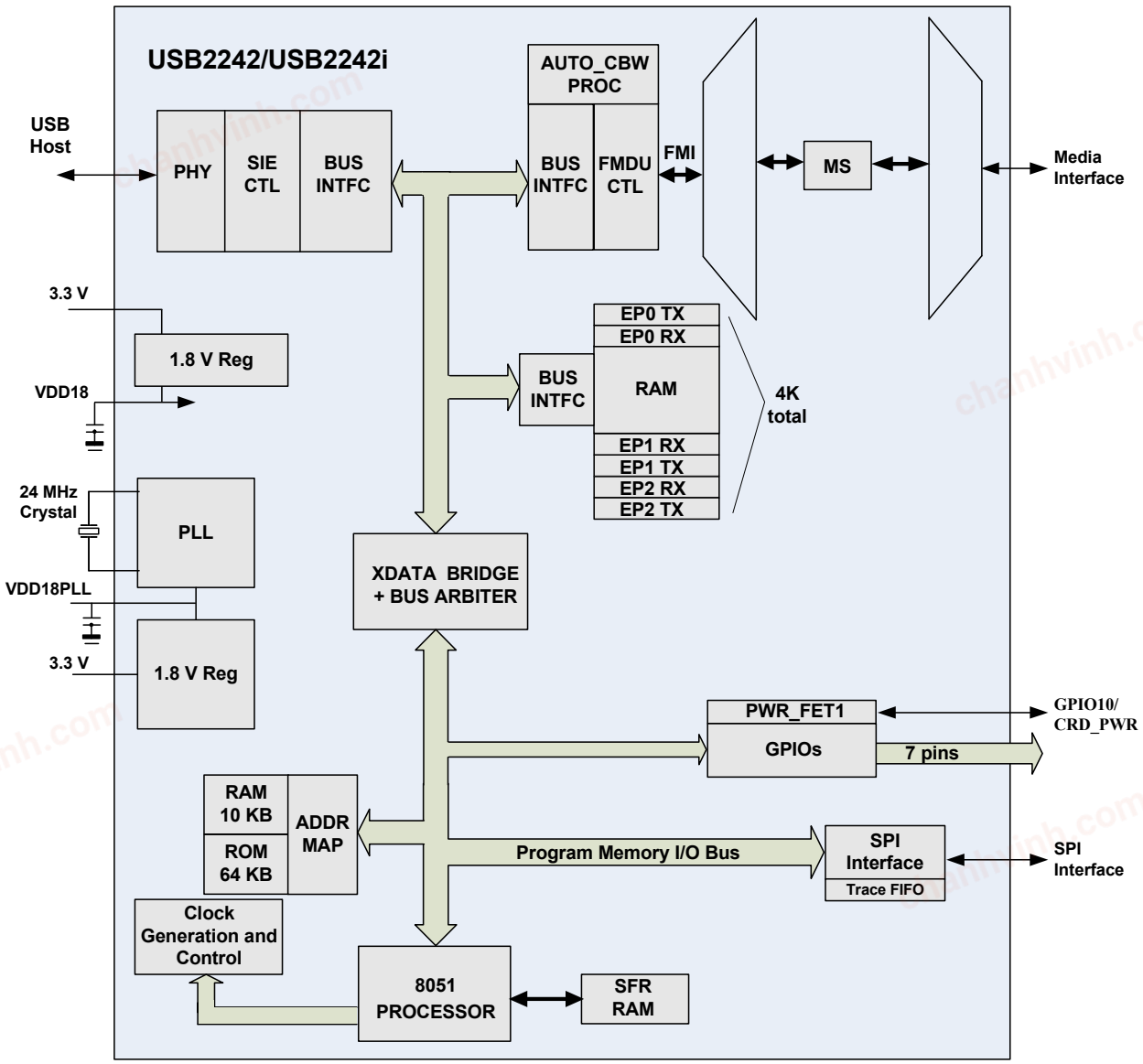


Figure 3.2 USB2242/42i Block Diagram

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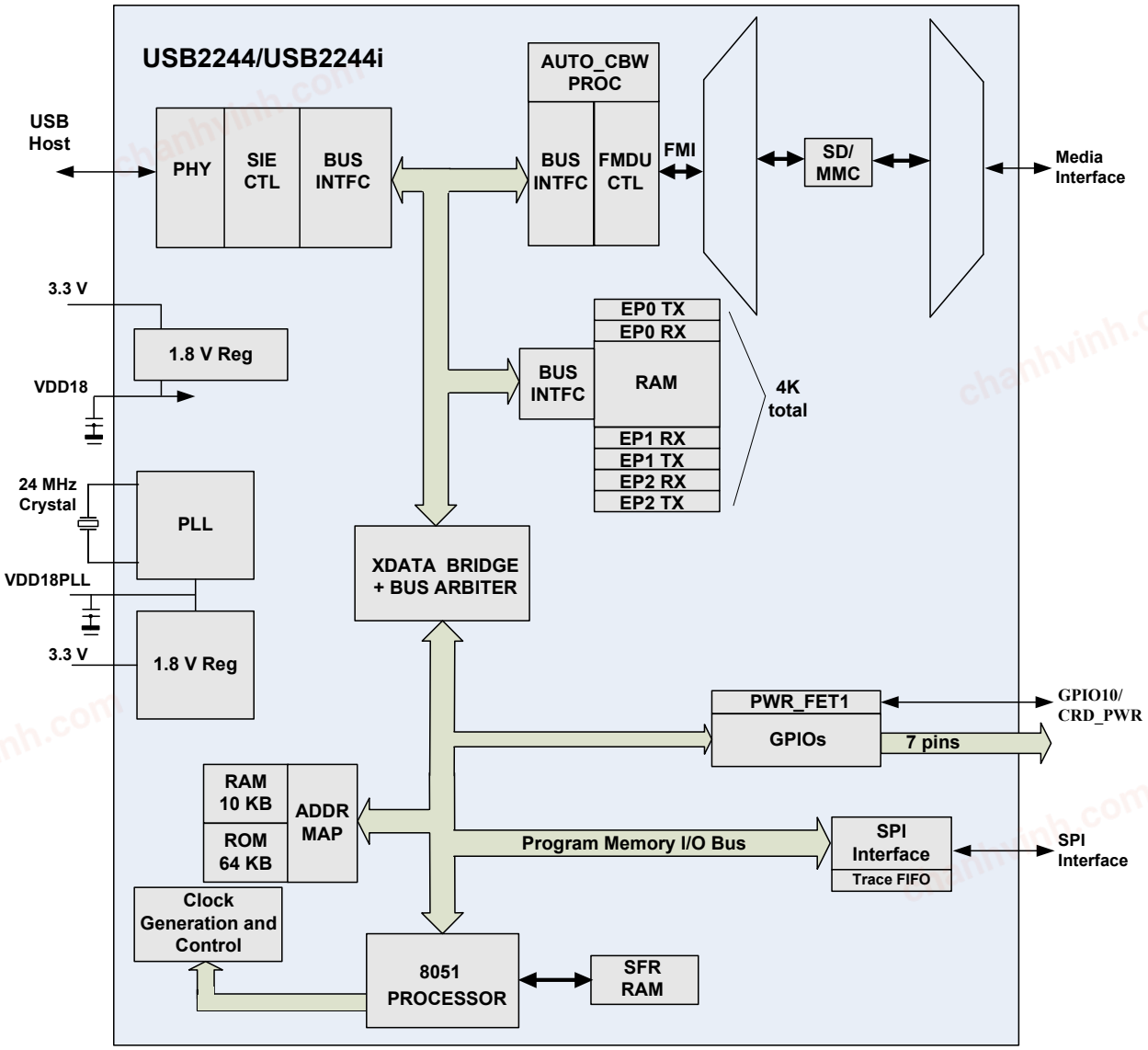


Figure 3.3 USB2244/44i Block Diagram

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Chapter 4 Pin Configurations

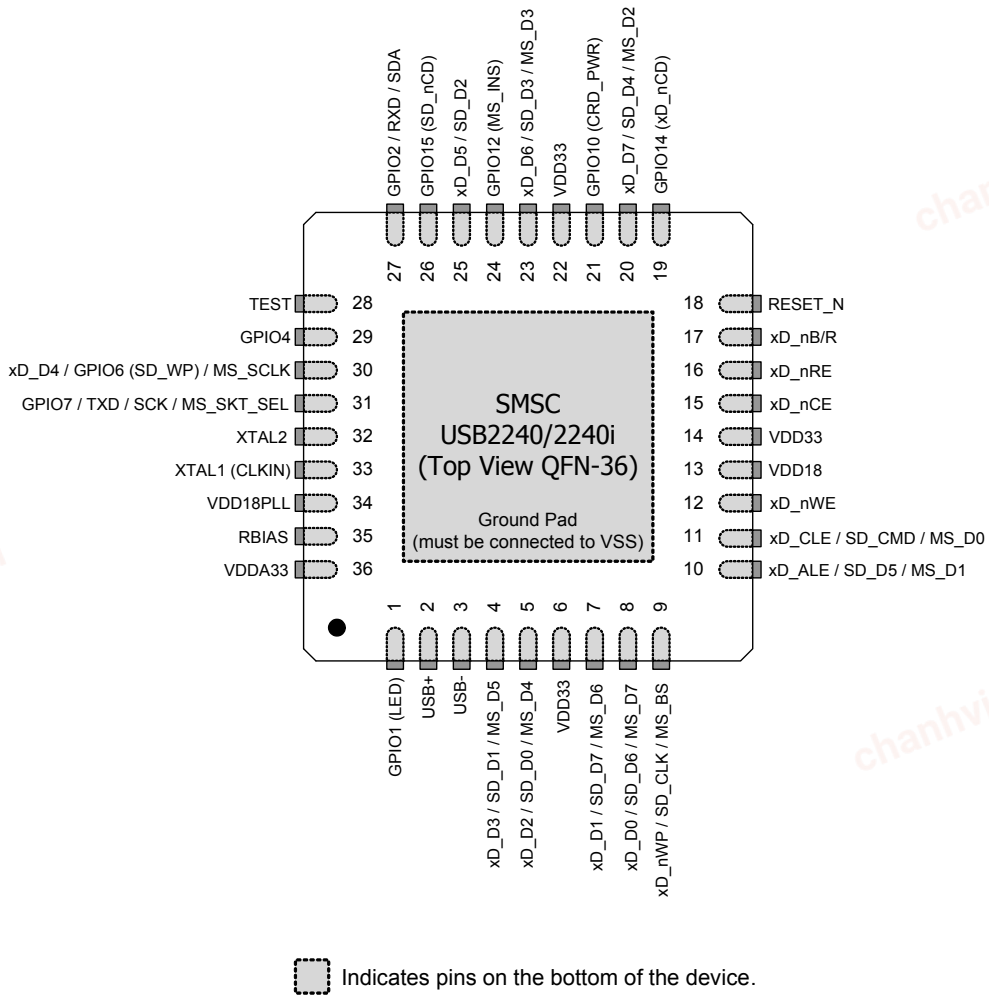


Figure 4.1 USB2240/USB2240i 36-Pin QFN Diagram

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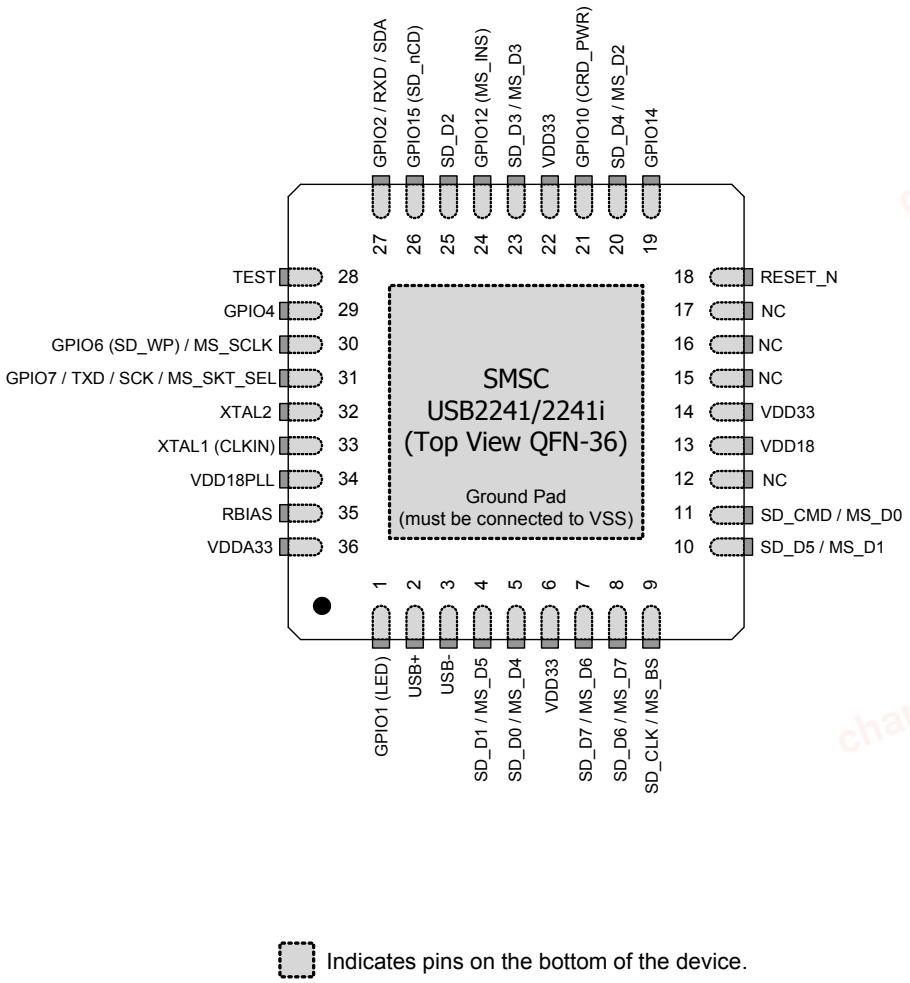


Figure 4.2 USB2241/USB2241i 36-Pin QFN Diagram

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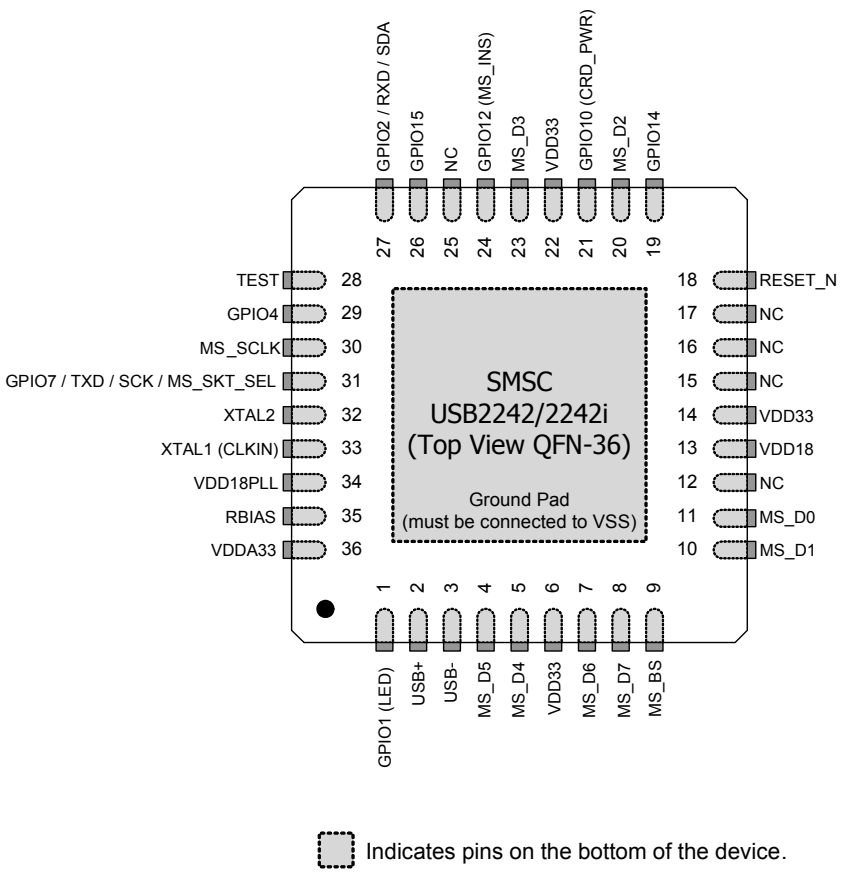


Figure 4.3 USB2242/USB2242i 36-Pin QFN Diagram

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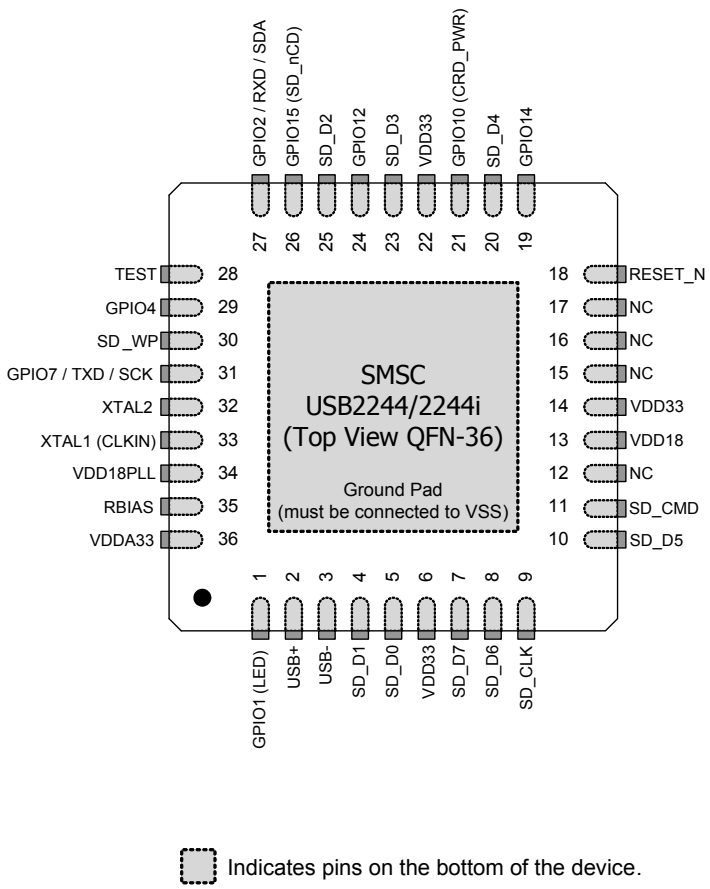


Figure 4.4 USB2244/USB2244i 36-Pin QFN Diagram

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Chapter 5 Pin Tables

Table 5.1 USB2240/2240i 36-Pin QFN Package

xD/SD/MS INTERFACE (18 PINS)			
xD_D3 / SD_D1 / MS_D5	xD_D2 / SD_D0 / MS_D4	xD_D1 / SD_D7 / MS_D6	xD_D0 / SD_D6 / MS_D7
xD_nWP / SD_CLK / MS_BS	xD_ALE / SD_D5 / MS_D1	xD_CLE / SD_CMD / MS_D0	xD_D7 / SD_D4 / MS_D2
xD_D6 / SD_D3 / MS_D3	xD_D5 / SD_D2	xD_nRE	xD_nWE
xD_D4 / GPIO6 (SD_WP) / MS_SCLK	xD_nB/R	xD_nCE	GPIO12 (MS_INS)
GPIO14 (xD_nCD)	GPIO15 (SD_nCD)		
USB INTERFACE (5 PINS)			
USB+	USB-	XTAL1 (CLKIN)	XTAL2
RBIAS			
MISC (7 Pins)			
GPIO1 (LED)	GPIO2 / RXD / SDA	GPIO4	GPIO7 / TXD / SCK / MS_SKT_SEL
GPIO10 (CRD_PWR)	TEST	RESET_N	
DIGITAL, POWER (6 PINS)			
(3) VDD33	VDDA33	VDD18	VDD18PLL
TOTAL 36			

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Table 5.2 USB2241/2241i 36-Pin QFN Package

SD/MS INTERFACE (14 PINS)			
SD_D1 / MS_D5	SD_D0 / MS_D4	SD_D7 / MS_D6	SD_D6 / MS_D7
SD_CLK / MS_BS	SD_D5 / MS_D1	SD_CMD / MS_D0	SD_D4 / MS_D2
SD_D3 / MS_D3	SD_D2	GPIO6 (SD_WP) / MS_SCLK	GPIO12 (MS_INS)
GPIO14	GPIO15 (SD_nCD)		
USB INTERFACE (5 PINS)			
USB+	USB-	XTAL1 (CLKIN)	XTAL2
RBIAS			
MISC (11 Pins)			
GPIO1 (LED)	GPIO2 / RXD / SDA	GPIO4	GPIO7 / TXD / SCK / MS_SKT_SEL
GPIO10 (CRD_PWR)	TEST	RESET_N	(4) NC
DIGITAL, POWER (6 PINS)			
(3) VDD33	VDDA33	VDD18	VDD18PLL
TOTAL 36			

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Table 5.3 USB2242/2242i 36-Pin QFN Package

MS INTERFACE (11 PINS)			
MS_D0	MS_D1	MS_D2	MS_D3
MS_D4	MS_D5	MS_D6	MS_D7
MS_BS	MS_SCLK	GPIO12 (MS_INS)	
USB INTERFACE (5 PINS)			
USB+	USB-	XTAL1 (CLKIN)	XTAL2
RBIAS			
MISC (14 PINS)			
GPIO1 (LED)	GPIO2 / RXD / SDA	GPIO4	GPIO7 / TXD / SCK / MS_SKT_SEL
GPIO10 (CRD_PWR)	GPIO14	GPIO15	(5) NC
TEST	RESET_N		
DIGITAL, POWER (6 PINS)			
(3) VDD33	VDDA33	VDD18	VDD18PLL
TOTAL 36			

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Table 5.4 USB2244/2244i 36-Pin QFN Package

SD/MMC INTERFACE (12 Pins)			
SD_D0	SD_D1	SD_D2	SD_D3
SD_D4	SD_D5	SD_D6	SD_D7
SD_CLK	SD_CMD	SD_WP	GPIO15 (SD_nCD)
USB INTERFACE (5 PINS)			
USB+	USB-	XTAL1 (CLKIN)	XTAL2
RBIAS			
MISC (13 PINS)			
GPIO1 (LED)	GPIO2 / RXD / SDA	GPIO4	GPIO7 / TXD / SCK
GPIO10 (CRD_PWR)	GPIO12	GPIO14	(4) NC
TEST	RESET_N		
DIGITAL, POWER (6 PINS)			
(3)VDD33	VDDA33	VDD18	VDD18PLL
TOTAL 36			

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Chapter 6 Pin Descriptions

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface. The pin descriptions are applied when using the internal default firmware and can be referenced in Chapter 7, "Pin Configurations," on page 26. Please reference Chapter 2, "Acronyms," on page 7 for a list of the acronyms used.

The “n” symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. When “n” is not present in the signal name, the signal is asserted at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

6.1 USB224x 36-Pin QFN Pin Descriptions

Table 6.1 USB224x 36-PiN QFN Pin Descriptions

SYMBOL	USB2240/40i	USB2241/41i	USB2242/42i	USB2244/44i	BUFFER TYPE	DESCRIPTION
xD-PICTURE CARD (xD) INTERFACE (APPLIES ONLY TO USB2240/USB2240i)						
xD_D[7:0]	20 23 25 30 4 5 7 8				I/O12PD	xD Data These bi-directional data signals have weak internal pull-down resistors.
xD_nWP	9				O12PD	xD Write Protect This pin is an active low write protect signal for the xD device and has a weak pull-down resistor that is permanently enabled.
xD_ALE	10				O12PD	xD Address Strobe This pin is an active high Address Latch Enable signal for the xD device and has a weak pull-down resistor that is permanently enabled.
xD_CLE	11				O12PD	xD Command Strobe This pin is an active high Command Latch Enable signal for the xD device and has a weak pull-down resistor that is permanently enabled.

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Table 6.1 USB224x 36-PiN QFN Pin Descriptions (continued)

SYMBOL	USB2240/40i	USB2241/41i	USB2242/42i	USB2244/44i	BUFFER TYPE	DESCRIPTION
xD_nRE	16				O12PU	xD Read Enable This pin is an active low read strobe signal for the xD device. When using the internal FET, this pin has a weak internal pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (Internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used).
xD_nWE	12				O12PU	xD Write Enable This pin is an active low write strobe signal for the xD device. When using the internal FET, this pin has a weak internal pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (Internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used).
xD_nB/R	17				IPU	xD Busy or Data Ready This pin is connected to the BSY/RDY pin of the xD device. When using the internal FET, this pin has a weak internal pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (Internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used).
GPIO14 (Note 6.1) (xD_nCD)	19				I/O12	xD Card Detection GPIO This is a GPIO designated by the default firmware as the xD-Picture card detection pin. **Note:** This pin can be left unconnected if the socket is not used.
xD_nCE	15				O12PU	xD Chip Enable This pin is the active low chip enable signal to the xD device. When using the internal FET, this pin has a weak internal pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (Internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used).

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Table 6.1 USB224x 36-PiN QFN Pin Descriptions (continued)

SYMBOL	USB2240/40i	USB2241/41i	USB2242/42i	USB2244/44i	BUFFER TYPE	DESCRIPTION
MEMORY STICK (MS) INTERFACE						
MS_D[7:0]	8 7 4 5 23 20 10 11				I/O12PD	MS System Data In/Out These pins are the bi-directional data signals for the MS device. MS_D0, MS_D2, and MS_D3 have weak pull-down resistors. In serial mode, the most significant bit (MSB) of each byte is transmitted first by either MSC or MS device on MS_D0. In parallel mode, MS_D1 has a pull-down resistor, otherwise it is disabled. In 4- or 8-bit parallel mode, there is a weak pull-down resistor on all MS_D7 - 0 signals.
MS_BS	9				O12	MS Bus State This pin is connected to the bus state (BS) pin of the MS device. It is used to control the bus states 0, 1, 2 and 3 (BS0, BS1, BS2 and BS3) of the MS device.
MS_SCLK	30				O12	MS System CLK This pin is an output clock signal to the MS device. The clock frequency is software configurable.
GPIO12 (Note 6.1) (MS_INS)	24				IPU	MS Card Insertion GPIO This is a GPIO designated by the default firmware as the Memory Stick card detection pin. **Note:** This pin can be left unconnected if the socket is not used.
SECURE DIGITAL (SD) / MULTIMEDIACARD (MMC) INTERFACE						
SD_D[7:0]	7 8 10 20 23 25 4 5			7 8 10 20 23 25 4 5	I/O12PU	SD Data The pins are bi-directional data signals SD_D0 - SD_D7 and have weak pull-up resistors.
SD_CLK	9			9	O12	SD Clock This is an output clock signal to SD/MMC device. The clock frequency is software configurable.
SD_CMD	11			11	I/O12PU	SD Command This is a bi-directional signal that connects to the CMD signal of the SD/MMC device and has a weak internal pull-up resistor.

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Table 6.1 USB224x 36-PiN QFN Pin Descriptions (continued)

SYMBOL	USB2240/40i	USB2241/41i	USB2242/42i	USB2244/44i	BUFFER TYPE	DESCRIPTION
GPIO6 (Note 6.1) (SD_WP)	30				I/O12	SD Write Protect Detection GPIO This is a GPIO designated by the default firmware as the Secure Digital card mechanical write protect detection pin.
GPIO15 (Note 6.1) (SD_nCD)	26				I/O12	SD Card Detect GPIO This is a GPIO designated by the default firmware as the Secure Digital card detection pin.
USB INTERFACE						
USB+ USB-	2 3				I/O-U	USB Bus Data These pins connect to the USB bus data signals.
RBIAS	35				I-R	USB Transceiver Bias A 12.0 kΩ, ± 1.0% resistor is attached from VSS to this pin in order to set the transceiver's internal bias currents.
XTAL1 (CLKIN)	33				ICLKx	24 MHz Crystal (External clock input) This pin can be connected to one terminal of the crystal or can be connected to an external 24 MHz clock when a crystal is not used.
XTAL2	32				OCLKx	24 MHz Crystal This is the other terminal of the crystal, or it is left open when an external clock source is used to drive XTAL1(CLKIN).
VDDA33	36					3.3 V Analog Power
VDD18PLL	34					1.8 V PLL Power +1.8 V Filtered analog power for internal PLL. This pin must have a 1.0 µF ± 20% (ESR < 0.1 Ω) capacitor to VSS.
MISC						
GPIO1 (Note 6.1) (LED)	1				I/O12	General Purpose I/O (GPIO): This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function. LED: GPIO1 can be used as an LED output.

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Table 6.1 USB224x 36-PiN QFN Pin Descriptions (continued)

SYMBOL	USB2240/40i	USB2241/41i	USB2242/42i	USB2244/44i	BUFFER TYPE	DESCRIPTION
GPIO2 (Note 6.1)/	27				I/O12	GPIO: This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
RXD /					I	RXD: This signal can be used as input to the RXD of UART in the device. Custom firmware is required to activate this function.
SDA					I/O12	SDA: This is the data pin when used with an external serial EEPROM.
GPIO4 (Note 6.1)	29				I/O12	GPIO: This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function. For the USB2240/USB2240i only, this pin can be used as the xD-Picture card detection pin.
GPIO7 (Note 6.1)/	31				I/O12	GPIO: This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
TXD /					O12	TXD: The GPIO7 can be used as an output TXD of UART in the device. Custom firmware is required to activate this function.
SCK /					O12	SCK: This is the clock output when used with an external EEPROM.
MS_SKT_SEL					I	MS_SKT_SEL: On the positive edge of RESET_N, this pin is sampled to determined the Memory Stick socket size. 1 = 8-bit 0 = 4-bit
GPIO10 (Note 6.1)	21				I/O200	GPIO: This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function.
(CRD_PWR)						CRD_PWR: Card power drive of 3.3 V at either 100 mA or 200 mA.
RESET_N	18				IS	RESET Input: This active low signal is used by the system to reset the chip. The active low pulse should be at least 1 µs wide.
TEST	28				I	TEST Input: Tie this pin to ground for normal operation.
GPIO12 (Note 6.1)				24	I/O12	This pin may be used either as input, edge sensitive interrupt input, or output.
GPIO14 (Note 6.1)			19		I/O12	This pin may be used either as input, edge sensitive interrupt input, or output.
GPIO15 (Note 6.1)			26		I/O12	This pin may be used either as input, edge sensitive interrupt input, or output.

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Table 6.1 USB224x 36-PiN QFN Pin Descriptions (continued)

SYMBOL	USB2240/40i	USB2241/41i	USB2242/42i	USB2244/44i	BUFFER TYPE	DESCRIPTION
NC		12 15 16 17	12 15 16 17 25	12 15 16 17		No Connect. No trace or signal should be routed/attached to these pins.
DIGITAL / POWER						
VDD18	13					+1.8 V core power. This pin must have a 1.0 µF ± 20% (ESR <0.1 Ω) capacitor to VSS.
VDD33	6 14 22					3.3 V Power and Regulator Input
VSS	ePad					Ground Pad/ePad: the package slug is the only VSS for the device and must be tied to ground with an array of 3x3 vias.

Note 6.1 See Table 11.1, "USB2240/40i and USB2241/41i GPIO Usage", Table 11.2, "USB2242/42i GPIO Usage", or Table 11.3, “USB2244/44i GPIO Usage,” on page 49 for GPIO pin usage for the internal default configuration.

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6.2 Buffer Type Descriptions

Table 6.2 Buffer Type Descriptions

BUFFER	DESCRIPTION
I	Input
IPU	Input with internal weak pull-up resistor
IS	Input with Schmitt trigger
I/O12	Input/output buffer with 12 mA sink and 12 mA source
I/O200	Input/Output buffer 12 mA with FET disabled, 100/200 mA source only when the FET is enabled
I/O12PD	Input/output buffer with 12 mA sink and 12 mA source with an internal weak pull-down resistor
I/O12PU	Input/output buffer with 12 mA sink and 12 mA source with a pull-up resistor
O12	Output buffer with 12 mA source
O12PU	Output buffer with 12 mA sink and 12 mA source, with a pull-up resistor
O12PD	Output buffer with 12 mA sink and 12 mA source, with a pull-down resistor
ICLKx	XTAL clock input
OCLKx	XTAL clock output
I/O-U	Analog input/output as defined in the USB 2.0 Specification
I-R	RBIAS

Note: The DC characteristics are outlined in Section 9.3, on page 43.

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Chapter 7 Pin Configurations

7.1 Card Reader

The SMSC USB224x is fully compliant with the following flash media card reader specifications:

- Secure Digital 2.0
  - HS-SD and SDHC
  - TransFlash™ and reduced form factor media
- MultiMediaCard 4.2
  - 1/4/8 bit MMC
- Memory Stick 1.43
- Memory Stick Pro Format 1.02
- Memory Stick Pro-HG Duo Format 1.01
  - Memory Stick, MS Duo, HS-MS, MS Pro-HG, MS Pro
- Memory Stick Duo 1.10
- xD-Picture Card 1.2

7.2 System Configurations

7.2.1 EEPROM

The USB224x can be configured via a 2-wire (I^2C) EEPROM (512x8) flash device containing the options for the USB224x. If an external configuration device does not exist the internal default values will be used. If one of the external devices is used for configuration, the OEM can update the values through the USB interface. The device will then “attach” to the upstream USB host.

The USBDM tool set is available in the USB224x/USB225x Card Reader software release package. To download the software package from SMSC's website, please visit:

https://www2.smsc.com/mkt/CW_SFT_PUB.nsf/Agreements/OBJ+Card+Reader

to go to the OBJ Card Reader Software Download Agreement. Review the license, and if you agree, check the "I agree" box and then select “Confirm”. You will then be able to download the USB224x/USB225x Card reader combo release package zip file containing the USBDM tool set. Please note that the following applies to the system values and descriptions when used:

- N/A = Not applicable to this part
- Reserved = For internal use

7.2.2 EEPROM Data Descriptor

Table 7.1 Internal Flash Media Controller Configurations

ADDRESS	REGISTER NAME	DESCRIPTION	INTERNAL DEFAULT VALUE
00h	USB_SER_LEN	USB Serial String Descriptor Length	1Ah
01h	USB_SER_TYP	USB Serial String Descriptor Type	03h
02h-19h	USB_SER_NUM	USB Serial Number	"000000225001" (See Note 7.1)

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Table 7.1 Internal Flash Media Controller Configurations (continued)

ADDRESS	REGISTER NAME	DESCRIPTION	INTERNAL DEFAULT VALUE
1Ah-1Bh	USB_VID	USB Vendor Identifier	0424
1Ch-1Dh	USB_PID	USB Product Identifier	2240
1Eh	USB_LANG_LEN	USB Language String Descriptor Length	04h
1Fh	USB_LANG_TYP	USB Language String Descriptor Type	03h
20h	USB_LANG_ID_LSB	USB Language Identifier Least Significant Byte	09h (See Note 7.2)
21h	USB_LANG_ID_MSB	USB Language Identifier Most Significant Byte	04h (See Note 7.2)
22h	USB_MFR_STR_LEN	USB Manufacturer String Descriptor Length	10h
23h	USB_MFR_STR_TYP	USB Manufacturer String Descriptor Type	03h
24h-31h	USB_MFR_STR	USB Manufacturer String	“Generic” (See Note 7.1)
32h-5Dh	Reserved	-	00h
5Eh	USB_PRD_STR_LEN	USB Product String Descriptor Length	24h
5Fh	USB_PRD_STR_TYP	USB Product String Descriptor Type	03h
60h-99h	USB_PRD_STR	USB Product String	“Ultra Fast Media Reader" (See Note 7.1)
9Ah	USB_BM_ATT	USB BmAttribute	80h
9Bh	USB_MAX_PWR	USB Max Power	30h (96 mA)
9Ch	ATT_LB	Attribute Lo byte	40h (Reverse SD_WP only)
9Dh	ATT_HLB	Attribute Hi Lo byte	00h
9Eh	ATT_LHB	Attribute Lo Hi byte	00h
9Fh	ATT_HB	Attribute Hi byte	00h
A0h	MS_PWR_LB	Memory Stick Device Power Lo byte	08h
A1h	MS_PWR_HB	Memory Stick Device Power Hi byte	00h
A2h	Reserved	-	80h
A3h	Reserved	-	00h
A4h	xD_PWR_LB	xD-Picture Card Device Power Lo byte	00h
A5h	xD_PWR_HB	xD-Picture Card Device Power Hi byte	08h

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Table 7.1 Internal Flash Media Controller Configurations (continued)

ADDRESS	REGISTER NAME	DESCRIPTION	INTERNAL DEFAULT VALUE
A6h	SD_PWR_LB	Secure Digital Device Power Lo byte	00h
A7h	SD_PWR_HB	Secure Digital Device Power Hi byte	80h
A8h	LED_BLK_INT	LED Blink Interval	02h
A9h	LED_BLK_DUR	LED Blink After Access	28h
AAh - B0h	DEV0_ID_STR	Device 0 Identifier String	“COMBO”
B1h - B7h	DEV1_ID_STR	Device 1 Identifier String	“MS”
B8h - BEh	DEV2_ID_STR	Device 2 Identifier String	“SM” (See Note 7.3)
BFh - C5h	DEV3_ID_STR	Device 3 Identifier String	“SD/MMC”
C6h - CDh	INQ_VEN_STR	Inquiry Vendor String	“Generic”
CEh-D2h	INQ_PRD_STR	Inquiry Product String	2240
D3h	DYN_NUM_LUN	Dynamic Number of LUNs	FFh
D4h - D7h	DEV_LUN_MAP	Device to LUN Mapping	FFh, FFh, FFh, FFh
D8h - DAh	Reserved	-	00h, 03h, 07h
DBh - DDh	Reserved	-	5Ch, 56h, 97h
DEh-FBh	Not Applicable	-	00h
FCh-FFh	NVSTORE_SIG	Non-Volatile Storage Signature	“ATA2”

Note 7.1 This value is a UNICODE UTF-16LE encoded string value that meets the USB 2.0 specification (Revision 2.0, 2000). Values in double quotations without this note are ASCII values.

Note 7.2 For a list of the most current 16-bit language ID’s defined by the USB-IF, please visit http://www.unicode.org or consult *The Unicode Standard, Worldwide Character Encoding*, (Version 4.0), The Unicode Consortium, Addison-Wesley Publishing Company, Reading, Massachusetts.

Note 7.3 The “SM” value will be overridden with “xD” once an xD-Picture Card has been identified.

7.2.3 EEPROM Data Descriptor Register Descriptions

7.2.3.1 00h: USB Serial String Descriptor Length

BYTE	NAME	DESCRIPTION
0	USB_SER_LEN	USB serial string descriptor length as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bLength” which describes the size of the string descriptor (in bytes).

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7.2.3.2 01h: USB Serial String Descriptor Type

BYTE	NAME	DESCRIPTION
1	USB_SER_TYP	USB serial string descriptor type as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bDescriptorType” which is a constant value associated with a string descriptor type.

7.2.3.3 02h-19h: USB Serial Number Option

BYTE	NAME	DESCRIPTION
25:2	USB_SER_NUM	Maximum string length is 12 hex digits. Must be unique to each device.

7.2.3.4 1Ah-1Bh: USB Vendor ID Option

BYTE	NAME	DESCRIPTION
1:0	USB_VID	This ID is unique for every vendor. The vendor ID is assigned by the USB Implementer’s Forum.

7.2.3.5 1Ch-1Dh: USB Product ID Option

BYTE	NAME	DESCRIPTION
1:0	USB_PID	This ID is unique for every product. The product ID is assigned by the vendor.

7.2.3.6 1Eh: USB Language Identifier Descriptor Length

BYTE	NAME	DESCRIPTION
0	USB_LANG_LEN	USB language ID string descriptor length as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bLength” which describes the size of the string descriptor (in bytes).

7.2.3.7 1Fh: USB Language Identifier Descriptor Type

BYTE	NAME	DESCRIPTION
1	USB_LANG_TYP	USB language ID string descriptor type as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bDescriptorType” which is a constant value associated with a string descriptor type.

7.2.3.8 20h: USB Language Identifier Least Significant Byte

BYTE	NAME	DESCRIPTION
2	USB_LANG_ID _LSB	English language code = ‘0409’. See Note 7.2 to reference additional language ID’s defined by the USB-IF.

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7.2.3.9 21h: USB Language Identifier Most Significant Byte

BYTE	NAME	DESCRIPTION
3	USB_LANG_ID_MSB	English language code = '0409'. See Note 7.2 to reference additional language ID's defined by the USB-IF.

7.2.3.10 22h: USB Manufacturer String Descriptor Length

BYTE	NAME	DESCRIPTION
0	USB_MFR_STR_LEN	USB manufacturer string descriptor length as defined by Section 9.6.7 "String" of the USB 2.0 Specification (Revision 2.0, 2000). This field is the "bLength" which describes the size of the string descriptor (in bytes).

7.2.3.11 23h: USB Manufacturer String Descriptor Type

BYTE	NAME	DESCRIPTION
1	USB_MFR_STR_TYP	USB manufacturer string descriptor type as defined by Section 9.6.7 "String" of the USB 2.0 Specification (Revision 2.0, 2000). This field is the "bDescriptorType" which is a constant value associated with a string descriptor type.

7.2.3.12 24h-31h: USB Manufacturer String Option

BYTE	NAME	DESCRIPTION
15:2	USB_MFR_STR	The maximum string length is 29 characters.

7.2.3.13 32h-5Dh: Reserved

BYTE	NAME	DESCRIPTION
59:16	Reserved	Reserved.

7.2.3.14 5Eh: USB Product String Descriptor Length

BYTE	NAME	DESCRIPTION
0	USB_PRD_STR_LEN	USB product string descriptor length as defined by Section 9.6.7 "String" of the USB 2.0 Specification (Revision 2.0, 2000). This field is the "bLength" which describes the size of the string descriptor (in bytes). Maximum string length is 29 characters

7.2.3.15 5Fh: USB Product String Descriptor Type

BYTE	NAME	DESCRIPTION
1	USB_PRD_STR_TYP	USB product string descriptor type as defined by Section 9.6.7 "String" of the USB 2.0 Specification (Revision 2.0, 2000). This field is the "bDescriptorType" which is a constant value associated with a string descriptor type.

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7.2.3.16 60h-99h: USB Product String Option

BYTE	NAME	DESCRIPTION
59:2	USB_PRD_STR	This string will be used during the USB enumeration process in the Windows® operating system. Maximum string length is 29 characters.

7.2.3.17 9Ah: USB BmAttribute (1 byte)

BIT	NAME	DESCRIPTION
7:0	USB_BM_ATT	Self- or Bus-Power: Selects between self- and bus-powered operation. The hub is either self-powered (draws less than 2 mA of upstream bus power) or bus-powered (limited to a 100 mA maximum of upstream power prior to being configured by the host controller). When configured as a bus-powered device, the SMSC device consumes less than 100 mA of current prior to being configured. After configuration, the bus-powered SMSC device (along with all associated device circuitry, any embedded devices if part of a compound device, and 100 mA per externally available downstream port) must consume no more than 500 mA of upstream VBUS current. The current consumption is system dependent, and the OEM must ensure that the USB 2.0 Specification is not violated. When configured as a self-powered device, <1 mA of upstream VBUS current is consumed and all ports are available, with each port being capable of sourcing 500 mA of current. **80 = Bus-powered operation (default)** C0 = Self-powered operation A0 = Bus-powered operation with remote wake-up E0 = Self-powered operation with remote wake-up

7.2.3.18 9Bh: USB MaxPower (1 byte)

BIT	NAME	DESCRIPTION
7:0	USB_MAX_PWR	USB Max Power per the USB 2.0 Specification. Do NOT set this value greater than 100 mA.

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7.2.3.19 9Ch-9Fh: Attribute Byte Descriptions

BYTE	BYTE NAME	BIT	DESCRIPTION
0	ATT_LB	3:0	Always reads ‘0’.
		4	Inquire Manufacturer and Product ID Strings ‘1’ - Use the Inquiry Manufacturer and Product ID Strings. ‘0’ (default) - Use the USB Descriptor Manufacturer and Product ID Strings.
		5	Always reads ‘0’.
		6	Reverse SD Card Write Protect Sense ‘1’ (default) - SD cards will be write protected when SW_nWP is high, and writable when SW_nWP is low. ‘0’ - SD cards will be write protected when SW_nWP is low, and writable when SW_nWP is high.
		7	Reserved.
1	ATT_HLB	3:0	Always reads ‘0’.
		4	Activity LED True Polarity ‘1’ - Activity LED to Low True. ‘0’ (default) - Activity LED polarity to High True.
		5	Common Media Insert / Media Activity LED ‘1’ - The activity LED will function as a common media inserted/media access LED. ‘0’ (default) - The activity LED will remain in its idle state until media is accessed.
		6	Always reads ‘0’.
		7	Reserved.
2	ATT_LHB	0	Attach on Card Insert / Detach on Card Removal ‘1’ - Attach on Insert is enabled. ‘0’ (default) - Attach on Insert is disabled.
		1	Always reads ‘0’.
		2	Enable Device Power Configuration ‘1’ - Custom Device Power Configuration stored in the NVSTORE is used. ‘0’ (default) - Default Device Power Configuration is used.
		7:3	Always reads ‘0’.
3	ATT_HB	6:0	Always reads ‘0’.
		7	xD Player Mode

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7.2.4 A0h-A7h: Device Power Configuration

The USB224x has one internal FET which can be utilized for card power. This section describes the default internal configuration. The settings are stored in NVSTORE and provide the following features:

1. A card can be powered by an external FET or by an internal FET.

2. The power limit can be set to 100 mA or 200 mA (Default) for the internal FET.

Each media uses two bytes to store its device power configuration. Bit 3 selects between internal or external card power FET options. For internal FET card power control, bits 0 through 2 are used to set the power limit. The “Device Power Configuration” bits are ignored unless the “Enable Device Power Configuration” bit is set. See Section 7.2.3.19, "9Ch-9Fh: Attribute Byte Descriptions," on page 32.

7.2.4.1 A0h-A1h: Memory Stick Device Power Configuration

FET	TYPE	BITS	BIT TYPE	DESCRIPTION
0	FET Lo Byte MS_PWR_LB	3:0	Low Nibble	0000b Disabled
1		7:4	High Nibble	
2	**FET Hi Byte** MS_PWR_HB	**3:0**	**Low Nibble**	0000b Disabled 0001b External FET enabled 1000b Internal FET with 100 mA power limit **1010b Internal FET with 200 mA power limit**
3		7:4	High Nibble	0000b Disabled

7.2.4.2 A2h-A3h: Not Applicable

BYTE	NAME	DESCRIPTION
1:0	Not Applicable	Not applicable.

7.2.4.3 A4h-A5h: xD-Picture Card Device Power Configuration

When applicable, the "SM" value will be overridden with “xD” once an xD-Picture Card has been identified.

FET	TYPE	BITS	BIT TYPE	DESCRIPTION
0	FET Lo Byte xD_PWR_LB	3:0	Low Nibble	0000b Disabled
1		7:4	High Nibble	
2	**FET Hi Byte** xD_PWR_HB	**3:0**	**Low Nibble**	0000b Disabled 0001b External FET enabled 1000b Internal FET with 100 mA power limit **1010b Internal FET with 200 mA power limit**
3		7:4	High Nibble	0000b Disabled

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7.2.4.4 A6h-A7h: Secure Digital Device Power Configuration

FET	TYPE	BITS	BIT TYPE	DESCRIPTION
0	FET Lo Byte SD_PWR_LB	3:0	Low Nibble	0000b Disabled
1		7:4	High Nibble	
2	**FET Hi Byte** SD_PWR_HB	**3:0**	**Low Nibble**	0000b Disabled 0001b External FET enabled 1000b Internal FET with 100 mA power limit **1010b Internal FET with 200 mA power limit**
3		7:4	High Nibble	0000b Disabled

7.2.4.5 A8h: LED Blink Interval

BYTE	NAME	DESCRIPTION
0	LED_BLK_INT	The blink rate is programmable in 50 ms intervals. The high bit (7) indicates an idle state: '0' - Off '1' - On The remaining bits (6:0) are used to determine the blink interval up to a max of 128 x 50 ms.

7.2.4.6 A9h: LED Blink Duration

BYTE	NAME	DESCRIPTION
1	LED_BLK_DUR	LED Blink After Access. This byte is used to designate the number of seconds that the GPIO1 LED will continue to blink after a drive access. Setting this byte to "05" will cause the GPIO 1 LED to blink for 5 seconds after a drive access.

7.2.5 Device ID Strings

These bytes are used to specify the LUN descriptor returned by the device. These bytes are used in combination with the device to LUN mapping bytes in applications where the OEM wishes to reorder and rename the LUNs. If multiple devices are mapped to the same LUN (a COMBO LUN), then the CLUN#_ID_STR will be used to name the COMBO LUN instead of the individual device strings. When applicable, the "SM" value will be overridden with xD once an xD-Picture Card has been identified.

7.2.5.1 AAh-B0h: Device 0 Identifier String

BYTE	NAME	DESCRIPTION
6:0	DEV0_ID_STR	Not applicable.

7.2.5.2 B1h-B7h: Device 1 Identifier String

BYTE	NAME	DESCRIPTION
6:0	DEV1_ID_STR	This ID string is associated with the Memory Stick device.

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7.2.5.3 B8h-BEh: Device 2 Identifier String

BYTE	NAME	DESCRIPTION
6:0	DEV2_ID_STR	This ID string is associated with the xD-Picture Card device.

7.2.5.4 BFh-C5h: Device 3 Identifier String

BYTE	NAME	DESCRIPTION
6:0	DEV3_ID_STR	This ID string is associated with the Secure Digital / MultiMediaCard device.

7.2.5.5 C6h-CDh: Inquiry Vendor String

BYTE	NAME	DESCRIPTION
7:0	INQ_VEN_STR	If bit 4 of the 1st attribute byte is set, the device will use these strings in response to a USB inquiry command, instead of the USB descriptor manufacturer and product ID strings.

7.2.5.6 CEh-D2h: Inquiry Product String

BYTE	NAME	DESCRIPTION
4:0	INQ_PRD_STR	If bit 4 of the 1st attribute byte is set, the device will use these strings in response to a USB inquiry command, instead of the USB descriptor manufacturer and product ID strings.

7.2.5.7 D3h: Dynamic Number of LUNs

BIT	NAME	DESCRIPTION
7:0	DYN_NUM_LUN	These bytes are used to specify the number of LUNs the device exposes to the host. These bytes are also used for icon sharing by assigning more than one LUN to a single icon. This is used in applications where the device utilizes a combo socket and the OEM wishes to have only a single icon displayed for one or more interfaces. If this field is set to "FF", the program assumes that you are using the default value and icons will be configured per the default configuration.

7.2.5.8 D4h-D7h: Device to LUN Mapping

BYTE	NAME	DESCRIPTION
3:0	DEV_LUN_MAP	These registers map a device controller (SD/MMC, SM, and MS) to a Logical Unit Number (LUN). The device reports the mapped LUNs to the USB host in the USB descriptor during enumeration. The icon installer associates custom icons with the LUNs specified in these fields. Setting a register to "FF" indicates that the device is not mapped. Setting all of the DEV_LUN_MAP registers for all devices to "FF" forces the use of the default mapping configuration. Not all configurations are valid. Valid configurations depend on the hardware, packaging, and OEM board layout. The number of unique LUNs mapped must match the value in the Section 7.2.5.7, "D3h: Dynamic Number of LUNs," on page 35.

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7.2.5.9 D8h-FBh: Not Applicable

BYTE	NAME	DESCRIPTION
35:0	Not Applicable	Not Applicable.

7.2.5.10 FCh-FFh: Non-Volatile Storage Signature

BYTE	NAME	DESCRIPTION
3:0	NVSTORE_SIG	This signature is used to verify the validity of the data in the first 256 bytes of the configuration area. The signature must be set to 'ATA2' for USB224x.

7.3 Default Configuration Option

The SMSC device can be configured via its internal default configuration. Please see Section 7.2.2, "EEPROM Data Descriptor" for specific details on how to enable default configuration. Please refer to Table 7.1 for the internal default values that are loaded when this option is selected.

7.3.1 External Hardware RESET_N

A valid hardware reset is defined as assertion of RESET_N for a minimum of 1 µs after all power supplies are within operating range. While reset is asserted, the device (and its associated external circuitry) consumes less than 500 µA of current from the upstream USB power source.

Assertion of RESET_N (external pin) causes the following:

1. The PHY is disabled and the differential pair will be in a high-impedance state.
2. All transactions immediately terminate; no states are saved.
3. All internal registers return to the default state.
4. The external crystal oscillator is halted.
5. The PLL is halted.
6. The processor is reset.
7. All media interfaces are reset.

7.3.1.1 RESET_N for EEPROM Configuration

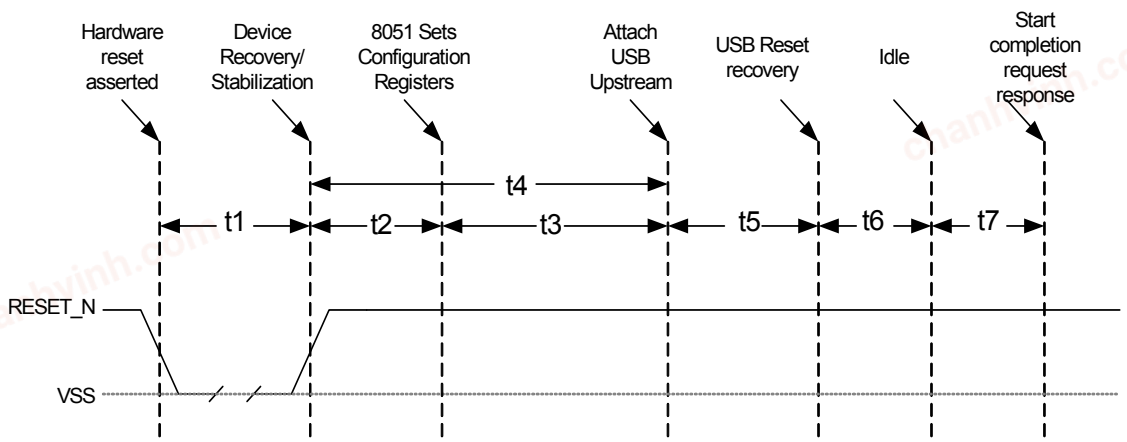


Figure 7.1 RESET_N Timing for EEPROM Mode

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Table 7.2 RESET_N Timing for EEPROM Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	RESET_N asserted	1			µsec
t2	Device recovery/stabilization			500	µsec
t3	8051 programs device configuration		20	50	msec
t4	USB attach			100	msec
t5	Host acknowledges attach and signals USB reset	100			msec
t6	USB idle		Undefined		msec
t7	Ready to handle requests (with or without data)			5	msec

Note: All power supplies must have reached the operating levels mandated in Chapter 9, DC Parameters, prior to (or coincident with) the assertion of RESET_N.

7.3.2 USB Bus Reset

In response to the upstream port signaling a reset to the device, the device does the following:

1. Sets default address to ‘0’.
2. Sets configuration to: Unconfigured.
3. All transactions are stopped.
4. Processor reinitializes and restarts.
5. All media interfaces are disabled.

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Chapter 8 Pin Reset States

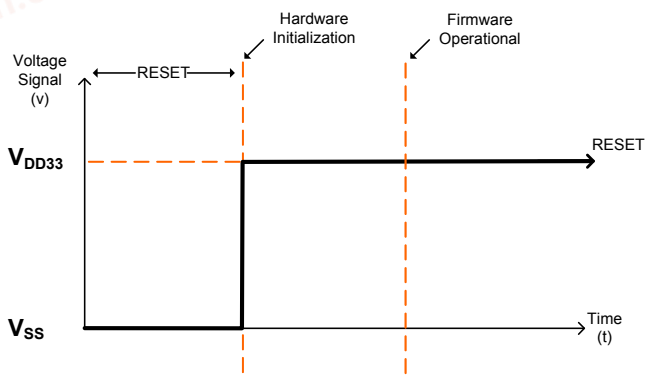


Figure 8.1 Pin Reset States

Table 8.1 Legend for Pin Reset States Table

SYMBOL	DESCRIPTION
0	Output driven low
1	Output driven high
IP	Input enabled
PU	Hardware enables pull-up
PD	Hardware enables pull-down
--	Hardware disables function
Z	Hardware disables pad. Both output driver and input buffers are disabled.

8.1 USB2240/40i/41/41i Pin Reset States

Table 8.2 USB2240/40i/41/41i 36-Pin Reset States

		RESET STATE		
PIN	PIN NAME	FUNCTION	INPUT/ OUT-PUT	PU/ PD
8	xD_D0 / SD_D6 / MS_D7	none	z	--
7	xD_D1 / SD_D7 / MS_D6	none	z	--
5	xD_D2 / SD_D0 / MS_D4	none	z	--
4	xD_D3 / SD_D1 / MS_D5	none	z	--
30	xD_D4 / GPIO6 (SD_WP) / MS_SCLK	SD_WP	0	--
25	xD_D5 / SD_D2	none	z	--
26	GPIO15 (SD_nCD)	GPIO	IP	pu

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Table 8.2 USB2240/40i/41/41i 36-Pin Reset States (continued)

		RESET STATE		
PIN	PIN NAME	FUNCTION	INPUT/ OUT-PUT	PU/ PD
24	GPIO12 (MS_INS)	GPIO	IP	pu
23	xD_D6 / SD_D3 / MS_D3	none	z	--
20	xD_D7 / SD_D4 / MS_D2	none	z	--
9	xD_nWP / SD_CLK / MS_BS	none	z	--
10	xD_ALE / SD_D5 / MS_D1	none	z	--
11	xD_CLE / SD_CMD / MS_D0	none	z	--
19	GPIO14 (xD_nCD)	GPIO	IP	pu
1	GPIO1 (LED)	GPIO	0	--
16	xD_nRE	none	z	--
27	GPIO2 / RXD / SDA	GPIO	0	--
29	GPIO4	GPIO	0	--
31	GPIO7 / TXD / SCK / MS_SKT_SEL	GPIO	0	--
21	GPIO10 (CRD_PWR)	GPIO	z	--
28	TEST	TEST	IP	--
18	RESET_N	RESET_N	IP	--
12	xD_nWE	none	z	--
17	xD_nB/R	none	z	--
15	xD_nCE	none	z	--
2	USB+	USB+	z	--
3	USB-	USB-	z	--

Note: xD signals only apply to USB2240/USB2240i.

8.2 USB2242/42i Pin Reset States

Table 8.3 USB2242/42i 36-Pin Reset States

		RESET STATE			POST-RESET STATE MS MODE			
PIN	PIN NAME	FUNCTION	INPUT / OUT-PUT	PU/ PD	FUNCTION	OUT-PUT	PU/ PD	IN-PUT
8	MS_D7	none	z	--	MS_D7	hw	pd	yes

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		RESET STATE			POST-RESET STATE MS MODE			
PIN	PIN NAME	FUNCTION	INPUT / OUT-PUT	PU/ PD	FUNCTION	OUT-PUT	PU/ PD	IN-PUT
7	MS_D6	none	z	--	MS_D6	hw	pd	yes
5	MS_D4	none	z	--	MS_D4	hw	pd	yes
4	MS_D5	none	z	--	MS_D5	hw	hw	yes
30	MS_SCLK	SD_WP	0	--	MS_SCLK	hw	hw	--
25	NC	none	z	--	none	z	--	--
23	MS_D3	none	z	--	MS_D3	hw	pd	yes
20	MS_D2	none	z	--	MS_D2	hw	pd	yes
9	MS_BS	none	z	--	MS_BS	hw	hw	--
10	MS_D1	none	z	--	MS_D1	hw	hw	yes
11	MS_D0	none	z	--	MS_D0	hw	pd	yes
19	GPIO14	GPIO	IP	pu				
26	GPIO15	GPIO	IP	pu				
24	GPIO12 (MS_INS)	GPIO	IP	pu				
27	GPIO2 / RXD / SDA	GPIO	0	--				
29	GPIO4	GPIO	0	--				
31	GPIO7 / TXD / SCK / MS_SKT_SEL	GPIO	0	--				
21	GPIO10 (CRD_PWR)	GPIO	z	--				
28	TEST	TEST	IP	--				
18	RESET_N	RESET_N	IP	--				
1	GPIO1 (LED)	GPIO	0	--				
16	NC	none	z	--	none	z	--	--
12	NC	none	z	--	none	z	--	--
17	NC	none	z	--	none	z	--	--
15	NC	none	z	--	none	z	--	--
2	USB+	USB+	z	--				
3	USB-	USB-	z	--				
35	RBIAS							
33	XTAL1 (CLKIN)							
32	XTAL2							

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8.3 USB2244/44i Pin Reset States

Table 8.4 USB2244/USB2244i 36-Pin Reset States

		RESET STATE			Post-Reset State SD Mode			
PIN	PIN NAME	FUNCTION	INPUT / OUT-PUT	PU/ PD	FUNCTION	OUT-PUT	PU/ PD	IN-PUT
8	SD_D6	none	z	--	SD_D6	hw	pu	yes
7	SD_D7	none	z	--	SD_D7	hw	pu	yes
5	SD_D0	none	z	--	SD_D0	hw	pu	yes
4	SD_D1	none	z	--	SD_D1	hw	pu	yes
30	SD_WP	SD_WP	0	--	SD_WP	(fw)	(fw)	(fw)
25	SD_D2	none	z	--	SD_D2	hw	pu	yes
23	SD_D3	none	z	--	SD_D3	hw	pu	yes
20	SD_D4	none	z	--	SD_D4	hw	pu	yes
9	SD_CLK	none	z	--	SD_CLK	hw	--	yes
10	SD_D5	none	z	--	SD_D5	hw	pu	yes
11	SD_CMD	none	z	--	SD_CMD	hw	pu	yes
19	GPIO14	GPIO	IP	pu				
26	GPIO15 (SD_nCD)	GPIO	IP	pu				
24	GPIO12	GPIO	IP	pu				
27	GPIO2 / RXD / SDA	GPIO	0	--	RXD	z	pu	yes
29	GPIO4	GPIO	0	--				
31	GPIO7 / TXD / SCK	GPIO	0	--	TXD	hw	--	--
21	GPIO10 (CRD_PWR)	GPIO	z	--	PWR	VDD	--	--
28	TEST	TEST	IP	--				
18	RESET_N	RESET_N	IP	--				
1	GPIO1 (LED)	GPIO	0	--				
17:15	NC	none	z	--	none	z	--	--
12	NC	none	z	--	none	z	--	--
2	USB+	USB+	z	--				
3	USB-	USB-	z	--				
35	RBIAS							
33	XTAL1 (CLKIN)							
32	XTAL2							

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Chapter 9 DC Parameters

9.1 Maximum Guaranteed Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Storage Temperature	T_A	-55	150	°C	
Lead Temperature				°C	Please refer to JEDEC specification J-STD-020D.
3.3 V supply voltage	V_{DD33}	-0.5	4.0	V	
Voltage on USB+ and USB- pins		-0.5	(3.3 V supply voltage + 2) ≤ 6	V	
Voltage on GPIO10		-0.5	V_{DD33} + 0.3	V	When internal power FET operation of this pin is enabled, this pin may be simultaneously shorted to ground or any voltage up to 3.63 V indefinitely, without damage to the device as long as V_{DD33} and V_{DDA33} are less than 3.63 V and T_A is less than 70°C.
Voltage on any signal pin		-0.5	V_{DD33} + 0.3	V	
Voltage on XTAL1		-0.5	3.6	V	
Voltage on XTAL2		-0.5	V_{DD18} + 0.3	V	

Note 9.1 Stresses above the specified parameters may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any condition above those indicated in the operation sections of this specification is not implied.

Note 9.2 When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

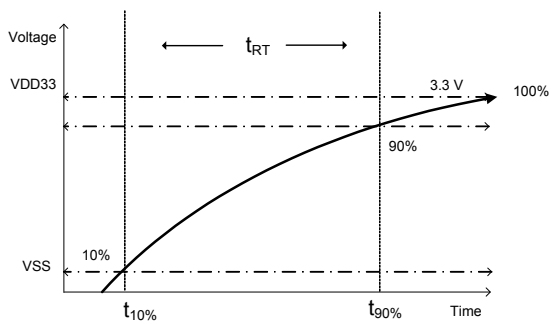


Figure 9.1 Supply Rise Time Model

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9.2 Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Commercial Part Industrial Part	T_A T_A	0 -40	70 85	°C °C	Operating Temperature Ambient temperature in still air.
3.3 V supply voltage	V_{DD33}	3.0	3.6	V	(Note 9.3)
3.3 V supply rise time	t_{RT}	0	400	µs	
Voltage on USB+ and USB- pins		-0.3	5.5	V	If any 3.3 V supply voltage drops below 3.0 V, then the MAX becomes: (3.3 V supply voltage) + 0.5 ≤ 5.5
Voltage on any signal pin		-0.3	V_{DD33}	V	
Voltage on XTAL1		-0.3	V_{DD33}	V	
Voltage on XTAL2		-0.3	V_{DD18}	V	

Note 9.3 A 3.3 V regulator with an output tolerance of 1% must be used if the output of the internal power FETs must support a 5% tolerance.

9.3 DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I, IPU, IPD Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	
IS Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Hysteresis	V_{HYSI}		420		mV	
ICLK Input Buffer						
Low Input Level	V_{ILCK}			0.5	V	
High Input Level	V_{IHCK}	1.4			V	
Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0 to V_{DD33}

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PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Input Leakage (All I and IS buffers)						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	V_{IN} = V_{DD33}
O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA @ V_{DD33}= 3.3 V
High Output Level	V_{OH}	V_{DD33} - 0.4			V	I_{OH} = -12 mA @ V_{DD33}= 3.3 V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DD33} (Note 9.4)
I/O12, I/O12PU & I/O12PD Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA @ V_{DD33}= 3.3 V
High Output Level	V_{OH}	V_{DD33} - 0.4			V	I_{OH} = -12 mA @ V_{DD33}= 3.3 V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DD33} (Note 9.4)
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	
IO-U (Note 9.5)						
I-R (Note 9.6)						

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PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I/O200 Integrated Power FET for GPIO10						
High Output Current Mode	I_{OUT}	200			mA	$Vdrop_{FET}$ = 0.46 V
Low Output Current Mode (Note 9.7)	I_{OUT}	100			mA	$Vdrop_{FET}$ = 0.23 V
On Resistance (Note 9.7)	R_{DSON}			2.1	Ω	I_{FET} = 70 mA
Output Voltage Rise Time	t_{DSON}			800	µs	C_{LOAD} = 10 µF
Supply Current Unconfigured	I_{CCINIT}		80	90	mA	
Supply Current Active Full Speed	I_{CC}		110	140	mA	
High Speed	I_{CC}		135	165	mA	
Supply Current Suspend	I_{CSBY}		350	700	µA	
Industrial Temperature Suspend	I_{CSBYI}		350	900	µA	

Note 9.4 Output leakage is measured with the current pins in high impedance.

Note 9.5 See The USB 2.0 Specification, Chapter 7, for USB DC electrical characteristics

Note 9.6 RBIAS is a 3.3 V tolerant analog pin.

Note 9.7 Output current range is controlled by program software, software disables FET during short circuit condition.

Note 9.8 The assignment of each Integrated Card Power FET to a designated Card Connector is controlled by both firmware and the specific board implementation. Firmware will default to the settings listed in Table 11.1, “USB2240/40i and USB2241/41i GPIO Usage,” on page 49.

Note 9.9 The 3.3 V supply should be at least at 75% of its operating condition before the 1.8 V supply is allowed to ramp up.

9.4 Capacitance

T_A = 25°C; fc = 1 MHz; V_{DD}, V_{DDP} = 1.8 V

Table 9.1 Pin Capacitance

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{XTAL}			2	pF	All pins (except USB pins and pins under test) are tied to AC ground.
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

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9.5 Package Thermal Specifications

Table 9.2 36-Pin QFN Package Thermal Parameters

PARAMETER	VELOCITY (meters/sec)	SYMBOL	VALUE	UNIT
Thermal Resistance	0	Θ_{JA}	33.2	°C/W
	1		29	
	2		26	
Junction-to-Top-of-Package	0	Ψ_{JT}	2.6	°C/W
	1		2.6	
	2		2.6	

Note 9.10 Thermal parameters are measured or estimated for devices with the exposed pad soldered to thermal vias in a multilayer 2S2P PCB per JESD51. Thermal resistance is measured from the die to the ambient air.

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Chapter 10 AC Specifications

10.1 Oscillator/Crystal

Parallel Resonant, Fundamental Mode, 24 MHz ± 350 ppm.

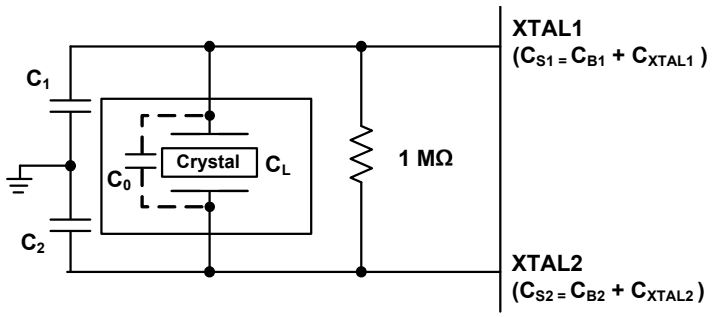


Figure 10.1 Typical Crystal Circuit

Table 10.1 Crystal Circuit Legend

SYMBOL	DESCRIPTION	IN ACCORDANCE WITH
C_0	Crystal shunt capacitance	Crystal manufacturer's specification (See Note 10.1)
C_L	Crystal load capacitance	
C_B	Total board or trace capacitance	OEM board design
C_S	Stray capacitance	SMSC IC and OEM board design
C_{XTAL}	XTAL pin input capacitance	SMSC IC
C_1	Load capacitors installed on OEM board	Calculated values based on Figure 10.2, "Capacitance Formulas" (See Note 10.2)
C_2		

$$C_1 = 2 \times (C_L - C_0) - C_{S1}$$

$$C_2 = 2 \times (C_L - C_0) - C_{S2}$$

Figure 10.2 Capacitance Formulas

Note 10.1 C_0 is usually included (subtracted by the crystal manufacturer) in the specification for C_L and should be set to '0' for use in the calculation of the capacitance formulas in Figure 10.2, "Capacitance Formulas". However, the OEM PCB itself may present a parasitic capacitance between XTAL1 and XTAL2. For an accurate calculation of C_1 and C_2, take the parasitic capacitance between traces XTAL1 and XTAL2 into account.

Note 10.2 Each of these capacitance values is typically approximately 18 pF.

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10.2 Ceramic Resonator

24 MHz ± 350 ppm

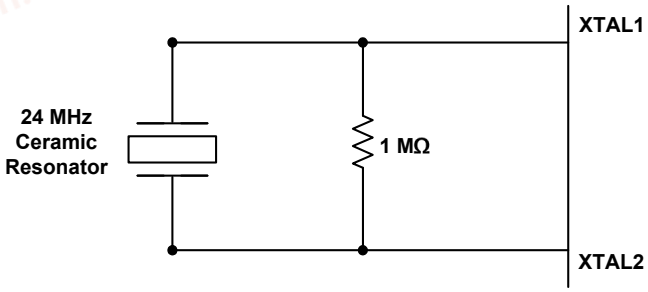


Figure 10.3 Ceramic Resonator Usage with SMSC IC

10.3 External Clock

50% Duty cycle ± 10%, 24 MHz ± 350 ppm, Jitter < 100 ps rms.

The external clock is recommended to conform to the signaling level designated in the JESD76-2 specification on 1.8 V CMOS Logic. XTAL2 should be treated as a no connect or drive only a CMOS-like buffer.

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Chapter 11 GPIO Usage

Table 11.1 USB2240/40i and USB2241/41i GPIO Usage

NAME	ACTIVE LEVEL	SYMBOL	DESCRIPTION AND NOTE
GPIO1	H	LED	LED indicator
GPIO2	H	RXD / SDA	Receive Port of Debugger / Serial EEPROM Data
GPIO4	N/A	GPIO	Not used
GPIO6	L	SD_WP	SD Write Protect Detection
GPIO7	H	TXD / SCK / MS_SKT_SEL	Transmit Port of Debugger / Serial EEPROM Clock / Memory Stick Socket (1 = 8-bit; 0 = 4-bit)
GPIO10	L	CRD_PWR	Card Power Control
GPIO12	L	MS_INS	Memory Stick Card Insertion
GPIO14	L	xD_nCD	xD-Picture Card detect (USB2240/40i only)
GPIO15	L	SD_nCD	Secure Digital card detect

Table 11.2 USB2242/42i GPIO Usage

NAME	ACTIVE LEVEL	SYMBOL	DESCRIPTION AND NOTE
GPIO1	H	LED	LED indicator
GPIO2	H	RXD / SDA	Receive Port of Debugger / Serial EEPROM Data
GPIO4	N/A	GPIO	Not used
GPIO6	L	SD_WP	SD Write Protect Detection
GPIO7	H	TXD / SCK / MS_SKT_SEL	Transmit Port of Debugger / Serial EEPROM Clock / Memory Stick Socket (1 = 8-bit; 0 = 4-bit)
GPIO10	L	CRD_PWR	Card Power Control
GPIO12	L	MS_INS	Memory Stick Card Insertion
GPIO14	N/A	GPIO	Not used
GPIO15	N/A	GPIO	Not used

Table 11.3 USB2244/44i GPIO Usage

NAME	ACTIVE LEVEL	SYMBOL	DESCRIPTION AND NOTE
GPIO1	H	LED	LED indicator
GPIO2	H	RXD / SDA	Receive Port of Debugger / Serial EEPROM Data
GPIO4	N/A	GPIO	Not used

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Table 11.3 USB2244/44i GPIO Usage (continued)

GPIO6	H	SD_WP	SD Write Protect Detection
GPIO7	H	TXD / SCK / MS_SKT_SEL	Transmit Port of Debugger / Serial EEPROM Clock / Memory Stick Socket (1 = 8-bit; 0 = 4-bit)
GPIO10	L	CRD_PWR	Card Power Control
GPIO12	N/A	GPIO	Not used
GPIO14	N/A	GPIO	Not used
GPIO15	L	SD_nCD	Secure Digital card detect

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Chapter 12 Package Outline

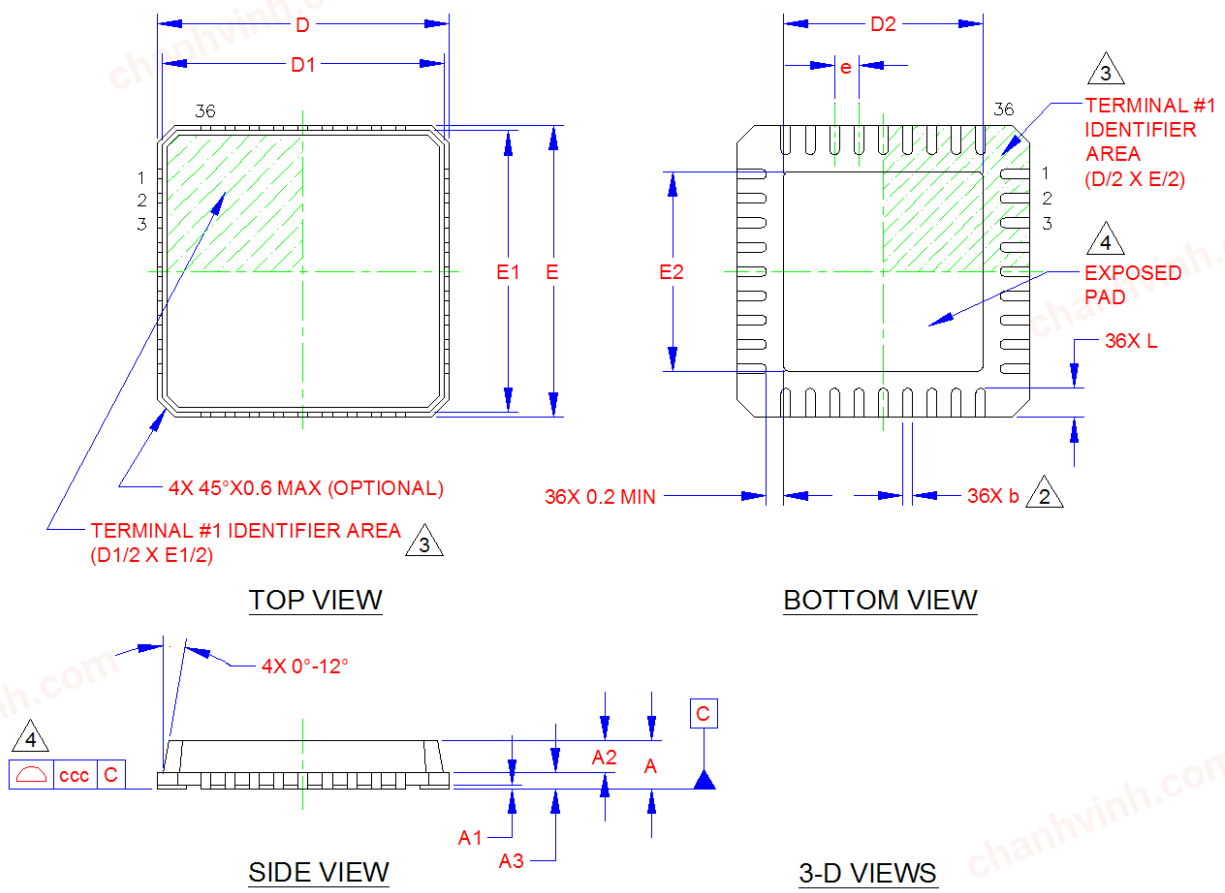


Figure 12.1 USB224x 36-QFN, 6x6 mm Body, 0.5 mm Pitch

Table 12.1 Package Parameters

SYMBOL	MIN	NOMINAL	MAX	NOTE	REMARKS
A	0.80	~	1.00	-	Overall Package Height
A1	0	0.02	0.05	-	Standoff
A2	0.60	~	0.80	-	Mold Thickness
A3		0.20 REF		-	Leadframe Thickness
D/E	5.85	6.00	6.15	-	X/Y Overall Body Size
D1/E1	5.55	~	5.95	-	X/Y Mold Cap Size
D2/E2	4.00	4.10	4.20	2	X/Y Exposed Pad Size
L	0.50	0.60	0.75	-	Terminal Length
b	0.18	0.25	0.30	2	Terminal Width
e		0.50 BSC		-	Terminal Pitch

Note 12.1 All dimensions are in millimeters.

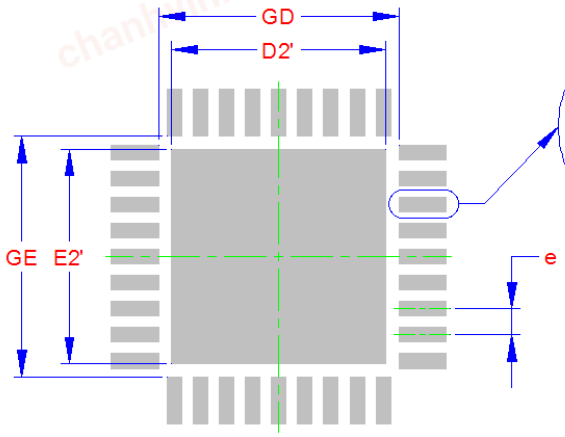
Note 12.2 Position tolerance of each terminal and exposed pad is ±0.05 mm at maximum material condition.

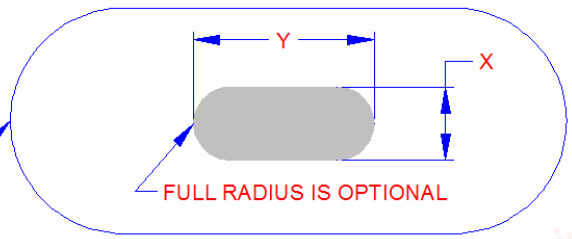
Note 12.3 Dimension “b” applies to plated terminals and is measured between 0.15 mm and 0.30 mm from the terminal tip.

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Note 12.4 Details of terminal #1 identifier are optional but must be located within the area indicated.

Note 12.5 Coplanarity zone applies to exposed pad and terminals.





THE USER MAY MODIFY THE PCB LAND PATTERN DIMENSIONS BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY

LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	4.60	-	-
D2'/E2'	-	4.10	-
X	-	-	0.28
Y	-	-	0.90
e		0.50	

RECOMMENDED PCB LAND PATTERN

Figure 12.2 Additional Package Information and Notes

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Datasheet Revision History

Table 12.2 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 2.1 (02-07-13)	Document co-branded: Microchip logo added to cover; company disclaimer modified. Added the following to the ordering information: “Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.”	
Rev 2.1 (12-22-10)	Chapter 3, Figure 3.1, 3.2, and 3.3	Upgraded to put the mux for the multiplexed interface inside the part, put in a SPI interface for outside access to the Program Memory I/O bus.
Rev 2.1 (11-23-10)	Chapter 6, Table 6.1	Removed “ It may not be used to drive any external circuitry other than the crystal circuit” from the XTAL2 description.
Rev. 2.1 (10-21-10)	Chapter 11, Table 11.3	Changed the active level from L to H for GPIO6.