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TN2640

N-Channel Enhancement-Mode Vertical DMOS FET

Features

- 2V Maximum Low Threshold
- High Input Impedance
- Low Input Capacitance
- Fast Switching Speeds
- Low On-Resistance
- Free from Secondary Breakdown
- Low Input and Output Leakage

Applications

- Logic-Level Interfaces (Ideal for TTL and CMOS)
- Solid-State Relays
- Battery-Operated Systems
- Photovoltaic Drives
- Analog Switches
- General Purpose Line Drivers
- Telecommunication Switches

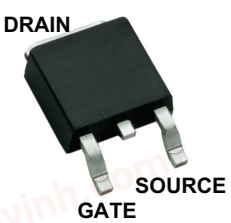
General Description

The TN2640 low-threshold Enhancement-mode (normally-off) transistor uses a vertical DMOS structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

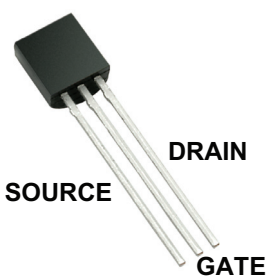
Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Types

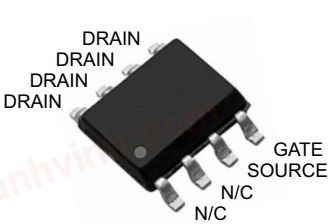
3-lead TO-252 (D-PAK)
(Top view)



3-lead TO-92
(Top view)



8-lead SOIC
(Top view)



See Table 3-1, Table 3-2, and Table 3-3 for pin information.

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Drain-to-Source Voltage ..... BV_{DSS}
Drain-to-Gate Voltage ..... BV_{DGS}
Gate-to-Source Voltage..... ±20V
Operating Ambient Temperature, T_A ..... –55°C to +150°C
Storage Temperature, T_S ..... –55°C to +150°C

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C unless otherwise specified. All DC parameters are 100% tested at 25°C unless otherwise stated. (Pulse test: 300 µs pulse, 2% duty cycle)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	400	—	—	V	V_{GS} = 0V, I_D = 1 mA
Gate Threshold Voltage	$V_{GS(th)}$	0.8	—	2	V	V_{GS} = V_{DS}, I_D = 2 mA
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	–2.5	–4	mV/°C	V_{GS} = V_{DS}, I_D = 2 mA (**Note 1**)
Gate Body Leakage Current	I_{GSS}	—	—	100	nA	V_{GS} = ±20V, V_{DS} = 0V
Zero-Gate Voltage Drain Current	I_{DSS}	—	—	10	µA	V_{GS} = 0V, V_{DS} = Maximum rating
		—	—	1	mA	V_{DS} = 0.8 Maximum rating, V_{GS} = 0V, T_A = 125°C (**Note 1**)
On-State Drain Current	$I_{D(ON)}$	1.5	3.5	—	A	V_{GS} = 5V, V_{DS} = 25V
		2	4	—	A	V_{GS} = 10V, V_{DS} = 25V
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	3.2	5	Ω	V_{GS} = 4.5V, I_D = 500 mA
		—	3	5	Ω	V_{GS} = 10V, I_D = 500 mA
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	—	0.75	%/°C	V_{GS} = 10V, I_D = 500 mA (**Note 1**)

Note 1: Specification is obtained by characterization and is not 100% tested.

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AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C unless otherwise specified. All AC parameters are not 100% sample tested.						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Forward Transconductance	G_{FS}	200	330	—	mmho	V_{DS} = 25V, I_D = 100 mA
Input Capacitance	C_{ISS}	—	210	225	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1 MHz
Common-Source Output Capacitance	C_{OSS}	—	30	50	pF	
Reverse Transfer Capacitance	C_{RSS}	—	8	15	pF	
Turn-On Delay Time	$t_{d(ON)}$	—	4	15	ns	V_{DD} = 25V, I_D = 2A, R_{GEN} = 25Ω
Rise Time	t_r	—	15	20	ns	
Turn-Off Delay Time	$t_{d(OFF)}$	—	20	25	ns	
Fall Time	t_f	—	22	27	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V_{SD}	—	—	0.9	V	V_{GS} = 0V, I_{SD} = 200 mA (**Note 1**)
Reverse Recovery Time	t_{rr}	—	300	—	ns	V_{GS} = 0V, I_{SD} = 1A

Note 1: All DC parameters are 100% tested at 25°C unless otherwise stated. (Pulse test: 300 µs pulse, 2% duty cycle)

TEMPERATURE SPECIFICATIONS

Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–55	—	+150	°C	
Storage Temperature	T_S	–55	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
3-lead TO-252 (D-PAK)	θ_{JA}	—	81	—	°C/W	
8-lead SOIC	θ_{JA}	—	101	—	°C/W	
3-lead TO-92	θ_{JA}	—	132	—	°C/W	

THERMAL CHARACTERISTICS

Package	**I_D (Note 1) (Continuous) (mA)**	**I_D (Pulsed) (A)**	**Power Dissipation at T_A = 25°C (W)**	**I_{DR} (Note 1) (mA)**	**I_{DRM} (A)**
3-lead TO-252 (D-PAK)	500	3	2.5 (**Note 2**)	500	3
8-lead SOIC	260	2	1.3 (**Note 2**)	260	2
3-lead TO-92	220	2	0.74	220	2

Note 1: I_D (continuous) is limited by maximum T_J.

2: Mounted on an FR4 board, 25 mm x 25 mm x 1.57 mm

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

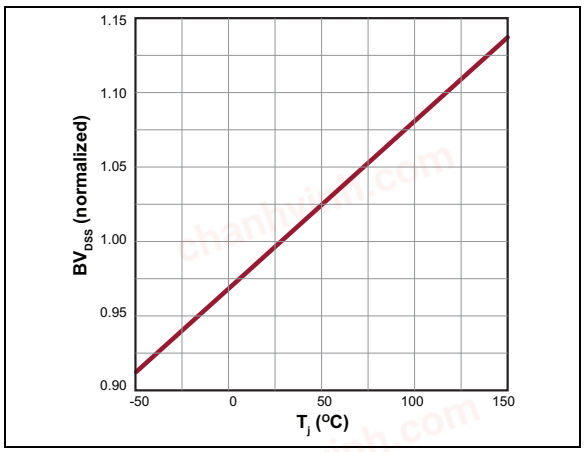


FIGURE 2-1: *BV_{DSS} Variation with Temperature.*

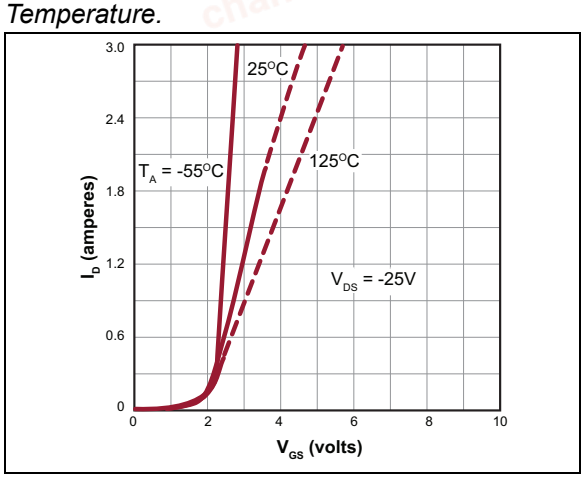


FIGURE 2-2: *Transfer Characteristics.*

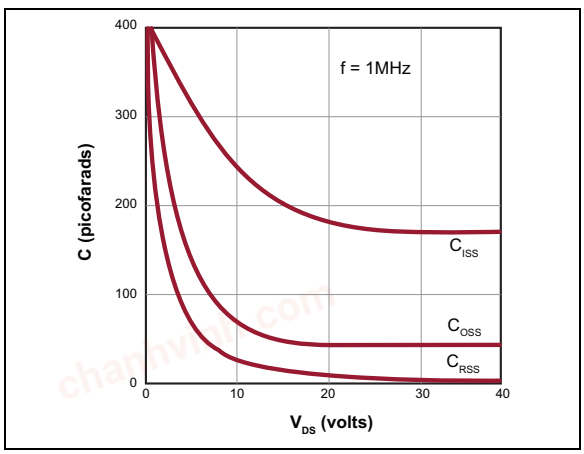


FIGURE 2-3: *Capacitance vs. Drain-to-source Voltage.*

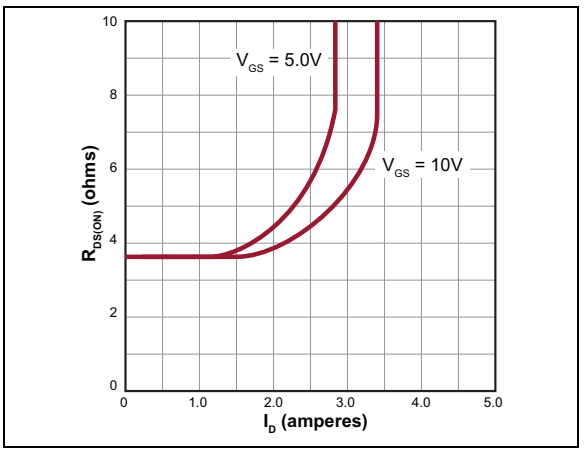


FIGURE 2-4: *On-resistance vs. Drain Current.*

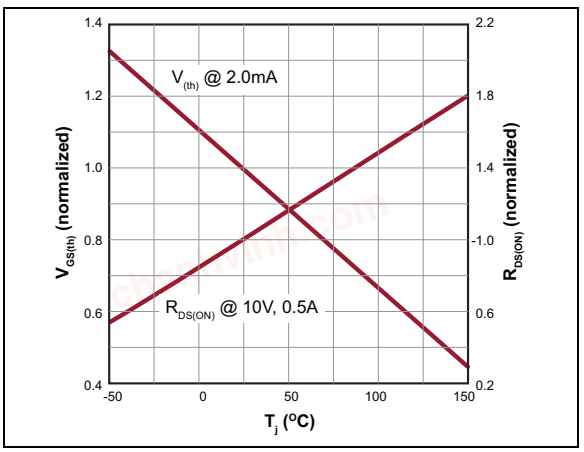


FIGURE 2-5: *$V_{GS(th)}$ and $R_{DS(ON)}$ Variation with Temperature.*

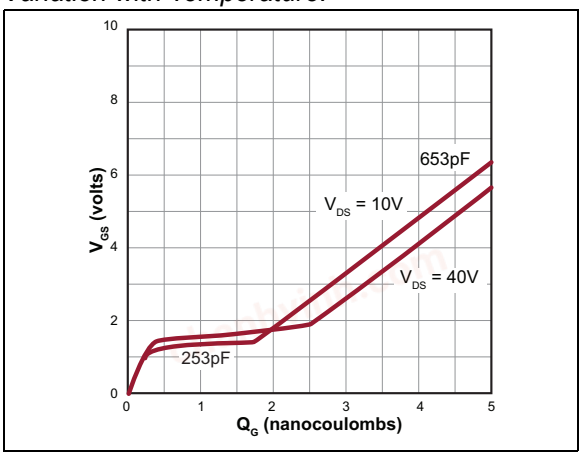


FIGURE 2-6: *Gate Drive Dynamic Characteristics.*

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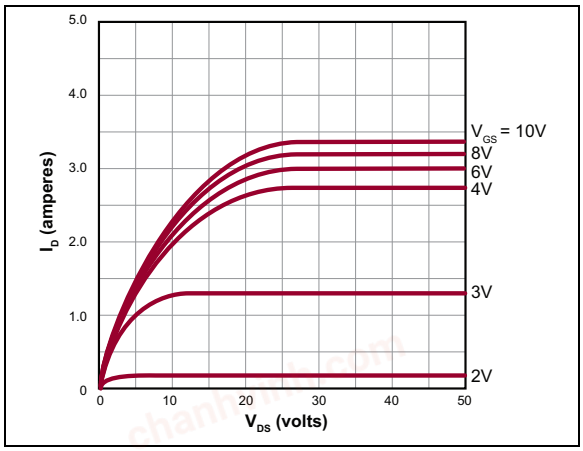


FIGURE 2-7: *Output Characteristics.*

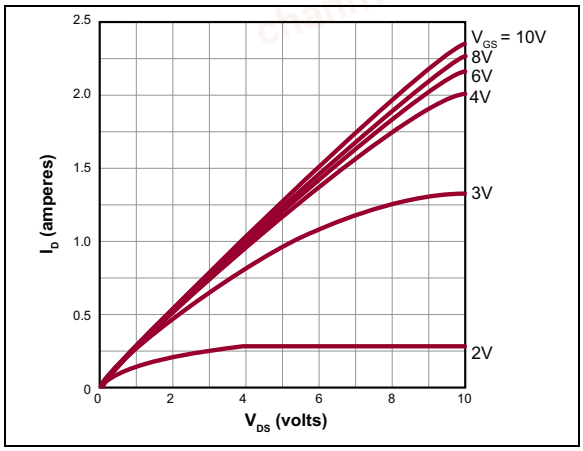


FIGURE 2-10: *Saturation Characteristics.*

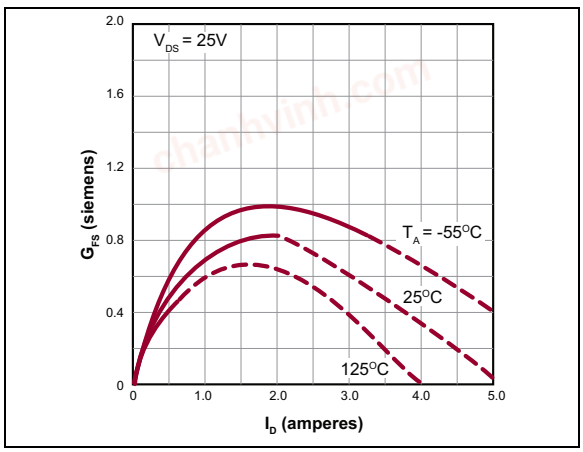


FIGURE 2-8: *Transconductance vs. Drain Current.*

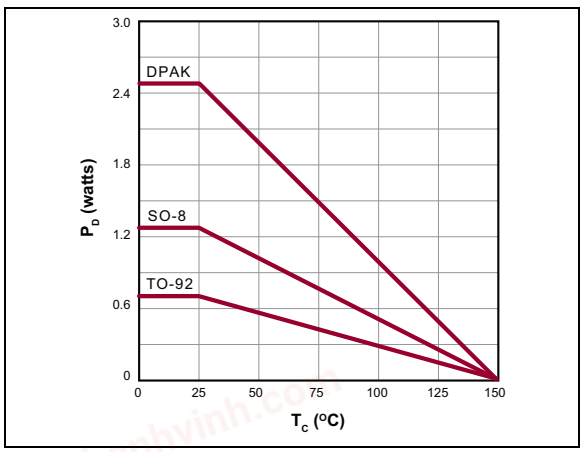


FIGURE 2-11: *Power Dissipation vs. Temperature.*

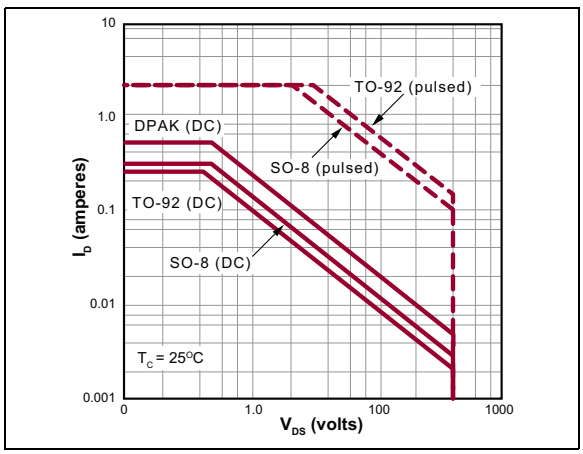


FIGURE 2-9: *Maximum Rated Safe Operating Area.*

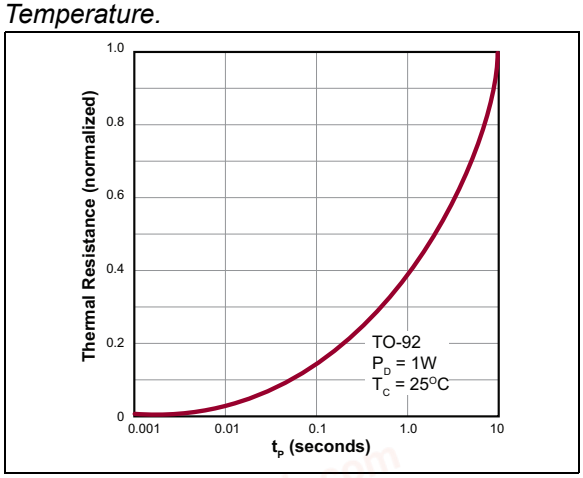


FIGURE 2-12: *Thermal Response Characteristics.*

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3.0 PIN DESCRIPTION

Table 3-1, Table 3-2, and Table 3-3 show the description of pins in TN2640. Refer to **Package Types** for the location of the pins.

TABLE 3-1: 3-LEAD TO-252 (DPAK) PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Gate	Gate
3	Source	Source
4	Drain	Drain

TABLE 3-2: 8-LEAD SOIC PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	N/C	No connect
2	N/C	No connect
3	Source	Source
4	Gate	Gate
5	Drain	Drain
6	Drain	Drain
7	Drain	Drain
8	Drain	Drain

TABLE 3-3: 3-LEAD TO-92 PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Source	Source
2	Gate	Gate
3	Drain	Drain

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4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for TN2640.

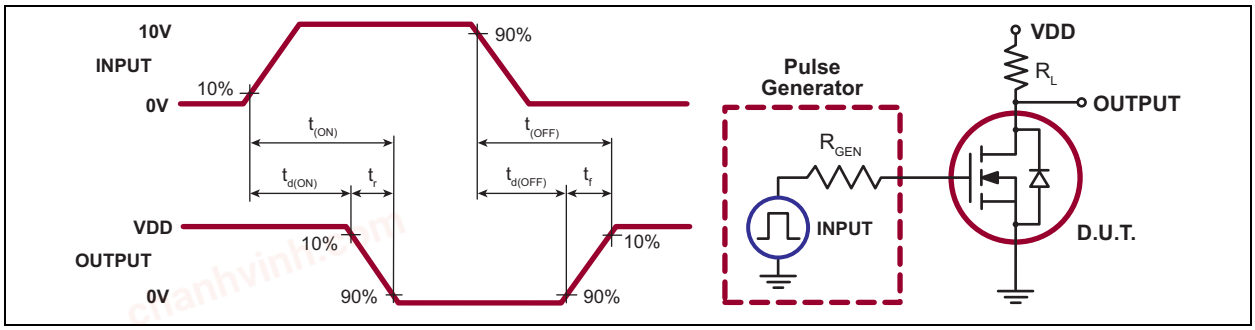


FIGURE 4-1: *Switching Waveforms and Test Circuit.*

TABLE 4-1: PRODUCT SUMMARY

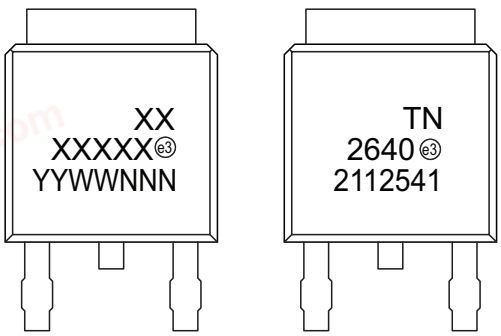
BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (Maximum) (Ω)	$I_{D(ON)}$ (Minimum) (A)	$V_{GS(th)}$ (Maximum) (V)
400	5	2	2

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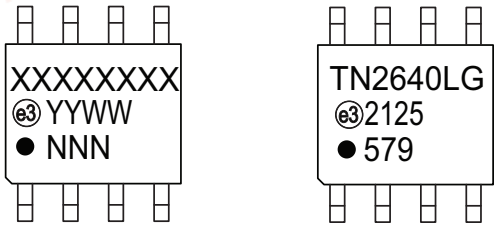
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

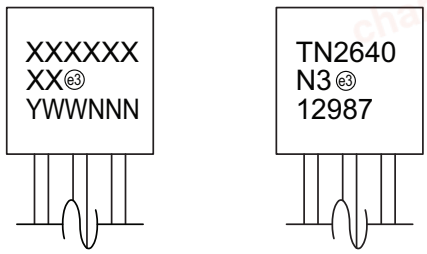
TO-252 (D-PAK) Example



8-lead SOIC Example



3-lead TO-92 Example



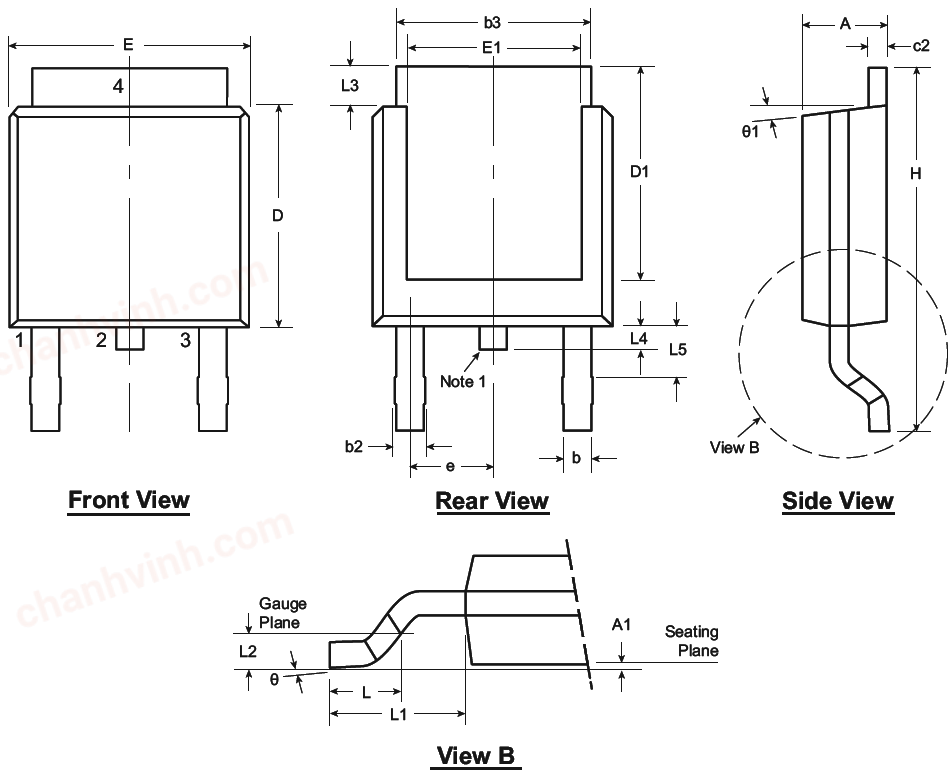
Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

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3-Lead TO-252 (D-PAK) Package Outline (K4)



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. Although 4 terminal locations are shown, only 3 are functional. Lead number 2 was removed.

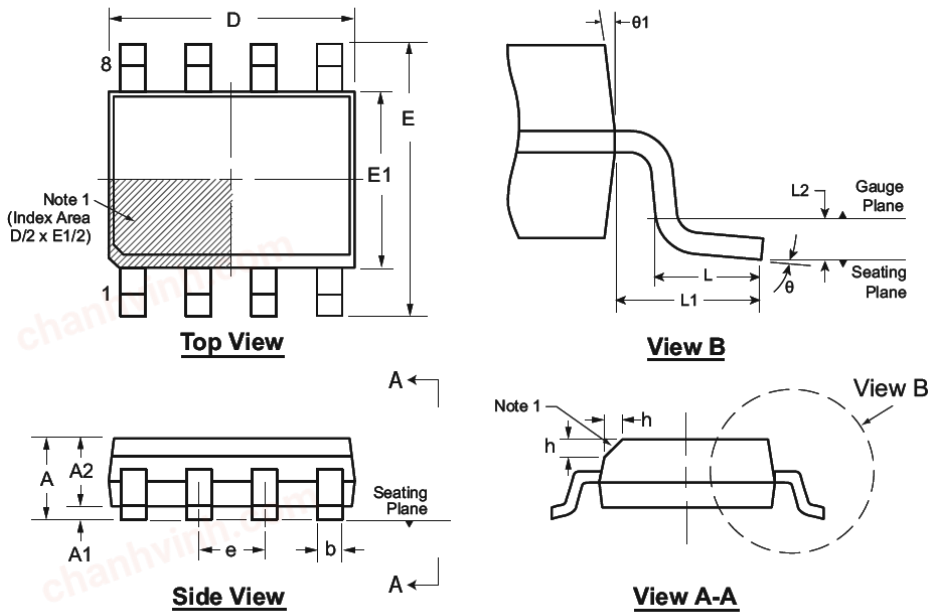
Symbol		A	A1	b	b2	b3	c2	D	D1	E	E1	e	H	L	L1	L2	L3	L4	L5	θ	θ1
Dimension (inches)	MIN	.086	.000*	.025	.030	.195	.018	.235	.205	.250	.170	.090 BSC	.370	.055	.108 REF	.020 BSC	.035	.025*	.035†	0°	0°
	NOM	-	-	-	-	-	-	.240	-	-	-		-	.060			-	-	-	-	-
	MAX	.094	.005	.035	.045	.215	.035	.245	.217*	.265	.200*		.410	.070			.050	.040	.060	10°	15°

JEDEC Registration TO-252, Variation AA, Issue E, June 2004.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

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8-Lead SOIC (Narrow Body) Package Outline (LG/TG)

4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

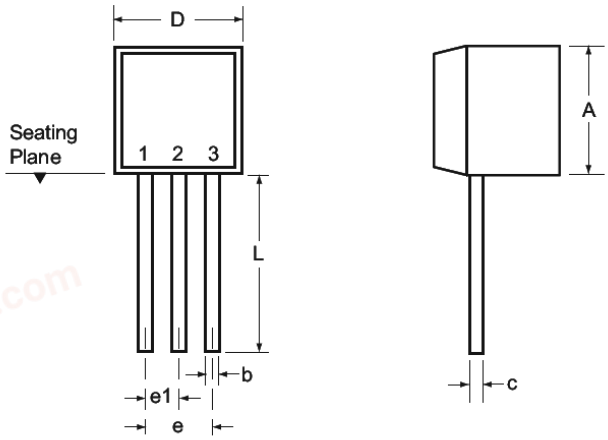
** This dimension is not specified in the JEDEC drawing.*

Drawings are not to scale.

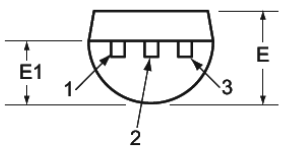
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3-Lead TO-92 Package Outline (L/LL/N3)



Front View **Side View**



Bottom View

Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014†	.014†	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022†	.022†	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

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NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (February 2021)

- Converted Supertex Doc# DSFP-TN2640 to Microchip DS20005795A
- Changed the package marking format
- Updated the quantity of the 8-lead SOIC from 2500/Reel to 3300/Reel to align it with the actual BQM
- Removed the TO-92 N3 P002, P003, P005, P013, and P015 media types to align package specifications with the actual BQM
- Made minor text changes throughout the document

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	TN2640	=	N-Channel Enhancement-Mode Vertical DMOS FET
Packages:	K4	=	3-lead TO-252 (D-PAK)
	LG	=	8-lead SOIC
	N3	=	3-lead TO-92
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Types:	(blank)	=	2000/Reel for a K4 Package
		=	3300/Reel for an LG Package
		=	1000/Bag for an N3 Package

Examples:

a) TN2640K4-G: N-Channel Enhancement-Mode Vertical DMOS FET, 3-lead TO-252 (D-PAK), 2000/Reel

b) TN2640LG-G: N-Channel Enhancement-Mode Vertical DMOS FET, 8-lead SOIC, 3300/Reel

c) TN2640N3-G: N-Channel Enhancement-Mode Vertical DMOS FET, 3-lead TO-92, 1000/Bag

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Note the following details of the code protection feature on Microchip devices:

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- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
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