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TC4426A/TC4427A/TC4428A

1.5A Dual High-Speed Power MOSFET Drivers

Features

- Passes AEC-Q100 Automotive Reliability Testing
- High Peak Output Current: 1.5A
- Wide Input Supply Voltage Operating Range:
  - 4.5V to 18V
- High Capacitive Load Drive Capability: 1000 pF in 25 ns (typical)
- Short Delay Times: 30 ns (typical)
- Matched Rise, Fall and Delay Times
- Low Supply Current:
  - With Logic '1' Input – 1 mA (typical)
  - With Logic '0' Input – 100 µA (typical)
- Low Output Impedance: 7Ω (typical)
- Latch-Up Protected: Will Withstand 0.5A Reverse Current
- Input Withstands Negative Inputs Up to 5V
- Electrostatic Discharge (ESD) Protected: 2 kV
- Pin-compatible with TC426/TC427/TC428 and TC4426/TC4427/TC4428
- Space-saving 8-Pin MSOP and 8-Pin 6x5 DFN-S Packages

Applications

- Switch Mode Power Supplies
- Line Drivers
- Pulse Transformer Drive

General Description

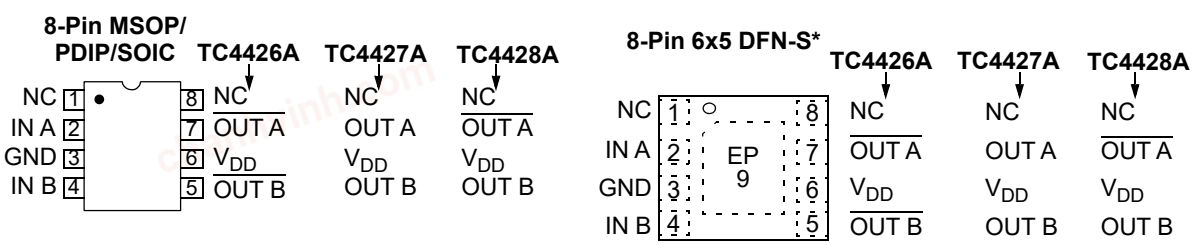
The TC4426A/TC4427A/TC4428A are improved versions of the earlier TC4426/TC4427/TC4428 family of MOSFET drivers. In addition to matched rise and fall times, the TC4426A/TC4427A/TC4428A devices have matched leading and falling edge propagation delay times.

These devices are highly latch-up resistant under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking (of either polarity) occurs on the Ground pin. They can accept, without damage or logic upset, up to 500 mA of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against Electrostatic Discharge (ESD) up to 2 kV.

The TC4426A/TC4427A/TC4428A MOSFET drivers can easily charge/discharge 1000 pF gate capacitances in under 30 ns. These devices provide low enough impedances in both the On and Off states to ensure the MOSFET's intended state will not be affected, even by large transients.

The TC4426A/TC4427A/TC4428A is AEC-Q100 qualified for automotive applications.

Package Types

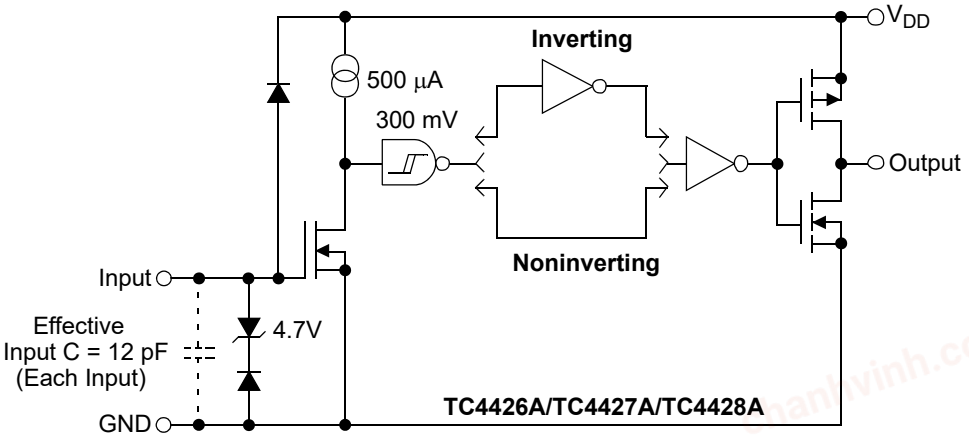


* Includes Exposed Thermal Pad (EP); see Table 3-1.

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Functional Block Diagram



Note 1: TC4426A has two inverting drivers, while the TC4427A has two noninverting drivers. The TC4428A has one inverting and one noninverting driver.

2: Ground any unused driver input.

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage ..... +22V
Input Voltage, IN A or IN B ..... (V_{DD} + 0.3V) to (GND – 5V)
Package Power Dissipation ($T_A \leq +70°C$)
DFN-S ..... Note 2
MSOP ..... 340 mW
PDIP ..... 730 mW
SOIC ..... 470 mW

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, over operating temperature range with 4.5V $\leq V_{DD} \leq$ 18V.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input						
Logic ‘1’, High Input Voltage	V_{IH}	2.4	—	—	V	
Logic ‘0’, Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Current	I_{IN}	-1.0	—	+1.0	µA	$0V \leq V_{IN} \leq V_{DD}$
		-10	—	+10		
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC Test
Low Output Voltage	V_{OL}	—	—	0.025	V	DC Test
Output Resistance	R_O	—	7	9	Ω	I_{OUT} = 10 mA, V_{DD} = 18V, T_A = +25°C
		—	7	10		0°C ≤ T_A ≤ +70°C
		—	8	11		-40°C ≤ T_A ≤ +85°C
		—	8	12		-40°C ≤ T_A ≤ +125°C
Peak Output Current	I_{PK}	—	1.5	—	A	V_{DD} = 18V
Latch-Up Protection Withstand Reverse Current	I_{REV}	—	> 0.5	—	A	Duty cycle ≤ 2%, t ≤ 300 µs V_{DD} = 18V
Switching Time (Note 1)						
Rise Time	t_R	—	25	35	ns	T_A = +25°C
		—	27	40		0°C ≤ T_A ≤ +70°C
		—	29	40		-40°C ≤ T_A ≤ +85°C
		—	30	40		-40°C ≤ T_A ≤ +125°C, Figure 4-1
Fall Time	t_F	—	25	35	ns	T_A = +25°C
		—	27	40		0°C ≤ T_A ≤ +70°C
		—	29	40		-40°C ≤ T_A ≤ +85°C
		—	30	40		-40°C ≤ T_A ≤ +125°C, Figure 4-1

Note 1: Switching times ensured by design.
2: Package power dissipation is dependent on the copper pad area on the PCB.

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DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, over operating temperature range with 4.5V ≤ V_{DD} ≤ 18V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Delay Time	t_{D1}	—	30	35	ns	T_A = +25°C
		—	33	40		0°C ≤ T_A ≤ +70°C
		—	35	45		-40°C ≤ T_A ≤ +85°C
		—	38	50		-40°C ≤ T_A ≤ +125°C, **Figure 4-1**
Delay Time	t_{D2}	—	30	35	ns	T_A = +25°C
		—	33	40		0°C ≤ T_A ≤ +70°C
		—	35	45		-40°C ≤ T_A ≤ +85°C
		—	38	50		-40°C ≤ T_A ≤ +125°C, **Figure 4-1**
Power Supply						
Power Supply Current	I_S	—	1.0	2.0	mA	V_{IN} = 3V (Both inputs)
		—	0.1	0.2		V_{IN} = 0V (Both inputs), V_{DD} = 18V

Note 1: Switching times ensured by design.

2: Package power dissipation is dependent on the copper pad area on the PCB.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply with 4.5V ≤ V_{DD} ≤ 18V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range (C)	T_A	0	—	+70	°C	
Specified Temperature Range (E)	T_A	-40	—	+85	°C	
Specified Temperature Range (V)	T_A	-40	—	+125	°C	
Maximum Junction Temperature	T_J	—	—	+150	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Package Thermal Resistances						
Thermal Resistance, 8L-6x5 DFN-S	θ_{JA}	—	35.7	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	211	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	89.3	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	149.5	—	°C/W	

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, over operating temperature range with $4.5V \leq V_{DD} \leq 18V$.

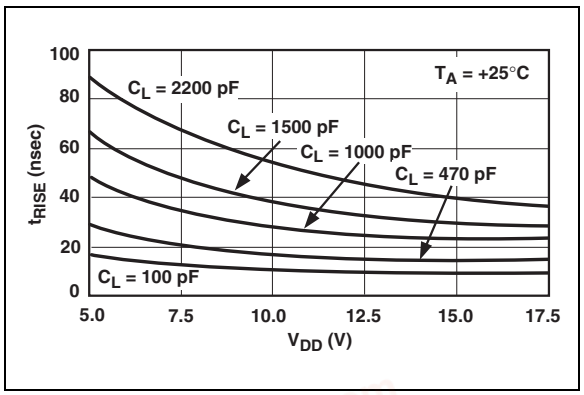


FIGURE 2-1: *Rise Time vs. Supply Voltage.*

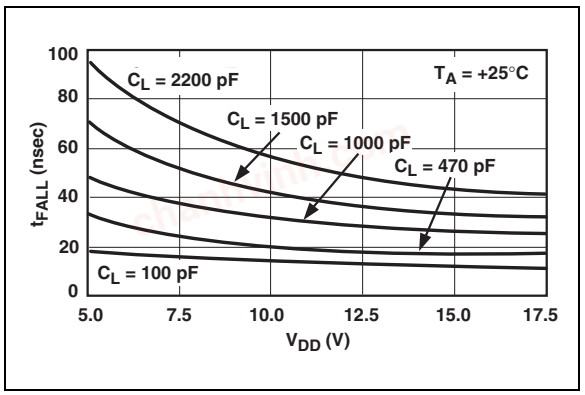


FIGURE 2-4: *Fall Time vs. Supply Voltage.*

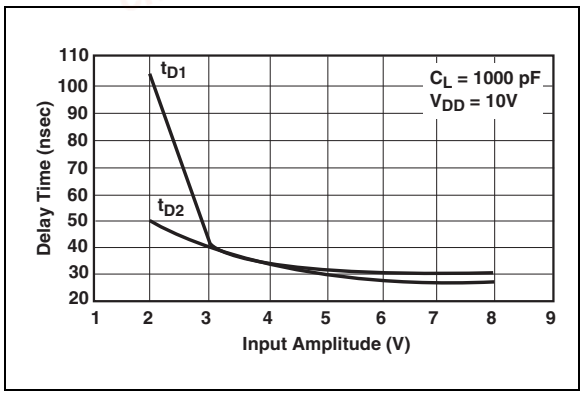


FIGURE 2-2: *Delay Time vs. Input Amplitude.*

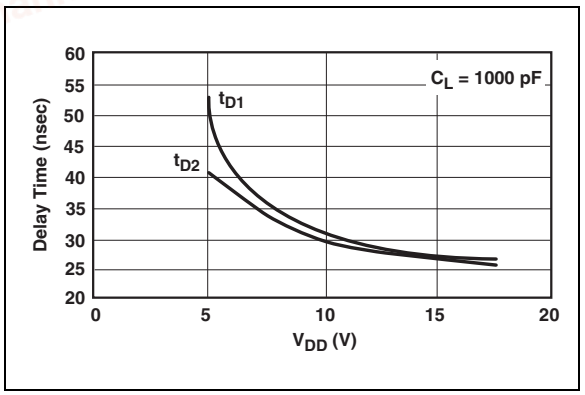


FIGURE 2-5: *Propagation Delay Time vs. Supply Voltage.*

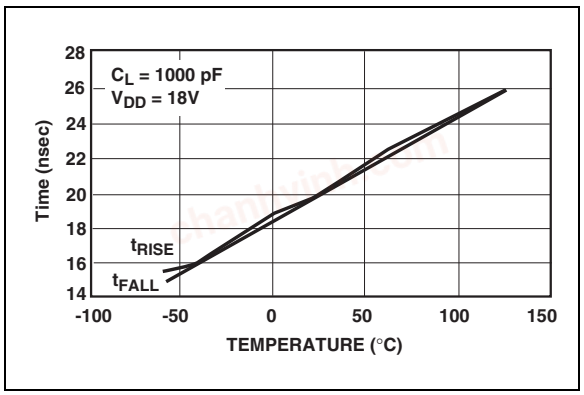


FIGURE 2-3: *Rise and Fall Times vs. Temperature.*

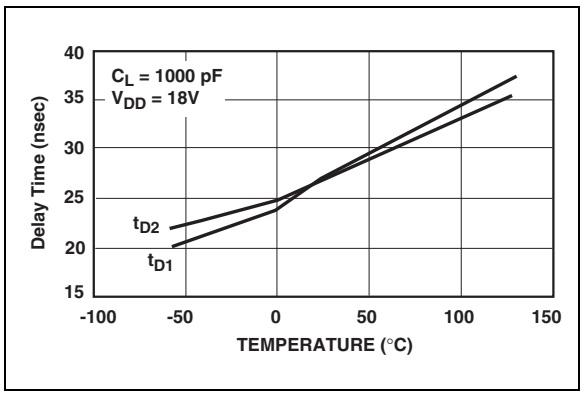


FIGURE 2-6: *Propagation Delay Time vs. Temperature.*

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Note: Unless otherwise indicated, over operating temperature range with $4.5V \leq V_{DD} \leq 18V$.

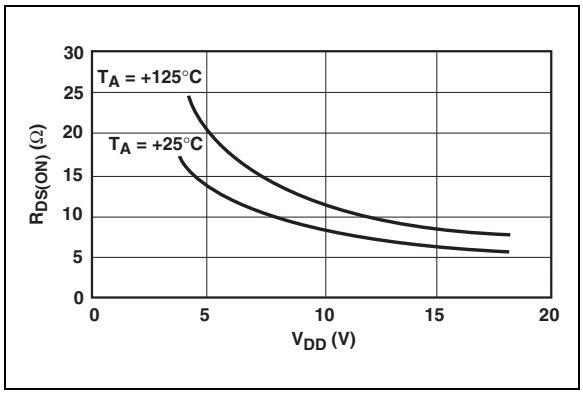


FIGURE 2-7: *High-State Output Resistance.*

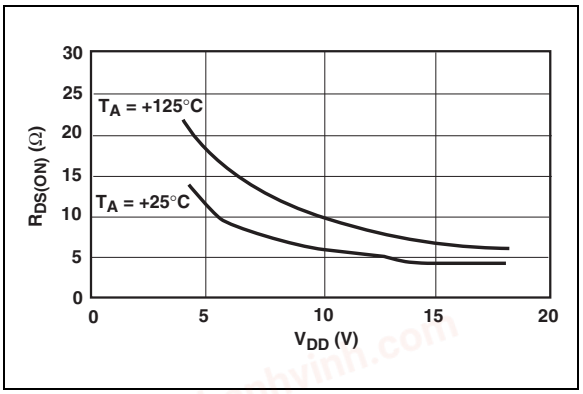


FIGURE 2-10: *Low-State Output Resistance.*

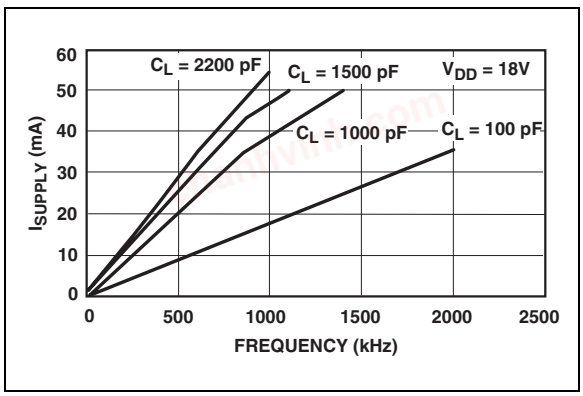


FIGURE 2-8: *Supply Current vs. Frequency.*

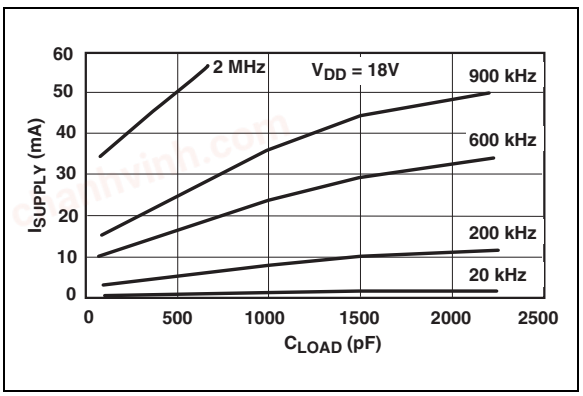


FIGURE 2-11: *Supply Current vs. Capacitive Load.*

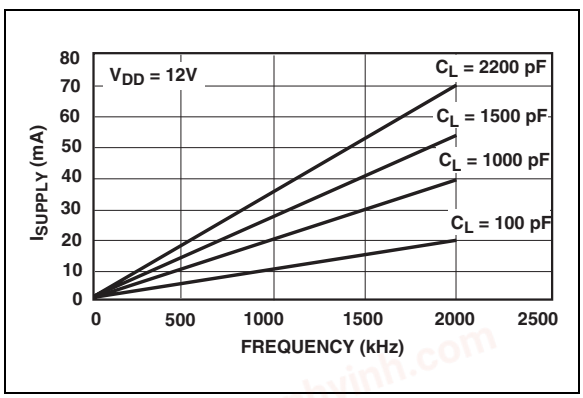


FIGURE 2-9: *Supply Current vs. Frequency.*

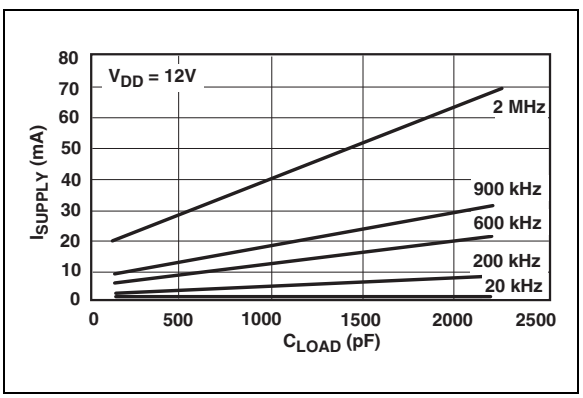


FIGURE 2-12: *Supply Current vs. Capacitive Load.*

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Note: Unless otherwise indicated, over operating temperature range with $4.5V \leq V_{DD} \leq 18V$.

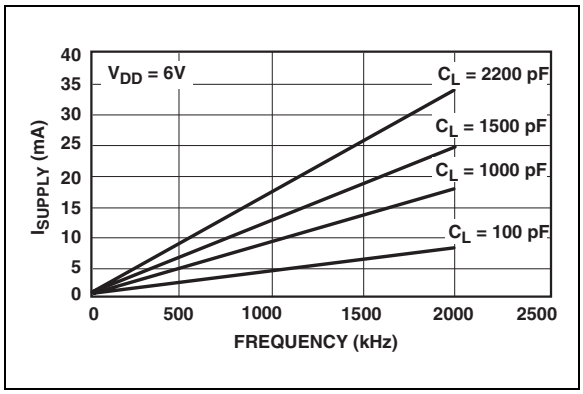


FIGURE 2-13: *Supply Current vs. Frequency.*

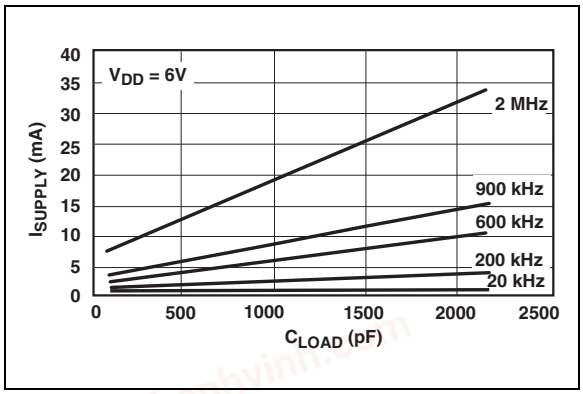


FIGURE 2-15: *Supply Current vs. Capacitive Load.*

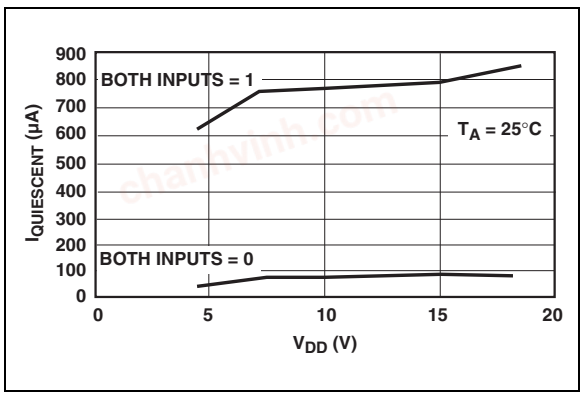


FIGURE 2-14: *Quiescent Supply Current vs. Voltage.*

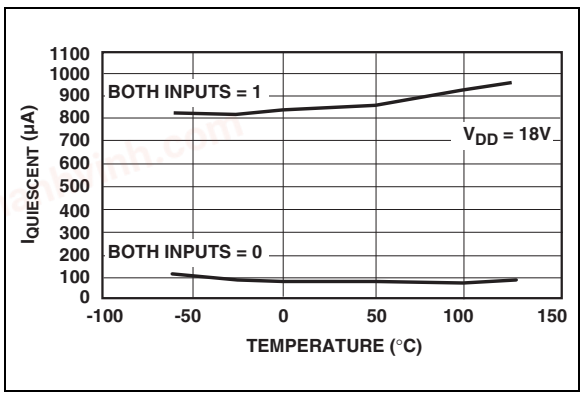


FIGURE 2-16: *Quiescent Supply Current vs. Temperature.*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE (Note 1)

PDIP, MSOP, SOIC	6x5 DFN-S	Symbol	Description
1	1	NC	No connection
2	2	IN A	Input A
3	3	GND	Ground
4	4	IN B	Input B
5	5	OUT B	Output B
6	6	V_{DD}	Supply input
7	7	OUT A	Output A
8	8	NC	No connection
—	9	EP	Exposed Metal Pad

Note 1: Duplicate pins must be connected for proper operation.

3.1 Inputs A and B (IN A, IN B)

MOSFET driver inputs A and B are high-impedance, TTL/CMOS compatible inputs. These inputs also have 300 mV of hysteresis between the high and low thresholds that prevents output glitching, even when the rise and fall time of the input signal is very slow.

3.2 Ground (GND)

The Ground pin is the return path for both the bias current and the high-peak current that discharges the external load capacitance. The Ground pin should be tied into a ground plane or have a very short trace to the bias supply source return.

3.3 Output A and B (OUT A, OUT B)

MOSFET driver outputs A and B are low-impedance, CMOS push-pull style outputs. The pull-down and pull-up devices are of equal strength, making the rise and fall times equivalent.

3.4 Supply Input (V_{DD})

The V_{DD} input is the bias supply for the MOSFET driver and is rated for 4.5V to 18V, with respect to the ground pin. The V_{DD} input should be bypassed with local ceramic capacitors. The value of these capacitors should be chosen based on the capacitive load that is being driven.

3.5 Exposed Metal Pad (EP)

The exposed metal pad of the 6x5 DFN-S package is not internally connected to any potential. Therefore, this pad can be connected to a ground plane or other copper plane on a printed circuit board, to aid in heat removal from the package.

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4.0 APPLICATIONS INFORMATION

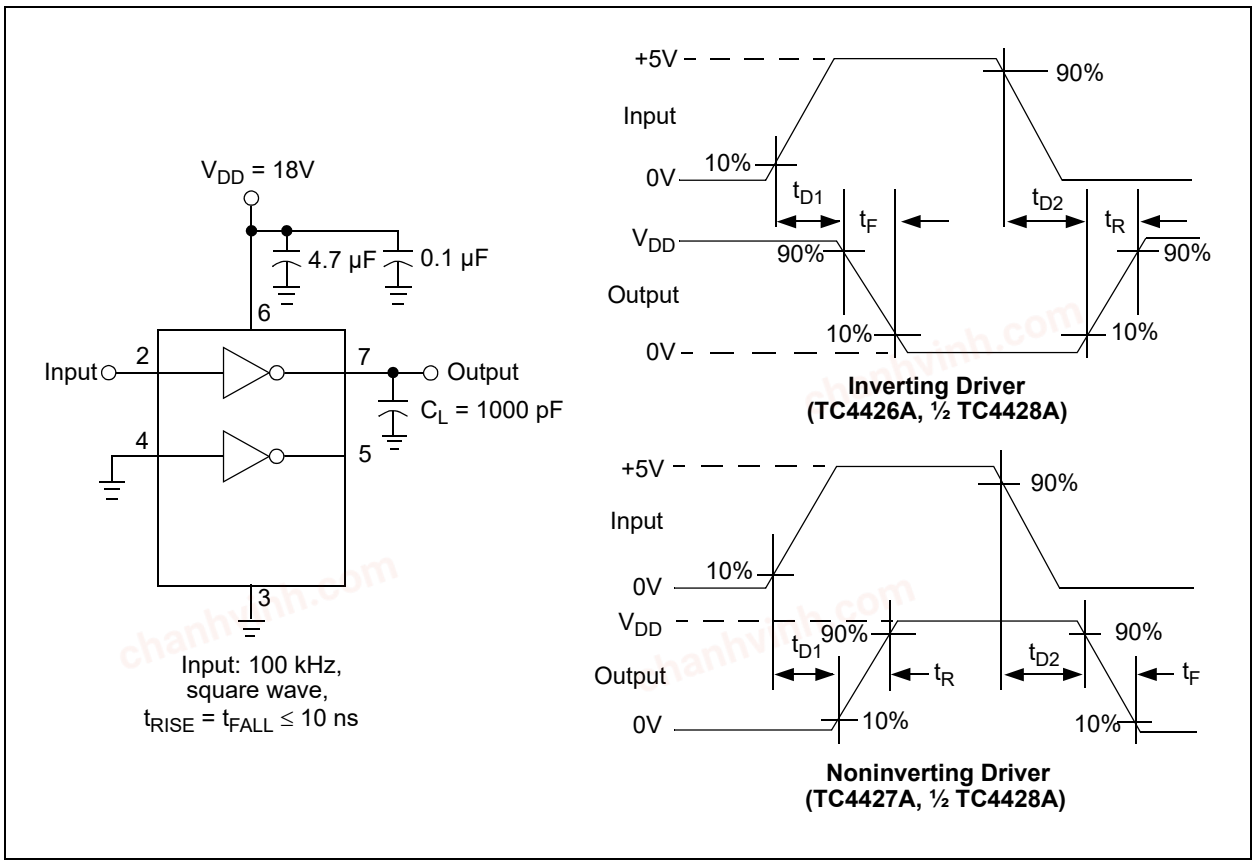


FIGURE 4-1: *Switching Time Test Circuit.*

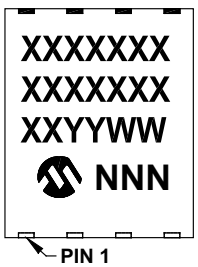
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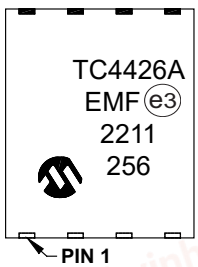
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

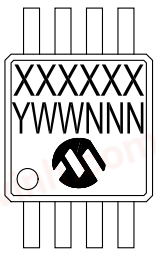
8-Lead DFN-S (6x5x0.9 mm)



Example



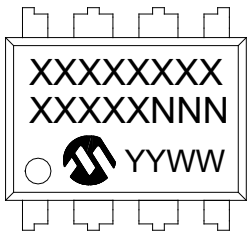
8-Lead MSOP (3x3 mm)



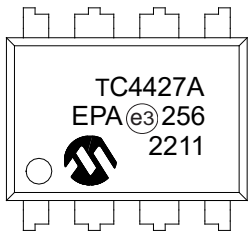
Example



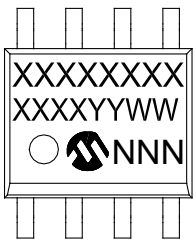
8-Lead PDIP (300 mil)



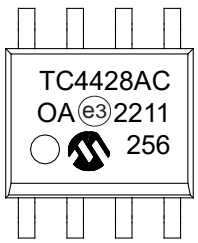
Example



8-Lead SOIC (3.90 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

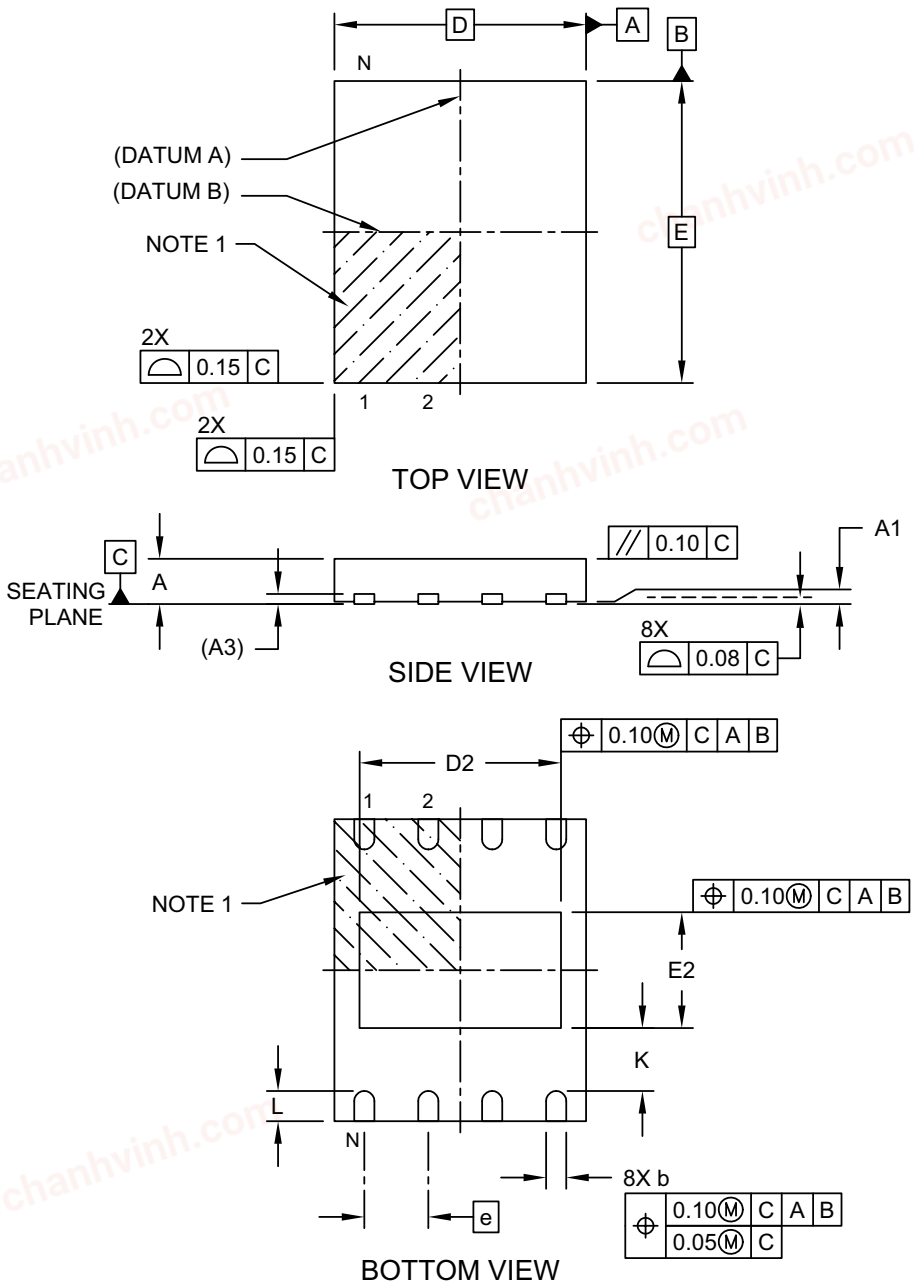
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S]
Saw Singulated

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

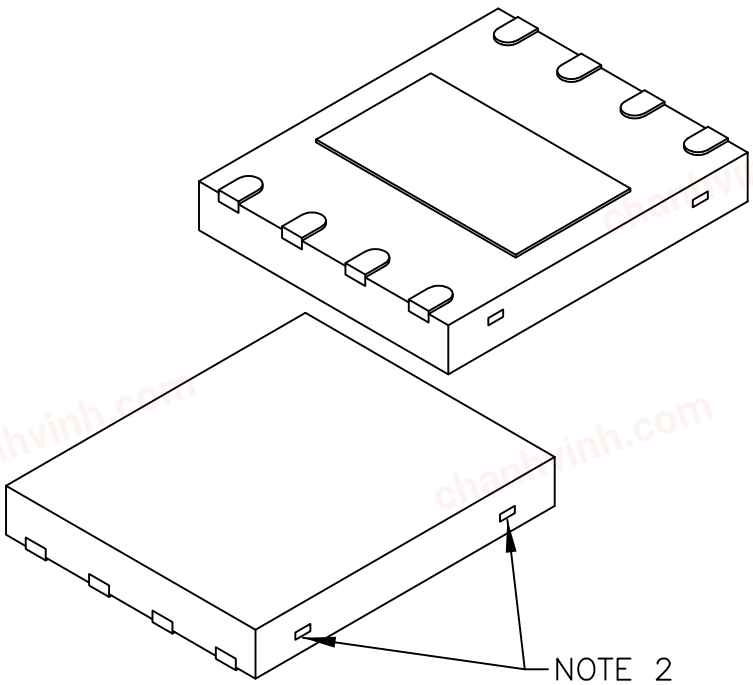


Microchip Technology Drawing C04-122 Rev D Sheet 1 of 2

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8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S] Saw Singulated

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	0.80	0.85	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.90	4.00	4.10
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	2.20	2.30	2.40
Terminal Width	b	0.30	0.40	0.50
Terminal Length	L	0.50	0.60	0.75
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one ore more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

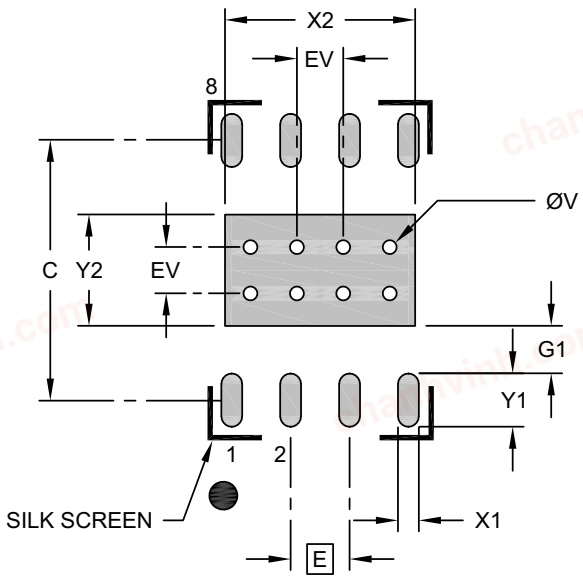
Microchip Technology Drawing C04-122 Rev D Sheet 2 of 2

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8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S]
Saw Singulated

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Optional Center Pad Length	X2			4.10
Optional Center Pad Width	Y2			2.40
Contact Pad Spacing	C		5.60	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.15
Contact Pad to Center Pad (X20)	G1	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

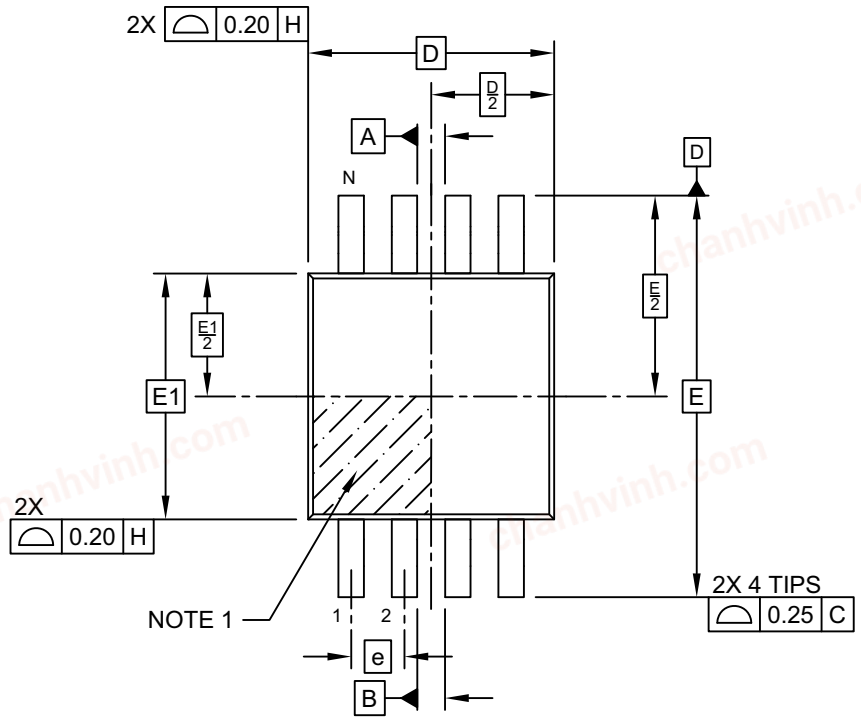
Microchip Technology Drawing C04-2122 Rev D

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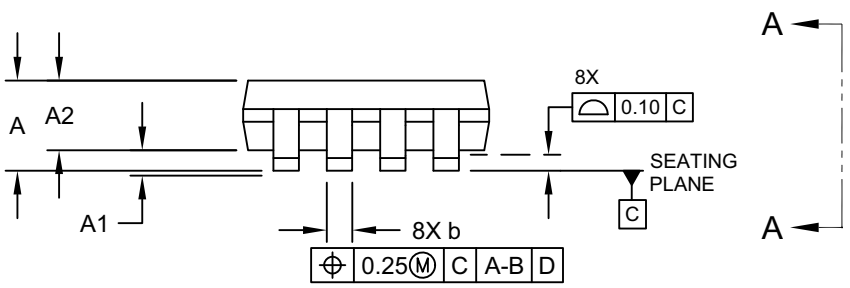
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8-Lead Plastic Micro Small Outline Package (UA) - 3x3 mm Body [MSOP]

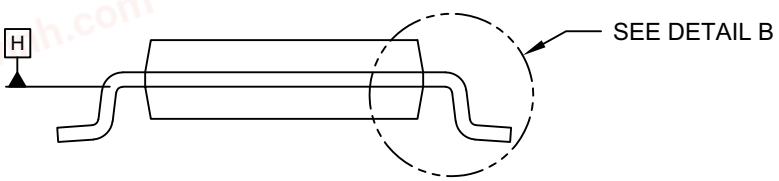
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



VIEW A–A

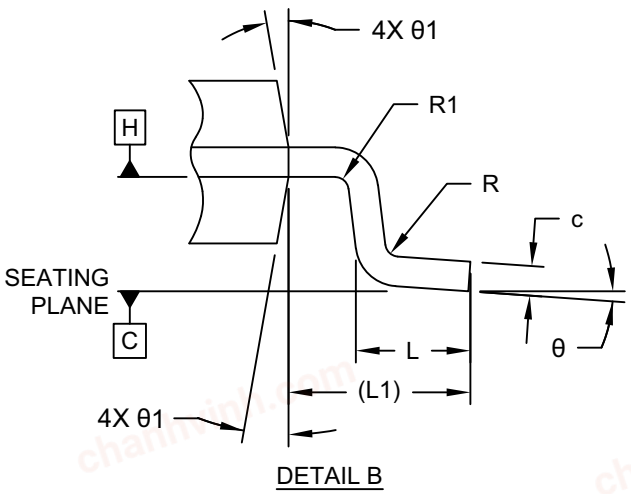
Microchip Technology Drawing C04-111-UA Rev D Sheet 1 of 2

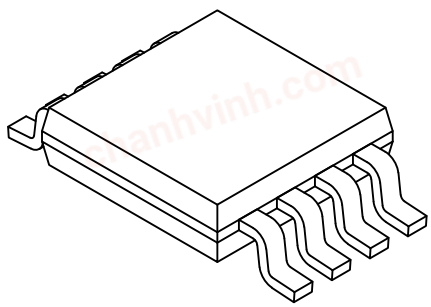
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8-Lead Plastic Micro Small Outline Package (UA) - 3x3 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Standoff	A1	0.00	–	0.15
Molded Package Thickness	A2	0.75	0.85	0.95
Overall Length	D		3.00 BSC	
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Terminal Width	b	0.22	–	0.40
Terminal Thickness	c	0.08	–	0.23
Terminal Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

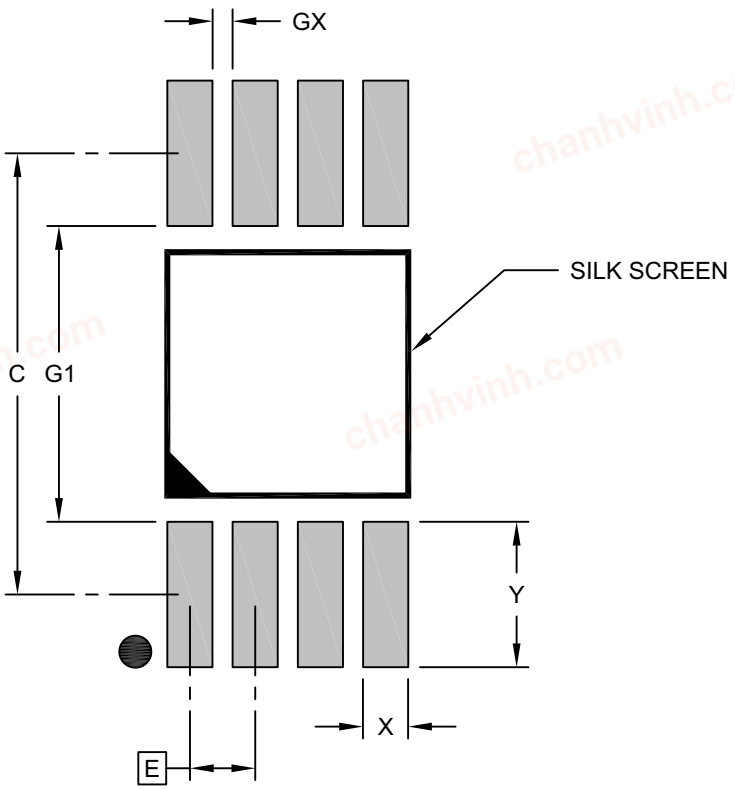
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8-Lead Plastic Micro Small Outline Package (UA) - 3x3 mm Body [MSOP]

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RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		4.40	
Contact Pad Width (X8)	X			0.45
Contact Pad Length (X8)	Y			1.45
Contact Pad to Contact Pad (X4)	G1	2.95		
Contact Pad to Contact Pad (X6)	GX	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

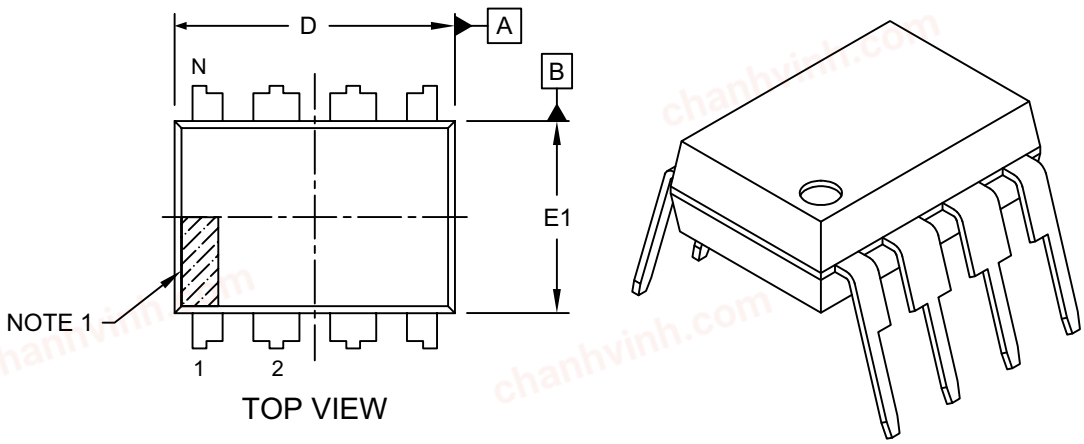
Microchip Technology Drawing C04-2111-UA Rev D

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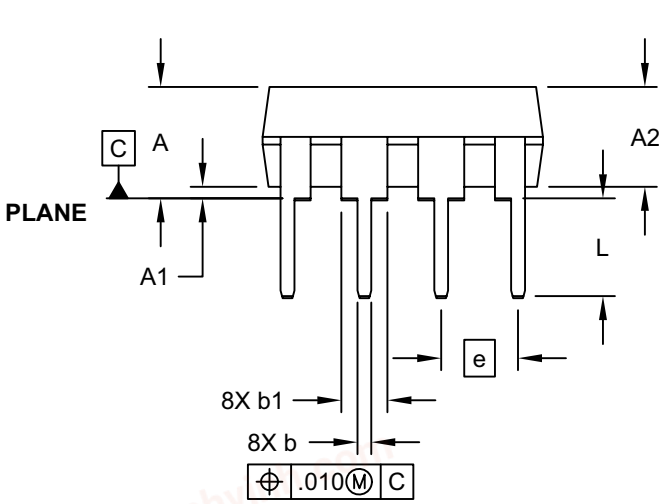
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8-Lead Plastic Dual In-Line (PA) - 300 mil Body [PDIP]

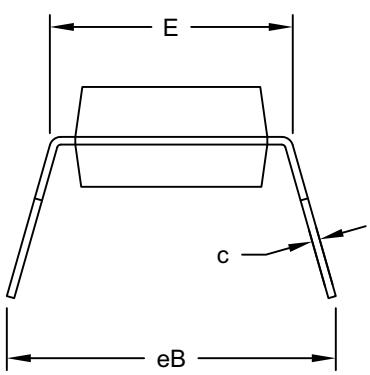
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TOP VIEW



SIDE VIEW



END VIEW

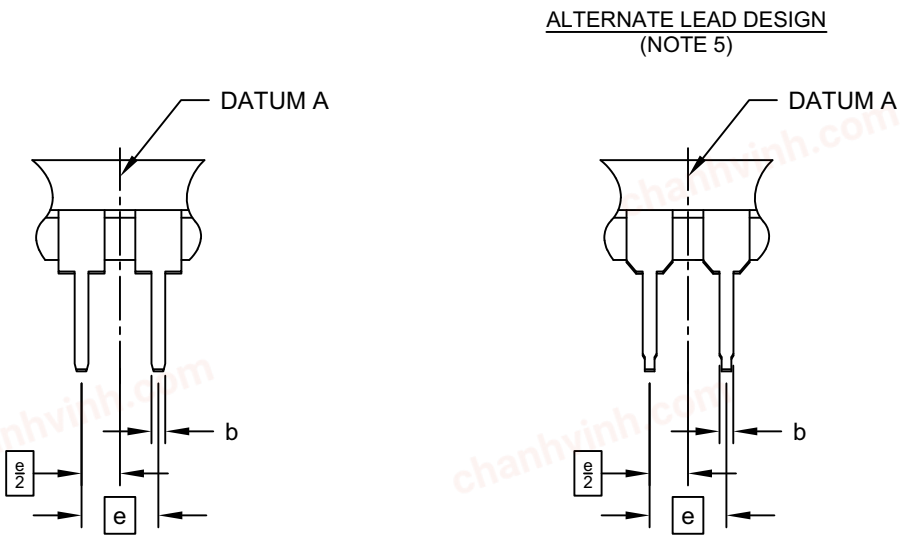
Microchip Technology Drawing No. C04-018-PA Rev F Sheet 1 of 2

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8-Lead Plastic Dual In-Line (PA) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

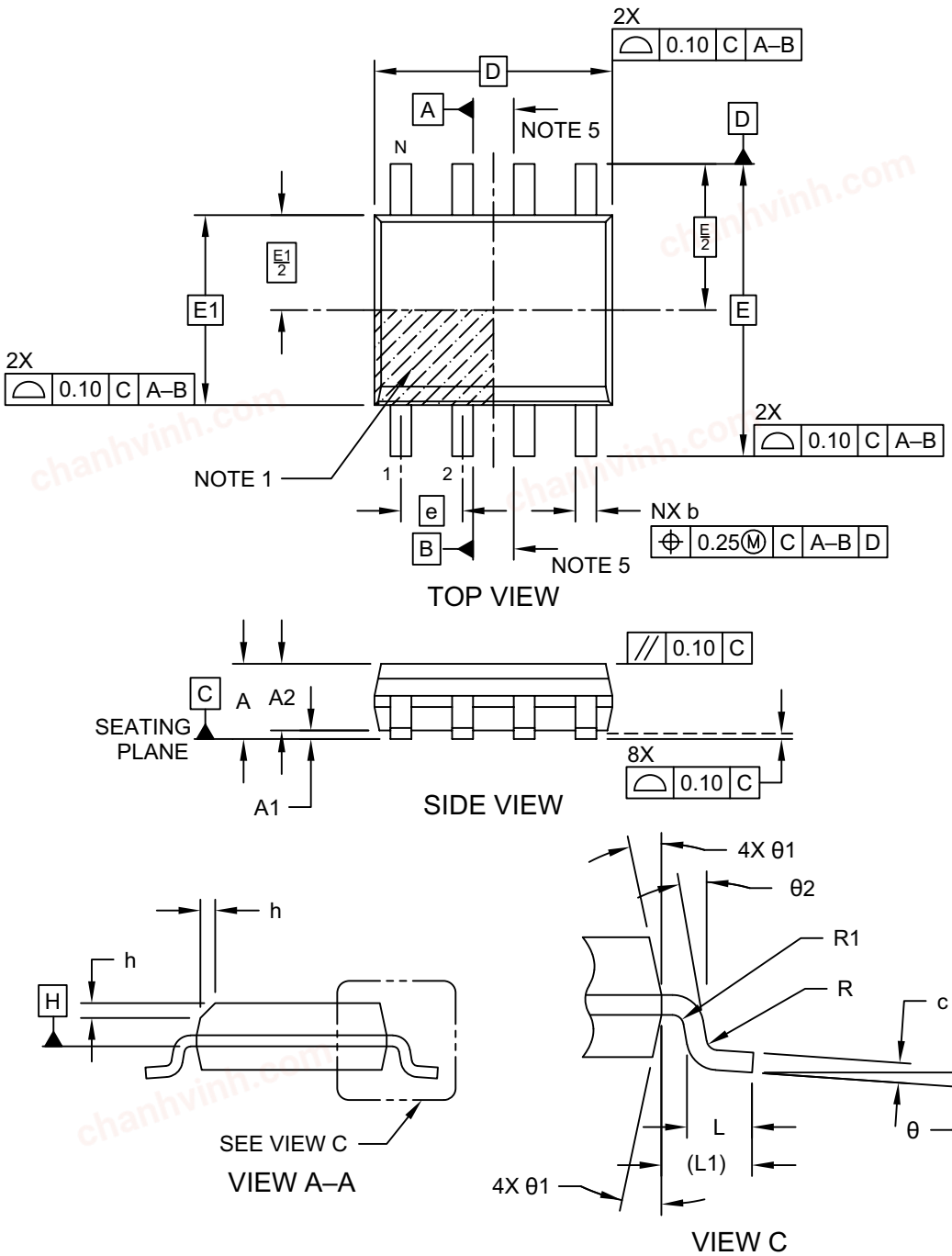
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8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



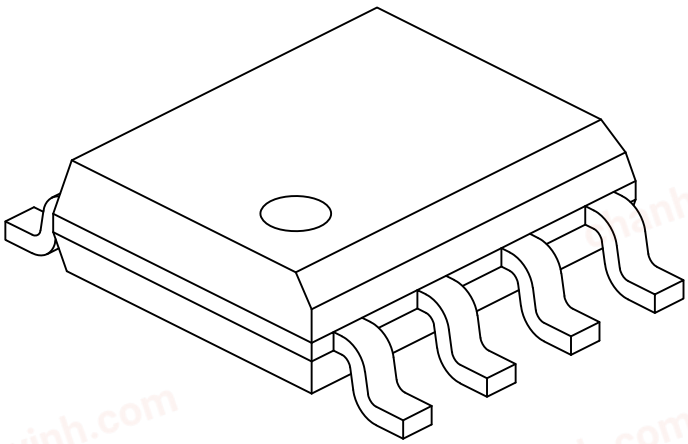
Microchip Technology Drawing No. C04-057-SN Rev J Sheet 1 of 2

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8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	8°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

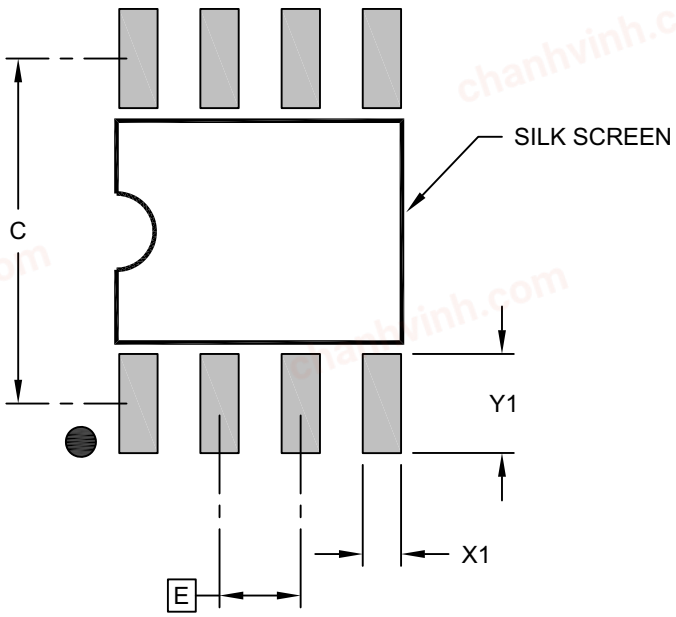
Microchip Technology Drawing No. C04-057-SN Rev J Sheet 2 of 2

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8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev J

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APPENDIX A: REVISION HISTORY

Revision K (November 2022)

- Added information about the Automotive Qualification status of the device in section **Section "Features"**.
- Updated package drawings in **Section 5.0 "Packaging Information"**.
- Updated **Section "Product Identification System"**, with Automotive Qualified devices.
- Minor text and format changes throughout.

Revision J (July 2014)

The following is the list of modifications:

1. Updated Figure 4-1.

Revision H (September 2013)

The following is the list of modifications:

1. Changed ESD protection value to 2 kV on the Features page.
2. Updated the package specification drawings in **Section 5.0 "Packaging Information"**, to show all views available.
3. Minor typographical corrections.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX	XXX(1)	-XXX
Device	Temperature Range	Package	Tape and Reel Option	Qualification

Device:	TC4426A:	1.5A Dual MOSFET Driver, Inverting
	TC4427A:	1.5A Dual MOSFET Driver, Noninverting
	TC4428A:	1.5A Dual MOSFET Driver, Complementary
Temperature Range:	C	= 0°C to +70°C (PDIP & SOIC Only)
	E	= -40°C to +85°C
	V	= -40ºC to +125°C
Package:	MF	= Dual, Flat, No-Lead (6X5 mm Body), 8-Lead
	OA	= Plastic SOIC, (150 mil Body), 8-Lead
	PA	= Plastic DIP (300 mil Body), 8-Lead
	UA	= Plastic Micro Small Outline (MSOP), 8-Lead
Tape and Reel Option:	713	= Tape and Reel
Qualification:	Blank	= Standard Part
	VAO	= Automotive AEC-Q100 Qualified

Examples:

a) TC4426ACOA: 1.5A Dual Inverting MOSFET Driver, 0°C to +70°C, 8-Lead SOIC package

b) TC4426AEOA: 1.5A Dual Inverting MOSFET Driver, -40°C to +85°C, 8-Lead SOIC package

c) TC4426AEMF: 1.5A Dual Inverting MOSFET Driver, -40°C to +85°C, 8-Lead DFN-S package

d) TC4426AVOA713-VAO: 1.5A Dual Inverting MOSFET Driver, -40°C to +125°C, 8-Lead SOIC package, Tape and Reel, Automotive Qualified

a) TC4427ACPA: 1.5A Dual Noninverting MOSFET Driver, 0°C to +70°C, 8-Lead PDIP package 8-Lead PDIP package

b) TC4427AEPA: 1.5A Dual Noninverting MOSFET Driver, -40°C to +85°C, 8-Lead PDIP package

c) TC4427AVMF713: 1.5A Dual Noninverting MOSFET Driver, -40°C to +125°C, 8-Lead DFN-S package, Tape and Reel

d) TC4427AVOA-VAO: 1.5A Dual Noninverting MOSFET Driver, -40°C to +125°C, 8-Lead SOIC package, Automotive Qualified

a) TC4428AEUA: 1.5A Dual Complementary MOSFET Driver, -40°C to +85°C, 8-Lead MSOP package

b) TC4428ACOA713: 1.5A Dual Complementary MOSFET Driver, 0°C to +70°C, 8-Lead SOIC package, Tape and Reel

c) TC4428AVMF: 1.5A Dual Complementary MOSFET Driver, -40°C to +125°C, 8-Lead DFN-S package

d) TC4428AVOA713-VAO: 1.5A Dual Complementary MOSFET Driver, -40°C to +125°C, 8-Lead SOIC package, Tape and Reel, Automotive Qualified

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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