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SST26VF040A

2.5V/3.0V 4-Mbit Serial Quad I/O™ (SQI™) Flash Memory

Features

- Single Voltage Read and Write Operations:
  - 2.7V-3.6V or 2.3V-3.6V
- Serial Interface Architecture:
  - Nibble-wide multiplexed I/O's with SPI-like serial command structure:
    - Mode 0 and Mode 3
  - x1/x2/x4 Serial Peripheral Interface (SPI) Protocol
- High-Speed Clock Frequency:
  - 2.7V-3.6V: 104 MHz maximum (Industrial)
  - 2.3V-3.6V: 80 MHz maximum (Industrial and Extended)
- Burst Modes:
  - Continuous linear burst
  - 8/16/32/64-byte linear burst with wrap-around
- Superior Reliability:
  - Endurance: 100,000 cycles (minimum)
  - Greater than 100 years data retention
- Low-Power Consumption:
  - Active Read current: 15 mA (typical @ 104 MHz)
  - Standby Current: 15 µA (typical)
- Fast Erase Time:
  - Sector/Block Erase: 20 ms (typical), 25 ms (maximum)
  - Chip Erase: 40 ms (typical), 50 ms (maximum)
- Page-Program:
  - 256 bytes per page in x1 or x4 mode
- End-of-Write Detection:
  - Software polling the BUSY bit in STATUS register
- Flexible Erase Capability:
  - Uniform 4-Kbyte sectors
  - Uniform 32-Kbyte overlay blocks
  - Uniform 64-Kbyte overlay blocks
- Write-Suspend:
  - Suspend program or erase operation to access another block/sector
- Software Reset (RST) mode
- Software Write Protection:
  - Write protection through Block Protection bits in STATUS register
- Security ID:
  - One-Time-Programmable (OTP) 2-Kbyte Secure ID:
    - 128-bit unique, factory preprogrammed identifier
    - User-programmable area
- Temperature Range:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C
- Automotive AEC-Q100 Qualified
- Packages Available:
  - 8-contact WDFN (6 mm x 5 mm)
  - 8-lead SOIC (3.90 mm)
- All Devices are RoHS Compliant

Product Description

The Serial Quad I/O™ (SQI™) family of Flash memory devices features a six-wire, 4-bit I/O interface that allows for low-power, high-performance operation in a low pin count package. SST26VF040A also supports full command-set compatibility to traditional Serial Peripheral Interface (SPI) protocol. System designs using SQI Flash devices occupy less board space and ultimately lower system costs.

All members of the 26 Series, SQI family are manufactured with proprietary, high-performance CMOS SuperFlash® technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches.

SST26VF040A significantly improves performance and reliability, while lowering power consumption. These devices write (Program or Erase) with a single-power supply of 2.3V-3.6V. The total energy consumed is a function of the applied voltage, current and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any erase or program operation is less than alternative Flash memory technologies.

See Figure 2-1 for pin assignments.

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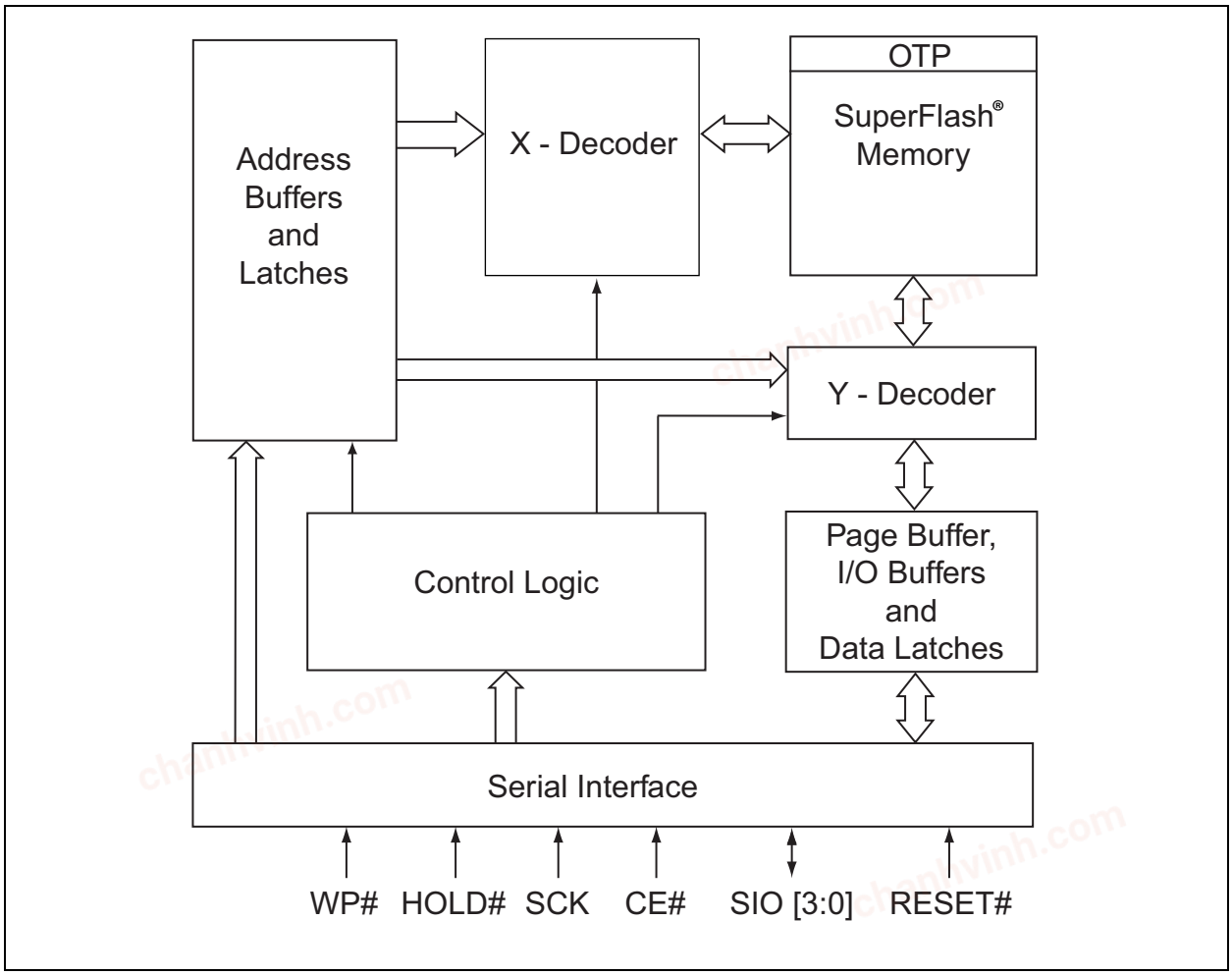
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1.0 BLOCK DIAGRAM

FIGURE 1-1: FUNCTIONAL BLOCK DIAGRAM



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2.0 PIN DESCRIPTION

FIGURE 2-1: PIN DESCRIPTIONS

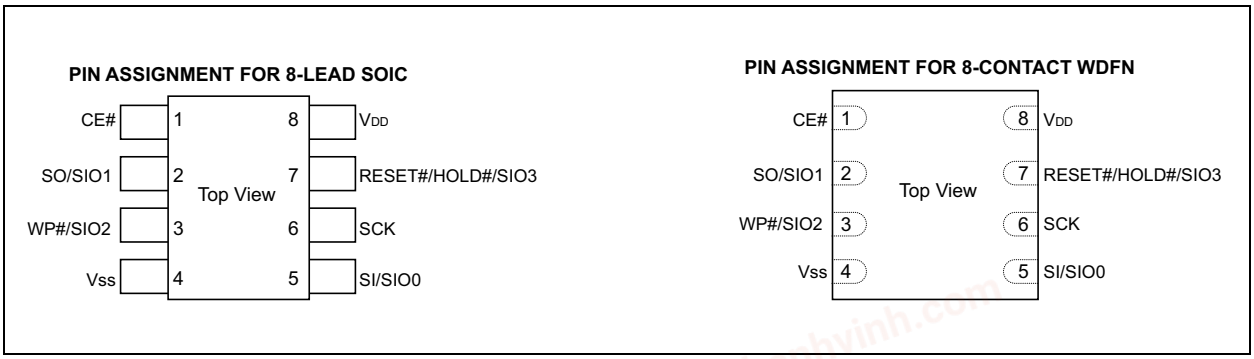


TABLE 2-1: PIN DESCRIPTION

Symbol	Pin Name	Functions
SCK	Serial Clock	Provide the timing of the serial interface. Commands, addresses, or input data are latched on the rising edge of the clock input, while output data is shifted out on the falling edge of the clock input.
SIO[3:0]	Serial Data Input/Output	Transfer commands, addresses, or data serially into the device or data out of the device. Inputs are latched on the rising edge of the serial clock. Data is shifted out on the falling edge of the serial clock. The Enable Quad I/O (EQIO) command instruction configures these pins for Quad I/O mode.
SI	Serial Data Input for SPI mode	Transfer commands, addresses or data serially into the device. Inputs are latched on the rising edge of the serial clock. SI is the default state after a Power-on Reset or hardware Reset.
SO	Serial Data Output for SPI mode	Transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock. SO is the default state after a Power-on Reset or hardware Reset.
CE#	Chip Enable	The device is enabled by a high-to-low transition on CE#. CE# must remain low for the duration of any command sequence; or in the case of write operations, for the command/data input sequence.
WP#	Write-Protect	The WP# pin is used in conjunction with the WPEN and IOC bits in the Configuration register to prohibit write operations to the Block Protection register. This pin only works in SPI, single-bit and dual-bit Read mode.
HOLD#	Hold	Temporarily stops serial communication with the SPI Flash memory while the device is selected. This pin only works in SPI, single-bit and dual-bit Read mode and must be tied high when not in use.
RESET#	Reset	Reset the operation and internal logic of the device.
VDD	Power Supply	Provide power supply voltage.
VSS	Ground	

Note: The exposed pad on the bottom side of WDFN package is internally not connected. It can externally be soldered to ground for better device attachment to the board.

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3.0 MEMORY ORGANIZATION

The SST26VF040A SQI memory array is organized in uniform, 4-Kbyte erasable sectors with the following erasable blocks: with 32-Kbyte overlay erasable blocks and 64-Kbyte overlay erasable blocks.

4.0 DEVICE OPERATION

SST26VF040A supports both Serial Peripheral Interface (SPI) bus protocol and a 4-bit multiplexed SQI bus protocol. To provide backward compatibility to traditional SPI Serial Flash devices, the device's initial state after a Power-on Reset is SPI mode which supports multi-I/O (x1/x2/x4) read/write commands. A command instruction configures the device to SQI mode. The dataflow in the SQI mode is similar to the SPI mode, except it uses four multiplexed I/O signals for command, address, and data sequence.

SQI Flash memory supports both Mode 0 (0,0) and Mode 3 (1,1) bus operations. The difference between the two modes is the state of the SCK signal when the bus host is in Standby mode and no data is being transferred. The SCK signal is low for Mode 0 and SCK signal is high for Mode 3. For both modes, the Serial Data I/O (SIO[3:0]) is sampled at the rising edge of the SCK clock signal for input, and driven after the falling edge of the SCK clock signal for output. The traditional SPI protocol uses separate input (SI) and output (SO) data signals as shown in Figure 4-1. The SQI protocol uses four multiplexed signals, SIO[3:0], for both data in and data out, as shown in Figure 4-2. This means the SQI protocol quadruples the traditional bus transfer speed at the same clock frequency, without the need for more pins on the package.

FIGURE 4-1: SPI PROTOCOL (TRADITIONAL 25 SERIES SPI DEVICE)

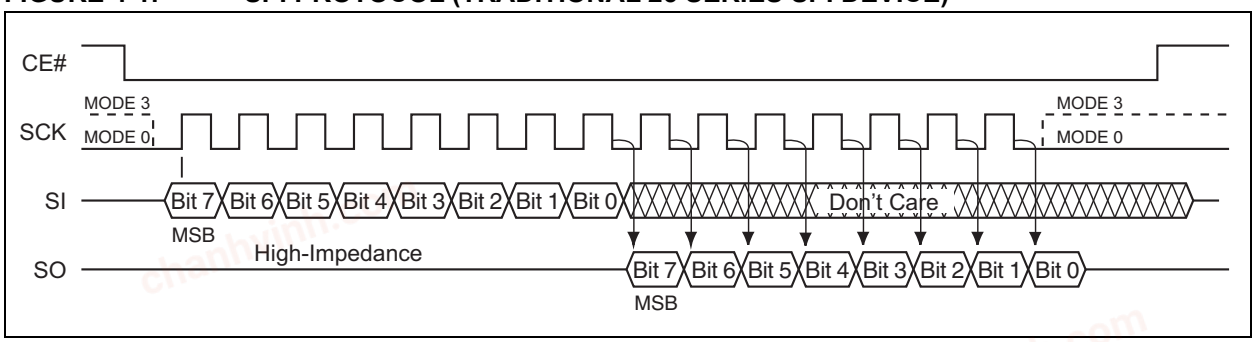
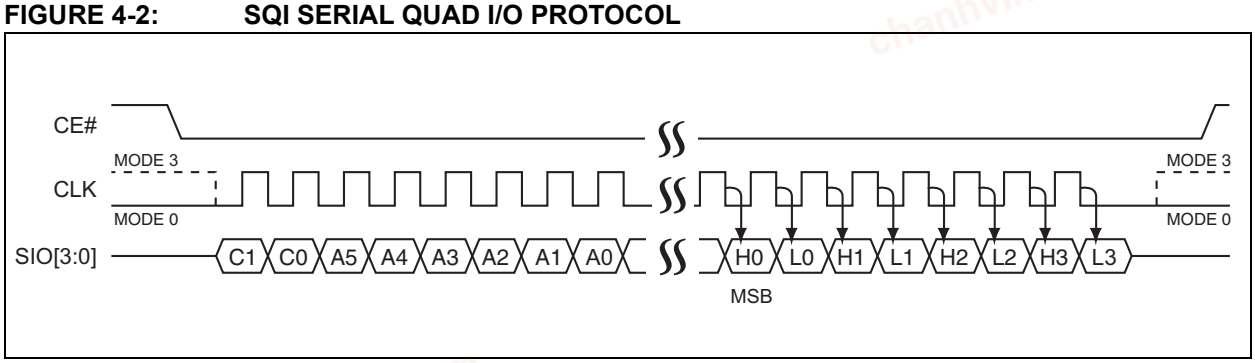


FIGURE 4-2: SQI SERIAL QUAD I/O PROTOCOL



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4.1 Device Protection

SST26VF040A offers a software write protection scheme that allows group protection of selected blocks in memory array. The Write Protection Pin (WP#) enables or disables the lock-down (BPL bit) of the STATUS register. In addition, the Lock-Down Protection Settings command also prevents any changes to the block protection setting (BP0, BP1 and BP2) during device operation. To avoid inadvertent writes during power-up, the device is write-protected by default after a Power-on Reset cycle.

4.1.1 GROUP BLOCK PROTECTION

The Block Protection bits (BP0, BP1, BP2, and BPL) in the STATUS register provide write protection to the memory array and the STATUS register. See Table 4-4 for the Block Protection description.

4.1.2 VOLATILE LOCK PROTECTION

To prevent changes to the Block Protection settings, use the Lock-Down Protection Settings (LDPS) command to enable Volatile Lock Protection. Once Volatile Lock Protection is enabled, the Block Protection settings cannot be changed. To avoid inadvertent lock-down, the WREN command must be executed prior to the LDPS command. To reset Volatile Lock Protection, performing a hardware Reset or power cycle on the device is required. The Volatile Lock Protection status may be read from the Configuration register.

4.2 Hardware Write Protection

The hardware Write Protection pin (WP#) is used in conjunction with the WPEN and IOC bits in the Configuration register to enable the lock-down function of the BPL bit (bit 7) in the STATUS register and the Configuration register. The WP# pin function only works in SPI Single-Bit and Dual-Bit Read mode when the IOC bit in the Configuration register is set to '0'. The WP# pin function is disabled when the WPEN bit in the Configuration register is '0'. This allows installation of the device in a system with a grounded WP# pin while still enabling write to the BP bits in the STATUS register.

The factory default setting at power-up of the WPEN bit is '0', disabling the Write-Protect function of the WP# pin after power-up. WPEN is a nonvolatile bit; once the bit is set to '1', the Write-Protect function of the WP# pin continues to be enabled after power-up. The WP# pin only protects the BPL bit in the STATUS register and Configuration register from changes. Therefore, if the WP# pin is set to low while an internal write is in progress, it will have no effect on the write command. The IOC bit takes priority over the WPEN bit in the Configuration register. When the IOC bit is '1', the function of the WP# pin is disabled and the WPEN bit serves no function. When WP# is driven low and IOC bit = 0, the execution of the Write STATUS Register (WRSR) instruction to change the BP bits in the STATUS register is determined by the value of the BPL bit (see Table 4-1). When WP# is high, the lock-down function of the BPL bit is disabled.

TABLE 4-1: WRITE PROTECTION LOCK-DOWN STATES

VLP	WP#	IOC	WPEN	BPL	WRSR Instruction to Change BP0, BP1, BP2, BP3 Bits in STATUS Register	WRSR Instruction to Change Configuration Register
0	L	0	0	X	Allowed	Allowed
0	L	0	1	0	Allowed	Not Allowed
0	L	0	1	1	Not Allowed	Not Allowed
0	L	1	X	X	Allowed	Allowed
0	H	X	X	X	Allowed	Allowed
1	L	0	0	X	Not Allowed	Allowed
1	L	0	1	X	Not Allowed	Not Allowed
1	L	1	X	X	Not Allowed	Allowed
1	H	X	X	X	Not Allowed	Allowed

Note: X = "Don't care"

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4.3 Security ID

SST26VF040A offers a 2-Kbyte Security ID (Sec ID) feature. The Security ID space is divided into two parts: one factory-programmed, 128-bit segment, and one user-programmable segment.
The factory-programmed segment is programmed during part manufacture with a unique number and cannot be changed. The user-programmable segment is left unprogrammed for the customer to program as desired.

Use the Program Security ID (PSID) command to program the Security ID using the address shown in Table 5-5. The Security ID can be locked using the Lockout Security ID (LSID) command. This prevents any future write operations to the Security ID.

The factory-programmed portion of the Security ID can not be programmed by the user; neither the factory-programmed nor user-programmable areas can be erased.

4.4 Hold Operation

The HOLD# pin pauses active serial sequences without resetting the clocking sequence. **This pin is active after every power-up and only operates during SPI Single-bit and Dual-bit modes**.

SST26VF040A ships with the IOC bit set to '0' and the HOLD# pin function enabled. The HOLD# pin is always disabled in SQI mode and only works in SPI Single-bit and Dual-bit Read mode.

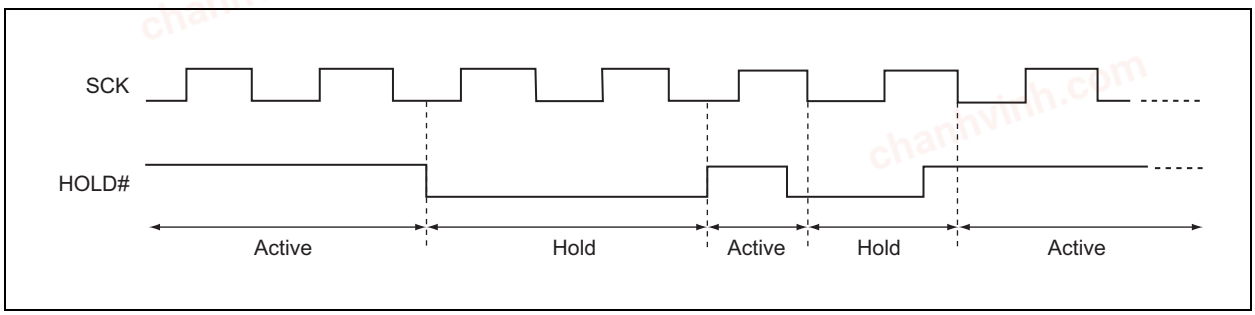
To activate the Hold mode, CE# must be in active-low state. The Hold mode begins when the SCK active-low state coincides with the falling edge of the HOLD# signal. The Hold mode ends when the HOLD# signal's rising edge coincides with the SCK active-low state.

If the falling edge of the HOLD# signal does not coincide with the SCK active-low state, then the device enters Hold mode when the SCK next reaches the active-low state. Similarly, if the rising edge of the HOLD# signal does not coincide with the SCK active-low state, then the device exits Hold mode when the SCK next reaches the active-low state. See Figure 4-3.

Once the device enters Hold mode, SO will be in high-impedance state while SI and SCK can be VIL or VIH.

If CE# is driven active-high during a Hold condition, it resets the internal logic of the device. As long as HOLD# signal is low, the memory remains in the Hold condition. To resume communication with the device, HOLD# must be driven active-high, and CE# must be driven active-low.

FIGURE 4-3: HOLD CONDITION WAVEFORM



4.5 Reset Operation

If the RST#/HOLD#SIO3 pin is used as a Reset pin, RST# pin provides a hardware method for resetting the device. SST26VF040A supports both hardware and software Reset operation. Hardware Reset is only allowed using SPI x1 and x2 protocol. Software Reset commands 66H and 99H are supported in all protocols. See Table 4-2 and for Figure 4-4 for hardware and software Reset functionality.

Note:	A device Reset during an active program or erase operation aborts the operation and data of the targeted address range may be corrupted or lost due to the aborted erase or program operation.

Depending on the prior operation, the Reset timing may vary. Recovery from a write operation requires more latency time than recovery from other operations.

4.5.1 HARDWARE RESET OPERATION

To configure the RESET#/HOLD#/SIO3 pin as a RESET# pin, bit 6 of the Configuration register must be set to '1'. The factory default setting of bit 6 is '0'-HOLD# pin enabled. This is a nonvolatile bit, so the register value at power-up will be the value prior to power-down. Driving the RESET# pin high puts the device in normal operating mode. The RESET# pin must be driven low for a minimum of TRST time to reset the device. The SIO1 pin (SO) is in high-impedance state while the device is in Reset. A successful Reset operation will reset the protocol to SPI mode, STATUS register bits will become as follows: BUSY = 0, WEL = 0, BP0 = 1, BP1 = 1, BP2 = 1 and BPL = 0; reset the burst length to 8 bytes. Reset during an active program or erase operation aborts the operation and data of the targeted address range may be corrupted or lost due to the aborted erase or program operation.

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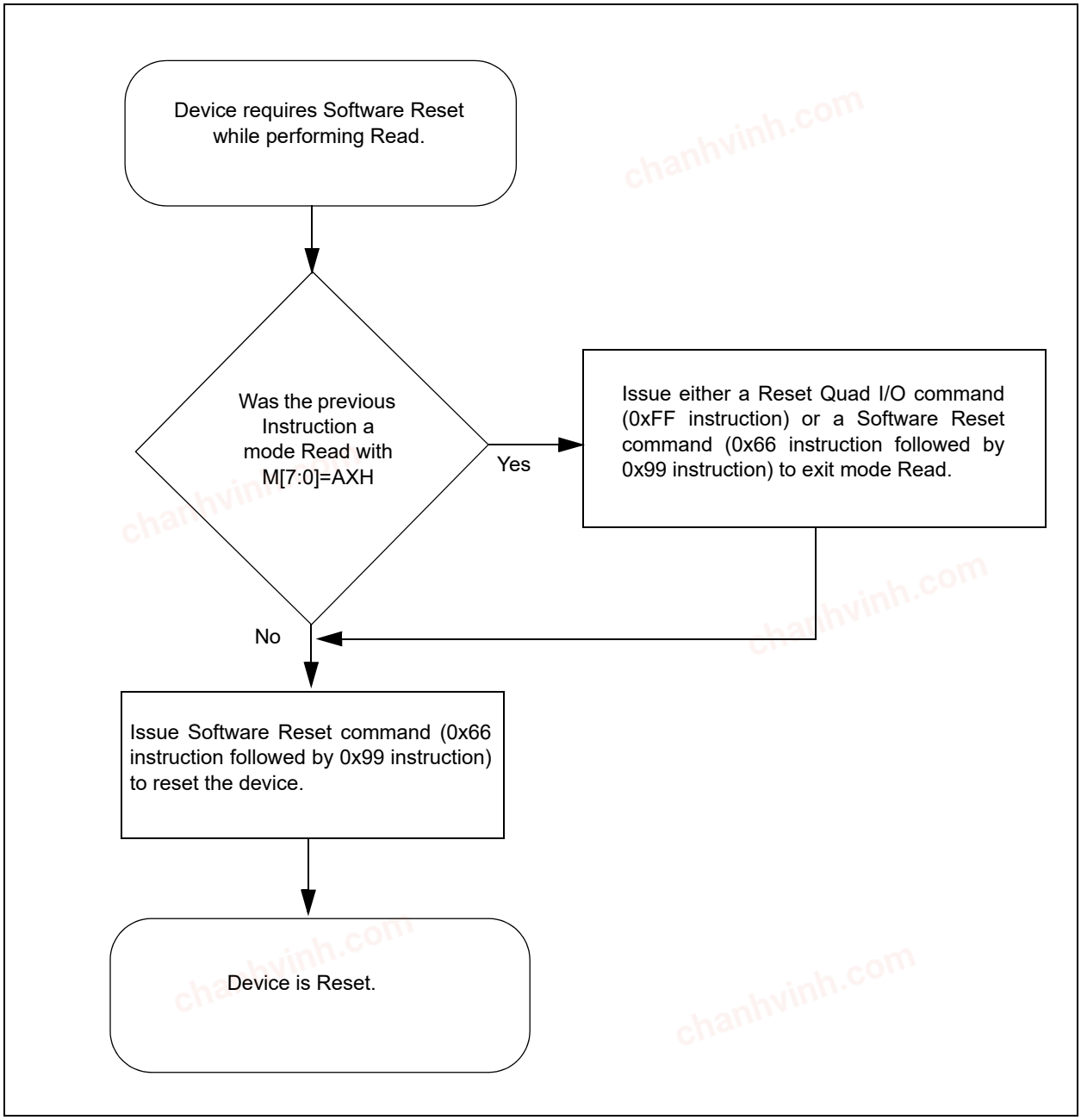
4.5.2 SOFTWARE RESET OPERATION

The Reset operation requires the Reset Enable command, 66H, followed by the Reset command, 99H.

Note:	Any command other than the Reset command after the Reset Enable command will disable the Reset Enable.

Once the Reset Enable and Reset commands are successfully executed, the device returns to normal operation Read mode and then does the following: resets the protocol to SPI mode, resets the burst length to 8 bytes, STATUS register bits BUSY = 0, WEL = 0; and clears bit 1 (IOC) in the Configuration register to its default state.

FIGURE 4-4: PERFORMING SOFTWARE RESET DURING READ



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TABLE 4-2: REGISTER SETTINGS AFTER HARDWARE AND SOFTWARE RESET

	After Power Cycle	After Hardware Reset	After Software Reset
Status Register Bits			
Busy Bit	0	0	0
WEL Bit	0	0	0
BP0 Bit	1	1	Unchanged
BP1 Bit	1	1	Unchanged
BP2 Bit	1	1	Unchanged
BPL Bit	0	0	Unchanged
Configuration Register Bits			
IOC Bit	0	0	0
VLP Bit	0	0	Unchanged
SEC Bit	Unchanged	Unchanged	Unchanged
WSE Bit	0	0	0
WSP Bit	0	0	0
RSTHLD Bit	Unchanged	Unchanged	Unchanged
WPEN Bit	Unchanged	Unchanged	Unchanged

4.6 STATUS Register

The software STATUS register provides status on whether the Flash memory array is available for any read or write operation, whether the device is write-enabled, and the state of the memory write protection. During an internal erase or program operation, the STATUS register may be read only to determine the completion of an operation in progress. Table 4-3 describes the function of each bit in the software STATUS register.

TABLE 4-3: SOFTWARE STATUS REGISTER

Bit	Name	Function	Default at Power-Up	Read/Write
0	BUSY	1 = Internal write operation is in progress 0 = No internal write operation is in progress	0	R
1	WEL	1 = Device is memory write-enabled 0 = Device is not memory write-enabled	0	R
2	BP0	Indicate current level of block write protection (see Table 4-4)	1	R/W
3	BP1	Indicate current level of block write protection (see Table 4-4)	1	R/W
4	BP2	Indicate current level of block write protection (see Table 4-4)	1	R/W
5	BP3	Indicate current level of block write protection (see Table 4-4)	0	R/W
6	RES	Reserved	0	R
7	BPL	1 = BP3, BP2, BP1, BP0 are read-only bits 0 = BP3, BP2, BP1, BP0 are read/writable	0	R/W

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4.6.1 BUSY

The BUSY bit determines whether there is an internal erase or program operation in progress. A '1' for the BUSY bit indicates the device is busy with an operation in progress. A '0' indicates the device is ready for the next valid operation.

4.6.2 WRITE ENABLE LATCH (WEL)

The Write Enable Latch bit indicates the status of the internal memory Write Enable Latch. If the Write Enable Latch bit is set to '1', it indicates the device is write-enabled. If the bit is set to '0' (Reset), it indicates the device is not write-enabled and does not accept any memory write (program/erase) commands. The Write Enable Latch bit is automatically reset under the following conditions:

- Power-Up
- Write Disable (WRDI) instruction completion
- Page Program instruction completion
- Sector Erase instruction completion
- Block Erase instructions (32-Kbyte and 64-Kbyte) completion
- Chip Erase instruction completion
- Write STATUS Register instruction completion
- Software or hardware Reset
- Lock-Down Protection Setting instruction completion
- Program Security ID instruction completion
- Lockout Security ID instruction completion
- Write-Suspend instruction
- SPI Quad Page program instruction completion

4.6.3 BLOCK PROTECTION (BP3, BP2, BP1, BP0)

The Block Protection (BP3, BP2, BP1, BP0) bits define the size of the memory area, as defined in Table 4-4, to be software-protected against any memory write (program or erase) operations.

The Write STATUS Register (WRSR) instruction is used to program the BP3, BP2, BP1 and BP0 bits as long as WP# pin is high or the Block Protect Lock (BPL) bit is '0'. Chip Erase can only be executed if Block Protection bits are '0'. After power-up, BP3, BP2, BP1 and BP0 are set to defaults specified in Table 4-4.

4.6.4 BLOCK PROTECTION LOCK-DOWN (BPL)

WP# pin driven low (V_{IL}), IO bit = 0 and WPEN bit = 1 enable the Block Protection Lock-Down (BPL) bit. When BPL is set to '1', it prevents any further alteration of the BPL, BP3, BP2, BP1, and BP0 bits. When the WP# pin is driven high (V_{IH}), the BPL bit has no effect and its value is "don't care". After power-up and hardware Reset, the BPL bit is reset to '0'.

TABLE 4-4: SOFTWARE STATUS REGISTER BLOCK PROTECTION

Protected Level	STATUS Register Bit				Protected Memory Address
	BP3	BP2	BP1	BP0	8 Mbit
None	X	0	0	0	None
Upper 1/8	X	0	0	1	70000H-7FFFFH
Upper 1/4	X	0	1	0	60000H-7FFFFH
Upper 1/2	X	0	1	1	40000H-7FFFFH
All	X	1	0	0	00000H-7FFFFH
All	X	1	0	1	00000H-7FFFFH
All	X	1	1	0	00000H-7FFFFH
All	X	1	1	1	00000H-7FFFFH

Note 1: X = "Don't care" (Reserved) default is '0'.

2: Default at power-up for BP3, BP2, BP1 and BP0 is '0111'.

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4.7 Configuration Register

The Configuration register is a Read/Write register that stores a variety of configuration information. See Table 4-5 for the function of each bit in the register.

TABLE 4-5: CONFIGURATION REGISTER

Bit	Name	Function	Default at Power-Up	Read/Write (R/W)
0	Reserved			R
1	IOC	I/O Configuration 1 = WP# and RST# or HOLD# pins disabled 0 = WP# and RST# or HOLD# pins enabled	0(1)	R/W
2	VLP	Volatile Lock Protection 1 = Locks Protection bit setting of BP0, BP1, BP2, BP3 of STATUS register 0 = Protection bit BP0, BP1, BP2, BP3 setting not locked by VLP bit	0(1)	R
3	SEC	Security ID Status 1 = Security ID space locked 0 = Security ID space not locked	0(2)	R
4	WSE	Write Suspend Erase Status 1 = Erase suspended 0 = Erase is not suspended	0	R
5	WSP	Write Suspend Program Status 1 = Program suspended 0 = Program is not suspended	0	R
6	RSTHLD	RST# pin or HOLD# Pin Enable 1 = RST# pin enabled 0 = HOLD# pin enabled	0(3)	R/W
7	WPEN	Write Protection Pin (WP#) Enable 1 = WP# enabled 0 = WP# disabled	0(3)	R/W

Note 1: Default at power-up or after hardware Reset is '0'.

2: The Security ID status will always be '1' at power-up after a successful execution of the Lockout Security ID instruction, otherwise default at power-up is '0'.

3: Factory default setting. This is a nonvolatile bit, default at power-up will be the setting prior to power-down.

4.7.1 I/O CONFIGURATION (IOC)

The I/O Configuration (IOC) bit reconfigures the I/O pins. The IOC bit is set by writing a '1' to Bit 1 of the Configuration register. When IOC bit is '0' the WP# pin and HOLD# pin or RST# pin are enabled (SPI or Dual configuration setup). When the IOC bit is set to '1' the SIO2 and SIO3 pins are enabled (SPI Quad I/O configuration setup). The IOC bit must be set to '1' before issuing the following SPI commands: SQOR (6BH), SQIOR (EBH), SPI Quad page program (32H) and RBSPI (ECH). Without setting the IOC bit to '1', those SPI commands are not valid. The I/O Configuration bit does not apply when in SQI mode. The default at power-up and after hardware/software Reset is '0'.

4.7.2 VOLATILE LOCK PROTECTION (VLP)

The Volatile Lock Protection (VLP) bit is a volatile bit which is set to '1' when a lock-down protection settings (LDPS) command is executed. When VLP bit is set to '1', it locks the protection bit BP0, BP1, BP2, BP3 settings of the STATUS register. The VLP bit can be cleared to '0' only by performing a hardware Reset or by performing a power cycle.

4.7.3 SECURITY ID STATUS (SEC)

The Security ID Status (SEC) bit indicates when the Security ID space is locked to prevent a write command. The SEC bit is '1' after the host issues a Lockout SID command. Once the host issues a Lockout SID command, the SEC bit can never be reset to '0'.

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4.7.4 WRITE SUSPEND ERASE STATUS (WSE)

The Write Suspend Erase status (WSE) indicates when an erase operation is suspended. The WSE bit is '1' after the host issues a suspend command during an erase operation. Once the suspended erase resumes, the WSE bit is reset to '0'.

4.7.5 WRITE SUSPEND PROGRAM STATUS (WSP)

The Write Suspend Program status (WSP) bit indicates when a program operation is suspended. The WSP is '1' after the host issues a suspend command during the program operation. Once the suspended program operation resumes, the WSP bit is reset to '0'.

4.7.6 RESET/HOLD ENABLE (RSTHLD)

The Reset/Hold Enable (RSTHLD) bit is a nonvolatile bit that configures the RST#/HOLD#/SIO3 pin to be either the RST# pin or the Hold# pin when not configured as an I/O. There is latency associated with writing to the RSTHLD bit. Poll the BUSY bit in the STATUS register or wait TCONFIG for the completion of the internal, self-timed write operation.

4.7.7 WRITE-PROTECT ENABLE (WPEN)

The Write-Protect Enable (WPEN) bit is a nonvolatile bit that enables the WP# pin. The Write-Protect (WP#) pin and the Write-Protect Enable (WPEN) bit control the programmable hardware write-protect feature. Setting the WP# pin to low, and the WPEN bit to '1', enables hardware write protection. To disable hardware write protection, set either the WP# pin to high or the WPEN bit to '0'. There is latency associated with writing to the WPEN bit. Poll the BUSY bit in the STATUS register or wait TCONFIG for the completion of the internal, self-timed write operation. When the chip is hardware write-protected, only write operations to the BPL bit in the STATUS register and Configuration register are disabled. See **Section 4.2 "Hardware Write Protection"** and Table 4-1 for more information about the functionality of the WPEN bit.

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5.0 INSTRUCTIONS

Instructions are used to read, write (erase and program), and configure the SST26VF040A. The complete list of the instructions is provided in Table 5-1.

TABLE 5-1: DEVICE OPERATION INSTRUCTIONS

Instruction	Description	Op Code Cycle(1)	Mode		Address Cycle(s)(2,3)	Dummy Cycle(s)(3)	Data Cycle(s)(3)	Maximum Frequency (4)
			SPI	SQI				
Configuration								
NOP	No Operation	00H	X	X	0	0	0	104 MHz/80 MHz
RSTEN	Reset Enable	66H	X	X	0	0	0	
RST	Reset Memory	99H	X	X	0	0	0	
EQIO	Enable Quad I/O	38H	X		0	0	0	
RSTQIO	Reset Quad I/O	FFH	X	X	0	0	0	
RDSR(5)	Read STATUS Register	05H	X		0	0	1 to ∞	
				X	0	1	1 to ∞	
WRSR	Write STATUS Register	01H	X	X	0	0	1 to 2	
RDCR	Read Configuration Register	35H	X		0	0	1 to ∞	
				X	0	1	1 to ∞	
Read								
READ	Read Memory	03H	X		3	0	1 to ∞	40 MHz
High-Speed Read	Read Memory at Higher Speed	0BH	X		3	1	1 to ∞	104 MHz/80 MHz
				X	3	3	1 to ∞	
SDOR(6)	SPI Dual Output Read	3BH	X		3	1	1 to ∞	
SDIOR (7,8)	SPI Dual I/O Read	BBH	X		3	1	1 to ∞	80 MHz
SQOR (9)	SPI Quad Output Read	6BH	X		3	1	1 to ∞	104 MHz/80 MHz
SQIOR (10)	SPI Quad I/O Read	EBH	X		3	3	1 to ∞	
SB	Set Burst Length	C0H	X	X	0	0	1	
RBSQI	SQI nB Burst with Wrap	0CH		X	3	3	n to ∞	
RBSPI	SPI nB Burst with Wrap	ECH	X		3	3	n to ∞	
Identification								
JEDEC ID	JEDEC® ID Read	9FH	X		0	0	3 to ∞	104 MHz/80 MHz
Quad J-ID	Quad I/O J-ID Read	AFH		X	0	1	3 to ∞	
SFDP	Serial Flash Discoverable Parameters	5AH	X		3	1	1 to ∞	

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TABLE 5-1: DEVICE OPERATION INSTRUCTIONS (CONTINUED)

Instruction	Description	Op Code Cycle[1]	Mode		Address Cycle(s)[2,3]	Dummy Cycle(s)[3]	Data Cycle(s)[3]	Maximum Frequency [4]
			SPI	SQI				
Write								
WREN	Write Enable	06H	X	X	0	0	0	104 MHz/80 MHz
WRDI	Write Disable	04H	X	X	0	0	0	
4-Kbyte Sector Erase[11]	Erase 4 Kbyte of Memory Array	20H	X	X	3	0	0	
32-Kbyte Block Erase[12]	Erase 32 Kbyte of Block Memory Array	52H	X	X	3	0	0	
64-Kbyte Block Erase[13]	Erase 64 Kbyte of Block Memory Array	D8H	X	X	3	0	0	
Chip Erase	Erase Full Memory Array	60H or C7H	X	X	0	0	0	
Page Program	To Program 1 to 256 Data Bytes	02H	X	X	3	0	1 to 256	
SPI Quad PP[9]	SPI Quad Page Program	32H	X		3	0	1 to 256	
WRSU	Suspends Program/Erase	B0H	X	X	0	0	0	
WRRE	Resume Program/Erase	30H	X	X	0	0	0	
Protection								
LDPS	Lock-Down Protection Settings	8DH	X	X	0	0	0	104 MHz/80 MHz
RSID	Read Security ID	88H	X		2	1	1 to 1024	
				X	2	3	1 to 1024	
PSID	Program User Security ID Area	A5H	X	X	2	0	1 to 256	
LSID	Lockout Security ID Programming	85H	X	X	0	0	0	

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TABLE 5-1: DEVICE OPERATION INSTRUCTIONS (CONTINUED)

Instruction	Description	Op Code Cycle[1]	Mode		Address Cycle(s)[2,3]	Dummy Cycle(s)[3]	Data Cycle(s)[3]	Maximum Frequency [4]
			SPI	SQI				
Power-Saving								
DPD	Deep Power-Down Mode	B9H	X	X	0	0	0	104 MHz/80 MHz
RDPD	Release from Deep Power-Down and Read ID	ABH	X	X	3	0	1 to ∞	

Note 1: Command cycle is two clock periods in SQI mode and eight clock periods in SPI mode.
2: Address bits above the Most Significant bit of each density can be VIL or VIH.
3: Address, Dummy/Mode bits, and data cycles are two clock periods in SQI and eight clock periods in SPI mode.
4: The maximum frequency for all instructions is up to 104 MHz from 2.7V-3.6V and up to 80 MHz from 2.3V-3.6V unless otherwise noted. For extended temperature (125°C) the maximum frequency is up to 80 MHz.
5: The Read STATUS register is continuous with ongoing clock cycles until terminated by a low-to-high transition on CE#.
6: Data cycles are four clock periods.
7: The maximum frequency for SDIOR is up to 80 MHz from 2.3V-3.6V.
8: Address, Dummy/Mode bits, and data cycles are four clock periods.
9: Data cycles are two clock periods. IOC bit must be set to '1' before issuing the command.
10: Address, Dummy/Mode bits, and data cycles are two clock periods. IOC bit must be set to '1' before issuing the command.
11: 4-Kbyte Sector Erase addresses: use AMS-A12, remaining addresses are "don't care" but must be set either at VIL or VIH.
12: 32-Kbyte Block Erase addresses: use AMS-A15, remaining addresses are "don't care" but must be set either at VIL or VIH.
13: 64-Kbyte Block Erase addresses: use AMS-A16, remaining addresses are "don't care" but must be set either at VIL or VIH.

5.1 No Operation (NOP)

The No Operation command only cancels a Reset Enable command. NOP has no impact on any other command.

5.2 Reset Enable (RSTEN) and Reset (RST)

The Reset operation is used as a system (software) Reset that puts the device in normal operating Ready mode. This operation consists of two commands: Reset Enable (RSTEN) followed by Reset (RST).

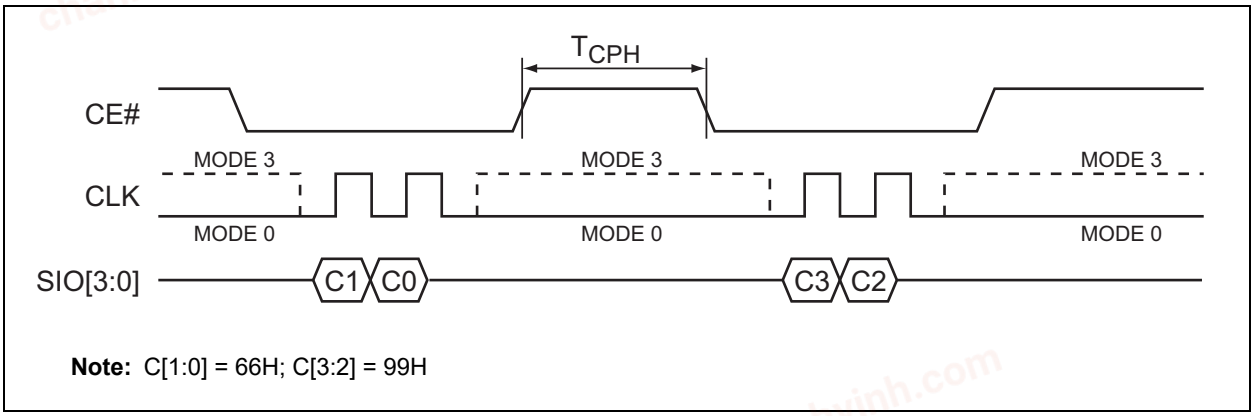
To reset SST26VF040A, the host drives CE# low, sends the Reset Enable command (66H), and drives CE# high. Next, the host drives CE# low again, sends the Reset command (99H), and drives CE# high, see Figure 5-1.

The Reset operation requires the Reset Enable command followed by the Reset command. Any command other than the Reset command after the Reset Enable command will disable the Reset Enable.

Once the Reset Enable and Reset commands are successfully executed, the device returns to normal operation Read mode and then does the following: resets the protocol to SPI mode, resets the burst length to 8 bytes, clears BUSY bit and WEL bit in the STATUS register to their default states, and clears IOC bit, WSE bit and WSP bit in the Configuration register to its default state. A device Reset during an active program or erase operation aborts the operation, which can cause the data of the targeted address range to be corrupted or lost. Depending on the prior operation, the Reset timing may vary. Recovery from a write operation requires more latency time than recovery from other operations. See Table 8-2 for Reset timing parameters.

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FIGURE 5-1: RESET SEQUENCE



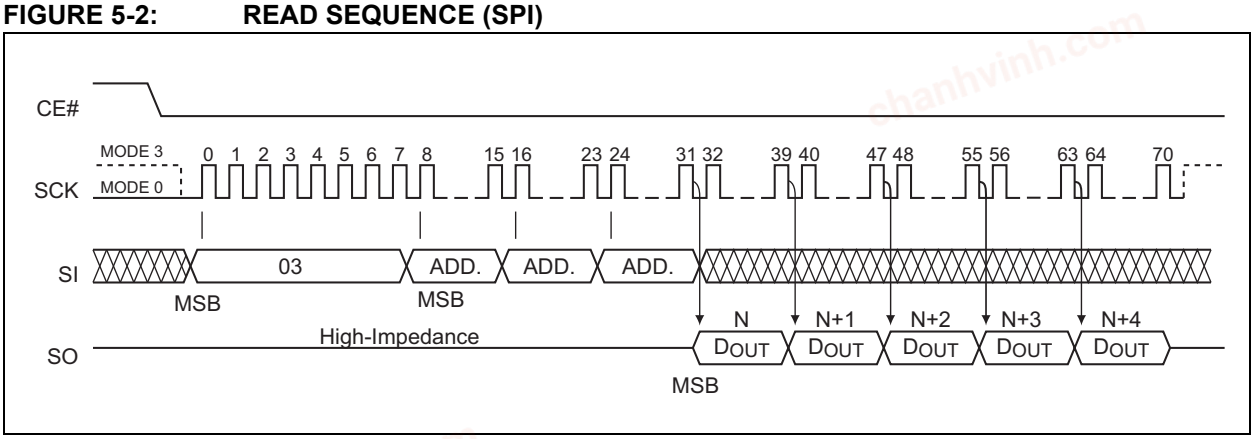
Note: C[1:0] = 66H; C[3:2] = 99H

5.3 Read (40 MHz)

The READ instruction, 03H, is supported in SPI bus protocol only with clock frequencies up to 40 MHz.
This command is not supported in SQI bus protocol. The device outputs the data starting from the specified address location, then continuously streams the data output through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the Address Pointer will automatically return to the beginning (wrap-around) of the address space.

Initiate the READ instruction by executing an 8-bit command, 03H, followed by address bits A[23:0]. CE# must remain active-low for the duration of the Read cycle. See Figure 5-2 for the Read sequence.

FIGURE 5-2: READ SEQUENCE (SPI)

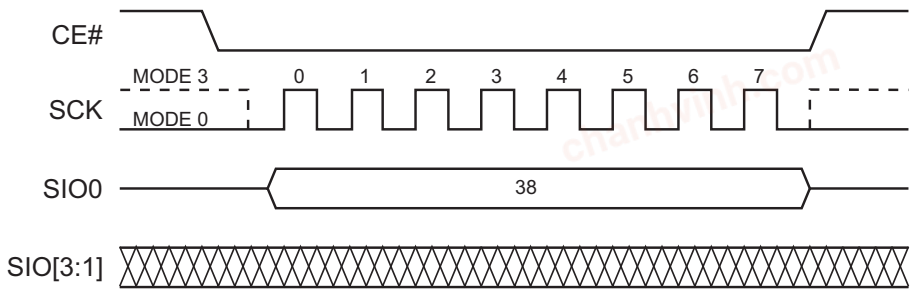


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5.4 Enable Quad I/O (EQIO)

The Enable Quad I/O (EQIO) instruction, 38H, enables the Flash device for SQI bus operation. Upon completion of the instruction, all instructions thereafter are expected to be 4-bit multiplexed input/output (SQI mode) until a power cycle or a Reset Quad I/O instruction is executed. See Figure 5-3.

FIGURE 5-3: ENABLE QUAD I/O SEQUENCE



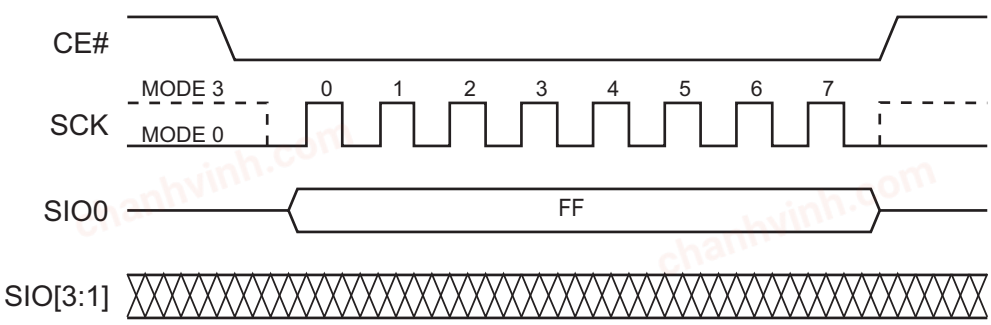
Note: SIO[3:1] must be driven VIH.

5.5 Reset Quad I/O (RSTQIO)

The Reset Quad I/O instruction, FFH, resets the device to 1-bit SPI protocol operation or exits the Set Mode configuration during a read sequence. This command allows the Flash device to return to the default I/O state (SPI) without a power cycle, and executes in either 1-bit or 4-bit mode. If the device is in the Set Mode configuration, while in SQI High-Speed Read mode, the RSTQIO command will only return the device to a state where it can accept new command instruction. An additional RSTQIO is required to reset the device to SPI mode.

To execute a Reset Quad I/O operation, the host drives CE# low, sends the Reset Quad I/O command cycle (FFH) then drives CE# high. Execute the instruction in either SPI (8 clocks) or SQI (2 clocks) command cycles. For SPI, SIO[3:1] are “don’t care” for this command, but should be driven to VIH or VIL. See Figures 5-4 and 5-5.

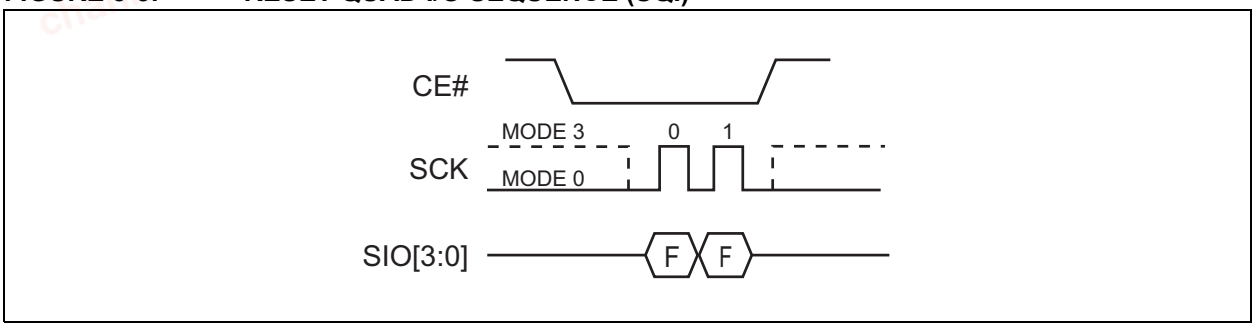
FIGURE 5-4: RESET QUAD I/O SEQUENCE (SPI)



Note: SIO[3:1] must be driven VIH.

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FIGURE 5-5: RESET QUAD I/O SEQUENCE (SQI)

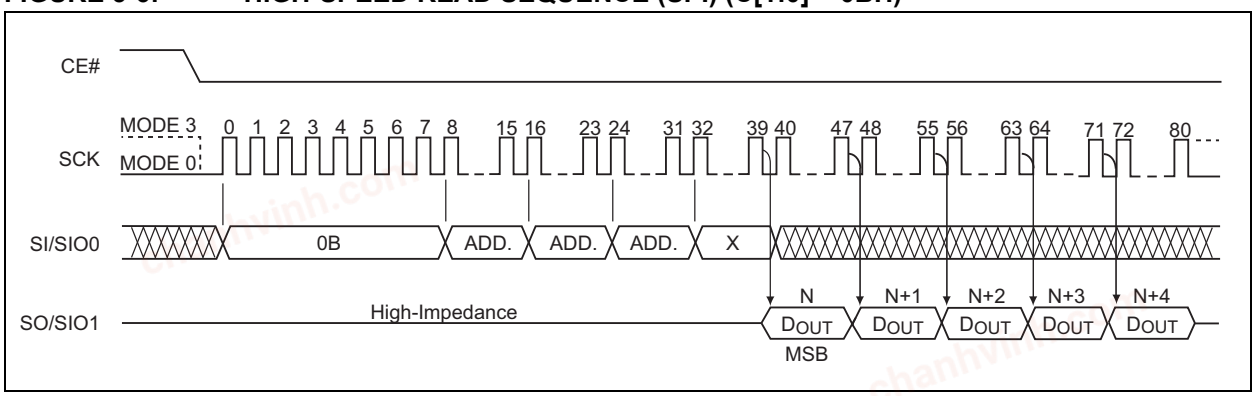


5.6 High-Speed Read

The High-Speed Read instruction, 0BH, is supported in both SPI bus protocol and SQI protocol. This instruction supports frequencies of up to 104 MHz from 2.7V-3.6V and up to 80 MHz from 2.3V-3.6V. On power-up, the device is set to use SPI.

Initiate High-Speed Read by executing an 8-bit command, 0BH, followed by address bits A[23:0] and a dummy byte. CE# must remain active-low for the duration of the High-Speed Read cycle. See Figure 5-6 for the High-Speed Read sequence for SPI bus protocol.

FIGURE 5-6: HIGH-SPEED READ SEQUENCE (SPI) (C[1:0] = 0BH)



In SQI protocol, the host drives CE# low then sends one High-Speed Read command cycle, 0BH, followed by three address cycles, a Set Mode configuration cycle, and two dummy cycles. Each cycle is two nibbles (clocks) long, Most Significant nibble first.

After the dummy cycles, the device outputs data on the falling edge of the SCK signal starting from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer automatically increments until the highest memory address is reached, at which point the Address Pointer returns to address location 000000H. During this operation, blocks that are read-locked will output data 00H.

The Set Mode Configuration bit M[7:0] indicates if the next instruction cycle is another SQI High-Speed Read command.

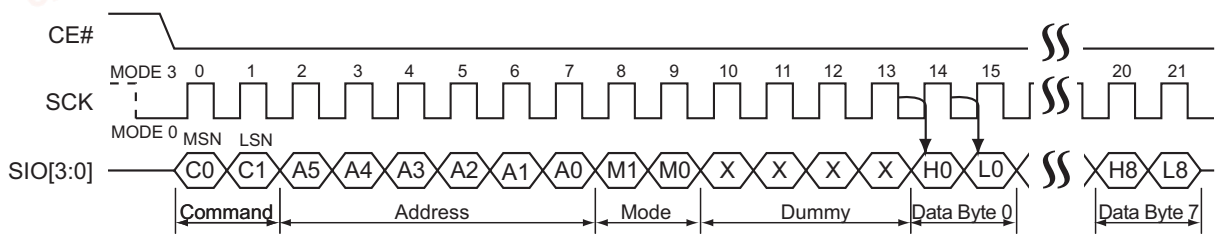
When M[7:0] = AXH, the device expects the next continuous instruction to be another read command, 0BH, and does not require the opcode to be entered again. The host may initiate the next read cycle by driving CE# low, then sending the 4-bit input for address A[23:0], followed by the Set Mode Configuration bits M[7:0], and two dummy cycles. After the two dummy cycles, the device outputs the data starting from the specified address location. There are no restrictions on address location access.

When M[7:0] is any value other than AXH, the device expects the next instruction initiated to be a command instruction. To reset/exit the Set Mode configuration, execute the Reset Quad I/O command, FFH. While in the Set Mode configuration, the RSTQIO command will only return the device to a state where it can accept a new command instruction. An additional RSTQIO is required to reset the device to SPI mode. See Figure 5-10 for the SPI Quad I/O Mode Read sequence when M[7:0] = AXH.

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FIGURE 5-7: HIGH-SPEED READ SEQUENCE (SQI)



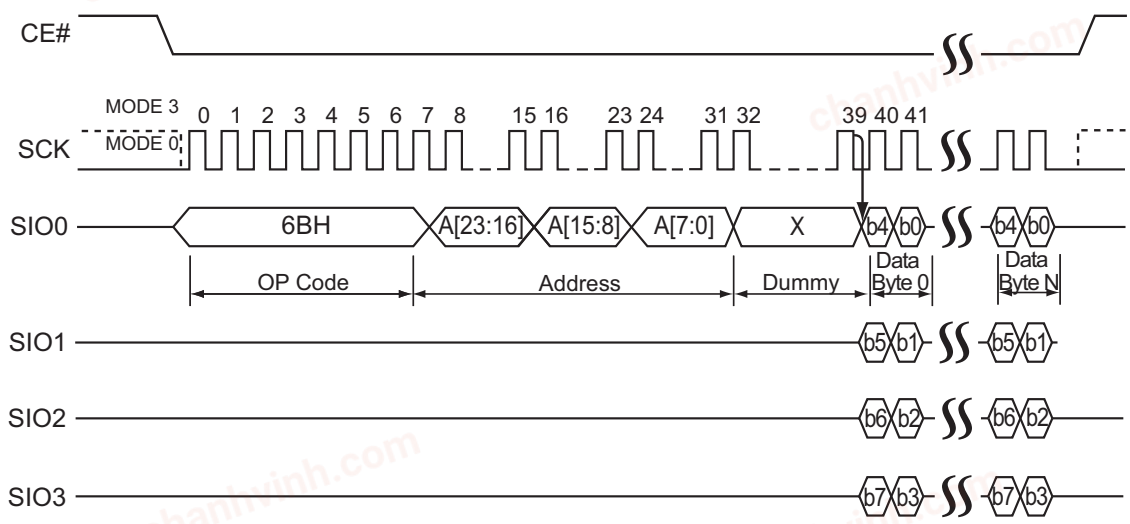
Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble
Hx = High Data Nibble, Lx = Low Data Nibble C[1:0] = 0BH

5.7 SPI Quad Output Read

The SPI Quad Output Read instruction supports frequencies of up to 104 MHz from 2.7V-3.6V and up to 80 MHz from 2.3V-3.6V. SST26VF040A requires the IOC bit in the Configuration register to be set to '1' prior to executing the command. Initiate SPI Quad Output Read by executing an 8-bit command, 6BH, followed by address bits A[23:0] and a dummy byte. CE# must remain active-low for the duration of the SPI Quad Mode Read. See Figure 5-8 for the SPI Quad Output Read sequence.

Following the dummy byte, the device outputs data from SIO[3:0] starting from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer automatically increments until the highest memory address is reached, at which point the Address Pointer returns to the beginning of the address space.

FIGURE 5-8: SPI QUAD OUTPUT READ



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble

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5.8 SPI Quad I/O Read

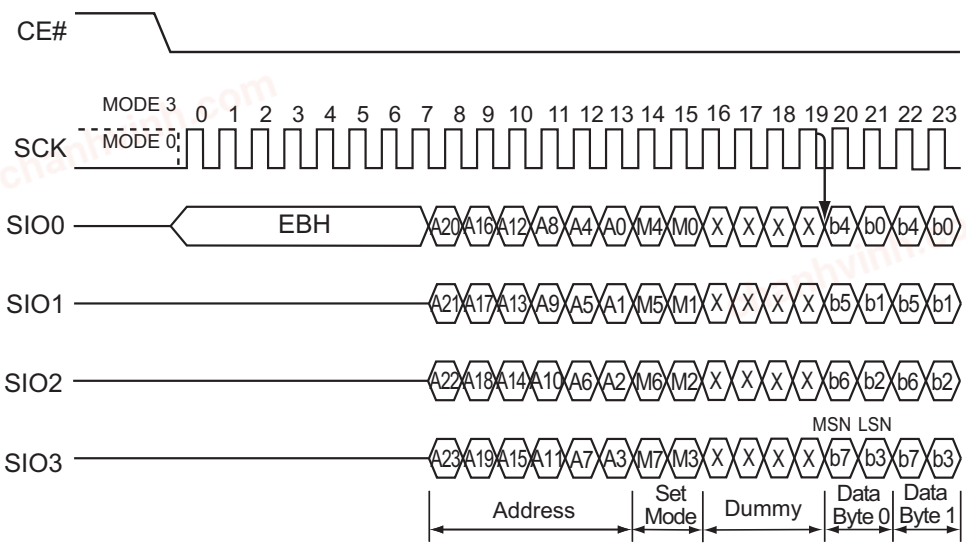
The SPI Quad I/O Read (SQIOR) instruction supports frequencies of up to 104 MHz from 2.7V-3.6V and up to 80 MHz from 2.3V-3.6V. SST26VF040A requires the IOC bit in the Configuration register to be set to '1' prior to executing the command. Initiate SQIOR by executing an 8-bit command, EBH. The device then switches to 4-bit I/O mode for address bits A[23:0], followed by the Set Mode Configuration bits M[7:0], and two dummy bytes. CE# must remain active-low for the duration of the SPI Quad I/O Read. See Figure 5-9 for the SPI Quad I/O Read sequence.

Following the dummy bytes, the device outputs data from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer automatically increments until the highest memory address is reached, at which point the Address Pointer returns to the beginning of the address space.

The Set Mode Configuration bit M[7:0] indicates if the next instruction cycle is another SPI Quad I/O Read command. When M[7:0] = AXH, the device expects the next continuous instruction to be another read command, EBH, and does not require the opcode to be entered again. The host may set the next SQIOR cycle by driving CE# low, then sending the 4-bit wide input for address A[23:0], followed by the Set Mode Configuration bits M[7:0], and two dummy cycles. After the two dummy cycles, the device outputs the data starting from the specified address location. There are no restrictions on address location access.

When M[7:0] is any value other than AXH, the device expects the next instruction initiated to be a command instruction. To reset/exit the Set Mode configuration, execute the Reset Quad I/O command, FFH. See Figure 5-10 for the SPI Quad I/O Mode Read sequence when M[7:0] = AXH.

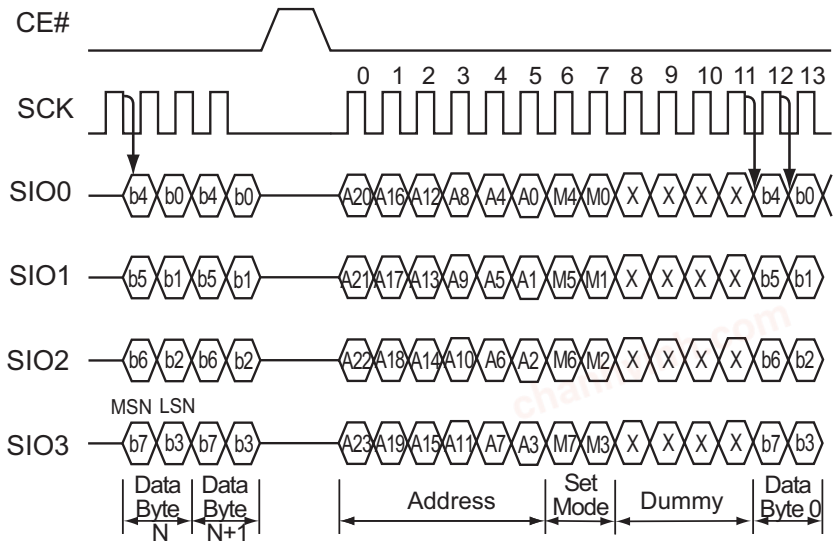
FIGURE 5-9: SPI QUAD I/O READ SEQUENCE



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble

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FIGURE 5-10: BACK-TO-BACK SPI QUAD I/O READ SEQUENCES WHEN M[7:0] = AXH



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble

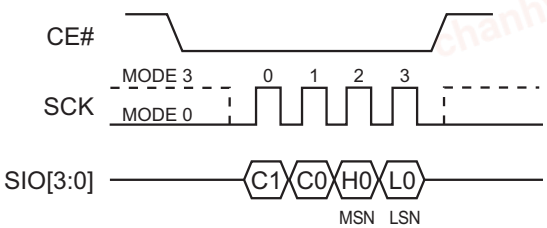
5.9 Set Burst

The Set Burst command specifies the number of bytes to be output during a Read Burst command before the device wraps around. It supports both SPI and SQI protocols. To set the burst length the host drives CE# low, sends the Set Burst command cycle (C0H) and one data cycle, then drives CE# high. After power-up or Reset, the burst length is set to eight bytes (00H). See Table 5-2 for burst length data and Figures 5-11 and 5-12 for the sequences.

TABLE 5-2: BURST LENGTH DATA

Burst Length	High Nibble (H0)	Low Nibble (L0)
8 Bytes	0h	0h
16 Bytes	0h	1h
32 Bytes	0h	2h
64 Bytes	0h	3h

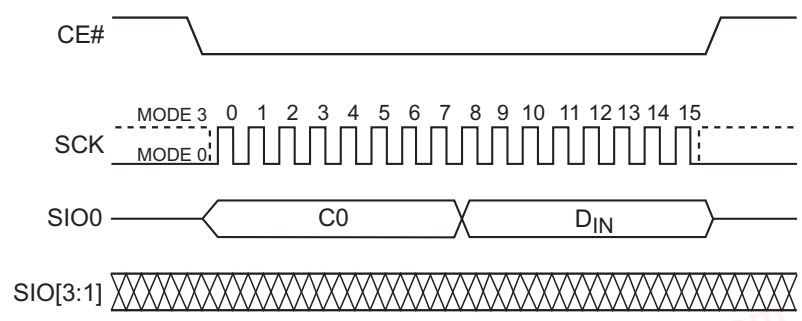
FIGURE 5-11: SET BURST LENGTH SEQUENCE (SQI)



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble, C[1:0] = C0H

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FIGURE 5-12: SET BURST LENGTH SEQUENCE (SPI)



Note: SIO[3:1] must be driven VIH.

5.10 SQI Read Burst with Wrap (RBSQI)

SQI Read Burst with Wrap is similar to High-Speed Read in SQI mode, except data will output continuously within the burst length until a low-to-high transition on CE#. To execute a SQI Read Burst operation, drive CE# low then send the Read Burst command cycle (0CH), followed by three address cycles, and then three dummy cycles. Each cycle is two nibbles (clocks) long, Most Significant nibble first.

After the dummy cycles, the device outputs data on the falling edge of the SCK signal starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#.

During RBSQI, the internal Address Pointer automatically increments until the last byte of the burst is reached, then it wraps around to the first byte of the burst. All bursts are aligned to addresses within the burst length, see Table 5-3. For example, if the burst length is eight bytes, and the start address is 06h, the burst sequence would be: 06h, 07h, 00h, 01h, 02h, 03h, 04h, 05h, 06h, etc. The pattern repeats until the command is terminated by a low-to-high transition on CE#.

During this operation, blocks that are read-locked will output data 00H.

5.11 SPI Read Burst with Wrap (RBSPI)

SPI Read Burst with Wrap (RBSPI) is similar to SPI Quad I/O Read except the data will output continuously within the burst length until a low-to-high transition on CE#. To execute a SPI Read Burst with Wrap operation, drive CE# low, then send the Read Burst command cycle (ECH), followed by three address cycles, and then three dummy cycles.

After the dummy cycle, the device outputs data on the falling edge of the SCK signal starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#.

During RBSPI, the internal Address Pointer automatically increments until the last byte of the burst is reached, then it wraps around to the first byte of the burst. All bursts are aligned to addresses within the burst length, see Table 5-3. For example, if the burst length is eight bytes, and the start address is 06h, the burst sequence would be: 06h, 07h, 00h, 01h, 02h, 03h, 04h, 05h, 06h, etc. The pattern repeats until the command is terminated by a low-to-high transition on CE#.

During this operation, blocks that are read-locked will output data 00H.

TABLE 5-3: BURST ADDRESS RANGES

Burst Length	Burst Address Ranges
8 Bytes	00-07H, 08-0FH, 10-17H, 18-1FH...
16 Bytes	00-0FH, 10-1FH, 20-2FH, 30-3FH...
32 Bytes	00-1FH, 20-3FH, 40-5FH, 60-7FH...
64 Bytes	00-3FH, 40-7FH, 80-BFH, C0-FFH

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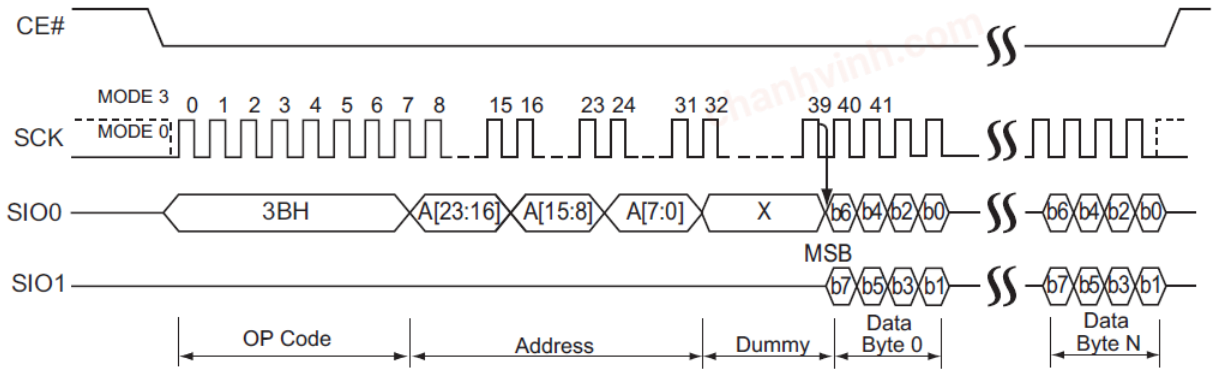
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5.12 SPI Dual Output Read

The SPI Dual Output Read instruction supports frequencies of up to 104 MHz from 2.7V-3.6V and up to 80 MHz from 2.3V-3.6V. Initiate SPI Dual Output Read by executing an 8-bit command, 3BH, followed by address bits A[23:0] and a dummy byte. CE# must remain active-low for the duration of the SPI Dual Output Read operation. See Figure 5-13 for the SPI Dual Output Read sequence.

Following the dummy byte, SST26VF040A outputs data from SIO[1:0] starting from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer automatically increments until the highest memory address is reached, at which point the Address Pointer returns to the beginning of the address space.

FIGURE 5-13: FAST READ, DUAL-OUTPUT SEQUENCE



Note: MSB = Most Significant Bit

5.13 SPI Dual I/O Read

The SPI Dual I/O Read (SDIOR) instruction supports up to 80 MHz frequency. Initiate SDIOR by executing an 8-bit command, BBH. The device then switches to 2-bit I/O mode for address bits A[23:0], followed by the Set Mode Configuration bits M[7:0]. CE# must remain active-low for the duration of the SPI Dual I/O Read. See Figure 5-14 for the SPI Dual I/O Read sequence.

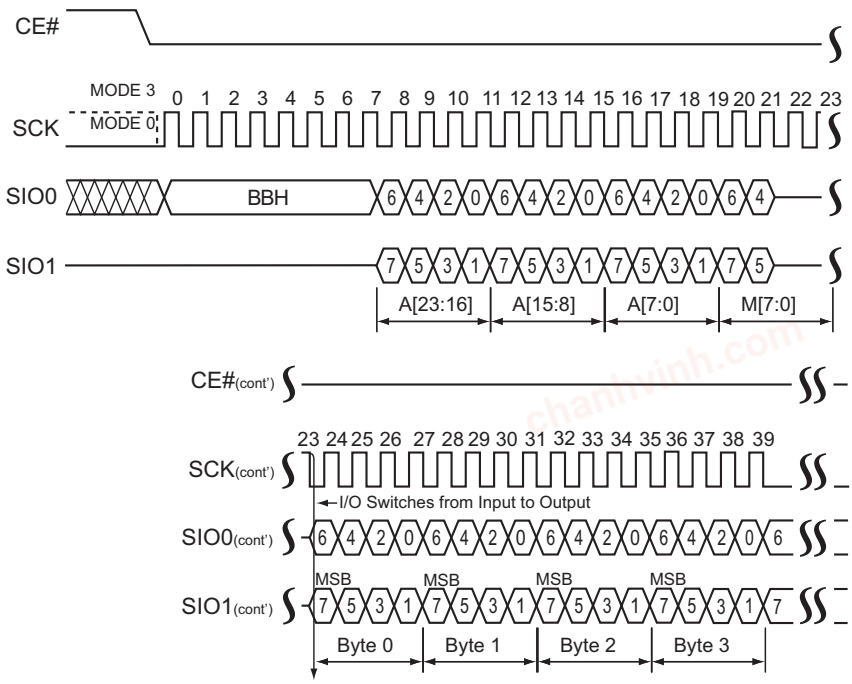
Following the Set Mode Configuration bits, the SST26VF040A outputs data from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer automatically increments until the highest memory address is reached, at which point the Address Pointer returns to the beginning of the address space.

The Set Mode Configuration bit M[7:0] indicates if the next instruction cycle is another SPI Dual I/O Read command. When M[7:0] = AXH, the device expects the next continuous instruction to be another SDIOR command, BBH, and does not require the opcode to be entered again. The host may set the next SDIOR cycle by driving CE# low, then sending the 2-bit wide input for address A[23:0], followed by the Set Mode Configuration bits M[7:0]. After the Set Mode Configuration bits, the device outputs the data starting from the specified address location. There are no restrictions on address location access.

When M[7:0] is any value other than AXH, the device expects the next instruction initiated to be a command instruction. To reset/exit the Set Mode configuration, execute the Reset Quad I/O command, FFH. See Figure 5-15 for the SPI Dual I/O Read sequence when M[7:0] = AXH.

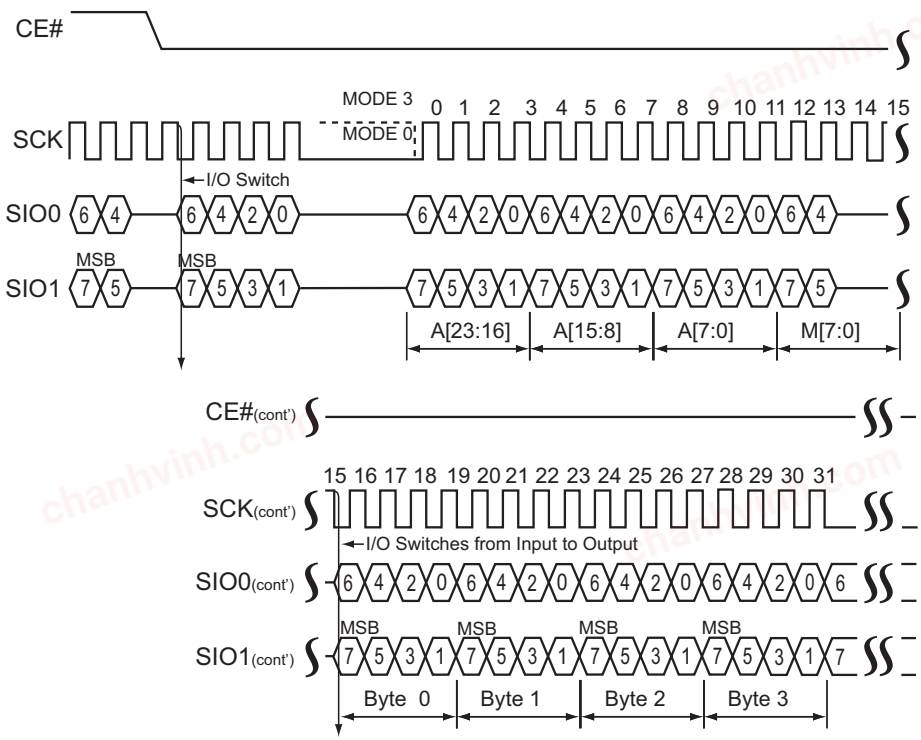
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FIGURE 5-14: SPI DUAL I/O READ SEQUENCE



Note: MSB = Most Significant Bit

FIGURE 5-15: BACK-TO-BACK SPI DUAL I/O READ SEQUENCES WHEN M[7:0] = AXH



Note: MSB = Most Significant Bit, LSB = Least Significant Bit

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5.14 JEDEC ID Read (SPI Protocol)

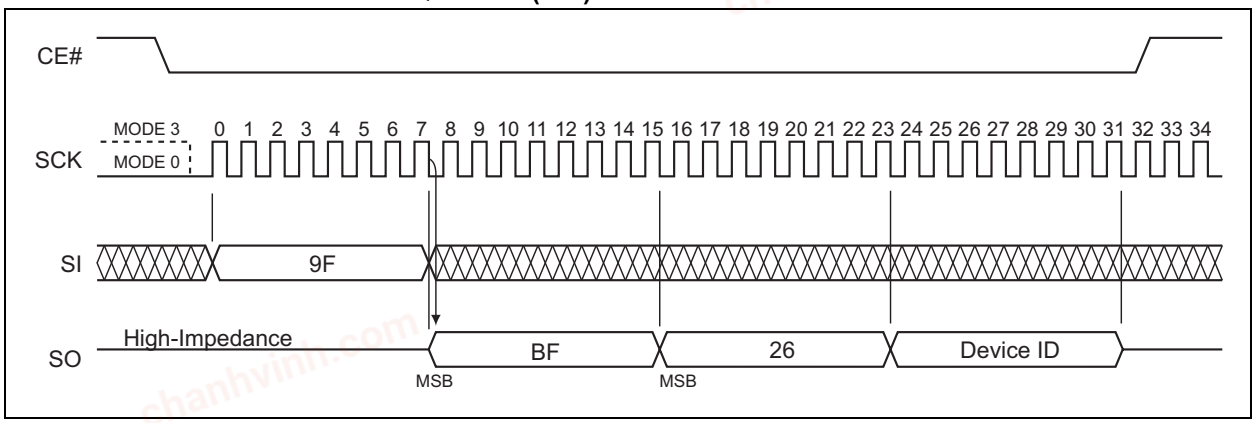
Using traditional SPI protocol, the JEDEC ID Read instruction identifies the device as SST26VF040A and the manufacturer as Microchip. To execute a JEDEC ID operation the host drives CE# low then sends the JEDEC ID command cycle (9FH).

Immediately following the command cycle, SST26VF040A output data on the falling edge of the SCK signal. The data output stream is continuous until terminated by a low-to-high transition on CE#. The device outputs three bytes of data: manufacturer, device type, and device ID, see Table 5-4. See Figure 5-16 for instruction sequence.

TABLE 5-4: DEVICE ID DATA OUTPUT

Product	Manufacturer ID (Byte 1)	Device ID	
		Device Type (Byte 2)	Device ID (Byte 3)
SST26VF040A	BFH	26H	14H

FIGURE 5-16: JEDEC ID SEQUENCE (SPI)

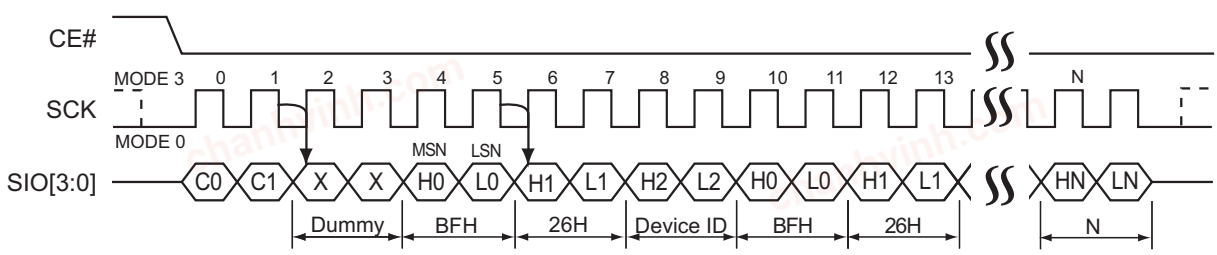


5.15 Read Quad J-ID Read (SQI Protocol)

The Read Quad J-ID Read instruction identifies the device as SST26VF040A and manufacturer as Microchip. To execute a Quad J-ID operation the host drives CE# low and then sends the Quad J-ID command cycle (AFH). Each cycle is two nibbles (clocks) long, Most Significant nibble first.

Immediately following the command cycle and one dummy cycle, SST26VF040A outputs data on the falling edge of the SCK signal. The data output stream is continuous until terminated by a low-to-high transition of CE#. The device outputs three bytes of data: manufacturer, device type, and device ID, see Table 5-4. See Figure 5-17 for instruction sequence.

FIGURE 5-17: QUAD J-ID READ SEQUENCE



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble, C[1:0] = AFH

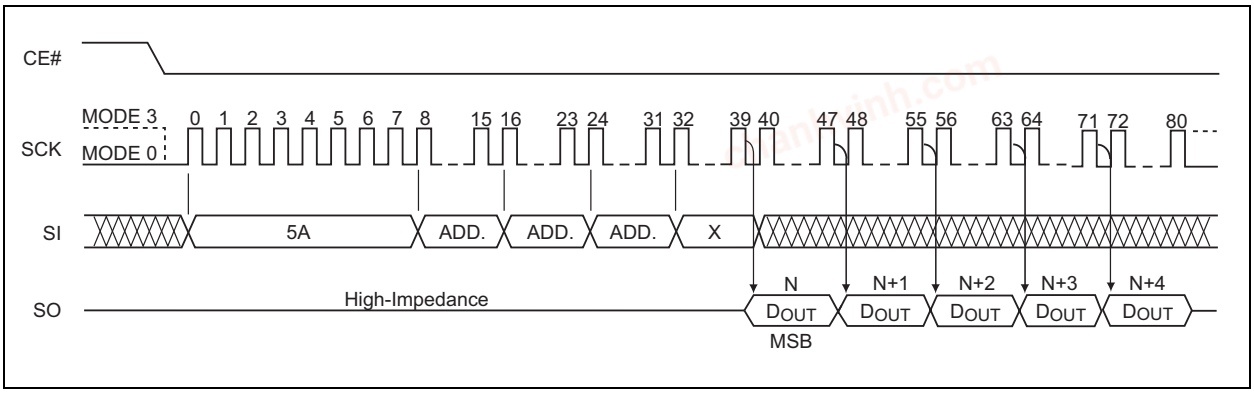
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5.16 Serial Flash Discoverable Parameters (SFDP)

The Serial Flash Discoverable Parameters (SFDP) contain information describing the characteristics of the device. This allows device-independent, JEDEC ID-independent, and forward/backward-compatible software support for all future Serial Flash device families. See Table 11-1 for address and data values.

Initiate SFDP by executing an 8-bit command, 5AH, followed by address bits A[23:0] and a dummy byte. CE# must remain active-low for the duration of the SFDP cycle. For the SFDP sequence, see Figure 5-18.

FIGURE 5-18: SERIAL FLASH DISCOVERABLE PARAMETERS SEQUENCE

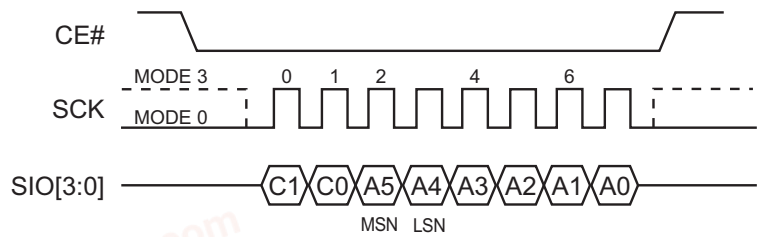


5.17 Sector Erase

The Sector Erase instruction clears all bits in the selected 4-KByte sector to '1', but it does not change a protected memory area. Prior to any write operation, the Write Enable (WREN) instruction must be executed.

To execute a Sector Erase operation, the host drives CE# low, then sends the Sector Erase command cycle (20H) and three address cycles, and then drives CE# high. Address bits [AMS:A_{12}] (AMS = Most Significant Address) determine the sector address (SA_X); the remaining address bits can be VIL or VIH. To identify the completion of the internal, self-timed, write operation, poll the BUSY bit in the STATUS register, or wait TSE. See Figures 5-19 and 5-20 for the Sector Erase sequence.

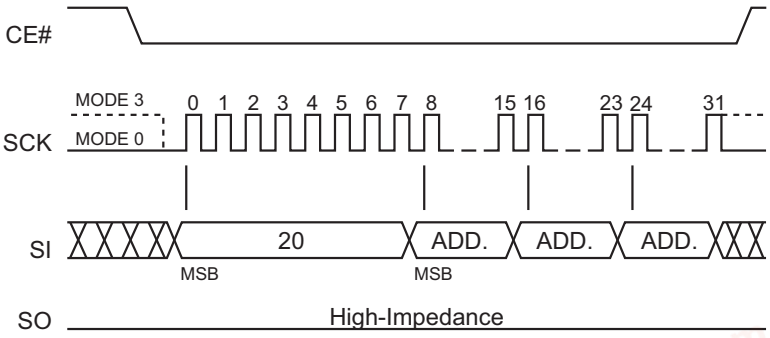
FIGURE 5-19: 4-KBYTE SECTOR ERASE SEQUENCE – SQI MODE



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble, C[1:0] = 20H

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FIGURE 5-20: 4-KBYTE SECTOR ERASE SEQUENCE (SPI)

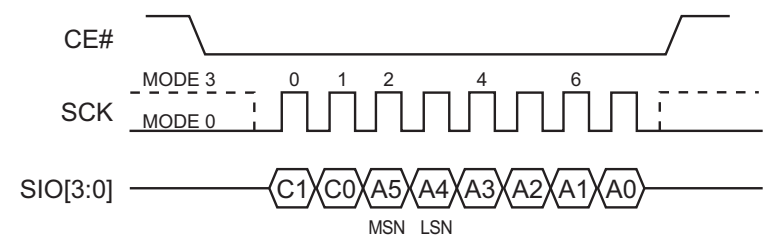


5.18 32-Kbyte Block Erase and 64-Kbyte Block Erase

The 32-Kbyte Block Erase instruction clears all bits in the selected 32-Kbyte block to FFH. The 64-Kbyte Block Erase instruction clears all bits in the selected 64-Kbyte block to FFH. A 32-Kbyte Block Erase or 64-Kbyte Block Erase instruction applied to a protected memory area will be ignored. Prior to any block erase operation, the Write Enable (WREN) instruction must be executed. CE# must remain active-low for the duration of any command sequence. The 32-Kbyte Block Erase instruction is initiated by executing an 8-bit command 52H, followed by address bits [A23:A0]. Address bits [AMS:A15] (AMS = Most Significant Address) are used to determine block address (BAX), remaining address bits can be VIL or VIH. CE# must be driven high before the instruction is executed.

The 64-Kbyte Block Erase instruction is initiated by executing an 8-bit command D8H, followed by address bits [A23:A0]. Address bits [AMS:A16] (AMS = Most Significant Address) are used to determine block address (BAX), remaining address bits can be VIL or VIH. CE# must be driven high before the instruction is executed. The user may poll the BUSY bit in the software STATUS register or wait TBE for the completion of the internal self-timed 32-Kbyte Block Erase or 64-Kbyte Block Erase cycles. See Figures 5-21 and 5-22 for the 32-Kbyte Block Erase sequence and Figures 5-23 and 5-24 for the 64-Kbyte Block Erase sequence.

FIGURE 5-21: 32-KBYTE BLOCK-ERASE SEQUENCE (SQI)



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble, C[1:0] = 52H

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FIGURE 5-22: 32-KBYTE BLOCK-ERASE SEQUENCE (SPI)

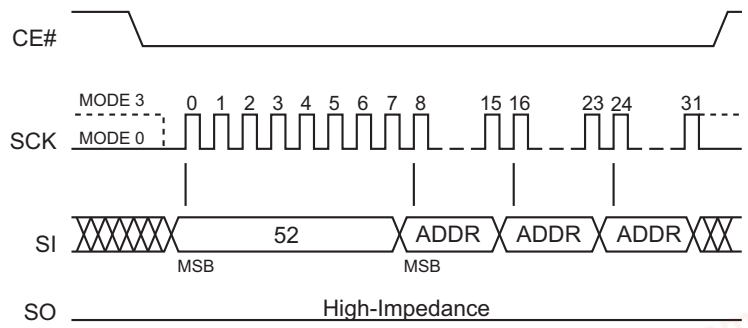
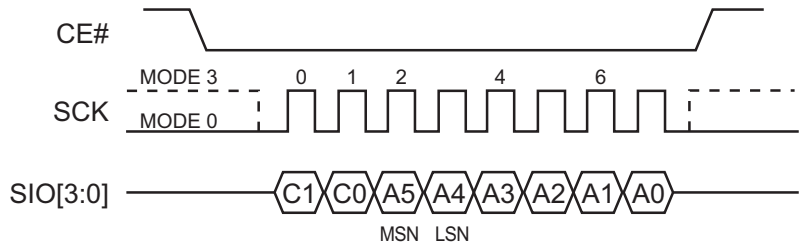
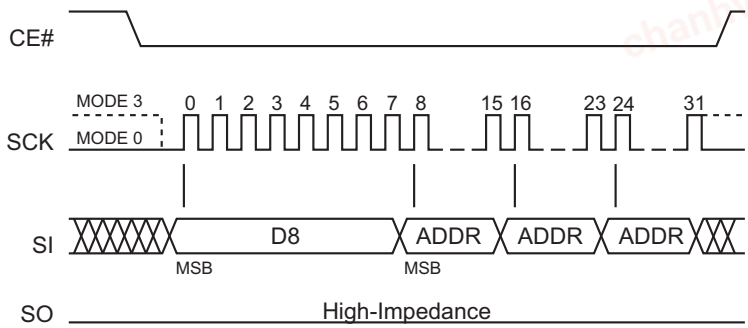


FIGURE 5-23: 64-KBYTE BLOCK-ERASE SEQUENCE (SQI)



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble, C[1:0] = D8H

FIGURE 5-24: 64-KBYTE BLOCK-ERASE SEQUENCE (SPI)



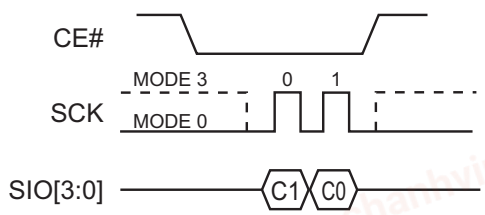
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5.19 Chip Erase

The Chip Erase instruction clears all bits in the device to '1'. The Chip Erase instruction is ignored if any of the memory area is protected. Prior to any write operation, execute the WREN instruction.

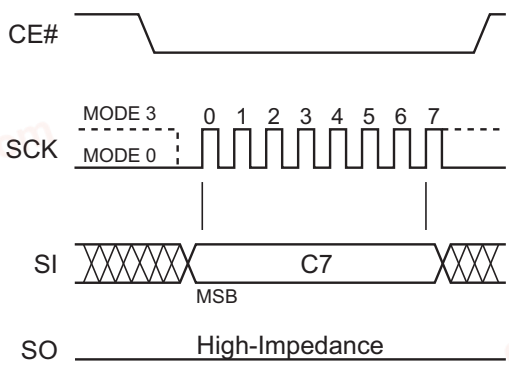
To execute a Chip Erase operation, the host drives CE# low, sends the Chip Erase command cycle (C7H or 60H), then drives CE# high. Poll the BUSY bit in the STATUS register, or wait T_{SCE}, for the completion of the internal, self-timed, write operation. See Figures 5-25 and 5-26 for the Chip Erase sequence.

FIGURE 5-25: CHIP ERASE SEQUENCE (SQI)



Note: C[1:0] = C7H

FIGURE 5-26: CHIP ERASE SEQUENCE (SPI)



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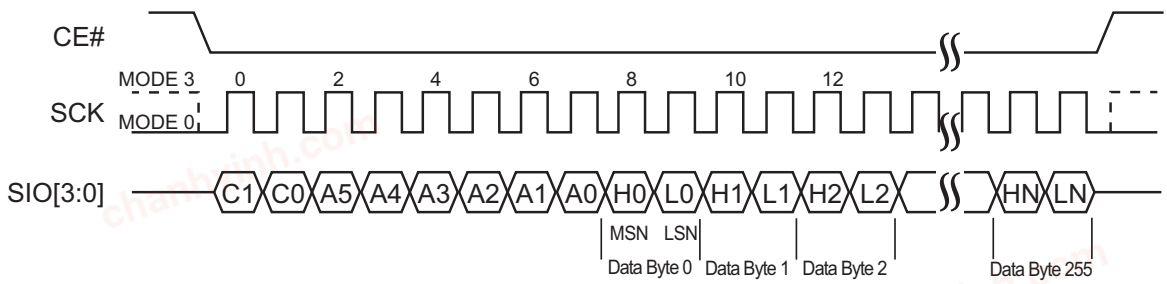
5.20 Page Program

The Page Program instruction programs up to 256 bytes of data in the memory, and supports both SPI and SQI protocols. The data for the selected page address must be in the erased state (FFH) before initiating the Page Program operation. A Page Program applied to a protected memory area will be ignored. Prior to the program operation, execute the WREN instruction.

To execute a Page Program operation, the host drives CE# low then sends the Page Program command cycle (02H), three address cycles followed by the data to be programmed, then drives CE# high. The programmed data must be between 1 to 256 bytes and in whole-byte increments; sending less than a full byte will cause the partial byte to be ignored. Poll the BUSY bit in the STATUS register, or wait TPP for the completion of the internal, self-timed, write operation. See Figures 5-27 and 5-28 for the Page Program sequence.

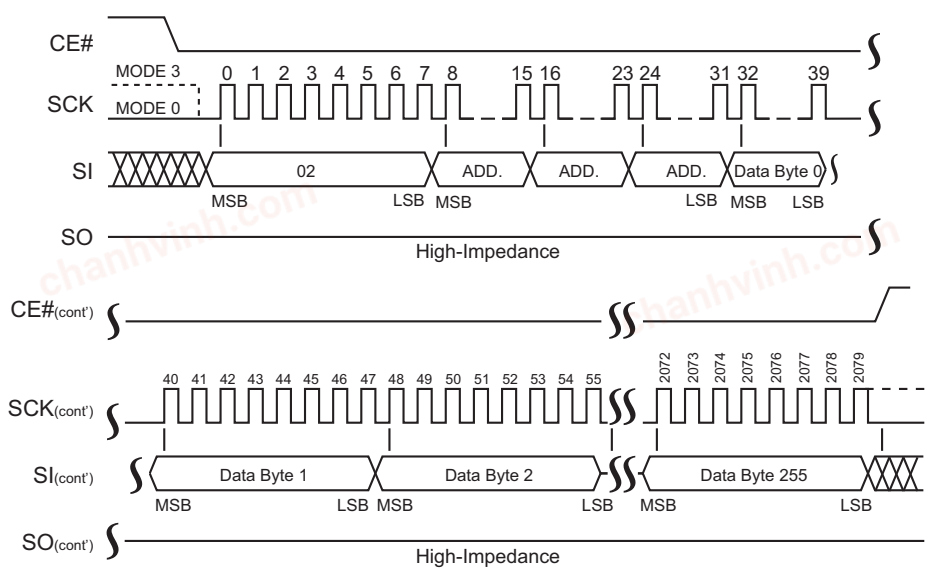
When executing Page Program, the memory range for the SST26VF040A is divided into 256-byte page boundaries. The device handles shifting of more than 256 bytes of data by maintaining the last 256 bytes of data as the correct data to be programmed. If the target address for the Page Program instruction is not the beginning of the page boundary (A[7:0] are not all zero), and the number of bytes of data input exceeds or overlaps the end of the address of the page boundary, the excess data inputs wrap-around and will be programmed at the start of that target page.

FIGURE 5-27: PAGE-PROGRAM SEQUENCE (SQI)



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble

FIGURE 5-28: PAGE-PROGRAM SEQUENCE (SPI)



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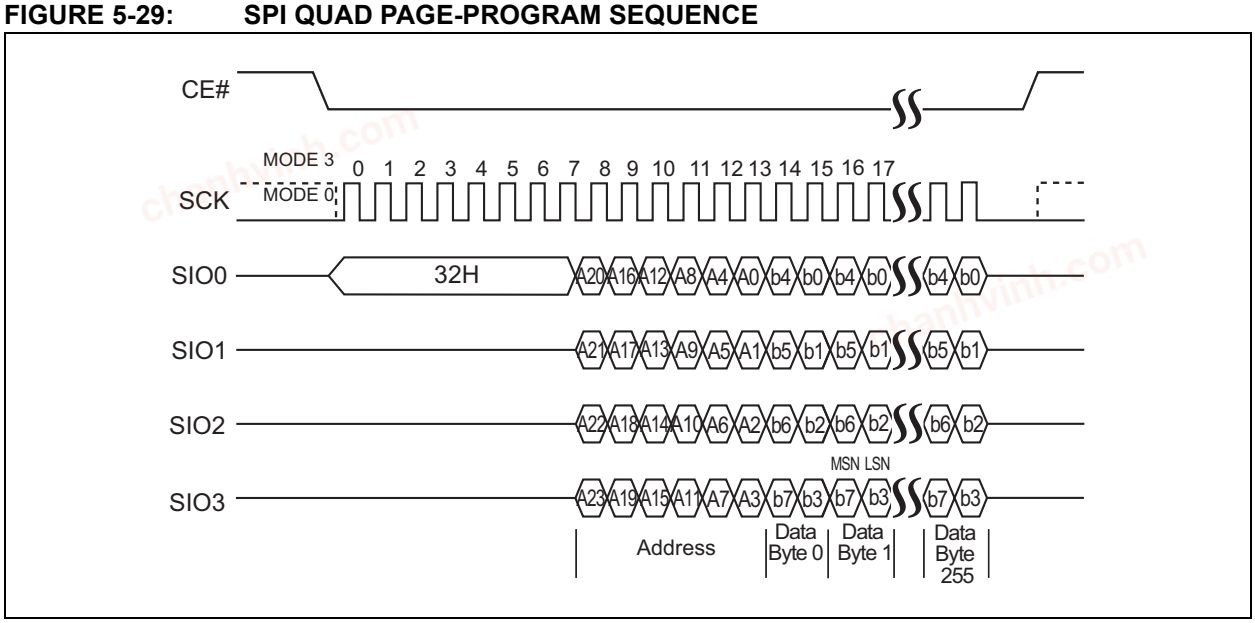
5.21 SPI Quad Page Program

The SPI Quad Page Program instruction programs up to 256 bytes of data in the memory. The data for the selected page address must be in the erased state (FFH) before initiating the SPI Quad Page Program operation. A SPI Quad Page Program applied to a protected memory area will be ignored. SST26VF040A requires the ICO bit in the Configuration register to be set to '1' prior to executing the command. Prior to the program operation, execute the WREN instruction.

To execute a SPI Quad Page Program operation, the host drives CE# low then sends the SPI Quad Page Program command cycle (32H), three address cycles followed by the data to be programmed, then drives CE# high. The programmed data must be between 1 to 256 bytes and in whole-byte increments. The command cycle is eight clocks long, the address and data cycles are each two clocks long, Most Significant bit first. Poll the BUSY bit in the STATUS register, or wait TPP for the completion of the internal, self-timed, write operation. See Figure 5-29.

When executing SPI Quad Page Program, the memory range for the SST26VF040A is divided into 256-byte page boundaries. The device handles shifting of more than 256 bytes of data by maintaining the last 256 bytes of data as the correct data to be programmed. If the target address for the SPI Quad Page Program instruction is not the beginning of the page boundary (A[7:0] are not all zero), and the of bytes of data input exceeds or overlaps the end of the address of the page boundary, the excess data inputs wrap-around and will be programmed at the start of that target page.

FIGURE 5-29: SPI QUAD PAGE-PROGRAM SEQUENCE



5.22 Write Suspend and Write Resume

Write Suspend allows the interruption of Sector Erase, 32-Kbyte Block Erase, 64-Kbyte Block Erase, SPI Quad Page Program, or Page Program operations in order to erase, program or read data in another portion of memory. The original operation can be continued with the Write Resume command. This operation is supported in both SQI and SPI protocols.

Only one write operation can be suspended at a time; if an operation is already suspended, the device will ignore the Write Suspend command. Write Suspend during Chip Erase is ignored; Chip Erase is not a valid command while a write is suspended.

The Write Resume command is ignored until any write operation (Program or Erase) initiated during the Write Suspend is complete. The device requires a minimum of 500 µs between each Write Suspend command.

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5.23 Write Suspend During Sector Erase or Block Erase

Issuing a Write Suspend instruction during Sector Erase or 32-Kbyte Block Erase or 64-Kbyte Block Erase allows the host to program or read any sector that was not being erased. The device will ignore any programming commands pointing to the suspended sector(s). Any attempt to read from the suspended sector(s) will output unknown data because the Sector or 32-Kbyte Block Erase or 64-Kbyte Block Erase will be incomplete.

To execute a Write Suspend operation, the host drives CE# low, sends the Write Suspend command cycle (B0H), then drives CE# high. The Configuration register indicates that the erase has been suspended by changing the WSE bit from '0' to '1', but the device will not accept another command until it is ready. To determine when the device will accept a new command, poll the BUSY bit in the STATUS register or wait TWS.

5.24 Write Suspend During Page Programming or SPI Quad Page Programming

Issuing a Write Suspend instruction during Page Programming allows the host to erase or read any sector that is not being programmed. Erase commands pointing to the suspended sector(s) will be ignored. Any attempt to read from the suspended page will output unknown data because the program will be incomplete.

To execute a Write Suspend operation, the host drives CE# low, sends the Write Suspend command cycle (B0H), then drives CE# high. The Configuration register indicates that the programming has been suspended by changing the WSP bit from '0' to '1', but the device will not accept another command until it is ready. To determine when the device will accept a new command, poll the BUSY bit in the STATUS register or wait TWS.

5.25 Write Resume

Write Resume restarts a write command that was suspended, and changes the suspend Status bit in the Configuration register (WSE or WSP) back to '0'.

To execute a Write Resume operation, the host drives CE# low, sends the Write Resume command cycle (30H), then drives CE# high. To determine if the internal, self-timed write operation is completed, poll the BUSY bit in the STATUS register, or wait the specified time TSE, TBE or TPP for Sector-Erase, Block-Erase, or Page-Programming, respectively. The total write time before suspend and after resume will not exceed the uninterrupted write times TSE, TBE or TPP.

5.26 Read Security ID

The Read Security ID operation is supported in both SPI and SQI modes. To execute a Read Security ID (SID) operation in SPI mode, the host drives CE# low, sends the Read Security ID command cycle (88H), two address cycles, and then one dummy cycle. To execute a Read Security ID operation in SQI mode, the host drives CE# low and then sends the Read Security ID command, two address cycles, and three dummy cycles.

After the dummy cycles, the device outputs data on the falling edge of the SCK signal, starting from the specified address location. The data output stream is continuous through all SID addresses until terminated by a low-to-high transition on CE#. See Table 5-5 for the Security ID address range.

5.27 Program Security ID

The Program Security ID instruction programs one to 2032 bytes of data in the user-programmable, Security ID space. This Security ID space is one-time-programmable (OTP). The device ignores a Program Security ID instruction pointing to an invalid or protected address, see Table 5-5. Prior to the program operation, execute WREN.

To execute a Program SID operation, the host drives CE# low, sends the Program Security ID command cycle (A5H), two address cycles, the data to be programmed, then drives CE# high. The programmed data must be between 1 to 256 bytes and in whole-byte increments.

The device handles shifting of more than 256 bytes of data by maintaining the last 256 bytes of data as the correct data to be programmed. If the target address for the Program Security ID instruction is not the beginning of the page boundary, and the number of data input exceeds or overlaps the end of the address of the page boundary, the excess data inputs wrap-around and will be programmed at the start of that target page.

The Program Security ID operation is supported in both SPI and SQI mode. To determine the completion of the internal, self-timed Program SID operation, poll the BUSY bit in the software STATUS register, or wait TPSID for the completion of the internal self-timed Program Security ID operation.

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TABLE 5-5: PROGRAM SECURITY ID

Program Security ID	Address Range
Unique ID Preprogrammed at Factory	0000-000FH
User-Programmable	0010H-07FFH

5.28 Lockout Security ID

The Lockout Security ID instruction prevents any future changes to the Security ID, and is supported in both SPI and SQI modes. Prior to the operation, execute WREN.

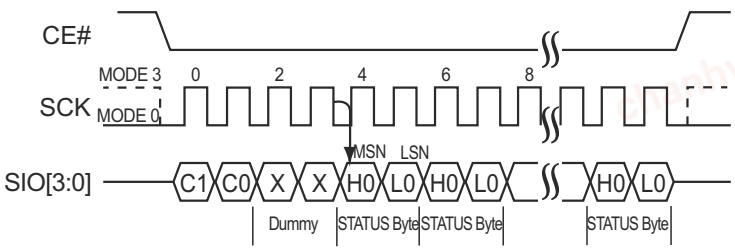
To execute a Lockout SID, the host drives CE# low, sends the Lockout Security ID command cycle (85H), then drives CE# high. Poll the BUSY bit in the software STATUS register, or wait TPSID for the completion of the Lockout Security ID operation.

5.29 Read STATUS Register (RDSR) and Read Configuration Register (RDCR)

The Read STATUS Register (RDSR) and Read Configuration Register (RDCR) commands output the contents of the STATUS and Configuration registers. These commands function in both SPI and SQI modes. The STATUS register may be read at any time, even during a write operation. When a write is in progress, poll the BUSY bit before sending any new commands to assure that the new commands are properly received by the device.

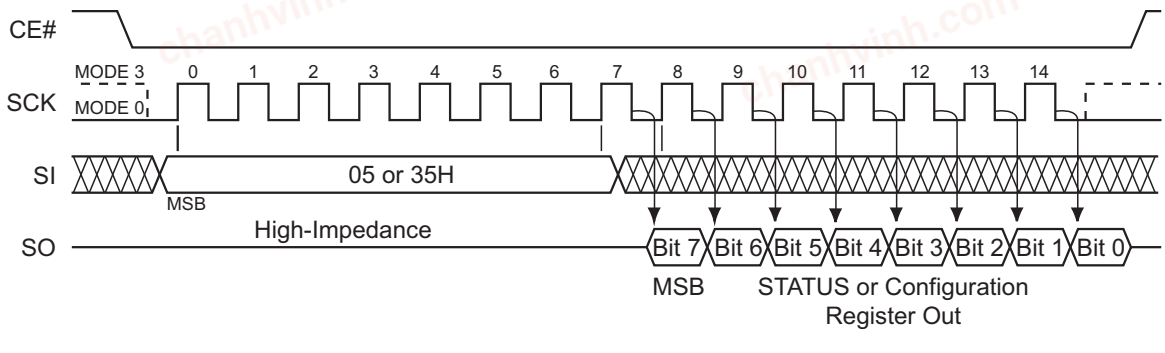
To read the STATUS or Configuration registers, the host drives CE# low, then sends the Read STATUS Register command cycle (05H) or the Read Configuration Register command (35H). A dummy cycle is required in SQI mode. Immediately after the command cycle, the device outputs data on the falling edge of the SCK signal. The data output stream continues until terminated by a low-to-high transition on CE#. See Figures 5-30 and 5-31 for the instruction sequence.

FIGURE 5-30: READ STATUS REGISTER AND READ CONFIGURATION REGISTER SEQUENCE (SQI)



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble, C[1:0] = 05H or 35H

FIGURE 5-31: READ STATUS REGISTER AND READ CONFIGURATION REGISTER SEQUENCE (SPI)

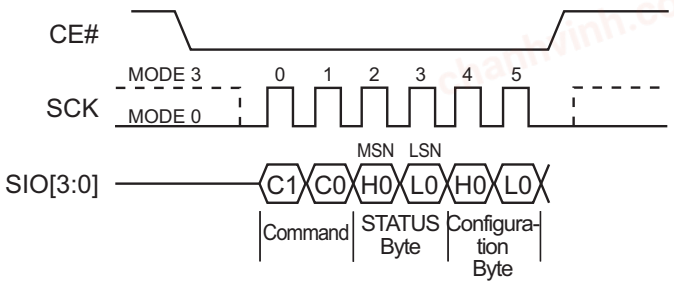


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5.30 Write STATUS Register (WRSR)

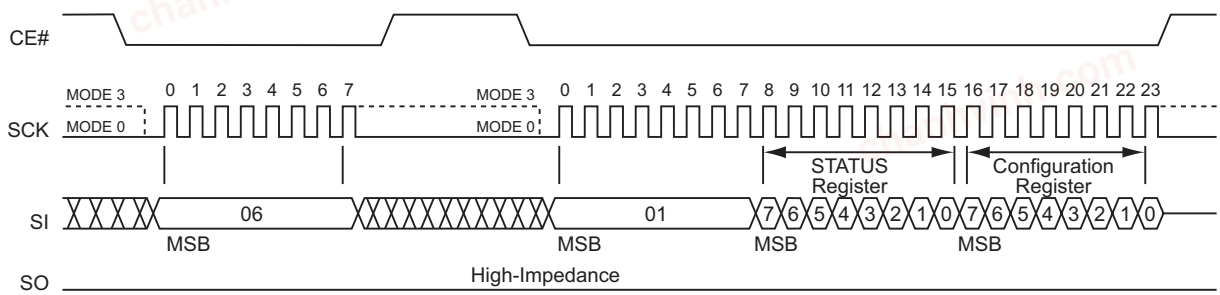
The Write STATUS Register (WRSR) command writes new values to the STATUS register and Configuration register. To execute a Write STATUS Register operation, the host drives CE# low, then sends the Write STATUS Register command cycle (01H), and one or two cycles of data, and then drives CE# high. The first cycle of data points to the STATUS register, the second points to the Configuration register. See Figures 5-32 and 5-33.

FIGURE 5-32: WRITE STATUS REGISTER SEQUENCE (SQI)



Note: MSN = Most Significant Nibble; LSN = Least Significant Nibble, XX = “Don’t Care”, C[1:0] = 01H

FIGURE 5-33: WRITE STATUS REGISTER SEQUENCE (SPI)



Note: XX = “Don’t Care”

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5.31 Write Enable (WREN)

The Write Enable (WREN) instruction sets the Write Enable Latch bit in the STATUS register to '1', allowing write operations to occur. The WREN instruction must be executed prior to any of the following operations: Sector Erase, 32-Kbyte Block Erase or 64-Kbyte Block Erase, Chip Erase, Page Program, Program Security ID, Lockout Security ID, Lock-Down Protection Settings, SPI Quad Page program, and Write STATUS register. To execute a Write Enable the host drives CE# low then sends the Write Enable command cycle (06H) then drives CE# high. See Figures 5-34 and 5-35 for the WREN instruction sequence.

FIGURE 5-34: WRITE ENABLE SEQUENCE (SQI)

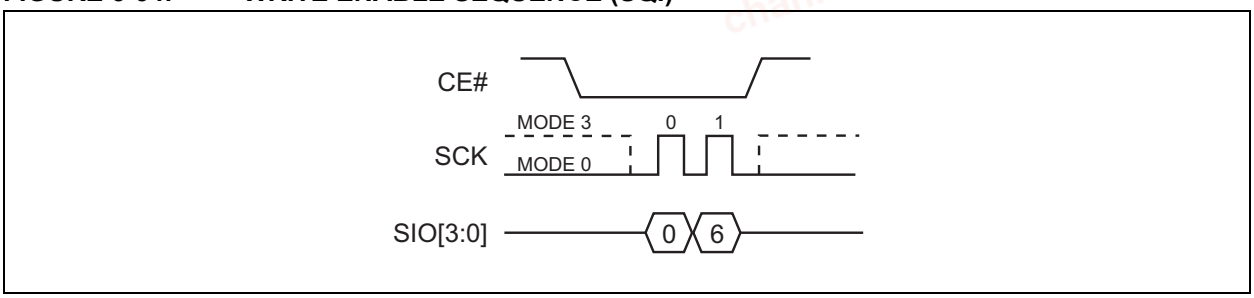
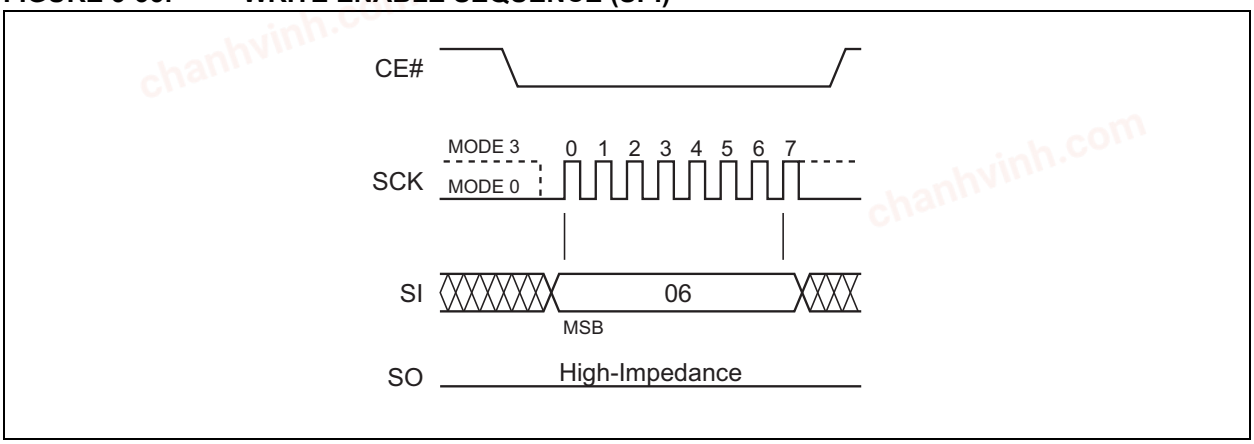


FIGURE 5-35: WRITE ENABLE SEQUENCE (SPI)



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5.32 Write Disable (WRDI)

The Write Disable (WRDI) instruction sets the Write Enable Latch bit in the STATUS register to '0', preventing write operations. The WRDI instruction is ignored during any internal write operations. Any write operation started before executing WRDI will complete. Drive CE# high before executing WRDI.

To execute a Write Disable, the host drives CE# low, sends the Write Disable command cycle (04H), then drives CE# high. See Figures 5-36 and 5-37.

FIGURE 5-36: WRITE DISABLE (WRDI) SEQUENCE (SQI)

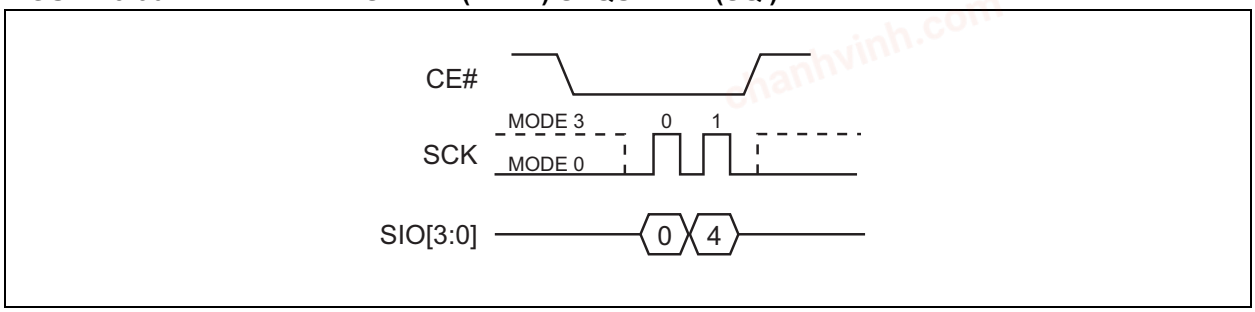
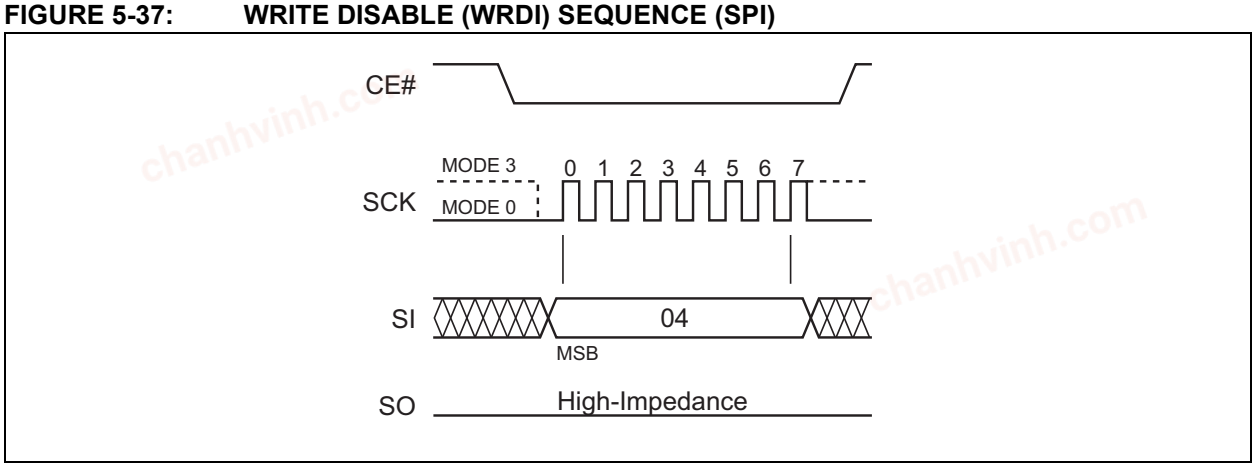


FIGURE 5-37: WRITE DISABLE (WRDI) SEQUENCE (SPI)

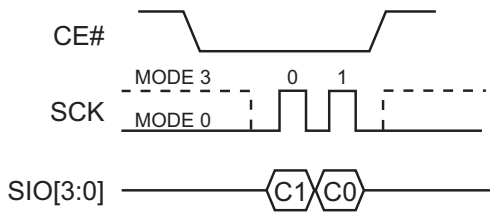


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5.33 Lock-Down Protection Settings (LDPS)

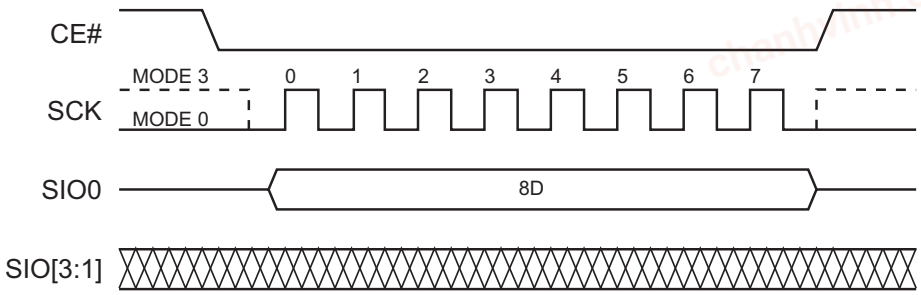
The Lock-Down Protection Settings instruction prevents changes to the Block Protection bits (BP0, BP1, BP2, BP3) of the STATUS register during device operation. Lock-Down resets after power cycling or hardware Reset; this allows the Block Protection settings to be changed. Execute WREN before initiating the Lock-Down Protection Settings instruction. To execute a Lock-Down Protection Settings command, the host drives CE# low, then sends the Lock-Down Protection Settings command cycle (8DH), then drive CE# high. Executing the LDPS instruction will set the VLP bit in the Configuration register.

FIGURE 5-38: LOCK-DOWN PROTECTION SETTINGS (SQI)



Note: C[1:0] = 8DH

FIGURE 5-39: LOCK-DOWN PROTECTION SETTINGS (SPI)



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5.34 Deep Power-Down

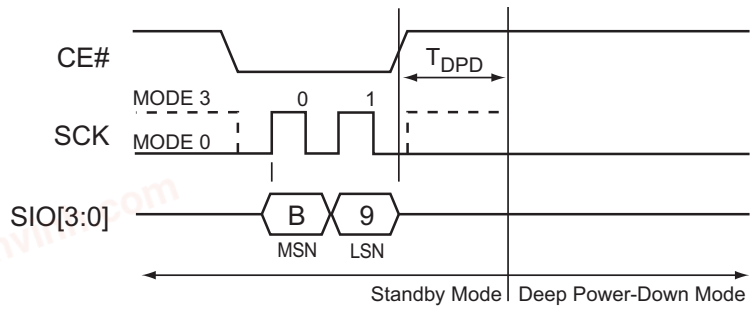
The Deep Power-Down (DPD) instruction puts the device in the lowest power consumption mode – the Deep Power-Down mode. The Deep Power-Down instruction is ignored during an internal write operation. While the device is in Deep Power-Down mode, all instructions will be ignored except for the Release Deep Power-Down instruction.

Enter Deep Power-Down mode by initiating the Deep Power-Down (DPD) instruction (B9H) while driving CE# low. CE# must be driven high before executing the DPD instruction. After CE# is driven high, it requires a delay of T_{DPD} before the standby current I_{SB} is reduced to deep power-down current I_{DPD}. See Table 5-6 for Deep Power-Down timing. If the device is busy performing an internal erase or program operation, initiating a Deep Power-Down instruction will not place the device in Deep Power-Down mode. See Figures 5-40 and 5-41 for the DPD instruction sequence.

TABLE 5-6: DEEP POWER-DOWN

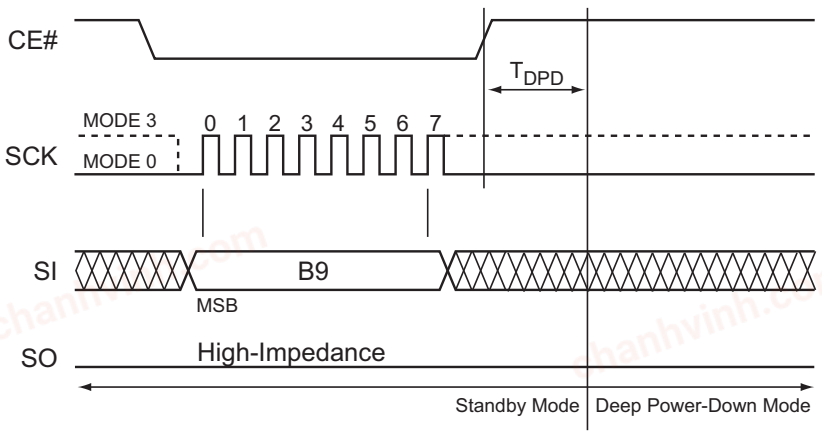
Symbol	Parameter	Min.	Max.	Units
T_{DPD}	CE# High to Deep Power-Down	—	3	µs
T_{SBR}	CE# High to Standby Mode	—	10	µs

FIGURE 5-40: DEEP POWER-DOWN (DPD) SEQUENCE – SQI MODE



Note: MSN = Most Significant Nibble; LSN = Least Significant Nibble

FIGURE 5-41: DEEP POWER-DOWN (DPD) SEQUENCE – SPI MODE



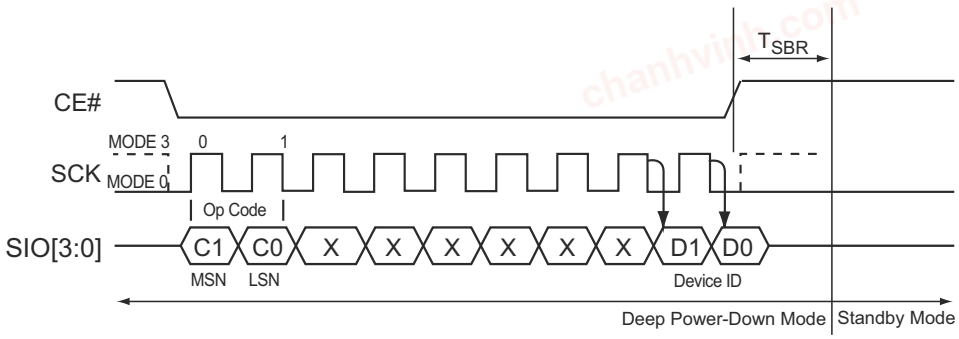
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5.35 Release from Deep Power-Down and Read ID

Release from Deep Power-Down (RDPD) and Read ID instruction exits Deep Power-Down mode. To exit Deep Power-Down mode, execute the RDPD. During this command, the host drives CE# low, then sends the Deep Power-Down command cycle (ABH), and then drives CE# high. The device will return to Standby mode and be ready for the next instruction after TSBR.

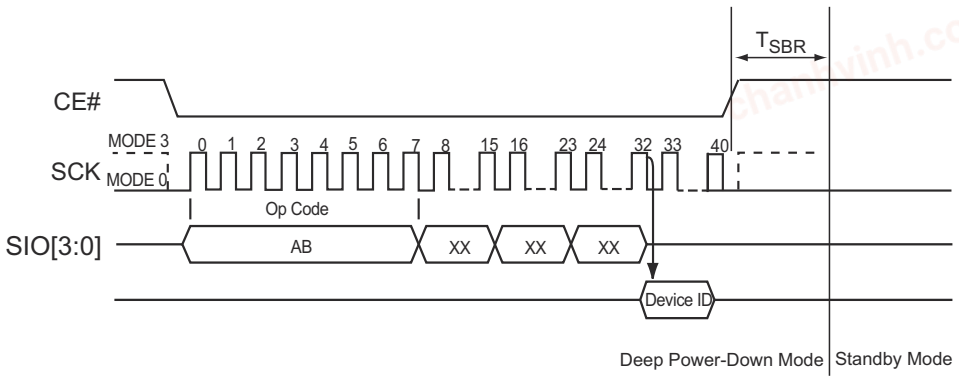
To execute RDPD and read the Device ID, the host drives CE# low then sends the Deep Power-Down command cycle (ABH), three dummy clock cycles, and then drives CE# high. The device outputs the Device ID on the falling edge of the SCK signal following the dummy cycles. The data output stream is continuous until terminated by a low-to-high transition on CE, and will return to Standby mode and be ready for the next instruction after TSBR. See Figures 5-42 and 5-43 for the command sequence.

FIGURE 5-42: RELEASE FROM DEEP POWER-DOWN (RDPD) AND READ ID SEQUENCE – SQI MODE



Note: C[1:0] = ABH

FIGURE 5-43: RELEASE FROM DEEP POWER-DOWN (RDPD) AND READ ID SEQUENCE – SPI MODE



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6.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (†)

Temperature under bias ..... -55°C to +125°C

Storage temperature ..... -65°C to +150°C

DC voltage on any pin to ground potential ..... -0.5V to VDD+0.5V

Transient voltage (<20 ns) on any pin to ground potential ..... -2.0V to VDD+2.0V

Package power dissipation capability (TA = 25°C) 1.0W

Surface mount solder reflow temperature ..... 260°C for 10 seconds

Output short circuit current[1] ..... 50 mA

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Output shorted for no more than one second. No more than one output shorted at a time.

TABLE 6-1: OPERATING RANGE

Range	Ambient Temp.	VDD
Industrial	-40°C to +85°C	2.3V-3.6V
Extended[1]	-40°C to +125°C	

Note 1: Maximum operating frequency for Extended temperature is 80 MHz.

TABLE 6-2: AC CONDITIONS OF TEST[1]

Input Rise/Fall Time	Output Load
3 ns	CL = 30 pF

Note 1: See Figure 8-6.

6.1 Power-Up Specifications

All functionalities and DC specifications are specified for a VDD ramp rate of greater than 1V per 100 ms (0V to 3.0V in less than 300 ms). See Table 6-3 and Figure 6-1 for more information.

When VDD drops from the operating voltage to below the minimum VDD threshold at power-down, all operations are disabled and the device does not respond to commands. Data corruption may result if a power-down occurs while a write registers, program, or erase operation is in progress. See Figure 6-2.

TABLE 6-3: RECOMMENDED SYSTEM POWER-UP/POWER-DOWN TIMINGS

Symbol	Parameter	Minimum	Maximum	Units	Condition
TPU-READ[1]	VDD Minimum to Read Operation	100	—	µs	
TPU-WRITE[1]	VDD Minimum to Write Operation	100	—	µs	
TPD[1]	Power-Down Duration	100	—	ms	
VOFF	VDD Off	—	0.3	V	0V recommended

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

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FIGURE 6-1: POWER-UP TIMING DIAGRAM

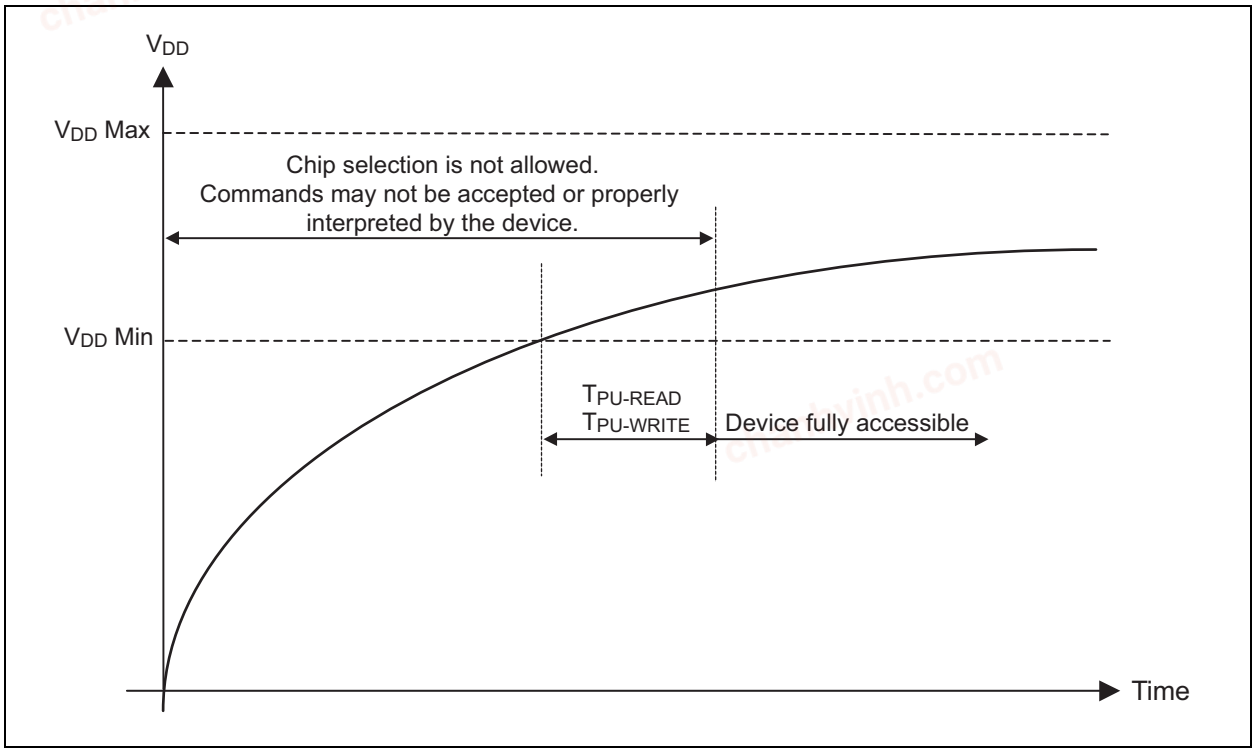
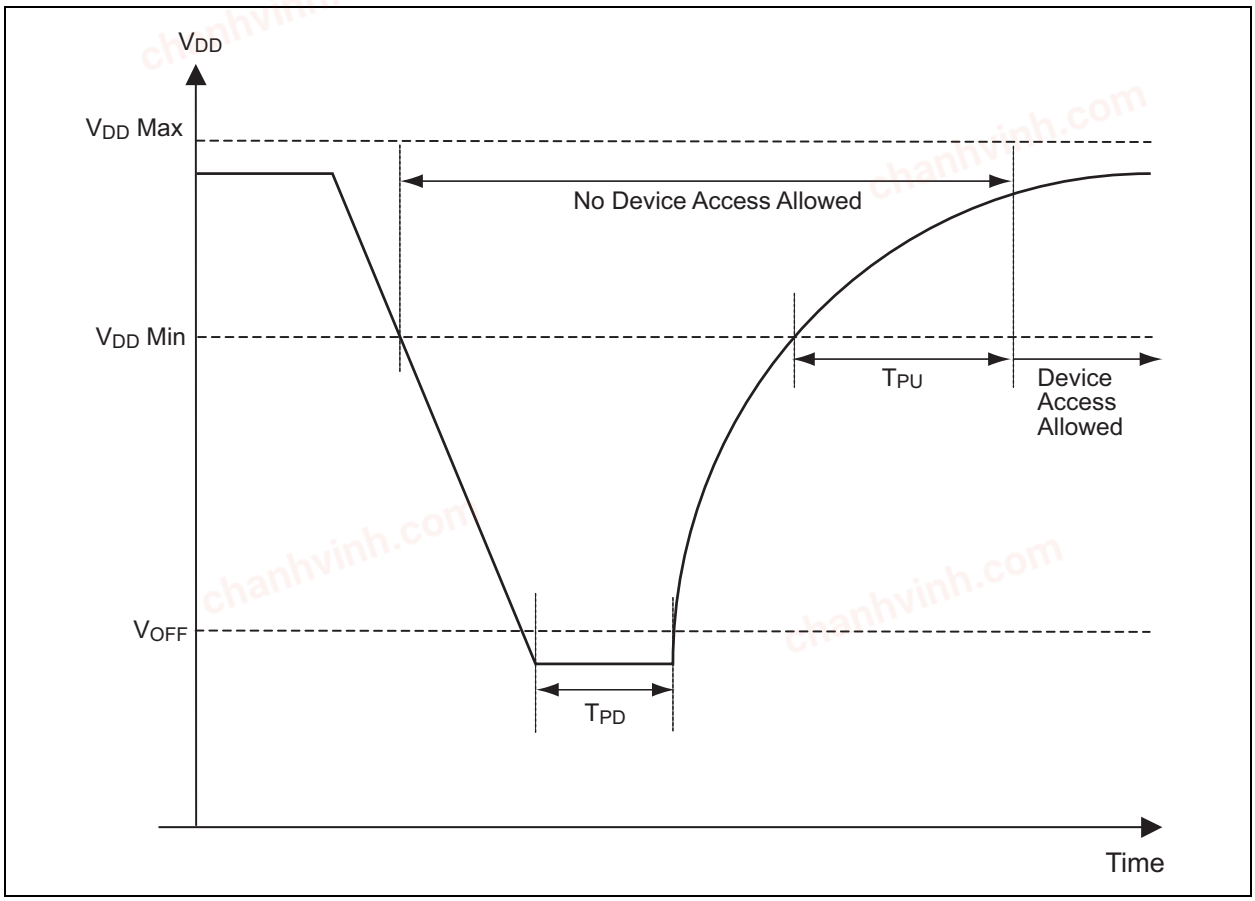


FIGURE 6-2: POWER-DOWN AND VOLTAGE DROP DIAGRAM



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7.0 DC CHARACTERISTICS

TABLE 7-1: DC OPERATING CHARACTERISTICS (V_{DD} = 2.3V-3.6V)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typical	Max.	Unit	
I_{DDR1}	Read Current	—	8	15	mA	V_{DD} = V_{DD} Max, CE# = 0.1 V_{DD}/0.9 V_{DD}@40 MHz, SO = Open
I_{DDR2}	Read Current	—	—	20	mA	V_{DD} = V_{DD} Max, CE# = 0.1 V_{DD}/0.9 V_{DD}@104 MHz, SO = Open
I_{DDW}	Program and Erase Current	—	—	25	mA	V_{DD} Max
I_{SB1}	Standby Current	—	15	30	µA	CE# =V_{DD}, V_{IN}=V_{DD} or V_{SS}
I_{SB2}	Standby Curent	—	—	50	µA	CE# =V_{DD}, V_{IN}=V_{DD} or V_{SS} at 125°C
I_{DPD1}	Deep Power-Down Current	—	8	20	µA	CE# = V_{DD}, V_{IN}=V_{DD} or V_{SS}
I_{DPD2}	Deep Power-Down Current	—	—	30	µA	CE# = V_{DD}, V_{IN}=V_{DD} or V_{SS} at 125°C
I_{LI}	Input Leakage Current	—	—	2	µA	V_{IN} = GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current	—	—	2	µA	V_{OUT} = GND to V_{DD}, V_{DD} = V_{DD} Max
V_{IL}	Input Low Voltage	—	—	0.8	V	V_{DD} = V_{DD} Min
V_{IH}	Input High Voltage	0.7 V_{DD}	—	—	V	V_{DD} = V_{DD} Max
V_{OL}	Output Low Voltage	—	—	0.2	V	I_{OL} = 100 µA, V_{DD} = V_{DD} Min
V_{OH}	Output High Voltage	V_{DD}-0.2	—	—	V	I_{OH} = -100 µA, V_{DD} = V_{DD} Min

TABLE 7-2: Capacitance (T_A = 25°C, f = 1 MHz, Other Pins Open)

Parameter	Description	Test Condition	Maximum
C_{OUT}(1)	Output Pin Capacitance	V_{OUT} = 0V	8 pF
C_{IN}(1)	Input Capacitance	V_{IN} = 0V	6 pF

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 7-3: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Unit	Test Method
N_{END}(1)	Endurance	100,000	Cycles	JEDEC Standard A117 and AEC-Q100-005
T_{DR}(1)	Data Retention	100	Years	JEDEC Standard A103 and AEC-Q100-005
I_{LTH}(1)	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78 and AEC-Q100-004

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 7-4: WRITE TIMING PARAMETERS (V_{DD} = 2.3V-3.6V)

Symbol	Parameter	Minimum	Maximum	Unit
T_{SE}	Sector Erase	—	25	ms
T_{BE}	Block Erase	—	25	ms
T_{SCE}	Chip Erase	—	50	ms
T_{PP}(1)	Page Program	—	1.5	ms
T_{PSID}	Program Security ID	—	1.5	ms
T_{WS}	Write Suspend Latency	—	25	µs
T_{CONFIG}	Configuration Register Write Latency	—	25	ms

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TABLE 7-4: WRITE TIMING PARAMETERS (V_{DD} = 2.3V-3.6V) (CONTINUED)

Symbol	Parameter	Minimum	Maximum	Unit

Note 1: Estimate for typical conditions less than 256 bytes: Programming Time (µs) = 55 + (3.75 x # of bytes).

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8.0 AC CHARACTERISTICS

TABLE 8-1: AC OPERATING CHARACTERISTICS (V_{DD}[1] = 2.3V-3.6V)

Symbol	Parameter	Limits - 40 MHz		Limits - 80 MHz[2]		Limits - 104 MHz		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
F_{CLK}	Serial Clock Frequency	—	40	—	80	—	104	MHz
T_{CLK}	Serial Clock Period	—	25	—	12.5	—	9.6	ns
T_{SCKH}	Serial Clock High Time	11	—	5.5	—	4.5	—	ns
T_{SCKL}	Serial Clock Low Time	11	—	5.5	—	4.5	—	ns
T_{SCKR}[3]	Serial Clock Rise Time (slew rate)	0.1	—	0.1	—	0.1	—	V/ns
T_{SCKF}[3]	Serial Clock Fall Time (slew rate)	0.1	—	0.1	—	0.1	—	V/ns
T_{CES}[4]	CE# Active Setup Time	8	—	5	—	5	—	ns
T_{CEH}[4]	CE# Active Hold Time	8	—	5	—	5	—	ns
T_{CHS}[4]	CE# Not Active Setup Time	8	—	5	—	5	—	ns
T_{CHH}[4]	CE# Not Active Hold Time	8	—	5	—	5	—	ns
T_{CPH}	CE# High Time	25	—	12.5	—	12	—	ns
T_{CHZ}	CE# High-to-High Z Output	—	19	—	12.5	—	12	ns
T_{CLZ}	SCK Low-to-Low Z Output	0	—	0	—	0	—	ns
T_{HLS}	HOLD# Low Setup Time	8	—	5	—	5	—	ns
T_{HHS}	HOLD# High Setup Time	8	—	5	—	5	—	ns
T_{HLH}	HOLD# Low Hold Time	8	—	5	—	5	—	ns
T_{HHH}	HOLD# High Hold Time	8	—	5	—	5	—	ns
T_{HZ}	HOLD# Low-to-High Z Output	—	8	—	8	—	8	ns
T_{LZ}	HOLD# High-to-Low Z Output	—	8	—	8	—	8	ns
T_{DS}	Data In Setup Time	3	—	3	—	3	—	ns
T_{DH}	Data In Hold Time	4	—	4	—	4	—	ns
T_{OH}	Output Hold from SCK Change	0	—	0	—	0	—	ns
T_V	Output Valid from SCK	—	8/5[5]	—	8/5[5]	—	8/5[5]	ns

Note 1: Maximum operating frequency for 2.7V-3.6V is 104 MHz and for 2.3V-3.6V is 80 MHz.

2: Maximum frequency for 125°C is 80 MHz.

3: Maximum Rise and Fall time may be limited by T_{SCKH} and T_{SCKL} requirements.

4: Relative to SCK.

5: 30 pF/10 pF

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FIGURE 8-1: HOLD TIMING DIAGRAM

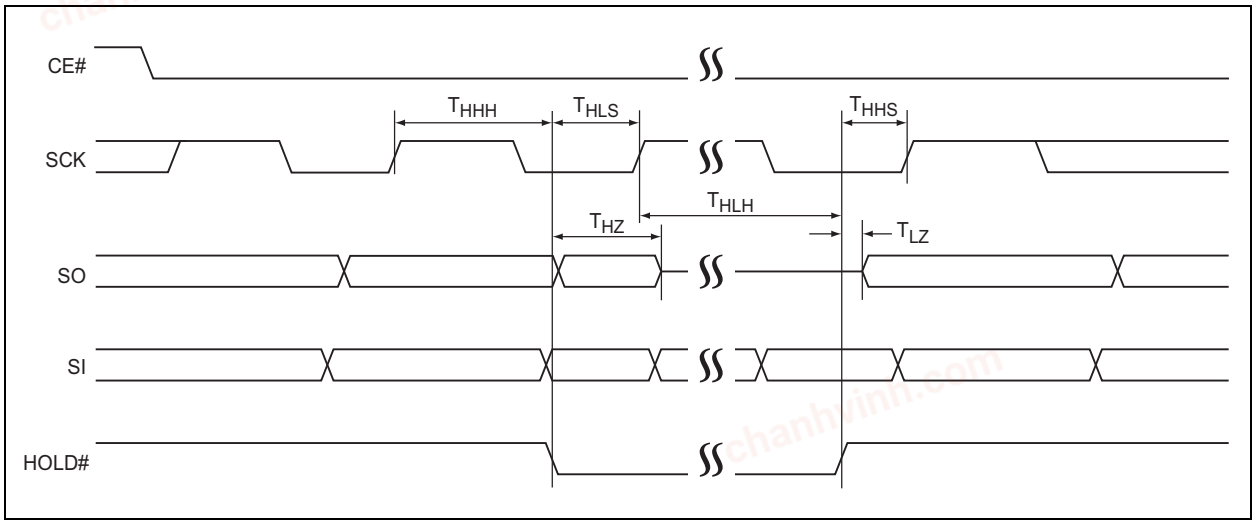


FIGURE 8-2: SERIAL INPUT TIMING DIAGRAM

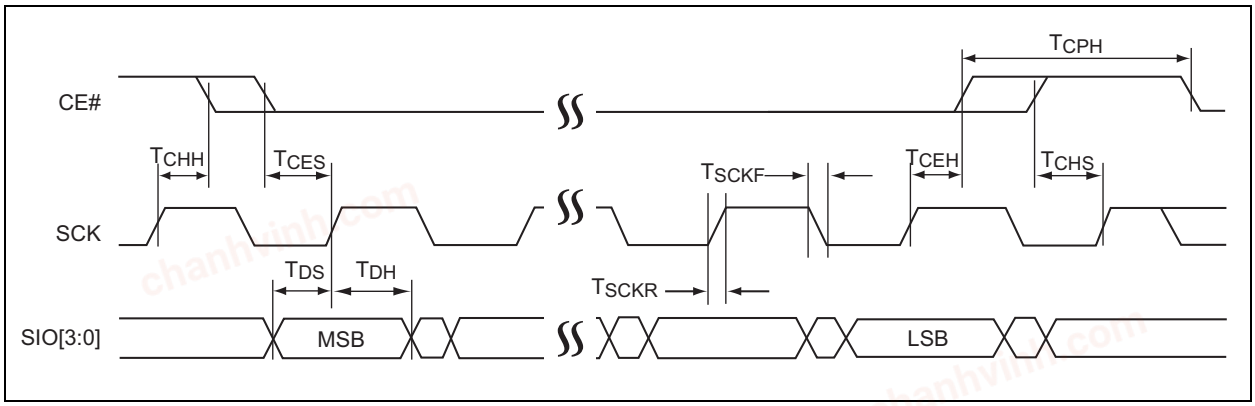
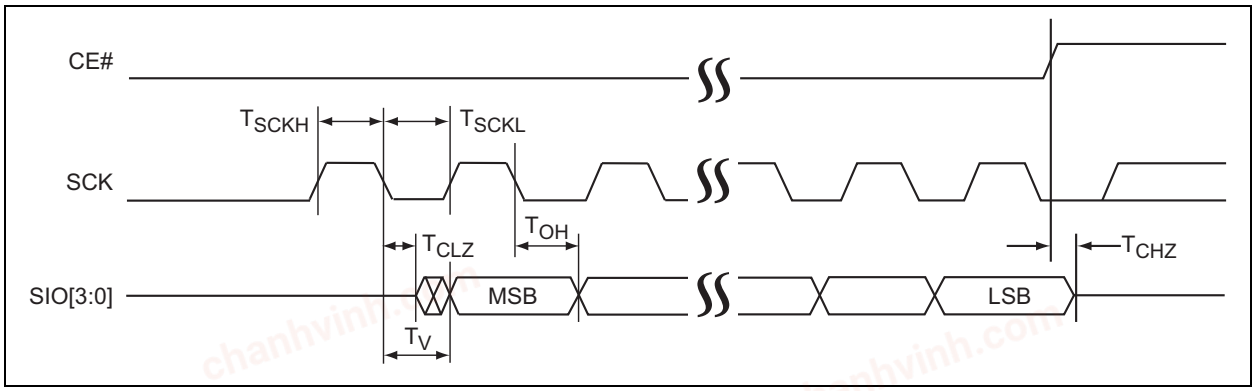
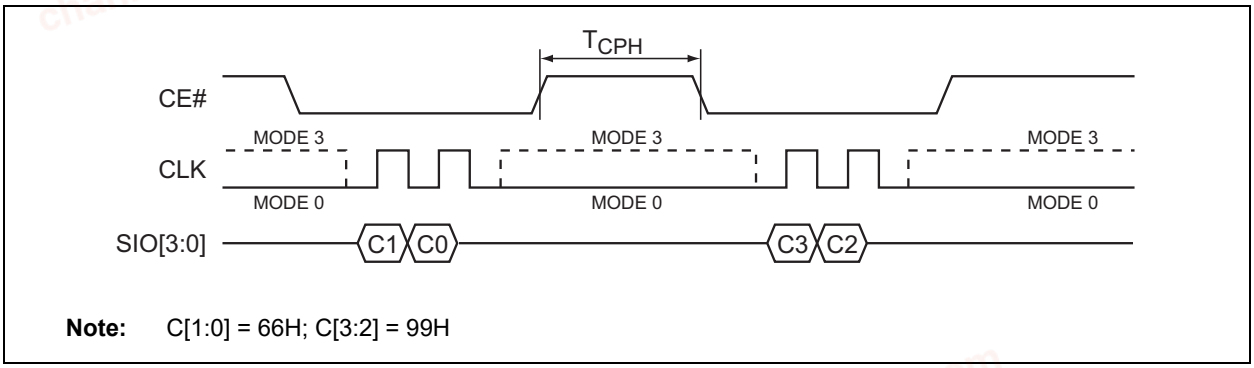


FIGURE 8-3: SERIAL OUTPUT TIMING DIAGRAM



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FIGURE 8-4: RESET TIMING DIAGRAM

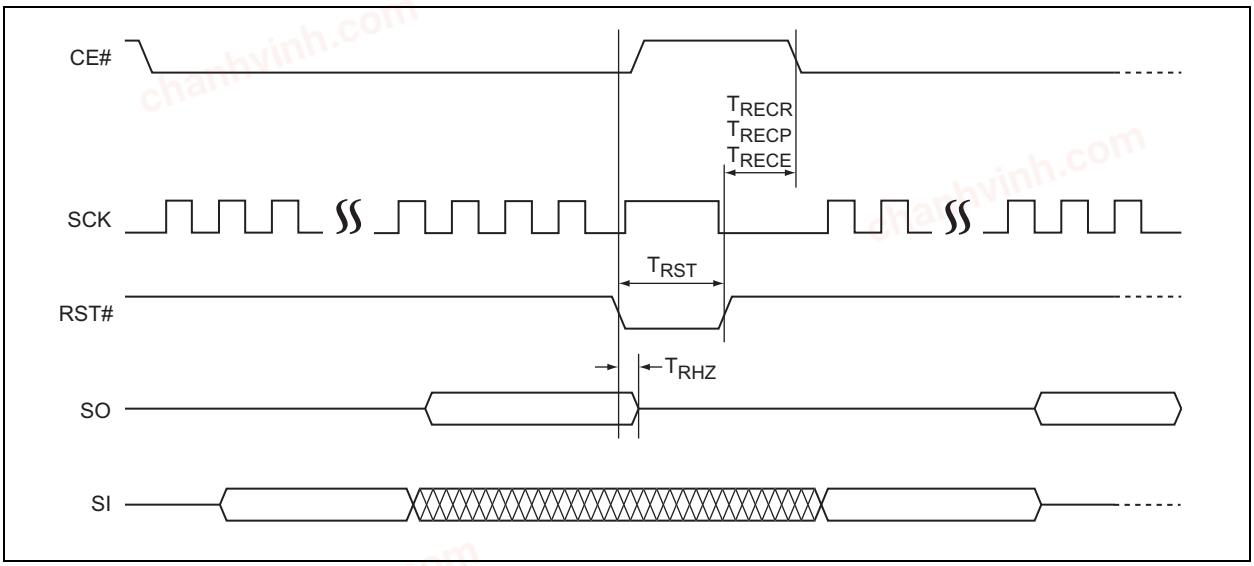


Note: C[1:0] = 66H; C[3:2] = 99H

TABLE 8-2: RESET TIMING PARAMETERS

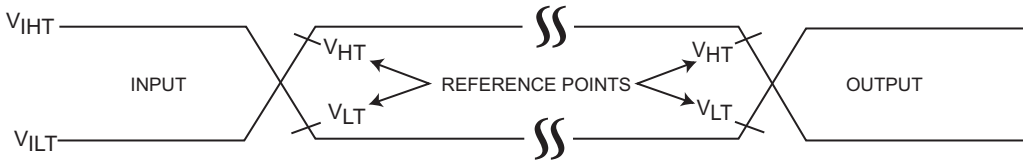
TR(I)	Parameter	Minimum	Maximum	Units
TRECR	Reset to Read (non-data operation)	—	20	ns
TRECP	Reset Recovery from Program or Suspend	—	100	µs
TRECE	Reset Recovery from Erase	—	1	ms
TRST	Reset Pulse Width (Hardware Reset)	100	—	ns
TRHZ	Reset to High Z Output	—	105	ns

FIGURE 8-5: HARDWARE RESET TIMING DIAGRAM



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FIGURE 8-6: AC INPUT/OUTPUT REFERENCE WAVEFORMS



AC test inputs are driven at V_{IHT} (0.9V_{DD}) for a logic '1' and V_{ILT} (0.1V_{DD}) for a logic '0'. Measurement reference points for inputs and outputs are V_{HT} (0.6V_{DD}) and V_{LT} (0.4V_{DD}). Input rise and fall times (10% ↔ 90%) are <3 ns.

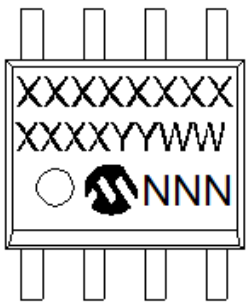
Note: V_{HT} - V_{HIGH} Test
V_{LT} - V_{LOW} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

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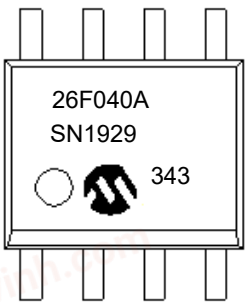
9.0 PACKAGING INFORMATION

9.1 Package Marking

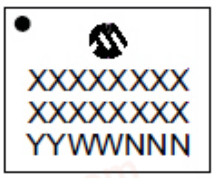
8-Lead SOIC (3.90 mm)



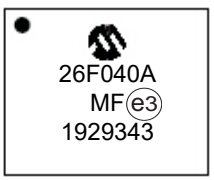
Example



8-Lead WDFN (5x6 mm)



Example



Part Number	1st Line Marking Codes	
	SOIC	WDFN
SST26VF040A	26F040A	26F040A

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)

Note: For very small packages with no room for the Pb-free JEDEC® designator (e3) , the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

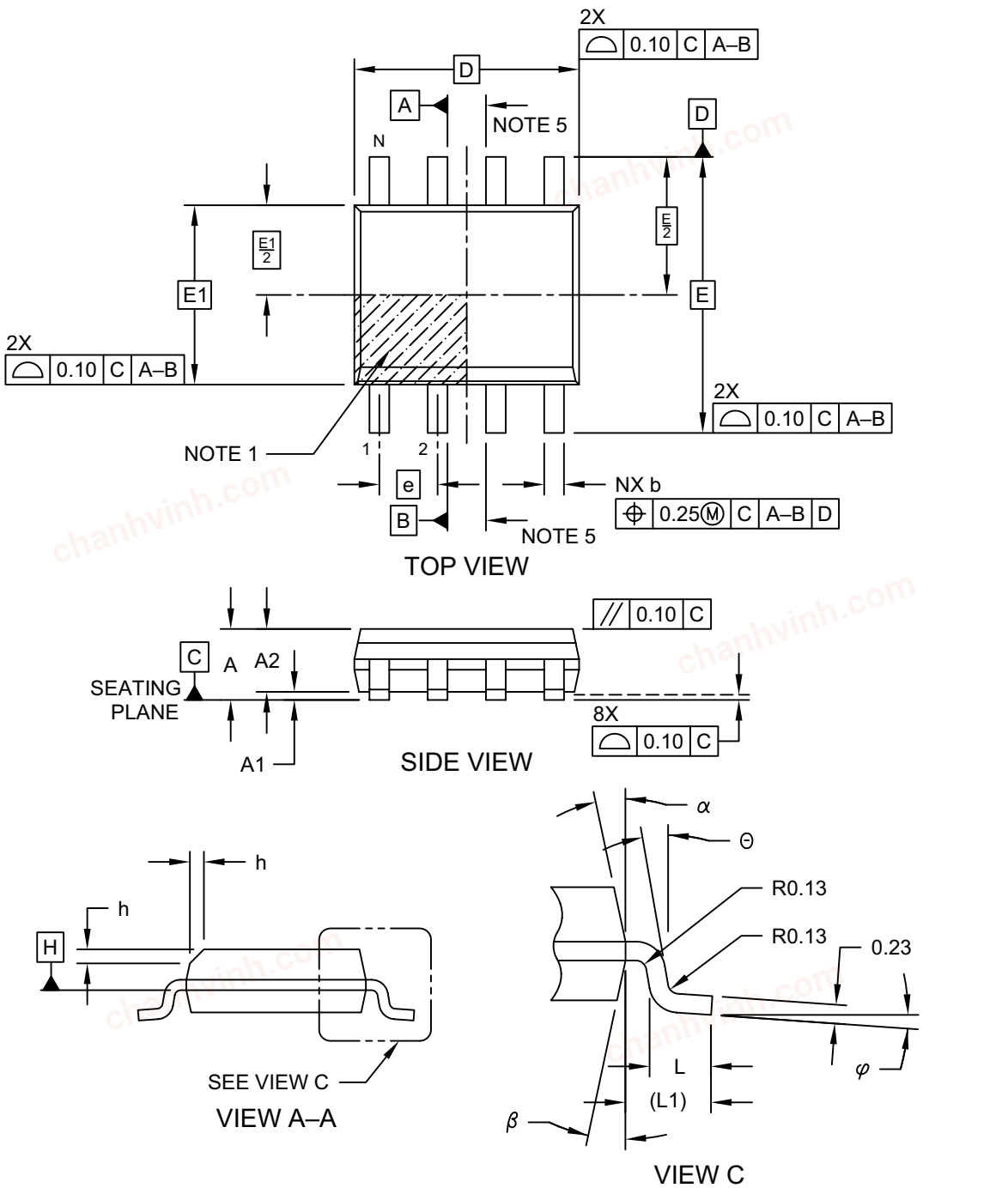
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9.2 Packaging Diagrams

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

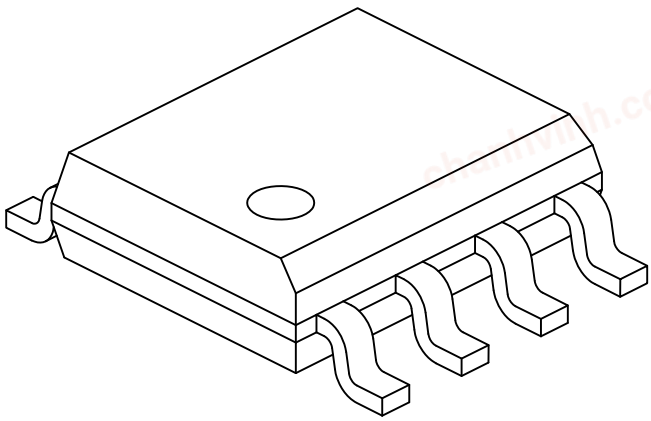


Microchip Technology Drawing No. C04-057-SN Rev F Sheet 1 of 2

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8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

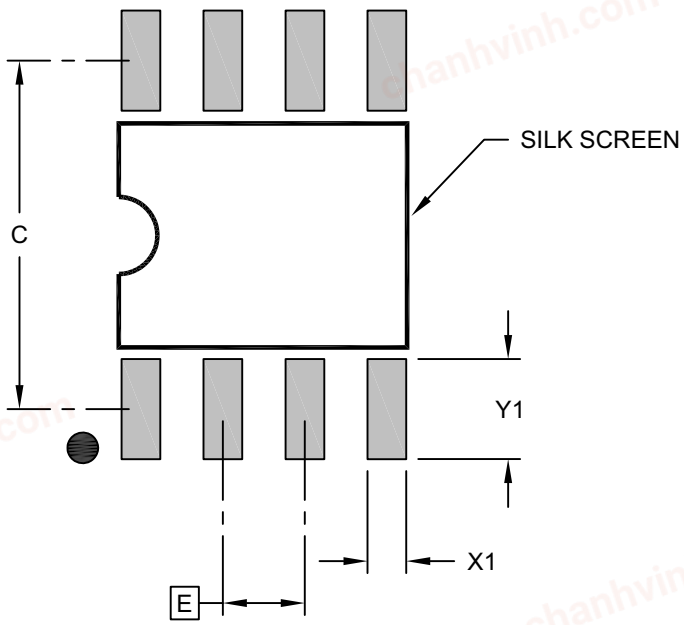
Microchip Technology Drawing No. C04-057-SN Rev F Sheet 2 of 2

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8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

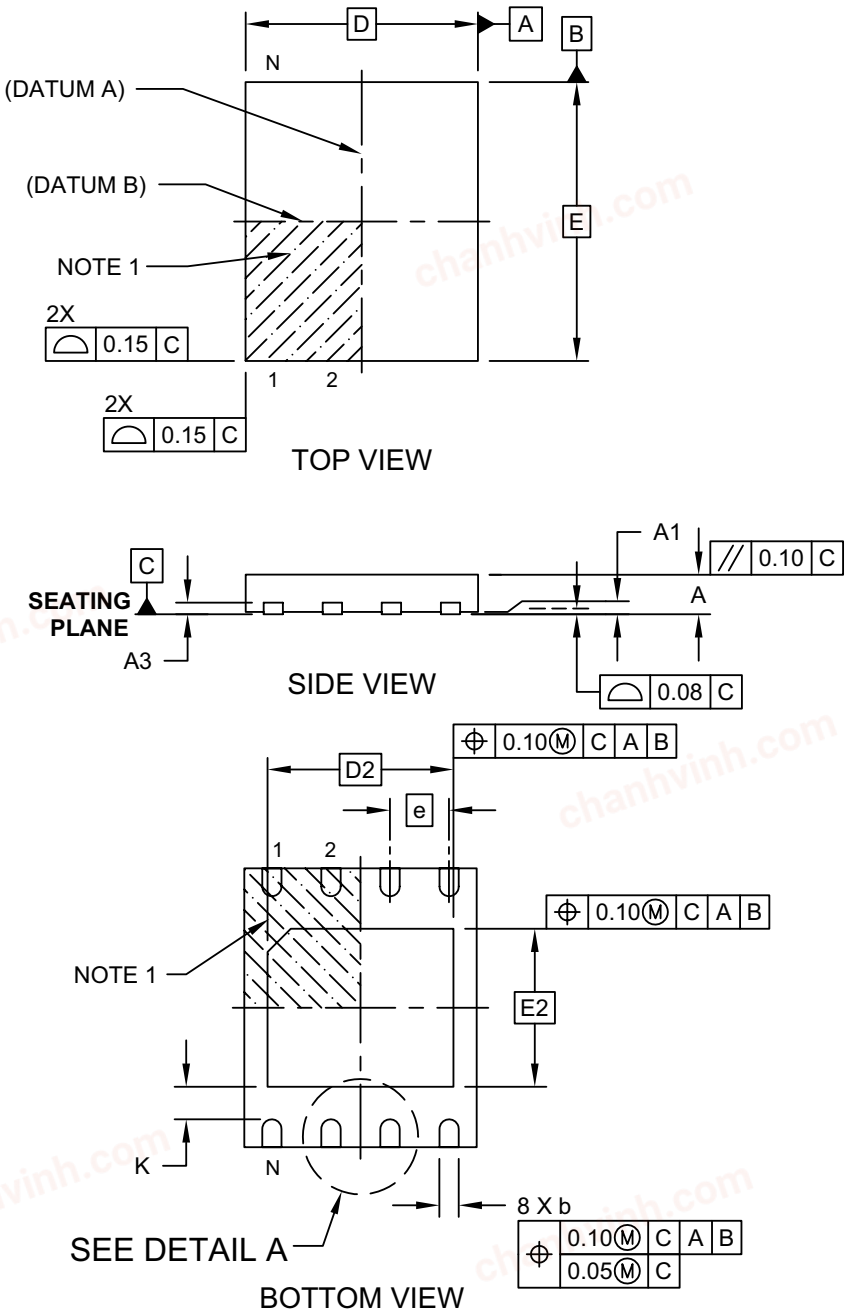
Microchip Technology Drawing C04-2057-SN Rev F

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8-Lead Plastic Very, Very Thin Small Outline No-Lead (MF) - 5x6 mm Body [WDFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

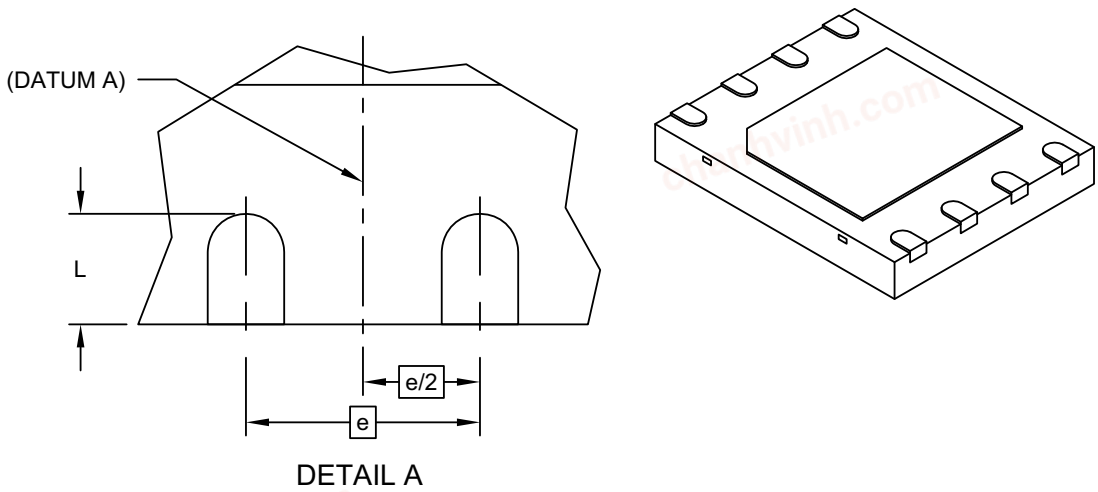


Microchip Technology Drawing C04-210B Sheet 1 of 2

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8-Lead Plastic Very, Very Thin Small Outline No-Lead (MF) - 5x6 mm Body [WDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	D		5.00 BSC	
Exposed Pad Width	D2		4.00 BSC	
Overall Length	E		6.00 BSC	
Exposed Pad Length	E2		3.40 BSC	
Terminal Width	b	0.35	0.42	0.48
Terminal Length	L	0.50	0.60	0.70
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

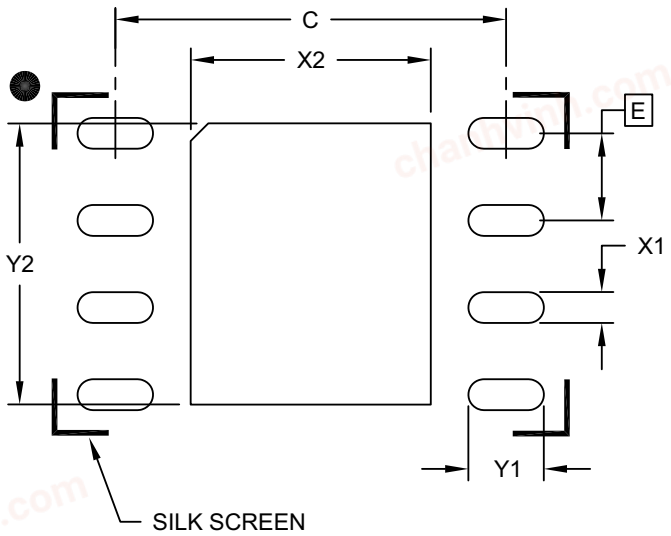
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8-Lead Plastic Very, Very Thin Small Outline No-Lead (MF) - 5x6 mm Body [WDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Optional Center Pad Width	X2			3.50
Optional Center Pad Length	Y2			4.10
Contact Pad Spacing	C		5.70	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.10

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2210A

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10.0 REVISION HISTORY

Revision B (July 2021)

Added note to Table 2-1. Updated Figure 5-13. Added Product Identification System (Automotive). Updated SOIC package drawing.

Revision A (January 2020)

Initial release of the document.

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PRODUCT IDENTIFICATION SYSTEM (NON-AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	–XXX	X	/XX
Device	Tape and Reel Indicator	Operating Frequency	Temperature	Package

Device:	SST26VF040A	= 4 Mbit, 2.5V/3.0V, SQI Flash memory WP#/Hold# pin enable at power-up
Tape and Reel Indicator:	Blank	= Standard packaging (tube or tray)
	T	= Tape and Reel(1)
Operating Frequency	104	= 104 MHz
	80	= 80 MHz
Temperature Range:	I	= -40°C to +85°C (Industrial)
	E	= -40°C to +125°C (Extended)
Package:	SN	= SOIC (3.90 mm Body), 8-lead
	MF	= WDFN (6 mm x 5 mm Body), 8-lead

Valid Combinations:

a) SST26VF040A-104I/SN
b) SST26VF040AT-104I/SN
c) SST26VF040A-104I/MF
d) SST26VF040AT-104I/MF

e) SST26VF040A-80E/SN
f) SST26VF040AT-80E/SN
g) SST26VF040A-80E/MF
h) SST26VF040AT-80E/MF

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	–XXX	X	/XX	XXX(2,3)
Device	Tape and Reel Indicator	Operating Frequency	Temperature	Package	Variant

Device:	SST26VF040A	= 4 Mbit, 2.5V/3.0V, SQI Flash memory WP#/Hold# pin enable at power-up
Tape and Reel Indicator:	Blank	= Standard packaging (tube or tray)
	T	= Tape and Reel(1)
Operating Frequency	104	= 104 MHz
	80	= 80 MHz
Temperature Range:	I	= -40°C to +85°C (AEC-Q100 Grade 3)
	E	= -40°C to +125°C (AEC-Q100 Grade 1)
Package:	SN	= SOIC (3.90 mm Body), 8-lead
	MF	= WDFN (6 mm x 5 mm Body), 8-lead
Variant(2,3):	VAO	= Standard Automotive
	VXX	= Customer Specific Automotive

Valid Combinations:

a) SST26VF040A-80E/SN70SVAO
b) SST26VF040A-80E/MF70SVAO
c) SST26VF040AT-80E/SN70SVAO
d) SST26VF040AT-80E/MF70SVAO

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: The VAO/VXX automotive variants have been designed, manufactured, tested and qualified in accordance with AEC-Q100 requirements for automotive applications.

3: For customers requesting a PPAP, a customer-specific part number will be generated and provided. A PPAP is not provided for VAO part numbers.

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11.0 APPENDIX

TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 1 OF 13)

Address	Bit Address	Data	Comments
SFDP Header			
SFDP Header: 1st DWORD			
00H	A7:A0	53H	**SFDP Signature** SFDP Signature = 50444653H
01H	A15:A8	46H	
02H	A23:A16	44H	
03H	A31:A24	50H	
SFDP Header: 2nd DWORD			
04H	A7:A0	06H	**SFDP Minor Revision Number**
05H	A15:A8	01H	**SFDP Major Revision Number**
06H	A23:A16	02H	**Number of Parameter Headers (NPH) = 3**
07H	A31:A24	FFH	**Unused**. Contains FF and cannot be changed.
Parameter Headers			
JEDEC Flash Parameter Header: 1st DWORD			
08H	A7:A0	00H	**Parameter ID LSB Number** When this field is set to 00H, it indicates a JEDEC-specified header. For vendor-specified headers, this field must be set to the vendor's manufacturer ID.
09H	A15:A8	06H	**Parameter Table Minor Revision Number** Minor revisions are either clarifications or changes that add parameters in existing Reserved locations. Minor revisions do NOT change overall structure of SFDP. Minor revision starts at 00H.
0AH	A23:A16	01H	**Parameter Table Major Revision Number** Major revisions are changes that reorganize or add parameters to locations that are NOT currently Reserved. Major revisions would require code (BIOS/firmware) or hardware change to get previously defined discoverable parameters. Major revision starts at 01H.
0BH	A31:A24	10H	**Parameter Table Length** Number of DWORDs that are in the Parameter table.
JEDEC Flash Parameter Header: 2nd DWORD			
0CH	A7:A0	30H	**Parameter Table Pointer (PTP)** A 24-bit address that specifies the start of this header's Parameter table in the SFDP structure. The address must be DWORD-aligned.
0DH	A15:A8	00H	
0EH	A23:A16	00H	
0FH	A31:A24	FFH	**Parameter ID MSB Number**
JEDEC Sector Map Parameter Header: 3rd DWORD			
10H	A7:A0	81H	**Parameter ID LSB Number** Sector Map Function specific table is assigned 81H.
11H	A15:A8	00H	**Parameter Table Minor Revision Number** Minor revisions are either clarifications or changes that add parameters in existing Reserved locations. Minor revisions do NOT change overall structure of SFDP. Minor revision starts at 00H.
12H	A23:A16	01H	**Parameter Table Major Revision Number** Major revisions are changes that reorganize or add parameters to locations that are NOT currently Reserved. Major revisions would require code (BIOS/firmware) or hardware change to get previously defined discoverable parameters. Major revision starts at 01H.
13H	A31:A24	02H	**Parameter Table Length** Number of DWORDs that are in the Parameter table.

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TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 2 OF 13)

Address	Bit Address	Data	Comments
JEDEC Sector Map Parameter Header: 4th DWORD			
14H	A7:A0	00H	**Parameter Table Pointer (PTP)** This 24-bit address specifies the start of this header's Parameter table in the SFDP structure. The address must be DWORD-aligned.
15H	A15:A8	01H	
16H	A23:A16	00H	
17H	A31:A24	FFH	**Parameter ID MSB Number**
Microchip (Vendor) Parameter Header: 5th DWORD			
18H	A7:A0	BFH	**ID Number** Manufacture ID (vendor specified header)
19H	A15:A8	00H	**Parameter Table Minor Revision Number**
1AH	A23:A16	01H	**Parameter Table Major Revision Number**, Revision 1.0
1BH	A31:A24	13H	**Parameter Table Length**, 19 Double Words
Microchip (Vendor) Parameter Header: 6th DWORD			
1CH	A7:A0	00H	**Parameter Table Pointer (PTP)** This 24-bit address specifies the start of this header's Parameter table in the SFDP structure. The address must be DWORD-aligned.
1DH	A15:A8	02H	
1EH	A23:A16	00H	
1FH	A31:A24	01H	Used to indicate bank number (vendor specific).
JEDEC Flash Parameter Table			
JEDEC Flash Parameter Table: 1st DWORD			
30H	A1:A0	FDH	**Block/Sector Erase Sizes** 00: Reserved **01: 4-Kbyte Erase** 10: Reserved 11: Use this setting only if the 4-Kbyte erase is unavailable.
	A2		**Write Granularity** 0: Single-byte programmable devices or buffer programmable devices with buffer is less than 64 bytes (32 words). **1: For buffer programmable devices when the buffer size is 64 bytes (32 words) or larger**.
	A3		**Volatile STATUS Register** 0: Target Flash has nonvolatile Status bit. Write/Erase commands do not require STATUS register to be written on every power-on. **1: Target Flash has volatile Status bits**.
	A4		**Write Enable Opcode Select for Writing to Volatile STATUS Register** 0: 0x50. Enables a STATUS register write when bit 3 is set to '1'. **1: 0x06 Enables a STATUS register write when bit 3 (A3) is set to '1'**.
	A7:A5		**Unused**. Contains 111b and cannot be changed.
31H	A15:A8	20H	**4-Kbyte Erase Opcode**

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TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 3 OF 13)

Address	Bit Address	Data	Comments
32H	A16	F1H	**Supports (1-1-2) Fast Read** 0: (1-1-2) Fast Read NOT supported **1: (1-1-2) Fast Read supported**
	A18:A17		**Address Bytes** Number of bytes used in addressing Flash array read, write and erase **00: 3-Byte only addressing** 01: 3- or 4-Byte addressing (e.g., defaults to 3-Byte mode; enters 4-Byte mode on command) 10: 4-Byte only addressing 11: Reserved
	A19		**Supports Double Transfer Rate (DTR) Clocking** Indicates the device supports some type of double transfer rate clocking. **0: DTR NOT supported** 1: DTR Clocking supported
	A20		**Supports (1-2-2) Fast Read** Device supports single input opcode, dual input address, and dual output data Fast Read. 0: (1-2-2) Fast Read NOT supported **1: (1-2-2) Fast Read supported**
	A21		**Supports (1-4-4) Fast Read** Device supports single input opcode, quad input address, and quad output data Fast Read 0: (1-4-4) Fast Read NOT supported **1: (1-4-4) Fast Read supported**
	A22		**Supports (1-1-4) Fast Read** Device supports single input opcode & address and quad output data Fast Read. 0: (1-1-4) Fast Read NOT supported **1: (1-1-4) Fast Read supported**
	A23		**Unused**. Contains '1' cannot be changed.
33H	A31:A24	FFH	**Unused**. Contains FF cannot be changed.
JEDEC Flash Parameter Table: 2nd DWORD			
34H	A7:A0	FFH	**Flash Memory Density** SST26VF040A = 003FFFFFH
35H	A15:A8	FFH	
36H	A23:A16	3FH	
37H	A31:A24	00H	
JEDEC Flash Parameter Table: 3rd DWORD			
38H	A4:A0	44H	**(1-4-4) Fast Read Number of Wait states (dummy clocks) needed before valid output** 00100b: 4 dummy clocks (16 dummy bits) are needed with a Quad Input Address Phase instruction.
	A7:A5		**Quad Input Address Quad Output (1-4-4) Fast Read Number of Mode Bits** 010b: 2 dummy clocks (8 mode bits) are needed with a single input opcode, quad input address and quad output data Fast Read instruction.
39H	A15:A8	EBH	**(1-4-4) Fast Read Opcode** Opcode for single input opcode, quad input address and quad output data Fast Read instruction.

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TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 4 OF 13)

Address	Bit Address	Data	Comments
3AH	A20:A16	08H	**(1-1-4) Fast Read Number of Wait states (dummy clocks) needed before valid output** 01000b: 8 dummy bits are needed with a single input opcode & address and quad output data Fast Read instruction.
	A23:A21		**(1-1-4) Fast Read Number of Mode Bits** 000b: No mode bits are needed with a single input opcode & address and quad output data Fast Read instruction.
3BH	A31:A24	6BH	**(1-1-4) Fast Read Opcode** Opcode for single input opcode & address and quad output data Fast Read instruction.
JEDEC Flash Parameter Table: 4th DWORD			
3CH	A4:A0	08H	**(1-1-2) Fast Read Number of Wait states (dummy clocks) needed before valid output** 01000b: 8 dummy clocks are needed with a single input opcode, address and dual output data Fast Read instruction.
	A7:A5		**(1-1-2) Fast Read Number of Mode Bits** 000b: No mode bits are needed with a single input opcode & address and quad output data Fast Read instruction.
3DH	A15:A8	3BH	**(1-1-2) Fast Read Opcode** Opcode for single input opcode & address and dual output data Fast Read instruction.
3EH	A20:A16	80H	**(1-2-2) Fast Read Number of Wait states (dummy clocks) needed before valid output** 00000b: 0 clocks of dummy cycle.
	A23:A21		**(1-2-2) Fast Read Number of Mode Bits (in clocks)** 100b: 4 clocks of mode bits are needed.
3FH	A31:A24	BBH	**(1-2-2) Fast Read Opcode** Opcode for single input opcode, dual input address, and dual output data Fast Read instruction.
JEDEC Flash Parameter Table: 5th DWORD			
40H	A0	FEH	**Supports (2-2-2) Fast Read** Device supports dual input opcode & address and dual output data Fast Read. **0: (2-2-2) Fast Read NOT supported** 1: (2-2-2) Fast Read supported
	A3:A1		**Reserved**. Bits default to all 1's.
	A4		**Supports (4-4-4) Fast Read** Device supports Quad input opcode & address and quad output data Fast Read. 0: (4-4-4) Fast Read NOT supported **1: (4-4-4) Fast Read supported**
	A7:A5		**Reserved**. Bits default to all 1's.
41H	A15:A8	FFH	**Reserved**. Bits default to all 1's.
42H	A23:A16	FFH	**Reserved**. Bits default to all 1's.
43H	A31:A24	FFH	**Reserved**. Bits default to all 1's.
JEDEC Flash Parameter Table: 6th DWORD			
44H	A7:A0	FFH	**Reserved**. Bits default to all 1's.
45H	A15:A8	FFH	**Reserved**. Bits default to all 1's.

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TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 5 OF 13)

Address	Bit Address	Data	Comments
46H	A20:A16	00H	**(2-2-2) Fast Read Number of Wait states (dummy clocks) needed before valid output** 00000b: No dummy bit is needed
	A23:A21		**(2-2-2) Fast Read Number of Mode Bits** 000b: No mode bits are needed
47H	A31:A24	FFH	**(2-2-2) Fast Read Opcode** Opcode for dual input opcode & address and dual output data Fast Read (not supported).
JEDEC Flash Parameter Table: 7th DWORD			
48H	A7:A0	FFH	**Reserved**. Bits default to all 1's.
49H	A15:A8	FFH	**Reserved**. Bits default to all 1's.
4AH	A20:A16	44H	**(4-4-4) Fast Read Number of Wait states (dummy clocks) needed before valid output** 00100b: 4 clocks dummy are needed with a quad input opcode & address and quad output data Fast Read instruction.
	A23:A21		**(4-4-4) Fast Read Number of Mode Bits** 010b: 2 clocks mode bits are needed with a quad input opcode & address and quad output data Fast Read instruction.
4BH	A31:A24	0BH	**(4-4-4) Fast Read Opcode** Opcode for quad input opcode/address, quad output data Fast Read.
JEDEC Flash Parameter Table: 8th DWORD			
4CH	A7:A0	0CH	**Sector Type 1 Size** 4-Kbyte, Sector/Block size = 2^N bytes
4DH	A15:A8	20H	**Sector Type 1 Opcode** Opcode used to erase the number of bytes specified by Sector Type 1 Size.
4EH	A23:A16	0FH	**Sector Type 2 Size** 32-Kbyte, Sector/Block size = 2^N bytes
4FH	A31:A24	D8H	**Sector Type 2 Opcode** Opcode used to erase the number of bytes specified by Sector Type 2 Size.
JEDEC Flash Parameter Table: 9th DWORD			
50H	A7:A0	10H	**Sector Type 3 Size** 64-Kbyte, Sector/Block size = 2^N bytes
51H	A15:A8	D8H	**Sector Type 3 Opcode** Opcode used to erase the number of bytes specified by Sector Type 3 Size.
52H	A23:A16	00H	**Sector Type 4 Size** 64-Kbyte, Sector/Block size = 2^N bytes
53H	A31:A24	00H	**Sector Type 4 Opcode** Opcode used to erase the number of bytes specified by Sector Type 4 Size.
JEDEC Flash Parameter Table: 10th DWORD			
54H	A3:A0	20H	Multiplier from typical erase time to maximum erase time. Maximum time = 2*(count +1)*Typical erase time Count = 0 **A3:A0 = 0000b**
	A7:A4		Erase Type 1 Erase, Typical time Typical time = (count+1)*units 1 ms to 32 ms, 16 ms to 512 ms, 128 ms to 4096 ms, 1s to 32s 10:9 units (**00b: 1 ms**, 01b: 16 ms, 10b: 128 ms, 11b: 1s) **A8:A4 count = 18 = 10010b** **A10:A9 unit = 1 ms = 00b**

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TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 6 OF 13)

Address	Bit Address	Data	Comments
55H	A10:A8	91H	**A10:A8 = 001b**
	A15:A11		Erase Type 2 Erase, Typical time Typical time = (count+1)*units 1 ms to 32 ms, 16 ms to 512 ms, 128 ms to 4096 ms, 1s to 32s 17:16 units (**00b: 1 ms**, 01b: 16 ms, 10b: 128 ms, 11b: 1s) **A15:A11 count = 18 = 10010b** **A17:A16 unit = 1 ms = 00b**
56H	A17:A16	48H	**A17:A16 = 00b**
	A23:A18		Erase Type 3 Erase, Typical time Typical time = (count+1)*units 1 ms to 32 ms, 16 ms to 512 ms, 128 ms to 4096 ms, 1s to 32s 24:23 units (**00b: 1 ms**, 01b: 16 ms, 10b: 128 ms, 11b: 1s) **A22:A18 count = 18 = 10010b** **A24:A23 unit = 1ms = 00b**
57H	A24	24H	**A24 = 0b**
	A31:A25		Erase Type 4 Erase, Typical time Typical time = (count+1)*units 1 ms to 32 ms, 16 ms to 512 ms, 128 ms to 4096 ms, 1s to 32s 31:30 units (**00b: 1 ms**, 01b: 16 ms, 10b: 128 ms, 11b: 1s) **A29:A25 count = 18 = 10010b** **A31:A30 unit = 1 ms = 00b**
JEDEC Flash Parameter Table: 11th DWORD			
58H	A3:A0	80H	Multiplier from typical program time to maximum program time Maximum time = 2*(count +1)*Typical program time **Count = 0** **A3:A0 = 0000b**
	A7:A4		Page Size Page size = 2^N bytes **N = 8** **A7:A4 = 1000b**
59H	A31:A8	6FH	Page Program Typical time, Program time = (count+1)*units 13 units (0b: 8 µs, **1b: 64 µs**) **A12:A8 count = 11 = 01111b** **A13 unit = 64 µs = 1b**
	A15:A14		Byte Program Typical time, first byte Typical time = (count+1)*units 18 units (0b: 1 µs, **1b: 8 µs)** **A17:A14 count = 5 = 0101b** **A18 = 8 µs = 1b**
5AH	A18:A16	1DH	**A18:A16 = 101b**
	A23:A19		Byte Program Typical time, additional byte Typical time = (count+1)*units 23 units (**0b: 1 µs**, 1b: 8 µs) **A22:A19 count = 0011b** **A23 = 1 µs = 0b**

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TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 7 OF 13)

Address	Bit Address	Data	Comments
5AH	A30:A24	81H	Chip Erase Typical time Typical time = (count+1)*units 16 ms to 512 ms, 256 ms to 8192 ms, 4s to 128s, 64s to 2048s **A28:A24 count = 1 = 00001b** **A30:A29 units = 16 ms = 00b**
	A31		Reserved **A31 = 1b**
JEDEC Flash Parameter Table: 12th DWORD			
5CH	A3:A0	EDH	Prohibited Operations During Program Suspend xxx0b: May not initiate a new erase anywhere **xxx1b: May not initiate a new erase in the program suspended page size** **xx0xb: May not initiate a new page program anywhere** xx1xb: May not initiate a new page program in program suspended page size x0xxb: Refer to the data sheet **x1xxb: May not initiate a read in the program suspended page size** 0xxxb: Additional erase or program restrictions apply **1xxxb: The erase and program restrictions in bits 1:0 are sufficient**
	A7:A4		Prohibited Operation During Erase Suspend **xxx0b: May not initiate a new erase anywhere** xxx1b: May not initiate a new erase in the erase suspended page size xx0xb: May not initiate a new page program anywhere **xx1xb: May not initiate a new page program in erase suspended erase type size** x0xxb: Refer to the data sheet **x1xxb: May not initiate a read in the erase suspended page size** 0xxxb: Additional erase or program restrictions apply **1xxxb: The erase and program restrictions in bits 5:4 are sufficient**
5DH	A8	0FH	Reserved = 1b
	A12:A9		Program Resume to Suspend Interval The device requires this typical amount of time to make progress on the program operation before allowing another suspend. Interval = 500 µs Program resume to suspend interval = (count+1)*64 µs A12:A9 = 7 = **0111b**
	A15:A13		Suspend in-progress program max latency Maximum time required by the Flash device to suspend an in-progress program and be ready to accept another command which accesses the Flash array. Max. latency = 25 µs program max. latency =(count+1)*units units (00b: 128 ns, 01b: 1 µs, 10b: 8 µs, 11b: 64 µs) **A17:A13 = count = 24 = 11000b** **A19:A18 = 1 µs = 01b**
5EH	A19:A16	77H	**0111b**
	A23:A20		Erase Resume to Suspend Interval The device requires this typical amount of time to make progress on the erase operation before allowing another suspend. Interval = 500 µs Erase resume to suspend interval = (count+1)*64 µs A23:A20 = 7 = **0111b**

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TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 8 OF 13)

Address	Bit Address	Data	Comments
5FH	A30:A24	38H	Suspend in-progress erase max. latency Maximum time required by the Flash device to suspend an in-progress erase and be ready to accept another command which accesses the Flash array. Max. latency = 25 µs Erase max. latency = (count+1)*units units (00b: 128 ns, 01b: 1µs, 10b: 8 µs, 11b: 64 µs) **A28:A24= count = 24 = 11000b** **A30:A29 = 1 µs = 01b**
	A31		Suspend/Resume supported **0: supported** 1: not supported
JEDEC Flash Parameter Table: 13th DWORD			
60H	A7:A0	30H	Program Resume Instruction
61H	A15:A8	B0H	Program Suspend Instruction
62H	A23:A16	30H	Resume Instruction
63H	A31:A24	B0H	Suspend Instruction
JEDEC Flash Parameter Table: 14th DWORD			
64H	A1:A0	F7H	Reserved = 11b
	A7:A2		STATUS Register Polling Device Busy 111101b: Use of legacy polling is supported by reading the STATUS register with 05h instruction and checking WIP bit [0] (0 = ready, 1 = busy)
65H	A14:A8	A9H	Exit Deep Power-Down to next operation delay – 10 µs Delay = (count+1)*unit A12:A8 = count = 9 = 01001b A14:A13 units = 01b = 1 µs
	A15		Exit Power-Down Instruction – ABH= 10101011b A15 = 1b
66H	A22:A16	D5H	A22:A16 = 1010101b
	A23		Enter Power-Down Instruction – B9H = 10111001b A23 = 1b
67H	A30:A24	5CH	A30:A24 = 1011100
	A31		Deep Power-Down Supported **0: supported** 1: not supported
JEDEC Flash Parameter Table: 15th DWORD			
68H	A3:A0	29H	4-4-4 mode disable sequences Xxx1b: issue FF instruction 1xxxb: issue the Soft Reset 66/99 sequence
	A7:A4		4-4-4 mode enable sequences X_xx1xb: issue instruction 38H
69H	A8	C2H	4-4-4 mode enable sequences A8 = 0
	A9		0-4-4 mode supported 0: not supported **1: supported**
	A15:A10		0-4-4 Mode Exit Method X1_xxxx: Mode Bit[7:0] Not = AXh 1x_xxxx: Reserved = 1

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TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 9 OF 13)

Address	Bit Address	Data	Comments
6AH	A19:A16	5CH	0-4-4 Mode Entry Method **X1xxb: M[7:0] = AXh** 1xxxb: Reserved = 1
	A22:A20		Quad Enable Requirements (QER) **101b: Quad Enable is bit 1 of the Configuration register**.
	A23		HOLD and Reset Disable **0: feature is not supported**
6BH	A31:A24	FFH	Reserved bits = 0xFF
JEDEC Flash Parameter Table: 16th DWORD			
6C	A6:A0	F0H	Volatile or Nonvolatile Register and Write Enable Instructions for STATUS Register 1 Xx1_xxxxb: STATUS Register 1 contains a mix of volatile and nonvolatile bits. The 06h instruction is used to enable writing to the register. X1x_xxxxb: Reserved = 1 1xx_xxxxb: Reserved = 1
	A7		Reserved =1b
6D	A13:A8	30H	Soft Reset and Rescue Sequence Support X1_xxxxb: Reset Enable instruction 66h is issued followed by Reset instruction 99h. 1x_xxxxb: exit 0-4-4 mode is required prior to other Reset sequences.
	A15:A14		Exit 4-Byte Addressing Not supported
6E	A23:A16	C0H	Exit 4-Byte Addressing Not supported A21:A14 = 00000000b A23 and A22 are Reserved bits which are = 1
6F	A31:A24	80H	Enter 4-Byte Addressing Not supported 1xxx_xxxx: Reserved = 1
JEDEC Sector Map Parameter Table			
100H	A7:A0	FFH	A7:A2 = Reserved = 111111b A1 = Descriptor Type = Map = 1b A0 = Last map = 1b
101H	A15:A8	00H	Configuration ID = 00h
102H	A23:A16	00H	Region Count = 1 Region
103H	A31:A24	FFH	Reserved = FFh
104H	A7:A0	F7H	Region 0 supports 4-Kbyte erase, 32-Kbyte erase and 64-Kbyte erase A3:A0 = 0111b A7:A4 = Reserved = 1111b
105H	A15:A8	FFH	Region 0 Size For 4 Mbit device Count = 4 Mbit/256 bytes = 2048 Value = count - 1 = 2047 A31:A8 = 0007FFh
106H	A23:A16	07H	
107H	A31:A24	00H	

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TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 10 OF 13)

Address	Bit Address	Data	Comments
SST26VF040A (Vendor) Parameter Table			
SST26VF040A Identification			
200H	A7:A0	BFH	**Manufacturer ID**
201H	A15:A8	26H	**Memory Type**
202H	A23:A16	14H	**Device ID** SST26VF040A = 14H
203H	A31:A24	FFH	**Reserved**. Bits default to all 1's.
SST26VF040A Interface			
204H	A2:A0	B9H	**Interfaces Supported** 000: SPI only **001: Power-up default is SPI; Quad can be enabled/disabled** 010: Reserved • • • 111: Reserved
	A3		**Supports Enable Quad** 0: not supported **1: supported**
	A6:A4		**Supports Hold#/RST# Function** 000: Hold# 001: RST# 010: HOLD/RST# **011: I/O when in SQI(4-4-4), 1-4-4 or 1-1-4 Read**
	A7		**Supports Software Reset** 0: not supported **1: supported**
205H	A8	DFH	**Supports Quad Reset** 0: not supported **1: supported**
	A10:A9		**Reserved**. Bits default to all 1's.
	A13:A11		**Byte-Program or Page-Program (256 Bytes)** **011:** Byte Program/Page Program in SPI and Quad Page Program once Quad is enabled
	A14		**Program-Erase Suspend Supported** 0: Not Supported **1: Program/Erase Suspend Supported**
	A15		**Deep Power-Down Mode Supported** 0: Not Supported **1: Deep Power-Down Mode Supported**

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TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 11 OF 13)

Address	Bit Address	Data	Comments
206H	A16	F3H	**OTP Capable (Security ID) Supported** 0: not supported **1: supported**
	A17		**Supports Block Group Protect** 0: not supported **1: supported**
	A18		**Supports Independent Block Protect** **0: not supported** 1: supported
	A19		**Supports Independent Nonvolatile Lock (Block or Sector becomes OTP)** **0: not supported** 1: supported
	A23:A20		**Reserved**. Bits default to all 1's.
207H	A31:A24	FFH	**Reserved**. Bits default to all 1's.
208H	A7:A0	30H	**VDD Minimum Supply Voltage** 2.30V (F230)
209H	A15:A8	F2H	
20AH	A23:A16	60H	**VDD Maximum Supply Voltage** 3.60V (F360H)
20BH	A31:A24	F3H	
20CH	A7:A0	32H	**Typical Time-out for Byte Program: 50 µs** Typical time-out for Byte Program is in µs. Represented by conversion of the actual time from the decimal to hexadecimal number.
20DH	A15:A8	FFH	**Reserved**. Bits default to all 1's.
20EH	A23:A16	0AH	**Typical Time-out for Page Program**: 1.0 ms (xxH*(0.1 ms)
20FH	A31:A24	12H	**Typical Time-out for Sector Erase/Block Erase**: 18 ms Typical time-out for Sector/Block-Erase is in ms. Represented by conversion of the actual time from the decimal to hexadecimal number.
210H	A7:A0	23H	**Typical Time-out for Chip Erase**: 35 ms Typical time-out for Chip Erase is in ms. Represented by conversion of the actual time from the decimal to hexadecimal number.
211H	A15:A8	46H	**Maximum Time-out for Byte Program**: 70 µs Typical time-out for Byte Program is in µs. Represented by conversion of the actual time from the decimal to hexadecimal number.
212H	A23:A16	FFH	**Reserved**. Bits default to all 1's.
213H	A31:A24	0FH	**Maximum Time-out for Page Program**: 1.5 ms Typical time-out for Page Program in xxH*(0.1 ms) ms
214H	A7:A0	19H	**Maximum Time-out for Sector Erase/Block Erase**: 25 ms Maximum time-out for Sector/Block Erase in ms
215H	A15:A8	32H	**Maximum Time-out for Chip Erase**: 50 ms. Maximum time-out for Chip Erase in ms.
216H	A23:A16	0FH	**Maximum Time-out for Program Security ID**: 1.5 ms Maximum time-out for Program Security ID in xxH*(0.1 ms) ms
217H	A31:A24	19H	**Maximum Time-out for Write Protection Enable Latency**: 25 ms Maximum time-out for Write Protection Enable Latency is in ms. Represented by conversion of the actual time from the decimal to hexadecimal number.
218H	A7:A0	19H	**Maximum Time-out for Write Suspend Latency**: 25 µs Maximum time-out for Write Suspend Latency is in µs. Represented by conversion of the actual time from the decimal to hexadecimal number.

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TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 12 OF 13)

Address	Bit Address	Data	Comments
219H	A15:A8	03H	**Maximum Time to Deep Power-Down** 3 µs = 03H
21AH	A23:A16	0AH	**Maximum Time-out from Deep Power-Down mode to Standby mode** 10 µs = 0AH
21BH	A31:A24	FFH	**Reserved**. Bits default to all 1's.
21CH	A7:A0	FFH	**Reserved**. Bits default to all 1's.
21DH	A15:A8	FFH	**Reserved**. Bits default to all 1's.
21EH	A23:A16	FFH	**Reserved**. Bits default to all 1's.
21FH	A31:A24	FFH	**Reserved**. Bits default to all 1's.
Supported Instructions			
220H	A7:A0	00H	**No Operation**
221H	A15:A8	66H	**Reset Enable**
222H	A23:A16	99H	**Reset Memory**
223H	A31:A24	38H	**Enable Quad I/O**
224H	A7:A0	FFH	**Reset Quad I/O**
225H	A15:A8	05H	**Read STATUS Register**
226H	A23:A16	01H	**Write STATUS Register**
227H	A31:A24	35H	**Read Configuration Register**
228H	A7:A0	06H	**Write Enable**
229H	A15:A8	04H	**Write Disable**
22AH	A23:A16	02H	**Byte Program or Page Program**
22BH	A31:A24	32H	**SPI Quad Page Program**
22CH	A7:A0	B0H	**Suspends Program/Erase**
22DH	A15:A8	30H	**Resumes Program/Erase**
22EH	A23:A16	FFH	**Reserved**
22FH	A31:A24	FFH	**Reserved**
230H	A7:A0	FFH	**Reserved**
231H	A15:A8	FFH	**Reserved**
232H	A23:A16	FFH	**Reserved**
233H	A31:A24	88H	**Read Security ID**
234H	A7:A0	A5H	**Program User Security ID Area**
235H	A15:A8	85H	**Lockout Security ID Programming**
236H	A23:A16	C0H	**Set Burst Length**
237H	A31:A24	9FH	**JEDEC-ID**
238H	A7:A0	AFH	**Quad J-ID**
239H	A15:A8	5AH	**SFDP**
23AH	A23:A16	B9H	**Deep Power-Down Mode**
23BH	A31:A24	ABH	**Release Deep Power-Down Mode**
23CH	A4:A0	06H	**(1-4-4) SPI nB Burst with Wrap Number of Wait states (dummy clocks) needed before valid output** 00110b: 6 clocks of dummy cycle
	A7:A5		**(1-4-4) SPI nB Burst with Wrap Number of Mode Bits** 000b: Set Mode bits are not supported
23DH	A15:A8	ECH	**(1-4-4) SPI nB Burst with Wrap Opcode**

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TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 13 OF 13)

Address	Bit Address	Data	Comments
23EH	A20:A16	06H	**(4-4-4) SQI nB Burst with Wrap Number of Wait states (dummy clocks) needed before valid output** 00110b: 6 clocks of dummy cycle
	A23:A21		000b: Set Mode bits are not supported
23FH	A31:A24	0CH	**(4-4-4) SQI nB Burst with Wrap Opcode**
240H	A4:A0	00H	**(1-1-1) Read Memory Number of Wait states (dummy clocks) needed before valid output** 00000b: Wait states/dummy clocks are not supported
	A7:A5		**(1-1-1) Read Memory Number of Mode Bits** 000b: Mode bits are not supported
241H	A15:A8	03H	**(1-1-1) Read Memory Opcode**
242H	A20:A16	08H	**(1-1-1) Read Memory at Higher Speed Number of Wait states (dummy clocks) needed before valid output** 01000: 8 clocks (8 bits) of dummy cycle
	A23:A21		**(1-1-1) Read Memory at Higher Speed Number of Mode Bits** 000b: Mode bits are not supported
243H	A31:A24	0BH	**(1-1-1) Read Memory at Higher Speed Opcode**
244H	A7:A0	FFH	**Reserved**. Bits default to all 1's.
245H	A15:A8	FFH	**Reserved**. Bits default to all 1's.
246H	A23:A16	FFH	**Reserved**. Bits default to all 1's.
247H	A31:A24	FFH	**Reserved**. Bits default to all 1's.
248H	A7:A0	FFH	**Security ID size in bytes** Example: If the size is 2 Kbytes, this field would be 07FFH **Security ID Range** Unique ID (preprogrammed at factory): 0000H-000FH User-programmable: 0010H-07FFH
249H	A15:A8	07H	
24AH	A23:A16	FFH	**Reserved**. Bits default to all 1's.
24BH	A31:A24	FFH	**Reserved**. Bits default to all 1's.

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