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SST25VF080B

8-Mbit SPI Serial Flash

Features

- Single-Voltage Read and Write Operations:
  - 2.7V to 3.6V
- Serial Interface Architecture:
  - SPI-Compatible: Mode 0 and Mode 3
- High-Speed Clock Frequency:
  - Up to 66 MHz
- Superior Reliability:
  - Endurance: 100,000 cycles (typical)
  - Greater than 100 years data retention
- Low-Power Consumption:
  - Active Read current: 10 mA (typical)
  - Standby current: 5 µA (typical)
- Flexible Erase Capability:
  - Uniform 4 KB sectors
  - Uniform 32 KB overlay blocks
  - Uniform 64 KB overlay blocks
- Fast Erase and Byte Program:
  - Chip Erase time: 35 ms (typical)
  - Sector/Block Erase time: 18 ms (typical)
  - Byte Program time: 7 µs (typical)
- Auto Address Increment (AAI) Programming:
  - Decrease total chip programming time over byte-program operations
- End-of-Write Detection:
  - Software polling of the BUSY bit in the STATUS register
  - Busy status readout on the SO pin in AAI mode
- Hold Pin (HOLD#):
  - Suspends a serial sequence to the memory without deselecting the device
- Write Protection (WP#):
  - Enables/Disables the lockdown function of the STATUS register
- Software Write Protection:
  - Write protection through Block Protection bits in the STATUS register
- Temperature Range:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
- All Devices are RoHS compliant

Packages

- 8-Lead PDIP (300 mils), 8-Lead SOIC (200 mils), 8-Lead USON (2 mm x 3 mm) and 8-Contact WSON (6 mm x 5 mm)

Product Description

The 25 Series serial Flash family features a four-wire, SPI-compatible interface that enables low pin-count packages, reduces board space and lowers total system costs. The SST25VF080B devices are enhanced with improved operating frequency and lower power consumption. SST25VF080B SPI serial Flash memories are manufactured with proprietary high-performance CMOS SuperFlash® technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches.

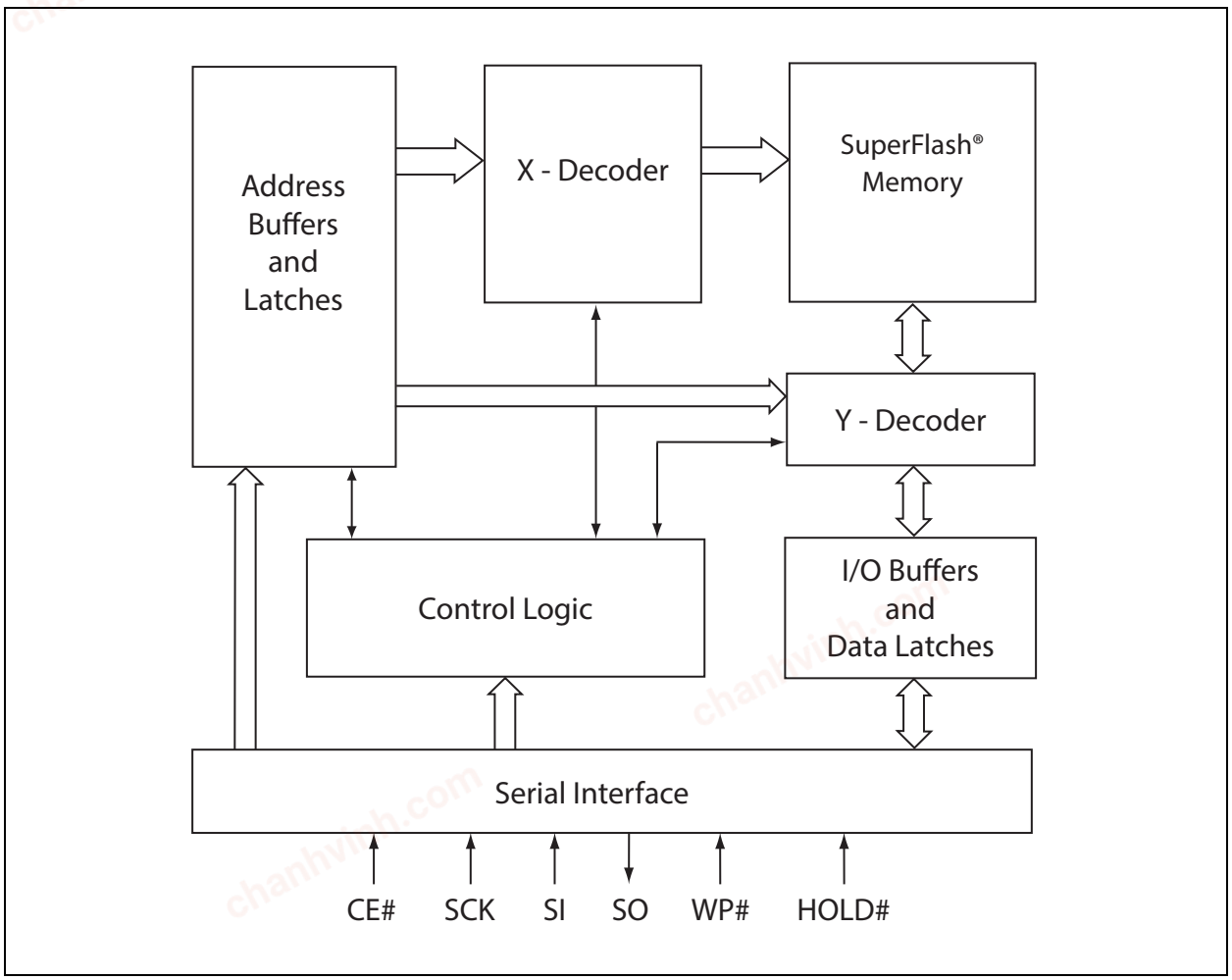
The SST25VF080B devices significantly improve performance and reliability while reducing power consumption. The devices write (program or erase) using a single 2.7V to 3.6V power supply. Total energy consumption depends on the applied voltage, current and application time. Because SuperFlash technology uses less programming current and shorter erase times, total energy consumption during erase and program operations is lower than that of alternative Flash memory technologies. See Figure 2-1 for pin assignments.

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1.0 BLOCK DIAGRAM

FIGURE 1-1: FUNCTIONAL BLOCK DIAGRAM



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2.0 PIN DESCRIPTION

FIGURE 2-1: PIN ASSIGNMENTS

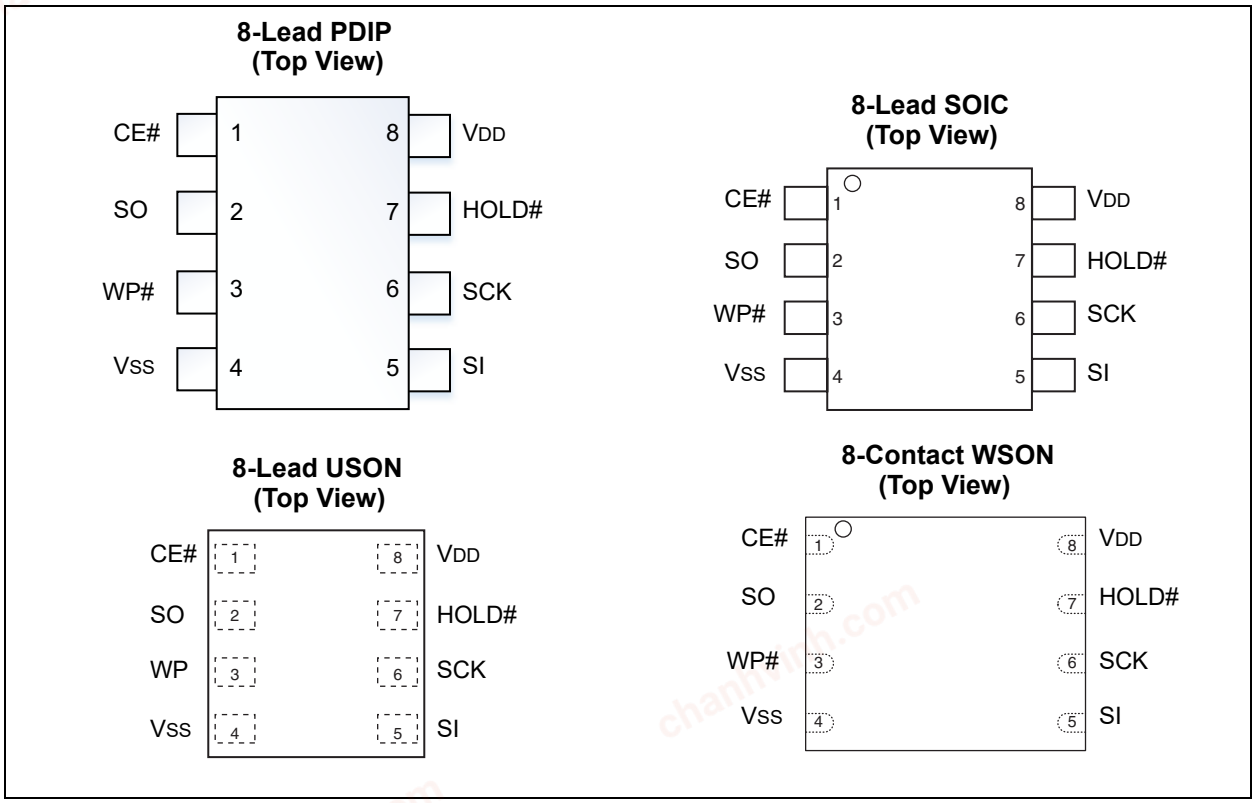


TABLE 2-1: PIN DESCRIPTION

Symbol	Pin Name	Functions
CE#	Chip Enable	The device is enabled by a high-to-low transition on the CE# pin. CE# must remain low for the duration of any command sequence.
SO	Serial Data Output	Transfers data serially out of the device. Data are shifted out on the falling edge of the serial clock. Outputs Flash busy status during AAI programming when reconfigured as the RY/BY# pin. See **Section 4.4.6 "Hardware End-of-Write Detection"** for details.
WP#	Write Protect	The Write Protect (WP#) pin is used to enable or disable BPL bit in the STATUS register.
V_{SS}	Ground	
SI	Serial Data Input	Transfers commands, addresses, or data serially into the device. Inputs are latched on the rising edge of the serial clock.
SCK	Serial Clock	Provides the timing of the serial interface. Commands, addresses and input data are latched on the rising edge of the clock input, while output data are shifted out on the falling edge of the clock input.
HOLD#	Hold	Temporarily suspends serial communication with SPI Flash memory without resetting the device.
V_{DD}	Power Supply	Provides the power supply voltage.

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3.0 MEMORY ORGANIZATION

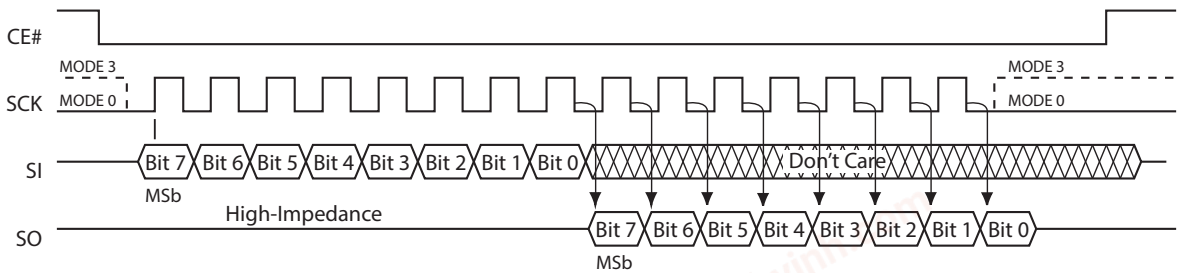
The SST25VF080B SuperFlash memory array is organized in uniform 4 KB erasable sectors with 32 KB overlay blocks and 64 KB overlay erasable blocks.

4.0 DEVICE OPERATION

The SST25VF080B is accessed through the SPI (Serial Peripheral Interface) bus compatible protocol. The SPI bus consists of four control lines: Chip Enable (CE#), which is used to select the device, and Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK), which are used for data access.

The SST25VF080B supports both SPI Mode 0 (0,0) and Mode 3 (1,1) operations. As shown in Figure 4-1, the difference between the two modes is the state of the SCK signal when the host is in Standby mode and no data are being transferred. The SCK signal is low for Mode 0 and high for Mode 3. For both modes, Serial Data Input (SI) is sampled on the rising edge of SCK, and Serial Data Output (SO) is driven on the falling edge of SCK.

FIGURE 4-1: SPI PROTOCOL



Note: MSb = Most Significant bit

4.1 Hold Operation

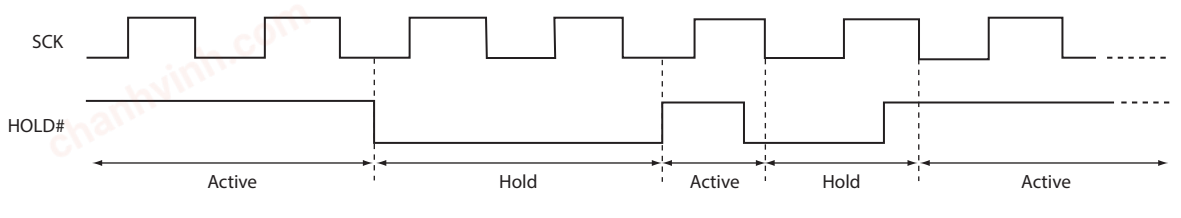
The HOLD# pin is used to pause a serial sequence in progress with the SPI Flash memory without resetting the clock sequence. To activate HOLD# mode, CE# must be in the active-low state. HOLD# mode begins when the falling edge of the HOLD# signal coincides with the active-low state of SCK. HOLD# mode ends when the rising edge of the HOLD# signal coincides with the active-low state of SCK.

If the falling edge of the HOLD# signal does not coincide with the active-low state of SCK, the device enters HOLD# mode when SCK next reaches the active-low state. Similarly, if the rising edge of the HOLD# signal does not coincide with the low state of SCK, the device exits HOLD# mode when SCK next reaches the active-low state. See Figure 4-2 for the hold-condition waveform.

Once the device enters HOLD# mode, SO enters the high-impedance state while SI and SCK can be V_{IL} or V_{IH}.

If CE# is driven active-high during a Hold condition, the internal logic of the device is reset. As long as the HOLD# signal remains low, the memory remains in the hold condition. To resume communication with the device, HOLD# must be driven active-high and CE# must be driven active-low. See Figure 5-6 for hold timing.

FIGURE 4-2: HOLD CONDITION WAVEFORM



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4.2 Write Protection

The SST25VF080B provides software write protection. The Write Protect pin (WP#) enables or disables the lockdown function of the STATUS register. The Block Protection bits (BP3, BP2, BP1, BP0 and BPL) in the STATUS register provide write protection to the memory array and the STATUS register. See Table 4-3 for the block protection description.

4.2.1 WRITE PROTECT PIN (WP#)

The Write Protect (WP#) pin enables the lockdown function of the BPL bit (bit 7) in the STATUS register. When WP# is driven low, execution of the Write Status Register (WRSR) instruction is determined by the value of the BPL bit (see Table 4-1). When WP# is driven high, the lockdown function of the BPL bit is disabled.

TABLE 4-1: CONDITIONS TO EXECUTE WRITE STATUS REGISTER (WRSR) INSTRUCTION

WP#	BPL	Execute WRSR Instruction
L	1	Not Allowed
L	0	Allowed
H	X	Allowed

4.3 STATUS Register

The software STATUS register indicates whether the Flash memory array is available for read or write operations, whether the device is write-enabled, and the current memory write-protection state. During an internal erase or program operation, the STATUS register may only be read to determine whether the operation has completed. Table 4-2 describes the function of each bit in the software STATUS register.

TABLE 4-2: SOFTWARE STATUS REGISTER

Bit	Name	Function	Default at Power-up	Read/Write
0	BUSY	1 = Internal write operation in progress 0 = No internal write operation in progress	0	R
1	WEL	1 = Device is memory write-enabled 0 = Device is not memory write-enabled	0	R
2	BP0	Indicates the current level of block write protection (see Table 4-3)	1	R/W
3	BP1	Indicates the current level of block write protection (see Table 4-3)	1	R/W
4	BP2	Indicates the current level of block write protection (see Table 4-3)	1	R/W
5	BP3	Indicates the current level of block write protection (see Table 4-3)	0	R/W
6	AAI	Auto Address Increment programming status 1 = AAI programming mode 0 = Byte-Program mode	0	R
7	BPL	1 = BP3, BP2, BP1 and BP0 are read-only 0 = BP3, BP2, BP1 and BP0 are read/write	0	R/W

4.3.1 BUSY

The BUSY bit indicates whether an internal erase or program operation is in progress. A value of '1' indicates that the device is busy performing an operation, while a value of '0' indicates that the device is ready for the next valid operation.

4.3.2 WRITE ENABLE LATCH (WEL)

The Write Enable Latch bit indicates the status of the internal memory write-enable latch. If the Write Enable Latch bit is set to '1', the device is write-enabled. If the bit is set to '0' (reset), the device is not write-enabled and does not accept write (program or erase) commands. The Write Enable Latch bit is automatically reset under the following conditions:

- Power-up
- Write Disable (WRDI) instruction completion
- Byte Program instruction completion
- Completion of Auto Address Increment (AAI) programming
- Sector Erase instruction completion
- Block Erase instruction completion
- Chip Erase instruction completion
- Write Status Register instruction completion

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4.3.3 AUTO ADDRESS INCREMENT (AAI)

The Auto Address Increment status bit indicates whether the device is in AAI programming mode or Byte-Program mode. The default at power-up is Byte Program mode.

4.3.4 BLOCK PROTECTION (BP3, BP2, BP1, BP0)

The Block Protection (BP3, BP2, BP1 and BP0) bits define the size of the memory area (see Table 4-3) that is software-protected against write operations (program or erase). The Write Status Register (WRSR) instruction is used to program the BP3, BP2, BP1 and BP0 bits, provided that the WP# is high or the Block Protect Lock (BPL) bit is set to '0'. The Chip Erase operation can be executed only when Block Protection bits are set to '0'. After power-up, BP3, BP2, BP1 and BP0 are set to '1'.

4.3.5 BLOCK PROTECTION LOCKDOWN (BPL)

When the WP# pin is driven low (V_{IL}), the Block Protection Lockdown (BPL) bit is enabled. When BPL is set to '1', further modification of the BPL, BP3, BP2, BP1 and BP0 bits is prevented. When the WP# pin is driven high (V_{IH}), the BPL bit has no effect, and its value is "don't care". After power-up, the BPL bit is reset to '0'.

TABLE 4-3: SOFTWARE STATUS REGISTER BLOCK PROTECTION FOR SST25VF080B

Protection Level	STATUS Register Bit				Protected Memory Address
	BP3	BP2(2)	BP1(2)	BP0(2)	8 Mbits
None	X(1)	0	0	0	None
Upper 1/16	X(1)	0	0	1	F0000H-FFFFFH
Upper 1/8	X(1)	0	1	0	E0000H-FFFFFH
Upper 1/4	X(1)	0	1	1	C0000H-FFFFFH
Upper 1/2	X(1)	1	0	0	80000H-FFFFFH
All blocks	X(1)	1	0	1	00000H-FFFFFH
All blocks	X(1)	1	1	0	00000H-FFFFFH
All blocks	X(1)	1	1	1	00000H-FFFFFH

Note 1: X indicates a "Don't Care" (reserved) value, with a default setting of '0'.

2: Default at power-up for BP2, BP1 and BP0 are '111' (all blocks protected).

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4.4 Instructions

Instructions are used to read, write (erase and program), and configure the SST25VF080B. Instruction bus cycles are 8 bits each for commands (opcode), data and addresses. Prior to executing any Byte Program, Auto Address Increment (AAI) programming, Sector Erase, Block Erase, Write Status Register, or Chip Erase instruction, the Write Enable (WREN) instruction must be executed first. The complete list of instructions is provided in Table 4-4. All instructions are synchronized with the high-to-low transition of CE#. Inputs are accepted on the rising edge of SCK, beginning with the Most Significant bit (MSb). CE# must be driven low before an instruction is entered and driven high after the last bit of the instruction has been shifted in (except for Read, Read ID and Read Status Register instructions). Any low-to-high transition on CE# before the last bit of an instruction bus cycle is received terminates the instruction in progress and returns the device to Standby mode. Instruction commands (opcode), addresses and data are input beginning with the Most Significant bit (MSb) first.

TABLE 4-4: DEVICE OPERATION INSTRUCTIONS

Instruction	Description	Opcode Cycle(1)	Address Cycle(s)(2)	Dummy Cycle(s)	Data Cycle(s)
Read	Read memory	0000 0011b (03H)	3	0	1 to ∞
High-Speed Read	Read Memory at higher speed	0000 1011b (0BH)	3	1	1 to ∞
4 KB Sector Erase(3)	Erase 4 KB of the memory array	0010 0000b (20H)	3	0	0
32 KB Block Erase(4)	Erase 32 KB block of memory array	0101 0010b (52H)	3	0	0
64 KB Block Erase(5)	Erase 64 KB block of memory array	1101 1000b (D8H)	3	0	0
Chip Erase	Erase full memory array	0110 0000b (60H) or 1100 0111b (C7H)	0	0	0
Byte Program	Program one data byte	0000 0010b (02H)	3	0	1
AAI Word Program(6)	Auto Address Increment programming	1010 1101b (ADH)	3	0	2 to ∞
RDSR(7)	Read Status Register	0000 0101b (05H)	0	0	1 to ∞
EWSR	Enable Write Status Register	0101b 0000b (50H)	0	0	0
WRSR	Write Status Register	0000 0001b (01H)	0	0	1
WREN	Write Enable	0000 0110b (06H)	0	0	0
WRDI	Write Disable	0000 0100b (04H)	0	0	0
RDID(8)	Read ID	1001 0000b (90H) or 1010 1011b (ABH)	3	0	1 to ∞
JEDEC ID	JEDEC ID read	1001 1111b (9FH)	0	0	3 to ∞

Note 1: One bus cycle is eight clock periods.

2: Address bits above the Most Significant bit of each density can be V_{IL} or V_{IH}.

3: 4 KB Sector Erase addresses: use A_{MS}-A_{12}. Remaining addresses are “don’t care” but must be set to either at V_{IL} or V_{IH}.

4: 32 KB Block Erase addresses: use A_{MS}-A_{15}. Remaining addresses are “don’t care” but must be set to either V_{IL} or V_{IH}.

5: 64 KB Block Erase addresses: use A_{MS}-A_{16}. Remaining addresses are “don’t care” but must be set to either V_{IL} or V_{IH}.

6: To continue programming at the next sequential address location, enter the 8-bit command, ADH, followed by 2 bytes of data. Data Byte 0 is programmed into the initial address [A_{23}-A_1] with A_0 = 0. Data Byte 1 is programmed into the initial address [A_{23}-A_1] with A_0 = 1.

7: The Read Status Register operation continues during clock cycles until terminated by a low-to-high transition on CE#.

8: The Manufacturer ID is read with A_0 = 0, and the Device ID is read with A_0 = 1. All other address bits are set to 00H. The Manufacturer ID and Device ID output stream continues until terminated by a low-to-high transition on CE#.

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TABLE 4-4: DEVICE OPERATION INSTRUCTIONS

Instruction	Description	Opcode Cycle(1)	Address Cycle(s)(2)	Dummy Cycle(s)	Data Cycle(s)
EBSY	Enable SO to output RY/BY# status during AAI programming	0111 0000b (70H)	0	0	0
DBSY	Disable SO as RY/BY# status during AAI programming	1000 0000b (80H)	0	0	0

Note 1: One bus cycle is eight clock periods.

2: Address bits above the Most Significant bit of each density can be V_{IL} or V_{IH}.

3: 4 KB Sector Erase addresses: use A_{MS}-A_{12}. Remaining addresses are “don’t care” but must be set to either at V_{IL} or V_{IH}.

4: 32 KB Block Erase addresses: use A_{MS}-A_{15}. Remaining addresses are “don’t care” but must be set to either V_{IL} or V_{IH}.

5: 64 KB Block Erase addresses: use A_{MS}-A_{16}. Remaining addresses are “don’t care” but must be set to either V_{IL} or V_{IH}.

6: To continue programming at the next sequential address location, enter the 8-bit command, ADH, followed by 2 bytes of data. Data Byte 0 is programmed into the initial address [A_{23}-A_1] with A_0 = 0. Data Byte 1 is programmed into the initial address [A_{23}-A_1] with A_0 = 1.

7: The Read Status Register operation continues during clock cycles until terminated by a low-to-high transition on CE#.

8: The Manufacturer ID is read with A_0 = 0, and the Device ID is read with A_0 = 1. All other address bits are set to 00H. The Manufacturer ID and Device ID output stream continues until terminated by a low-to-high transition on CE#.

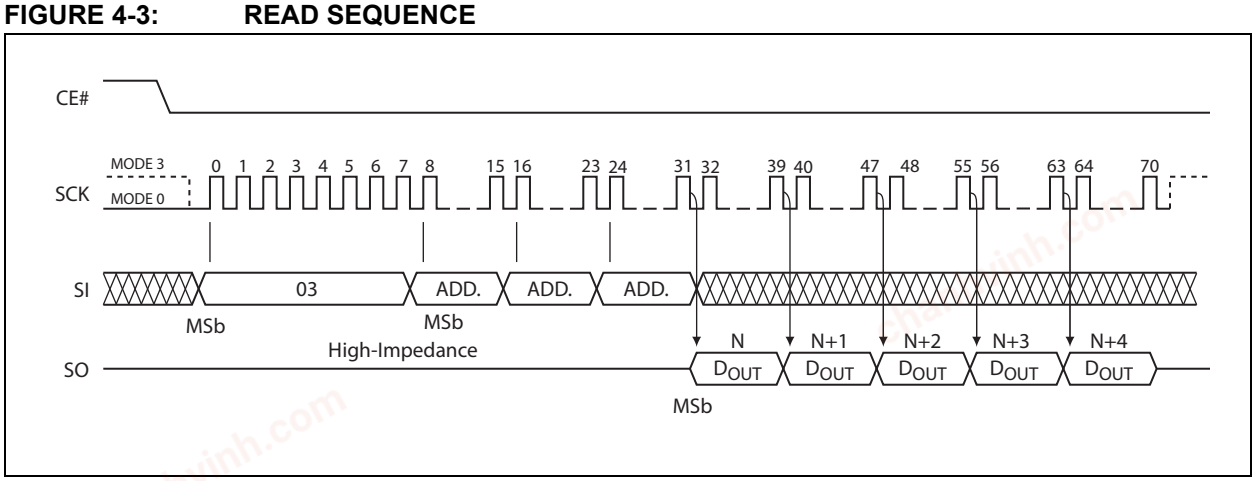
4.4.1 READ (25 MHz)

The Read instruction (03H) supports read operations at frequencies up to 25 MHz. The device outputs data beginning at the specified address location. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer automatically increments until the highest memory address is reached.

Once the highest memory address is reached, the Address Pointer automatically increments to the beginning of the address space (wrap-around). After data from address location FFFFFH are read, the next output is from address location 00000H.

The Read instruction is initiated by executing an 8-bit command (03H) followed by address bits [A_{23}-A_0]. CE# must remain active-low for the duration of the Read cycle. See Figure 4-3 for the Read sequence.

FIGURE 4-3: READ SEQUENCE



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4.4.2 HIGH-SPEED READ (66 MHz)[1]

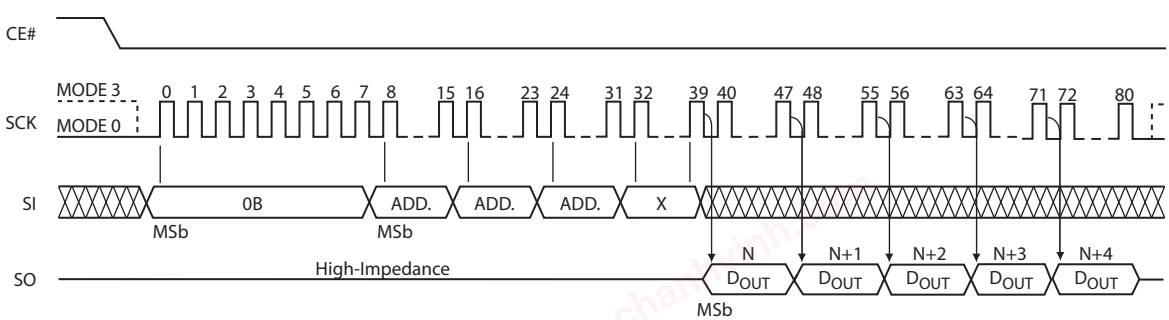
The High-Speed Read instruction supports read operations up to 66 MHz. The instruction is initiated by executing an 8-bit command (0BH) followed by address bits [A23-A0] and a dummy byte. CE# must remain active-low for the duration of the High-Speed Read cycle. See Figure 4-4 for the High-Speed Read sequence.

Following a dummy cycle, the High-Speed Read instruction outputs the data beginning from the specified address location. The data output stream continues through all addresses until terminated by a low-to-high transition on CE#.

The internal Address Pointer automatically increments until the highest memory address is reached. Once the highest memory address is reached, the Address Pointer automatically increments to the beginning of the address space (wrap-around). After data from address location FFFFFH are read, the next output is from address location 00000H.

Note 1: 66 MHz operation occurs under the conditions specified in Table 5-7.

FIGURE 4-4: HIGH-SPEED READ SEQUENCE



Note: X = Dummy Byte: 8-clock input dummy cycle (VIL or VIH)

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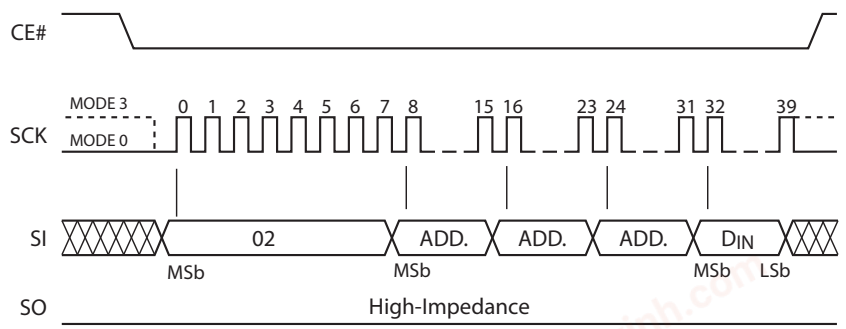
4.4.3 BYTE PROGRAM

The Byte Program instruction programs the selected byte with the desired data. The selected byte must be in the erased state (FFH) before a program operation is initiated. The device ignores Byte Program instructions applied to protected memory area.

Before any write operation, the Write Enable (WREN) instruction must be executed. CE# must remain active-low for the duration of the Byte Program instruction.

The Byte Program instruction is initiated by executing an 8-bit command (02H) followed by address bits [A_{23}-A_0]. Following the address, data are input sequentially from MSb (bit 7) to LSb (bit 0). CE# must be driven high before the instruction is executed. The user may poll the BUSY bit in the software STATUS register or wait T_{BP} for completion of the internal self-timed Byte Program operation. See Figure 4-5 for the Byte Program sequence.

FIGURE 4-5: BYTE PROGRAM SEQUENCE



4.4.4 AUTO ADDRESS INCREMENT (AAI) WORD PROGRAM

The AAI program instruction allows multiple bytes of data to be programmed without reissuing the next sequential addresses. This feature decreases total programming time when multiple bytes or the entire memory array are programmed. The device ignores AAI Word Program instructions targeting protected memory areas. The selected address range must be in the erased state (FFH) before an AAI Word Program operation is initiated. During the AAI Word Programming sequence, only the following instructions are valid: for software end-of-write detection—AAI Word (ADH), WRDI (04H) and RDSR (05H); for hardware end-of-write detection—AAI Word (ADH) and WRDI (04H). There are three options to determine the completion of each AAI Word program cycle: hardware detection by reading the Serial Output, software detection by polling the BUSY bit in the software STATUS register, or waiting for T_{BP}. Refer to **Section 4.4.5 "End-of-Write Detection"** for details.

Prior to any write operation, the Write Enable (WREN) instruction must be executed. The AAI Word Program instruction is initiated by executing an 8-bit command (ADH), followed by address bits [A_{23}-A_0]. Following the addresses, two bytes of data are input sequentially, beginning with MSb (bit 7) and ending with LSb (bit 0). The first byte of data (D0) is programmed into the initial address [A_{23}-A_1] with A_0 = 0. The second byte of data (D1) is programmed into the initial address [A_{23}-A_1] with A_0 = 1. CE# must be driven high before the AAI Word Program instruction is executed. Check the BUSY bit before issuing the next valid command. Once the device is no longer busy, data for the next two sequential addresses may be programmed, followed by subsequent pairs of sequential addresses as needed.

When programming the last desired word or the highest unprotected memory address, determine program completion using either the hardware or software detection method (RDSR instruction). Once programming is complete, use the appropriate method to terminate AAI programming. If the device is operating in software End-of-Write detection mode, execute the Write Disable (WRDI) instruction, 04H. If the device is operating in AAI Hardware End-of-Write detection mode, execute the Write Disable (WRDI) instruction (04H), followed by the 8-bit DBSY command (80H). During AAI programming, wrap mode is not supported after the highest unprotected memory address is reached. See Figure 4-8 and Figure 4-9 for the AAI Word programming sequence.

4.4.5 END-OF-WRITE DETECTION

There are three methods to determine the completion of a program cycle during AAI Word programming: hardware detection by reading the Serial Output, software detection by polling the BUSY bit in the Software STATUS Register, or waiting for T_{BP}. The Hardware End-of-Write detection method is described in the section below.

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4.4.6 HARDWARE END-OF-WRITE DETECTION

The hardware End-of-Write detection method eliminates the overhead associated with polling the BUSY bit in the software STATUS register during an AAI Word Program operation. The 8-bit command (70H) configures the Serial Output (SO) pin to indicate Flash busy status during AAI Word programming (see Figure 4-6). The 70H command must be executed prior to initiating an AAI Word Program instruction. Once an internal programming operation begins, asserting CE# immediately outputs the internal Flash busy status on the SO pin.

A '0' indicates that the device is busy, and a '1' indicates that the device is ready for the next instruction. Deasserting CE# returns the SO pin to tri-state. While operating in AAI and hardware End-of-Write detection mode, the only valid instructions are AAI Word (ADH) and WRDI (04H).

To exit AAI hardware End-of-Write detection mode, first execute the WRDI instruction (04H) to reset the Write Enable Latch bit (WEL = 0) and the AAI bit. Then execute the 8-bit DBSY command (80H) to disable RY/BY# status output during AAI programming (see Figure 4-7).

FIGURE 4-6: ENABLE SO AS HARDWARE RY/BY# DURING AAI PROGRAMMING

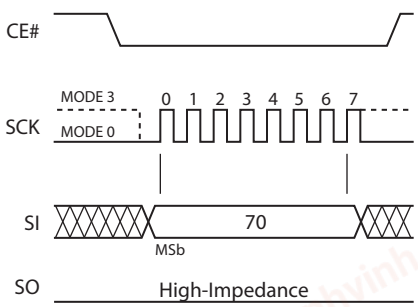
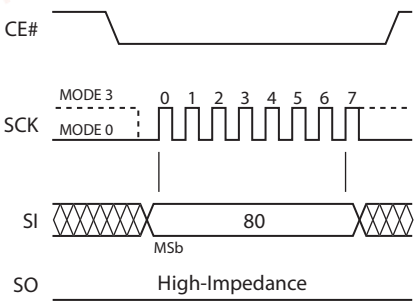


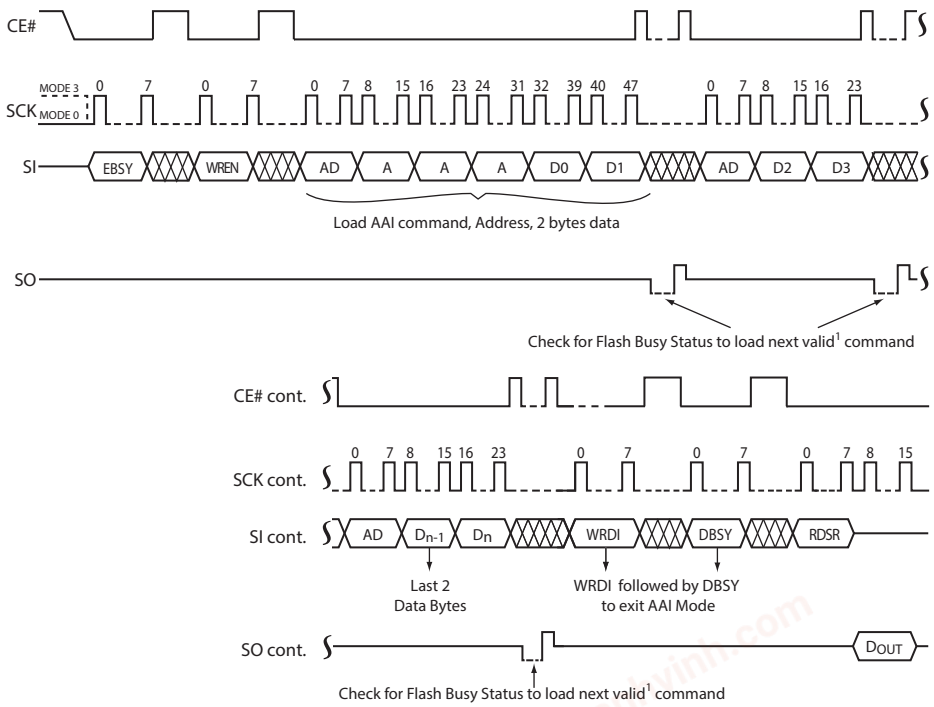
FIGURE 4-7: DISABLE SO AS HARDWARE RY/BY# DURING AAI PROGRAMMING



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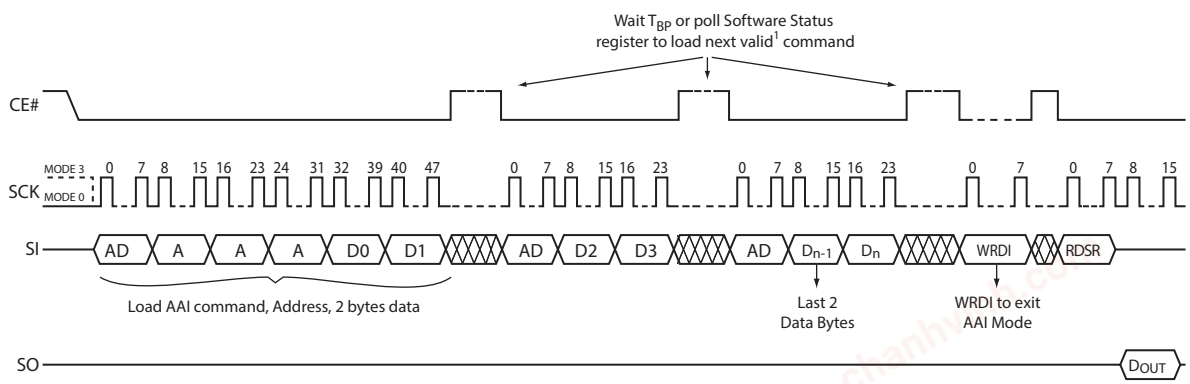
FIGURE 4-8: AUTO ADDRESS INCREMENT (AAI) WORD PROGRAM SEQUENCE WITH HARDWARE END-OF-WRITE DETECTION



Note 1: Valid commands during AAI programming: AAI command or WRDI command.

2: User must configure the SO pin to output Flash busy status during AAI programming.

FIGURE 4-9: AUTO ADDRESS INCREMENT (AAI) WORD PROGRAM SEQUENCE WITH SOFTWARE END-OF-WRITE DETECTION



Note 1: Valid commands during AAI programming: RDSR command or WRDI command.

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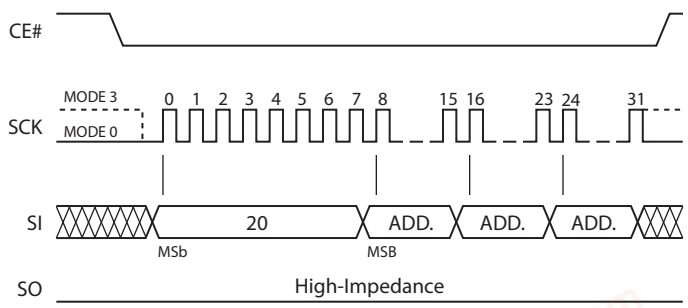
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4.4.7 4 KB SECTOR ERASE

The Sector Erase instruction clears all bits in the selected 4 KB sector to FFH. The device ignores Sector Erase instructions applied to protected memory areas. Prior to any write operation, the Write Enable (WREN) instruction must be executed. CE# must remain active-low for the duration of the command sequence. The Sector Erase instruction is initiated by executing the 8-bit command (20H) followed by address bits [A_{23}-A_0].

Address bits [A_{MS}-A_{12}] (A_{MS} = Most Significant address) are used to determine the sector address (SA_X). Remaining address bits can be either V_{IL} or V_{IH}. CE# must be driven high before the instruction is executed. The user may poll the BUSY bit in the software STATUS register or wait T_{SE} for completion of the internal self-timed Sector Erase cycle. See Figure 4-10 for the Sector Erase sequence.

FIGURE 4-10: SECTOR ERASE SEQUENCE



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4.4.8 32 KB AND 64 KB BLOCK ERASE

The 32 KB Block Erase instruction clears all bits in the selected 32 KB block to FFH.The device ignores Block Erase instructions applied to protected memory areas. The 64 KB Block Erase instruction clears all bits in the selected 64 KB block to FFH. The device ignores Block Erase instructions applied to protected memory areas. Prior to any write operation, the Write Enable (WREN) instruction must be executed. CE# must remain active-low for the duration of the command sequence. The 32 KB Block Erase instruction is initiated by executing an 8-bit command (52H) followed by address bits [A_{23}-A_0]. Address bits [A_{MS}-A_{15}] (A_{MS} = Most Significant address) are used to determine the block address (BA_X). Remaining address bits can be either V_{IL} or V_{IH}.

CE# must be driven high before the instruction is executed. The 64 KB Block Erase instruction is initiated by executing the 8-bit command (D8H) followed by address bits [A_{23}-A_0]. Address bits [A_{MS}-A_{16}] are used to determine block address (BA_X). Remaining address bits can be either V_{IL} or V_{IH}. CE# must be driven high before the instruction is executed. The user may poll the BUSY bit in the software STATUS register or wait T_{BE} for completion of the internal self-timed 32 KB Block Erase or 64 KB Block Erase cycle. See Figure 4-11 and Figure 4-12 for the 32 KB Block Erase and 64 KB Block Erase sequences.

FIGURE 4-11: 32 KB BLOCK ERASE SEQUENCE

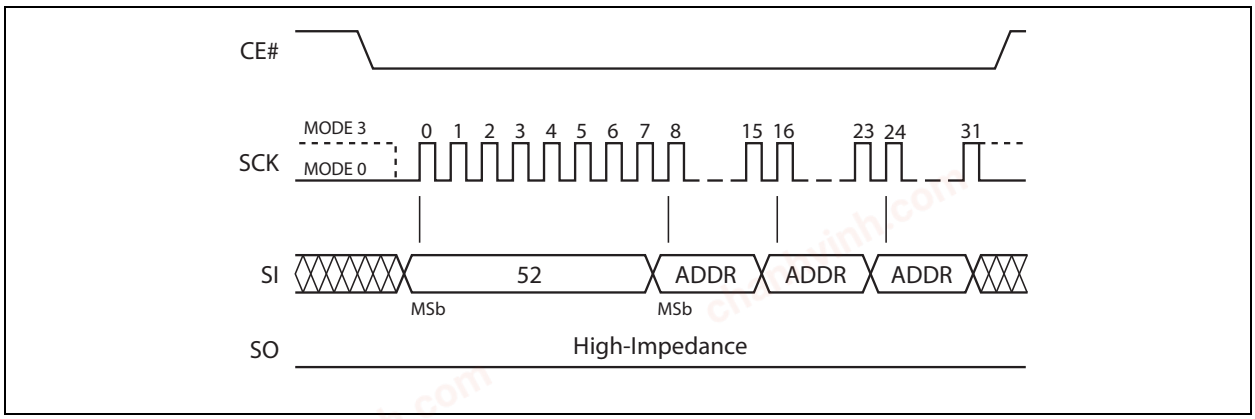
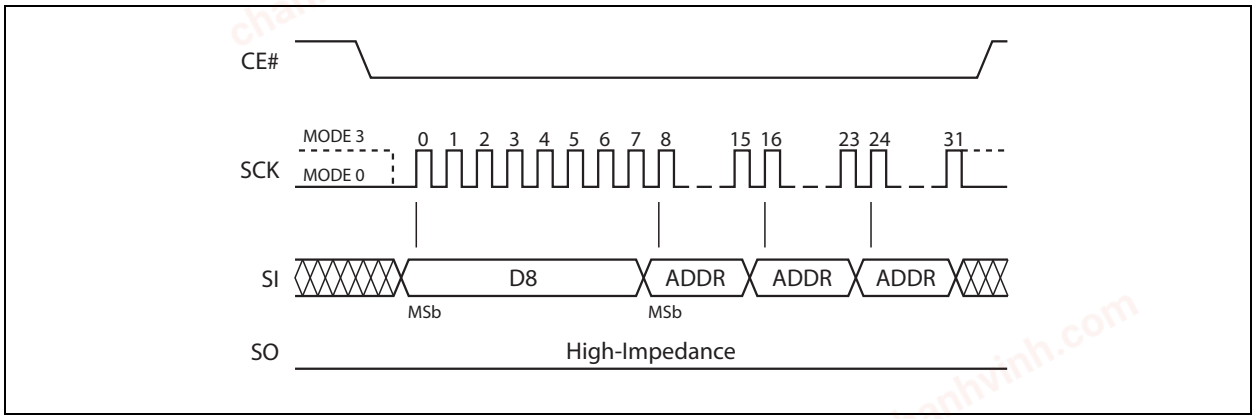


FIGURE 4-12: 64 KB BLOCK ERASE SEQUENCE



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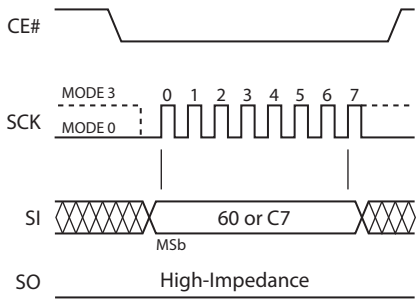
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4.4.9 CHIP ERASE

The Chip Erase instruction clears all bits in the device to FFH. The device ignores the Chip Erase instruction if any memory area is protected. Prior to any write operation, the Write Enable (WREN) instruction must be executed. CE# must remain active-low for the duration of the Chip Erase instruction sequence.

The Chip Erase instruction is initiated by executing the 8-bit command (60H or C7H). CE# must be driven high before the instruction is executed. The user may poll the BUSY bit in the software STATUS register or wait TCE for completion of the internal self-timed Chip Erase cycle. See Figure 4-13 for the Chip Erase sequence.

FIGURE 4-13: CHIP ERASE SEQUENCE

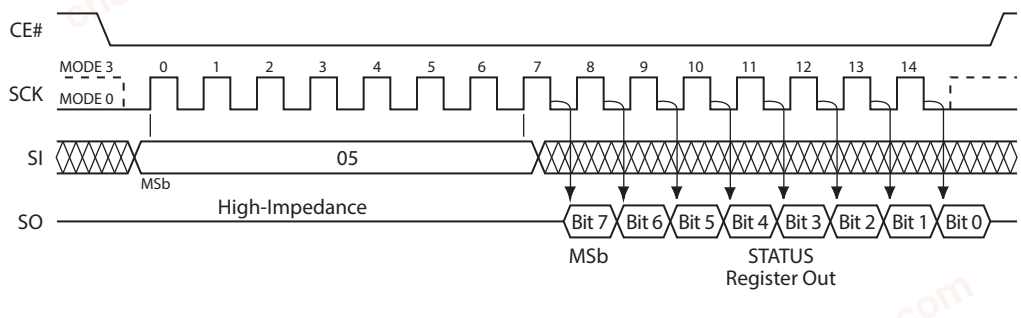


4.4.10 READ STATUS REGISTER (RDSR)

The Read Status Register (RDSR) instruction allows the STATUS register to be read. The STATUS register may be read at any time, including during a write operation (program or erase). When a write operation is in progress, the BUSY bit may be checked before issuing new instructions to ensure that the instructions are properly received by the device.

CE# must be driven low before the RDSR instruction is entered and must remain low until the status data are read. The Read Status Register operation continues during clock cycles until terminated by a low-to-high transition on CE#. See Figure 4-14 for the RDSR instruction sequence.

FIGURE 4-14: READ STATUS REGISTER (RDSR) SEQUENCE



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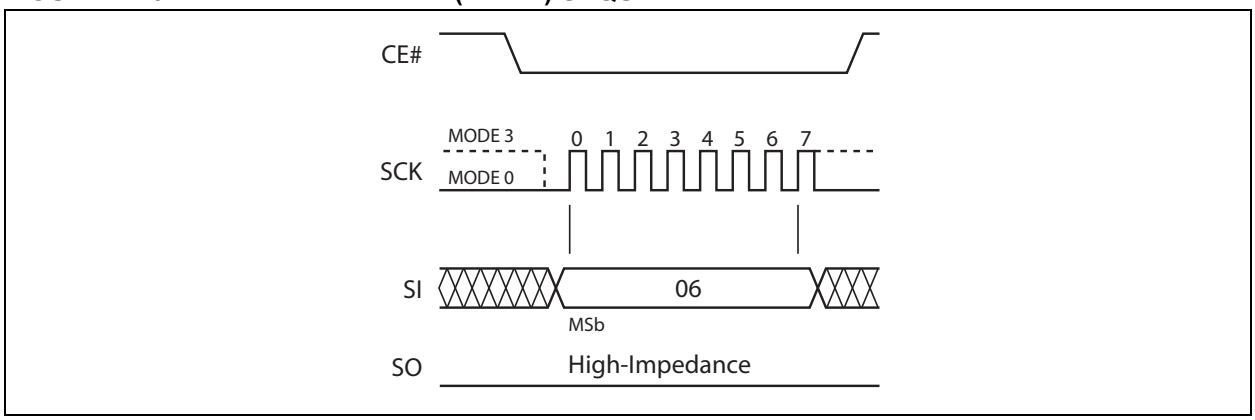
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4.4.11 WRITE ENABLE (WREN)

The Write Enable (WREN) instruction sets the Write Enable Latch bit in the STATUS register to '1', allowing write operations to occur. The WREN instruction must be executed prior to any write operation (program or erase).

The WREN instruction may also be used to allow execution of the Write Status Register (WRSR) instruction. However, the Write Enable Latch bit in the STATUS register is cleared upon the rising edge CE# of the WRSR instruction. CE# must be driven high before the WREN instruction is executed.

FIGURE 4-15: WRITE ENABLE (WREN) SEQUENCE

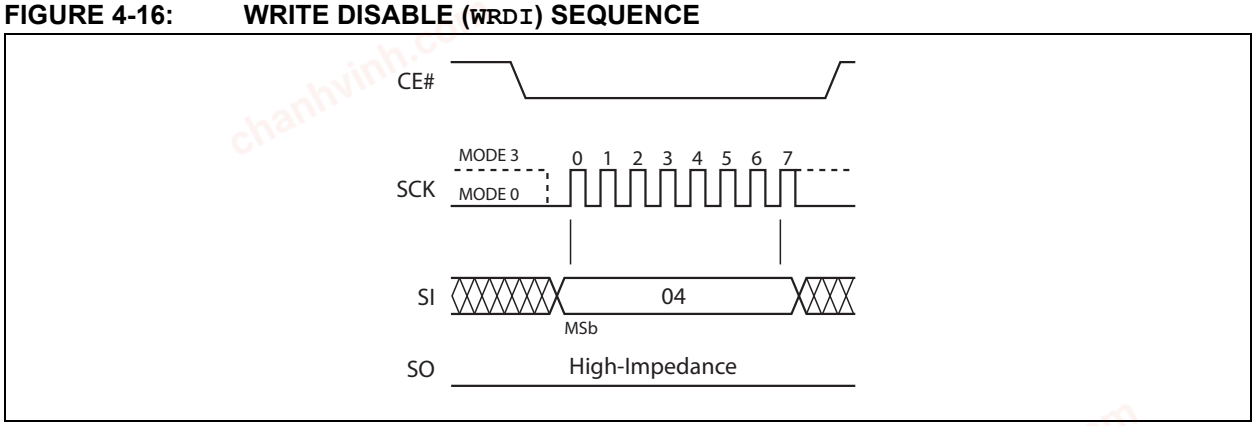


4.4.12 WRITE DISABLE (WRDI)

The Write Disable (WRDI) instruction resets the Write Enable Latch bit and AAI bit to '0', prevending new write operations. The WRDI instruction does not terminate any program operation already in progress.

Any program operation already in progress may continue for up to TBP after executing the WRDI instruction. CE# must be driven high before the WRDI instruction is executed.

FIGURE 4-16: WRITE DISABLE (WRDI) SEQUENCE



4.4.13 ENABLE WRITE STATUS REGISTER (EWSR)

The Enable Write Status Register (EWSR) instruction enables execution of the Write Status Register (WRSR) instruction and allows modification of the STATUS register. The Write Status Register instruction must be executed immediately after the Enable Write Status Register instruction. This two-step instruction sequence, consisting of the EWSR instruction followed by the WRSR instruction, operates like an SDP (software data protection) command structure to prevent accidental modification of STATUS register values.

CE# must be driven low before the EWSR instruction is entered and must be driven high before the EWSR instruction is executed.

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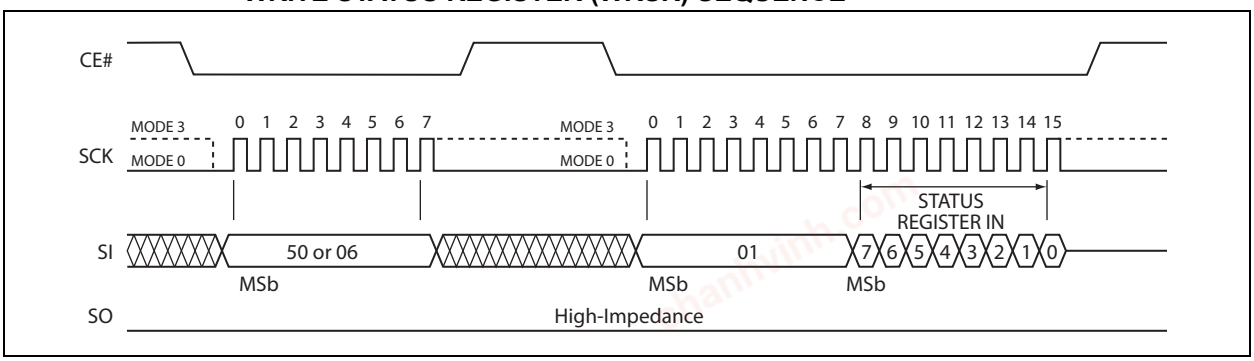
4.4.14 WRITE STATUS REGISTER (WRSR)

The Write Status Register instruction writes new values to the BP3, BP2, BP1, BP0 and BPL bits in the STATUS register. CE# must be driven low before the WRSR instruction sequence is issued and driven high before the WRSR instruction is executed. See Figure 4-17 for the EWSR or WREN and WRSR instruction sequences.

The device ignores the Write Status Register instruction when WP# is low and the BPL bit is set to '1'. When WP# is low, the BPL bit can only transition from '0' to '1' to lock down the STATUS register, but cannot be reset from '1' to '0'.

When WP# is high, the lockdown function of the BPL bit is disabled, and the BPL, BP0, and BP1 and BP2 bits in the STATUS register can be modified. As long as the BPL bit is set to '0' or the WP# pin is driven high (V_{IH}) before the low-to-high transition on CE# at the end of the WRSR instruction, the STATUS register bits can be modified by the WRSR instruction. In this case, a single WRSR instruction can set the BPL bit to '1' to lock down the STATUS register while also modifying the BP0, BP1 and BP2 bits. See Table 4-1 for a summary of WP# and BPL functions.

FIGURE 4-17: ENABLE WRITE STATUS REGISTER (EWSR) OR WRITE ENABLE (WREN) AND WRITE STATUS REGISTER (WRSR) SEQUENCE



4.4.15 JEDEC READ ID

The JEDEC Read ID instruction identifies the device as SST25VF080B device and the manufacturer as Microchip. Device information is read by issuing the 8-bit command, 9FH. After the JEDEC Read ID instruction is issued, the 8-bit Manufacturer ID (BFH) is output from the device.

A 16-bit Device ID is then shifted out on the SO pin. Byte 1 (BFH) identifies Microchip as the manufacturer. Byte 2 (25H) identifies the memory type as SPI serial Flash. Byte 3 (8EH) identifies the device as SST25VF080B. The instruction sequence is shown in Figure 4-18. The JEDEC Read ID instruction is terminated by a low-to-high transition on CE# at any time during data output.

FIGURE 4-18: JEDEC READ ID SEQUENCE

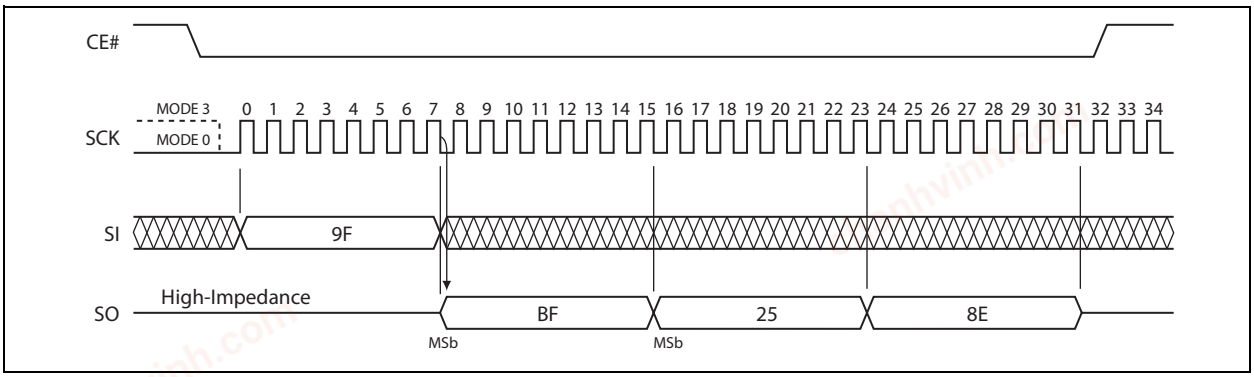


TABLE 4-5: JEDEC READ ID DATA

Manufacturer ID	Device ID	
	Memory Type	Memory Capacity
Byte1	Byte 2	Byte 3
BFH	25H	8EH

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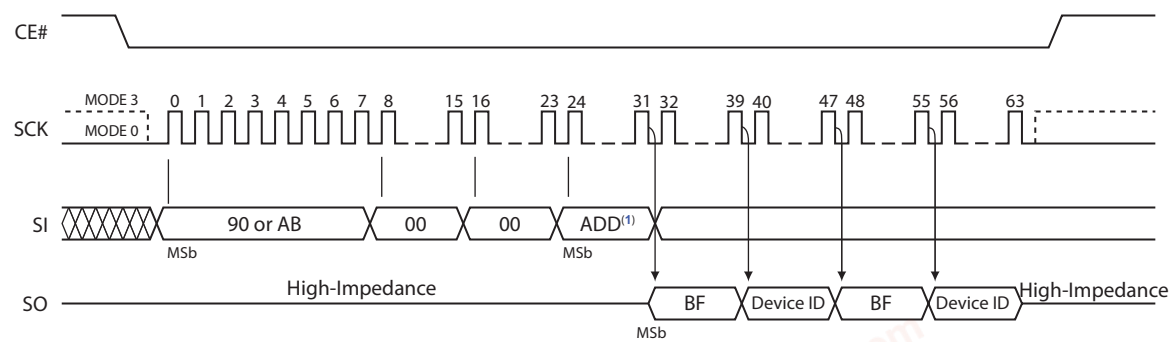
4.4.16 READ ID (RDID)

The Read ID instruction (RDID) identifies the device as SST25VF080B and the manufacturer as Microchip. This command is backward-compatible and should be used as the default device-identification method when multiple versions of SPI serial Flash devices are used in a design. Device information is read by issuing the 8-bit command, 90H or ABH, followed by address bits [A23-A0].

Following the Read-ID instruction, the Manufacturer ID is located at address 00000H, and the Device ID is located at address 00001H. Once the device enters Read-ID mode, the Manufacturer and Device ID output alternate between address 00000H and 00001H until terminated by a low-to-high transition on CE#.

Refer to Table 4-5 and Table 4-6 for device-identification data.

FIGURE 4-19: READ ID SEQUENCE



Note 1: The Manufacturer and Device ID output stream is continuous until terminated by a low-to-high transition on CE#. The Device ID for SST25VF080B is 8EH.

TABLE 4-6: PRODUCT IDENTIFICATION

	Address	Data
Manufacturer ID	00000H	BFH
Device ID		
SST25VF080B	00001H	8EH

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5.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (†)

Temperature under bias ..... -55°C to +125°C

Storage temperature ..... -65°C to +150°C

DC voltage on any pin to ground potential ..... -0.5V to V_{DD}+0.5V

Transient voltage (< 20 ns) on any pin to ground potential ..... -2.0V to V_{DD}+2.0V

Package power dissipation capability (T_A = +25°C) 1.0W

Surface mount solder reflow temperature ..... +260°C for 10 seconds

Output short circuit current[1] ..... 50 mA

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Output shorted for no more than one second. No more than one output shorted at a time.

TABLE 5-1: OPERATING RANGE

Range	Ambient Temperature	V_{DD}
Commercial	0°C to +70°C	2.7V to 3.6V
Industrial	-40°C to +85°C	2.7V to 3.6V

TABLE 5-2: AC CONDITIONS OF TEST[1]

Input Rise/Fall Time	Output Load
5 ns	C_L = 30 pF

Note 1: See Figure 5-2 and Figure 5-3.

5.1 Power-Up Specifications

All functionality and DC specifications are valid for a V_{DD} ramp rate greater than 1V per 100 ms (0V to 3.0V in less than 300 ms). See Table 5-3 and Figure 5-1 for additional information.

TABLE 5-3: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	V_{DD} Minimum to Read Operation	100	µs
$T_{PU-WRITE}$[1]	V_{DD} Minimum to Write Operation	100	µs

Note 1: This parameter is measured only during initial qualification and after a design or process change that may affect the parameter.

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FIGURE 5-1: POWER-UP TIMING DIAGRAM

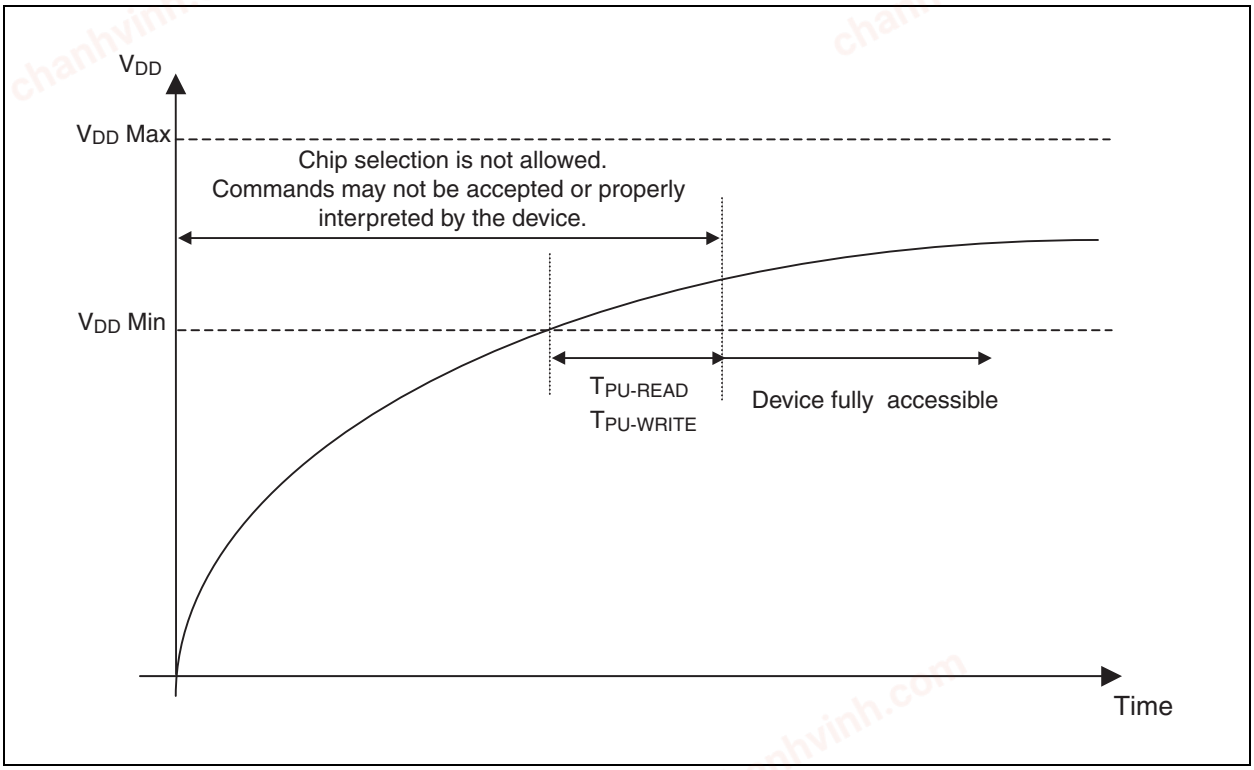
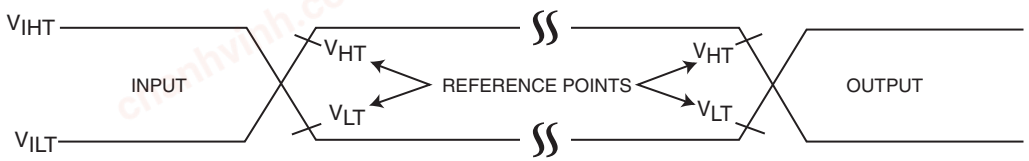


FIGURE 5-2: AC INPUT/OUTPUT REFERENCE WAVEFORMS



AC test inputs are driven at VIHT (0.9 VDD) for a logic '1' and VILT (0.1 VDD) for a logic '0'. Measurement reference points for inputs and outputs are VHT (0.6 VDD) and VLT (0.4 VDD).

Input rise/fall times (10% ↔ 90%) are < 5 ns.

Note: VHT - VHIGH Test
VLT - VLOW Test
VIHT - VINPUT HIGH Test
VILT - VINPUT LOW Test

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FIGURE 5-3: A TEST LOAD EXAMPLE

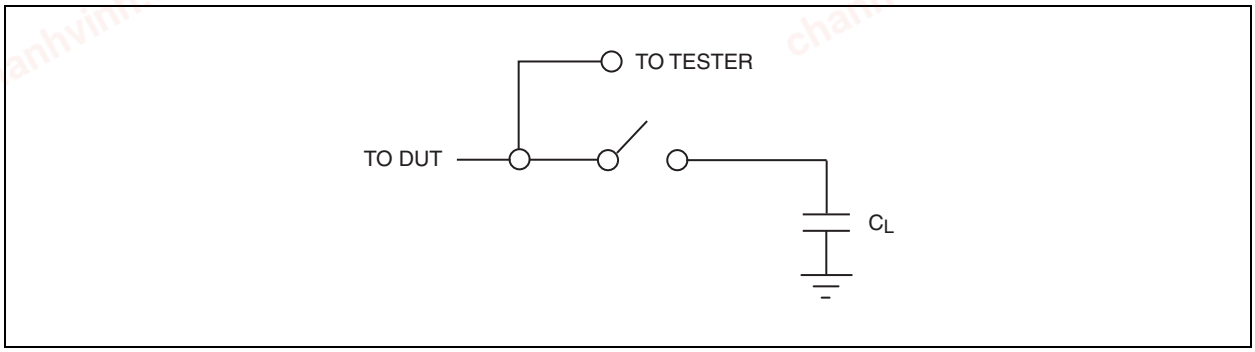


TABLE 5-4: DC OPERATING CHARACTERISTICS

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Units	
I_{DDR1}	Read Current	—	10	mA	CE# = 0.1 V_{DD}/0.9 V_{DD}@25 MHz, SO = open
I_{DDR2}	Read Current	—	15	mA	CE# = 0.1 V_{DD}/0.9 V_{DD}@50 MHz, SO = open
I_{DDW}	Program and Erase Current	—	30	mA	CE# = V_{DD}
I_{SB}	Standby Current	—	20	µA	CE# = V_{DD}, V_{IN} = V_{DD} or V_{SS}
I_{LI}	Input Leakage Current	—	1	µA	V_{IN} = GND to V_{DD}, V_{DD} = V_{DD} maximum
I_{LO}	Output Leakage Current	—	1	µA	V_{OUT} = GND to V_{DD}, V_{DD} = V_{DD} maximum
V_{IL}	Input Low Voltage	—	0.8	V	V_{DD} = V_{DD} minimum
V_{IH}	Input High Voltage	0.7 V_{DD}	—	V	V_{DD} = V_{DD} maximum
V_{OL1}	Output Low Voltage	—	0.2	V	I_{OL} = 100 µA, V_{DD} = V_{DD} minimum
V_{OL2}	Output Low Voltage	—	0.4	V	I_{OL} = 1.6 mA, V_{DD} = V_{DD} minimum
V_{OH}	Output High Voltage	V_{DD} -0.2	—	V	I_{OH} =- 100 µA, V_{DD} = V_{DD} minimum

TABLE 5-5: CAPACITANCE (T_A = +25°C, F = 1 MHz, OTHER PINS OPEN)

Parameter	Description	Test Condition	Maximum
$^1C_{OUT}$(1)	Output Pin Capacitance	V_{OUT} = 0V	12 pF
C_{IN}(1)	Input Capacitance	V_{IN} = 0V	6 pF

Note 1: This parameter is measured only during initial qualification and after a design or process change that could affect this parameter.

TABLE 5-6: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}(1)	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}(1)	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}(1)	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

Note 1: This parameter is measured only for initial qualification and after a design or process change that may affect the parameter.

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TABLE 5-7: AC OPERATING CHARACTERISTICS

Symbol	Parameter	25 MHz		50 MHz		66 MHz (1,2)		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
F_{CLK}(3)	Serial Clock Frequency	—	25	—	50	—	66	MHz
T_{SCKH}	Serial Clock High Time	18	—	9	—	7	—	ns
T_{SCKL}	Serial Clock Low Time	18	—	9	—	7	—	ns
T_{SCKR}(4)	Serial Clock Rise Time (slew rate)	0.1	—	0.1	—	0.1	—	V/ns
T_{SCKF}	Serial Clock Fall Time (slew rate)	0.1	—	0.1	—	0.1	—	V/ns
T_{CES}(5)	CE# Active Setup Time	10	—	5	—	4	—	ns
T_{CEH}(5)	CE# Active Hold Time	10	—	5	—	4	—	ns
T_{CHS}(5)	CE# Not Active Setup Time	10	—	5	—	4	—	ns
T_{CHH}(5)	CE# Not Active Hold Time	10	—	5	—	4	—	ns
T_{CPH}	CE# High Time	100	—	50	—	100	—	ns
T_{CHZ}	CE# High-to-High Z Output	—	15	—	8	—	6	ns
T_{CLZ}	SCK Low-to-Low Z Output	0	—	0	—	0	—	ns
T_{DS}	Data In Setup Time	5	—	2	—	2	—	ns
T_{DH}	Data In Hold Time	5	—	5	—	3	—	ns
T_{HLS}	HOLD# Low Setup Time	10	—	5	—	4	—	ns
T_{HHS}	HOLD# High Setup Time	10	—	5	—	4	—	ns
T_{HLH}	HOLD# Low Hold Time	10	—	5	—	4	—	ns
T_{HHH}	HOLD# High Hold Time	10	—	5	—	4	—	ns
T_{HZ}	HOLD# Low-to-High Z Output	—	20	—	8	—	8	ns
T_{LZ}	HOLD# High-to-Low Z Output	—	15	—	8	—	8	ns
T_{OH}	Output Hold from SCK Change	0	—	0	—	0	—	ns
T_V	Output Valid from SCK	—	15	—	8	—	6	ns
T_{SE}	Sector Erase	—	25	—	25	—	25	ms
T_{BE}	Block Erase	—	25	—	25	—	25	ms
T_{SCE}	Chip Erase	—	50	—	50	—	50	ms
T_{BP}	Byte Program	—	10	—	10	—	10	µs

Note 1: V_{DD} = 3.0V to 3.6V, C_L = 15 pF

2: Characterized but not fully tested.

3: The maximum clock frequency for the Read instruction (03H) is 25 MHz.

4: The maximum rise and fall times may be limited by T_{SCKH} and T_{SCKL} requirements.

5: Relative to SCK.

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FIGURE 5-4: SERIAL INPUT TIMING DIAGRAM

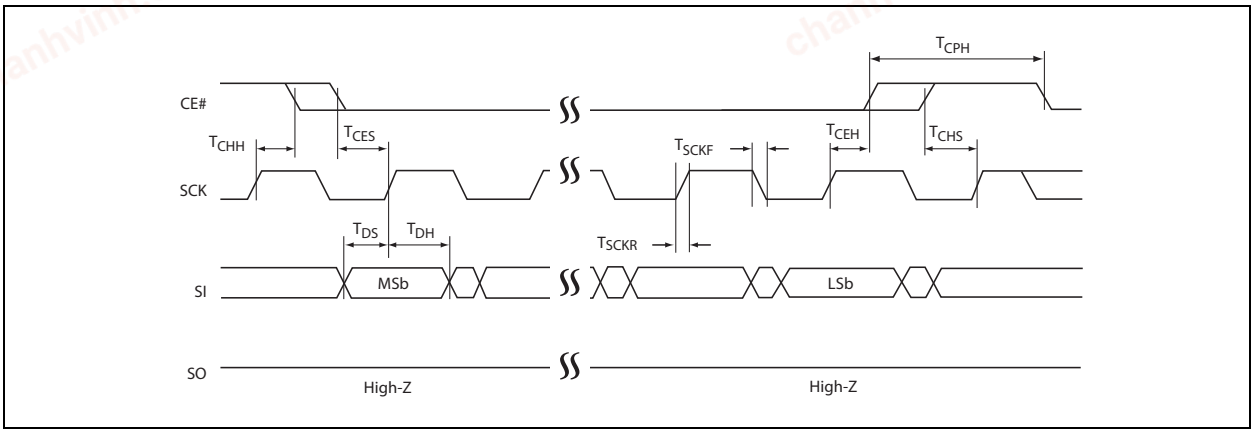


FIGURE 5-5: SERIAL OUTPUT TIMING DIAGRAM

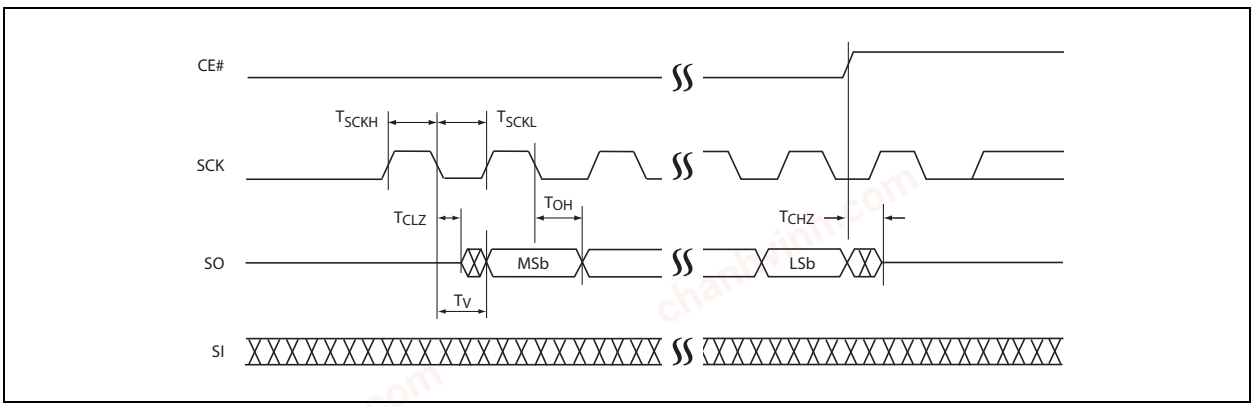
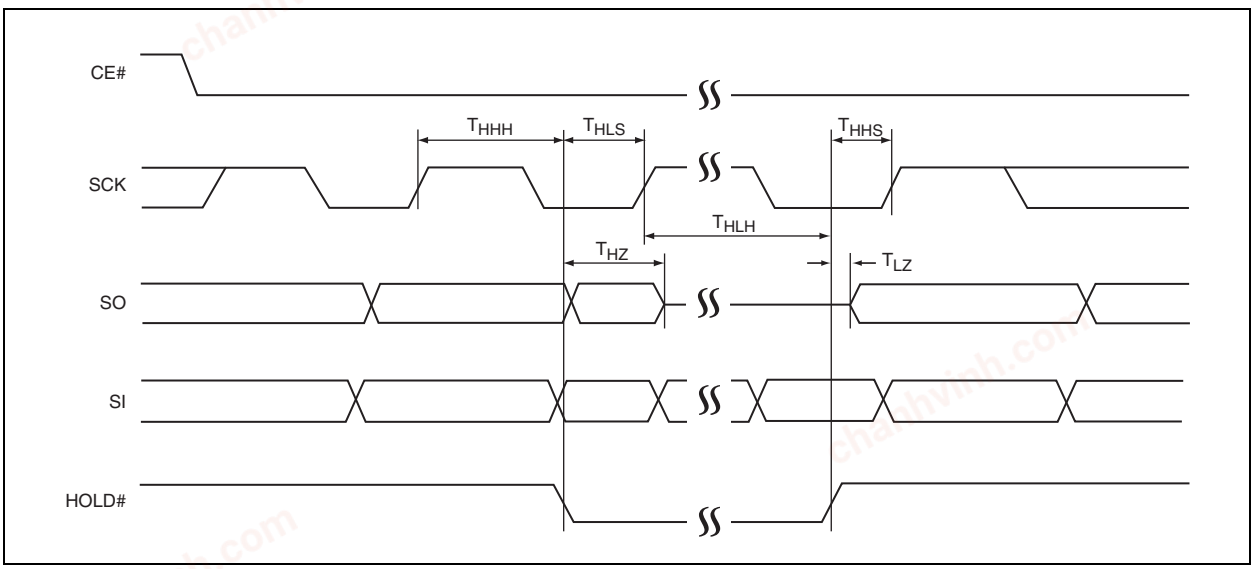


FIGURE 5-6: HOLD TIMING DIAGRAM



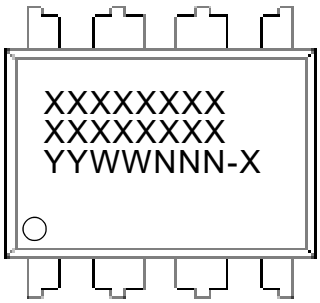
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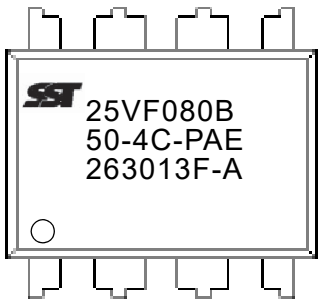
6.0 PACKAGING INFORMATION

6.1 Package Marking

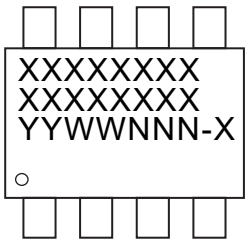
8-Lead PDIP (300 mil)
(Top View)



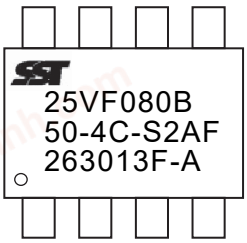
Example



8-Lead SOIC (3.90 mm)
(Top View)



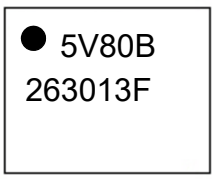
Example



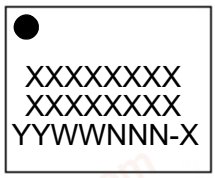
8-Lead USON (2x3 mm)
(Top View)



Example



8-Contact WSON (6x5 mm)
(Top View)



Example



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Part Number	1st Line Marking Codes			
	PDIP	SOIC	USON	WSON
SST25VF080B	25VF080B	25VF080B	5V80B	25VF080B

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	RoHS compliant JEDEC® designator for Matte Tin (Sn)

Note: For very small packages with no room for the RoHS compliant JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

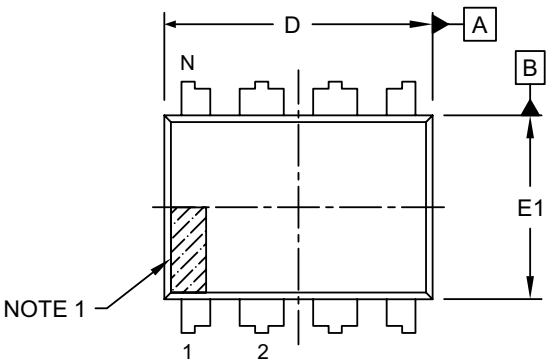
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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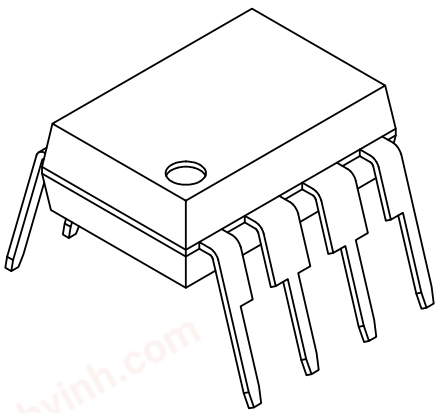
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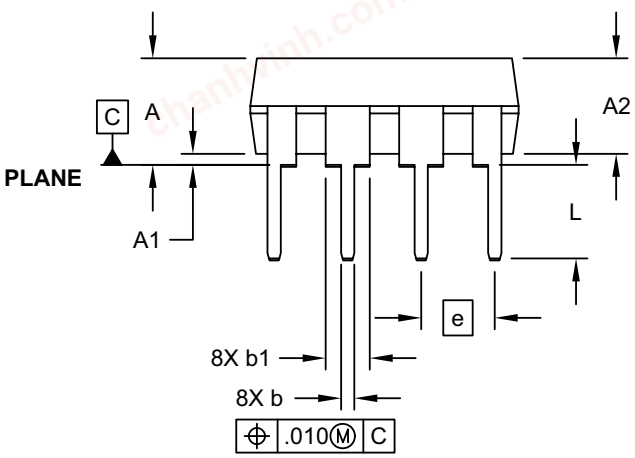
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

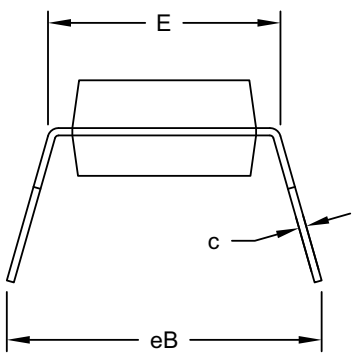


TOP VIEW





SIDE VIEW



END VIEW

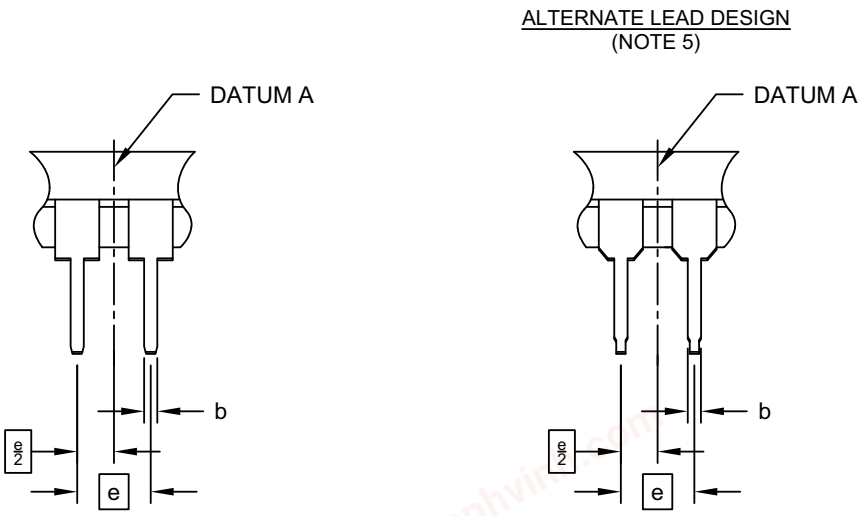
Microchip Technology Drawing No. C04-018-P Rev G Sheet 1 of 2

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8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

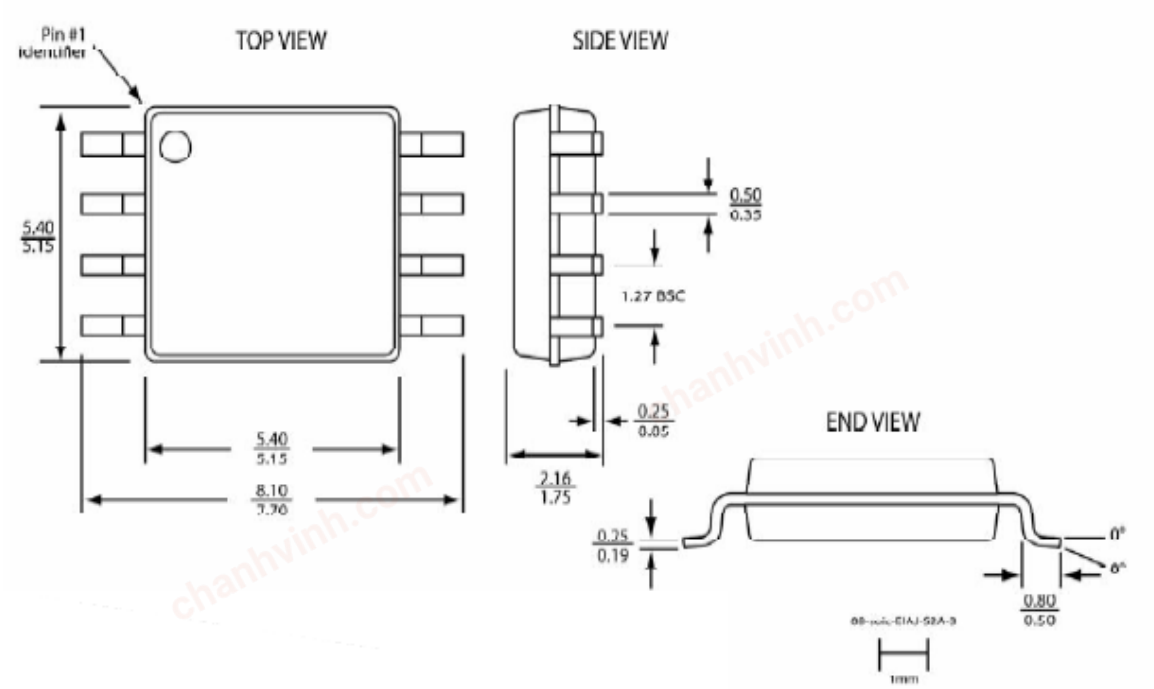
Microchip Technology Drawing No. C04-018-P Rev G Sheet 2 of 2

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8-Lead Small Outline Integrated Circuit (S2AE/F) - .208 Inch Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Note:

1. All linear dimensions are in millimeters (max/min).
2. Coplanarity: 0.1 mm
3. Maximum allowable mold flash is 0.15 mm at the package ends and 0.25 mm between leads.

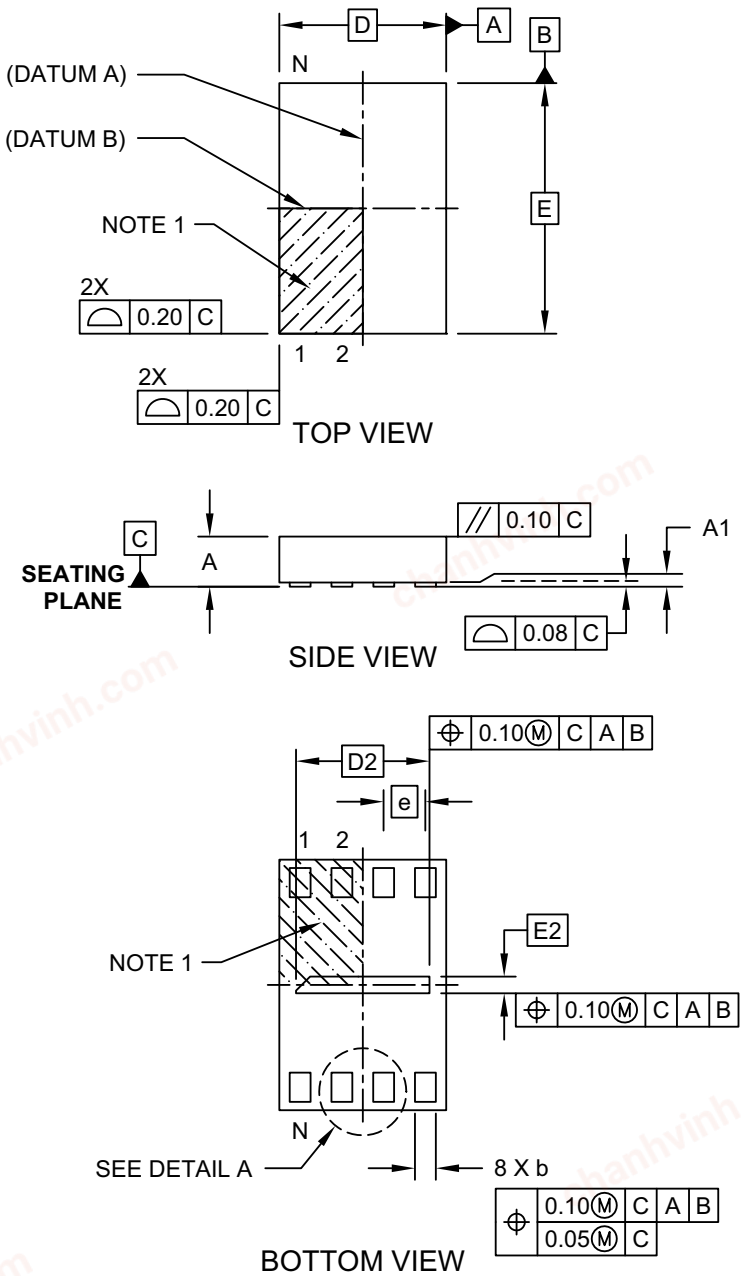
Microchip Technology Drawing C04-14005A Sheet 1 of 1

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8-Lead Plastic Ultra Thin Small Outline No Lead Package (PRX) - 2x3 mm Body [USON] [Also called UDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



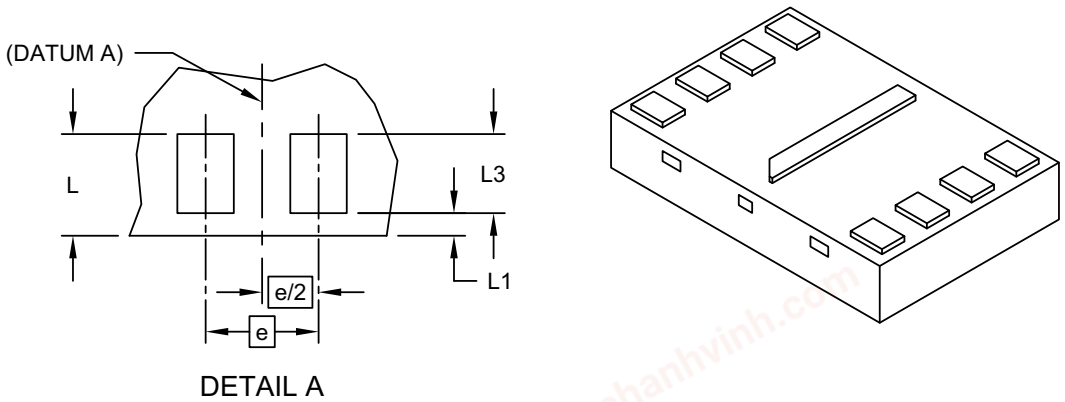
Microchip Technology Drawing C04-203C [PRX] Sheet 1 of 2

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8-Lead Plastic Ultra Thin Small Outline No Lead Package (PRX) - 2x3 mm Body [USON] [Also called UDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.45	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Overall Width	D		2.00 BSC	
Exposed Pad Width	D2	1.50	1.60	1.70
Overall Length	E		3.00 BSC	
Exposed Pad Length	E2	0.10	0.20	0.30
Terminal Width	b	0.20	0.25	0.30
Package Edge to Terminal Edge	L	0.40	0.45	0.50
Package Edge to Terminal Edge	L1	—	0.10	—
Terminal Length	L3	0.30	0.35	0.40

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

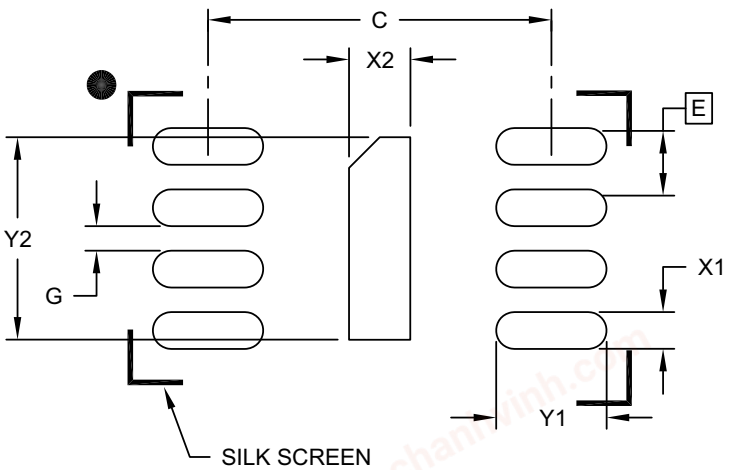
Microchip Technology Drawing C04-203C [PRX] Sheet 2 of 2

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8-Lead Plastic Ultra Thin Small Outline No Lead Package (PRX) - 2x3 mm Body [USON] [Also called UDFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Terminal Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			0.30
Optional Center Pad Length	Y2			1.70
Terminal Pad Spacing	C		2.80	
Terminal Pad Width (X8)	X1			0.30
Terminal Pad Length (X8)	Y1			0.90
Mininum Between Terminal Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

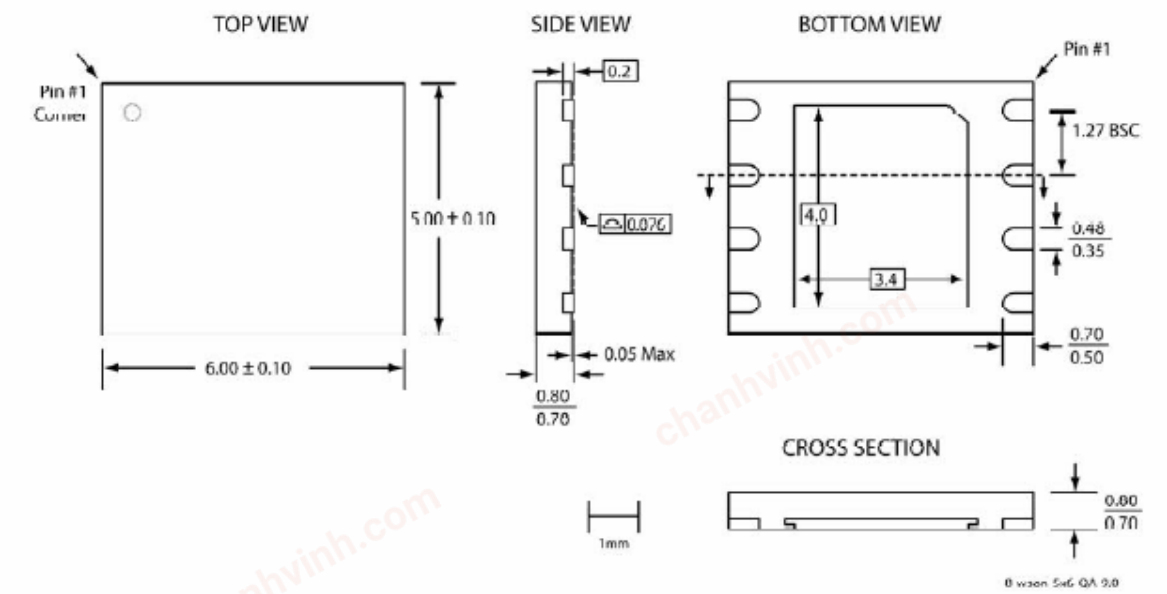
Microchip Technology Drawing C04-2203B [PRX]

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8-Lead Very, Very Thin Small Outline No-Leads (QAE/F) - 5x6 mm Body [WSON]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Note:

1. All linear dimensions are in millimeters (max/min).
2. Untoleranced dimensions (shown with box surround) are nominal target dimensions.
3. The external paddle is electrically connected to the die back-side and possibly to certain VSS leads. This paddle can be soldered to the PC board; it is suggested to connect this paddle to the VSS of the unit. Connection of this paddle to any other voltage potential can result in shorts and/or electrical malfunction of the device.

Microchip Technology Drawing C04-14008A Sheet 1 of 1

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APPENDIX A: REVISION HISTORY

Revision E (July 2026)

Added 8-contact USON (2 mm x 3 mm) package and removed 16-ball XFBGA package; Editorial updates throughout the document.

Revision D (March 2020)

Updated standby current. Updated formatting to current template. Updated package drawings to latest versions. Added package marking section. Updated Product Identification System Nickel plating note. Added 16-ball XFBGA package.

Revision C (February 2015)

Corrected a typo on page 8.

Revision B (June 2014)

EOL of all 80 MHz parts. Replacement parts are the 50 MHz counterparts found in this document. Removed all 80 MHz information. See DS20005266. EOL of SAE package. Updated document to new format. Replaced all package drawings with drawings in the new format.

Revision A (September 2011)

Added “Power-Up Specifications” on page 21. Updated Table 5-7 on page 21. Released document under letter revision system. Updated Spec number from S71296 to DS25045.

Revision 05 (February 2011)

Updated “Auto Address Increment (AAI) Word Program”, “End of Write Detection”, and “Hardware End of Write Detection” on page 10. Revised Figures 4-8 and 4-9 on page 11. Updated document to new format. Added SAE package drawing and SAE information.

Revision 04 (January 2010)

Added 80 MHz High Speed Clock Frequency to Features. Removed Maximum Frequency from Table 4-4 on page 7. Edited “Read (25 MHz)” on page 8 and “High-Speed-Read (66 MHz)” on page 8. Added 80 MHz information to “Electrical Specifications” on page 18. Edited Product Ordering Information. Added Valid Combinations SST25VF080B-80-4C-S2AE, SST25VF080B-80-4I-S2AE, SST25VF080B-80-4C-QAE
and SST25VF080B-80-4I-QAE.

Revision 03 (March 2009)

Modified “Features”, “Pin Description” and “Packaging Diagrams” to include the PAE package. Updated Figures 4-8 and 4- 9 on page 11.

Revision 02 (June 2007)

Updated Features. Updated Table 4-4 on page 7. Updated “High-Speed-Read (66 MHz)” on page 8. Updated Table 5-6 on page 19.

Revision 01 (January 2006)

Migrated document to a Data Sheet. Updated Surface Mount Solder Reflow Temperature information.

Revision 00 (September 2005)

Initial release of the document.

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SST25VF080B

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–	XX	–	XX	–	XX	–	X[1]
Device		Operating Frequency		Minimum Endurance / Temp Range		Package		Tape/Reel Indicator

Device:	SST25VF080B	= 8 Mbit, 2.7V-3.6V, SPI Flash Memory
Operating Frequency:	50	= 50 MHz/66 MHz
Minimum Endurance	4	= 10,000 cycles
Temperature Range:	I	= -40°C to +85°C (Industrial)
	C	= 0°C to +70°C (Commercial)
Package:	PAE/PAF	= PDIP (300 mil Body), 8-Lead
	S2AF/S2AE	= SOIC (200 mil Body), 8-Lead
	PR	= USON (2 mm x 3 mm Body), 8-Lead
	QAF/QAE	= WSON (6 mm x 5 mm Body), 8-Contact
Package Modifier:	A	= 8 leads or contacts
Environmental Attribute:	E	= Matte Tin finish
	F	= Nickel plating with Gold top (outer) layer finish or Matte Tin finish
Tape and Reel Indicator[1]	Blank	= Standard packaging (tube or tray)
	T	= Tape and Reel

Valid Combinations:

a) SST25VF080B-50-4C-S2AF
b) SST25VF080B-50-4C-S2AF-T
c) SST25VF080B-50-4I-S2AF
d) SST25VF080B-50-4I-S2AF-T
e) SST25VF080B-50-4I-S2AE
f) SST25VF080B-50-4I-S2AE-T
g) SST25VF080B-50-4C-QAF
h) SST25VF080B-50-4C-QAF-T
i) SST25VF080B-50-4I-QAF
j) SST25VF080B-50-4I-QAF-T
k) SST25VF080B-50-4I-QAE
l) SST25VF080B-50-4I-QAE-T
m) SST25VF080B-50-4C-PAE
n) SST25VF080B-50-4I-PRAE-T

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package.

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