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SAM9X75 System-in-Package (SiP) MPU with up to 2-Gbit DDR SDRAM

SAM9X75 SiP Data Sheet

Product Page Links

Scope

This document is an overview of the main features of the SAM9X75 SiP microprocessor. The sole reference documents for product information on SAM9X7 Series microprocessors and DDR2/DDR3L SDRAM memories are listed in Reference Documents.

Introduction

The SAM9X75 SiP integrates the ARM926 Arm® processor-based SAM9X75 MPU with an up to 2-Gbit DDR SDRAM. By combining the SAM9X75 with a DDR SDRAM in a single package, PCB routing complexity, area and number of layers are reduced in the majority of cases. This makes board design easier and more robust by facilitating design for EMI, ESD and signal integrity.

The SAM9X75 SiP is available in three pin-to-pin compatible SDRAM memory types and densities:

- 512-Mbit DDR2 SDRAM
- 1-Gbit DDR3L SDRAM
- 2-Gbit DDR3L SDRAM

The SAM9X75 SiP is available in ambient temperature ranges up to 105°C and is AEC-Q100 grade 2 qualified.

Reference Documents

Type	Name	Available	Literature No.
Data sheet	SAM9X7 Series	www.microchip.com	DS60001813
Data sheet	8M × 4 BANKS × 16 BIT DDR2 SDRAM (512 Mbits)	www.winbond.com	W9751G6NB
Data sheet	8M × 8 BANKS × 16 BIT DDR3L SDRAM (1 Gbit)	www.winbond.com	W631GU6NB
Data sheet	16M × 8 BANKS × 16 BIT DDR3L SDRAM (2 Gbits)	www.winbond.com	W632GU6NB

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1. Features

- CPU Running up to 800 MHz
  - ARM926EJ-S Arm Thumb® processor
  - 32-Kbyte data cache, 32-Kbyte instruction cache, Memory Management Unit (MMU)
- Memories
  - One 176-Kbyte internal ROM
    - 80-Kbyte internal ROM embedding a secure bootloader program supporting boot on NAND Flash, SD Card, SPI or QSPI Flash; bootloader features selectable by OTP bits
    - 96-Kbyte ROM for NAND Flash BCH ECC table
  - One 64-Kbyte internal SRAM (SRAM0), single cycle access at system speed
  - Internal DDR2 or DDR3L SDRAM running at up to 266 MHz
  - External Bus Interface (EBI) supporting:
    - 8-bit NAND Flash with up to 24-bit programmable multi-bit error correcting code
  - One 10-Kbyte OTP memory for secure key storage with Emulation mode (OTP bits are emulated by a 4-Kbyte SRAM (SRAM1))
- System Running up to 266 MHz
  - Power-on reset cells, reset controller, shutdown controller, periodic interval timer, watchdog timer running on internal slow RC oscillator (32 kHz typical) and real-time clock running on slow crystal oscillator (32.768 kHz)
  - Two internal trimmed RC oscillators with typical values: 32 kHz (slow) and 12 MHz (fast)
  - Two crystal oscillators: 32.768 kHz (slow) and 20 to 50 MHz (fast)
  - One PLL for the system and one PLL optimized for USB high-speed operation (480 MHz)
    - One PLL for audio operations, with dedicated output clock
    - One PLL in LVDS I/F (LVDS usage only)
    - One PLL in MIPI DPHY (MIPI DSI usage only)
  - One dual-port 16-channel DMA controller
  - Advanced interrupt controller and debug unit
  - JTAG port with disable bit in OTP memory
  - Two programmable clock output signals
- Low-Power Modes
  - Backup mode with RTC, eight 32-bit general-purpose backup registers, and a shutdown controller to control the external power supply
  - Clock generator and power management controller
  - Software-programmable ultra-low power modes: very slow clock operating mode (ULP0) and no-clock operating mode (ULP1) with fast wake-up capabilities
  - Software programmable power optimization capabilities
- Peripherals
  - LCD controller with overlay, alpha blending, rotation, scaling and color conversion; up to 720p resolution
    - RGB, LVDS, MIPI-DSI interfaces
  - 2D graphics controller supporting fill BLT, copy BLT, transparent BLT, blend/alpha BLT, ROP4 BLT (raster operations) and command ring buffer

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  - Image sensor controller with ITU-R BT; 601/656/1120 video interface support up to 5 Mpixels; support of raw Bayer 12, YCbCr, monochrome and JPEG compressed sensors up to 12 bits
    - MIPI CSI2 I/F support
    - 12-bit parallel I/F support
  - One high-speed USB device, three high-speed USB hosts with dedicated on-chip transceivers
  - One 10/100/1000 Mbps Ethernet Mac controller with IEEE-1588 and TSN support, RGMII and RMII support
  - Two 4-bit secure digital multimedia card controllers
  - Two CAN FD controllers with timestamping
  - One Quad/Octal SPI controller
  - Two 3-channel 32-bit timers/counters
  - Two high-resolution (64-bit) periodic interval timers
  - One synchronous serial controller
  - One inter-IC sound multi-channel controller with TDM support
  - One audio class D controller with single-ended or bridge-tied load connection to power stage
  - One 4-channel 16-bit PWM controller
  - Thirteen FLEXCOMs (USART, SPI and TWI/I2C)
  - One 8-channel, 12-bit, analog-to-digital converter with 4/5 wires resistive touchscreen support
- Hardware Cryptography
  - SHA (SHA1, SHA224, SHA256, SHA384, SHA512) and HMAC compliant with FIPS PUB 180
  - AES: 256-, 192-, 128-bit key algorithms compliant with FIPS PUB 197
  - AES/SHA tight coupling for IPsec hardware acceleration
  - TDES: 2-key or 3-key algorithms compliant with FIPS PUB 46
  - True random number generator compliant with NIST Special Publication 800-22 Test Suite and FIPS PUBs 140-2 and 140-3
  - Key bus providing private key transfers between AES, TDES, TRNG, OTPC
  - Physical Unclonable Function (PUF) including NIST SP 800-90B (DRNG) and embedding four Kbytes of SRAM (PUFSRAM)
- I/O Ports
  - Four 32-bit parallel input/output controllers
  - Up to 106 programmable I/O lines multiplexed with up to four peripheral I/Os
  - Input change interrupt capability on each I/O line, optional Schmitt Trigger input
  - Individually programmable open-drain, pull-up and pull-down resistors, synchronous output
  - General-purpose analog and digital inputs tolerant to positive and negative current injection
- Package
  - 16x16 mm^2, 0.8-mm pitch, 243-ball BGA optimized for standard class PCB layout (down to four layers)
- Design for Low ElectroMagnetic Interference (EMI)
  - Slewrate-controlled I/Os
  - DDR PHY with impedance-calibrated drivers
  - Spread spectrum PLLs
  - BGA power/ground ball assignment to provide optimum decoupling capacitors placement

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- Qualification
  - AEC-Q100 Grade 2 ([-40°C to +105°C] ambient temperature); applies to -V/4TBVAO devices only
  - The AEC-Q006 set of tests applies, as only copper wire interconnections are used
- Operating Conditions
  - Ambient temperature (T_A) range:
    - -40°C to +85°C for SAM9X75D5M, SAM9X75D1G, SAM9X75D2G
    - -40°C to +105°C for SAM9X75D5M
  - Junction temperature (T_J) range: -40°C to +125°C

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2. Ordering Information

Ordering Code[1][2]	Memory Type	Memory Size	Package	Ambient Temperature Range
SAM9X75D5M(T)-V/4TB(-SLx)(VAO)	DDR2 SDRAM	512 Mbits	TFBGA243	-40°C to +105°C
SAM9X75D5M(T)-I/4TB(-SLx)				-40°C to +85°C
SAM9X75D1G(T)-I/4TB(-SLx)	DDR3L SDRAM	1 Gbit		
SAM9X75D2G(T)-I/4TB(-SLx)		2 Gbits		

Notes:

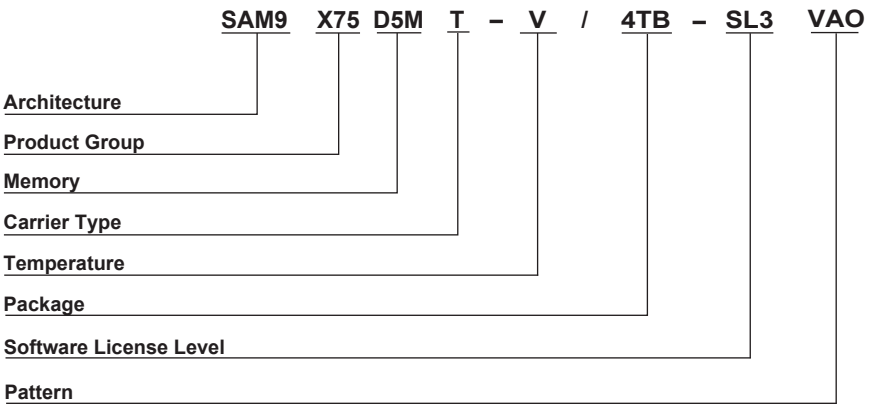
1. For details on ordering codes, see Product Identification System.
2. For SL1, SL2 and SL3 device availability, contact a Microchip Sales representative.

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3. Product Identification System

To order or obtain information, for example, on pricing or delivery, contact Microchip: https://www.microchip.com/en-us/about/contact-us.



Architecture:	SAM9	= ARM926EJ–S Arm Thumb microprocessor
Product Group:	X75	= General purpose microprocessor
Memory Type and Size:	D5M	= 512-Mbit DDR2 SDRAM
	D1G	= 1-Gbit DDR3L SDRAM
	D2G	= 2-Gbit DDR3L SDRAM
Carrier Type:	Blank	= Standard packaging (tray)
	T	= Tape and reel
Ambient Temperature Range:	I	= –40°C to +85°C (industrial)
	V	= –40°C to +105°C (extended industrial or automotive (AEC-Q100 grade 2))
Package:	4TB	= TFBGA243
Software License Level:	Blank	= Standard
	SL1	= Level 1
	SL2	= Level 2
	SL3	= Level 3
Pattern:	Blank	= Standard device
	VAO	= Automotive flow/material without PPAP. Available upon request.
	Vxx	= Automotive flow/material with associated PPAP. Available upon request.

Example:

- SAM9X75D5MT–V/4TB-SL3VAO = ARM926EJ–S Arm Thumb microprocessor, 512-Mbit DDR2 SDRAM, tape and reel packaging, –40°C to +105°C temperature range, 243-ball TFBGA package, software license level 3, automotive flow/material without PPAP

Note:
The Tape and Reel identifier and the Software License Level identifier only appear in the catalog part number description. These identifiers are used for ordering purposes and are not printed on the device package. Check with your Microchip Sales Office for package availability.

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4. DDR2 SDRAM Features

The SAM9X75 SiP is available with a 512-Mbit DDR2 SDRAM memory option.

For power consumption, electrical characteristics and memory timings, refer to the manufacturer's documentation listed in Reference Documents.

- Power Supply: DDRM_VDD = 1.8V ±0.1V
- Double Data Rate architecture: two data transfers per clock cycle
- CAS latency: 3
- Burst length: 8
- Bidirectional, differential data strobes (DQS and DQSN) are transmitted/received with data
- Edge-aligned with read data and center-aligned with write data
- DLL aligns DQ and DQS transitions with clock
- Differential clock inputs (CLK and CLKN)
- Data masks (DM) for write data
- Commands entered on each positive CLK edge; data and data mask referenced to both edges of DQS
- Auto-Refresh and Self-Refresh modes
- Precharged power-down and active power-down
- Write data mask
- Write latency = read latency - 1 (WL = RL - 1)

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5. DDR3L SDRAM Features

The SAM9X75 SiP is available with 1-Gbit and 2-Gbit DDR3L SDRAM memory options.

For power consumption, electrical characteristics and timings of these memories, refer to the manufacturer's documentation listed in Reference Documents.

- Power supply: DDRM_VDD = 1.283V to 1.45V
- 2-Kbyte page size (x16)
- 8-bank operation controlled by BA0, BA1 and BA2
- Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- Precharge: auto-precharge option for each burst access
- Auto-Refresh and Self-Refresh modes
- Average refresh period:
  - 7.8 µs at $T_J \leq +85°C$
  - 3.9 µs at $T_J \leq +105°C$
  - 1.95 µs at $T_J \leq +125°C$
- High-speed data transfer realized by the 8-bit prefetch pipelined architecture
- Double Data Rate architecture: two data transfers per clock cycle
- Bidirectional differential data strobe (DQS and /DQS) transmitted/received with data for capturing data at the receiver
- DQS edge-aligned with data for reads and center-aligned with data for writes
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted CAS by programmable additive latency for better command and data bus efficiency
- MultiPurpose Register (MPR) for predefined pattern read out
- ZQ calibration for DQ drive and ODT (pin DDRM_ZQ)
- Programmable Partial Array Self-Refresh (PASR)
- Self-Refresh Temperature (SRT) range: normal/extended
- Automatic Self-Refresh (ASR)
- Programmable output driver impedance control

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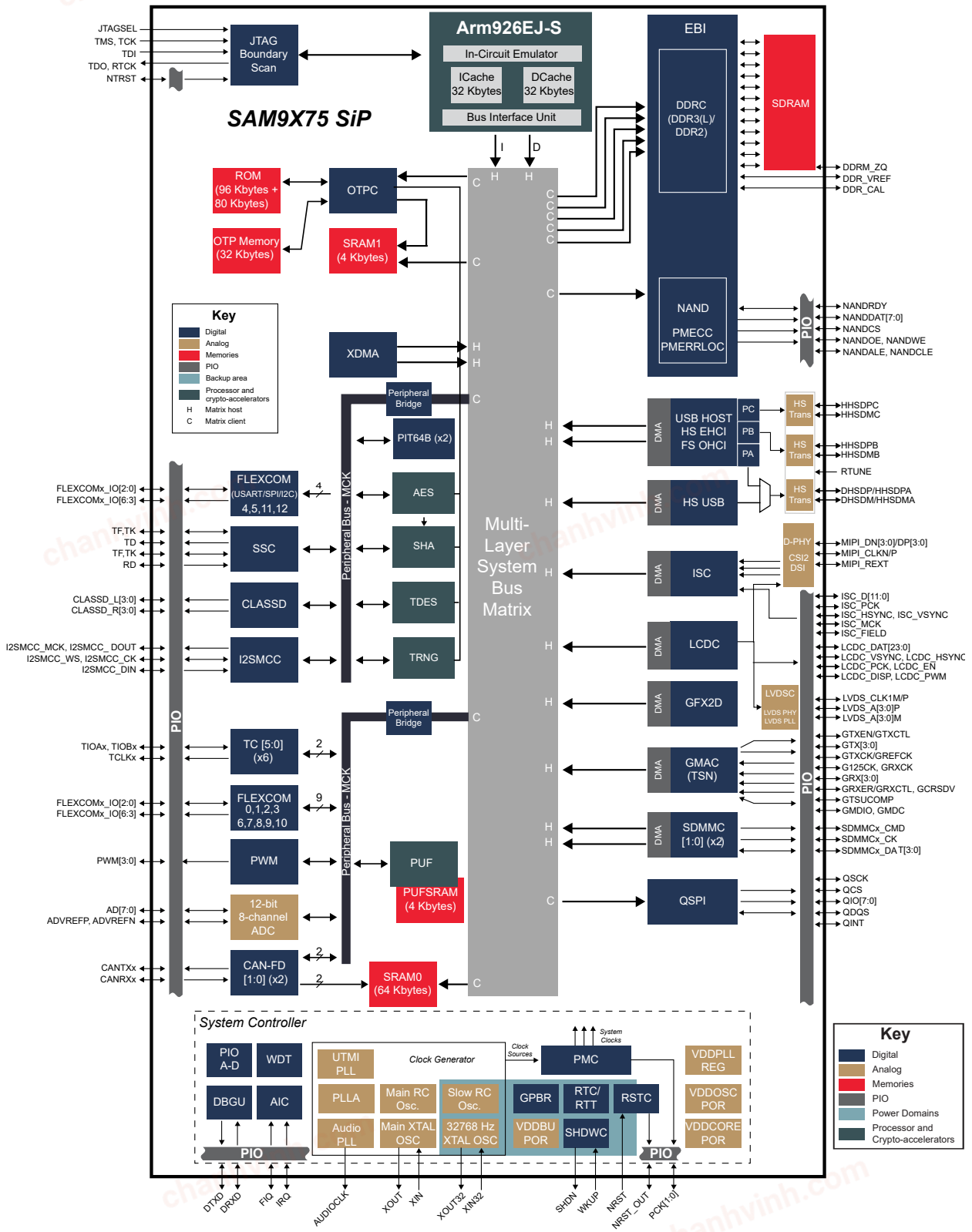
6. Configuration Summary

Feature	SAM9X75D5M	SAM9X75D1G	SAM9X75D2G
Package	BGA243, 16x16mm^2, pitch 0.8 mm		
EBI	8-bit NAND Flash controller		
SDRAM embedded in SiP	512-Mbit DDR2 SDRAM	1-Gbit DDR3L SDRAM	2-Gbit DDR3L SDRAM
Ambient temperature range	–40°C to +85°C		
	–40°C to +105°C	–	–
MIPI DPHY	Bidirectional, 4 lanes		
PIOs	106		
SRAM0/SRAM1	64/4 Kbytes		
Quad/Octal SPI	1		
LCD + GFX2D	LVDS, MIPI DSI, RGB interface		
Camera interface (ISC)	MIPI CSI2, parallel port		
GMAC	10/100/1000 with IEEE 1588 and TSN		
CAN-FD	2		
USB	3 (3 hosts or 2 host/1 device)		
UART/SPI/I2C	13		
SDIO/SD/MMC	2		
I2SMCC/SSC/Class D	1/1/1		
ADC inputs	8 (8 channels)		
64-bit timers/32-bit timers	2/6		
PWM	4 (PWMC)		
Cryptography	AES/TDES/SHA/TRNG		

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7. Block Diagram



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8. Chip Identifier

Table 8-1. Chip ID and Extended ID Definition

Chip Name	CHIPID_CIDR	CHIPID_EXID(1)
SAM9X75D5M	0x8975003x	0x00000010
		0x000000C8 (SL1)
		0x000000C9 (SL2)
		0x000000CA (SL3)
SAM9X75D1G		0x00000018
		0x000000CC (SL1)
		0x000000CD (SL2)
		0x000000CE (SL3)
SAM9X75D2G		0x00000020
		0x000000D0 (SL1)
		0x000000D1 (SL2)
		0x000000D2 (SL3)

Note:

1. For more information, refer to Product Identification System.

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9. Package and Pinout

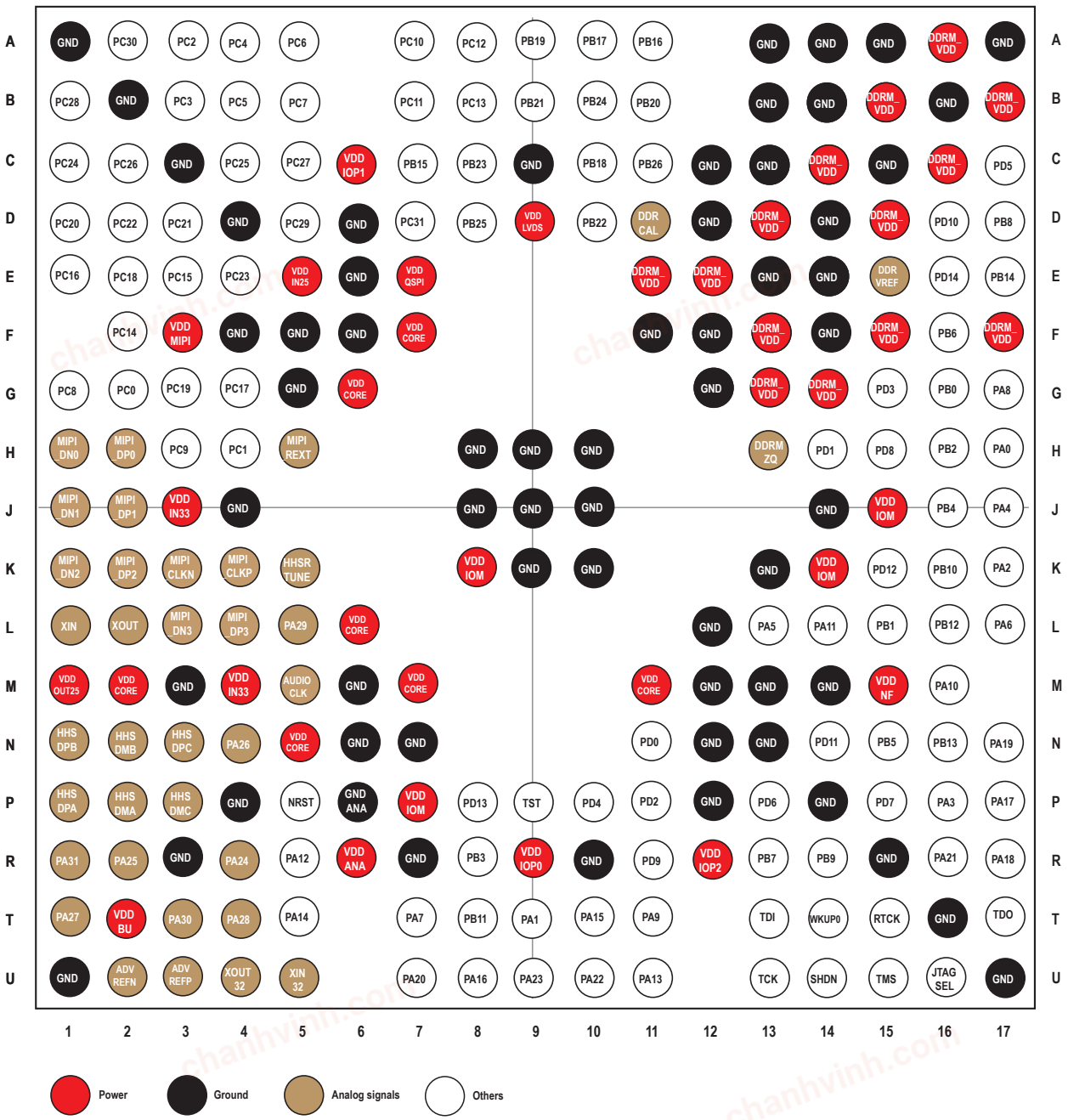
512-Mbit, 1-Gbit and 2-Gbit SAM9X75 SiP devices are pin-to-pin compatible.

Package Name	Ball Count	Ball Pitch	Package Size
TFBGA243	243	0.8 mm	16 x 16 (mm)

For further details, see Mechanical Characteristics.

9.1. TFBGA243 Package

Figure 9-1. 243-Ball TFBGA Pinout



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9.2. Ball Description

Table 9-1. Ball Description

BGA243 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State(1)
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
H17	VDDIOP0	GPIO	PA0	I/O	–	–	A	SDMMC0_DAT0	I/O	1	PIO, I, PU, ST
T9	VDDIOP0	GPIO	PA1	I/O	–	–	A	SDMMC0_CMD	I/O	1	PIO, I, PU, ST
K17	VDDIOP0	GPIO	PA2	I/O	WKUP1	–	A	SDMMC0_CK	I/O	1	PIO, I, PU, ST
P16	VDDIOP0	GPIO	PA3	I/O	–	–	A	SDMMC0_DAT1	I/O	1	PIO, I, PU, ST
J17	VDDIOP0	GPIO	PA4	I/O	–	–	A	SDMMC0_DAT2	I/O	1	PIO, I, PU, ST
L13	VDDIOP0	GPIO	PA5	I/O	–	–	A	SDMMC0_DAT3	I/O	1	PIO, I, PU, ST
L17	VDDIOP0	GPIO	PA6	I/O	–	–	A	FLEXCOM0_IO4	O	1	PIO, I, PU, ST
							B	SDMMC1_DAT1	I/O	1	
T7	VDDIOP0	GPIO	PA7	I/O	WKUP2	–	A	FLEXCOM0_IO3	I/O	1	PIO, I, PU, ST
							B	SDMMC1_DAT2	I/O	1	
G17	VDDIOP0	GPIO	PA8	I/O	WKUP3	–	A	FLEXCOM0_IO2	I/O	1	PIO, I, PU, ST
							B	SDMMC1_DAT3	I/O	1	
T11	VDDIOP0	GPIO	PA9	I/O	–	–	A	FLEXCOM4_IO1	I/O	1,2	PIO, I, PU, ST
							B	SDMMC1_DAT0	I/O	1	
M16	VDDIOP0	GPIO	PA10	I/O	–	–	A	FLEXCOM4_IO0	I/O	1,2	PIO, I, PU, ST
							B	SDMMC1_CMD	I/O	1	
L14	VDDIOP0	GPIO	PA11	I/O	–	–	A	FLEXCOM4_IO2	I/O	1,2	PIO, I, PU, ST
							B	SDMMC1_CK	I/O	1	
R5	VDDIOP0	GPIO	PA12	I/O	–	–	A	FLEXCOM4_IO3	I/O	1,2	PIO, I, PU, ST
							C	FLEXCOM5_IO4	O	1	
U11	VDDIOP0	GPIO	PA13	I/O	–	–	A	FLEXCOM2_IO0	I/O	1	PIO, I, PU, ST
							B	FLEXCOM4_IO4	O	1	
T5	VDDIOP0	GPIO	PA14	I/O	–	–	A	FLEXCOM2_IO1	I/O	1	PIO, I, PU, ST
							B	FLEXCOM5_IO3	I/O	1,2	
							C	FLEXCOM4_IO5	O	1	
T10	VDDIOP0	GPIO	PA15	I/O	–	–	A	TIOA0	I/O	1	PIO, I, PU, ST
							B	FLEXCOM5_IO1	I/O	1,2	
							C	CLASSD_R0	O	1	
U8	VDDIOP0	GPIO	PA16	I/O	–	–	A	TIOA1	I/O	1	PIO, I, PU, ST
							B	FLEXCOM5_IO0	I/O	1,2	
							C	CLASSD_R1	O	1	
P17	VDDIOP0	GPIO	PA17	I/O	–	–	A	TIOA2	I/O	1	PIO, I, PU, ST
							B	FLEXCOM5_IO2	I/O	1,2	
							C	CLASSD_R2	O	1	
R17	VDDIOP0	GPIO	PA18	I/O	–	–	A	TCLK0	I	1	PIO, I, PU, ST
							B	TK	I/O	1	
							C	CLASSD_L0	O	1	

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Table 9-1. Ball Description (continued)

BGA243 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State(1)
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
N17	VDDIOP0	GPIO	PA19	I/O	–	–	A	TCLK1	I	1	PIO, I, PU, ST
							B	TF	I/O	1	
							C	CLASSD_L1	O	1	
U7	VDDIOP0	GPIO	PA20	I/O	WKUP4	–	A	TCLK2	I	1	PIO, I, PU, ST
							B	TD	O	1	
							C	CLASSD_L2	O	1	
R16	VDDIOP0	GPIO	PA21	I/O	–	–	A	TIOB0	I/O	1	PIO, I, PU, ST
							B	RD	I	1	
							C	CLASSD_L3	O	1	
U10	VDDIOP0	GPIO	PA22	I/O	–	–	A	TIOB1	I/O	1	PIO, I, PU, ST
							B	RK	I/O	1	
							C	CLASSD_R3	O	1	
U9	VDDIOP0	GPIO	PA23	I/O	–	–	A	TIOB2	I/O	1	PIO, I, PU, ST
							B	RF	I/O	1	
							C	FLEXCOM2_IO7	I	1	
R4	VDDANA	GPIO	PA24	I/O	AD0	–	A	FLEXCOM6_IO0	I/O	1	PIO, I, PU, ST
							B	FLEXCOM5_IO6	O	1	
R2	VDDANA	GPIO	PA25	I/O	AD1	–	A	FLEXCOM6_IO1	I/O	1	PIO, I, PU, ST
							B	FLEXCOM5_IO5	O	1	
N4	VDDANA	GPIO	PA26	I/O	AD2	–	A	DRXD	I	1	PIO, I, PU, ST
							B	CANRX0	I	1	
T1	VDDANA	GPIO	PA27	I/O	AD3	–	A	DTXD	O	1	PIO, I, PU, ST
							B	CANTX0	O	1	
T4	VDDANA	GPIO	PA28	I/O	AD4	–	A	FLEXCOM1_IO0	I/O	1	PIO, I, PU, ST
							B	CANTX1	O	1	
L5	VDDANA	GPIO	PA29	I/O	AD5	–	A	FLEXCOM1_IO1	I/O	1	PIO, I, PU, ST
							B	CANRX1	I	1	
T3	VDDANA	GPIO	PA30	I/O	AD6	–	A	FLEXCOM0_IO0	I/O	1	PIO, I, PU, ST
							B	FLEXCOM5_IO4	O	2	
							C	FLEXCOM4_IO4	O	2	
R1	VDDANA	GPIO	PA31	I/O	AD7	–	A	FLEXCOM0_IO1	I/O	1	PIO, I, PU, ST
							B	FLEXCOM4_IO5	O	2	
							C	GTSUCOMP	O	1	
G16	VDDIOP2	GPIO	PB0	I/O	WKUP5	–	A	GRX2	I	1	PIO, I, PU, ST
							B	FLEXCOM2_IO4	O	1	
							C	GRXER	I	1	
L15	VDDIOP2	GPIO	PB1	I/O	–	–	A	GRX3	I	1	PIO, I, PU, ST
							B	FLEXCOM2_IO3	I/O	1	

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Table 9-1. Ball Description (continued)

BGA243 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State(1)
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
H16	VDDIOP2	GPIO	PB2	I/O	–	–	A	G125CK	I	1	PIO, I, PU, ST
							B	FLEXCOM2_IO2	I/O	1	
R8	VDDIOP2	GPIO	PB3	I/O	WKUP6	–	A	GCRSDV/GRXCTL	I	1	PIO, I, PU, ST
							B	FLEXCOM4_IO6	O	1	
J16	VDDIOP2	GPIO	PB4	I/O	–	–	A	GTX2	O	1	PIO, I, PU, ST
							B	FLEXCOM8_IO0	I/O	1	
N15	VDDIOP2	GPIO	PB5	I/O	–	–	A	GTX3	O	1	PIO, I, PU, ST
							B	FLEXCOM8_IO1	I/O	1	
F16	VDDIOP2	GPIO	PB6	I/O	–	–	A	GTXCK/GREFCK	I/O	1	PIO, I, PU, ST
							B	FLEXCOM0_IO7	I	1	
R13	VDDIOP2	GPIO	PB7	I/O	–	–	A	GTXEN/GTXCTL	O	1	PIO, I, PU, ST
							C	FLEXCOM6_IO2	I/O	1	
D17	VDDIOP2	GPIO	PB8	I/O	–	–	A	GRXCK	I	1	PIO, I, PU, ST
							C	FLEXCOM6_IO3	I/O	1	
R14	VDDIOP2	GPIO	PB9	I/O	–	–	A	GMDIO	I/O	1	PIO, I, PU, ST
							B	PCK1	O	1	
							C	FLEXCOM6_IO4	O	1	
K16	VDDIOP2	GPIO	PB10	I/O	–	–	A	GMDC	O	1	PIO, I, PU, ST
							B	PCK0	O	1	
							C	FLEXCOM8_IO2	I/O	1	
T8	VDDIOP2	GPIO	PB11	I/O	–	–	A	GRX0	I	1	PIO, I, PU, ST
							B	PWM0	O	2	
							C	FLEXCOM8_IO3	I/O	1	
L16	VDDIOP2	GPIO	PB12	I/O	–	–	A	GRX1	I	1	PIO, I, PU, ST
							B	PWM1	O	2	
							C	FLEXCOM8_IO4	O	1	
N16	VDDIOP2	GPIO	PB13	I/O	–	–	A	GTX0	O	1	PIO, I, PU, ST
							B	PWM2	O	2	
E17	VDDIOP2	GPIO	PB14	I/O	–	–	A	GTX1	O	1	PIO, I, PU, ST
							B	PWM3	O	2	
C7	VDDQSPI	GPIO	PB15	I/O	–	–	A	QIO5	I/O	1	PIO, I, PU, ST
							C	FLEXCOM11_IO0	I/O	1	
							D	I2SMCC_WS	I/O	1	
A11	VDDQSPI	GPIO	PB16	I/O	–	–	A	QIO6	I/O	1	PIO, I, PU, ST
							C	FLEXCOM11_IO1	I/O	1	
							D	I2SMCC_DIN0	I	1	

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Table 9-1. Ball Description (continued)

BGA243 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State(1)
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
A10	VDDQSPI	GPIO	PB17	I/O	–	–	A	QIO7	I/O	1	PIO, I, PU, ST
							C	FLEXCOM12_IO0	I/O	1	
							D	I2SMCC_DOUT0	O	1	
C10	VDDQSPI	GPIO	PB18	I/O	WKUP7	–	A	QDQS	I	1	PIO, I, PU, ST
							B	ADTRG	I	1	
							C	FLEXCOM12_IO1	I/O	1	
							D	IRQ	I	1	
A9	VDDQSPI	GPIO	PB19	I/O	–	–	A	QSCK	O	1	PIO, I, PU, ST
							C	FLEXCOM12_IO2	I/O	1	
B11	VDDQSPI	GPIO	PB20	I/O	–	–	A	QCS	O	1	PIO, I, PU, ST
							C	FLEXCOM12_IO3	I/O	1	
B9	VDDQSPI	GPIO	PB21	I/O	–	–	A	QIO0	I/O	1	PIO, I, PU, ST
							C	FLEXCOM12_IO4	O	1	
D10	VDDQSPI	GPIO	PB22	I/O	–	–	A	QIO1	I/O	1	PIO, I, PU, ST
							C	FLEXCOM9_IO2	I/O	1	
C8	VDDQSPI	GPIO	PB23	I/O	–	–	A	QIO2	I/O	1	PIO, I, PU, ST
							C	FLEXCOM9_IO3	I/O	1	
B10	VDDQSPI	GPIO	PB24	I/O	–	–	A	QIO3	I/O	1	PIO, I, PU, ST
							C	FLEXCOM9_IO4	O	1	
D8	VDDQSPI	GPIO	PB25	I/O	WKUP8	–	A	QINT	I	1	PIO, I, PU, ST
							D	I2SMCC_MCK	O	1	
C11	VDDQSPI	GPIO	PB26	I/O	–	–	A	QIO4	I/O	1	PIO, I, PU, ST
							D	I2SMCC_CK	I/O	1	
G2	VDDIOP1	GPIO	PC0	I/O	–	–	A	LCDC_DAT0	O	1	PIO, I, PU, ST
							B	ISC_D0	I	1	
							C	FLEXCOM7_IO0	I/O	1	
H4	VDDIOP1	GPIO	PC1	I/O	–	–	A	LCDC_DAT1	O	1	PIO, I, PU, ST
							B	ISC_D1	I	1	
							C	FLEXCOM7_IO1	I/O	1	
A3	VDDLVDS	GPIO	PC2	I/O	LVDS_A0M	–	A	LCDC_DAT2	O	1	PIO, I, PU, ST
							B	ISC_D2	I	1	
							C	TIOA3	I/O	1	
B3	VDDLVDS	GPIO	PC3	I/O	LVDS_A0P	–	A	LCDC_DAT3	O	1	PIO, I, PU, ST
							B	ISC_D3	I	1	
							C	TIOB3	I/O	1	
A4	VDDLVDS	GPIO	PC4	I/O	LVDS_A1M	–	A	LCDC_DAT4	O	1	PIO, I, PU, ST
							B	ISC_D4	I	1	
							C	TCLK3	I	1	

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Table 9-1. Ball Description (continued)

BGA243 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State(1)
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
B4	VDDLVDS	GPIO	PC5	I/O	LVDS_A1P	–	A	LCDC_DAT5	O	1	PIO, I, PU, ST
							B	ISC_D5	I	1	
							C	TIOA4	I/O	1	
A5	VDDLVDS	GPIO	PC6	I/O	LVDS_A2M	–	A	LCDC_DAT6	O	1	PIO, I, PU, ST
							B	ISC_D6	I	1	
							C	TIOB4	I/O	1	
B5	VDDLVDS	GPIO	PC7	I/O	LVDS_A2P	–	A	LCDC_DAT7	O	1	PIO, I, PU, ST
							B	ISC_D7	I	1	
							C	TCLK4	I	1	
G1	VDDIOP1	GPIO	PC8	I/O	–	–	A	LCDC_DAT8	O	1	PIO, I, PU, ST
							B	ISC_D8	I	1	
							C	FLEXCOM9_IO0	I/O	1	
H3	VDDIOP1	GPIO	PC9	I/O	–	–	A	LCDC_DAT9	O	1	PIO, I, PU, ST
							B	ISC_D9	I	1	
							C	FLEXCOM9_IO1	I/O	1	
A7	VDDLVDS	GPIO	PC10	I/O	LVDS_CLK1M	–	A	LCDC_DAT10	O	1	PIO, I, PU, ST
							B	ISC_D10	I	1	
							C	PWM0	O	3	
B7	VDDLVDS	GPIO	PC11	I/O	LVDS_CLK1P	–	A	LCDC_DAT11	O	1	PIO, I, PU, ST
							B	ISC_D11	I	1	
							C	PWM1	O	3	
A8	VDDLVDS	GPIO	PC12	I/O	LVDS_A3M	–	A	LCDC_DAT12	O	1	PIO, I, PU, ST
							B	ISC_PCK	I	1	
							C	TIOA5	I/O	1	
B8	VDDLVDS	GPIO	PC13	I/O	LVDS_A3P	–	A	LCDC_DAT13	O	1	PIO, I, PU, ST
							B	ISC_VSYNC	I	1	
							C	TIOB5	I/O	1	
F2	VDDIOP1	GPIO	PC14	I/O	–	–	A	LCDC_DAT14	O	1	PIO, I, PU, ST
							B	ISC_HSYNC	I	1	
							C	TCLK5	I	1	
E3	VDDIOP1	GPIO	PC15	I/O	–	–	A	LCDC_DAT15	O	1	PIO, I, PU, ST
							B	ISC_MCK	O	1	
							C	PCK0	O	2	
E1	VDDIOP1	GPIO	PC16	I/O	–	–	A	LCDC_DAT16	O	1	PIO, I, PU, ST
							B	ISC_FIELD	I	1	
							C	FLEXCOM10_IO0	I/O	1	

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Table 9-1. Ball Description (continued)

BGA243 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State(1)
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
G4	VDDIOP1	GPIO	PC17	I/O	–	–	A	LCDC_DAT17	O	1	PIO, I, PU, ST
							B	FLEXCOM1_IO7	I	1	
							C	FLEXCOM10_IO1	I/O	1	
E2	VDDIOP1	GPIO	PC18	I/O	–	–	A	LCDC_DAT18	O	1	PIO, I, PU, ST
							B	FLEXCOM10_IO2	I/O	1	
							C	PWM0	O	1	
G3	VDDIOP1	GPIO	PC19	I/O	–	–	A	LCDC_DAT19	O	1	PIO, I, PU, ST
							B	FLEXCOM10_IO3	I/O	1	
							C	PWM1	O	1	
D1	VDDIOP1	GPIO	PC20	I/O	–	–	A	LCDC_DAT20	O	1	PIO, I, PU, ST
							B	FLEXCOM10_IO4	O	1	
							C	PWM2	O	1	
D3	VDDIOP1	GPIO	PC21	I/O	–	–	A	LCDC_DAT21	O	1	PIO, I, PU, ST
							C	PWM3	O	1	
D2	VDDIOP1	GPIO	PC22	I/O	–	–	A	LCDC_DAT22	O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO0	I/O	1	
E4	VDDIOP1	GPIO	PC23	I/O	WKUP9	–	A	LCDC_DAT23	O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO1	I/O	1	
C1	VDDIOP1	GPIO	PC24	I/O	WKUP10	–	A	LCDC_DISP	O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO4	O	1	
C4	VDDIOP1	GPIO	PC25	I/O	WKUP12	–	A	NTRST	I	1	NRST_OUT, O, PD
							B	FLEXCOM3_IO3	I/O	1	
							C	NRST_OUT	O	1	
C2	VDDIOP1	GPIO	PC26	I/O	WKUP13	–	A	LCDC_PWM	O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO2	I/O	1	
C5	VDDIOP1	GPIO	PC27	I/O	–	–	A	LCDC_VSYNC	O	1	PIO, I, PU, ST
							C	FLEXCOM1_IO4	O	1	
B1	VDDIOP1	GPIO	PC28	I/O	–	–	A	LCDC_HSYNC	O	1	PIO, I, PU, ST
							C	FLEXCOM1_IO3	I/O	1	
D5	VDDIOP1	GPIO	PC29	I/O	–	–	A	LCDC_DEN	O	1	PIO, I, PU, ST
							C	FLEXCOM1_IO2	I/O	1	
A2	VDDIOP1	GPIO	PC30	I/O	–	–	A	LCDC_PCK	O	1	PIO, I, PU, ST
							C	FLEXCOM3_IO7	I	1	
D7	VDDIOP1	GPIO	PC31	I/O	WKUP11	–	A	FIQ	I	1	PIO, I, PU, ST
							C	PCK1	O	2	
N11	VDDNF	GPIO	PD0	I/O	–	–	A	NANDOE	O	1	PIO, I, PU
							C	FLEXCOM7_IO2	I/O	1	

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Table 9-1. Ball Description (continued)

BGA243 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State(1)
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
H14	VDDNF	GPIO	PD1	I/O	–	–	A	NANDWE	O	1	PIO, I, PU
							C	FLEXCOM7_IO3	I/O	1	
P11	VDDNF	GPIO	PD2	I/O	–	–	A	NANDALE	O	1	A21,O, PD
							C	FLEXCOM7_IO4	O	1	
G15	VDDNF	GPIO	PD3	I/O	–	–	A	NANDCLE	O	1	A22,O, PD
							C	FLEXCOM11_IO2	I/O	1	
P10	VDDNF	GPIO	PD4	I/O	–	–	A	NANDCS	O	1	PIO, I, PU
							C	FLEXCOM11_IO3	I/O	1	
C17	VDDNF	GPIO	PD5	I/O	–	–	C	FLEXCOM11_IO4	O	1	PIO, I, PU
P13	VDDNF	GPIO	PD6	I/O	–	–	A	NANDDAT0	I/O	1	PIO, I, PU
P15	VDDNF	GPIO	PD7	I/O	–	–	A	NANDDAT1	I/O	1	PIO, I, PU
H15	VDDNF	GPIO	PD8	I/O	–	–	A	NANDDAT2	I/O	1	PIO, I, PU
R11	VDDNF	GPIO	PD9	I/O	–	–	A	NANDDAT3	I/O	1	PIO, I, PU
D16	VDDNF	GPIO	PD10	I/O	–	–	A	NANDDAT4	I/O	1	PIO, I, PU
N14	VDDNF	GPIO	PD11	I/O	–	–	A	NANDDAT5	I/O	1	PIO, I, PU
K15	VDDNF	GPIO	PD12	I/O	–	–	A	NANDDAT6	I/O	1	PIO, I, PU
P8	VDDNF	GPIO	PD13	I/O	–	–	A	NANDDAT7	I/O	1	PIO, I, PU
E16	VDDNF	GPIO	PD14	I/O	–	–	A	NANDRDY	I	1	PIO, I, PU
A1	GND	Ground	GND	I	–	–	–	–	–	–	–
A13	GND	Ground	GND	I	–	–	–	–	–	–	–
A14	GND	Ground	GND	I	–	–	–	–	–	–	–
A15	GND	Ground	GND	I	–	–	–	–	–	–	–
A17	GND	Ground	GND	I	–	–	–	–	–	–	–
B2	GND	Ground	GND	I	–	–	–	–	–	–	–
B13	GND	Ground	GND	I	–	–	–	–	–	–	–
B14	GND	Ground	GND	I	–	–	–	–	–	–	–
B16	GND	Ground	GND	I	–	–	–	–	–	–	–
C3	GND	Ground	GND	I	–	–	–	–	–	–	–
C9	GND	Ground	GND	I	–	–	–	–	–	–	–
C12	GND	Ground	GND	I	–	–	–	–	–	–	–
C13	GND	Ground	GND	I	–	–	–	–	–	–	–
C15	GND	Ground	GND	I	–	–	–	–	–	–	–
D4	GND	Ground	GND	I	–	–	–	–	–	–	–
D6	GND	Ground	GND	I	–	–	–	–	–	–	–
D12	GND	Ground	GND	I	–	–	–	–	–	–	–
D14	GND	Ground	GND	I	–	–	–	–	–	–	–
E6	GND	Ground	GND	I	–	–	–	–	–	–	–
E13	GND	Ground	GND	I	–	–	–	–	–	–	–

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Table 9-1. Ball Description (continued)

BGA243 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State(1)
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
E14	GND	Ground	GND	I	–	–	–	–	–	–	–
F4	GND	Ground	GND	I	–	–	–	–	–	–	–
F5	GND	Ground	GND	I	–	–	–	–	–	–	–
F6	GND	Ground	GND	I	–	–	–	–	–	–	–
F11	GND	Ground	GND	I	–	–	–	–	–	–	–
F12	GND	Ground	GND	I	–	–	–	–	–	–	–
F14	GND	Ground	GND	I	–	–	–	–	–	–	–
G5	GND	Ground	GND	I	–	–	–	–	–	–	–
G12	GND	Ground	GND	I	–	–	–	–	–	–	–
H8	GND	Ground	GND	I	–	–	–	–	–	–	–
H9	GND	Ground	GND	I	–	–	–	–	–	–	–
H10	GND	Ground	GND	I	–	–	–	–	–	–	–
J4	GND	Ground	GND	I	–	–	–	–	–	–	–
J8	GND	Ground	GND	I	–	–	–	–	–	–	–
J9	GND	Ground	GND	I	–	–	–	–	–	–	–
J10	GND	Ground	GND	I	–	–	–	–	–	–	–
J14	GND	Ground	GND	I	–	–	–	–	–	–	–
K9	GND	Ground	GND	I	–	–	–	–	–	–	–
K10	GND	Ground	GND	I	–	–	–	–	–	–	–
K13	GND	Ground	GND	I	–	–	–	–	–	–	–
L12	GND	Ground	GND	I	–	–	–	–	–	–	–
M3	GND	Ground	GND	I	–	–	–	–	–	–	–
M6	GND	Ground	GND	I	–	–	–	–	–	–	–
M12	GND	Ground	GND	I	–	–	–	–	–	–	–
M13	GND	Ground	GND	I	–	–	–	–	–	–	–
M14	GND	Ground	GND	I	–	–	–	–	–	–	–
N6	GND	Ground	GND	I	–	–	–	–	–	–	–
N7	GND	Ground	GND	I	–	–	–	–	–	–	–
N12	GND	Ground	GND	I	–	–	–	–	–	–	–
N13	GND	Ground	GND	I	–	–	–	–	–	–	–
P4	GND	Ground	GND	I	–	–	–	–	–	–	–
P12	GND	Ground	GND	I	–	–	–	–	–	–	–
P14	GND	Ground	GND	I	–	–	–	–	–	–	–
R3	GND	Ground	GND	I	–	–	–	–	–	–	–
R7	GND	Ground	GND	I	–	–	–	–	–	–	–
R10	GND	Ground	GND	I	–	–	–	–	–	–	–
R15	GND	Ground	GND	I	–	–	–	–	–	–	–
T16	GND	Ground	GND	I	–	–	–	–	–	–	–

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Table 9-1. Ball Description (continued)

BGA243 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State(1)
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
U1	GND	Ground	GND	I	–	–	–	–	–	–	–
U17	GND	Ground	GND	I	–	–	–	–	–	–	–
J15	VDDIOM	Power	VDDIOM	I	–	–	–	–	–	–	–
K8	VDDIOM	Power	VDDIOM	I	–	–	–	–	–	–	–
K14	VDDIOM	Power	VDDIOM	I	–	–	–	–	–	–	–
P7	VDDIOM	Power	VDDIOM	I	–	–	–	–	–	–	–
M15	VDDNF	Power	VDDNF	I	–	–	–	–	–	–	–
R9	VDDIOP0	Power	VDDIOP0	I	–	–	–	–	–	–	–
C6	VDDIOP1	Power	VDDIOP1	I	–	–	–	–	–	–	–
R12	VDDIOP2	Power	VDDIOP2	I	–	–	–	–	–	–	–
T2	VDDBU	Power	VDDBU	I	–	–	–	–	–	–	–
R6	VDDANA	Power	VDDANA	I	–	–	–	–	–	–	–
P6	GNDANA	Ground	GNDANA	I	–	–	–	–	–	–	–
E5	VDDIN25	Power	VDDIN25	I	–	–	–	–	–	–	–
M1	VDDOUT25	Power	VDDOUT25	I	–	–	–	–	–	–	–
J3	VDDIN33	Power	VDDIN33	I	–	–	–	–	–	–	–
M4	VDDIN33	Power	VDDIN33	I	–	–	–	–	–	–	–
F7	VDDCORE	Power	VDDCORE	I	–	–	–	–	–	–	–
G6	VDDCORE	Power	VDDCORE	I	–	–	–	–	–	–	–
L6	VDDCORE	Power	VDDCORE	I	–	–	–	–	–	–	–
M2	VDDCORE	Power	VDDCORE	I	–	–	–	–	–	–	–
M7	VDDCORE	Power	VDDCORE	I	–	–	–	–	–	–	–
M11	VDDCORE	Power	VDDCORE	I	–	–	–	–	–	–	–
N5	VDDCORE	Power	VDDCORE	I	–	–	–	–	–	–	–
E7	VDDQSPI	Power	VDDQSPI	I	–	–	–	–	–	–	–
F3	VDDMIPI	Power	VDDMIPI	I	–	–	–	–	–	–	–
D9	VDDLVDS	Power	VDDLVDS	I	–	–	–	–	–	–	–
E15	VDDIOM	Analog	DDR_VREF	I	–	–	–	–	–	–	–
D11	VDDIOM	Analog	DDR_CAL	I	–	–	–	–	–	–	–
H13	DDRM_VDD	Analog	DDRM_ZQ	I	–	–	–	–	–	–	–
A16	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
B15	DDRM_VDD	Power	DDRM_VDD		–	–	–	–	–	–	–
B17	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
C14	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
C16	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
D13	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
D15	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
E11	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–

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Table 9-1. Ball Description (continued)

BGA243 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State[1]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
E12	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
F13	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
F15	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
F17	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
G13	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
G14	DDRM_VDD	Power	DDRM_VDD	I	–	–	–	–	–	–	–
U3	VDDANA	GPIO	ADVREFP	–	–	–	–	–	–	–	I
U2	VDDANA	GPIO	ADVREFN	–	–	–	–	–	–	–	I
K5	VDDIN33	USBHS	HHSRTUNE	–	–	–	–	–	–	–	I
P1	VDDIN33	USBHS	HHSDPA	–	DHSDP	–	–	–	–	–	O, PD
P2	VDDIN33	USBHS	HHSDMA	–	DHSDM	–	–	–	–	–	O, PD
N1	VDDIN33	USBHS	HHSDPB	–	–	–	–	–	–	–	O, PD
N2	VDDIN33	USBHS	HHSDMB	–	–	–	–	–	–	–	O, PD
N3	VDDIN33	USBHS	HHSDPC	–	–	–	–	–	–	–	O, PD
P3	VDDIN33	USBHS	HHSDMC	–	–	–	–	–	–	–	O, PD
T14	VDDBU	GPIO	WKUP0	–	–	–	–	–	–	–	I, ST
U14	VDDBU	GPIO	SHDN	–	–	–	–	–	–	–	O, PD
U16	VDDBU	GPIO	JTAGSEL	–	–	–	–	–	–	–	I, PD
P9	VDDBU	GPIO	TST	–	–	–	–	–	–	–	I, PD, ST
U13	VDDIOP0	GPIO	TCK	–	–	–	–	–	–	–	I, ST
T13	VDDIOP0	GPIO	TDI	–	–	–	–	–	–	–	I, ST
T17	VDDIOP0	GPIO	TDO	–	–	–	–	–	–	–	O
U15	VDDIOP0	GPIO	TMS	–	–	–	–	–	–	–	I, ST
T15	VDDIOP0	GPIO	RTCK	–	–	–	–	–	–	–	O
P5	VDDIOP0	GPIO	NRST	–	–	–	–	–	–	–	I, PU, ST
U5	VDDBU	CLOCK	XIN32	–	–	–	–	–	–	–	I
U4	VDDBU	CLOCK	XOUT32	–	–	–	–	–	–	–	O
L1	VDDIN33	CLOCK	XIN	–	–	–	–	–	–	–	I
L2	VDDIN33	CLOCK	XOUT	–	–	–	–	–	–	–	O
H1	VDDMIPI	Analog	MIPI_DN0	I/O	–	–	–	–	–	–	HiZ
H2	VDDMIPI	Analog	MIPI_DP0	I/O	–	–	–	–	–	–	HiZ
J1	VDDMIPI	Analog	MIPI_DN1	I/O	–	–	–	–	–	–	HiZ
J2	VDDMIPI	Analog	MIPI_DP1	I/O	–	–	–	–	–	–	HiZ
K1	VDDMIPI	Analog	MIPI_DN2	I/O	–	–	–	–	–	–	HiZ
K2	VDDMIPI	Analog	MIPI_DP2	I/O	–	–	–	–	–	–	HiZ
L3	VDDMIPI	Analog	MIPI_DN3	I/O	–	–	–	–	–	–	HiZ
L4	VDDMIPI	Analog	MIPI_DP3	I/O	–	–	–	–	–	–	HiZ
K3	VDDMIPI	Analog	MIPI_CLKN	O	–	–	–	–	–	–	HiZ

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Table 9-1. Ball Description (continued)

BGA243 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State[1]
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	
K4	VDDMIPI	Analog	MIPI_CLKP	O	–	–	–	–	–	–	HiZ
H5	VDDMIPI	Analog	MIPI_REXT	I	–	–	–	–	–	–	I
M5	VDDANA	GPIO	AUDIO_CLK	–	–	–	–	–	–	–	O

Note:

1. HiZ = High impedance; PIO = GPIO; PD = Pull–Down; PU = Pull–Up, ST = Schmitt Trigger

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10. Electrical Characteristics

Electrical characteristics, schematics, procedures and recommendations are the same as those given in the SAM9X7 Series data sheet (see Reference Documents).

- The VDDQ and VDD power inputs described in the DDR2 SDRAM and DDR3L SDRAM data sheets are connected to the SAM9X75 SiP balls called “DDRM_VDD”. Therefore, the requirements placed on VDDQ and VDD power inputs in the “Absolute Maximum Ratings” and “Recommended DC Operating Conditions” sections of these data sheets apply to the DDRM_VDD power inputs.
- The VDDIN25 input powers the LVDS PLL of the device. It must be connected to VDDOUT25 on the PCB. From an Absolute Maximum Ratings perspective, VDDIN25 has the same specification as VDDLVDS.

10.1. Recommended Thermal Operating Conditions

Table 10-1. Recommended Thermal Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
T_A	Ambient temperature range	SAM9X75D5M(T)-V devices	-40	105	°C
		SAM9X75D5M(T)-I devices		85	°C
		SAM9X75D1G(T)-I devices			°C
		SAM9X75D2G(T)-I devices			°C
T_{J_MPU}	Junction temperature range	–		125	°C
T_{J_DDRx}		–			°C

Table 10-2. BGA243 Package Thermal Characteristics(1)(2)

Symbol	Parameter	Typ	Unit
R_{JC}	Junction-to-case thermal resistance	7	°C/W
R_{JB}	Junction-to-board thermal resistance	25	°C/W
$\Psi_{J\text{-}top}$	Junction-to-package-top characterization parameter	0.31	°C/W

Notes:

1. $R_{JA} = (T_{J_MPU} - T_A) / P_{TOT}$, where T_A is the ambient temperature and P_{TOT} is the power consumption of both the processor and the embedded DDR memory. The DDR SDRAM junction temperature is always lower than the MPU junction temperature.
2. The package characteristics in the above table are provided according to the JEDEC JESD51-2 standard with the 2s2p board and 0 m/s air flow. These values are not directly applicable to the final application. As per JEDEC standards, these parameters represent the device mounted on a specific PCB under controlled conditions. In real-world applications, the PCB design and construction, airflow, and other factors may significantly impact thermal characteristics.

10.2. Power Sequences

The DDR SDRAM power rail (DDRM_VDD) must be connected to VDDIOM on the PCB. Refer to the section “Recommended Power Supply Sequencing” in the SAM9X7 Series data sheet (see Reference Documents).

10.3. Device Power Consumption in Applicative Use Cases

Table 10-4 provides the processor power consumption in the following conditions:

- f_{CPU_CLK} = 800 MHz
- f_{MCK} = 266 MHz
- I & D caches are enabled.
- Use cases run on Linux®.

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- Current consumptions are measured as shown in Figure 10-1. Note that external component current consumptions are not counted.
- Ambient temperature: 25°C

The measurements are provided for typical SAM9X75D1G and SAM9X75D2G devices.

Figure 10-1. Current Measurement for Applicative Use Cases (DDR3L Example)

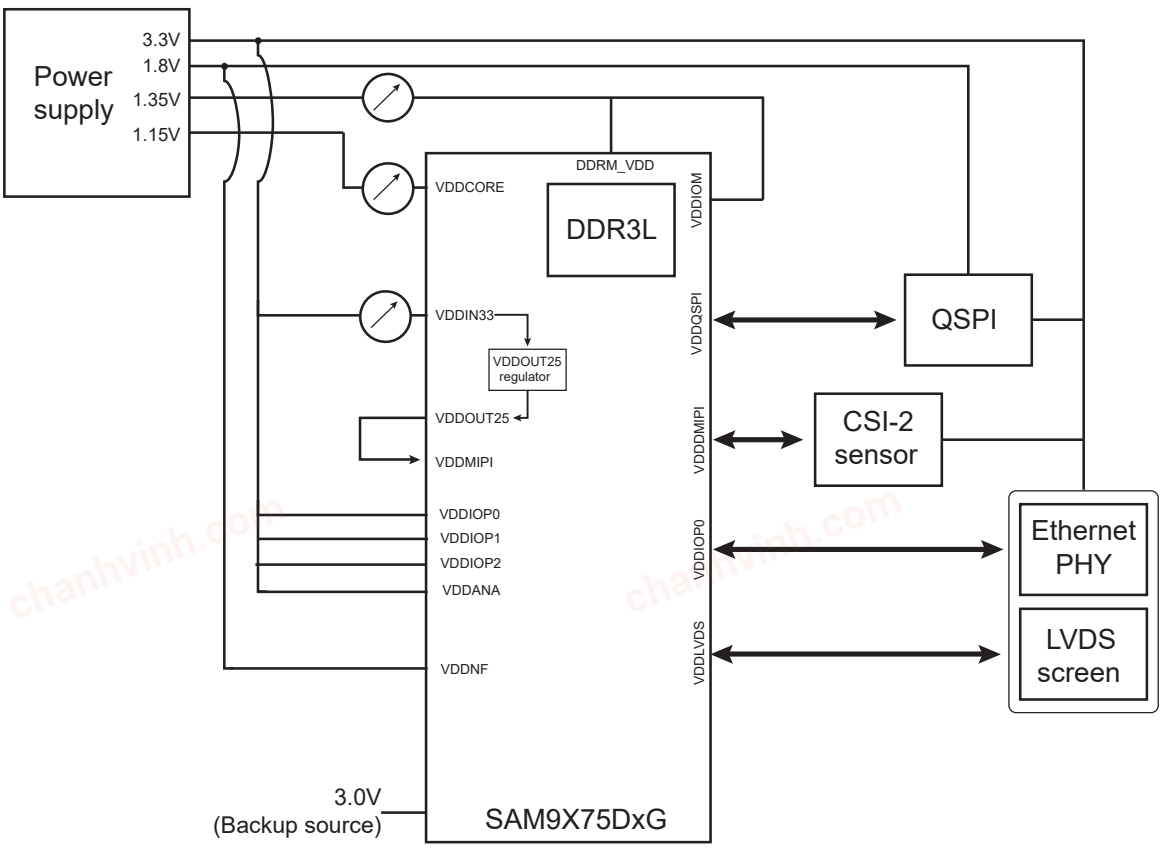


Table 10-3. Use Case Definition

Use Case	Description
1	After Linux boot root prompt
2	Running 2D graphics benchmark with EGT monitor (800x480 DSI panel @ 46 fps) - 22% CPU usage
3	Run Bonnie++ on USB mass storage
4	SAM9X75 running as iPerf server
5	Image sensor video recording with QVGA resolution - 10 fps

Table 10-4. Power Consumption (mW) in Applicative Use Cases

Use Case	VDDCORE 1.15V	VDDIOM+DDRM_VDD		VDDIN33 3.30V	Total (DDR3L)	Total (DDR2)
		1.35V	1.80V			
1	135	41	45	165	341	345
2	165	55	60	125	345	350
3	190	84	57	115	389	362
4	165	95	108	165	425	438
5	170	61	–	330	561	–

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10.4. SDRAM Power Consumption in Idle and Ultra-Low Power (ULP0, ULP1) Modes with SDRAM in Self-Refresh

For a complete description of how to enter and exit ULP0 or ULP1 mode, refer to the SAM9X7 Series data sheet (see Reference Documents).

Table 10-5. Typical Power Consumption in Idle, ULP0 or ULP1 Mode on VDDIOM and DDRM_VDD

VDDIOM DDRM_VDD	T_A= -40°C	T_A= 25°C	T_A= 50°C	T_A= 70°C	T_A= 85°C	T_A= 105°C	Unit
1.35V (DDR3L)	3.7	4.3	5.1	6.3	7.7	–	mW
1.8V (DDR2)	3.7	3.8	3.9	4.2	4.4	5.5	

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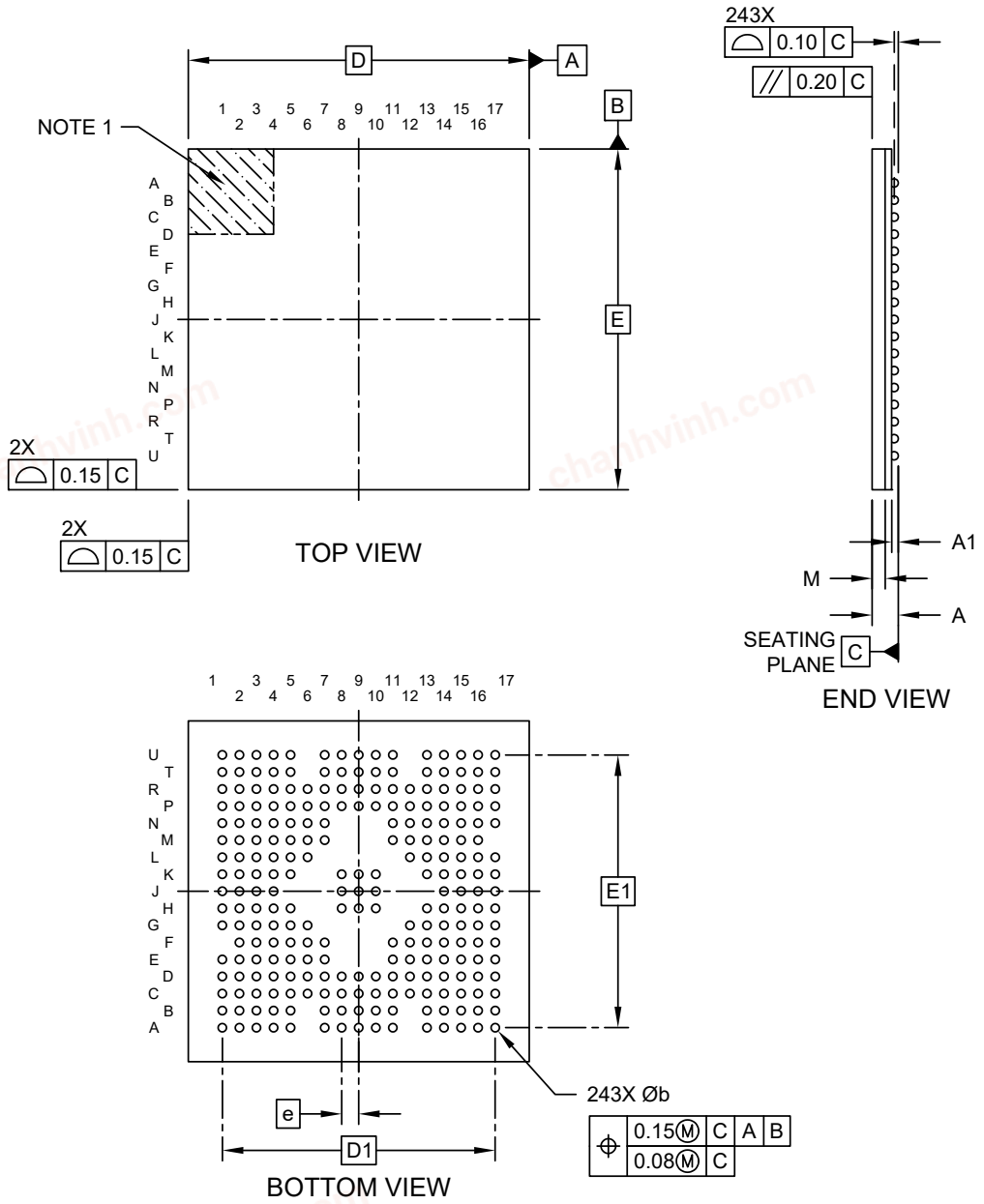
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11. Mechanical Characteristics

11.1. 243-Ball TFBGA Mechanical Characteristics

243-Ball Thin Fine-Pitch Ball Grid Array (4TB) - 16x16x1.23 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



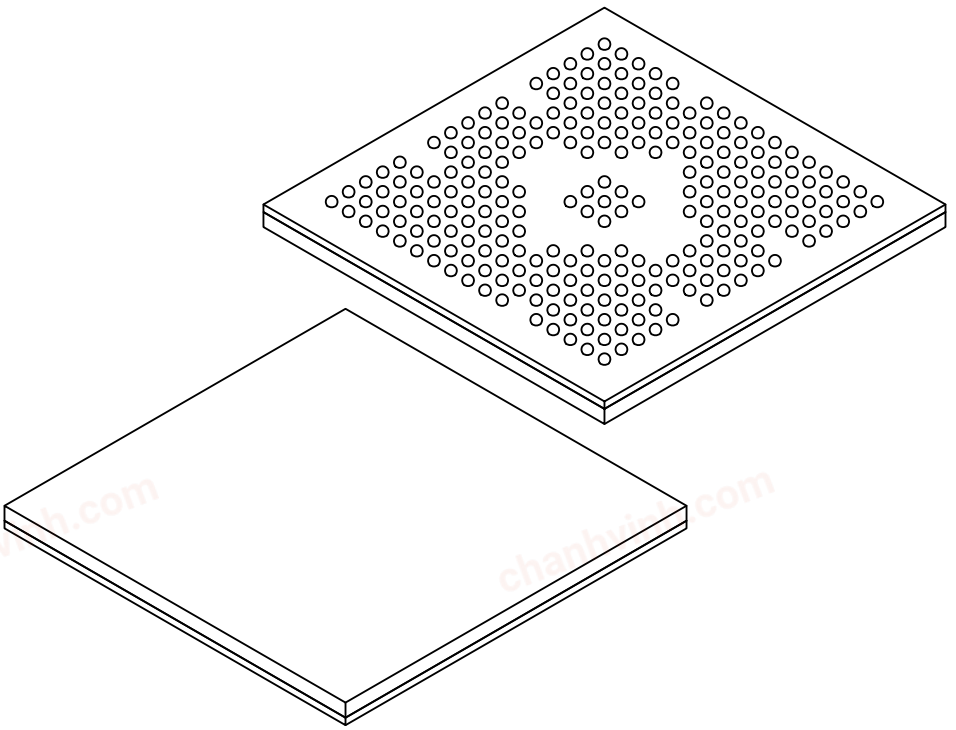
Microchip Technology Drawing C04-21556 Rev B Sheet 1 of 2

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243-Ball Thin Fine-Pitch Ball Grid Array (4TB) - 16x16x1.23 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		243	
Pitch	e		0.80 BSC	
Overall Height	A	–	–	1.23
Ball Height	A1	–	0.21	0.312
Mold Thickness	M	0.51	0.56	0.61
Overall Length	D		16.00 BSC	
Ball Array Length	D2		12.80 BSC	
Overall Width	E		16.00 BSC	
Ball Array Width	E2		12.80 BSC	
Ball Diameter	b	0.35	0.40	0.45

Notes:

1. Terminal A1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

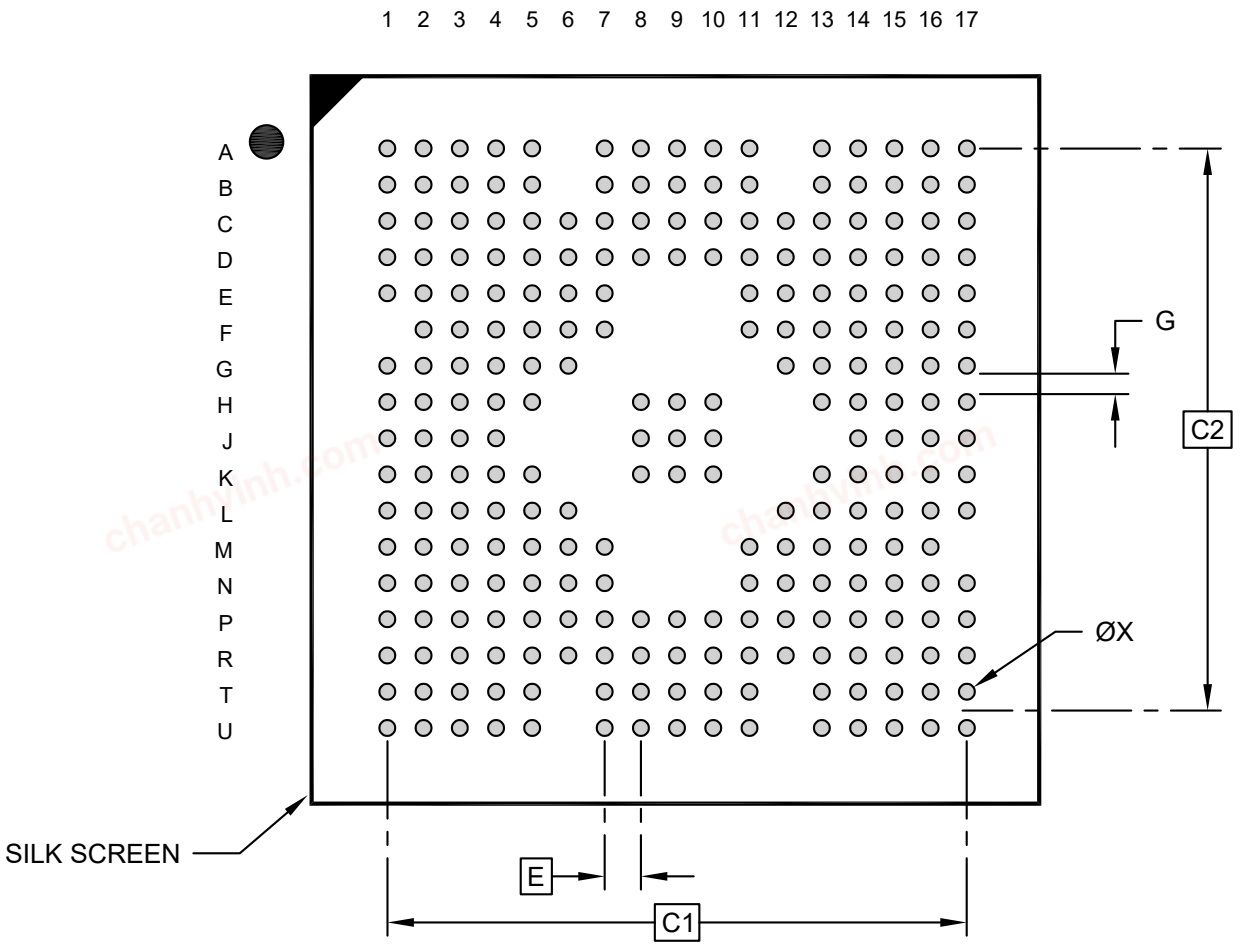
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243-Ball Thin Fine-Pitch Ball Grid Array (4TB) - 16x16x1.23 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		12.80 BSC	
Contact Pad Spacing	C2		12.80 BSC	
Contact Pad Width (X243)	X			0.35
Contact Pad to Contact Pad	G	0.45		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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Table 11-1. 243-ball TFBGA Package Characteristics

Moisture sensitivity level	MSL3

Table 11-2. Device and 243-ball TFBGA Package Weight

520	mg

Table 11-3. Package Reference

JEDEC drawing reference	NA
J-STD-609 classification	e8

Table 11-4. 243-ball TFBGA Package Information

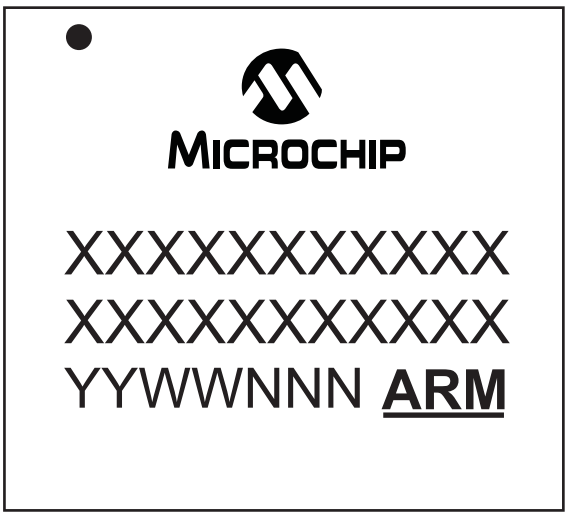
Ball land	0.450 mm
Nominal ball diameter	0.400 mm
Solder mask opening	0.350 mm
Solder mask definition	Solder Mask Defined (SMD)
Solder	SAC105

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12. Marking

Top marking follows the scheme below:



with possible values:

Line	Description	Values
1	Company logo	Microchip logo
2	Company name	Microchip
3	Device name	SAM9X75D5M SAM9X75D1G SAM9X75D2G
4	Temperature code/Packaging code, Jedec symbol	I/4TB e8 V/4TB e8
5	Lot traceability, Arm logo	YYWWNNN ARM

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13. Revision History

13.1. DS60001827D - 08/2025

Changes
Throughout: added content related to the Automotive variant SAM9X75D5M(T)-V/4TB(-SLx)VAO

13.2. DS60001827C - 12/2024

Changes
Throughout: added content related to the 512-Mbit device (SAM9X75D5M) Updated: • Reference Documents • Ordering Information • Product Identification System • Block Diagram • 243-Ball TFBGA Pinout figure • D11 and H13 information in Ball Description table • BGA243 Package Thermal Characteristics table • Typical Current Consumption in Idle, ULP0 or ULP1 Mode on VDDIOM and DDRM_VDD table

13.3. DS60001827B - 11/2023

Changes
Various updates, including in document title and Configuration Summary

13.4. DS60001827A - 09/2023

Changes
First issue.

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SAM9X75D1G, SAM9X75D2G, SAM9X75D5M

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