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SAM9X7 Series Silicon Errata and Data Sheet Clarifications

SAM9X7 Series

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Scope

The SAM9X7 Series device that you have received conforms functionally to the current SAM9X7 Series data sheet (DS60001813) or SAM9X75 System-in-Package (SiP) data sheet (DS60001827), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the device revision and device identification listed in the following table. The silicon issues are summarized in the Silicon Issue Summary section.

Data sheet clarifications and corrections (if applicable) are located in the Data Sheet Clarifications section.

The silicon device revisions and device IDs are shown in the following table.

Table 1. SAM9X7 Series Device Identification

Ordering Code	Device Revision	Device Identification DBGU_CIDR[31:0]
SAM9X70(T)-I/4PB	A0	0x89750030
SAM9X70(T)-V/4PB		
SAM9X72(T)-I/4PB		
SAM9X72(T)-V/4PB		
SAM9X75(T)-I/4PB		
SAM9X75(T)-V/4PB		
SAM9X75D1G(T)-I/4TB	A0-D1G	
SAM9X75D2G(T)-I/4TB	A0-D2G	
SAM9X70(T)-I/4PB	A1	0x89750031
SAM9X70(T)-V/4PB		
SAM9X70(T)-V/6GW		
SAM9X72(T)-I/4PB		
SAM9X72(T)-V/4PB		
SAM9X72(T)-V/6GW		
SAM9X75(T)-I/4PB		
SAM9X75(T)-V/4PB(VAO)		
SAM9X75(T)-V/6GW		
SAM9X75D5M(T)-I/4TB	A1-D5M	
SAM9X75D5M(T)-V/4TB(VAO)		
SAM9X75D1G(T)-I/4TB	A1-D1G	
SAM9X75D2G(T)-I/4TB	A1-D2G	

Note: Refer to the “Debug Unit (DBGU)” and “Product Identification System” sections in the current device data sheet for detailed information on chip identification for your specific device.

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1. Silicon Issue Summary

In this table and in subsequent sections, the following applies:

- "X" means the device revision is affected by the erratum.
- "–" means the device revision is not affected by the erratum.

Table 1-1. Silicon Issue Summary

Module	Erratum	Affected Device Revisions	
		A0 A0-D1G A0-D2G	A1 A1-D5M A1-D1G A1-D2G
ROM Code	The device does not boot on some QSPI memories	X	–
	Card Detect for SDMMC boot limited to PIOA pins	X	X
	Boot failure on e.MMC memories	X	X
LCDC	LCDC Register Write Protection status incorrect on some registers	X	X
PMC	PLL_INT Interrupt Enable has no effect	X	X
	Delay to first establish PCK	X	X
	PCK and GCLK Ready status issue	X	X
	Processor (CPU_CLK) and main system bus clock (MCK) source selection	X	X
RSTC	RSTC_SR.RSTTYP not showing GENERAL_RST	X	X
SMC	Register Write Protection not effective on SMC_OCMS register	X	X
AES	SPLIP mode does not work with some header sizes	X	X
QSPI	QSPI read with XDMA limited performance	X	X
MCAN	MCAN_TSU_TSCFG reset after read	X	X
	MCAN_TSU_TSS1 not reset after a MCAN_TSU_TSx read	X	X
	MCAN_TSU_ATB read resets the timebase value	X	X
	Debug message handling state machine not reset to Idle state when CCCR.INIT is set	X	X

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2. ROM Code

2.1. The device does not boot on some QSPI memories

A bug in the ROM code can prevent toggling some QSPI memory models in Quad SPI mode (1-4-4) before issuing a (1-4-4) fast read quad I/O command. As a result, booting is not possible using these memories.

Work Around

Use a memory with Quad mode enabled by default (for example, using an SST26VF064**BA** model instead of an SST26VF064**B** model).

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D1G A1-D2G A1-D5M						
X	–						

2.2. Card Detect for SDMMC boot limited to PIOA pins

A wrong PIO_ID bitfield decoding in ROM code limits the selection of the Card Detect pin (for SDMMC boot) to PIOA pins only. As a consequence, in the Boot Configuration Packet, the SDMMC MEM_CFGx[1] PIO_ID field must be filled as shown below to select the PIOA controller:

Value	Description
0	DNU
1	DNU
2	PIOA
3	DNU

Work Around

None

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D1G A1-D2G A1-D5M						
X	X						

2.3. Boot failure on e.MMC memories

The device fails to load a bootstrap program (boot.bin) from an e.MMC **USER** partition.

Work Around

- Always use the e.MMC **BOOT** partition to store the boot.bin file and enable the e.MMC **BOOT** partition feature, and
- Set the selected SDMMCx interface as boot media 1 and boot media 2 in the Boot Configuration Packet.

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Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D1G A1-D2G A1-D5M						
X	X						

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3. LCD Controller (LCDC)

3.1. LCDC Register Write Protection status incorrect on some registers

WPVS bit does not rise when a write protect violation occurs on the following registers:

LCDC_HEOVTAP10Px [x=0..15]

LCDC_HEOVTAP32Px [x=0..15]

LCDC_HEOHTAP10Px [x=0..15]

LCDC_HEOHTAP32Px [x=0..15]

Note the protection is effective even if the status bit does not rise.

Work Around

None

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D1G A1-D2G A1-D5M						
X	X						

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4. Power Management Controller (PMC)

4.1. PLL_INT Interrupt Enable has no effect

The PLL_INT interrupt bit in Interrupt Enable register PMC_IER has no effect.

Work Around

Use the LOCKx and UNLOCKx bits in PMC_PLL_IER, PMC_PLL_IDR, PMC_PLL_IMR and PMC_PLL_ISR0 to manage the interrupt behavior.

For example, to handle an interrupt event associated with the PLLA lock status:

1. Configure and enable the PMC interrupt as usual for all peripherals in the system.
2. Enable the interrupt source by setting PMC_PLL_IER.LOCKA.
3. When a PMC interrupt event raises, use the PMC_PLL_ISR0 and PMC_PLL_IMR registers to detect if LOCKA was the trigger.
4. Perform the required operations and manage the interrupt exit as usual, using PMC_PLL_IDR.LOCKA and the PMC interrupt system functions.

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D1G A1-D2G A1-D5M						
X	X						

4.2. Delay to first establish PCK

When enabling a PCK after a reset, the delay before establishing the PCK with the correct frequency is 255 cycles of the PCK source clock. Once this delay has elapsed, and as long as the core reset is not asserted, there is no more additional delay when disabling/enabling the PCK.

Work Around

None

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D1G A1-D2G A1-D5M						
X	X						

4.3. PCK and GCLK Ready status issue

The PCK and GCLK Ready signals are only affected by the enable/disable of the corresponding clock (PMC_SCER.PCKx, PMC_SCDR.PCKx or PMC_SR.GCLKEN).

A Ready signal at '1' does not imply the clock is correctly established with the required frequency, hence the Ready status is not affected by the modification of the source or the dividing ratio of the clock. This means that:

1. modifying PMC_PCKx.CSS or PMC_PCKx.PRES does not make PMC_SR.PCKRDYx fall,
2. modifying PMC_PCR.GCLKCSS or PMC_PCR.GCLKDIV does not make PMC_SR.GCLKRDY fall.

Work Around

None

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Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D1G A1-D2G A1-D5M						
X	X						

4.4. Processor (CPU_CLK) and main system bus clock (MCK) source selection

When changing the fields CSS or CPCSS in the CPU Clock register (PMC_CPU_CKR) from any PLL source clocks (PLLxCKx) to Slow Clock source (SLOW_CLK), the clock switching circuitry first switches from the PLL source to MAINCK source, then to Slow Clock source.

There is no impact on the clock switching sequence or device behavior. This intermediate step can be observed when the main system bus clock is output on a PCK pin.

Work Around

None

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D1G A1-D2G A1-D5M						
X	X						

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5. Reset Controller (RSTC)

5.1. RSTC_SR.RSTTYP not showing GENERAL_RST

In the Status register (RSTC_SR), the RSTTYP field shows BACKUP_RST instead of GENERAL_RST.

Work Around

None

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D1G A1-D2G A1-D5M						
X	X						

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6. Static Memory Controller (SMC)

6.1. Register write protection not effective on SMC_OCMS register

The register SMC_OCMS is not write-protected when the bit WPEN is set in SMC_WPMR.

Work Around

None

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D1G A1-D2G A1-D5M						
X	X						

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7. Advanced Encryption Standard (AES)

7.1. SPLIP mode does not work with some header sizes

The Secure Protocol Layers Improved Performances (SPLIP) mode does not work when the ESP header is not an integer multiple of 4 words.

Work Around

When the ESP header is not an integer multiple of 4 words, disable SPLIP mode to stop AES from automatically uploading the encrypted payload into SHA, and use the central DMA to feed SHA with the encrypted payload.

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D1G A1-D2G A1-D5M						
X	X						

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8. Quad Serial Peripheral Interface (QSPI)

8.1. QSPI read with XDMA limited performance

The bandwidth achievable in QSPI read when using the XDMA is limited due to burst accesses split into single accesses.

For example, in Quad mode at 100 MHz, the maximum achievable bandwidth is 19 MB/s instead of 46 MB/s.

Work Around

Use the CPU with MMU and caches enabled to reach 37 MB/s in the same conditions as above.

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D1G A1-D2G A1-D5M						
X	X						

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9. Controller Area Network (MCAN)

9.1. MCAN_TSU_TSCFG reset after read

When a write is issued to configure the TSU Timestamp Configuration register (MCAN_TSU_TSCFG), any attempt to read it resets the register content.

Work Around

Save the content of MCAN_TSU_TSCFG in memory to access the value without reading the register.

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D1G A1-D2G A1-D5M						
X	X						

9.2. MCAN_TSU_TSS1 not reset after a MCAN_TSU_TSx read

TSL[15:0] and TSN[15:0] in MCAN TSU Timestamp Status 1 (MCAN_TSU_TSS1) are not reset after reading a MCAN TSU Timestamp Status (MCAN_TSU_TSx) register.

Work Around

Proceed as follows:

1. Read MCAN_TSU_TSx.
2. For each bit set, read the corresponding MCAN_TSU_TSx and save the values.
3. Write the same MCAN_TSU_TSx register with value ‘0’ to reset the corresponding bit in MCAN_TSU_TSS1.

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D1G A1-D2G A1-D5M						
X	X						

9.3. MCAN_TSU_ATB read resets the timebase value

Each access to the Actual Timebase register (MCAN_TSU_ATB) resets the Timebase Prescaler MCAN_TSU_TSCFG.TBPRE.

Work Around

None

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D1G A1-D2G A1-D5M						
X	X						

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9.4. Debug message handling state machine not reset to Idle state when CCCR.INIT is set

Attention: This erratum is applicable for CAN 2.0.

In case MCAN_CCCR.INIT is set by the Host by writing to register MCAN_CCCR or when the CAN enters BusOff state, the debug message handling state machine stays in its current state instead of being reset to Idle state. Setting MCAN_CCCR.CCE does not change MCAN_RXF1S.DMS.

Work Around

In case the debug message handling state machine has stopped while MCAN_RXF1S.DMS="01" or MCAN_RXF1S.DMS="10", it can be reset to Idle state by a hardware reset or by reception of debug messages after MCAN_CCCR.INIT is reset to zero.

Affected Device Revisions

A0 A0-D1G A0-D2G	A1 A1-D1G A1-D2G A1-D5M						
X	X						

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10. Data Sheet Clarifications

There are no known data sheet clarifications as of this publication date.

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11. Revision History

11.1. DS80001082G - 08/2025

Extended scope to the SAM9X75D5M(T)-V/4TBVAO device

11.2. DS80001082F - 03/2025

- Throughout:
  - Extended scope to the following devices:
    - SAM9X70(T)-V/6GW
    - SAM9X72(T)-V/6GW
    - SAM9X75(T)-V/4PBVAO
  - Changed terminology from “silicon revision” to “device revision”
- Updated Note
- Added Boot failure on e.MMC memories

11.3. DS80001082E - 12/2024

Extended scope to the following devices:

- SAM9X75(T)-V/6GW
- SAM9X75D5M(T)-V/4TB
- SAM9X75D5M(T)-I/4TB

11.4. DS80001082D - 10/2024

Added A1 device revision information throughout

Added The device does not boot on some QSPI memories, Card Detect for SDMMC boot limited to PIOA pins, QSPI read with XDMA limited performance

Updated Data Sheet Clarifications

11.5. DS80001082C - 02/2024

Throughout: added references to SAM9X75 System-in-Package (SiP) devices.

Updated Table 1.

Added:

- SPLIP mode does not work with some header sizes
- Controller Area Network (MCAN)

Rephrased Processor (CPU_CLK) and main system bus clock (MCK) source selection

11.6. DS80001082B - 09/2023

Data Sheet Clarifications: added “Incorrect DDR3L calibration value in section “DDR3-SDRAM/DDR3L-SDRAM Initialization”

Power Management Controller (PMC): updated “Incorrect MCK intermediate state when switching clocks”

11.7. DS80001082A - 03/2023

First issue

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