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PIC32MX1XX/2XX/5XX 64/100-PIN

PIC32MX1XX/2XX/5XX 64/100-pin Family Silicon Errata and Data Sheet Clarification

The PIC32MX1XX/2XX/5XX 64/100-pin family of devices that you have received conform functionally to the current Device Data Sheet (DS20006624A**C**), except for the anomalies described in this document.

The errata described in this document will be addressed in future revisions of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices.

Note: The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1 and Table 2. The last column of each table represents the latest silicon revision for the devices listed. If applicable, the silicon issues are summarized in Table 3.

Data Sheet clarifications and corrections, if applicable, start on page 10.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. Select *Window > Dashboard*, and then click the **Refresh Debug Tool Status** icon ( ).
5. The part number and the Device and Revision ID values appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various PIC32MX1XX/2XX/5XX 64/100-pin family silicon revisions are shown in Table 1 and Table 2.

TABLE 1: SILICON DEVREV VALUES FOR DEVICES WITH 256 KB OR 512 KB OF FLASH MEMORY

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)	
		A0	B0
PIC32MX150F256H	0x06A10053	0x0	0x3
PIC32MX150F256L	0x06A11053		
PIC32MX170F512H	0x06A30053		
PIC32MX170F512L	0x06A31053		
PIC32MX250F256H	0x06A12053		
PIC32MX250F256L	0x06A13053		
PIC32MX270F512H	0x06A32053		
PIC32MX270F512L	0x06A33053		
PIC32MX550F256H	0x06A14053		
PIC32MX550F256L	0x06A15053		
PIC32MX570F512H	0x06A34053		
PIC32MX570F512L	0x06A35053		

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS20006624A**C**) for detailed information on Device and Revision IDs for your specific device.

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TABLE 2: SILICON DEVREV VALUES FOR DEVICES WITH 64 KB OR 128 KB OF FLASH MEMORY

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)			
		A0	A2	B0	B1
PIC32MX120F064H	0x06A50053	0x0	0x2	0x3	0x4
PIC32MX130F128H	0x06A00053				
PIC32MX130F128L	0x06A01053				
PIC32MX230F128H	0x06A02053				
PIC32MX230F128L	0x06A03053				
PIC32MX530F128H	0x06A04053				
PIC32MX530F128L	0x06A05053				

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS20006624A**C**) for detailed information on Device and Revision IDs for your specific device.

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TABLE 3: SILICON ISSUE SUMMARY

Module	Feature	Item	Issue Summary	Device Flash Memory (KB)	Affected Revisions			
					A0	A2	B0	B1
ADC Reference: ADC006-14	Differential Nonlinearity	1.	The ADC module is not within the published data sheet specification when operating at a conversion rate above 500 ksps.	64/128	X	X	X	X
				256/512	X	—	X	—
Clock Reference: DSCAPP-3890	Clock Out	2.	A clock signal is present on the CLKO pin, regardless of the clock source and setting of the CLKO Enable Configuration bit, during a Power-on Reset (POR) condition.	64/128	X	X	X	X
				256/512	X	—	X	—
JTAG Reference: CHIP002-409	Boundary Scan	3.	Boundary scan in not supported.	64/128	X	X	X	X
				256/512	X	—	X	—
Watchdog Timer Reference: DSCAPP-4218	Windowed Watchdog	4.	Clearing the Watchdog Timer inside the window when in Window mode may cause a reset.	64/128	X	X	X	X
				256/512	X	—	X	—
USB Reference: DSCAPP-3630	Idle Interrupt	5.	USB Idle interrupts cease if the IDLEIF flag is cleared and the bus is left idle for more than 3 ms.	64/128	X	X	X	X
				256/512	X	—	X	—
UART Reference: DSCAPP-4666	Receive Overflow	6.	A receive FIFO overflow condition causes the shift register to stop receiving data and lose synchronization with the serial data stream.	64/128	X	X	X	X
				256/512	X	—	X	—
Comparator Voltage Reference Reference: Not Listed	—	7.	Some operational mode combinations of the Comparator Voltage Reference do not meet the data sheet specifications.	64/128	X	X	X	X
				256/512	X	—	X	—
Comparator Voltage Reference Reference: DSCAPP-4382	—	8.	The Comparator Voltage Reference always behaves as if the CVRR bit is = 1, which specifies a range of 0 to 0.67 CV_{RSRC} with a CV_{RSRC}/24 step size.	64/128	X	X	X	X
				256/512	X	—	X	—
CTMU Reference: DSCAPP-3748	Trigger	9.	The EDGEN bit generates a glitch on the CTED input causing a false trigger.	64/128	X	X	X	X
				256/512	X	—	X	—
CTMU Reference: DSCAPP-4684	Module Operation	10.	The CTMU module is not functional.	64/128	X	X	X	X
				256/512	X	—	X	—
ADC Reference: DSCAPP-4664	IV_{REF}	11.	The IV_{REF} input to the ADC is not functional.	64/128	X	X	X	X
				256/512	X	—	X	—
HVD Reference: DSCAPP-4761	HVDR	12.	On power-up, the High-Voltage Detect Reset event flag, HVDR bit in the RCON register, is being set.	64/128	X	X	X	X
				256/512	X	—	X	—

Legend: An 'X' indicates the issue is present in this revision of silicon;
shaded cells with an Em dash ('—') indicate that this silicon revision does not exist for this issue;
blank cells indicate an issue has been corrected or does not exist in this revision of silicon.

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TABLE 3: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item	Issue Summary	Device Flash Memory (KB)	Affected Revisions			
					A0	A2	B0	B1
Power-Saving Modes Reference: DSCAPP-4763	Idle	13.	On exit from Sleep mode, the SLEEP and IDLE status bits in the RCON register are being set.	64/128	X	X	X	X
				256/512	X	—	X	—
UART Reference: Not Listed	Auto-baud	14.	Auto-baud does not function to set the baud rate.	64/128	X	X	X	X
				256/512	X	—	X	—
Bus Matrix Reference: MCU32S-233	Flash Size	15.	The Flash Memory Size register (BMXPFMSZ) was not programmed with the correct value.	64/128	Date code pre-1750			
				256/512				
I/O Port Reference: PTEO-264	Drive Strength	16.	Pins RD15 & RF13 must be considered 4x Sink Driver Pins and not 8x Sink Driver Pins.	64/128	X	X	X	X
				256/512	X	—	X	—
Flash Memory Reference: M32S-245	Flash Memory Integrity	17.	Flash Memory may corrupt if $\overline{\text{MCLR}}$ is active before BOR event is reached.	64/128	X	X	X	X
				256/512	X	—	X	—
USB Low-Speed Mode Reference: CHIP002-3111	USB Low Speed	18.	USB Low-Speed Device and Host mode is not supported.	64/128	X	X	X	X
				256/512	X	—	X	—
Data Sheet Clarifications	RTSP		RTSP of Configuration Words is not functional	64/128	X	X	X	X
				256/512	X	—	X	—

Legend: An 'X' indicates the issue is present in this revision of silicon;
shaded cells with an Em dash ('—') indicate that this silicon revision does not exist for this issue;
blank cells indicate an issue has been corrected or does not exist in this revision of silicon.

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Silicon Errata Issues

Note 1: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. The table provided in each issue indicates which issues exist for a particular revision of silicon based on Flash memory size.

2: The following applies to the Affected Silicon Revision tables in each silicon issue:

- An 'X' indicates the issue is present in this revision of silicon
- Shaded cells with an Em dash ('—') indicate that this silicon revision does not exist for this issue
- Blank cells indicate an issue has been corrected or does not exist in this revision of silicon.

1. Module: ADC Reference: ADC006-14

When the ADC is configured for 10-bit operation, the specifications in the data sheet are not met for operation above 500 ksps.

Work around

For 600 ksps operation, RIN = 500 ohms, TSAMP = 2 TAD. The module specifications are shown in Table 4. For 1000 ksps operation, RIN = 200 ohms, TSAMP = 2 TAD. The module specifications are shown in Table 5.

TABLE 4: 600 KSPS OPERATION

Parameter No.	Symbol	Minimum	Typical	Maximum	Units
AD17	RIN	—	—	200	Ohm
ADC Accuracy – Measurements taken with External VREF+/VREF-					
AD21c	INL	-1.5	—	1.5	LSB
AD22c	DNL	-1.4	—	2.1	LSB
AD23c	GERR	-1.2	—	1.2	LSB
ADC Accuracy – Measurements taken with Internal VREF+/VREF-					
AD21d	INL	-1.5	—	1.5	LSB
AD22d	DNL	-1.4	—	2.1	LSB

TABLE 5: 1000 KSPS OPERATION

Parameter No.	Symbol	Minimum	Typical	Maximum	Units
AD17	RIN	—	—	200	Ohm
ADC Accuracy – Measurements taken with External VREF+/VREF-					
AD21c	INL	-5.2	—	6.5	LSB
AD22c	DNL	-3.4	—	7	LSB
AD23c	GERR	-1.5	—	1.5	LSB
ADC Accuracy – Measurements taken with Internal VREF+/VREF-					
AD21d	INL	-5.2	—	6.5	LSB
AD22d	DNL	-3.4	—	7	LSB

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2	B0	B1	
64/128	X	X	X	X	
256/512	X	—	X	—	

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2. Module: Clock Reference: DSCAPP-3890

A clock signal is present on the CLKO pin, regardless of the clock source and setting of the CLKO Enable Configuration bit, OSCIOFNC (DEVCFG1<10>), during a Power-on Reset (POR) condition.

Work around

Do not connect the CLKO pin to a device that would be adversely affected by rapid pin toggling or a frequency other than that defined by the oscillator configuration. Do not use the CLKO pin as an input if the device connected to the CLKO pin would be adversely affected by the pin driving a signal out.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2	B0	B1	
64/128	X	X	X	X	
256/512	X	—	X	—	

3. Module: JTAG Reference: CHIP002-409

Boundary Scan is not supported.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2	B0	B1	
64/128	X	X	X	X	
256/512	X	—	X	—	

4. Module: Watchdog Timer Reference: DSCAPP-4218

When the Watchdog Timer module is used in Windowed mode, the module may issue a reset even if the user tries to clear the module within the allowed window.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2	B0	B1	
64/128	X	X	X	X	
256/512	X	—	X	—	

5. Module: USB Reference: DSCAPP-3630

If the bus has been idle for more than 3 ms, the IDLEIF interrupt flag is set. If software clears the interrupt flag and the bus remains idle, the IDLEIF interrupt flag will not be set again.

Work around

Software can leave the IDLEIF bit set until it has received some indication of bus resumption (i.e., Resume, Reset, SOF, or Error).

Note: Resume and Reset are the only interrupts that should be following IDLEIF assertion. If the IDLEIF bit is set, it should be okay to suspend the USB module (as long as this code is protected by the GUARD and/or ACTPEND logic). This will require software to clear the IDLEIF interrupt enable bit to exit the USB ISR (if using interrupt driven code).

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2	B0	B1	
64/128	X	X	X	X	
256/512	X	—	X	—	

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6. Module: UART Reference: DSCAPP-4666

During receive FIFO overflow conditions, the shift register stops receiving data, which causes the UART to lose synchronization with the serial data stream.

The only way to recover from this condition is to turn the UART OFF and ON until it synchronizes. This could require several OFF/ON sequences.

Work arounds

Work around 1:

Avoid the RX overrun condition by ensuring that the UARTx module has a high enough interrupt priority such that other peripheral interrupt processing latencies do not exceed the time to overrun the UART RX buffer based on the application baud rate. Alternately or in addition to, set the URXISEL bits in the UxSTA register to generate an earlier RX interrupt based on RX FIFO fill status to buy more time for interrupt latency processing requirements.

Work around 2:

If avoiding RX FIFO overruns is not possible, implement a ACK/NAK software handshake protocol to repeat lost packet transfers after restoring UART synchronization.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2	B0	B1	
64/128	X	X	X	X	
256/512	X	—	X	—	

7. Module: Comparator Voltage Reference Reference: Not Listed

Three of the four Comparator Voltage Reference operational modes, defined in Table 6, do not meet data sheet specifications.

TABLE 6:

CVRCON <CVRSS>	CVRCON <CVRR>	Accuracy Specification	Actual Accuracy
0 = (AVDD/AVSS)	0 = (CVRSRC/32)	0.5 LSB	8.2 LSB
0 = (AVDD/AVSS)	1 = (CVRSRC/24)	0.25 LSB	0.34 LSB
1 = (VREF+/VREF-)	0 = (CVRSRC/32)	0.5 LSB	8.2 LSB

Work around

If possible, set both the CVRSS bit (CVRCON<4>) and the CVRR bit (CVRCON<5>) to '1', which specifies the Comparator Voltage Reference source CVRSRC = [(VREF+) - (VREF-)] and 0 to 0.67 CVRSRC with a step size of CVRSRC/24, respectively.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2	B0	B1	
64/128	X	X	X	X	
256/512	X	—	X	—	

8. Module: Comparator Voltage Reference Reference: DSCAPP-4382

The Comparator Voltage Reference always behaves as if the CVRR bit (CVRCON<5>) is equal to '1', which specifies a range of 0 to 0.67 CVRSRC with a step size of CVRSRC/24, instead of a range of 0.25 to 0.75 CVRSRC and a step size of CVRSRC/32.

Work around

If possible, set the CVRR bit (CVRCON<5>) = 1 (i.e., 0 to 0.67 CVRSRC, with CVRSRC/24 step size, respectively).

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2	B0	B1	
64/128	X	X	X	X	
256/512	X	—	X	—	

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9. Module: CTMU Reference: DSCAPP-3748

The EDGEN bit generates a glitch on CTED input causing a false trigger.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2	B0	B1	
64/128	X	X	X	X	
256/512	X	—	X	—	

10. Module: CTMU Reference: DSCAPP-4684

The CTMU module is not functional.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2	B0	B1	
64/128	X	X	X	X	
256/512	X	—	X	—	

11. Module: ADC Reference: DSCAPP-4664

Converting the Internal Band Gap (IVREF) voltage source generates a High-Voltage Detect (HVD) event and aborts the conversion; therefore, this feature is not functional.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2	B0	B1	
64/128	X	X	X	X	
256/512	X	—	X	—	

12. Module: HVD Reference: DSCAPP-4761

On power-up, the High-Voltage Detect Reset, event flag (HVDR bit in the RCON register) is set incorrectly.

On a power-up, only the POR, BOR, and EXTR bits should be set with the proper VCAP bypass capacitor value, as stated in the current data sheet.

Work around

Check the status of the POR bit in the RCON register when checking the HVDR bit. If the POR bit is set, both bits can be cleared as the HVDR bit is a false detection. If the POR bit is clear, the HVDR bit has been correctly detected and can be handled according to the requirements of the application.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2	B0	B1	
64/128	X	X	X	X	
256/512	X	—	X	—	

13. Module: Power-Saving Modes Reference: DSCAPP-4763

On exit from Sleep mode, both the SLEEP and IDLE status bits in the RCON register are set.

Work around

Add the following code to the user application at the point it wakes from Sleep mode:

```
rcon_var1 = RCON;
// ... enter Sleep mode
if (rcon_var1 & 0x4) Nop();
// If IDLE bit already set previously
// before sleep do nothing
else RCONbits.IDLE = 0x0;
// If IDLE bit is not set previously
// and is after Sleep mode then clear
```

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2	B0	B1	
64/128	X	X	X	X	
256/512	X	—	X	—	

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14. Module: UART Reference: Not Listed

The UART auto-baud feature is intended to set the baud rate during run time based on external data input. However, this feature does not function.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2	B0	B1	
64/128	X	X	X	X	
256/512	X	—	X	—	

15. Module: Bus Matrix Reference: MCU32S-233

The Flash Memory Size register (BMXPFMSZ) was not programmed with the correct value.

Work around

Use a fixed number based on the size of the part being used.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2	B0	B1	
64/128	Date code pre-1750				
256/512					

16. Module: I/O Port Reference: PTEO-264

The RD15 and RF13 pins must be considered 4x Sink Driver Pins and not 8x Sink Driver Pins. Refer to the parameters DO10, DO20, and DO20A in the data sheet.

Work around

None.

Affected Silicon Revisions

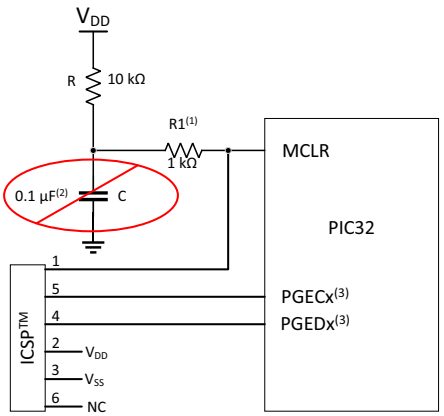
Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2	B0	B1	
64/128	X	X	X	X	
256/512	X	—	X	—	

17. Module: Flash Memory Reference: M32S-245

On power up, the internal Flash memory contents may be corrupted if MCLR is active before BOR event is reached. Either or both of the following workarounds may be required to prevent this issue.

Work around 1:

If, not using an external reset supervisor IC or equivalent, remove the MCLR capacitor as shown below, and retain the MCLR Pull-up resistor.



Work around 2:

If using an external reset supervisor IC or equivalent, increase the value of the VCAP capacitor to ≥47 µf ceramic or solid tantalum capacitor with an ESR ≤ 1 Ω.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2	B0	B1	
64/128	X	X	X	X	
256/512	X	—	X	—	

18. Module: USB Low-Speed Mode Reference: CHIP002-3111

USB Low-Speed mode is not functional in both Device and Host modes due to signal integrity compliance issues.

Work around:

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2	B0	B1	
64/128	X	X	X	X	
256/512	X	—	X	—	

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Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS20006624A**C**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

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APPENDIX A: REVISION HISTORY

Rev A Document (10/2014)

Initial release of this document, issued for revision A0 silicon, which includes silicon issues 1 (ADC Reference: ADC006-14), 2 (Clock Reference: DSCAPP-3890), 3 (JTAG Reference: CHIP002-409), 4 (Watchdog Timer Reference: DSCAPP-4218), 5 (USB Reference: DSCAPP-3630), 6 (UART Reference: DSCAPP-4666), 7 (Comparator Voltage Reference Reference: Not Listed), 8 (Comparator Voltage Reference Reference: DSCAPP-4382), 9 (CTMU Reference: DSCAPP-3748), 10 (CTMU Reference: DSCAPP-4684) and 11 (ADC Reference: DSCAPP-4664).

Rev B Document (7/2015)

Updated silicon issues 6 (UART Reference: DSCAPP-4666) and 11 (ADC Reference: DSCAPP-4664).

Added silicon issues 12 (HVD Reference: DSCAPP-4761) and 13 (Power-Saving Modes Reference: DSCAPP-4763).

Rev C Document (4/2016)

Revised document for silicon revisions A2.

Added silicon issue 14 (UART Reference: Not Listed).

Modified Silicon DEVREV Value Table 1 and added Silicon DEVREV Value Table 2.

Updated the Silicon Issue Summary table (Table 3) and silicon issue 9 (CTMU Reference: DSCAPP-3748).

Updated all Affected Silicon Revision tables.

Rev D Document (6/2018)

Added silicon issue 15 (Bus Matrix Reference: MCU32S-233).

Rev E Document (8/2018)

Added Silicon Issue 16 (**16. Module: "I/O Port Reference: PTEO-264"**).

Revision F Document (08/2019)

Added Data Sheet Clarification **""**.

Revision G Document (01/2020)

Added silicon issues **17. Module: "Flash Memory Reference: M32S-245"** and **18. Module: "USB Low-Speed Mode Reference: CHIP002-3111"**.

Revision H Document (03/2020)

Clarified Silicon Issues **17. Module: "Flash Memory Reference: M32S-245"** and **18. Module: "USB Low-Speed Mode Reference: CHIP002-3111"** to denote the lack of a Revision A2 silicon for devices with 256/512 KB Device Flash Memory.

Revision J Document (01/2025)

Revised the document to add silicon revisions B0 and B1 to all tables and silicon issues

Updated the verbiage for silicon issue **18. Module: "USB Low-Speed Mode Reference: CHIP002-3111"**

Revision K Document (04/2022)

Updated the silicon revision B0 details to all tables and silicon issues.

Revision L Document (09/2022)

Added Silicon Issue **"Data Sheet Clarifications"**

Revision M Document (07/2025)

Updated the image and verbiage for clarification in Silicon Issue **17. Module: "Flash Memory Reference: M32S-245"**.

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