chanhvinh.com

PIC32CZ CA8x/CA9x Family Silicon Errata and Data Sheet Clarifications

PIC32CZ CA8x/CA9x

Introduction

The PIC32CZ CA8x/CA9x family of devices that you have received conform functionally to the current device data sheet (DS60001749**K**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following tables. The silicon issues are summarized in the Table of Contents following this section.

The errata described in this document will be addressed in future revisions of the PIC32CZ CA8x/CA9x family of devices.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous, and current.

Data Sheet clarifications and corrections (if applicable) are located in the section Data Sheet Clarifications, following the discussion of silicon issues.

Table 1. PIC32CZ CA8x/CA9x Family Silicon Device Identification with 8M Flash

Part Number	Device ID (DID[31:0])	Mask Revision ('X' - DID[31:28])
		A1
PIC32CZ8110CA80208	0xX9200053	0x0
PIC32CZ8110CA80176	0xX9203053	
PIC32CZ8110CA80144	0xX9206053	
PIC32CZ8110CA80100	0xX9209053	
PIC32CZ8110CA90208	0xX920C053	
PIC32CZ8110CA90176	0xX920F053	
PIC32CZ8110CA90144	0xX9212053	
PIC32CZ8110CA90100	0xX9215053	

Table 2. PIC32CZ CA8x/CA9x Family Silicon Device Identification with 4M Flash

Part Number	Device ID (DID[31:0])	Mask Revision ('X' - DID[31:28])	
		A1	A2
PIC32CZ4010CA80208	0xX9201053	0x0	0x1
PIC32CZ4010CA80176	0xX9204053		
PIC32CZ4010CA80144	0xX9207053		
PIC32CZ4010CA80100	0xX920A053		
PIC32CZ4010CA90208	0xX920D053		-
PIC32CZ4010CA90176	0xX9210053		
PIC32CZ4010CA90144	0xX9213053		
PIC32CZ4010CA90100	0xX9216053		
PIC32CZ4010CA91208	0xX9218053	-	0x1
PIC32CZ4010CA91176	0xX9219053		
PIC32CZ4010CA91144	0xX921A053		
PIC32CZ4010CA91100	0xX921B053		

© 2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

Table 3. PIC32CZ CA8x/CA9x Family Silicon Device Identification with 2M Flash

Part Number	Device ID (DID[31:0])	Mask Revision ('X' - DID[31:28])	
		A1	A2
PIC32CZ2051CA80176	0xX9205053	0x0	0x2
PIC32CZ2051CA80144	0xX9208053		
PIC32CZ2051CA90100	0xX920B053		
PIC32CZ2051CA80208	0xX9202053		—
PIC32CZ2051CA90208	0xX920E053		
PIC32CZ2051CA90176	0xX9211053		
PIC32CZ2051CA90144	0xX9214053		
PIC32CZ2051CA90100	0xX9217053		
PIC32CZ2051CA91176	0xX921C053	—	0x2
PIC32CZ2051CA91144	0xX921D053		
PIC32CZ2051CA91100	0xX921E053		

Table 4. PIC32CZ CA8x/CA9x Family Silicon Device Identification with 1M Flash

Part Number	Device ID (DID[31:0])	Mask Revision ('X' - DID[31:28])
		A2
PIC32CZ1051CA82144	0xX921F053	0X3
PIC32CZ1051CA82100	0xX9220053	
PIC32CZ1051CA92144	0xX9221053	
PIC32CZ1051CA92100	0xX9222053	

Note: Refer to the “Device Service Unit” chapter in the current device data sheet (DS60001749**K**) for additional information on device identification and device-specific revision IDs.

© 2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

Table of Contents

Introduction....1

1. Silicon Issue Summary....4

2. Silicon Errata Issues....6
   - 2.1. AC....6
   - 2.2. Controller Area Network (CAN)....6
   - 2.3. DMA....6
   - 2.4. IxS....7
   - 2.5. MCLK....8
   - 2.6. MCRAMC....8
   - 2.7. NVMCTRL....8
   - 2.8. PORT....10
   - 2.9. RPMU....10
   - 2.10. SDHC....10
   - 2.11. SERCOM SPI....11
   - 2.12. Serial Quad Interface (SQI)....11
   - 2.13. TCC....12
   - 2.14. USB....13
   - 2.15. TRAM....13
   - 2.16. SERCOM....14
   - 2.17. FREQM....14
   - 2.18. OSCCTRL....15
   - 2.19. SUPC....15
   - 2.20. NMI....16
   - 2.21. Device....16
   - 2.22. DSU....16
   - 2.23. ITM....17

3. Data Sheet Clarifications....18

4. Revision History....19

Microchip Information....21
- Trademarks....21
- Legal Notice....21
- Microchip Devices Code Protection Feature....21

© 2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

1. Silicon Issue Summary

Table 1-1. Silicon Errata Summary

Module	Feature	Errata #	Issue Summary	Affected Revisions	
				A1	A2
AC	CTRLA.SWRST	2.1.1	Resisters that are not reset by SWRST can be written before SYNCBUSY.SWRST is cleared.	X	X
CAN	Debug Message Status Register	2.2.1	The CAN register field RXF1S.DMS is not cleared by setting CCCR.CCE.	X	X
CAN	Sequential CAN Msg TX	2.2.2	Message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID.	X	X
DMA	CRC	2.3.1	DMA Channel CRCROUT and CRCXOR settings are applied to CRC data only, and not applied on CRC Append Data.	X	X
DMA	BYTORD	2.3.2	Byte re-ordering settings incorrectly applied to descriptor data.	X	X
IxS	MCLKn	2.4.1	Assigning the IxS MCLKn signal to a pin through the I/O MUX does not enable the output.	X	X
IxS	FRMCNT	2.4.2	FRAMECTRL.FRMCNT set to 0x0 results in frame sync rate of 2.	X	X
IxS	I8S	2.4.3	When operating in I8S left/right justified client mode, data from the client is not transmitted properly and is erroneous.	X	X
MCLK	CLKDIV	2.5.1	PSLVERR is generated when RSVD values are written to CLKDIV registers.	X	X
MCRAMC	FLTCTRL	2.6.1	MCRAMC_FLTCTRL.FLTMD field is not write protected when FLTEN = 1	X	X
NVMCTRL	RDBUFWS	2.7.1	Setting RDBUFWS = 1 stalls the FCR read accesses.	X	-
NVMCTRL	PRM	2.7.2	NVMCTRL Power-Reduction mode is non-functional.	X	X
NVMCTRL	CRCMLEN	2.7.3	CRCMLEN active bits can exceed the PFM size for devices with Flash panels smaller than 8M Bytes.	X	X
NVMCTRL	CTRLA.ADRWS	2.7.4	When CTRLA.ADRWS is set to 1, reads to the same address across NVM regional boundaries can yield stale data.	X	-
NVMCTRL	CRC	2.7.5	FCR does not check addresses to verify they fall within a valid Flash memory region.	X	X
NVMCTRL	ECCCTRL	2.7.6	The ECC mode settings 0x10 and 0x01 are not functional for all possible read/write operations.	X	-
NVMCTRL	DBGCTRL.DBGECC	2.7.7	Bus errors reported to debugger when FCR -> DBGCTRL.DBGECC = 0 (NOERR).	X	X
PORT	WRCONFIG	2.8.1	Setting a pad in open drain mode will override other pin functions.	X	X
RPMU	BU Sleep Mode	2.9.1	Some registers that should persists after an RTC wake-up event from Back-Up Sleep mode are reset to zero.	X	X
RPMU	Hibernate Mode	2.9.2	RCAUSE.BKUPEXIT.HIB not set on wake up from Hibernate mode, when in Debug mode.	X	X
RPMU	RSTC.DBGCTRL	2.9.3	The RSTC DBCTRL register should only be reset by debugger reset but is also reset by other reset sources.	X	X
SDHC	PSR.CARDINS	2.10.1	The card detect status bit and downstream interrupt flag bits are updated only after internal clock is enabled.	X	X
SERCOM SPI	CTRLB.MSSEN	2.11.1	CTRLB.MSSEN is not useful for hardware control of $\overline{SS}$.	X	X
SERCOM SPI	I8S	2.11.2	When operating in I8S left/right justified, client mode, data from the client is not transmitted properly and is erroneous.	X	X
SQI	DDR	2.12.1	SQI Dual and Quad mode write modes are inoperable.	X	-
SQI	XIP	2.12.2	Byte and half-word transfers are not supported in XIP mode.	X	X
SQI	DMA	2.12.3	When using a DMA descriptor with the status polling option bit set, the PKTCOMPIF interrupt flag will set before the status check has completed.	X	X
TCC	DMA Request	2.13.1	The DMA One Shot trigger mode does not function in Capture Compare mode.	X	X
TCC	RAMP2	2.13.2	In two ramp modes (RAMP2, RAMP2A, RAMP2C, RAMP2CS) counting down mode is not supported.	X	X
TCC	RAMP2 Dithering	2.13.3	Retrigger in RAMP2 operations is not supported in Dithering mode.	X	X

© 2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

Table 1-1. Silicon Errata Summary (continued)

Module	Feature	Errata #	Issue Summary	Affected Revisions	
				A1	A2
TCC	CC	2.13.4	If a Retrigger event (EVCTRL.EVACTn = 0x1, RETRIGGER) occurs exactly at the Channel Compare Match [n] time, the next Waveform Output [n] is corrupted.	X	X
TCC	DMA	2.13.5	DMA trigger on Channel Compare Match is not functional.	X	X
USB	DBG	2.14.1	USB INTRUSB, and INTrRx and INTrTx registers are cleared by debug access.	X	X
USB	APB	2.14.2	Addressing some PHY registers set the APB clock request permanently.	X	X
TRAM	DRP	2.15.1	When Data Scrambling is enabled, accessing TRAM during DRP routine can lead to corrupted (read or write) data.	X	X
SERCOM	LIN	2.16.1	LIN Host mode adds non-conformal delay between break and sync bits.	X	X
SERCOM	LIN - Two Stop Bits	2.16.2	Two stop bits mode is not supported in SERCOM LIN operation.	X	X
FREQM	STATUS.BUSY	2.17.1	If during measurement slot, the STATUS.BUSY will never de-assert and DONE interrupt will not be raised.	X	X
OSCCTRL	DFLL48M	2.18.1	When the DFLL48M is used dynamically, tuning can be corrupted when re-enabling.	X	X
SUPC	BOR	2.19.1	The SUPC BOR register is reset after a watchdog or system reset.	X	X
NMI	GCLK	2.20.1	If NMI is configured in synchronous edge detection mode, spurious interrupts may occur after a software reset.	X	X
Device	Chip Erase	2.21.1	Chip erase is not functional for some parts.	-	X
DSU	FPACKAGE-100	2.22.1	Some GPIOs are not acting properly according to FPACKAGE-100 config.	X	X
ITM	Serial Wire Output (SWO)	2.23.1	SWO pin trace is not working.	X	X

Notes:

- Cells with 'X' indicate the issue is present in this revision of the silicon.
- Cells with '-' indicate this silicon revision does not exist for this issue.
- The blank cell indicates the issue has been corrected or does not exist in this revision of the silicon.

© 2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

2. Silicon Errata Issues

The following errata issues apply to the PIC32CZ CA8x/CA9x family of devices.

Note: Cells with an 'X' indicate the issue is present in this revision of the silicon.
Cells with a dash '-' indicate this silicon revision does not exist for this issue.

Blank cells indicate the issue has been corrected or does not exist in this revision of the silicon.

2.1. AC

2.1.1. CTRLA.SWRST

Registers that are not reset by SWRST can be written before SYNCBUSY.SWRST is cleared.

Workaround

Monitor SYNCBUSY.SWRST after setting CTRLA.SWRST to verify it has cleared before writing to any other registers in the AC module.

Affected Silicon Revisions

A1	A2				
X	X				

2.2. Controller Area Network (CAN)

2.2.1. Debug Message Status Register

The CAN register field, RXF1S.DMS, is not cleared by setting the CCCR.CCE.

Workaround

None.

Affected Silicon Revisions

A1	A2				
X	X				

2.2.2. Sequential CAN Msg TX

Several Tx Buffers are configured with the same Message ID. Transmission of these Tx Buffers is requested sequentially with a delay between the individual Tx requests. If multiple Tx Buffers are configured with the same Message ID, the Tx Buffers are not transmitted in order of the Tx Buffer number (lowest number first).

Workaround

Use the Tx FIFO instead of dedicated Tx Buffers for the transmission of several messages with the same Message ID in a specific order.

Affected Silicon Revisions

A1	A2				
X	X				

2.3. DMA

2.3.1. CRC

DMA Channel CRCROUT and CRCXOR settings are applied to CRC data only, and not applied on CRC Append Data.

© 2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

Workaround

None.

Affected Silicon Revisions

A1	A2				
X	X				

2.3.2. BYTORD

DMA.BYTORD: The DMA byte reordering settings for CHCTRLBk.BYTORD[1:0] and CHCTRLBk.WBOEN are incorrectly applied to descriptor data. The byte reordering feature is non-functional.

Workaround

None.

Affected Silicon Revisions

A1	A2				
X	X				

2.4. IxS

2.4.1. MCLKn

Assigning the IxS MCLKn signal to a pin through the I/O MUX does not enable the output.

Workaround

After assigning an IxS MCLKn signal to a pin, enable the output for the pin in the corresponding Data Direction register.

Affected Silicon Revisions

A1	A2				
X	X				

2.4.2. FRMCNT

When FRAMECTRL.FRMCNT is set to 0x0, a frame sync pulse must be generated for each serial word (slot). Actual behavior is that one frame sync pulse is generated for every two serial words (slots) when FRAMECTRL.FRMCNT is set to 0x0.

Workaround

None.

Affected Silicon Revisions

A1	A2				
X	X				

2.4.3. I8S

When operating in I8S left or right justified client mode, data from the client is not transmitted properly and is erroneous.

Workaround

Use TDM mode rather than I8S mode.

Affected Silicon Revisions

A1	A2				
X	X				

© 2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

2.5. MCLK

2.5.1. CLKDIV

Any Halfword write to offset 2 or BYTE write at offset 1/2/3 to the CLKDIV register with RSVD value is causing PSLVERR.

Workaround

Only WORD access is allowed to the CLKDIV register.

Affected Silicon Revisions

A1	A2				
X	X				

2.6. MCRAMC

2.6.1. FLTCTRL

MCRAMC.FLTCTRL.FLTMD field is not write protected when FLTEN = 1. It is possible for the FLTMD setting to become corrupted or to be overwritten while fault injection is enabled.

Workaround

None.

Affected Silicon Revisions

A1	A2				
X	X				

2.7. NVMCTRL

2.7.1. RDBUFWS

Setting the RDBUFWS bits = 1 stalls the FCR read access.

Workaround

The RDBUFWS bits should all be set to 0. The feature for deterministic FCR wait states is non-functional.

Affected Silicon Revisions

A1	A2				
X	-				

2.7.2. PRM

NVMCTRL Power Reduction mode is non-functional. The default values of NVMCTRL.CTRLB.PRM = 0x0 and NVMCTRL.CTRLB.SLP = 0x0 must be maintained for proper operation.

Workaround

None.

Affected Silicon Revisions

A1	A2				
X	X				

2.7.3. CRCMLEN

CRCMLEN active bits can exceed the PFM size for devices with Flash panels smaller than 8M Bytes.

© 2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

Workaround

The value written to CRCMLEN should not exceed the size of the PFM.

Examples: 8M – 0x800000 | 4M – 0x400000 | 2M – 0x200000

Affected Silicon Revisions

A1	A2				
X	X				

2.7.4. CTRLA.ADRWS

When CTRLA.ADRWS is set to 1, reads to the same address across NVM regional boundaries can yield stale data.

Workaround

CTRLA.ADRWS should be set to 0.

Affected Silicon Revisions

A1	A2				
X	-				

2.7.5. CRC

FCR does not check addresses to verify they fall within a valid Flash memory region.

Workaround

Application code should make certain that configured CRC calculations do not extend beyond the valid PFM address range.

Affected Silicon Revisions

A1	A2				
X	X				

2.7.6. ECCCTRL

The ECC mode settings 0x10 (Dynamic Writes with Dynamic Reads but w/o Bus Error) and 0x01 (Dynamic Writes with Dynamic Reads) are not functional for all possible read/write operations.

Workaround

Do not use the ECCCTRL settings 0x10 (Dynamic Writes with Dynamic Reads but w/o Bus Error) and 0x01 (Dynamic Writes with Dynamic Reads).

Affected Silicon Revisions

A1	A2				
X	-				

2.7.7. DBGCTRL.DGBECC

Bus errors reported to debugger when FCR -> DBGCTRL.DBGECC = 0 (NOERR).

Workaround

None.

Affected Silicon Revisions

A1	A2				
X	X				

© 2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

2.8. PORT

2.8.1. PORT.WRCONFIG.ODRAIN

Setting a pad in open drain mode will override other pin functions.

Workaround

Do not set the WRCONFIG.ODRAIN bit unless the open drain function is desired.

Affected Silicon Revisions

A1	A2				
X	X				

2.9. RPMU

2.9.1. BU Sleep Mode

Some registers that should persists after an RTC wake-up event from Back-Up Sleep mode are reset to zero. The RTC.DBGCTRL, SUPC.BOR registers and all of the FCW registers will be reset after an RTC wake-up event from Back-Up Sleep mode.

Workaround

Save the states of the affected registers before entering Back-Up Sleep mode and restore after the wake-up event.

Affected Silicon Revisions

A1	A2				
X	X				

2.9.2. Hibernate Mode

RCAUSE.BKUPEXIT.HIB is not set on wake-up from Hibernate mode when in Debug mode.

Workaround

None.

Affected Silicon Revisions

A1	A2				
X	X				

2.9.3. RSTC.DBGCTRL

The RSTC DBCTRL register should only be reset by debugger reset, but is also reset by other reset sources.

Workaround

None.

Affected Silicon Revisions

A1	A2				
X	X				

2.10. SDHC

2.10.1. SDHC.PSR.CARDINS

The Card Detect Status bit (SDHC.PSR.CARDINS) and downstream interrupt flag bits are updated only after internal clock is enabled (SDHC.CCR.INTCLKEN).

© 2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

Workaround

The SDHC.CCR.INTCLKEN bit must remain set or be set in order for the Card Detect Status bit (SDHC.PSR.CARDINS) and the Downstream Interrupt Flag bits to function.

Affected Silicon Revisions

A1	A2				
X	X				

2.11. SERCOM SPI

2.11.1. CTRLB.MSSEN

When Hardware SPI Select Control is enabled (CTRLB.MSSEN = 1), the SPI Select ($\overline{SS}$) pin goes high after each byte transfer, even if a new byte is ready to be sent.

Workaround

Set CTRLB.MSSEN = 0 and handle the SPI Select ($\overline{SS}$) pin in software.

Affected Silicon Revisions

A1	A2				
X	X				

2.11.2. I8S

When operating in I8S left/right justified client mode, data from the client is not transmitted properly and is erroneous.

Workaround

Use TDM mode rather than I8S mode.

Affected Silicon Revisions

A1	A2				
X	X				

2.12. Serial Quad Interface (SQI)

2.12.1. DDR

SQI Dual and Quad mode Double Data Rate (DDR) write modes are inoperable.

Workaround

None.

Affected Silicon Revisions

A1	A2				
X	-				

2.12.2. XIP

Byte and half-word transfers are not supported in XIP mode.

Workaround

When using XIP mode, transfer access should be limited to word size.

Affected Silicon Revisions

A1	A2				
X	X				

© 2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

2.12.3. DMA

When using a DMA descriptor with the Status Polling Option bit set, the PKTCOMPIF interrupt flag will set before the status check has completed.

Workaround

- Disable the interrupts for the descriptor that use status check.
- Add a new descriptor (preferably read) to the list right after the one with the status check bit set.
- Set the interrupt enable on this descriptor CBD_INT_EN & PKT_INT_EN.
- The execution of this descriptor will only happen after the previous one is complete (including its corresponding status check).
- Use the PKTCOMPIF will set after the whole operation has completed.

Note: Ensure to manually clear PKTCOMPIF when starting a DMA operation.

Affected Silicon Revisions

A1	A2				
X	X				

2.13. TCC

2.13.1. DMA Request

The DMA one-shot trigger mode (TCC.CTRLA.DMAOS) does not function on MC DMA triggers.

Workaround

None.

Affected Silicon Revisions

A1	A2				
X	X				

2.13.2. RAMP2

In two ramp modes (RAMP2, RAMP2A, RAMP2C, RAMP2CS) counting down mode is not supported.

Workaround

In two ramp modes (RAMP2, RAMP2A, RAMP2C, RAMP2CS) use counting up mode.

Affected Silicon Revisions

A1	A2				
X	X				

2.13.3. RAMP2 - Dithering

In two ramp modes (RAMP2, RAMP2A, RAMP2C, RAMP2CS) re-trigger is not supported in dithering mode.

Workaround

None.

Affected Silicon Revisions

A1	A2				
X	X				

© 2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

2.13.4. CC

If a Retrigger event (EVCTRL.EVACTn = 0x1, RETRIGGER) occurs exactly at the Channel Compare Match [n] time, the next Waveform Output [n] is corrupted.

Workaround

Use two channels to store their two successive (n and n+1) CC register values and combine their related waveform outputs to make signal redundancy.

Affected Silicon Revisions

A1	A2				
X	X				

2.13.5. DMA

DMA trigger on Channel Compare Match is not functional.

Workaround

Alternatively, use DMA trigger on Counter Overflow (OVF) or use the Channel Compare Match event output using the Event System as DMA trigger.

Affected Silicon Revisions

A1	A2				
X	X				

2.14. USB

2.14.1. DBG

USB INTRUSB/INTrRx and INTrTx registers are cleared by a read operation including debug access. This can lead to improper function during debugging.

Workaround

None.

Affected Silicon Revisions

A1	A2				
X	X				

2.14.2. APB

Addressing some PHY registers sets the APB clock request permanently.

Workaround

In the startup code, perform a dummy read to the USB.STATUS register. After accessing a register in the USB, the PHY subspace (starting with PHY00) should always be followed by a dummy read of the USB.STATUS register to clear the APB clock request.

Affected Silicon Revisions

A1	A2				
X	X				

2.15. TRAM

2.15.1. DRP

When Data Scrambling is enabled, accessing the RAM during a Data Remanence Prevention (DRP) routine can lead to corrupted (read/write) data.

© 2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

Workaround

Data Scrambling and DRP should not be used at the same time.

Affected Silicon Revisions

A1	A2				
X	X				

2.16. SERCOM

2.16.1. LIN

In SERCOM USART LIN Host mode (CTRLA.FORM = 0x2), in the case where break, sync, and identifier fields are automatically transmitted when DATA is written with the identifier (CTRLB.LINCMD = 0x2), the LIN Host Header delay between the sync and the ID transmission fields is not correct for the following cases:

- CTRLC.HDRDLY = 0x2: Where the delay between sync and ID transmission fields is 8-bit time instead of 4-bit time.
- CTRLC.HDRDLY = 0x3: Where the delay between sync and ID transmission fields is 14-bit time instead of 4-bit time.

Workaround

None.

Affected Silicon Revisions

A1	A2				
X	X				

2.16.2. LIN - Two Stop Bits

Two stop bits mode (CTRLB.SBMODE = 0x1) is not supported in SERCOM USART LIN Host mode (CTRLA.FORM = 0x2) in the case where break, sync, and identifier fields are automatically transmitted when DATA is written with the identifier (CTRLB.LINCMD = 0x2). Only one stop bit mode is supported.

Workaround

None.

Affected Silicon Revisions

A1	A2				
X	X				

2.17. FREQM

2.17.1. STATUS.BUSY

If during measurement slot, the measurement clock stalls or is very slow, the STATUS.BUSY will never de-assert and DONE interrupt will not be raised.

Workaround

None.

Affected Silicon Revisions

A1	A2				
X	X				

© 2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

2.18. OSCCTRL

2.18.1. DFLL48M

When the DFLL48M is used dynamically (enabled and disabled during application run-time, on-demand, or otherwise), tuning can be corrupted when re-enabled.

Workaround

To prevent this issue, it is necessary to use a small step size (recommend DFLLMUL.STEP = 1) and to disable quick lock (DFLLCTRLB.QLDIS = 1) in the case that dynamic operation of the DFLL48M is required.

Affected Silicon Revisions

A1	A2				
X	X				

2.19. SUPC

2.19.1. BOR

The SUPC BOR register is reset after a watchdog or system reset.

Workaround

None.

Affected Silicon Revisions

A1	A2				
X	X				

© 2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

2.20. NMI

2.20.1. GCLK

NMI.GLCK: If NMI is configured in synchronous edge detection mode (NMICTR.NMISENSE = 1, 2, or 3; NMICTRL.NMIASYNCH = 0), spurious NMI interrupts may occur after a software reset (CTRLA.SWRST = 1).

Workaround

- Configure one dummy EIC External Interrupt x (EXTINTx) in edge detection mode
- Enable EIC: CTRLA.ENABLE = 1
- Wait for synchronization completion (SYNCBUSY.ENABLE = 0)
- Configure the NMI in edge detection mode

Affected Silicon Revisions

A1	A2				
X	X				

2.21. Device

2.21.1. Chip Erase

Chip Erase is not functional on the following devices and executing Chip Erase will cause the device to remain in DAL = 0 mode until the next power cycle or reset:

PIC32CZ4010CA80208, PIC32CZ4010CA80176, PIC32CZ4010CA80144, PIC32CZ4010CA80100, PIC32CZ4010CA91208, PIC32CZ4010CA91176, PIC32CZ4010CA91144, and PIC32CZ4010CA91100.

⚠ WARNING To prevent the device from becoming inaccessible during development, the DAL level must remain at DAL = 2. The DAL level should only be lowered after development is completed and the device can be securely locked.

Workaround

In order to achieve a full device erasure, the user must implement an ‘as needed function’ to perform a page-by-page erase and clearing of RAM contents.

Affected Silicon Revisions

A1	A2				
-	X				

2.22. DSU

2.22.1. FPACKAGE-100

For 100-pin packages, when the FPACKAGE bit is set to 100 pins, GPIO PA18, PA19, and PA20 are disabled for TQFP100 parts.

Workaround

Set the FPACKAGE bit to 144 pin to enable PA18, PA19, and PA20. This configures the TQFP100 package to behave as a 144-pin package. Therefore, some ports that are not bonded out will be enabled.

© 2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

Affected Silicon Revisions

A1	A2				
X	X				

2.23. ITM

2.23.1. Serial Wire Output (SWO)

The SWO single-pin trace interface is currently non-functional.

Workaround

None.

Affected Silicon Revisions

A1	A2				
X	X				

© 2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the device data sheet (DS60001749**K**), and are showed in **BOLD** type:

There are currently no Data Sheet Clarifications to report.

© 2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

4. Revision History

Revision H - 09/2025

The following errata were updated in this revision:

- Device: 2.21.1 Chip Erase

Revision G - 06/2025

Updated the Data Sheet version to **K** throughout the document.

The following errata were updated in this revision:

- SQI: 2.12.1 DDR

The following errata were added in this revision:

- DSU: 2.22.1 FPACKAGE-100
- ITM: 2.23.1 Serial Wire Output (SWO)

Revision F - 12/2024

The following updates were performed for this revision:

- Updated the Data Sheet version to **J** throughout the document

Revision E - 11/2024

Minor updates were performed for silicon revisions and naming conventions in this version.

The following sections were updated for this revision:

- Updated the Silicon Revision tables in the Introduction
- Updated all the Silicon Revision tables for each Errata throughout the document

The following errata were added in this revision:

- SERCOM SPI: 2.11.2 I8S
- Device: 2.21.1 Chip Erase

Revision D - 07/2023

The following errata were updating during this revision with new verbiage:

- TCC: 2.13.1 DMA Request
- TCC: 2.13.3 RAMP2 - Dithering
- FREQM: 2.17.1 STATUS.BUSY

Revision C - 05/2023

The following Errata were added in this revision:

- DMA: 2.3.2 BYTORD
- NVMCTRL: 2.8.3 CRCMLEN
- NVMCTRL: 2.8.4 CTRLA.ADRWS
- NVMCTRL: 2.8.5 CRC
- NVMCTRL: 2.8.6 ECCCTRL
- NVMCTRL: 2.8.7 DBGCTRL.DBGECC
- TCC: 2.14.2 RAMP2
- TCC: 2.14.3 RAMP2 Dithering
- TCC: 2.14.6 DMA
- SQI: 2.12.2 XIP

© 2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

- USB: 2.15.2 APB
- TRAM: 2.16.1 DRP
- SERCOM: 2.17.1 LIN
- SERCOM: 2.17.2 LIN Two Stop Bits
- FREQM: 2.18.1 STATUS.BUSY
- OSCCTRL: 2.19.1 DFLL48M
- SUPC: 2.20.1 BOR
- NMI: 2.21.1 GCLK

Revision B - 02/2023

The following updates were performed for this revision:

- Added a new "Family Silicon Device Identification" table

Revision A - 07/2022

This is the initial released version of this document.

© 2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

Microchip Information

Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at https://www.microchip.com/en-us/about/legal-information/microchip-trademarks.

ISBN: 979-8-3371-2022-5

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP “AS IS”. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP’S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip products are strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

© 2025 Microchip Technology Inc. and its subsidiaries