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PIC24FJ64GP205/GU205 Family

16-Bit eXtreme Low-Power Microcontrollers with USB in Low Pin Count Packages

High-Performance CPU

- Modified Harvard Architecture
- 64 Kbytes of Flash Memory
- 8 Kbytes of SRAM
- Up to 16 MIPS Operation @ 32 MHz
- 8 MHz Fast RC (FRC) Internal Oscillator:
  - 96 MHz PLL option
  - Multiple clock divide options
  - Fast start-up
- 17-Bit x 17-Bit Single-Cycle Hardware Fractional/Integer Multiplier
- 32-Bit by 16-Bit Hardware Divider
- 16-Bit x 16-Bit Working Register Array
- C Compiler Optimized Instruction Set Architecture
- Two Address Generation Units (AGUs) for Separate Read and Write Addressing of Data Memory

Universal Serial Bus (USB) Features

- USB v2.0 On-The-Go (OTG)
- Dual Role Capable – Can Act as either Host or Device
- Low-Speed (1.5 Mb/s) and Full-Speed (12 Mb/s) USB Operation in Host mode
- Full-Speed USB Operation in Device mode
- High-Precision PLL for USB
- USB Device mode Operation from FRC Oscillator – No Crystal Oscillator Required
- Supports Up to 32 Endpoints (16 bidirectional):
  - USB module can use any RAM location on the device as USB endpoint buffers
- On-Chip USB Transceiver with Interface for Off-Chip USB Transceiver
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- On-Chip Pull-up and Pull-Down Resistors

Analog Features

- Up to 14-Channel, Software-Selectable 10/12-Bit Analog-to-Digital Converter:
  - 12-bit, 350K samples/second conversion rate (single Sample-and-Hold)
  - 10-bit, 400K samples/second conversion rate (single Sample-and-Hold)
  - Sleep mode operation
  - Low-voltage boost for input
  - Band gap reference input feature
  - Core-independent windowed threshold compare feature

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  - Auto-scan feature
- Three Analog Comparators with Input Multiplexing:
  - Programmable reference voltage for comparators

eXtreme Low-Power Features

- Sleep and Idle modes Selectively Shut Down Peripherals and/or Core for Substantial Power Reduction and Fast Wake-up
- Doze mode Allows CPU to Run at a Lower Clock Speed than Peripherals
- Alternate Clock modes Allow On-the-Fly Switching to a Lower Clock Speed for Selective Power Reduction
- Retention Sleep with On-Chip Ultra Low-Power Retention Regulator

Functional Safety and Security Peripherals

- Fail-Safe Clock Monitor Operation:
  - Detects clock failure and switches to on-chip, low-power RC Oscillator
- Power-on Reset (POR), Brown-out Reset (BOR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Programmable High/Low-Voltage Detect (HLVD)
- Flexible Watchdog Timer (WDT) with RC Oscillator for Reliable Operation
- Deadman Timer (DMT) for Safety-Critical Applications
- Programmable 32-Bit Cyclic Redundancy Check (CRC) Generator
- Flash OTP by ICSP™ Write Inhibit
- CodeGuard™ Security
- ECC Flash Memory (64 Kbytes) with Fault Injection:
  - Single Error Correction (SEC)
  - Double-Error Detection (DED)
- Customer OTP Memory
- Unique Device Identifier (UDID)

Special Microcontroller Features

- Supply Voltage Range of 2.0V to 3.6V
- Operating Ambient Temperature Range of -40°C to +125°C
- On-Chip Voltage Regulators (1.8V) for Low-Power Operation
- ECC Flash Memory (64 Kbytes):
  - 10,000 erase/write cycle endurance, typical
  - Data retention: 20 years minimum
  - Self-programmable under software control
  - Flash OTP emulation
- 8-Kbyte SRAM
- Programmable Reference Clock Output
- In-Circuit Serial Programming™ (ICSP™) and In-Circuit Emulation (ICE) via Two Pins
- JTAG Boundary Scan Support

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Peripheral Features

- High-Current Sink/Source 18 mA/18 mA on all I/O Pins
- Independent, Low-Power 32 kHz Timer Oscillator
- Two-Channel DMA Controller:
  - Minimizes CPU overhead and increases data throughput
- Timer1: 16-Bit Timer/Counter with External Crystal Oscillator; Timer1 can Provide an A/D Trigger
- Timer2/3: 16-Bit Timer/Counter, can Create 32-Bit Timer; Timer3 can Provide an A/D Trigger
- Five MCCP modules, Each with a Dedicated 16/32-Bit Timer:
  - Five 2-output MCCP modules
- Two Variable Width, Serial Peripheral Interface (SPI) Ports on All Devices; Three Operation modes:
  - Three-wire SPI (supports all four SPI modes)
  - Up to 32-byte deep FIFO buffer
  - I^2S mode
  - Speed up to 25 MHz
- Two I^2C Host and Client w/Address Masking, PMBus™ and IPMI Support
- Two UART modules:
  - LIN/J2602 bus support (auto-wake-up, Auto-Baud Detect, Break character support)
  - RS-232 and RS-485 support
  - IrDA® mode (hardware encoder/decoder functions)
- Five External Interrupt Pins
- Hardware Real-Time Clock and Calendar (RTCC)
- Peripheral Pin Select (PPS) Allows Independent I/O Mapping of Many Peripherals
- Configurable Interrupt-on-Change on All I/O Pins:
  - Each pin is independently configurable for rising edge or falling edge change detection
- Reference Clock Output with Programmable Divider
- Four Configurable Logic Cell (CLC) Blocks:
  - Two inputs and one output, all mappable to peripherals or I/O pins
  - AND/OR/XOR logic and D/JK flip-flop functions

PIC24FJ64GP205/GU205 Product Families

The device names, pin counts, memory sizes and peripheral availability of each device are listed in Table 1. The following pages show their pinout diagrams.

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Table 1. PIC24FJ64GP205/GU205 Family

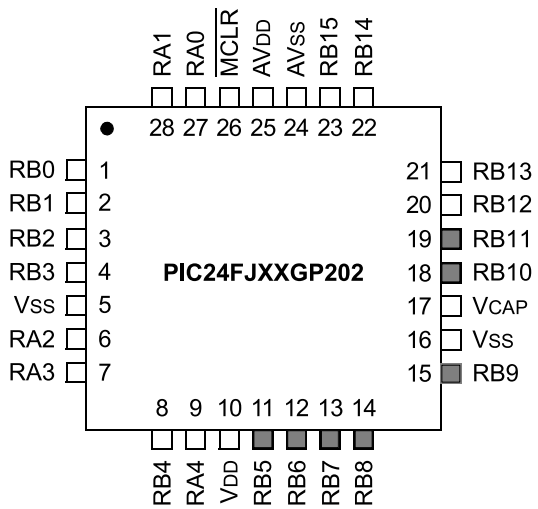
Device	Program Memory (Kbytes)	SRAM Memory (Kbytes)	Pins	I/O	PPS	DMA	10/12-Bit A/D Channels	Comparators	CRC	MCCP (Two-Output)	16-Bit Timers	I^2C	SPI	LIN-UART/ IrDA®	CLC	RTCC	USB OTG	JTAG BS
USB Devices																		
PIC24FJ64GU205	64	8	48	38	27/31	2	13	3	Yes	5	3	2	2	2	4	Yes	Yes	Yes
PIC24FJ64GU203	64	8	36	26	22/22	2	13	3	Yes	5	3	2	2	2	4	Yes	Yes	Yes
PIC24FJ64GU202	64	8	28	20	16/16	2	9	3	Yes	5	3	2	2	2	4	Yes	Yes	Yes
PIC24FJ32GU205	32	8	48	38	27/31	2	13	3	Yes	5	3	2	2	2	4	Yes	Yes	Yes
PIC24FJ32GU203	32	8	36	26	22/22	2	13	3	Yes	5	3	2	2	2	4	Yes	Yes	Yes
PIC24FJ32GU202	32	8	28	20	16/16	2	9	3	Yes	5	3	2	2	2	4	Yes	Yes	Yes
Non-USB Devices																		
PIC24FJ64GP205	64	8	48	39	29/33	2	14	3	Yes	5	3	2	2	2	4	Yes	No	Yes
PIC24FJ64GP203	64	8	36	27	24/24	2	14	3	Yes	5	3	2	2	2	4	Yes	No	Yes
PIC24FJ64GP202	64	8	28	21	18/18	2	10	3	Yes	5	3	2	2	2	4	Yes	No	Yes
PIC24FJ32GP205	32	8	48	39	29/33	2	14	3	Yes	5	3	2	2	2	4	Yes	No	Yes
PIC24FJ32GP203	32	8	36	27	24/24	2	14	3	Yes	5	3	2	2	2	4	Yes	No	Yes
PIC24FJ32GP202	32	8	28	21	18/18	2	10	3	Yes	5	3	2	2	2	4	Yes	No	Yes

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Pin Diagrams

28-Pin QFN, UQFN(1)



Note:

1. **Shaded** pins are up to 5.5 V_{DC} tolerant.

Table 2. PIC24FJXXGP202 QFN, UQFN(1)

Pin	Function(1)	Pin	Function(1)
1	PGED1/AN2/LVDIN/C2INB/**RP0**/RB0	15	TDO/C1INC/C2INC/C3INC/**RP9**/SDA1(2)/T1CK/RB9
2	PGEC1/AN1-/AN3/C2INA/**RP1**/RB1	16	V_{SS}
3	AN4/C1INB/**RP2**/SDA2/RB2	17	V_{CAP}
4	AN5/C1INA/**RP3**/SCL2/RB3	18	PGED2/TDI/**RP10**/ RB10
5	V_{SS}	19	PGEC2/TMS/**RP11**/ RB11
6	OSCI/CLKI/C1IND/RA2	20	AN8/LVDIN/**RP12**/RB12
7	OSCO/CLKO/C2IND/RA3	21	AN7/C1INC/**RP13**/ RB13
8	SOSCI/C2IND/**RP4**/RB4	22	CV_{REF}/AN6/C3INB/**RP14**/RB14
9	SOSCO/SCLKI/C2INC/PWRLCLK/RA4	23	AN9/C3INA/**RP15**/RB15
10	V_{DD}	24	AV_{SS}/V_{SS}
11	PGED3/**RP5**/ASDA1/RB5	25	AV_{DD}/V_{DD}
12	PGEC3/**RP6**/ASCL1/RB6	26	$\overline{MCLR}$
13	**RP7**/INT0/RB7	27	$V_{REF}+/CV_{REF}+$/AN0/C3INC/**RP26**/ RA0
14	TCK/**RP8**/SCL1(2)/RB8	28	CV_{REF}-/AN1/C3IND/**RP27**/RA1

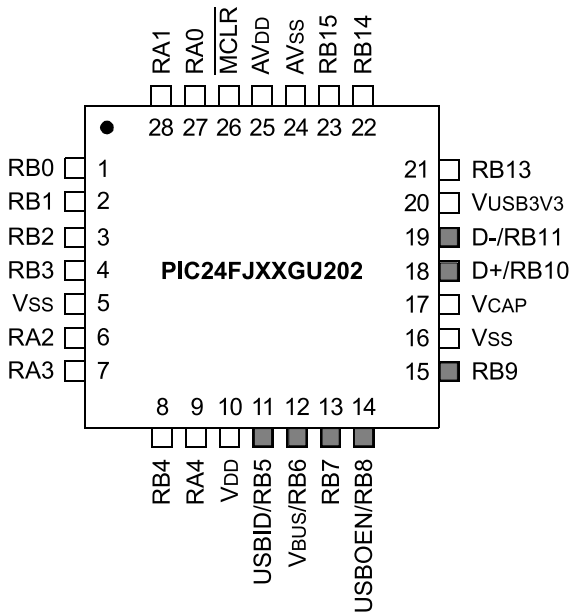
Notes:

1. **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.
2. Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

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Pin Diagrams

28-Pin QFN, UQFN(1)



Note:

1. **Shaded** pins are up to 5.5 V_{DC} tolerant.

Table 3. PIC24FJXXGU202 QFN, UQFN(1)

Pin	Function(1)	Pin	Function(1)
1	PGED1/AN2/LVDIN/C2INB/**RP0**/RB0	15	TDO/C1INC/C2INC/C3INC/**RP9**/SDA1(2)/T1CK/RB9
2	PGEC1/AN1-/AN3/C2INA/**RP1**/RB1	16	V_{SS}
3	AN4/C1INB/**RP2**/SDA2/RB2	17	V_{CAP}
4	AN5/C1INA/**RP3**/SCL2/RB3	18	PGED2/**RP10**/D+/ RB10
5	V_{SS}	19	PGEC2/**RP11**/ D-/RB11
6	OSCI/CLKI/C1IND/RA2	20	V_{USB3V3}
7	OSCO/CLKO/C2IND/RA3	21	AN7/C1INC/**RP13**/ RB13
8	SOSCI/C2IND/**RP4**/RB4	22	CV_{REF}/AN6/C3INB/**RP14**/RB14
9	SOSCO/SCLKI/C2INC/PWRLCLK/RA4	23	AN9/C3INA/**RP15**/RB15
10	V_{DD}	24	AV_{SS}/V_{SS}
11	TMS/**RP5**/USBID/RB5	25	AV_{DD}/V_{DD}
12	V_{BUS}/RB6	26	$\overline{MCLR}$
13	TDI/**RP7**/INT0/RB7	27	PGED3/V_{REF}+/CV_{REF}+/AN0/C3INC/**RP26**/ASDA1/RA0
14	TCK/**RP8**/SCL1(2)/$\overline{USBOEN}$/RB8	28	PGEC3/CV_{REF}-/AN1/C3IND/**RP27**/ASCL1/RA1

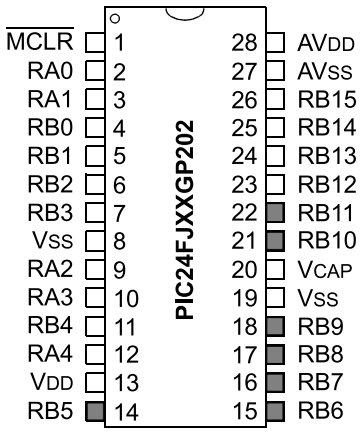
Notes:

1. **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.
2. Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

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Pin Diagrams

28-Pin SOIC, SSOP(1)



Note:

1. **Shaded** pins are up to 5.5 V_{DC} tolerant.

Table 4. PIC24FJXXGP202 SOIC, SSOP(1)

Pin	Function(1)	Pin	Function(1)
1	$\overline{MCLR}$	15	PGEC3/**RP6**/ASCL1/RB6
2	V_{REF}+/CV_{REF}+/AN0/C3INC/**RP26**/ RA0	16	**RP7**/INT0/RB7
3	CV_{REF}-/AN1/C3IND/**RP27**/RA1	17	TCK/**RP8**/SCL1(2)/RB8
4	PGED1/AN2/C2INB/**RP0**/RB0	18	TDO/C1INC/C2INC/C3INC/**RP9**/SDA1(2)/T1CK/RB9
5	PGEC1/AN1-/AN3/C2INA/**RP1**/RB1	19	V_{SS}
6	AN4/C1INB/**RP2**/SDA2/RB2	20	V_{CAP}
7	AN5/C1INA/**RP3**/SCL2/RB3	21	PGED2/TDI/**RP10**/RB10
8	V_{SS}	22	PGEC2/TMS/**RP11**/ RB11
9	OSCI/CLKI/C1IND/RA2	23	AN8/LVDIN/**RP12**/RB12
10	OSCO/CLKO/C2IND/RA3	24	AN7/C1INC/**RP13**/ RB13
11	SOSCI/C2IND/**RP4**/RB4	25	CV_{REF}/AN6/C3INB/**RP14**/RB14
12	SOSCO/SCLKI/C2INC/PWRLCLK/RA4	26	AN9/C3INA/**RP15**/RB15
13	V_{DD}	27	AV_{SS}/V_{SS}
14	PGED3/**RP5**/ASDA1/RB5	28	AV_{DD}/V_{DD}

Notes:

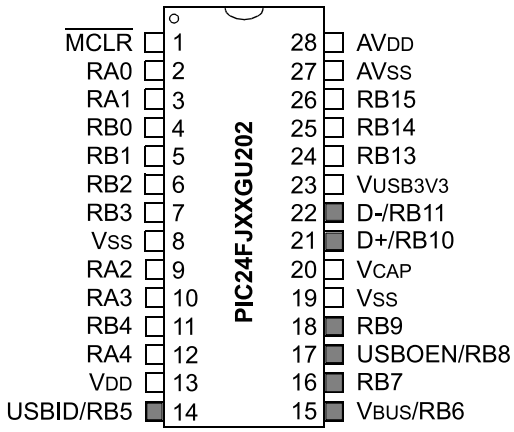
1. **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.
2. Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

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Pin Diagrams

28-Pin SOIC, SSOP(1)



Note:

1. **Shaded** pins are up to 5.5 V_{DC} tolerant.

Table 5. PIC24FJXXGU202 SOIC, SSOP(1)

Pin	Function(1)	Pin	Function(1)
1	$\overline{MCLR}$	15	V_{BUS}/RB6
2	PGED3/V_{REF}+/CV_{REF}+/AN0/C3INC/**RP26**/ASDA1/RA0	16	TDI/**RP7**/INT0/RB7
3	PGEC3/CV_{REF}-/AN1/C3IND/**RP27**/ASCL1/RA1	17	TCK/**RP8**/SCL1(2)/$\overline{USBOEN}$/RB8
4	PGED1/AN2/LVDIN/C2INB/**RP0**/RB0	18	TDO/C1INC/C2INC/C3INC/**RP9**/SDA1(2)/ T1CK/RB9
5	PGEC1/AN1-/AN3/C2INA/**RP1**/RB1	19	V_{SS}
6	AN4/C1INB/**RP2**/SDA2/RB2	20	V_{CAP}
7	AN5/C1INA/**RP3**/SCL2/RB3	21	PGED2/**RP10**/D+/RB10
8	V_{SS}	22	PGEC2/**RP11**/D-/RB11
9	OSCI/CLKI/C1IND/RA2	23	V_{USB3V3}
10	OSCO/CLKO/C2IND/RA3	24	AN7/C1INC/**RP13**/ RB13
11	SOSCI/C2IND/**RP4**/RB4	25	CV_{REF}/AN6/C3INB/**RP14**/RB14
12	SOSCO/SCLKI/C2INC/PWRLCLK/RA4	26	AN9/C3INA/**RP15**/RB15
13	V_{DD}	27	AV_{SS}/V_{SS}
14	TMS/**RP5**/USBID/RB5	28	AV_{DD}/V_{DD}

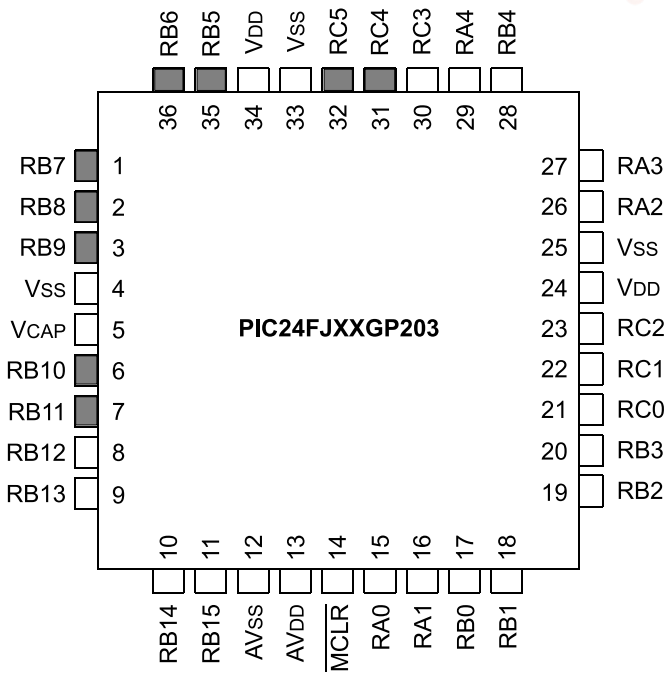
Notes:

1. **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.
2. Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

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Pin Diagrams

36-Pin UQFN(1)



Note:

1. **Shaded** pins are up to 5.5 V_{DC} tolerant.

Table 6. PIC24FJXXXGP203 Devices

Pin	Function(1)	Pin	Function(1)
1	**RP7**/INT0/RB7	19	AN4/C1INB/**RP2**/SDA2/RB2
2	TCK/**RP8**/SCL1(2)/RB8	20	AN5/C1INA/**RP3**/SCL2/RB3
3	TDO/C1INC/C2INC/ **RP9**/SDA1(2)/T1CK/RB9	21	AN10/**RP16**/RC0
4	V_{SS}	22	AN11/**RP17**/RC1
5	V_{CAP}	23	AN12/**RP18**/RC2
6	PGED2/TDI/**RP10**/ RB10	24	V_{DD}
7	PGEC2/TMS/**RP11**/ RB11	25	V_{SS}
8	AN8/LVDIN/**RP12**/RB12	26	OSCI/CLKI/C1IND/RA2
9	AN7/C1INC/**RP13**/ RB13	27	OSCO/CLKO/C2IND/RA3
10	CV_{REF}/AN6/**RP14**/RB14	28	SOSCI/C2IND/**RP4**/RB4
11	AN9 /**RP15**/RB15	29	SOSCO/SCLKI/C2INC/PWRLCLK/RA4
12	AV_{SS}	30	AN13/**RP19**/RC3
13	AV_{DD}	31	**RP20**/RC4
14	$\overline{MCLR}$	32	**RP21**/RC5
15	V_{REF}+/CV_{REF}+/AN0/**RP26**/RA0	33	V_{SS}
16	CV_{REF}-/AN1/**RP27**/RA1	34	V_{DD}

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.....continued			
Pin	**Function(1)**	**Pin**	**Function(1)**
17	PGED1/AN2/C2INB/**RP0**/RB0	35	PGED3/**RP5**/ASDA1/RB5
18	PGEC1/AN1-/AN3/C2INA/**RP1**/RB1	36	PGEC3/**RP6**/ASCL1/RB6

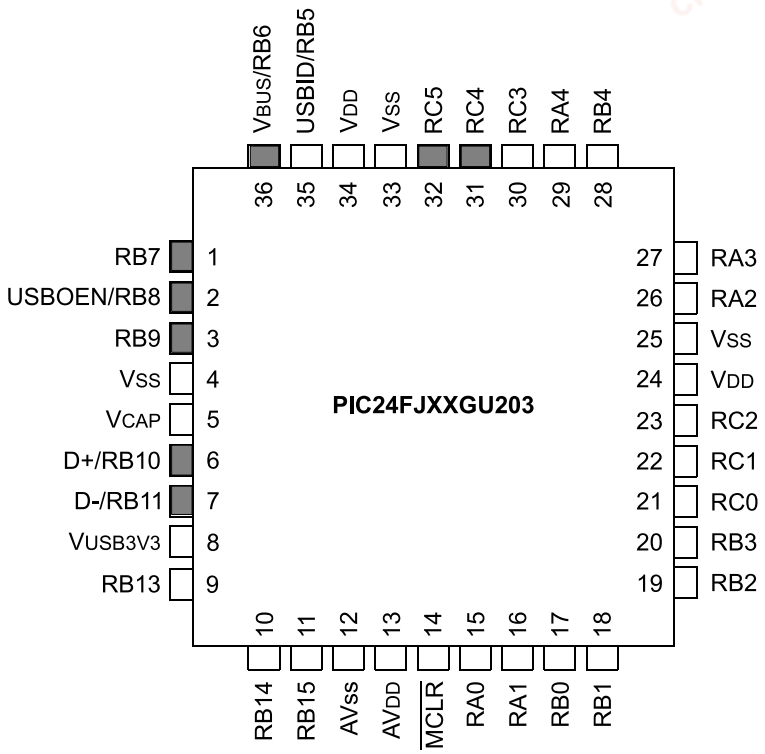
Notes:

1. **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.
2. Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

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Pin Diagrams

36-Pin UQFN(1)



Note:

1. **Shaded** pins are up to 5.5 V_{DC} tolerant.

Table 7. PIC24FJXXXGU203 Devices

Pin	Function(1)	Pin	Function(1)
1	**RP7**/INT0/RB7	19	AN4/C1INB/**RP2**/SDA2/RB2
2	TCK/RP8/SCL1(2)/USBOEN/RB8	20	AN5/C1INA/**RP3**/SCL2/RB3
3	TDO/C1INC/C2INC/RP9/SDA1(2)/T1CK/RB9	21	AN10/**RP16**/RC0
4	V_{SS}	22	AN11/**RP17**/RC1
5	V_{CAP}	23	AN12/**RP18**/RC2
6	PGED2/TDI/**RP10**/D+/RB10	24	V_{DD}
7	PGEC2/TMS/**RP11**/D-/RB11	25	V_{SS}
8	V_{USB3V3}	26	OSCI/CLKI/C1IND/RA2
9	AN7/C1INC/**RP13**/ RB13	27	OSCO/CLKO/C2IND/RA3
10	CV_{REF}/AN6/**RP14**/RB14	28	SOSCI/C2IND/**RP4**/RB4
11	AN9 /**RP15**/RB15	29	SOSCO/SCLKI/C2INC/PWRLCLK/RA4
12	AV_{SS}	30	AN13/**RP19**/RC3
13	AV_{DD}	31	**RP20**/RC4
14	MCLR	32	**RP21**/RC5

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.....continued			
Pin	**Function(1)**	**Pin**	**Function(1)**
15	V_{REF}+/CV_{REF}+/AN0/**RP26**/RA0	33	V_{SS}
16	CV_{REF}-/AN1/**RP27**/RA1	34	V_{DD}
17	PGED1/AN2/LVDIN/C2INB/**RP0**/RB0	35	PGED3/**RP5**/USBID/RB5
18	PGEC1/AN1-/AN3/C2INA/**RP1**/RB1	36	PGEC3/V_{BUS}/RB6

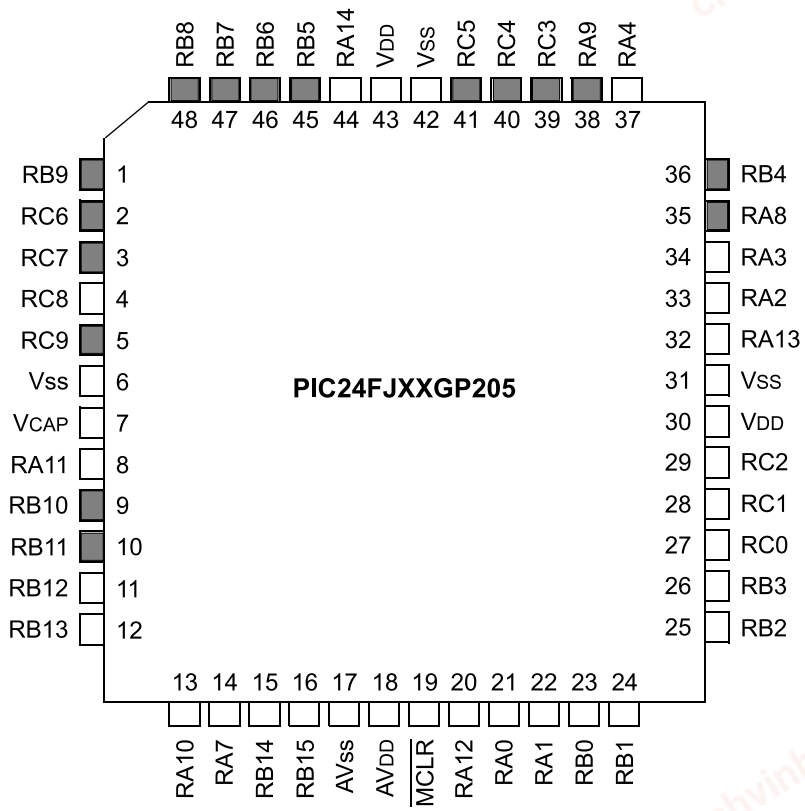
Notes:

1. **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.
2. Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

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Pin Diagrams

48-Pin UQFN, TQFP(1)



Note:

1. **Shaded** pins are up to 5.5 V_{DC} tolerant.

Table 8. PIC24FJXXXGP205 Devices

Pin	Function(1)	Pin	Function(1)
1	C1INC/C2INC/C3INC/**RP9**/SDA1(2)/T1CK/RB9	25	AN4/C1INB/**RP2**/SDA2/RB2
2	**RP22**/RC6	26	AN5/C1INA/**RP3**/SCL2/RB3
3	**RP23**/RC7	27	AN10/**RP16**/RC0
4	**RP24**/RC8	28	AN11/**RP17**/RC1
5	**RP25**/RC9	29	AN12/**RP18**/ RC2
6	V_{SS}	30	V_{DD}
7	V_{CAP}	31	V_{SS}
8	**RPI29**/RA11	32	**RPI31**/RA13
9	PGED2/**RP10**/RB10	33	OSCI/CLKI/C1IND/RA2
10	PGEC2/**RP11**/RB11	34	OSCO/CLKO/C2IND/RA3
11	AN8/LVDIN/**RP12**/RB12	35	TDO/RA8
12	AN7/C1INC/**RP13**/RB13	36	SOSCI/C2IND/**RP4**/RB4
13	TMS/**RP28**/RA10	37	SOSCO/SCLKI/C2INC/PWRLCLK/RA4

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.....continued			
Pin	**Function(1)**	**Pin**	**Function(1)**
14	TCK/RA7	38	TDI/RA9
15	CV_{REF}/AN6/C3INB/**RP14**/RB14	39	AN13/**RP19**/RC3
16	AN9/C3INA/**RP15**/RB15	40	**RP20**/RC4
17	AV_{SS}	41	**RP21**/RC5
18	AV_{DD}	42	V_{SS}
19	$\overline{MCLR}$	43	V_{DD}
20	**RPI30**/RA12	44	**RPI32**/RA14
21	V_{REF}+/CV_{REF}+/AN0/C3INC/**RP26**/RA0	45	PGED3/**RP5**/ASDA1/RB5
22	CV_{REF}-/AN1/C3IND/**RP27**/RA1	46	PGEC3/**RP6**/ASCL1/RB6
23	PGED1/AN2/C2INB/**RP0**/RB0	47	**RP7**/INT0/RB7
24	PGEC1/AN1-/AN3/C2INA/**RP1**/RB1	48	**RP8**/SCL1(2)/RB8

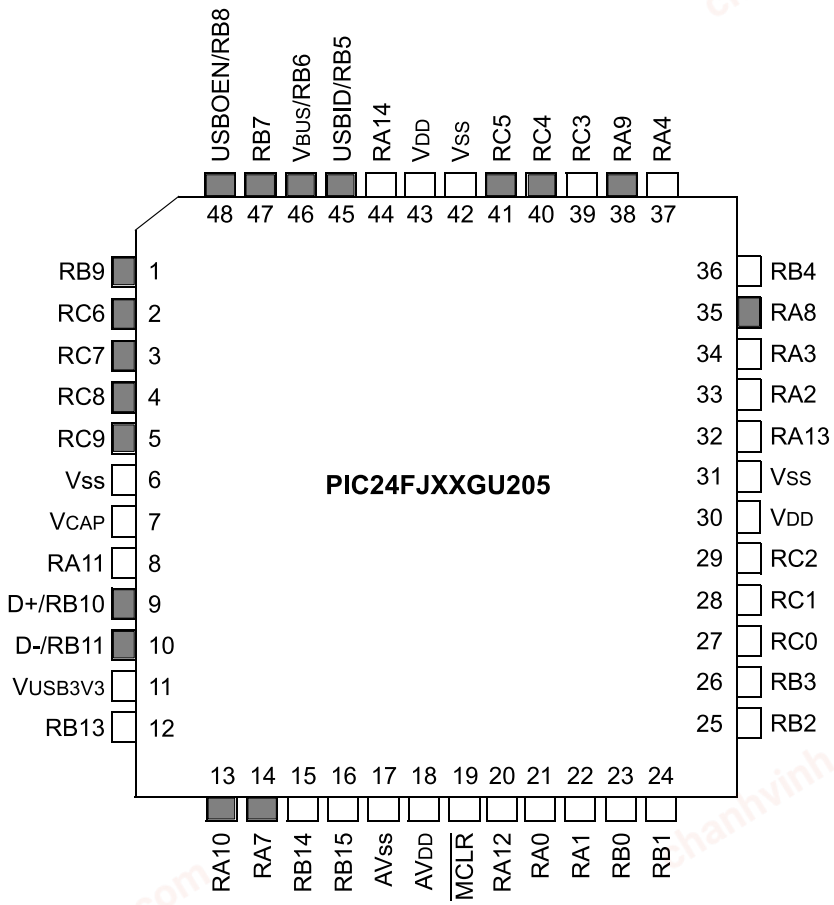
Notes:

1. **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.
2. Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

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Pin Diagrams

48-Pin UQFN, TQFP(1)



Note:

1. **Shaded** pins are up to 5.5 V_{DC} tolerant.

Table 9. PIC24FJXXXGU205 Devices

Pin	Function(1)	Pin	Function(1)
1	C1INC/C2INC/C3INC/**RP9**/SDA1(2)/T1CK/RB9	25	AN4/C1INB/**RP2**/SDA2/RB2
2	**RP22**/RC6	26	AN5/C1INA/**RP3**/SCL2/RB3
3	**RP23**/RC7	27	AN10/**RP16**/RC0
4	**RP24**/RC8	28	AN11/**RP17**/RC1
5	**RP25**/RC9	29	AN12/**RP18**/ RC2
6	V_{SS}	30	V_{DD}
7	V_{CAP}	31	V_{SS}
8	**RPI29**/RA11	32	**RPI31**/RA13
9	PGED2/RP10/D+/RB10	33	OSCI/CLKI/C1IND/RA2
10	PGEC2/RP11/D-/RB11	34	OSCO/CLKO/C2IND/RA3
11	V_{USB3V3}	35	TDO/RA8

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.....continued			
Pin	**Function(1)**	**Pin**	**Function(1)**
12	AN7/C1INC/**RP13**/RB13	36	SOSCI/C2IND/**RP4**/RB4
13	TMS/**RP28**/RA10	37	SOSCO/SCLKI/C2INC/PWRLCLK/RA4
14	TCK/RA7	38	TDI/RA9
15	CV_{REF}/AN6/C3INB/**RP14**/RB14	39	AN13/**RP19**/RC3
16	AN9/C3INA/**RP15**/RB15	40	**RP20**/RC4
17	AV_{SS}	41	**RP21**/RC5
18	AV_{DD}	42	V_{SS}
19	$\overline{MCLR}$	43	V_{DD}
20	**RPI30**/RA12	44	**RPI32**/RA14
21	PGED3/V_{REF}+/CV_{REF}+/AN0/C3INC/**RP26**/ASDA1/RA0	45	**RP5**/USBID/RB5
22	PGEC3/CV_{REF}-/AN1/C3IND/**RP27**/ASCL1/RA1	46	V_{BUS}/RB6
23	PGED1/AN2/LVDIN/C2INB/**RP0**/RB0	47	**RP7**/INT0/RB7
24	PGEC1/AN1-/AN3/C2INA/**RP1**/RB1	48	RP8/SCL1(2)/$\overline{USBOEN}$/RB8

Notes:

1. **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.
2. Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

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1. Device Overview

This document contains device-specific information for the following devices:

• PIC24FJ64GP205	• PIC24FJ64GU205
• PIC24FJ64GP203	• PIC24FJ64GU203
• PIC24FJ64GP202	• PIC24FJ64GU202
• PIC24F32GP205	• PIC24FJ32GU205
• PIC24FJ32GP203	• PIC24FJ32GU203
• PIC24FJ32GP202	• PIC24FJ32GU202

The PIC24FJ64GP205/GU205 family introduces eXtreme Low-Power Microcontrollers with USB in smaller package sizes. This is a 16-bit microcontroller family with a broad peripheral feature set and enhanced computational performance. This family also offers a new migration option for those high-performance applications which may be outgrowing their 8-bit platforms, but do not require the numerical processing power of a Digital Signal Processor (DSP).

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

1.1 Core Features

1.1.1 16-Bit Architecture

Central to all PIC24F devices is the 16-bit modified Harvard architecture, first introduced with Microchip's dsPIC® Digital Signal Controllers (DSCs). The PIC24F CPU core offers a wide range of enhancements, such as:

- 16-bit data and 24-bit address paths with the ability to move information between program and data memory spaces
- Linear addressing of up to 12 Mbytes (program space) and 32 Kbytes (data)
- A 16-element Working register array with built-in software stack support
- A 17 x 17 hardware multiplier with support for integer math
- Hardware support for 32 by 16-bit division
- An instruction set that supports multiple addressing modes and is optimized for high-level languages, such as 'C'
- Operational performance up to 16 MIPS

1.1.2 Power-Saving Technology

The PIC24FJ64GP205/GU205 family of devices includes low-voltage Sleep, a low-power mode with essential circuits being powered from a separate low-voltage regulator. This low-power mode also supports the continuous operation of the low-power, on-chip Real-Time Clock/Calendar (RTCC), making it possible for an application to keep time while the device is otherwise asleep.

Aside from this feature, PIC24FJ64GP205/GU205 family devices also include all of the legacy power-saving features of previous PIC24F microcontrollers, such as:

- On-the-Fly Clock Switching, allowing the selection of a lower power clock during run time
- Doze Mode Operation, for maintaining peripheral clock speed while slowing the CPU clock
- Instruction-Based Power-Saving Modes, for quick invocation of the Idle and Sleep modes

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1.1.3 Oscillator Options and Features

All of the devices in the PIC24FJ64GP205/GU205 family offer six different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes
- External Clock (EC) mode
- A Phase-Locked Loop (PLL) frequency multiplier, which allows processor speeds up to 32 MHz
- An internal Fast RC Oscillator (FRC), a nominal 8 MHz output with multiple frequency divider options
- A separate internal Low-Power RC (LPRC) Oscillator, 32 kHz nominal for low-power, timing-insensitive applications

The internal oscillator block also provides a stable reference source for the Fail-Safe Clock Monitor (FSCM). This option constantly monitors the main clock source against a reference signal provided by the internal oscillator and enables the controller to switch to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.

1.1.4 Easy Migration

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve. The consistent pinout scheme used throughout the entire family also aids in migrating from one device to the next larger device.

1.2 DMA Controller

PIC24FJ64GP205/GU205 family devices have a Direct Memory Access (DMA) Controller. This module acts in concert with the CPU, allowing data to move between data memory and peripherals without the intervention of the CPU, increasing data throughput and decreasing execution time overhead. Six independently programmable channels make it possible to service multiple peripherals at virtually the same time, with each channel peripheral performing a different operation. Many types of data transfer operations are supported.

1.3 USB On-The-Go (OTG)

The PIC24FJ64GP205/GU205 family of devices has USB On-The-Go functionality. This module provides on-chip functionality as a target device compatible with the USB 2.0 standard, as well as limited stand-alone functionality as a USB embedded host. By implementing USB Host Negotiation Protocol (HNP), the module can also dynamically switch between device and host operation, allowing for a much wider range of versatile USB-enabled applications on a microcontroller platform. In addition to USB host functionality, the PIC24FJ64GP205/GU205 family devices provide a true single chip USB solution, including an on-chip transceiver and voltage regulator, and a voltage boost generator for sourcing bus power during host operations.

1.4 Other Special Features

- Peripheral Pin Select: The Peripheral Pin Select (PPS) feature allows most digital peripherals to be mapped over a fixed set of digital I/O pins. Users may independently map the input and/or output of any one of the many digital peripherals to any one of the I/O pins.
- Configurable Logic Cell: The Configurable Logic Cell (CLC) module allows the user to specify combinations of signals as inputs to a logic function and to use the logic output to control other peripherals or I/O pins.
- Timing Modules: The PIC24FJ64GP205/GU205 family provides three independent, general purpose, 16-bit timers (two of which can be combined into two 32-bit timers). The devices also include five multiple output advanced Capture/Compare/PWM/Timer peripherals.
- Communications: The PIC24FJ64GP205/GU205 family incorporates a range of serial communication peripherals to handle a range of application requirements. There are two independent I^2C modules that support both Host and Client modes of operation. Devices also have, through the PPS feature, two independent UARTs with built-in IrDA® encoders/decoders and two SPI modules.
- Analog Features: All members of the PIC24FJ64GP205/GU205 family include a 12-bit A/D Converter (ADC) module and a triple comparator module. The A/D module incorporates a range of new features that allow the

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converter to assess and make decisions on incoming data, reducing CPU overhead for routine A/D conversions. The comparator module includes three analog comparators that are configurable for a wide range of operations.

- Real-Time Clock and Calendar (RTCC): This module implements a full-featured clock and calendar with alarm functions in hardware, freeing up timer resources and program memory space for use of the core application.
- Deadman Timer (DMT): This module is provided to interrupt the processor in the event of a software malfunction.

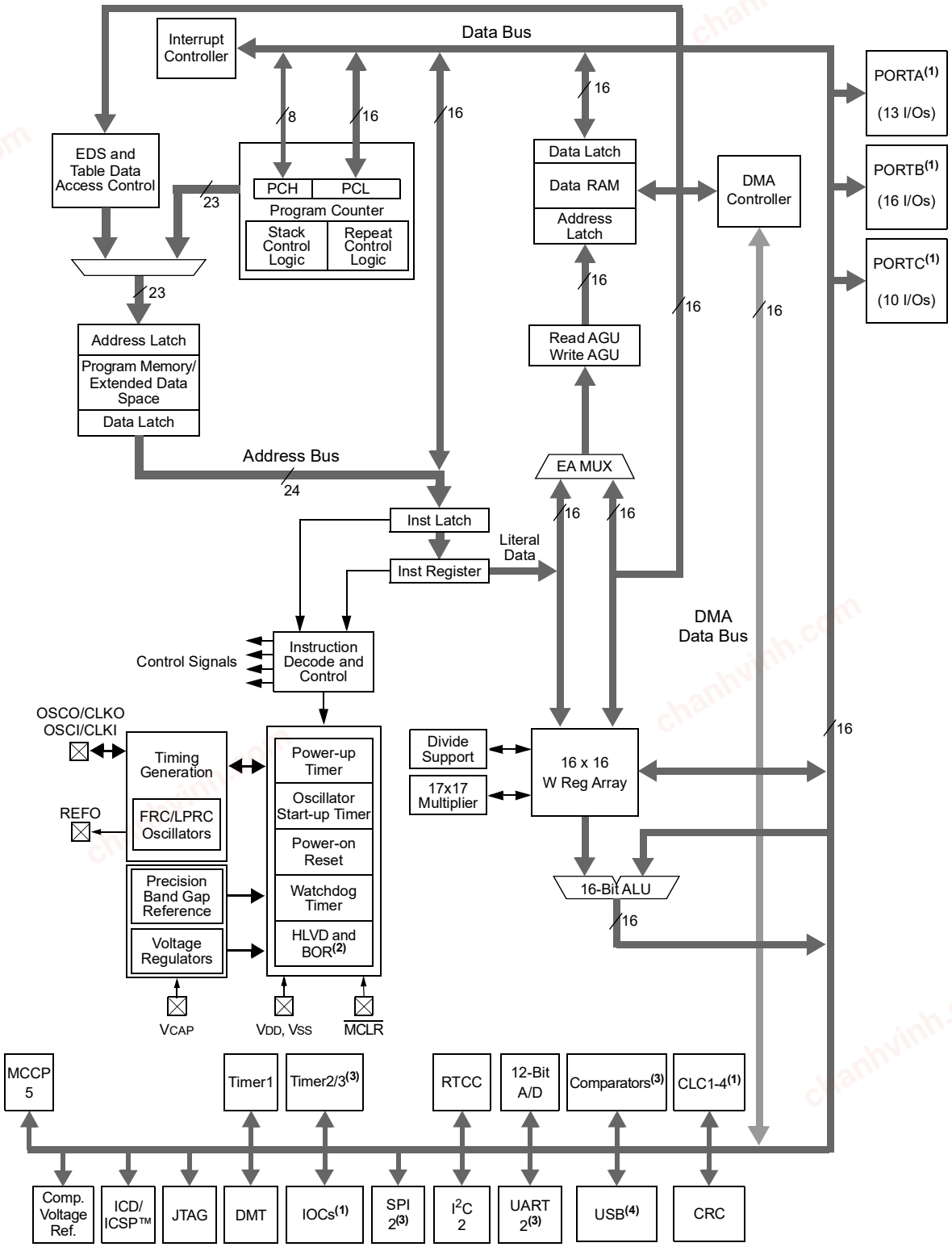
1.5 Feature Set

Devices in the PIC24FJ64GP205/GU205 family are available in 28-pin, 36-pin and 48-pin packages. The general block diagram for all devices is shown in Figure 1-1 .

A list of the pin features available on the PIC24FJ64GP205/GU205 family devices, sorted by function, is shown in Table 1-1. Pin feature information is provided in the pinout diagrams in the beginning of this data sheet. Multiplexed features are sorted by the priority given to a feature, with the highest priority peripheral being listed first.

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Figure 1-1. PIC24FJ64GP205/GU205 Family General Block Diagram



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Notes:

1. Not all I/O pins or features are implemented on all device pinout configurations. See pinout diagrams and tables for specific implementations by pin count.
2. BOR functionality is provided when the on-board voltage regulator is enabled.
3. Some peripheral I/Os are only accessible through remappable pins.
4. USB is available on PIC24FJXXX**GU**XXX devices only.

Table 1-1. PIC24FJ64GP205/GU205 Family Pinout Description

Pin Name	Pin Type	Buffer Type	PPS	Description
AN0-AN13	I	Analog	No	A/D Analog Inputs
AV_{DD}	P	—	No	Positive Supply for Analog Modules
AV_{SS}	P	—	No	Ground Reference for Analog Modules
C1INA-C1IND C1OUT	I O	Analog DIG	No Yes	Comparator 1 Inputs A through D Comparator 1 Output
C2INA-C2IND C2OUT	I O	Analog DIG	No Yes	Comparator 2 Inputs A through D Comparator 2 Output
AC2INC	I	Analog	No	Alternate Comparator 2 Input C
CLKI CLKO	— O	— DIG	No No	Primary Oscillator Clock Input (EC) System Clock Output
CV_{REF}	O	Analog	No	Comparator Voltage Reference Output
$CV_{REF}+$	I	Analog	No	Comparator Voltage Reference (high) Input
$CV_{REF}-$	I	Analog	No	Comparator Voltage Reference (low) Input
INT0 INT1-INT4	I I	ST ST	No Yes	External Interrupt Input 0 External Interrupt Inputs 1 through 4
LVDIN	I	Analog	No	Low-Voltage Detect Input
$\overline{MCLR}$	I	ST	No	Master Clear (device Reset) Input, this line is brought low to cause a Reset
ICM1A-ICM1B	I	ST	Yes	MCCP1 Capture Inputs A through B
TCKIA-TCKIB	I	ST	Yes	MCCP Timer Clock Inputs A through B
OCFA-OCFB	I	ST	Yes	MCCP Fault Inputs A through B
OCM1A-OCM1B	O	DIG	No	MCCP1 Outputs A through B
OCM2A-OCM2B	O	DIG	No	MCCP2 Outputs A through B
OCM3A-OCM3B	O	DIG	No	MCCP3 Outputs A through B
OCM4A-OCM4B	O	DIG	Yes	MCCP4 Outputs A through B
OCM5A-OCM5B	O	DIG	Yes	MCCP5 Outputs A through B
CLCINA-CLCIND CLC1OUT-CLC4OUT	I O	ST DIG	Yes Yes	CLC Inputs A through D CLC Outputs 1 through 4
OSCI OSCO	I O	Analog Analog	No No	Primary Oscillator Crystal Connection Input Primary Oscillator Crystal Connection Output
SOSCI SOSCO	I O	Analog Analog	No No	Secondary Oscillator Crystal Connection Input Secondary Oscillator Crystal Connection Output

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.....continued

Pin Name	Pin Type	Buffer Type	PPS	Description
CLKI CLKO	I O	ST DIG	No	Primary Oscillator Input (EC) CPU Clock Output
PGEC1	I	ST	No	ICSP™ Programming Clock 1
PGED1	I/O	DIG/ST	No	ICSP Programming Data 1
PGEC2	I	ST	No	ICSP Programming Clock 2
PGED2	I/O	DIG/ST	No	ICSP Programming Data 2
PGEC3	I	ST	No	ICSP Programming Clock 3
PGED3	I/O	DIG/ST	No	ICSP Programming Data 3
PWRLCLK	I	ST	No	Real-Time Clock 50/60 Hz Clock Input
$\overline{\text{TMPRN}}$	I	ST	Yes	Tamper Detect
PWRGT	O	DIG	Yes	RTCC Power Control
RTCC	O	DIG	Yes	RTCC Clock Output
REFO	O	DIG	Yes	Reference Clock Output
REFI	I	ST	Yes	Reference Clock Input
RA0-4, RA7-14	I/O	DIG/ST	No	PORTA Digital I/Os
RB0-15	I/O	DIG/ST	No	PORTB Digital I/Os
RC0-9, RC12-15	I/O	DIG/ST	No	PORTC Digital I/Os
RP0-RP33	I/O	DIG/ST	Yes	Remappable Peripherals (input or output)
RPI0-RPI29	I	ST	Yes	Remappable Peripherals (input only)
SCK1	I/O	ST	Yes	Synchronous Serial Clock Input/Output for SPI1
SDI1	I	ST	Yes	SPI1 Data In
SDO1	O	DIG	Yes	SPI1 Data Out
$\overline{\text{SS1}}$	I/O	ST	Yes	SPI1 Slave Synchronization or Frame Pulse I/O
SCK2	I/O	ST	Yes	Synchronous Serial Clock Input/Output for SPI2
SDI2	I	ST	Yes	SPI2 Data In
SDO2	O	DIG	Yes	SPI2 Data Out
$\overline{\text{SS2}}$	I/O	ST	Yes	SPI2 Slave Synchronization or Frame Pulse I/O
SCL1	I/O	DIG/I2C/SMB	No	I2C1 Synchronous Serial Clock Input/Output
SDA1	I/O	DIG/I2C/SMB	No	I2C1 Data Input/Output
ASCL1	I/O	DIG/I2C/SMB	No	Alternate I2C1 Synchronous Serial Clock Input/Output
ASDA1	I/O	DIG/I2C/SMB	No	Alternate I2C1 Data Input/Output
SCL2	I/O	DIG/I2C/SMB	No	I2C2 Synchronous Serial Clock Input/Output
SDA2	I/O	DIG/I2C/SMB	No	I2C2 Data Input/Output

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.....continued

Pin Name	Pin Type	Buffer Type	PPS	Description
$\overline{U1CTS}$	I	ST	Yes	UART1 Clear-to-Send
$\overline{U1RTS}$	O	DIG	Yes	UART1 Request-to-Send
U1RX	I	ST	Yes	UART1 Receive
U1TX	O	DIG	Yes	UART1 Transmit
$\overline{U2CTS}$	I	ST	Yes	UART2 Clear-to-Send
U2RTS	O	DIG	Yes	UART2 Request-to-Send
U2RX	I	ST	Yes	UART2 Receive
U2TX	O	DIG	Yes	UART2 Transmit
SCLKI	I	ST	No	Secondary Oscillator Clock Input
T1CK	I	ST	No	Timer1 Clock
T2CK-T3CK	I	ST	Yes	Timer2 through Timer3 Clock
TxCK	I	ST	Yes	Generic Timerx External Clock
TCK	I	ST	No	JTAG Test Clock/Programming Clock Input
TDI	I	ST	No	JTAG Test Data/Programming Data Input
TDO	O	DIG	No	JTAG Test Data Output
TMS	I	ST	No	JTAG Test Mode Select Input
V_{CAP}	P	—	No	External Filter Capacitor Connection (regulator enabled)
V_{DD}	P	—	No	Positive Supply for Peripheral Digital Logic and I/O Pins
$V_{REF}+$	I	Analog	No	Comparator and A/D Reference Voltage (high) Input
V_{SS}	P	—	No	Ground Reference for Peripheral Digital Logic and I/O Pins
D+	I/O	—		USB Signaling High
D-	I/O	—		USB Signaling Low
$\overline{USBOEN}$	I	DIG		USB Output Enable (active-low)
V_{BUS}	I	Analog		V_{USB} Supply Detect
V_{USB3V3}	P	—		3.3V V_{USB}
USBID	I	ST		USB OTG ID Input

Legend: DIG = Digital levels output, ST = Schmitt Trigger input buffer, I2C = I^2C/SMBus input buffer, Analog = Analog level input/output

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2. Guidelines for Getting Started with 16-Bit MCUs

2.1 Basic Connection Requirements

Getting started with the PIC24FJ64GP205/GU205 family of 16-bit microcontrollers requires attention to a minimal set of device pin connections before proceeding with development.

The following pins must always be connected:

- All V_{DD}, V_{USB3V3} and V_{SS} pins (see 2.2 Power Supply Pins)
- All AV_{DD} and AV_{SS} pins, regardless of whether or not the analog device features are used (see 2.2 Power Supply Pins)
- $\overline{MCLR}$ pin (see 2.3 Master Clear (MCLR) Pin)
- V_{CAP} pin (see 2.4 Voltage Regulator Pin (VCAP))

These pins must also be connected if they are being used in the end application:

- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see 2.5 ICSP Pins)
- OSCI and OSCO pins when an external oscillator is used (see 2.6 External Oscillator Pins)

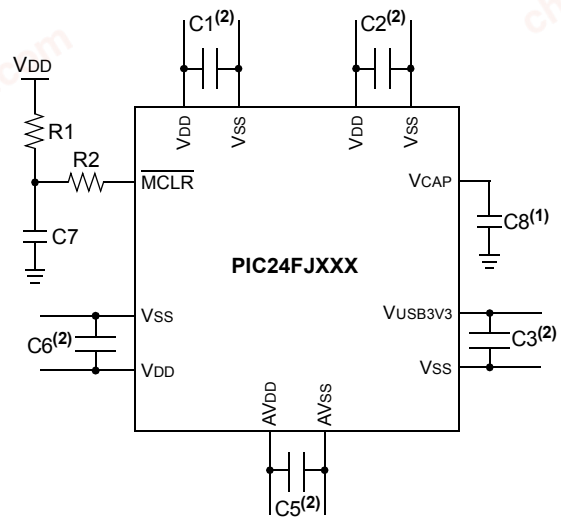
Additionally, the following pins may be required:

- V_{REF}+ pin used when external voltage reference for analog modules is implemented

Note: The AV_{DD} and AV_{SS} pins must always be connected, regardless of whether any of the analog modules are being used.

The minimum mandatory connections are shown in Figure 2-1.

Figure 2-1. Recommended Minimum Connections



Key (all values are recommendations):
C1 through C7: 0.1 µF, 20V ceramic
C8: 10 µF, 6.3V or greater, tantalum or ceramic
R1: 10 kΩ
R2: 100Ω to 470Ω

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Notes:

1. See 2.4 Voltage Regulator Pin (VCAP) for an explanation of voltage regulator pin connections.
2. The example shown is for a PIC24F device with five V_{DD}/V_{SS}, V_{USB3V3}/V_{SS} and AV_{DD}/AV_{SS} pin pairs. Other devices may have more or less pairs; adjust the number of decoupling capacitors appropriately.
3. These pins have an increased current drive strength.

2.2 Power Supply Pins

2.2.1 Decoupling Capacitors

The use of decoupling capacitors on every power supply pin, such as V_{DD}, V_{USB3V3} and AV_{DD}, is required.

Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: 0.1 µF (100 nF), 25V-50V capacitor is recommended. The capacitor should be a low-ESR device with a self-resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.
- Placement on the Printed Circuit Board: The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is no greater than 0.25 inch (6 mm).
- Handling high-frequency noise: If the board is experiencing high-frequency noise (upward of tens of MHz), add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to each primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (e.g., 0.1 µF in parallel with 0.001 µF).
- Maximizing performance: On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB trace
inductance.

2.2.2 Bulk Capacitors

On boards with power traces running longer than six inches in length, it is suggested to use a bulk capacitance of 10 µF or greater located near the MCU. The value of the capacitor should be determined based on the trace resistance that connects the power supply source to the device and the maximum current drawn by the device in the application. Typical values range from 10 µF to 47 µF.

2.3 Master Clear ($\overline{MCLR}$) Pin

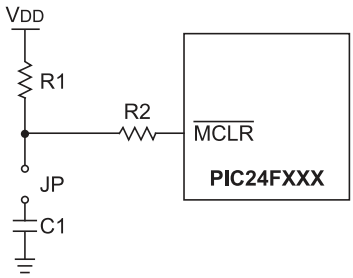
The $\overline{MCLR}$ pin provides two specific device functions: device Reset, and device programming and debugging. If programming and debugging are not required in the end application, a direct connection to V_{DD} may be all that is required. The addition of other components to help increase the application's resistance to spurious Resets from voltage sags may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{MCLR}$ pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, specific values of R1 and C1 will need to be adjusted based on the application and PCB requirements. For example, it is recommended that the capacitor, C1, be isolated from the $\overline{MCLR}$ pin during programming and debugging operations by using a jumper (Figure 2-2). The jumper is replaced for normal run-time operations.

Any components associated with the $\overline{MCLR}$ pin should be placed within 0.25 inch (6 mm) of the pin.

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Figure 2-2. Example of $\overline{MCLR}$ Pin Connections



Notes:

1. R1 ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the $\overline{MCLR}$ pin V_{IH} and V_{IL} specifications are met.
2. R2 ≤ 470Ω will limit any current flowing into $\overline{MCLR}$ from the external capacitor, C, in the event of a MCLR pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the $\overline{MCLR}$ pin V_{IH} and V_{IL} specifications are met.

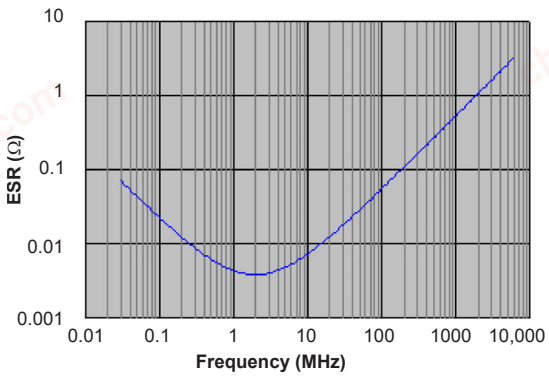
2.4 Voltage Regulator Pin (V_{CAP})

A low-ESR (< 5Ω) capacitor is required on the V_{CAP} pin to stabilize the voltage regulator output voltage. The V_{CAP} pin must not be connected to V_{DD} and must use a capacitor of 10 µF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in Table 2-1. Capacitors with equivalent specifications can be used.

Designers may use Figure 2-3 to evaluate the ESR equivalence of candidate devices.

The placement of this capacitor should be close to V_{CAP}. It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to 27.4 On-Chip Voltage Regulator for additional information.

Figure 2-3. Frequency vs. ESR Performance for Suggested V_{CAP}



Note: Typical data measurement at +25°C, 0V DC bias.

Table 2-1. Suitable Capacitor Equivalent (0805 Case Size)

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage
TDK Corporation	C2012X5R1E106K085AC	10 µF	±10%	25V
TDK Corporation	C2012X5R1C106K085AC	10 µF	±10%	16V
KEMET	C0805C106M4PACTU	10 µF	±10%	16V
Murata Electronics®	GRM21BR61E106KA3L	10 µF	±10%	25V
Murata Electronics	GRM21BR61C106KE15	10 µF	±10%	16V

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2.4.1 Considerations for Ceramic Capacitors

In recent years, large value, low-voltage, surface-mount ceramic capacitors have become very cost-effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the internal voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

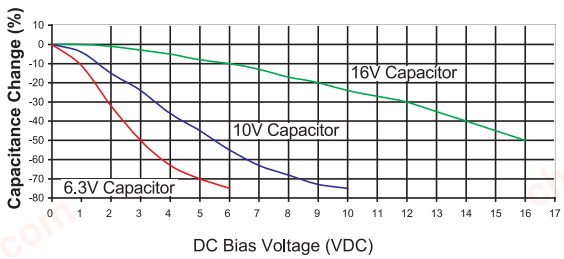
Typical low-cost, 10 µF ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as ±10% to ±20% (X5R and X7R) or -20%/+80% (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

The X5R and X7R capacitors typically exhibit satisfactory temperature stability (ex: ±15% over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of +22%/-82%. Due to the extreme temperature tolerance, a 10 µF nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum internal voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the internal regulator if the application must operate over a wide temperature range.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

A typical DC bias voltage vs. capacitance graph for X7R type capacitors is shown in Figure 2-4.

Figure 2-4. DC Bias Voltage vs. Capacitance Characteristics



When selecting a ceramic capacitor to be used with the internal voltage regulator, it is suggested to select a high-voltage rating so that the operating voltage is a small percentage of the maximum rated capacitor voltage. For example, choose a ceramic capacitor rated at a minimum of 16V for the 1.8V core voltage. Suggested capacitors are shown in Table 2-1.

2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of ohms, not to exceed 100Ω.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging.

For device emulation, ensure that the "Communication Channel Select" pins (i.e., PGECx/PGEDx) programmed into the device match the physical connections for the ICSP to the Microchip debugger/emulator tool.

For more information on available Microchip development tool connection requirements, refer to 28. Development Support.

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2.6 External Oscillator Pins

Many microcontrollers have options for at least two oscillators: a high-frequency Primary Oscillator and a low-frequency Secondary Oscillator (refer to 9. Oscillator Configuration for details).

The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins with no more than 0.5 inch (12 mm) between the circuit components and the pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

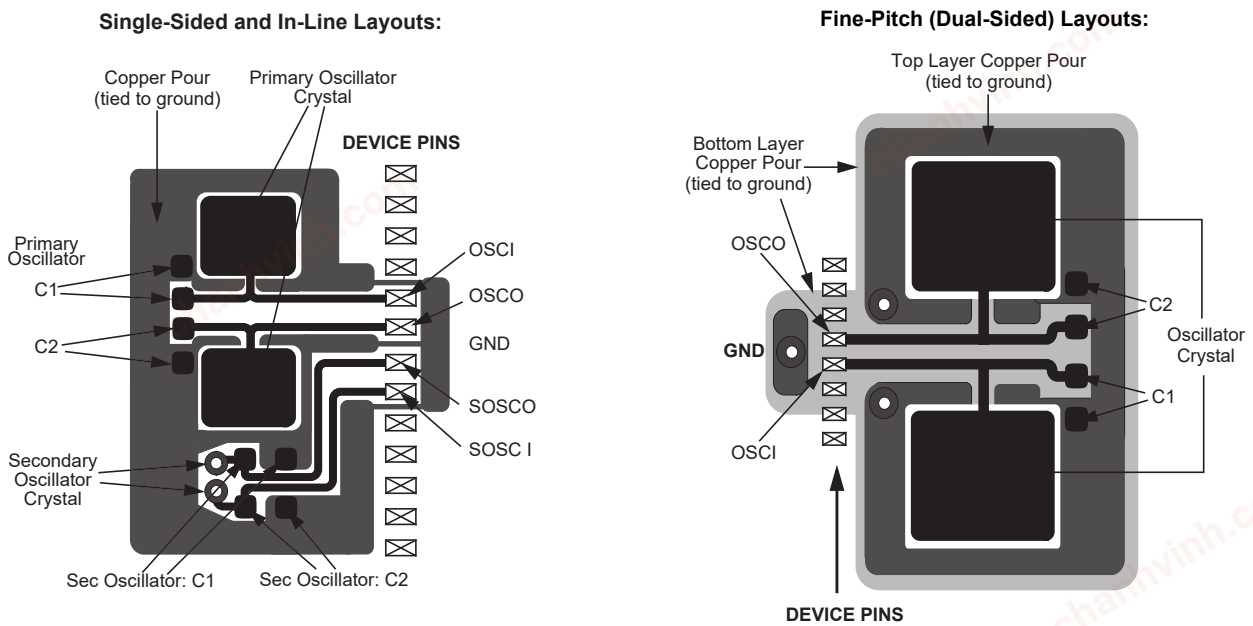
Layout suggestions are shown in Figure 2-5. In-line packages may be handled with a single-sided layout that completely encompasses the oscillator pins. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

In planning the application's routing and I/O assignments, ensure that adjacent port pins, and other signals in close proximity to the oscillator, are benign (i.e., free of high frequencies, short rise and fall times and other similar noise).

For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the corporate website (www.microchip.com):

- *AN943, "Practical PICmicro® Oscillator Analysis and Design"*
- *AN949, "Making Your Oscillator Work"*
- *AN1798, "Crystal Selection for Low-Power Secondary Oscillator"*

Figure 2-5. Suggested Placement of the Oscillator Circuit



2.7 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state. Alternatively, connect a 1 kΩ to 10 kΩ resistor to V_{SS} on unused pins.

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3. CPU

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the CPU, refer to **"CPU with Extended Data Space (EDS)"** (www.microchip.com/DS39732) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

The PIC24F CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set and a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M instructions of user program memory space. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double-word move (`MOV.D`) instruction and the table instructions. Overhead-free program loop constructs are supported using the `REPEAT` instructions, which are interruptible at any point.

PIC24F devices have sixteen, 16-bit Working registers in the programmer's model. Each of the Working registers can act as a Data, Address or Address Offset register. The 16th Working register (W15) operates as a Software Stack Pointer (SSP) for interrupts and calls.

The lower 32 Kbytes of the Data Space (DS) can be accessed linearly. The upper 32 Kbytes of the Data Space are referred to as Extended Data Space (EDS), to which the extended data RAM or program memory can be mapped.

The core supports Inherent (no operand), Relative, Literal and Memory Direct Addressing modes, along with three groups of addressing modes. All modes support Register Direct and various Register Indirect modes. Each group offers up to seven addressing modes. Instructions are associated with predefined addressing modes depending upon their functional requirements.

For most instructions, the core is capable of executing a data (or program data) memory read, a Working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing trinary operations (for example, A + B = C) to be executed in a single cycle.

A high-speed, 17-bit x 17-bit multiplier has been included to significantly enhance the core arithmetic capability and throughput. The multiplier supports Signed, Unsigned and Mixed mode, 16-bit x 16-bit or 8-bit x 8-bit, integer multiplication. All multiply instructions execute in a single cycle.

The 16-bit ALU has been enhanced with integer divide assist hardware that supports an iterative non-restoring divide algorithm. It operates in conjunction with the `REPEAT` instruction looping mechanism and a selection of iterative divide instructions to support 32-bit (or 16-bit), divided by 16-bit, integer signed and unsigned division. All divide operations require 19 cycles to complete but are interruptible at any cycle boundary.

The PIC24F has a vectored exception scheme with up to eight sources of non-maskable traps and up to 118 interrupt sources. Each interrupt source can be assigned to one of seven priority levels.

A block diagram of the CPU is shown in Figure 3-1.

3.1 Programmer's Model

The programmer's model for the PIC24F is shown in Figure 3-2. All registers in the programmer's model are memory-mapped and can be manipulated directly by instructions.

A description of each register is provided in Table 3-1. All registers associated with the programmer's model are memory-mapped.

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Figure 3-1. PIC24F CPU Core Block Diagram

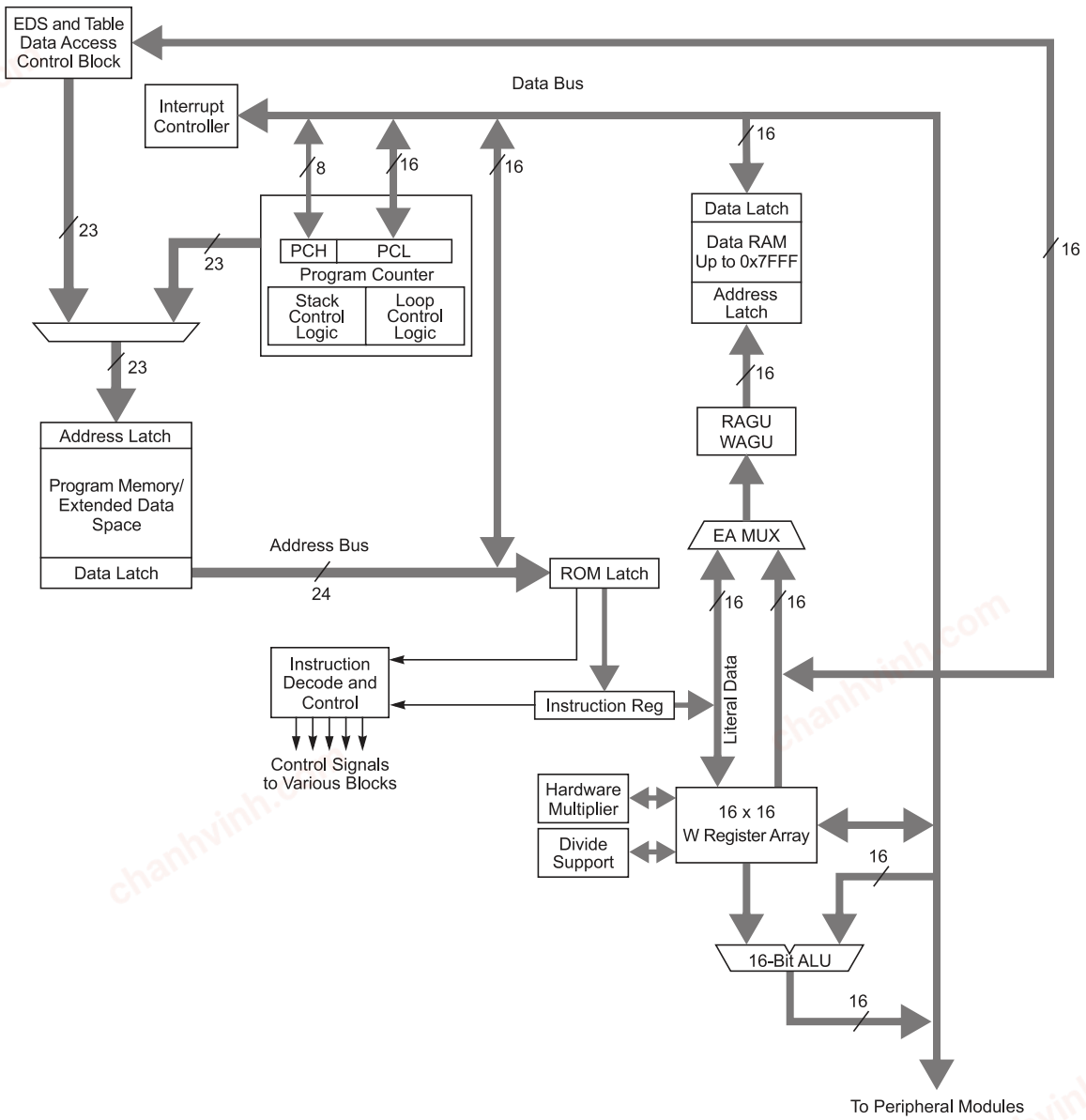


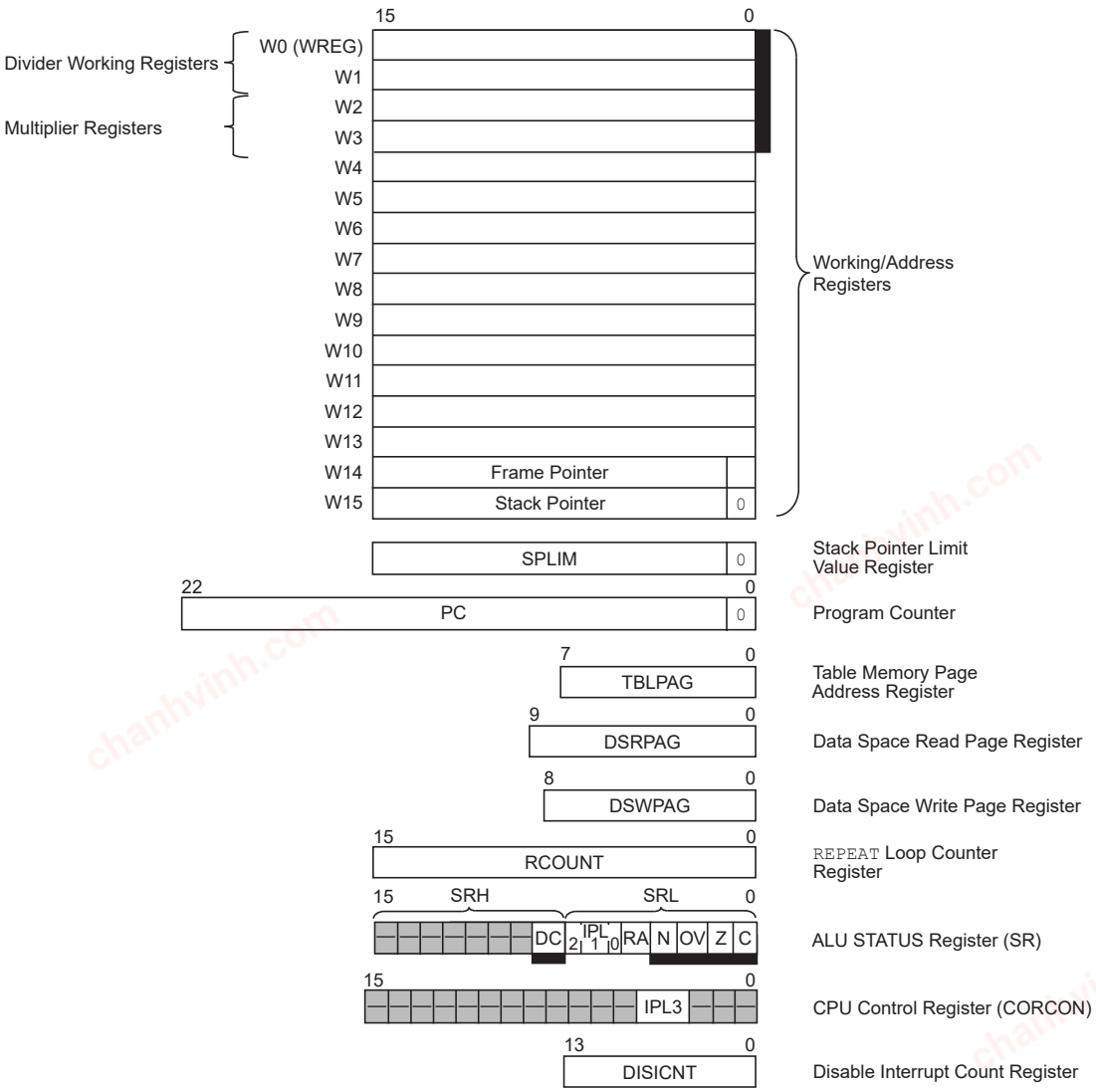
Table 3-1. CPU Core Registers

Register(s) Name	Description
W0 through W15	Working Register Array
PC	23-Bit Program Counter
SR	ALU STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register

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Register(s) Name	**Description**
RCOUNT	REPEAT Loop Counter Register
CORCON	CPU Control Register
DISICNT	Disable Interrupt Count Register
DSRPAG	Data Space Read Page Register
DSWPAG	Data Space Write Page Register

Figure 3-2. Programmer's Model



Registers or bits are shadowed for PUSH.S and POP.S instructions.

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3.2 Arithmetic Logic Unit (ALU)

The PIC24F ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. Depending on the operation, the ALU may affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array, or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

The PIC24F CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

3.2.1 Multiplier

The ALU contains a high-speed, 17-bit x 17-bit multiplier. It supports unsigned, signed or mixed sign operation in several multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

3.2.2 Divider

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 32-bit signed/16-bit signed divide
- 32-bit unsigned/16-bit unsigned divide
- 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. The 16-bit signed and unsigned `DIV` instructions can specify any W register for both the 16-bit divisor (Wn), and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.2.3 Multibit Shift Support

The PIC24F ALU supports both single bit and single-cycle, multibit arithmetic and logic shifts. Multibit shifts are implemented using a shifter block, capable of performing up to a 15-bit arithmetic right shift, or up to a 15-bit left shift, in a single cycle. All multibit shift instructions only support Register Direct Addressing for both the operand source and result destination.

A full summary of instructions that use the shift operation is provided in Table 3-2.

Table 3-2. Instructions that Use the Single Bit and Multibit Shift Operation

Instruction	Description
ASR	Arithmetic Shift Right source register by one or more bits.
SL	Shift Left source register by one or more bits.
LSR	Logical Shift Right source register by one or more bits.

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3.3 CPU Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	WREG0	7:0	WREG0[7:0]							
		15:8	WREG0[15:8]							
0x02	WREG1	7:0	WREG1[7:0]							
		15:8	WREG1[15:8]							
0x04	WREG2	7:0	WREG2[7:0]							
		15:8	WREG2[15:8]							
0x06	WREG3	7:0	WREG3[7:0]							
		15:8	WREG3[15:8]							
0x08	WREG4	7:0	WREG4[7:0]							
		15:8	WREG4[15:8]							
0x0A	WREG5	7:0	WREG5[7:0]							
		15:8	WREG5[15:8]							
0x0C	WREG6	7:0	WREG6[7:0]							
		15:8	WREG6[15:8]							
0x0E	WREG7	7:0	WREG7[7:0]							
		15:8	WREG7[15:8]							
0x10	WREG8	7:0	WREG8[7:0]							
		15:8	WREG8[15:8]							
0x12	WREG9	7:0	WREG9[7:0]							
		15:8	WREG9[15:8]							
0x14	WREG10	7:0	WREG10[7:0]							
		15:8	WREG10[15:8]							
0x16	WREG11	7:0	WREG11[7:0]							
		15:8	WREG11[15:8]							
0x18	WREG12	7:0	WREG12[7:0]							
		15:8	WREG12[15:8]							
0x1A	WREG13	7:0	WREG13[7:0]							
		15:8	WREG13[15:8]							
0x1C	WREG14	7:0	WREG14[7:0]							
		15:8	WREG14[15:8]							
0x1E	WREG15	7:0	WREG15[7:0]							
		15:8	WREG15[15:8]							
0x20	SPLIM	7:0	SPLIM[7:0]							
		15:8	SPLIM[15:8]							
0x22 ... 0x2D	Reserved									
0x2E	PCL	7:0	PCL[7:0]							
		15:8	PCL[15:8]							
0x30	PCH	7:0	PCH[7:0]							
		15:8								
0x32	DSRPAG	7:0	DSRPAG[7:0]							
		15:8							DSRPAG[9:8]	
0x33	DSWPAG	7:0	DSWPAG[7:0]							
		15:8								DSWPAG[8]
0x35	Reserved									
0x36	RCOUNT	7:0	RCOUNT[7:0]							
		15:8	RCOUNT[15:8]							
0x38 ... 0x41	Reserved									
0x42	SR	7:0		IPL[2:0]		RA	N	OV	Z	C
		15:8								DC
0x44	CORCON	7:0					IPL3	PSV		
		15:8								

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.....continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x46 ... 0x51	Reserved									
0x52	DISICNT	7:0	DISICNT[7:0]							
		15:8			DISICNT[13:8]					
0x54	TBLPAG	7:0	TBLPAG[7:0]							
		15:8								

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3.3.1 Working Register 0

Name: WREG0
Offset: 0x00

Bit	15	14	13	12	11	10	9	8
	WREG0[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WREG0[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – WREG0[15:0] Data bits

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3.3.2 Working Register 1

Name: WREG1
Offset: 0x02

Bit	15	14	13	12	11	10	9	8
	WREG1[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WREG1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – WREG1[15:0] Data bits

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3.3.3 Working Register 2

Name: WREG2
Offset: 0x04

Bit	15	14	13	12	11	10	9	8
	WREG2[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WREG2[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – WREG2[15:0] Data bits

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3.3.4 Working Register 3

Name: WREG3
Offset: 0x06

Bit	15	14	13	12	11	10	9	8
	WREG3[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WREG3[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – WREG3[15:0] Data bits

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3.3.5 Working Register 4

Name: WREG4
Offset: 0x08

Bit	15	14	13	12	11	10	9	8
	WREG4[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WREG4[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – WREG4[15:0] Data bits

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3.3.6 Working Register 5

Name: WREG5
Offset: 0x0A

Bit	15	14	13	12	11	10	9	8
	WREG5[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WREG5[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – WREG5[15:0] Data bits

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3.3.7 Working Register 6

Name: WREG6
Offset: 0x0C

Bit	15	14	13	12	11	10	9	8
	WREG6[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WREG6[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – WREG6[15:0] Data bits

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3.3.8 Working Register 7

Name: WREG7
Offset: 0x0E

Bit	15	14	13	12	11	10	9	8
	WREG7[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WREG7[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – WREG7[15:0] Data bits

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3.3.9 Working Register 8

Name: WREG8
Offset: 0x10

Bit	15	14	13	12	11	10	9	8
	WREG8[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WREG8[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – WREG8[15:0] Data bits

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3.3.10 Working Register 9

Name: WREG9
Offset: 0x12

Bit	15	14	13	12	11	10	9	8
	WREG9[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WREG9[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – WREG9[15:0] Data bits

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3.3.11 Working Register 10

Name: WREG10
Offset: 0x14

Bit	15	14	13	12	11	10	9	8
	WREG10[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WREG10[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – WREG10[15:0] Data bits

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3.3.12 Working Register 11

Name: WREG11
Offset: 0x16

Bit	15	14	13	12	11	10	9	8
	WREG11[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WREG11[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – WREG11[15:0] Data bits

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3.3.13 Working Register 12

Name: WREG12
Offset: 0x18

Bit	15	14	13	12	11	10	9	8
	WREG12[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WREG12[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – WREG12[15:0] Data bits

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3.3.14 Working Register 13

Name: WREG13
Offset: 0x1A

Bit	15	14	13	12	11	10	9	8
	WREG13[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WREG13[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – WREG13[15:0] Data bits

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3.3.15 Working Register 14

Name: WREG14
Offset: 0x1C

Bit	15	14	13	12	11	10	9	8
	WREG14[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WREG14[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – WREG14[15:0] Data or Frame Pointer bits

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3.3.16 Working Register 15

Name: WREG15
Offset: 0x1E

Bit	15	14	13	12	11	10	9	8
	WREG15[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WREG15[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – WREG15[15:0] Data or Stack Pointer bits

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3.3.17 Stack Pointer Limit Value Register

Name: SPLIM
Offset: 0x20

Bit	15	14	13	12	11	10	9	8
	SPLIM[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SPLIM[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – SPLIM[15:0] Stack Limit Address bits

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3.3.18 Program Counter Low Register

Name: PCL
Offset: 0x2E

Bit	15	14	13	12	11	10	9	8
	PCL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PCL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PCL[15:0] Program Counter Low Value bits

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3.3.19 Program Counter High Register

Name: PCH
Offset: 0x30

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	PCH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – PCH[7:0] Program Counter High Value bits

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3.3.20 Data Space Read Page Register

Name: DSRPAG
Offset: 0x32

Bit	15	14	13	12	11	10	9	8
							DSRPAG[9:8]	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	DSRPAG[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – DSRPAG[9:0] Data Space Read Page Value bits

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3.3.21 Data Space Write Page Register

Name: DSWPAG
Offset: 0x33

Bit	15	14	13	12	11	10	9	8
								DSWPAG[8]
Access								R/W
Reset								0

Bit	7	6	5	4	3	2	1	0
	DSWPAG[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 8:0 – DSWPAG[8:0] Data Space Write Page Value bits

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3.3.22 REPEAT Loop Counter Register

Name: RCOUNT
Offset: 0x36

Bit	15	14	13	12	11	10	9	8
	RCOUNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RCOUNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – RCOUNT[15:0] Current Loop Counter Value for `REPEAT` Instruction bits

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3.3.23 ALU STATUS Register

Name: SR
Offset: 0x42

Notes:

1. The IPLx Status bits are read-only when NSTDIS (INTCON1[15]) = 1.
2. The IPLx Status bits are concatenated with the IPL3 Status bit (CORCON[3]) to form the CPU Interrupt Priority Level (IPL). The value in parentheses indicates the IPL when IPL3 = 1.

Bit	15	14	13	12	11	10	9	8
								DC
Access								R/W
Reset								0

Bit	7	6	5	4	3	2	1	0
	IPL[2:0]			RA	N	OV	Z	C
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 8 – DC ALU Half Carry/Borrow bit

Value	Description
1	A carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred
0	No carry-out from the 4th or 8th low-order bit of the result has occurred

Bits 7:5 – IPL[2:0] CPU Interrupt Priority Level Status bits(1,2)

Value	Description
111	CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
110	SDOx pin is controlled by the module
101	CPU Interrupt Priority Level is 5 (13)
100	CPU Interrupt Priority Level is 4 (12)
011	CPU Interrupt Priority Level is 3 (11)
010	CPU Interrupt Priority Level is 2 (10)
001	CPU Interrupt Priority Level is 1 (9)
000	CPU Interrupt Priority Level is 0 (8)

Bit 4 – RA REPEAT Loop Active bit

Value	Description
1	REPEAT loop is in progress
0	REPEAT loop is not in progress

Bit 3 – N ALU Negative bit

Value	Description
1	Result was negative
0	Result was not negative (zero or positive)

Bit 2 – OV ALU Overflow bit

Value	Description
1	Overflow occurred for signed (two's complement) arithmetic in this arithmetic operation
0	No overflow has occurred

Bit 1 – Z ALU Zero bit

Value	Description
1	An operation, which affects the Z bit, has set it at some time in the past
0	The most recent operation, which affects the Z bit, has cleared it (i.e., a non-zero result)

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Bit 0 – C ALU Carry/Borrow bit

Value	Description
1	A carry-out from the Most Significant bit (MSb) of the result occurred
0	No carry-out from the Most Significant bit of the result occurred

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3.3.24 CPU Core Control Register

Name: CORCON
Offset: 0x44

Notes:

1. The IPL3 bit is concatenated with the IPL[2:0] bits (SR[7:5]) to form the CPU Interrupt Priority Level; see 3.3.23 SR for bit description.
2. If PSV = 0, any reads from data memory at 0x8000 and above will cause an address trap error instead of reading from the PSV section of program memory. This bit is not individually addressable.

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					IPL3	PSV		
Access					R/W	R/W		
Reset					0	0		

Bit 3 – IPL3 CPU Interrupt Priority Level Status bit(1)

Value	Description
1	CPU Interrupt Priority Level is greater than 7
0	CPU Interrupt Priority Level is 7 or less

Bit 2 – PSV Program Space Visibility (PSV) in Data Space Enable(2)

Value	Description
1	Program space is visible in Data Space
0	Program space is not visible in Data Space

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3.3.25 Disable Interrupt Count Register

Name: DISICNT
Offset: 0x52

Bit	15	14	13	12	11	10	9	8
			DISICNT[13:8]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DISICNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 13:0 – DISICNT[13:0] Current Counter Value for `DISI` Instruction bits

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3.3.26 Table Memory Page Address Register

Name: TBLPAG
Offset: 0x54

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	TBLPAG[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – TBLPAG[7:0] Table Memory Page Value bits

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4. Program Memory

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to **"PIC24F Flash Program Memory"** (www.microchip.com/DS30009715) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

As Harvard architecture devices, PIC24F microcontrollers feature separate program and data memory spaces and buses. This architecture also allows direct access of program memory from the Data Space during code execution.

The program memory is readable, writable and erasable. The Flash memory can be programmed in four ways:

- In-Circuit Serial Programming™ (ICSP™)
- Run-Time Self-Programming (RTSP)
- JTAG
- Enhanced In-Circuit Serial Programming (Enhanced ICSP)

ICSP allows a PIC24FJ64GP205/GU205 family device to be serially programmed while in the end application circuit. This is simply done with two lines for the programming clock and programming data (named PGECx and PGEDx, respectively), and three other lines for power (V_{DD}), ground (V_{SS}) and Master Clear ($\overline{MCLR}$). This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using `TBLRD` (Table Read) and `TBLWT` (Table Write) instructions. With RTSP, the user may write program memory data in blocks of 128 instructions (384 bytes) at a time and erase program memory in blocks of 1024 instructions (3072 bytes) at a time.

The device implements a 7-bit Error Correcting Code (ECC). The NVM block contains a logic to write and read ECC bits to and from the Flash memory. The Flash is programmed at the same time as the corresponding ECC parity bits. The ECC provides improved resistance to Flash errors. ECC single bit errors can be transparently corrected; ECC double-bit errors generate an interrupt.

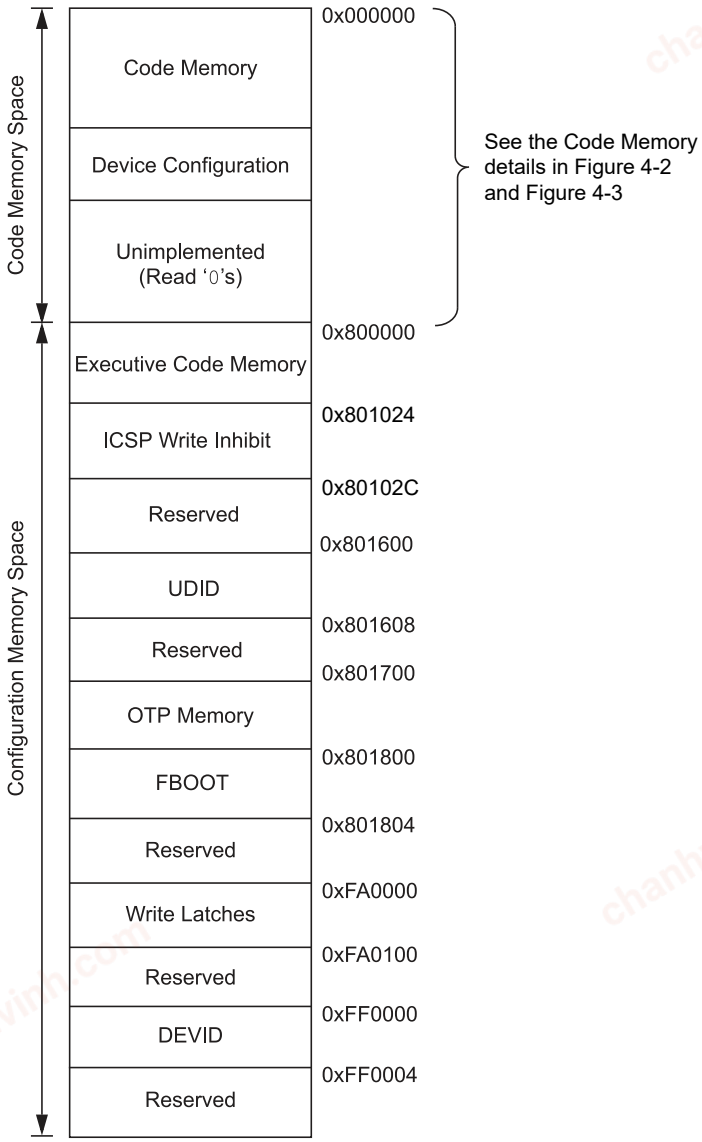
The program address memory space of the PIC24FJ64GP205/GU205 family devices is 4M instructions. The space is addressable by a 24-bit value derived from either the 23-bit Program Counter (PC) during program execution, or from table operation or Data Space remapping, as described in 5.5 Interfacing Program and Data Memory Spaces.

User access to the program memory space is restricted to the lower half of the address range (000000h to 7FFFFFh). The exception is the use of `TBLRD`/`TBLWT` operations, which use TBLPAG[7] to permit access to the Configuration bits and customer OTP sections of the configuration memory space.

The memory map for the PIC24FJ64GP205/GU205 family of devices is shown in Figure 4-1.

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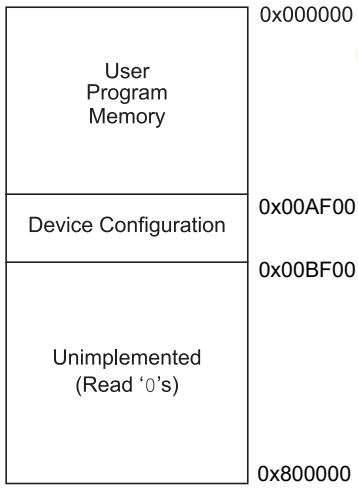
Figure 4-1. Program Memory Map for PIC24FJ64GP205/GU205 Family Devices



Note: Memory areas are not shown to scale.

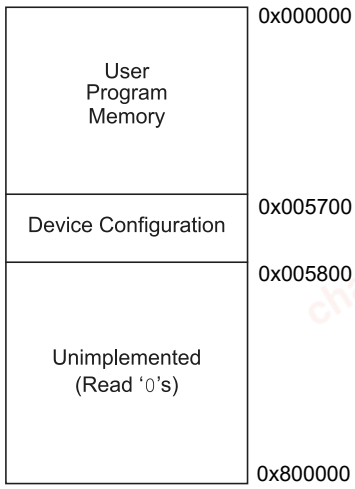
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Figure 4-2. Code Memory Map for Devices with 64 Kbytes Flash (PIC24FJ64GX2XX)



Note: Memory areas are not shown to scale

Figure 4-3. Code Memory Map for Devices with 32 Kbytes Flash (PIC24FJ32GX2XX)



Note: Memory areas are not shown to scale

4.1 Program Memory Organization

The program memory is organized as an array of 24-bit wide words. Although the program memory space is treated as 24 bits wide (3 bytes per instruction), the upper byte is not addressable. Only the lower 2 bytes of the words (instructions) have addresses. The entire 24-bits of the instruction words are read and decoded by the MCU. Also, the upper byte can be accessed from the application code using special table instructions (`TBLRD` and `TBLWT`).

The program memory array is organized into write blocks (rows) of 128 words (instructions). Eight write blocks form an erase block (page) of 1024 instructions. The program memory can be programmed one row (write block) at a time and can be erased by one page (erase block) at a time. Also, the double-word programming (two instructions) and entire code memory erase operations are supported.

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4.2 Hard Memory Vectors

All PIC24F devices reserve the addresses between 000000h and 000200h for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on a device Reset to the actual start of code. A `GOTO` instruction is programmed by the user at 000000h, with the actual address for the start of code at 000002h.

The PIC24FJ64GP205/GU205 devices can have up to two Interrupt Vector Tables (IVT). The first is located from addresses, 000004h to 0000FFh. The Alternate Interrupt Vector Table (AIVT) can be enabled by the AIVTDIS Configuration bit if the Boot Segment (BS) is present. If the user has configured a Boot Segment, the AIVT will be located at the address, ($\overline{\text{BSLIM}}$[12:0] – 1) x 800h. These vector tables allow each of the many device interrupt sources to be handled by separate ISRs. A more detailed discussion of the Interrupt Vector Tables is provided in Table 8-2.

4.3 Configuration Bits Overview

The Configuration bits are stored in the last page location of implemented program memory. These bits can be set or cleared to select various device configurations. There are two types of Configuration bits: system operation bits and code-protect bits. The system operation bits determine the power-on settings for system-level components, such as the oscillator and the Watchdog Timer. The code-protect bits prevent program memory from being read and written.

Refer to 27. Special Features for the full Configuration register description for each specific device.

4.4 Code-Protect Configuration Bits

The device implements intermediate security features defined by the FSEC register. The Boot Segment (BS) is the higher privileged segment and the General Segment (GS) is the lower privileged segment. The total user code memory can be split into BS or GS. The size of the segments is determined by the BSLIM[12:0] bits. The relative location of the segments within user space does not change, such that BS (if present) occupies the memory area just after the Interrupt Vector Table (IVT) and the GS occupies the space just after the BS (or if the Alternate IVT is enabled, just after it).

The Configuration Segment (CS) is a small segment (less than a page, typically just one row) within user Flash address space. It contains all user configuration data that are loaded by the NVM Controller during the Reset sequence.

4.5 Table Instructions and Flash Programming

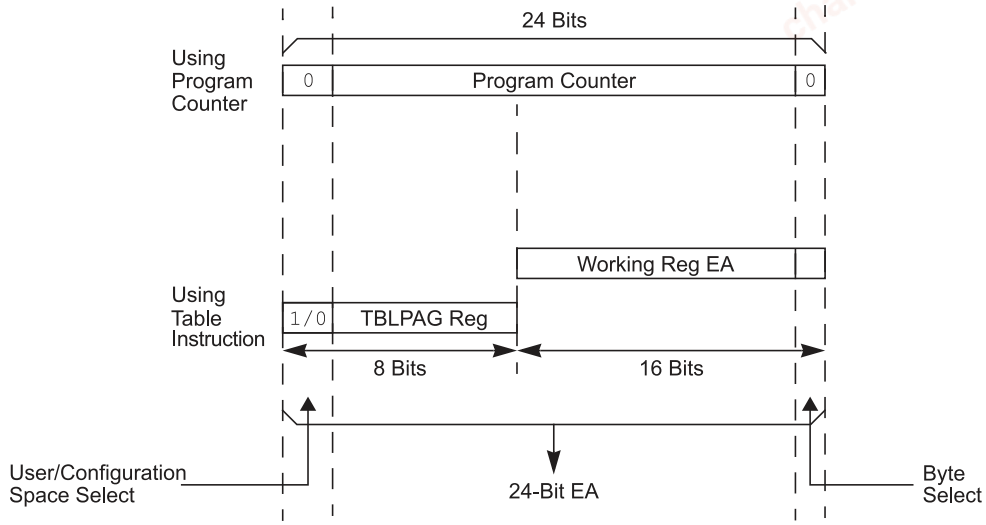
Regardless of the method used, all programming of Flash memory is done with the Table Read and Table Write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using the TBLPAG[7:0] bits and the Effective Address (EA) from a W register, specified in the table instruction, as shown in Figure 4-4.

The `TBLRDL` and the `TBLWTL` instructions are used to read or write to bits[15:0] of program memory. `TBLRDL` and `TBLWTL` can access program memory in both Word and Byte modes.

The `TBLRDH` and `TBLWTH` instructions are used to read or write to bits[23:16] of program memory. `TBLRDH` and `TBLWTH` can also access program memory in Word or Byte mode.

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Figure 4-4. Addressing for Table Registers



4.6 RTSP Operation

The PIC24F Flash program memory array is organized into rows of 128 instructions or 384 bytes. RTSP allows the user to erase blocks of eight rows (1024 instructions) at a time and to program one row at a time. It is also possible to program two instruction word blocks.

The eight-row erase blocks and single row write blocks are edge-aligned, from the beginning of program memory, on boundaries of 3072 bytes and 384 bytes, respectively.

When data are written to program memory using `TBLWT` instructions, the data are not written directly to memory. Instead, data written using Table Writes are stored in holding latches until the programming sequence is executed.

Any number of `TBLWT` instructions can be executed and a write will be successfully performed. However, 128 `TBLWT` instructions are required to write the full row of memory.

To ensure that no data are corrupted during a write, any unused address should be programmed with FFFFFFh. This is because the holding latches reset to an unknown state, so if the addresses are left in the Reset state, they may overwrite the locations on rows which were not rewritten.

The basic sequence for RTSP programming is to set the Table Pointer to point to the programming latches, do a series of `TBLWT` instructions to load the buffers and set the NVMADRU/NVMADR registers to point to the destination. Programming is performed by setting the control bits in the NVMCON register.

Data can be loaded in any order and the holding registers can be written to multiple times before performing a write operation. Subsequent writes, however, will wipe out any previous writes.

Note: Writing to a location multiple times without erasing is not allowed.

All of the Table Write operations are single-word writes (two instruction cycles), because only the buffers are written. A programming cycle is required for programming each row.

4.6.1 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. During a programming or erase operation, the processor stalls (waits) until the operation is finished. Setting the WR bit (NVMCON[15]) starts the operation and the WR bit is automatically cleared when the operation is finished.

4.6.2 Programming Algorithm for Flash Program Memory

The user can program one row of Flash program memory at a time. To do this, it is necessary to erase the eight-row erase block containing the desired row. The general process is:

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1. Read eight rows of program memory (1024 instructions) and store in data RAM.
2. Update the program data in RAM with the desired new data.
3. Erase the block (see Example 4-1):
   3.1. Set the NVMOP[3:0] bits (NVMCON[3:0]) to '0011' to configure for block erase. Set the WREN (NVMCON[14]) bit.
   3.2. Write the starting address of the block to be erased into the NVMADRU/NVMADR registers.
   3.3. Write 55h to NVMKEY.
   3.4. Write AAh to NVMKEY.
   3.5. Set the WR bit (NVMCON[15]). The erase cycle begins and the CPU stalls for the duration of the erase cycle. When the erase is done, the WR bit is cleared automatically.
4. Update the TBLPAG register to point to the programming latches on the device. Update the NVMADRU/NVMADR registers to point to the destination in the program memory.
5. Write the first 128 instructions from data RAM into the program memory buffers (see Example 4-2).
6. Write the program block to Flash memory:
   6.1. Set the NVMOPx bits to '0010' to configure for row programming. Set the WREN bit.
   6.2. Write 55h to NVMKEY.
   6.3. Write AAh to NVMKEY.
   6.4. Set the WR bit. The programming cycle begins and the CPU stalls for the duration of the write cycle. When the write to Flash memory is done, the WR bit is cleared automatically.
7. Repeat Steps 4 through 6, using the next available 128 instructions from the block in data RAM, by incrementing the value in NVMADRU/NVMADR until all 1024 instructions are written back to Flash memory.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPs.

Table 4-1. Page Erase

Step 1: Set the NVMCON register to erase a page.
`MOV #0x4003, W0` `MOV W0, NVMCON`
Step 2: Load the address of the page to be erased into the NVMADR register pair.

`MOV #PAGE_ADDR_LO, W0`
`MOV W0, NVMADR`
`MOV #PAGE_ADDR_HI, W0`
`MOV W0, NVMADRU`

Step 3: Set the WR bit.

`MOV #0x55, W0`
`MOV W0, NVMKEY`
`MOV #0xAA, W0`
`MOV W0, NVMKEY`
`BSET NVMCON, #WR`
`NOP`
`NOP`
`NOP`

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Example 4-1. Erasing a Program Memory Block ('C' Language Code)

```
// C example using MPLAB XC16
   unsigned long progAddr = 0xXXXXXX; // Address of row to write
   unsigned int offset;
//Set up pointer to the first memory location to be written
   NVMADRU = progAddr>>16;            // Initialize PM Page Boundary SFR
   NVMADR = progAddr & 0xFFFF;        // Initialize lower word of address
   NVMCON = 0x4003;                   // Initialize NVMCON
   asm("DISI #5");                    // Block all interrupts with priority <7
// for next 5 instructions
   __builtin_write_NVM();             // check function to perform unlock
                                      // sequence and set WR
```

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Table 4-2. Code Memory Programming Example: Row Writes

Step 1: Set the NVMCON register to program 128 instruction words.

```
MOV #0x4002, W0
MOV W0, NVMCON
```

Step 2: Initialize the TBLPAG register for writing to the latches.

```
MOV #0xFA, W12
MOV W12, TBLPAG
```

Step 3: Load W0:W5 with the next four instruction words to program.

```
MOV #<LSW0>, W0
MOV #<MSB1:MSB0>, W1
MOV #<LSW1>, W2
MOV #<LSW2>, W3
MOV #<MSB3:MSB2>, W4
MOV #<LSW3>, W5
```

Step 4: Set the Read Pointer (W6) and load the (next set of) write latches.

```
CLR W6
CLR W7
TBLWTL [W6++], [W7]
TBLWTH.B [W6++], [W7++]
TBLWTH.B [W6++], [++W7]
TBLWTL [W6++], [W7++]
TBLWTL [W6++], [W7]
TBLWTH.B [W6++], [W7++]
TBLWTH.B [W6++], [++W7]
TBLWTL [W6++], [W7++]
```

Step 5: Repeat Steps 4 and 5, for a total of 32 times, to load the write latches with 128 instructions.

Step 6: Set the NVMADRU/NVMADR register pair to point to the correct address.

```
MOV #DestinationAddress[15:0], W3
MOV #DestinationAddress[23:16], W4
MOV W3, NVMADR
MOV W4, NVMADRU
```

Step 7: Execute the WR bit unlock sequence and initiate the write cycle.

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```
MOV #0x55, W0
MOV W0, NVMKEY
MOV #0xAA, W0
MOV W0, NVMKEY
BSET NVMCON, #WR
NOP
NOP
NOP
```

Example 4-2. Example: Row Programming ('C' Language Code)

```
ROW PROGRAMMING ('C' LANGUAGE CODE)
   int varWord1L[128];
   int varWord1H[128];
   int targetWriteAddressL;          // bits[15:0]
   int targetWriteAddressH;          // bits[22:16]
   int i;
   NVMCON = 0x4002;                  // Set WREN and row program mode
   TBLPAG = 0xFA;
   NVMADRL = targetWriteAddressL;    // set target write address
   NVMADRH = targetWriteAddressH;
   for(i=0; i<128; i++)              // load write latches with data
   { // to be written
   __builtin_tblwtl( (i*2), varWord1L[i]);
   __builtin_tblwth( (i*2), varWord1H[i]);
   }
   __builtin_disi(5);               //Disable interrupts for NVM unlock
sequence
   __builtin_write_NVM();           // initiate write
```

4.6.3 Programming a Double Word of Flash Program Memory

If a Flash location has been erased, it can be programmed using Table Write instructions to write two instruction words (2 x 24-bit) into the write latch. The TBLPAG register is loaded with the address of the write latches and the NVMADRU/NVMADR registers are loaded with the address of the first of the two instruction words to be programmed. The `TBLWTL` and `TBLWTH` instructions write the desired data into the write latches. To configure the NVMCON register for a two-word write, set the NVMOPx bits (NVMCON[3:0]) to '`0001`'. The write is performed by executing the unlock sequence and setting the WR bit. An equivalent procedure in 'C', using the MPLAB® XC16 compiler and built-in hardware functions, is shown in Table 4-3.

Table 4-3. Programming a Double Word of Flash Program Memory

Step 1: Initialize the TBLPAG register for writing to the latches.
`MOV #0xFA, W12` `MOV W12, TBLPAG`
Step 2: Load W0:W2 with the next two packed instruction words to program.

`MOV #<LSW0>, W0`
`MOV #<MSB1:MSB0>, W1`
`MOV #<LSW1>, W2`

Step 3: Set the Read Pointer (W6) and Write Pointer (W7), and load the (next set of) write latches.

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```
CLR W6
CLR W7

TBLWTL [W6++], [W7]

TBLWTH.B [W6++], [W7++]

TBLWTH.B [W6++], [++W7]

TBLWTL.W [W6++], [W7++]
```

Step 4: Set the NVMADRU/NVMADR register pair to point to the correct address.

```
MOV #DestinationAddress[15:0], W3
MOV #DestinationAddress[23:16], W4

MOV W3, NVMADR

MOV W4, NVMADRU
```

Step 5: Set the NVMCON register to program two instruction words.

```
MOV #0x4001, W10
MOV W10, NVMCON

NOP
```

Step 6: Initiate the write cycle.

```
MOV #0x55, W1
MOV W1, NVMKEY

MOV #0xAA, W1

MOV W1, NVMKEY

BSET NVMCON, #WR

NOP

NOP

NOP
```

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Example 4-3. Programming a Double Word of Flash Program Memory ('C' Language Code)

```
// C example using MPLAB XC16
unsigned long progAddr = 0xXXXXXX;   // Address of word to program
unsigned int progData1L = 0xXXXX;    // Data to program lower word of word 1
unsigned char progData1H = 0xXX;     // Data to program upper byte of word 1
unsigned int progData2L = 0xXXXX;    // Data to program lower word of word 2
unsigned char progData2H = 0xXX;     // Data to program upper byte of word 2

//Set up NVMCON for word programming
NVMCON = 0x4001;                     // Initialize NVMCON
TBLPAG = 0xFA;                       // Point TBLPAG to the write latches

//Set up pointer to the first memory location to be written
NVMADRU = progAddr>>16;              // Initialize PM Page Boundary SFR
NVMADR = progAddr & 0xFFFF;          // Initialize lower word of address
//Perform TBLWT instructions to write latches
__builtin_tblwtl(0, progData1L);     // Write word 1 to address low word
__builtin_tblwth(0, progData2H);     // Write word 1 to upper byte
__builtin_tblwtl(1, progData2L);     // Write word 2 to address low word
__builtin_tblwth(1, progData2H);     // Write word 2 to upper byte
asm("DISI #5");                      // Block interrupts with priority <7 for
                                     // next 5 instructions

__builtin_write_NVM();               // XC16 function to perform unlock
sequence and set WR
```

4.7 Error Correcting Code (ECC)

In order to improve program memory performance and durability, these devices include Error Correcting Code (ECC) functionality as an integral part of the Flash memory controller. ECC can determine the presence of single bit errors in program data, including which bit is in error, and correct the data automatically without user intervention. ECC cannot be disabled.

When data are written to program memory, ECC generates a 7-bit Hamming code parity value for every two (24-bit) instruction words. The data are stored in blocks of 48 data bits and 7 parity bits; parity data are not memory-mapped and are inaccessible. When the data are read back, the ECC calculates the parity on them and compares them to the previously stored parity value. If a parity mismatch occurs, there are two possible outcomes:

- Single bit error has occurred and has been automatically corrected on read-back.
- Double-bit error has occurred and the read data are not changed.

The ECCSTATL register contains the parity information for single bit errors. The SECOUT[7:0] bits field contains the expected calculated SEC parity and the SECIN[7:0] bits contain the actual value from a Flash read operation. The SECSYNDx bits (ECCSTATH[7:0]) indicate the bit position of the single bit error within the 48-bit pair of instruction words. When no error is present, SECINx equals SECOUTx and the SECSYNDx bits are zero.

Double-bit error occurrences generate a generic hard trap and set the ECCDBE (INTCON4[1]) bit. The ECCSTATH register contains double-bit error status information. The DEDOUT bit is the expected calculated DED parity and DEDIN is the actual value from a Flash read operation. When no error is present, DEDIN equals DEDOUT.

4.7.1 ECC Fault Injection

To test Fault handling, an ECC error can be generated. Both single and double-bit errors can be generated in both the read and write data paths. Read path Fault injection first reads the Flash data and then modifies them prior to entering the ECC logic. Write path Fault injection modifies the actual data prior to them being written into the target Flash and will cause an EEC error on a subsequent Flash read. The following procedure is used to inject a Fault:

1. Load the Flash target address into the ECCADDR register.
2. Select 1st Fault bit determined by FLT1PTRx (ECCCONH[7:0]). The target bit is inverted to create the Fault.
3. If a double Fault is desired, select the 2nd Fault bit determined by FLT2PTRx (ECCCONH[15:8]); otherwise, set to all '1's.
4. Write the NVMKEY unlock sequence.

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5. Enable the ECC Fault injection logic by setting the FLTINJ bit (ECCCONL[0]).
6. Perform a read or write to the Flash target address.

4.8 Flash OTP by ICSP™ Write Inhibit

ICSP Write Inhibit is an access restriction feature that, when activated, restricts all of Flash memory. Once activated, ICSP Write Inhibit permanently prevents ICSP Flash programming and erase operations, and cannot be deactivated. This feature is intended to prevent alteration of Flash memory contents, with behavior similar to One-Time-Programmable (OTP) devices.

RTSP, including erase and programming operations, is not restricted when ICSP Write Inhibit is activated; however, code to perform these actions must be programmed into the device before ICSP Write Inhibit is activated. This allows for a bootloader-type application to alter Flash contents with ICSP Write Inhibit activated.

Entry into ICSP and Enhanced ICSP modes is not affected by ICSP Write Inhibit. In these modes, it will continue to be possible to read configuration memory space and any user memory space regions which are not code-protected. With ICSP writes inhibited, an attempt to set WR (NVMCON[15]) = 1 will maintain WR = 0 and instead, set WRERR (NVMCON[13]) = 1. All Enhanced ICSP erase and programming commands will have no effect with self-checked programming commands returning a FAIL response opcode (PASS if the destination already exactly matched the requested programming data).

Once ICSP Write Inhibit is activated, it is not possible for a device executing in Debug mode to erase/write Flash, nor can a debug tool switch the device to Production mode. ICSP Write Inhibit should therefore only be activated on devices programmed for production.

4.8.1 Activating Flash OTP by ICSP Write Inhibit

Note: It is not possible to deactivate ICSP Write Inhibit.

ICSP Write Inhibit is activated by executing a pair of NVMCON double-word programming commands to save two 16-bit activation values in the configuration memory space. The target NVM addresses and values required for activation are shown in Table 4-4. Once both addresses contain their activation values, ICSP Write Inhibit will take permanent effect on the next device Reset.

Only the lower 16 data bits stored at the activation addresses are evaluated; the upper eight bits and second 24-bit word, written by the double-word programming, should be written as '0's. The addresses can be programmed in any order and also during separate ICSP/Enhanced ICSP/RTSP sessions, but any attempt to program an incorrect 16-bit value, or use a row programming operation to program the values, will be aborted without altering the existing data.

Table 4-4. ICSP™ Write Inhibit Activation Addresses and Data

	Configuration Memory Address	ICSP Write Inhibit Activation Value
Write Lock 1	0x801024	0x006D63
Write Lock 2	0x801028	0x006870

4.9 JTAG Operation

The PIC24F family supports JTAG boundary scan. Boundary scan can improve the manufacturing process by verifying pin to PCB connectivity.

4.10 Enhanced In-Circuit Serial Programming

Enhanced In-Circuit Serial Programming uses an on-board bootloader, known as the Program Executive (PE), to manage the programming process. Using an SPI data frame format, the Program Executive can erase, program and verify program memory. For more information on Enhanced ICSP, see the device programming specification.

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4.11 Program Memory Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x075F	Reserved									
0x0760	NVMCON	7:0					NVMOP[3:0]			
		15:8	WR	WREN	WRERR	NVMSIDL	SFTSWP	P2ACTIV		
0x0762	NVMADR	7:0	NVMADR[7:0]							
		15:8	NVMADR[15:8]							
0x0764	NVMADRU	7:0	NVMADRU[7:0]							
		15:8								
0x0766	NVMKEY	7:0	NVMKEY[7:0]							
		15:8								
0x0768 ... 0x076B	Reserved									
0x076C	ECCCONL	7:0								FLTINJ
		15:8								
0x076E	ECCCONH	7:0	FLT1PTR[7:0]							
		15:8	FLT2PTR[7:0]							
0x0770	ECCADDRL	7:0	ECCADDR[7:0]							
		15:8	ECCADDR[15:8]							
0x0772	ECCADDRH	7:0	ECCADDR[23:16]							
		15:8								
0x0774	ECCSTATL	7:0	SECIN[7:0]							
		15:8	SECOUT[7:0]							
0x0774	ECCSTATH	7:0	SECSYND[7:0]							
		15:8							DEDOUT	DEDIN

4.11.1 Control Registers

There are four SFRs used to read and write the program Flash memory: NVMCON, NVMADRU, NVMADR and NVMKEY.

The NVMCON register (4.11.2 NVMCON) controls which blocks are to be erased, which memory type is to be programmed and when the programming cycle starts.

NVMKEY (4.11.5 NVMKEY) is a write-only register that is used for write protection. To start a programming or erase sequence, the user must consecutively write 55h and AAh to the NVMKEY register. Refer to 4.6.1 Programming Operations for further details.

The NVMADRU/NVMADR registers contain the upper byte and lower word of the destination of the NVM write or erase operation. Some operations (chip erase) operate on fixed locations and do not require an address value.

The ECCCONL/H, ECCADDRL/H and ECCSTATL/H registers control and allow capturing status information for the Error Correcting Code (ECC) feature.

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4.11.2 Nonvolatile Memory (NVM) Control Register

Name: NVMCON
Offset: 0x760

Notes:
1. These bits can only be reset on a Power-on Reset.
2. All other combinations of NVMOP[3:0] are unimplemented.
3. Unlock sequence must be executed before writing to this bit.

Legend: SO = Settable Only bit

Bit	15	14	13	12	11	10	9	8
	WR	WREN	WRERR	NVMSIDL	SFTSWP	P2ACTIV		
Access	R/SO	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					NVMOP[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – WR Write Control bit(1,3)

Value	Description
1	Initiates a Flash memory program or erase operation; the operation is self-timed and the bit is cleared by hardware once the operation is complete
0	Program or erase operation is complete and inactive

Bit 14 – WREN Write Enable bit(1)

Value	Description
1	Enables Flash program/erase operations
0	Inhibits Flash program/erase operations

Bit 13 – WRERR Write Sequence Error Flag bit(1)

Value	Description
1	An improper program or erase sequence attempt, or termination has occurred (bit is set automatically on any set attempt of the WR bit)
0	The program or erase operation completed normally

Bit 12 – NVMSIDL NVM Stop in Idle Control bit

Value	Description
1	Removes power from the program memory when device enters Idle mode
0	Powers program memory in Standby mode when the device enters Idle mode

Bit 11 – SFTSWP Soft Swap Status bit
In Single Partition Mode:
Read as '0'.
In Dual Partition Mode:

Value	Description
1	Partitions have been successfully swapped using the BOOTSWP instruction
0	Awaiting successful panel swap using the BOOTSWP instruction

Bit 10 – P2ACTIV Dual Partition Active Status bit
In Single Partition Mode:
Read as '0'.
In Dual Partition Mode:

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Value	Description
1	Partition 2 is mapped into the active region
0	Partition 1 is mapped into the active region

Bits 3:0 – NVMOP[3:0] NVM Operation Select bits(2)

Value	Description
1110	Chip Erase Operation, erases user memory (does not erase Device ID, customer OTP or executive memory)
1000	The next WR command will program FBOOT with the data held in the first 48 bits of the write latch and then will program the Dual Partition Signature (SIGN) bit in Flash. The device must be reset before the newly programmed mode can take effect.
0100	Erases user memory and Configuration Words in the Inactive Partition (Dual Partition modes only)
0011	Erases a page of program or executive memory
0010	Row programming operation
0001	Double-word programming operation

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4.11.3 Nonvolatile Memory (NVM) Write Address Low Register

Name: NVMADR
Offset: 0x762

Bit	15	14	13	12	11	10	9	8
	NVMADR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NVMADR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – NVMADR[15:0] Nonvolatile Memory Write Address Lower bits

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4.11.4 Nonvolatile Memory (NVM) Write Address High Register

Name: NVMADRU
Offset: 0x764

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	NVMADRU[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – NVMADRU[7:0] Nonvolatile Memory Write Address Upper bits

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4.11.5 Nonvolatile Memory (NVM) Key Register

Name: NVMKEY
Offset: 0x766

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	NVMKEY[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – NVMKEY[7:0] NVM Key Register bits (write-only)

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4.11.6 ECC Fault Injection Configuration Register Low

Name: ECCCONL
Offset: 0x76C

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
								FLTINJ
Access								R/W
Reset								0

Bit 0 – FLTINJ Fault Injection Sequence Enable bit
Write Enable bit.

Value	Description
1	Enabled
0	Disabled

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4.11.7 ECC Fault Injection Configuration Register High

Name: ECCCONH
Offset: 0x76E

Bit	15	14	13	12	11	10	9	8
	FLT2PTR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FLT1PTR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – FLT2PTR[7:0] ECC Fault Injection Bit Pointer 2 bits

Value	Description
11111111-10001001	No Fault injection occurs
10001000	Fault injection (bit inversion) occurs on bit 136 of ECC bit order
. . .	
00000001	Fault injection (bit inversion) occurs on bit 1 of ECC bit order
00000000	Fault injection (bit inversion) occurs on bit 0 of ECC bit order

Bits 7:0 – FLT1PTR[7:0] ECC Fault Injection Bit Pointer 1 bits

Value	Description
11111111-10001001	No Fault injection occurs
10001000	Fault injection (bit inversion) occurs on bit 136 of ECC bit order
. . .	
00000001	Fault injection (bit inversion) occurs on bit 1 of ECC bit order
00000000	Fault injection (bit inversion) occurs on bit 0 of ECC bit order

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4.11.8 ECC Fault Inject Address Compare Register Low

Name: ECCADDRL
Offset: 0x770

Bit	15	14	13	12	11	10	9	8
	ECCADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ECCADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ECCADDR[15:0] ECC Fault Injection NVM Address Match Compare bits

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4.11.9 ECC Fault Inject Address Compare Register High

Name: ECCADDRH
Offset: 0x772

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	ECCADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – ECCADDR[23:16] ECC Fault Injection NVM Address Match Compare bits

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4.11.10 ECC System Status Display Register Low

Name: ECCSTATL
Offset: 0x774

Bit	15	14	13	12	11	10	9	8
	SECOUT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SECIN[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – SECOUT[7:0] Calculated Single Error Correction Parity Value bits

Bits 7:0 – SECIN[7:0] Read Single Error Correction Parity Value bits
SECIN[7:0] bits are the actual parity value of a Flash read operation.

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4.11.11 ECC System Status Display Register High

Name: ECCSTATH
Offset: 0x774

Bit	15	14	13	12	11	10	9	8
							DEDOUT	DEDIN
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	SECSYND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 9 – DEDOUT Calculated Dual Bit Error Detection Parity bit

Bit 8 – DEDIN Read Dual Bit Error Detection Parity bit
DEDIN is the actual parity value of a Flash read operation.

Bits 7:0 – SECSYND[7:0] Calculated ECC Syndrome Value bits
Indicates the bit location that contains the error.

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5. Data Memory Space

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to **"Data Memory with Extended Data Space (EDS)"** (www.microchip.com/DS39733) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

The PIC24F core has a 16-bit wide data memory space, addressable as a single linear range. The Data Space is accessed using two Address Generation Units (AGUs), one each for read and write operations. The Data Space memory map is shown in Figure 5-1.

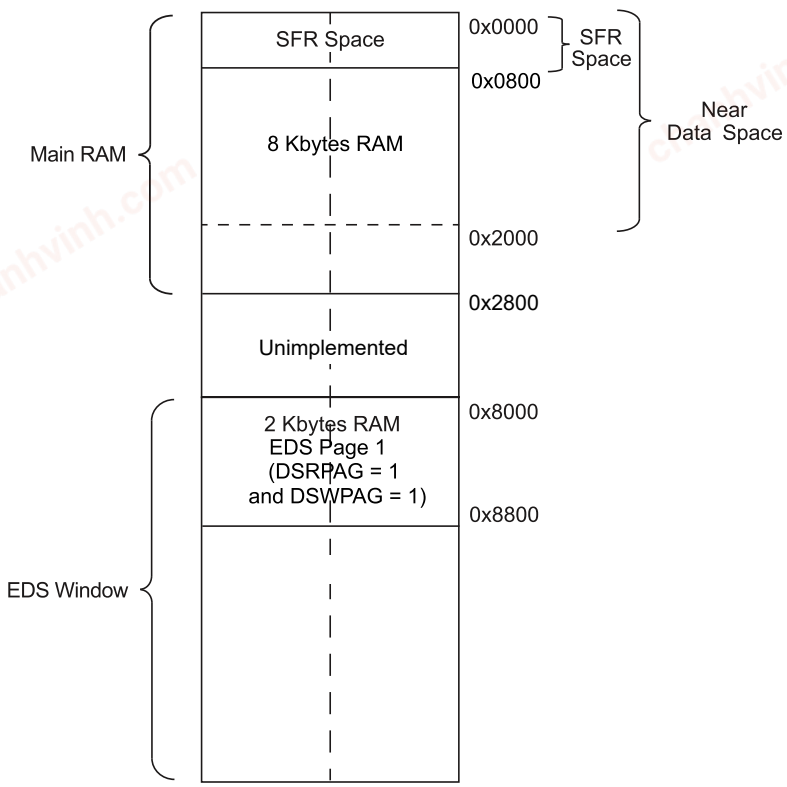
The 16-bit wide data addresses in the data memory space point to bytes within the Data Space (DS). This gives a DS address range of 64 Kbytes or 32K words. The lower half (0000h to 7FFFh) is used for implemented (on-chip) memory addresses.

The upper half of data memory address space (8000h to FFFFh) is used as a window into the Extended Data Space (EDS). This allows the microcontroller to directly access a greater range of data beyond the standard 16-bit address range. EDS is discussed in detail in 5.5 Interfacing Program and Data Memory Spaces.

5.1 Data Space Width

The data memory space is organized in byte-addressable, 16-bit wide blocks. Data are aligned in data memory and registers as 16-bit words, but all Data Space EAs resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses. The data memory map is shown in Figure 5-1.

Figure 5-1. Data Memory Map for PIC24FJ64GP205/GU205 Family Devices



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5.2 Data Memory Organization and Alignment

To maintain backward compatibility with PIC® MCUs and improve Data Space memory usage efficiency, the PIC24F instruction set supports both word and byte operations. As a consequence of byte accessibility, all EA calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode, [Ws++], will result in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

Data byte reads will read the complete word, which contains the byte, using the LSB of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel, byte-wide entities with shared (word) address decode, but separate write lines. Data byte writes only write to the corresponding side of the array or register which matches the byte address.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap will be generated. If the error occurred on a read, the instruction underway is completed; if it occurred on a write, the instruction will be executed but the write will not occur. In either case, a trap is then executed, allowing the system and/or user to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB. The Most Significant Byte (MSB) is not modified.

A Sign-Extend (`SE`) instruction is provided to allow users to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, users can clear the MSB of any W register by executing a Zero-Extend (`ZE`) instruction on the appropriate address.

Although most instructions are capable of operating on word or byte data sizes, it should be noted that some instructions operate only on words.

5.3 Near Data Space

The 8-Kbyte area, between 0000h and 1FFFh, is referred to as the Near Data Space. Locations in this space are directly addressable via a 13-bit absolute address field within all memory direct instructions. The remainder of the Data Space is addressable indirectly. Additionally, the whole Data Space is addressable using `MOV` instructions, which support Memory Direct Addressing with a 16-bit address field.

5.4 Special Function Register (SFR) Space

The first 2 Kbytes of the Near Data Space, from 0000h to 07FFh, are primarily occupied with Special Function Registers (SFRs). These are used by the PIC24F core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '`0`'. Each implemented area indicates a 32-byte region where at least one address is implemented as an SFR.

5.5 Interfacing Program and Data Memory Spaces

The PIC24F architecture uses a 24-bit wide program space and 16-bit wide Data Space. The architecture is also a modified Harvard scheme, meaning that data can also be present in the program space. To use these data successfully, they must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the PIC24F architecture provides two methods by which program space can be accessed during operation:

- Using table instructions to access individual bytes or words anywhere in the program space
- Remapping a portion of the program space into the Data Space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This makes the method ideal for accessing data tables that need to be updated from time to time. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis,

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which is ideal for look-ups from a large table of static data. It can only access the least significant word of the program word.

5.5.1 Addressing Program Space

Since the address ranges for the data and program spaces are 16 and 24 bits, respectively, a method is needed to create a 23-bit or 24-bit program address from 16-bit data registers. The solution depends on the interface method to be used.

For table operations, the 8-bit Table Memory Page Address register (TBLPAG) is used to define a 32K word region within the program space. This is concatenated with a 16-bit EA to arrive at a full 24-bit program space address. In this format, the MSBs of TBLPAG are used to determine if the operation occurs in the user memory (TBLPAG[7] = 0) or the configuration memory (TBLPAG[7] = 1).

For remapping operations, the 10-bit Extended Data Space Read register (DSRPAG) is used to define a 16K word page in the program space. When the Most Significant bit (MSb) of the EA is '1', and the MSb (bit 9) of DSRPAG is '1', the lower eight bits of DSRPAG are concatenated with the lower 15 bits of the EA to form a 23-bit program space address. The DSRPAG[8] bit decides whether the lower word (when the bit is '0') or the higher word (when the bit is '1') of program memory is mapped. Unlike table operations, this strictly limits remapping operations to the user memory area.

Table 5-1 and Figure 5-2 show how the program EA is created for table operations and remapping accesses from the data EA. Here, P[23:0] refers to a program space word, whereas D[15:0] refers to a Data Space word.

Table 5-1. Program Space Address Construction

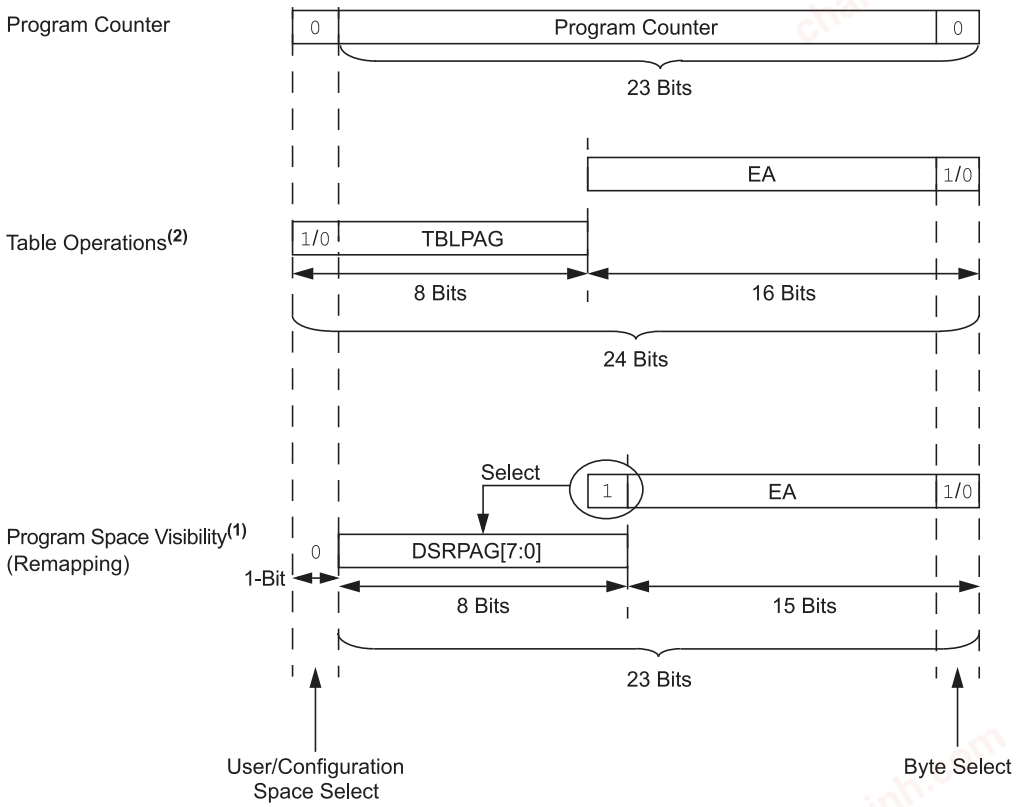
Access Type	Access Space	Program Space Address				
		[23]	[22:16]	[15]	[14:1]	[0]
Instruction Access (Code Execution)	User	0	PC[22:1]			0
		0xx xxxx xxxx xxxx xxxx xxx0				
TBLRD/TBLWT (Byte/Word Read/Write)	User	TBLPAG[7:0]		Data EA[15:0]		
		0xxx xxxx		xxxx xxxx xxxx xxxx		
	Configuration	TBLPAG[7:0]		Data EA[15:0]		
		1xxx xxxx		xxxx xxxx xxxx xxxx		
Program Space Visibility (Block Remap/Read)	User	0	DSRPAG[7:0](2)		Data EA[14:0](1)	
		0	xxxx xxxx		xxx xxxx xxxx xxxx	

Notes:

1. Data EA[15] is always '1' in this case, but is not used in calculating the program space address. Bit 15 of the address is DSRPAG[0].
2. DSRPAG[9] is always '1' in this case. DSRPAG[8] decides whether the lower word or higher word of program memory is read. When DSRPAG[8] is '0', the lower word is read and when it is '1', the higher word is read.

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Figure 5-2. Data Access from Program Space Address Generation



Notes:

1. DSRPAG[8] acts as word select. DSRPAG[9] should always be '1' to map program memory to data memory.
2. The instructions, TBLRDH/TBLWTH/TBLRDL/TBLWTL, decide if the higher or lower word of program memory is accessed. TBLRDH/TBLWTH instructions access the higher word and TBLRDL/TBLWTL instructions access the lower word. Table Read operations are permitted in the configuration memory space.

5.5.2 Data Access from Program Memory Using Table Instructions

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the program space without going through Data Space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper eight bits of a program space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two, 16-bit word-wide address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space which contains the least significant data word, and TBLRDH and TBLWTH access the space which contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from program space. Both function as either byte or word operations.

TBLRDL (Table Read Low): In Word mode, it maps the lower word of the program space location (P[15:0]) to a data address (D[15:0]).

In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when byte select is '1'; the lower byte is selected when it is '0'.

TBLRDH (Table Read High): In Word mode, it maps the entire upper word of a program address (P[23:16]) to a data address. Note that D[15:8], the 'phantom' byte, will always be '0'.

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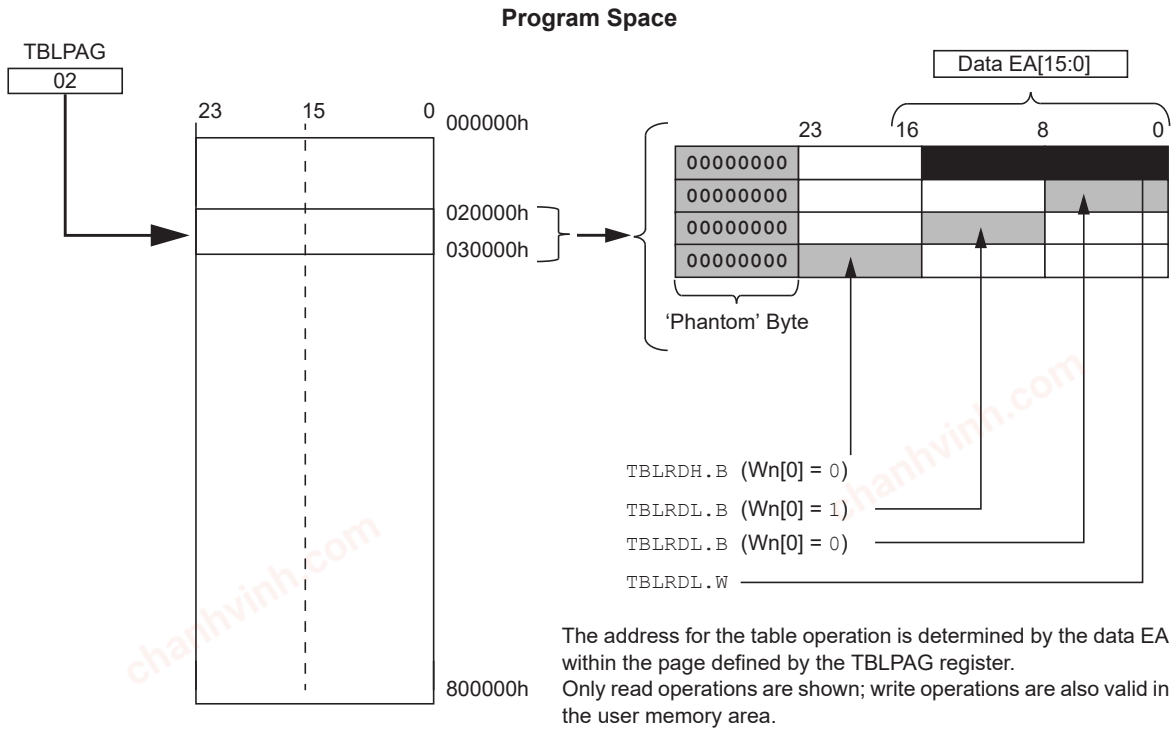
In Byte mode, it maps the upper or lower byte of the program word to D[7:0] of the data address, as above. Note that the data will always be '0' when the upper 'phantom' byte is selected (byte select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a program space address.

For all table operations, the area of program memory space to be accessed is determined by the Table Memory Page Address register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user and configuration spaces. When TBLPAG[7] = 0, the table page is located in the user memory space. When TBLPAG[7] = 1, the page is located in configuration space. The data access using table instructions is shown in Figure 5-3.

Note: Only Table Read operations will execute in the configuration memory space where Device IDs are located. Table Write operations are not allowed.

Figure 5-3. Access Program Memory with Table Instructions



5.5.3 Reading Data from Program Memory Using EDS

The upper 32 Kbytes of Data Space may optionally be mapped into any 16K word page of the program space. This provides transparent access of stored constant data from the Data Space without the need to use special instructions (i.e., TBLRDL/H).

Program space access through the Data Space occurs when the MSb of EA is '1' and the DSRPAG[9] bit is also '1'. The lower eight bits of DSRPAG are concatenated to the Wn[14:0] bits to form a 23-bit EA to access program memory. The DSRPAG[8] bit decides which word should be addressed; when the bit is '0', it is the lower word and when '1', the upper word of the program memory is accessed.

The entire program memory is divided into 512 EDS pages, from 200h to 3FFh, each consisting of 16K words of data. Pages, 200h to 2FFh, correspond to the lower words of the program memory, while 300h to 3FFh correspond to the upper words of the program memory.

Using this EDS technique, the entire program memory can be accessed. Previously, the access to the upper word of the program memory was not supported.

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Table 5-2 provides the corresponding 23-bit EDS address for program memory with EDS page and source addresses. EDS access is also explained in Figure 5-4 and Figure 5-5.

For operations that use PSV and are executed outside a REPEAT loop, the MOV and MOV.D instructions will require one instruction cycle in addition to the specified execution time. All other instructions will require two instruction cycles in addition to the specified execution time.

For operations that use PSV, which are executed inside a REPEAT loop, there will be some instances that require two instruction cycles in addition to the specified execution time of the instruction:

- Execution in the first iteration
- Execution in the last iteration
- Execution prior to exiting the loop due to an interrupt
- Execution upon re-entering the loop after an interrupt is serviced

Any other iteration of the REPEAT loop will allow the instruction accessing data, using PSV, to execute in a single cycle.

Table 5-2. EDS Program Address with Different Pages and Addresses

DSRPAG (Data Space Read Register)	Source Address while Indirect Addressing	23-Bit EA Pointing to EDS	Comment
200h • • • 2FFh	8000h to FFFFh	000000h to 007FFEh • • • 7F8000h to 7FFFFEh	Lower words of 4M program instructions (8 Mbytes) for read operations only.
300h • • • 3FFh		000001h to 007FFFh • • • 7F8001h to 7FFFFFh	Upper words of 4M program instructions (4 Mbytes remaining; 4 Mbytes are phantom bytes) for read operations only.
000h		Invalid Address	Address error trap.(1)

Note:
1. When the source/destination address is above 8000h and DSRPAG/DSWPAG is '0', an address error trap will occur.

Example 5-1. EDS Read Code from Program Memory in Assembly

```
; Set the EDS page from where the data to be read
   mov   #0x0202, w0
   mov   w0, DSRPAG   ;page 0x202, consisting lower words, is selected for read
   mov   #0x000A, w1  ;select the location (0x0A) to be read
   bset  w1, #15      ;set the MSB of the base address, enable EDS mode
;Read a byte from the selected location
   mov.b [w1++], w2   ;read Low byte
   mov.b [w1++], w3   ;read High byte
;Read a word from the selected location
   mov   [w1], w2     ;
;Read Double - word from the selected location
   mov.d [w1], w2     ;two word read, stored in w2 and w3
```

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Figure 5-4. Program Space Visibility Operation to Access Lower Word

When DSRPAG[9:8] = 10 and EA[15] = 1:

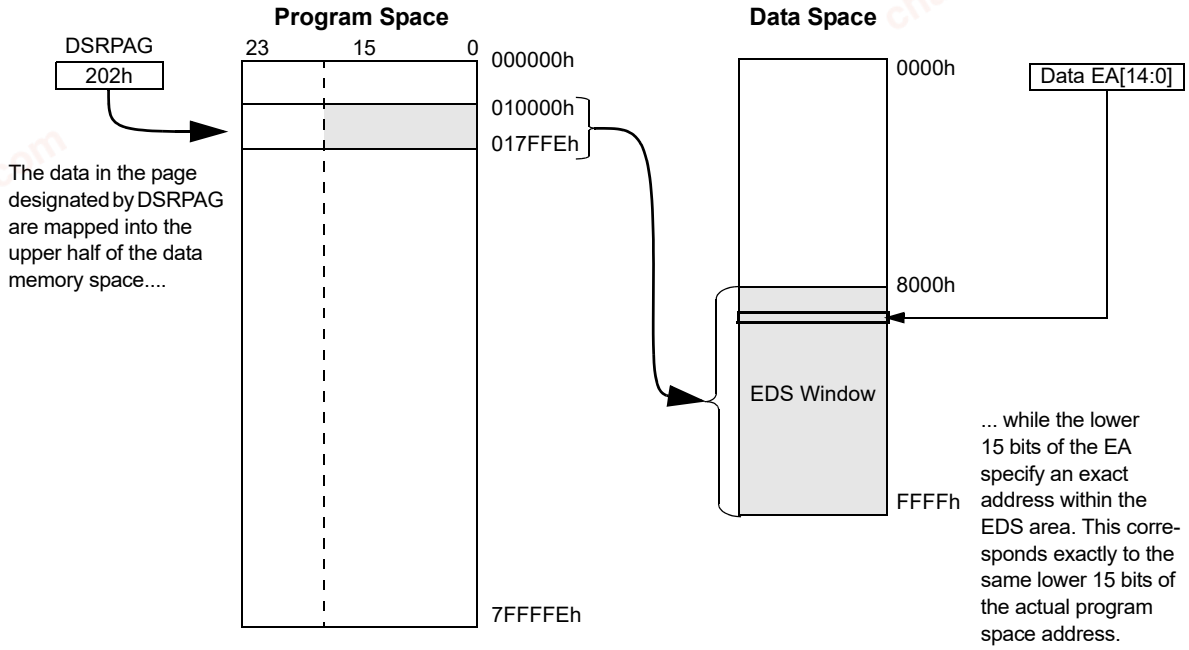
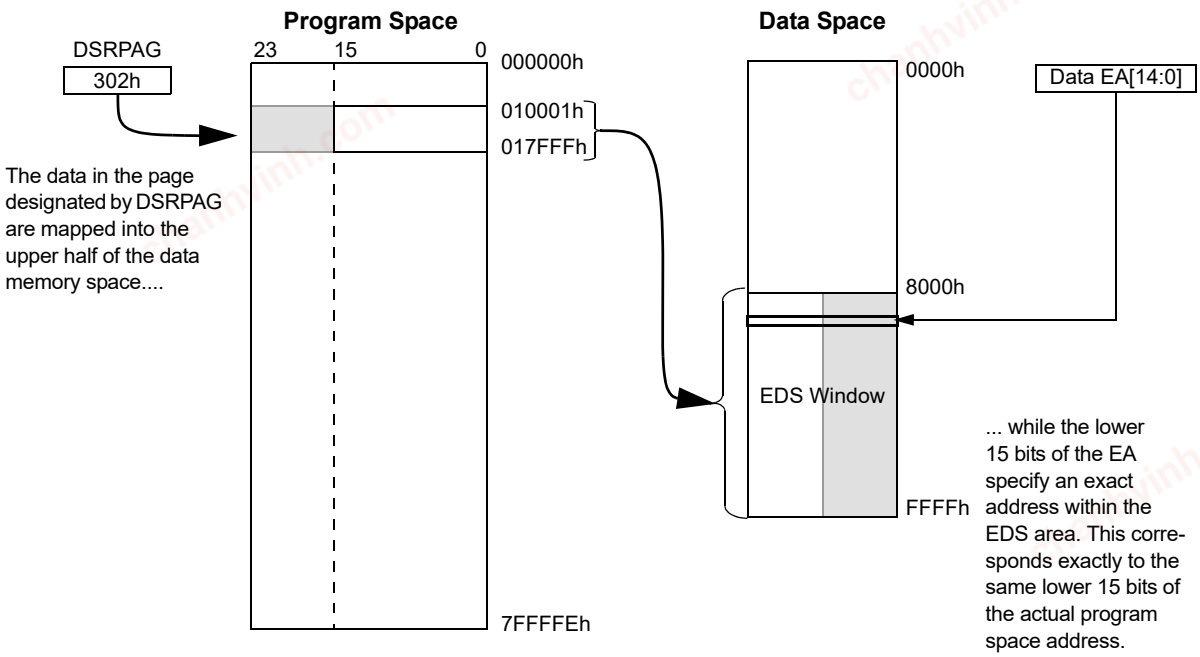


Figure 5-5. Program Space Visibility Operation to Access Upper Word

When DSRPAG[9:8] = 11 and EA[15] = 1:



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6. Direct Memory Access Controller (DMA)

Note: This data sheet summarizes the features of the PIC24FJ64GP205/GU205 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Direct Memory Access Controller (DMA)"** (www.microchip.com/DS30009742) in the *"dsPIC33/PIC24 Family Reference Manual"*). The information in this data sheet supersedes the information in the FRM.

The Direct Memory Access (DMA) Controller is designed to service high throughput data peripherals operating on the SFR bus, allowing them to access data memory directly and alleviating the need for CPU-intensive management. By allowing these data-intensive peripherals to share their own data path, the main data bus is also deloaded, resulting in additional power savings.

The DMA Controller functions both as a peripheral and a direct extension of the CPU. It is located on the microcontroller data bus between the CPU and DMA-enabled peripherals, with direct access to SRAM. This partitions the SFR bus into two buses, allowing the DMA Controller access to the DMA-capable peripherals located on the new DMA SFR bus. The controller serves as a Host device on the DMA SFR bus, controlling data flow from DMA-capable peripherals.

The controller also monitors CPU instruction processing directly, allowing it to be aware of when the CPU requires access to peripherals on the DMA bus and automatically relinquishing control to the CPU as needed. This increases the effective bandwidth for handling data without DMA operations causing a processor Stall. This makes the controller essentially transparent to the user.

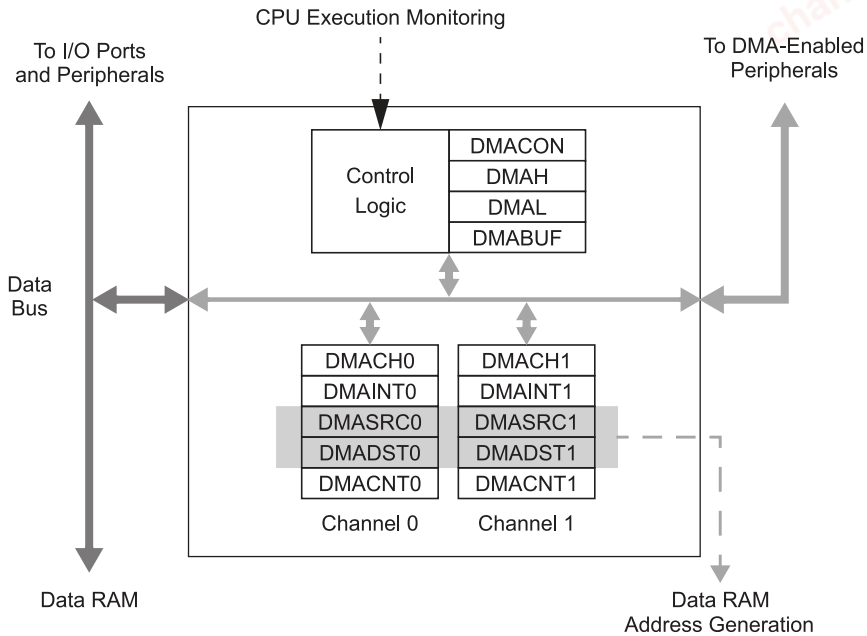
The DMA Controller has these features:

- Two Independent and Independently Programmable Channels
- Concurrent Operation with the CPU (no DMA caused Wait states)
- DMA Bus Arbitration
- Five Programmable Address modes
- Four Programmable Transfer modes
- Four Flexible Internal Data Transfer modes
- Byte or Word Support for Data Transfer
- 16-Bit Source and Destination Address Register for Each Channel, Dynamically Updated and Reloadable
- 16-Bit Transaction Count Register, Dynamically Updated and Reloadable
- Upper and Lower Address Limit Registers
- Counter Half-Full Level Interrupt
- Software Triggered Transfer
- Null Write mode for Symmetric Buffer Operations

A simplified block diagram of the DMA Controller is shown in Figure 6-1.

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Figure 6-1. DMA Functional Block Diagram



6.1 Summary of DMA Operations

The DMA Controller is capable of moving data between addresses according to a number of different parameters. Each of these parameters can be independently configured for any transaction; in addition, any or all of the DMA channels can independently perform a different transaction at the same time. Transactions are classified by these parameters:

- Source and destination (SFRs and data RAM)
- Data size (byte or word)
- Trigger source
- Transfer mode (One-Shot, Repeated or Continuous)
- Addressing modes (Fixed Address or Address Blocks, with or without Address Increment/ Decrement)

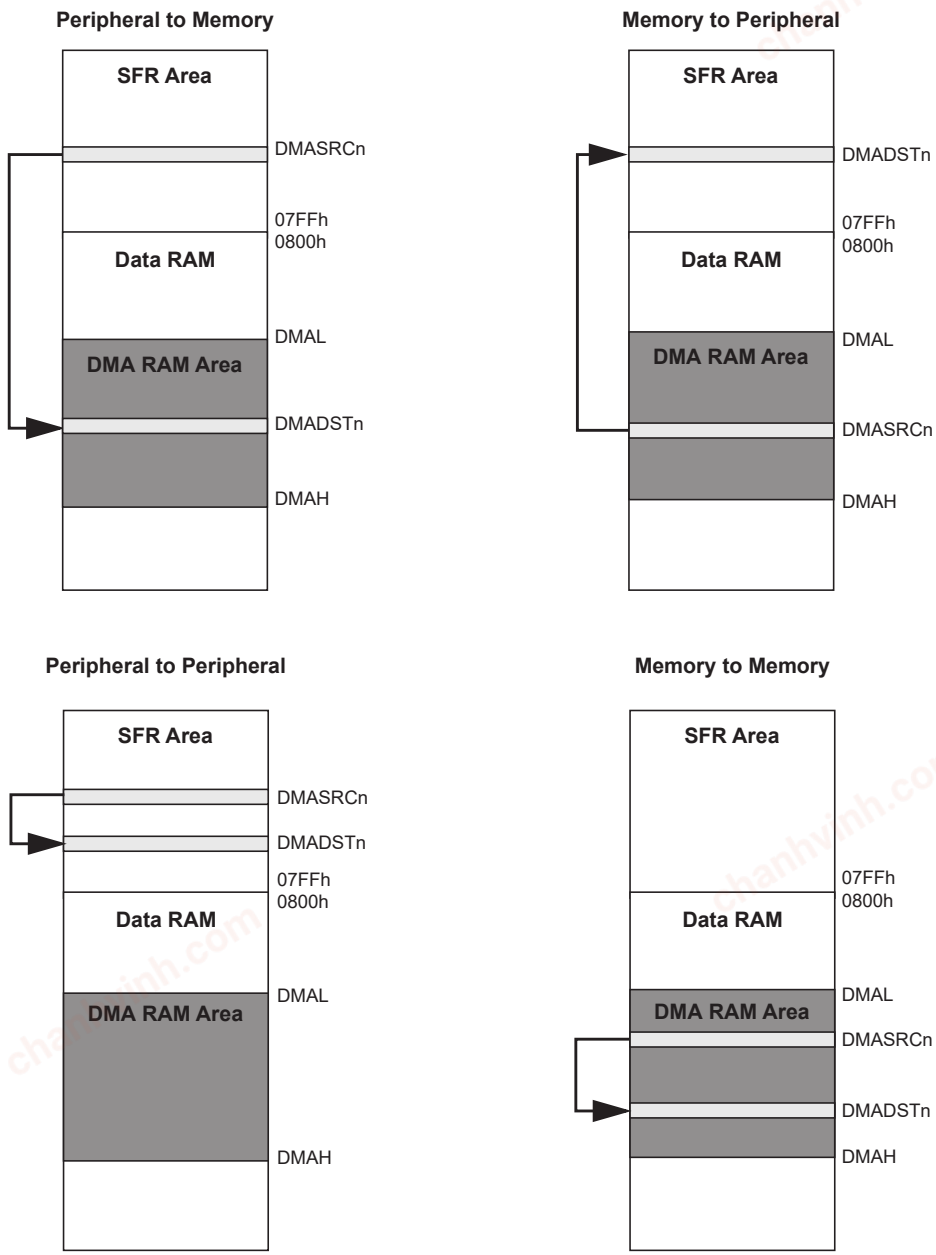
In addition, the DMA Controller provides channel priority arbitration for all channels.

6.1.1 Source and Destination

Using the DMA Controller, data may be moved between any two addresses in the Data Space. The SFR space (0000h to 07FFh), or the data RAM space (0800h to FFFFh), can serve as either the source or the destination. Data can be moved between these areas in either direction or between addresses in either area. The four different combinations are shown in Figure 6-2.

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Figure 6-2. Types of DMA Data Transfers



Note: Relative sizes of memory areas are not shown to scale.

If it is necessary to protect areas of data RAM, the DMA Controller allows the user to set upper and lower address boundaries for operations in the Data Space above the SFR space. The boundaries are set by the DMAH and DMAL Limit registers. If a DMA channel attempts an operation outside of the address boundaries, the transaction is terminated and an interrupt is generated.

6.1.2 Data Size

The DMA Controller can handle both 8-bit and 16-bit transactions. Size is user-selectable using the SIZE bit (DMACHn[1]). By default, each channel is configured for word-sized transactions. When byte-sized transactions are chosen, the LSb of the source and/or destination address determines if the data represent the upper or lower byte of the data RAM location.

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6.1.3 Trigger Source

The DMA Controller can use any one of the device's interrupt sources to initiate a transaction. The triggers for the DMA channels are selected by the CHSEL[6:0] bits in the DMAINTn registers. The DMA trigger sources are listed in Table 6-1.

Table 6-1. DMA Trigger Sources

CHSEL[6:0]	Trigger (Interrupt)	CHSEL[6:0]	Trigger (Interrupt)
7	MCCP5 IC/OC Interrupt	68	UART1 TX Interrupt
8	MCCP5 Timer Interrupt	69	UART1 RX Interrupt
9	MCCP4 IC/OC Interrupt	70	UART1 Error Interrupt
10	MCCP4 Timer Interrupt	71 ... 74	Reserved
11	MCCP3 IC/OC Interrupt		
12	MCCP3 Timer Interrupt		
13	MCCP2 IC/OC Interrupt		
14	MCCP2 Timer Interrupt		
15	MCCP1 IC/OC Interrupt	79	DMACHA1 Interrupt
16	MCCP1 Timer Interrupt	80	DMACHA0 Interrupt
17 ... 28	Reserved	81	ADC Interrupt
		82	USB Interrupt
		83	Reserved
		84	HLVD Interrupt
		85	CRC Interrupt
35	SPI2 Receive Interrupt	88	Reserved
36	SPI2 Transmit Interrupt	89	CLC4 Out
37	SPI2 General Interrupt	90	CLC3 Out
38	SPI1 Receive Interrupt	91	CLC2 Out
39	SPI1 Transmit Interrupt	92	CLC1 Out
40	SPI1 General Interrupt	93	Reserved
41 ... 43	Reserved	94	RTCC Alarm Interrupt
47	I2C2 Client Interrupt	98	TMR2 Interrupt
48	I2C2 Host Interrupt	99	TMR1 Interrupt
49	I2C2 Collision Interrupt	100	Reserved
50	I2C1 Client Interrupt	101	
51	I2C1 Host Interrupt	102	Reserved
52	I2C1 Collision Interrupt	103	Comparator Interrupt
		104	INT4 Interrupt
		105	INT3 Interrupt
		106	INT2 Interrupt
		107	INT1 Interrupt

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.....continued			
CHSEL[6:0]	Trigger (Interrupt)	CHSEL[6:0]	Trigger (Interrupt)
		108	INT0 Interrupt
		109	Interrupt-on-Change (IOC)
		110 ... 127	Reserved

Since the source and destination addresses for any transaction can be programmed independently of the trigger source, the DMA Controller can use any trigger to perform an operation on any peripheral. This also allows DMA channels to be cascaded to perform more complex transfer operations.

6.1.4 Transfer Mode

The DMA Controller supports four types of data transfers, based on the volume of data to be moved for each trigger.

- One-Shot: A single transaction occurs for each trigger.
- Continuous: A series of back-to-back transactions occur for each trigger; the number of transactions is determined by the DMACNTn transaction counter.
- Repeated One-Shot: A single transaction is performed repeatedly, once per trigger, until the DMA channel is disabled.
- Repeated Continuous: A series of transactions are performed repeatedly, one cycle per trigger, until the DMA channel is disabled.

All transfer modes allow the option to have the source and destination addresses, and counter value automatically reloaded after the completion of a transaction. Repeated mode transfers do this automatically.

6.1.5 Addressing Modes

The DMA Controller also supports transfers between single addresses or address ranges. The four basic options are:

- Fixed-to-Fixed: Between two constant addresses
- Fixed-to-Block: From a constant source address to a range of destination addresses
- Block-to-Fixed: From a range of source addresses to a single, constant destination address
- Block-to-Block: From a range of source addresses to a range of destination addresses

The option to select auto-increment or auto-decrement of source and/or destination addresses is available for Block Addressing modes.

In addition to the four basic modes, the DMA Controller also supports Peripheral Indirect Addressing (PIA) mode, where the source or destination address is generated jointly by the DMA Controller and a PIA-capable peripheral. When enabled, the DMA channel provides a base source and/or destination address, while the peripheral provides a fixed range offset address.

For PIC24FJ64GP205/GU205 family devices, the 12-bit A/D Converter module is the only PIA-capable peripheral. Details for its use in PIA mode are provided in 21. 12-Bit A/D Converter with Threshold Detect.

6.1.6 Channel Priority

Each DMA channel functions independently of the others, but also competes with the others for access to the data and DMA buses. When access collisions occur, the DMA Controller arbitrates between the channels using a user-selectable priority scheme. Two schemes are available:

- Round Robin: When two or more channels collide, the lower numbered channel receives priority on the first collision. On subsequent collisions, the higher numbered channels each receive priority based on their channel number.
- Fixed: When two or more channels collide, the lowest numbered channel always receives priority, regardless of past history; however, any channel being actively processed is not available for an immediate retrigger. If a higher priority channel is continually requesting service, it will be scheduled for service after the next lower priority channel with a pending request.

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6.2 Typical Setup

To set up a DMA channel for a basic data transfer:

1. Enable the DMA Controller (DMAEN = 1) and select an appropriate channel priority scheme by setting or clearing PRSSEL.
2. Program DMAH and DMAL with the appropriate upper and lower address boundaries for data RAM operations.
3. Select the DMA channel to be used and disable its operation (CHEN = 0).
4. Program the appropriate source and destination addresses for the transaction into the channel's DMASRCn and DMADSTn registers. For PIA mode addressing, use the base address value.
5. Program the DMACNTn register for the number of triggers per transfer (One-Shot or Continuous modes) or the number of words (bytes) to be transferred (Repeated modes).
6. Set or clear the SIZE bit to select the data size.
7. Program the TRMODE[1:0] bits to select the Data Transfer mode.
8. Program the SAMODE[1:0] and DAMODE[1:0] bits to select the addressing mode.
9. Enable the DMA channel by setting CHEN.
10. Enable the trigger source interrupt.

6.3 Peripheral Module Disable

Unlike other peripheral modules, the channels of the DMA Controller cannot be individually powered down using the Peripheral Module Disable (PMD) registers. Instead, the channels are controlled as two groups. The DMA03MD bit (PMD7[4]) selectively controls DMACH0 through DMACH3. Setting both bits effectively disables the DMA Controller.

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6.4 DMA Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x04C3	Reserved									
0x04C4	DMACON	7:0								PRSSEL
		15:8	DMAEN		DMASIDL					
0x04C6	DMABUF	7:0	DMABUF[7:0]							
		15:8	DMABUF[15:8]							
0x04C8	DMAL	7:0	LADDR[7:0]							
		15:8	LADDR[15:8]							
0x04CA	DMAH	7:0	HADDR[7:0]							
		15:8	HADDR[15:8]							
0x04CC	DMACH0	7:0	SAMODE[1:0]		DAMODE[1:0]		TRMODE[1:0]		SIZE	CHEN
		15:8				Reserved		NULLW	RELOAD	CHREQ
0x04CE	DMAINT0	7:0	HIGHIF	LOWIF	DONEIF	HALFIF	OVRUNIF			HALFEN
		15:8	DBUFWF	CHSEL[6:0]						
0x04D0	DMASRC0	7:0	SADDR[7:0]							
		15:8	SADDR[15:8]							
0x04D2	DMADST0	7:0	DADDR[7:0]							
		15:8	DADDR[15:8]							
0x04D4	DMACNT0	7:0	CNT[7:0]							
		15:8	CNT[15:8]							
0x04D6	DMACH1	7:0	SAMODE[1:0]		DAMODE[1:0]		TRMODE[1:0]		SIZE	CHEN
		15:8				Reserved		NULLW	RELOAD	CHREQ
0x04D8	DMAINT1	7:0	HIGHIF	LOWIF	DONEIF	HALFIF	OVRUNIF			HALFEN
		15:8	DBUFWF	CHSEL[6:0]						
0x04DA	DMASRC1	7:0	SADDR[7:0]							
		15:8	SADDR[15:8]							
0x04DC	DMADST1	7:0	DADDR[7:0]							
		15:8	DADDR[15:8]							
0x04DE	DMACNT1	7:0	CNT[7:0]							
		15:8	CNT[15:8]							

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6.4.1 DMA Engine Control Register

Name: DMACON
Offset: 0x4C4

Bit	15	14	13	12	11	10	9	8
	DMAEN		DMASIDL					
Access	R/W		R/W					
Reset	0		0					

Bit	7	6	5	4	3	2	1	0
								PRSSEL
Access								R/W
Reset								0

Bit 15 – DMAEN DMA Module Enable bit

Value	Description
1	Enables module
0	Disables module and terminates all active DMA operation(s)

Bit 13 – DMASIDL DMA Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode
0	Continues module operation in Idle mode

Bit 0 – PRSSEL Channel Priority Scheme Selection bit

Value	Description
1	Round robin scheme
0	Fixed priority scheme

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6.4.2 DMA Buffer Register

Name: DMABUF
Offset: 0x4C6

Bit	15	14	13	12	11	10	9	8
	DMABUF[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DMABUF[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – DMABUF[15:0] DMA Buffer bits

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6.4.3 DMA Low Address Limit Register

Name: DMAL
Offset: 0x4C8

Bit	15	14	13	12	11	10	9	8
	LADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – LADDR[15:0] DMA Low Address Limit bits

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6.4.4 DMA High Address Limit Register

Name: DMAH
Offset: 0x4CA

Bit	15	14	13	12	11	10	9	8
	HADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	HADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – HADDR[15:0] DMA High Address Limit bits

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6.4.5 DMA Channel 0 Control Register

Name: DMACH0
Offset: 0x4CC

Notes:
1. Only the original DMACNT0 is required to be stored to recover the original DMASRC0 and DMADST0 values.
2. DMACNT0 will always be reloaded in Repeated mode transfers, regardless of the state of the RELOAD bit.
3. The number of transfers executed while CHREQ is set depends on the configuration of TRMODE[1:0].

Legend: r = Reserved bit

Bit	15	14	13	12	11	10	9	8
				Reserved		NULLW	RELOAD	CHREQ
Access				r		R/W	R/W	R/W
Reset				0		0	0	0

Bit	7	6	5	4	3	2	1	0
	SAMODE[1:0]		DAMODE[1:0]		TRMODE[1:0]		SIZE	CHEN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 12 – Reserved Maintain as '0'.

Bit 10 – NULLW Null Write Mode bit

Value	Description
1	A dummy write is initiated to DMASRC0 for every write to DMADST0
0	No dummy write is initiated

Bit 9 – RELOAD Address and Count Reload bit(1)

Value	Description
1	DMASRC0, DMADST0 and DMACNT0 registers are reloaded to their previous values upon the start of the next operation
0	DMASRC0, DMADST0 and DMACNT0 are not reloaded on the start of the next operation(2)

Bit 8 – CHREQ DMA Channel Software Request bit(3)

Value	Description
1	A DMA request is initiated by software; automatically cleared upon completion of a DMA transfer
0	No DMA request is pending

Bits 7:6 – SAMODE[1:0] Source Address Mode Selection bits

Value	Description
11	Reserved
10	DMASRC0 is decremented based on the SIZE bit after a transfer completion
01	DMASRC0 is incremented based on the SIZE bit after a transfer completion
00	DMASRC0 remains unchanged after a transfer completion

Bits 5:4 – DAMODE[1:0] Destination Address Mode Selection bits

Value	Description
11	DMADST0 is used in Peripheral Indirect Addressing and remains unchanged
10	DMADST0 is decremented based on the SIZE bit after a transfer completion
01	DMADST0 is incremented based on the SIZE bit after a transfer completion
00	DMADST0 remains unchanged after a transfer completion

Bits 3:2 – TRMODE[1:0] Transfer Mode Selection bits

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Value	Description
11	Repeated Continuous mode
10	Continuous mode
01	Repeated One-Shot mode
00	One-Shot mode

Bit 1 – SIZE Data Size Selection bit

Value	Description
1	Byte (8-bit)
0	Word (16-bit)

Bit 0 – CHEN DMA Channel Enable bit

Value	Description
1	The corresponding channel is enabled
0	The corresponding channel is disabled

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6.4.6 DMA Channel 0 Interrupt Register

Name: DMAINT0
Offset: 0x4CE

Notes:
1. Setting these flags in software does not generate an interrupt.
2. Testing for address limit violations (DMASRC0 or DMADST0 is either greater than DMAH or less than DMAL) is NOT done before the actual access.

Bit	15	14	13	12	11	10	9	8
	DBUFWF	CHSEL[6:0]						
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	HIGHIF	LOWIF	DONEIF	HALFIF	OVRUNIF			HALFEN
Access	R/W	R/W	R/W	R/W	R/W			R/W
Reset	0	0	0	0	0			0

Bit 15 – DBUFWF DMA Buffered Data Write Flag bit(1)

Value	Description
1	The content of the DMA buffer has not been written to the location specified in DMADST0 or DMASRC0 in Null Write mode
0	The content of the DMA buffer has been written to the location specified in DMADST0 or DMASRC0 in Null Write mode

Bits 14:8 – CHSEL[6:0] DMA Channel Trigger Selection bits
See Table 6-1 for a complete list.

Bit 7 – HIGHIF DMA High Address Limit Interrupt Flag bit(1,2)

Value	Description
1	The DMA channel has attempted to access an address higher than DMAH or the upper limit of the data RAM space
0	The DMA channel has not invoked the high address limit interrupt

Bit 6 – LOWIF DMA Low Address Limit Interrupt Flag bit(1,2)

Value	Description
1	The DMA channel has attempted to access the DMA SFR address lower than DMAL, but above the SFR range (07FFh)
0	The DMA channel has not invoked the low address limit interrupt

Bit 5 – DONEIF DMA Complete Operation Interrupt Flag bit(1)

Value	Description
If CHEN = 1:	
1	The previous DMA session has ended with completion
0	The current DMA session has not yet completed
If CHEN = 0:	
1	The previous DMA session has ended with completion
0	The previous DMA session has ended without completion

Bit 4 – HALFIF DMA 50% Watermark Level Interrupt Flag bit(1)

Value	Description
1	DMACNT0 has reached the halfway point to 0000h
0	DMACNT0 has not reached the halfway point

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Bit 3 – OVRUNIF DMA Channel Overrun Flag bit(1)

Value	Description
1	The DMA channel is triggered while it's still completing the operation based on the previous trigger
0	The overrun condition has not occurred

Bit 0 – HALFEN Halfway Completion Watermark bit

Value	Description
1	Interrupts are invoked when DMACNT0 has reached its halfway point and at completion
0	An interrupt is invoked only at the completion of the transfer

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6.4.7 DMA Data Source Address Pointer 0 Register

Name: DMASRC0
Offset: 0x4D0

Bit	15	14	13	12	11	10	9	8
	SADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – SADDR[15:0] DMA Data Source Address Pointer bits

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6.4.8 DMA Data Source Address Pointer 0 Register

Name: DMADST0
Offset: 0x4D2

Bit	15	14	13	12	11	10	9	8
	DADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – DADDR[15:0] DMA Data Destination Address Pointer bits

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6.4.9 DMA Transaction Counter 0 Register

Name: DMACNT0
Offset: 0x4D4

Bit	15	14	13	12	11	10	9	8
	CNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CNT[15:0] DMA Transaction Counter bits

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6.4.10 DMA Channel 1 Control Register

Name: DMACH1
Offset: 0x4D6

Notes:
1. Only the original DMACNT1 is required to be stored to recover the original DMASRC1 and DMADST1 values.
2. DMACNT1 will always be reloaded in Repeated mode transfers, regardless of the state of the RELOAD bit.
3. The number of transfers executed while CHREQ is set depends on the configuration of TRMODE[1:0].

Legend: r = Reserved bit

Bit	15	14	13	12	11	10	9	8
				Reserved		NULLW	RELOAD	CHREQ
Access				r		R/W	R/W	R/W
Reset				0		0	0	0

Bit	7	6	5	4	3	2	1	0
	SAMODE[1:0]		DAMODE[1:0]		TRMODE[1:0]		SIZE	CHEN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 12 – Reserved Maintain as '0'.

Bit 10 – NULLW Null Write Mode bit

Value	Description
1	A dummy write is initiated to DMASRC1 for every write to DMADST1
0	No dummy write is initiated

Bit 9 – RELOAD Address and Count Reload bit(1)

Value	Description
1	DMASRC1, DMADST1 and DMACNT1 registers are reloaded to their previous values upon the start of the next operation
0	DMASRC1, DMADST1 and DMACNT1 are not reloaded on the start of the next operation(2)

Bit 8 – CHREQ DMA Channel Software Request bit(3)

Value	Description
1	A DMA request is initiated by software; automatically cleared upon completion of a DMA transfer
0	No DMA request is pending

Bits 7:6 – SAMODE[1:0] Source Address Mode Selection bits

Value	Description
11	Reserved
10	DMASRC1 is decremented based on the SIZE bit after a transfer completion
01	DMASRC1 is incremented based on the SIZE bit after a transfer completion
00	DMASRC1 remains unchanged after a transfer completion

Bits 5:4 – DAMODE[1:0] Destination Address Mode Selection bits

Value	Description
11	DMADST1 is used in Peripheral Indirect Addressing and remains unchanged
10	DMADST1 is decremented based on the SIZE bit after a transfer completion
01	DMADST1 is incremented based on the SIZE bit after a transfer completion
00	DMADST1 remains unchanged after a transfer completion

Bits 3:2 – TRMODE[1:0] Transfer Mode Selection bits

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Value	Description
11	Repeated Continuous mode
10	Continuous mode
01	Repeated One-Shot mode
00	One-Shot mode

Bit 1 – SIZE Data Size Selection bit

Value	Description
1	Byte (8-bit)
0	Word (16-bit)

Bit 0 – CHEN DMA Channel Enable bit

Value	Description
1	The corresponding channel is enabled
0	The corresponding channel is disabled

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6.4.11 DMA Channel 1 Interrupt Register

Name: DMAINT1
Offset: 0x4D8

Notes:
1. Setting these flags in software does not generate an interrupt.
2. Testing for address limit violations (DMASRC1 or DMADST1 is either greater than DMAH or less than DMAL) is NOT done before the actual access.

Bit	15	14	13	12	11	10	9	8
	DBUFWF	CHSEL[6:0]						
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	HIGHIF	LOWIF	DONEIF	HALFIF	OVRUNIF			HALFEN
Access	R/W	R/W	R/W	R/W	R/W			R/W
Reset	0	0	0	0	0			0

Bit 15 – DBUFWF DMA Buffered Data Write Flag bit(1)

Value	Description
1	The content of the DMA buffer has not been written to the location specified in DMADST1 or DMASRC1 in Null Write mode
0	The content of the DMA buffer has been written to the location specified in DMADST1 or DMASRC1 in Null Write mode

Bits 14:8 – CHSEL[6:0] DMA Channel Trigger Selection bits
See Table 6-1 for a complete list.

Bit 7 – HIGHIF DMA High Address Limit Interrupt Flag bit(1,2)

Value	Description
1	The DMA channel has attempted to access an address higher than DMAH or the upper limit of the data RAM space
0	The DMA channel has not invoked the high address limit interrupt

Bit 6 – LOWIF DMA Low Address Limit Interrupt Flag bit(1,2)

Value	Description
1	The DMA channel has attempted to access the DMA SFR address lower than DMAL, but above the SFR range (07FFh)
0	The DMA channel has not invoked the low address limit interrupt

Bit 5 – DONEIF DMA Complete Operation Interrupt Flag bit(1)

Value	Description
If CHEN = 1:	
1	The previous DMA session has ended with completion
0	The current DMA session has not yet completed
If CHEN = 0:	
1	The previous DMA session has ended with completion
0	The previous DMA session has ended without completion

Bit 4 – HALFIF DMA 50% Watermark Level Interrupt Flag bit(1)

Value	Description
1	DMACNT1 has reached the halfway point to 0000h
0	DMACNT1 has not reached the halfway point

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Bit 3 – OVRUNIF DMA Channel Overrun Flag bit(1)

Value	Description
1	The DMA channel is triggered while it's still completing the operation based on the previous trigger
0	The overrun condition has not occurred

Bit 0 – HALFEN Halfway Completion Watermark bit

Value	Description
1	Interrupts are invoked when DMACNT1 has reached its halfway point and at completion
0	An interrupt is invoked only at the completion of the transfer

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6.4.12 DMA Data Source Address Pointer 1 Register

Name: DMASRC1
Offset: 0x4DA

Bit	15	14	13	12	11	10	9	8
	SADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – SADDR[15:0] DMA Data Source Address Pointer bits

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6.4.13 DMA Data Source Address Pointer 1 Register

Name: DMADST1
Offset: 0x4DC

Bit	15	14	13	12	11	10	9	8
	DADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – DADDR[15:0] DMA Data Destination Address Pointer bits

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6.4.14 DMA Transaction Counter 1 Register

Name: DMACNT1
Offset: 0x4DE

Bit	15	14	13	12	11	10	9	8
	CNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CNT[15:0] DMA Transaction Counter bits

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7. Resets

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to **"Reset"** (www.microchip.com/DS39712) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

The Reset module combines all Reset sources and controls the device Master Reset Signal, $\overline{\text{SYSRST}}$. The following is a list of device Reset sources:

- POR: Power-on Reset
- $\overline{\text{MCLR}}$: Master Clear Pin Reset
- SWR: `RESET` Instruction
- WDT: Watchdog Timer Reset
- BOR: Brown-out Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Opcode Reset
- UWR: Uninitialized W Register Reset

A simplified block diagram of the Reset module is shown in Figure 7-1.

Any active source of Reset will make the $\overline{\text{SYSRST}}$ signal active. Many registers associated with the CPU and peripherals are forced to a known Reset state. Most registers are unaffected by a Reset; their status is unknown on POR and unchanged by all other Resets.

Note: Refer to the specific peripheral or CPU section of this manual for register Reset states.

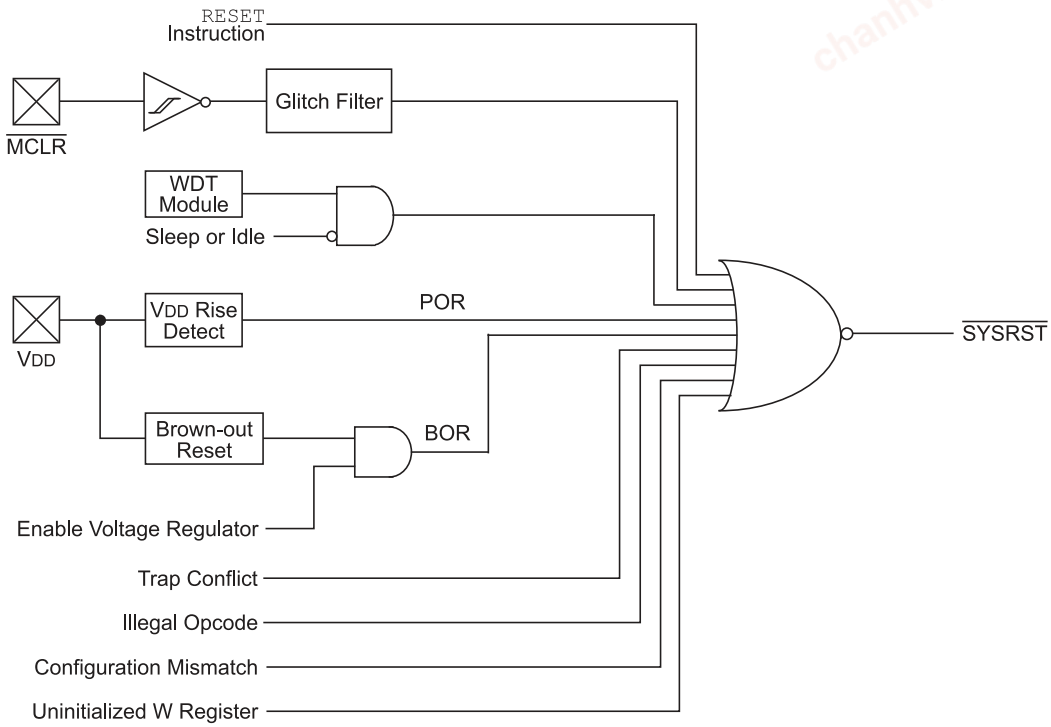
All types of device Reset will set a corresponding status bit in the RCON register to indicate the type of Reset (see 7.6.1 RCON(1,6)). A POR will clear all bits, except for the BOR and POR (RCON[1:0]) bits, which are set. The user may set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software will not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this data sheet.

Note: The status bits in the RCON register should be cleared after they are read so that the next RCON register values after a device Reset will be meaningful.

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Figure 7-1. Reset System Block Diagram



7.1 Special Function Register Reset States

Most of the Special Function Registers (SFRs) associated with the PIC24F CPU and peripherals are reset to a particular value at a device Reset. The SFRs are grouped by their peripheral or CPU function and their Reset values are specified in each section of this manual.

The Reset value for each SFR does not depend on the type of Reset, with the exception of four registers. The Reset value for the Reset Control register, RCON, will depend on the type of device Reset. The Reset value for the Oscillator Control register, OSCCON, will depend on the type of Reset and the programmed values of the FNOSC[2:0] bits in the FOSCSEL Flash Configuration Word. Some bits in the NVMCON register are only affected by a POR.

7.2 Device Reset Times

The Reset times for various types of device Reset are summarized in Table 7-1. Note that the Master Reset Signal, $\overline{\text{SYSRST}}$, is released after the POR delay time expires.

The time at which the device actually begins to execute code will also depend on the system oscillator delays, which include the Oscillator Start-up Timer (OST) and the PLL lock time. The OST and PLL lock times occur in parallel with the applicable $\overline{\text{SYSRST}}$ delay times.

The Fail-Safe Clock Monitor (FSCM) delay determines the time at which the FSCM begins to monitor the system clock source after the $\overline{\text{SYSRST}}$ signal is released.

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Table 7-1. Reset Delay Times for Various Device Resets

Reset Type	Clock Source	$\overline{SYSRST}$ Delay	System Clock Delay	Notes
POR	EC	$T_{POR} + T_{STARTUP} + T_{RST}$	—	**1, 2 , 3**
	ECPLL	$T_{POR} + T_{STARTUP} + T_{RST}$	T_{LOCK}	**1, 2, 3, 5**
	XT, HS, SOSC	$T_{POR} + T_{STARTUP} + T_{RST}$	T_{OST}	**1, 2, 3, 4**
	XTPLL, HSPLL	$T_{POR} + T_{STARTUP} + T_{RST}$	$T_{OST} + T_{LOCK}$	**1, 2, 3, 4, 5**
	FRC, OSCFDIV	$T_{POR} + T_{STARTUP} + T_{RST}$	T_{FRC}	**1, 2, 3, 6, 7**
	FRCPLL	$T_{POR} + T_{STARTUP} + T_{RST}$	$T_{FRC} + T_{LOCK}$	**1, 2, 3, 5, 6**
	LPRC	$T_{POR} + T_{STARTUP} + T_{RST}$	T_{LPRC}	**1, 2, 3, 6**
BOR	EC	$T_{STARTUP} + T_{RST}$	—	**2, 3**
	ECPLL	$T_{STARTUP} + T_{RST}$	T_{LOCK}	**2, 3, 5**
	XT, HS, SOSC	$T_{STARTUP} + T_{RST}$	T_{OST}	**2, 3, 4**
	XTPLL, HSPLL	$T_{STARTUP} + T_{RST}$	$T_{OST} + T_{LOCK}$	**2, 3, 4, 5**
	FRC, OSCFDIV	$T_{STARTUP} + T_{RST}$	T_{FRC}	**2, 3, 6, 7**
	FRCPLL	$T_{STARTUP} + T_{RST}$	$T_{FRC} + T_{LOCK}$	**2, 3, 5, 6**
	LPRC	$T_{STARTUP} + T_{RST}$	T_{LPRC}	**2, 3, 6**
$\overline{MCLR}$	Any Clock	T_{RST}	—	**3**
WDT	Any Clock	T_{RST}	—	**3**
Software	Any clock	T_{RST}	—	**3**
Illegal Opcode	Any Clock	T_{RST}	—	**3**
Uninitialized W	Any Clock	T_{RST}	—	**3**
Trap Conflict	Any Clock	T_{RST}	—	**3**

Note:

1. T_{POR} = Power-on Reset Delay (10 µs nominal).
2. $T_{STARTUP} = T_{VREG}$.
3. T_{RST} = Internal State Reset Time (2 µs nominal).
4. T_{OST} = Oscillator Start-up Timer (OST). A 10-bit counter counts 1024 oscillator periods before releasing the oscillator clock to the system.
5. T_{LOCK} = PLL Lock Time.
6. T_{FRC} and T_{LPRC} = RC Oscillator Start-up Times.
7. If Two-Speed Start-up is enabled, regardless of the Primary Oscillator selected, the device starts with FRC so the system clock delay is just T_{FRC}, and in such cases, FRC start-up time is valid; it switches to the Primary Oscillator after its respective clock delay.

7.3 Brown-out Reset (BOR)

PIC24FJ64GP205/GU205 family devices implement a BOR circuit that provides the user with several configuration and power-saving options. The BOR is controlled by the BOREN[1:0] (FPOR[1:0]) Configuration bits.

When BOR is enabled, any drop of V_{DD} below the BOR threshold results in a device BOR. Threshold levels are described in 30.2 DC Characteristics.

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7.4 Low-Power BOR

Low-Power BOR provides a downside protection when the main BOR controlled BOREN[1:0] Configuration bits are disabled.

Low-Power BOR re-arms the POR to ensure that the device will reset if V_{DD} drops below the POR threshold. The Low-Power BOR trip point is around 2.0V.

Low-Power BOR is selected in the configuration through the LPBOREN(FPOR[3]) bit. Because it is designed for very low-current consumption, the accuracy may vary slightly.

7.5 Clock Source at Reset

After Reset, the system clock source is always selected according to the Oscillator Configuration bits.

The oscillator start-up circuitry and its associated delay timers are not linked to the device Reset delays that occur at power-up. Some crystal circuits (especially low-frequency crystals) will have a relatively long start-up time. Therefore, one or more of the following conditions is possible after $\overline{\text{SYSRST}}$ is released:

- The oscillator circuit has not begun to oscillate.
- The Oscillator Start-up Timer has not expired (if a crystal oscillator is used).
- The PLL has not achieved a lock (if PLL is used).

The device will not begin to execute code until a valid clock source has been released to the system.

Therefore, the oscillator and PLL start-up delays must be considered when the Reset delay time must be known.

If the FSCM is enabled, it will begin to monitor the system clock source when $\overline{\text{SYSRST}}$ is released. If a valid clock source is not available at this time, the device will automatically switch to the FRC Oscillator and the user can switch to the desired crystal oscillator in the Trap Service Routine (TSR).

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7.6 Reset Register

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x010F	Reserved									
0x0110	RCON(1,6)	7:0	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR
		15:8	TRAPR	IOPUWR	SBOREN	RETEN			CM	VREGS

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7.6.1 Reset Control Register

Name: RCON(1,6)
Offset: 0x110

Notes:

1. All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
2. If the $\overline{\text{LPCFG}}$ Configuration bit is '1' (unprogrammed), the retention regulator is disabled and the RETEN bit has no effect.
3. Re-enabling the regulator after it enters Standby mode will add a delay, T_{VREG}, when waking up from Sleep. Applications that do not use the voltage regulator should set this bit to prevent this delay from occurring.
4. If the FWDTEN[1:0] Configuration bits are '11' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.
5. The BOREN[1:0] (FPOR[1:0]) Configuration bits must be set to '01' in order for SBOREN to have an effect.
6. On wake-up from Low-Voltage Sleep mode, RCON will have same value as a POR event.

Bit	15	14	13	12	11	10	9	8
	TRAPR	IOPUWR	SBOREN	RETEN			CM	VREGS
Access	R/W	R/W	R/W	R/W			R/W	R/W
Reset	0	0	1	0			0	0

Bit	7	6	5	4	3	2	1	0
	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	1	1

Bit 15 – TRAPR Trap Reset Flag bit

Value	Description
1	A Trap Conflict Reset has occurred
0	A Trap Conflict Reset has not occurred

Bit 14 – IOPUWR Illegal Opcode or Uninitialized W Register Access Reset Flag bit

Value	Description
1	An illegal opcode detection, an illegal address mode or Uninitialized W register used as an Address Pointer caused a Reset
0	An illegal opcode or Uninitialized W Register Reset has not occurred

Bit 13 – SBOREN Software Control Over the BOR Function bit(5)

Value	Description
1	BOR is enabled
0	BOR is disabled

Bit 12 – RETEN Retention Mode Enable bit(2)

Value	Description
1	Low-Voltage Regulator mode is enabled while device is in Sleep mode (1.2V regulator supplies to the core)
0	Low-Voltage Regulator mode is disabled

Bit 9 – CM Configuration Word Mismatch Reset Flag bit

Value	Description
1	A Configuration Word Mismatch Reset has occurred
0	A Configuration Word Mismatch Reset has not occurred

Bit 8 – VREGS Fast Wake-up from Sleep bit(3)

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Value	Description
1	Regulator Standby mode is disabled (fast wake-up, uses more power)
0	Regulator Standby mode is enabled (slow wake-up, uses less power)

Bit 7 – EXTR External Reset ($\overline{MCLR}$) Pin bit

Value	Description
1	A Master Clear (pin) Reset has occurred
0	A Master Clear (pin) Reset has not occurred

Bit 6 – SWR Software `RESET` (Instruction) Flag bit

Value	Description
1	A `RESET` instruction has been executed
0	A `RESET` instruction has not been executed

Bit 5 – SWDTEN Software Enable/Disable of WDT bit(4)

Value	Description
1	WDT is enabled
0	WDT is disabled

Bit 4 – WDTO Watchdog Timer Time-out Flag bit

Value	Description
1	WDT time-out has occurred
0	WDT time-out has not occurred

Bit 3 – SLEEP Wake-up from Sleep Flag bit

Value	Description
1	Device has been in Sleep mode
0	Device has not been in Sleep mode

Bit 2 – IDLE Wake-up from Idle Flag bit

Value	Description
1	Device has been in Idle mode
0	Device has not been in Idle mode

Bit 1 – BOR Brown-out Reset Flag bit

Value	Description
1	A Brown-out Reset has occurred (also set after a Power-on Reset)
0	A Brown-out Reset has not occurred

Bit 0 – POR Power-on Reset Flag bit

Value	Description
1	A Power-on Reset has occurred
0	A Power-on Reset has not occurred

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8. Interrupt Controller

This data sheet summarizes the features of the PIC24FJ64GP205/GU205 family devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Interrupts"** (www.microchip.com/DS70000600) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

The PIC24FJ64GP205/GU205 family interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the CPU.

The interrupt controller has the following features:

- Up to Eight Processor Exceptions and Software Traps
- Seven User-Selectable Priority Levels
- Interrupt Vector Table (IVT) with a Unique Vector for Each Interrupt or Exception Source
- Fixed Priority within a Specified User Priority Level
- Fixed Interrupt Entry and Return Latencies

8.1 Interrupt Vector Table

The PIC24FJ64GP205/GU205 family Interrupt Vector Table (IVT), shown in Figure 8-1, resides in program memory starting at location, 000004h. The IVT contains non-maskable trap vectors and interrupt vectors. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 takes priority over interrupts at any other vector address.

8.1.1 Alternate Interrupt Vector Table

The Alternate Interrupt Vector Table (AIVT) is located after the IVT, as shown in Figure 8-1. The AIVTEN (INTCON2[8]) control bit provides access to the AIVT. If the AIVTEN bit is set, all interrupt and exception processes will use the alternate vectors instead of the default vectors. The alternate vectors are organized in the same manner as the default vectors.

The AIVT is available only if the Boot Segment has been defined and the AIVT has been enabled. To enable the AIVT, both the Configuration bit, AIVTDIS (FSEC[15]), and the AIVTEN bit (INTCON2[8] in the SFR), have to be set. When the AIVT is enabled, all interrupts and exception processes use the alternate vectors instead of the default vectors. The AIVT begins at the start of the last page of the Boot Segment (BS) defined by the BSLIM[12:0] bits. The AIVT address is: ($\overline{\text{BSLIM}}$[12:0] – 1) x 0x800.

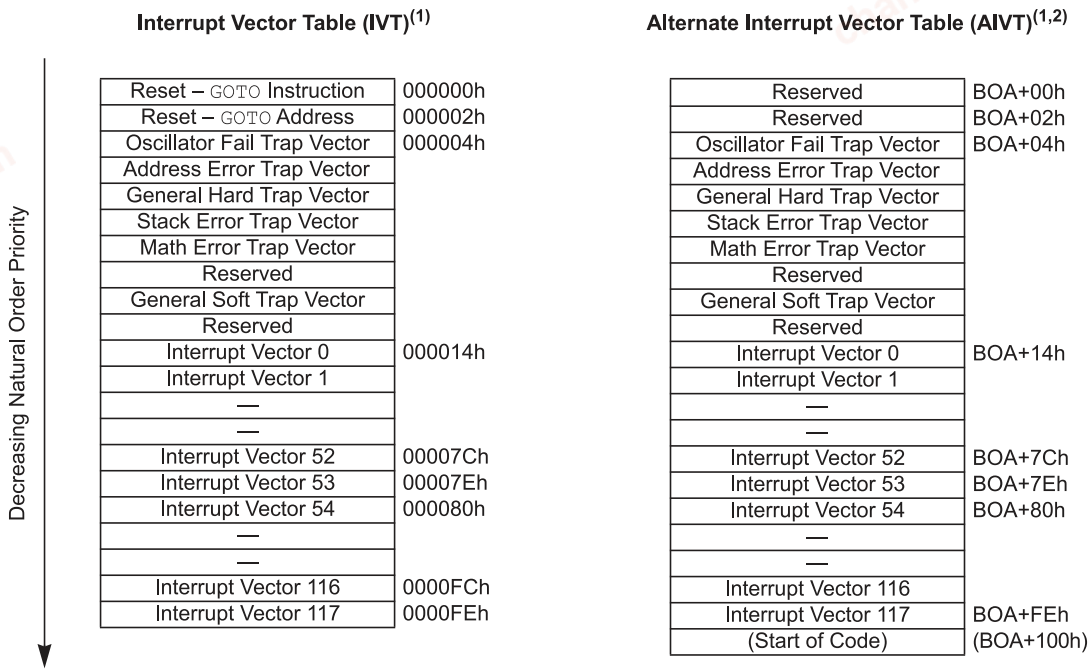
8.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The PIC24FJ64GP205/GU205 family devices clear their registers in response to a Reset, which forces the PC to zero. The device then begins program execution at location, 0x000000. A `GOTO` instruction at the Reset address can redirect program execution to the appropriate start-up routine.

Note: Any unimplemented or unused vector locations in the IVT should be programmed with the address of a default interrupt handler routine that contains a `RESET` instruction.

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Figure 8-1. PIC24F Interrupt Vector Tables



Legend: BOA: Base Offset Address for AIVT, which is the starting address of the last page of the Boot Segment. All addresses are in hexadecimal.

Notes:

1. See Table 8-1 and Table 8-2 for the vectors list.
2. AIVT is only available when a Boot Segment is implemented.

Table 8-1. Trap Vector Details

Trap Description	MPLAB® XC16 Trap ISR Name	Vector #	IVT or AIVT Address Offset	Trap Bit Location			
				Generic Flag	Source Flag	Enable	Priority
Oscillator Failure Trap	_OscillatorFail	0	0x000004	INTCON1[1]	—	—	15
Address Error Trap	_AddressError	1	0x000006	INTCON1[3]	—	—	14
Generic Hard Trap – ECCDBE	_HardTrapError	2	0x000008	—	INTCON4[1]	—	13
Generic Hard Trap – SGHT	_HardTrapError	2	0x000008	—	INTCON4[0]	INTCON2[13]	13
Stack Error Trap	_StackError	3	0x00000A	INTCON1[2]	—	—	12
Math Error Trap – DIV0ERR	_MathError	4	0x00000C	INTCON1[4]	—	—	11
Reserved	Reserved	5	0x00000E	—	—	—	—
Reserved	Reserved	5	0x000010	—	—	—	—

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Trap Description	MPLAB® XC16 Trap ISR Name	Vector #	IVT or AIVT Address Offset	Trap Bit Location			
				Generic Flag	Source Flag	Enable	Priority
Reserved	Reserved	7	0x000012	—	—	—	—

Table 8-2. Interrupt Vector Details

Interrupt Description	MPLAB® XC16 ISR Name	Vector #	IRQ #	IVT or AIVT Address Offset	Interrupt Bit Location		
					Flag	Enable	Priority
External Interrupt 0	_INT0Interrupt	8	0	000014h	IFS0[0]	IEC0[0]	IPC0[2:0]
Capture/ Compare/ Timer1	_CCT1Interrupt	9	1	000016h	IFS0[1]	IEC0[1]	IPC0[6:4]
Capture/ Compare/ Timer2	_CCT2Interrupt	10	2	000018h	IFS0[2]	IEC0[2]	IPC0[10:8]
Timer1	_T1Interrupt	11	3	00001Ah	IFS0[3]	IEC0[3]	IPC0[14:12]
Direct Memory Access 0	_DMA0Interrupt	12	4	00001Ch	IFS0[4]	IEC0[4]	IPC1[2:0]
Reserved	Reserved	13-14	5-6	00001Eh-000020h	—	—	—
Timer2	_T2Interrupt	15	7	000022h	IFS0[7]	IEC0[7]	IPC1[14:12]
Timer3	_T3Interrupt	16	8	000024h	IFS0[8]	IEC0[8]	IPC2[2:0]
SPI1 General	_SPI1Interrupt	17	9	000026h	IFS0[9]	IEC0[9]	IPC2[6:4]
SPI1 Transfer Done	_SPI1TXInterrupt	18	10	000028h	IFS0[10]	IEC0[10]	IPC2[10:8]
UART1 Receiver	_U1RXInterrupt	19	11	00002Ah	IFS0[11]	IEC0[11]	IPC2[14:12]
UART1 Transmitter	_U1TXInterrupt	20	12	00002Ch	IFS0[12]	IEC0[12]	IPC3[2:0]
A/D Converter 1	_ADC1Interrupt	21	13	00002Eh	IFS0[13]	IEC0[13]	IPC3[6:4]
Direct Memory Access 1	_DMA1Interrupt	22	14	000030h	IFS0[14]	IEC0[14]	IPC3[10:8]
NVM Program/ Erase Complete	_NVMInterrupt	23	15	000032h	IFS0[15]	IEC0[15]	IPC3[14:12]
I2C1 Client Events	_SI2C1Interrupt	24	16	000034h	IFS1[0]	IEC1[0]	IPC4[2:0]
I2C1 Host Events	_MI2C1Interrupt	25	17	000036h	IFS1[1]	IEC1[1]	IPC4[6:4]
Comparator	_CompInterrupt	26	18	000038h	IFS1[2]	IEC1[2]	IPC4[10:8]

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Interrupt Description	MPLAB® XC16 ISR Name	Vector #	IRQ #	IVT or AIVT Address Offset	Interrupt Bit Location		
					Flag	Enable	Priority
Interrupt-on-Change Interrupt	_IOCInterrupt	27	19	00003Ah	IFS1[3]	IEC1[3]	IPC4[14:12]
External Interrupt 1	_INT1Interrupt	28	20	00003Ch	IFS1[4]	IEC1[4]	IPC5[2:0]
Reserved	Reserved	29	21	00003Eh	—	—	—
Capture/ Compare 5	_CCP5Interrupt	30	22	000040h	IFS1[6]	IEC1[6]	IPC5[10:8]
Reserved	Reserved	33-34	25-26	000046h-000048h	—	—	—
External Interrupt 2	_INT2Interrupt	37	29	00004Eh	IFS1[13]	IEC1[13]	IPC7[6:4]
UART2 Receiver	_U2RXInterrupt	38	30	000050h	IFS1[14]	IEC1[14]	IPC7[10:8]
UART2 Transmitter	_U2TXInterrupt	39	31	000052h	IFS1[15]	IEC1[15]	IPC7[14:12]
SPI2 General	_SPI2Interrupt	40	32	000054h	IFS2[0]	IEC2[0]	IPC8[2:0]
SPI2 Transfer Done	_SPI2TXInterrupt	41	33	000056h	IFS2[1]	IEC2[1]	IPC8[6:4]
Reserved	Reserved	42-43	34-35	000058h-00005Ah	—	—	—
Reserved	Reserved	45-50	37-42	00005Eh-000068h	—	—	—
Capture/ Compare/ Timer3	_CCT3Interrupt	51	43	00006Ah	IFS2[11]	IEC2[11]	IPC10[14:12]
Capture/ Compare/ Timer4	_CCT4Interrupt	52	44	00006Ch	IFS2[12]	IEC2[12]	IPC11[2:0]
Reserved	Reserved	53	45	00006Eh	—	—	—
Capture/ Compare/ Timer5	_CCT5Interrupt	55	47	000072h	IFS2[15]	IEC2[15]	IPC11[14:12]
I2C2 Client Events	_SI2C2Interrupt	57	49	000076h	IFS3[1]	IEC3[1]	IPC12[6:4]
I2C2 Host Events	_MI2C2Interrupt	58	50	000078h	IFS3[2]	IEC3[2]	IPC12[10:8]
External Interrupt 3	_INT3Interrupt	61	53	00007Eh	IFS3[5]	IEC3[5]	IPC13[6:4]
External Interrupt 4	_INT4Interrupt	62	54	000080h	IFS3[6]	IEC3[6]	IPC13[10:8]
Reserved	Reserved	63-65	55-57	000082h-000086h	—	—	—
SPI1 Receive Done	_SPI1RXInterrupt	66	58	000088h	IFS3[10]	IEC3[10]	IPC14[10:8]

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Interrupt Description	MPLAB® XC16 ISR Name	Vector #	IRQ #	IVT or AIVT Address Offset	Interrupt Bit Location		
					Flag	Enable	Priority
SPI2 Receive Done	_SPI2RXInterrupt	67	59	00008Ah	IFS3[11]	IEC3[11]	IPC14[14:12]
Reserved	Reserved	68-69	60-61	00008Ch-00008Fh	—	—	—
Real-Time Clock and Calendar	_RTCCInterrupt	70	62	000090h	IFS3[14]	IEC3[14]	IPC15[10:8]
Capture/ Compare 1	_CCP1Interrupt	71	63	000092h	IFS3[15]	IEC3[15]	IPC15[14:12]
Capture/ Compare 2	_CCP2Interrupt	72	64	000094h	IFS4[0]	IEC4[0]	IPC16[2:0]
UART1 Error	_U1ErrInterrupt	73	65	000096h	IFS4[1]	IEC4[1]	IPC16[6:4]
UART2 Error	_U2ErrInterrupt	74	66	000098h	IFS4[2]	IEC4[2]	IPC16[10:8]
Cyclic Redundancy Check	_CRCInterrupt	75	67	00009Ah	IFS4[3]	IEC4[3]	IPC16[14:12]
Reserved	Reserved	76-77	68-69	00009Ch-00009Eh	—	—	—
High/Low-Voltage Detect	_HLVDInterrupt	80	72	0000A4h	IFS4[8]	IEC4[8]	IPC18[2:0]
Reserved	Reserved	83-85	75-87	0000AAh-0000AEh	—	—	—
Reserved	Reserved	87-88	79-80	0000B2h-0000B4h	—	—	—
I2C1 Bus Collision	_I2C1BCInterrupt	92	84	0000BCh	IFS5[4]	IEC5[4]	IPC21[2:0]
I2C2 Bus Collision	_I2C2BCInterrupt	93	85	0000BEh	IFS5[5]	IEC5[5]	IPC21[6:4]
USB OTG Interrupt	_USB1Interrupt	94	86	0000C0h	IFS5[6]	IEC5[6]	IPC21[10:8]
Capture/ Compare 3	_CCP3Interrupt	102	94	0000D0h	IFS5[14]	IEC5[14]	IPC23[10:8]
Capture/ Compare 4	_CCP4Interrupt	103	95	0000D2h	IFS5[15]	IEC5[15]	IPC23[14:12]
Configurable Logic Cell 1	_CLC1Interrupt	104	96	0000D4h	IFS6[0]	IEC6[0]	IPC24[2:0]
Configurable Logic Cell 2	_CLC2Interrupt	105	97	0000D6h	IFS6[1]	IEC6[1]	IPC24[6:4]
Configurable Logic Cell 3	_CLC3Interrupt	106	98	0000D8h	IFS6[2]	IEC6[2]	IPC24[10:8]
Configurable Logic Cell 4	_CLC4Interrupt	107	99	0000DAh	IFS6[3]	IEC6[3]	IPC24[14:12]
Reserved	Reserved	110-113	102-105	0000E0h-0000E6h	—	—	—

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Interrupt Description	MPLAB® XC16 ISR Name	Vector #	IRQ #	IVT or AIVT Address Offset	Interrupt Bit Location		
					Flag	Enable	Priority
FRC Self-Tuning Interrupt	_FSTInterrupt	114	106	0000E8h	IFS6[10]	IEC6[10]	IPC26[10:8]
Reserved	Reserved	115	107	0000EAh	—	—	—
Real-Time Clock Timestamp	_RTCCTSInterrupt	118	110	0000F0h	IFS6[14]	IEC6[14]	IPC27[10:8]
JTAG	_JTAGInterrupt	125	117	0000FEh	IFS7[5]	IEC7[5]	IPC29[6:4]

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8.3 Interrupt Controller Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x7F	Reserved									
0x80	INTCON1	7:0				MATHERR	ADDRERR	STKERR	OSCFAIL	
		15:8	NSTDIS							
0x82	INTCON2	7:0				INT4EP	INT3EP	INT2EP	INT1EP	INT0EP
		15:8	GIE	DISI	SWTRAP					AIVTEN
0x84	INTCON3	7:0								
		15:8	DMT							
0x86	INTCON4	7:0							ECCDBE	SGHT
		15:8								
0x88	IFS0	7:0	T2IF			DMA0IF	T1IF	CCT2IF	CCT1IF	INT0IF
		15:8	NVMIF	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1TXIF	SPI1IF	T3IF
0x8A	IFS1	7:0		CCP5IF		INT1IF	IOCIF	CMIF	MI2C1IF	SI2C1IF
		15:8	U2TXIF	U2RXIF	INT2IF					
0x8C	IFS2	7:0							SPI2TXIF	SPI2IF
		15:8	CCT5IF			CCT4IF	CCT3IF			
0x8E	IFS3	7:0		INT4IF	INT3IF			MI2C2IF	SI2C2IF	
		15:8	CCP1IF	RTCIF			SPI2RXIF	SPI1RXIF		
0x90	IFS4	7:0					CRCIF	U2ERIF	U1ERIF	CCP2IF
		15:8								HLVDIF
0x92	IFS5	7:0		USB1IF	I2C2BCIF	I2C1BCIF				
		15:8	CCP4IF	CCP3IF						
0x94	IFS6	7:0					CLC4IF	CLC3IF	CLC2IF	CLC1IF
		15:8		RTCCTSIF				FSTIF		
0x96	IFS7	7:0			JTAGIF					
		15:8								
0x98	IEC0	7:0	T2IE			DMA0IE	T1IE	CCT2IE	CCT1IE	INT0IE
		15:8	NVMIE	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1TXIE	SPI1IE	T3IE
0x9A	IEC1	7:0		CCP5IE		INT1IE	IOCIE	CMIE	MI2C1IE	SI2C1IE
		15:8	U2TXIE	U2RXIE	INT2IE					
0x9C	IEC2	7:0							SPI2TXIE	SPI2IE
		15:8	CCT5IE			CCT4IE	CCT3IE			
0x9E	IEC3	7:0		INT4IE	INT3IE			MI2C2IE	SI2C2IE	
		15:8	CCP1IE	RTCIE			SPI2RXIE	SPI1RXIE		
0xA0	IEC4	7:0					CRCIE	U2ERIE	U1ERIE	CCP2IE
		15:8								HLVDIE
0xA2	IEC5	7:0		USB1IE	I2C2BCIE	I2C1BCIE				
		15:8	CCP4IE	CCP3IE						
0xA4	IEC6	7:0					CLC4IE	CLC3IE	CLC2IE	CLC1IE
		15:8		RTCCTSIE				FSTIE		
0xA6	IEC7	7:0			JTAGIE					
		15:8								
0xA8	IPC0	7:0		CCT1IP[2:0]				INT0IP[2:0]		
		15:8		T1IP[2:0]				CCT2IP[2:0]		
0xAA	IPC1	7:0						DMA0IP[2:0]		
		15:8		T2IP[2:0]						
0xAC	IPC2	7:0		SPI1IP[2:0]				T3IP[2:0]		
		15:8		U1RXIP[2:0]				SPI1TXIP[2:0]		
0xAE	IPC3	7:0		AD1IP[2:0]				U1TXIP[2:0]		
		15:8		NVMIP[2:0]				DMA1IP[2:0]		
0xB0	IPC4	7:0		MI2C1IP[2:0]				SI2C1IP[2:0]		
		15:8		IOCIP[2:0]				CMIP[2:0]		
0xB2	IPC5	7:0						INT1IP[2:0]		
		15:8						CCP5IP[2:0]		

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0xB4 ... 0xB5	Reserved									
0xB6	IPC7	7:0			INT2IP[2:0]					
		15:8			U2TXIP[2:0]				U2RXIP[2:0]	
0xB8	IPC8	7:0			SPI2TXIP[2:0]				SPI2IP[2:0]	
		15:8								
0xBA ... 0xBB	Reserved									
0xBC	IPC10	7:0								
		15:8			CCT3IP[2:0]					
0xBE	IPC11	7:0							CCT4IP[2:0]	
		15:8			CCT5IP[2:0]					
0xC0	IPC12	7:0			SI2C2IP[2:0]					
		15:8							MI2C2IP[2:0]	
0xC2	IPC13	7:0			INT3IP[2:0]					
		15:8							INT4IP[2:0]	
0xC4	IPC14	7:0								
		15:8			SPI2RXIP[2:0]				SPI1RXIP[2:0]	
0xC6	IPC15	7:0								
		15:8			CCP1IP[2:0]				RTCIP[2:0]	
0xC8	IPC16	7:0			U1ERIP[2:0]				CCP2IP[2:0]	
		15:8			CRCIP[2:0]				U2ERIP[2:0]	
0xCA ... 0xCB	Reserved									
0xCC	IPC18	7:0							HLVDIP[2:0]	
		15:8								
0xCE ... 0xD1	Reserved									
0xD2	IPC21	7:0			I2C2BCIP[2:0]				I2C1BCIP[2:0]	
		15:8							USB1IP[2:0]	
0xD4 ... 0xD5	Reserved									
0xD6	IPC23	7:0								
		15:8			CCP4IP[2:0]				CCP3IP[2:0]	
0xD8	IPC24	7:0			CLC2IP[2:0]				CLC1IP[2:0]	
		15:8			CLC4IP[2:0]				CLC3IP[2:0]	
0xDA ... 0xDB	Reserved									
0xDC	IPC26	7:0								
		15:8							FSTIP[2:0]	
0xDE	IPC27	7:0								
		15:8							RTCCTSIP[2:0]	
0xE0 ... 0xE1	Reserved									
0xE2	IPC29	7:0			JTAGIP[2:0]					
		15:8								
0xE4	INTTREG	7:0	VECNUM[7:0]							
		15:8	CPUIRQ		VHOLD		ILR[3:0]			

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8.3.1 Interrupt Control and Status Registers Overview

Global interrupt control functions are controlled from INTCON1 and INTCON2. INTCON1 contains the Interrupt Nesting Disable (NSTDIS) bit, as well as the control and status flags for the processor trap sources.

The INTCON2 register controls global interrupt generation, the external interrupt request signal behavior and the use of the Alternate Interrupt Vector Table (AIVT).

The INTCON3 register contains the Deadman Timer (DMT) trap bit. The INTCON4 register contains the Software Generated Hard Trap bit (SGHT).

The IFSx registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared via software.

The IECx registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

The IPCx registers are used to set the Interrupt Priority Level (IPL) for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt Priority Level, which are latched into the Vector Number bits (VECNUM[7:0]) and Interrupt Priority Level bits (ILR[3:0]) fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence as they are listed in Table 8-2. For example, the INT0 (External Interrupt 0) is shown as having Vector Number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0[0], the INT0IE bit in IEC0[0] and the INT0IPx bits in the first position of IPC0 (IPC0[2:0]).

Two of the CPU Control registers contain bits that control interrupt functionality. For more information on these registers, refer to **"CPU with Extended Data Space (EDS)"** (www.microchip.com/DS39732) in the *"dsPIC33/PIC24 Family Reference Manual"*.

The CPU STATUS Register, SR, contains the IPL[2:0] bits (SR[7:5]). These bits indicate the current CPU Interrupt Priority Level. The user software can change the current CPU Interrupt Priority Level by writing to the IPLx bits.

The CORCON register contains the IPL3 bit, which together with the IPL[2:0] bits, also indicates the current CPU Interrupt Priority Level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described from 8.3.2 INTCON1 through 8.3.44 INTTREG in the following pages.

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8.3.2 Interrupt Control Register 1

Name: INTCON1
Offset: 0x80

Bit	15	14	13	12	11	10	9	8
	NSTDIS							
Access	R/W							
Reset	0							

Bit	7	6	5	4	3	2	1	0
				MATHERR	ADDRERR	STKERR	OSCFAIL	
Access				R/W	R/W	R/W	R/W	
Reset				0	0	0	0	

Bit 15 – NSTDIS Interrupt Nesting Disable bit

Value	Description
1	Interrupt nesting is disabled
0	Interrupt nesting is enabled

Bit 4 – MATHERR Math Error Status bit

Value	Description
1	Math error trap has occurred
0	Math error trap has not occurred

Bit 3 – ADDRERR Address Error Trap Status bit

Value	Description
1	Address error trap has occurred
0	Address error trap has not occurred

Bit 2 – STKERR Stack Error Trap Status bit

Value	Description
1	Stack error trap has occurred
0	Stack error trap has not occurred

Bit 1 – OSCFAIL Oscillator Failure Trap Status bit

Value	Description
1	Oscillator failure trap has occurred
0	Oscillator failure trap has not occurred

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8.3.3 Interrupt Control Register 2

Name: INTCON2
Offset: 0x82

Bit	15	14	13	12	11	10	9	8
	GIE	DISI	SWTRAP					AIVTEN
Access	R/W	R	R/W					R/W
Reset	1	0	0					0

Bit	7	6	5	4	3	2	1	0
				INT4EP	INT3EP	INT2EP	INT1EP	INT0EP
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 15 – GIE Global Interrupt Enable bit

Value	Description
1	Interrupts and associated interrupt enable bits are enabled
0	Interrupts are disabled, but traps are still enabled

Bit 14 – DISI `DISI` Instruction Status bit

Value	Description
1	`DISI` instruction is active
0	`DISI` instruction is not active

Bit 13 – SWTRAP Software Trap Status bit

Value	Description
1	Software trap is enabled
0	Software trap is disabled

Bit 8 – AIVTEN Alternate Interrupt Vector Table Enable bit

Value	Description
1	Uses Alternate Interrupt Vector Table (if enabled in Configuration bits)
0	Uses standard Interrupt Vector Table (default)

Bit 4 – INT4EP External Interrupt 4 Edge Detect Polarity Select bit

Value	Description
1	Interrupt on negative edge
0	Interrupt on positive edge

Bit 3 – INT3EP External Interrupt 3 Edge Detect Polarity Select bit

Value	Description
1	Interrupt on negative edge
0	Interrupt on positive edge

Bit 2 – INT2EP External Interrupt 2 Edge Detect Polarity Select bit

Value	Description
1	Interrupt on negative edge
0	Interrupt on positive edge

Bit 1 – INT1EP External Interrupt 1 Edge Detect Polarity Select bit

Value	Description
1	Interrupt on negative edge
0	Interrupt on positive edge

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Bit 0 – INT0EP External Interrupt 0 Edge Detect Polarity Select bit

Value	Description
1	Interrupt on negative edge
0	Interrupt on positive edge

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8.3.4 Interrupt Control Register 3

Name: INTCON3
Offset: 0x84

Bit	15	14	13	12	11	10	9	8
	DMT							
Access	R/W							
Reset	0							

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 15 – DMT Deadman Timer Soft Trap Status bit

Value	Description
1	Deadman Timer trap has occurred
0	Deadman Timer trap has not occurred

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8.3.5 Interrupt Control Register 4

Name: INTCON4
Offset: 0x86

Legend: C = Clearable bit

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							ECCDBE	SGHT
Access							R/C	R/C
Reset							0	0

Bit 1 – ECCDBE ECC Double-Bit Error Trap bit

Value	Description
1	ECC double-bit error trap has occurred
0	ECC double-bit error trap has not occurred

Bit 0 – SGHT Software Generated Hard Trap Status bit

Value	Description
1	Software generated hard trap has occurred
0	Software generated hard trap has not occurred

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8.3.6 Interrupt Request Flags Register 0

Name: IFS0
Offset: 0x88

Bit	15	14	13	12	11	10	9	8
	NVMIF	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1TXIF	SPI1IF	T3IF
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	T2IF			DMA0IF	T1IF	CCT2IF	CCT1IF	INT0IF
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bit 15 – NVMIF NVM Program/Erase Complete Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 14 – DMA1IF Direct Memory Access 1 Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 13 – AD1IF A/D Converter 1 Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 12 – U1TXIF UART1 Transmitter Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 11 – U1RXIF UART1 Receiver Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 10 – SPI1TXIF SPI1 Transfer Done Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 9 – SPI1IF SPI1 General Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 8 – T3IF Timer3 Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

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Bit 7 – T2IF Timer2 Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 4 – DMA0IF Direct Memory Access 0 Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 3 – T1IF Timer1 Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 2 – CCT2IF Capture/Compare/Timer2 Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 1 – CCT1IF Capture/Compare/Timer1 Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 0 – INT0IF External Interrupt 0 bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

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8.3.7 Interrupt Request Flags Register 1

Name: IFS1
Offset: 0x8A

Bit	15	14	13	12	11	10	9	8
	U2TXIF	U2RXIF	INT2IF					
Access	R/W	R/W	R/W					
Reset	0	0	0					

Bit	7	6	5	4	3	2	1	0
		CCP5IF		INT1IF	IOCIF	CMIF	MI2C1IF	SI2C1IF
Access		R/W		R/W	R/W	R/W	R/W	R/W
Reset		0		0	0	0	0	0

Bit 15 – U2TXIF UART2 Transmitter Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 14 – U2RXIF UART2 Receiver Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 13 – INT2IF External Interrupt 2 bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 6 – CCP5IF Capture/Compare 5 Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 4 – INT1IF External Interrupt 1 bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 3 – IOCIF Interrupt-on-Change Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 2 – CMIF Comparator Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 1 – MI2C1IF I2C1 Host Events Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

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Bit 0 – SI2C1IF I2C1 Client Events Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

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8.3.8 Interrupt Request Flags Register 2

Name: IFS2
Offset: 0x8C

Bit	15	14	13	12	11	10	9	8
	CCT5IF			CCT4IF	CCT3IF			
Access	R/W			R/W	R/W			
Reset	0			0	0			

Bit	7	6	5	4	3	2	1	0
							SPI2TXIF	SPI2IF
Access							R/W	R/W
Reset							0	0

Bit 15 – CCT5IF Capture/Compare/Timer5 Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 12 – CCT4IF Capture/Compare/Timer4 Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 11 – CCT3IF Capture/Compare/Timer3 Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 1 – SPI2TXIF SPI2 Transfer Done Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 0 – SPI2IF SPI2 General Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

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8.3.9 Interrupt Request Flags Register 3

Name: IFS3
Offset: 0x8E

Bit	15	14	13	12	11	10	9	8
	CCP1IF	RTCIF			SPI2RXIF	SPI1RXIF		
Access	R/W	R/W			R/W	R/W		
Reset	0	0			0	0		

Bit	7	6	5	4	3	2	1	0
		INT4IF	INT3IF			MI2C2IF	SI2C2IF	
Access		R/W	R/W			R/W	R/W	
Reset		0	0			0	0	

Bit 15 – CCP1IF Capture/Compare 1 Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 14 – RTCIF Real-Time Clock and Calendar bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 11 – SPI2RXIF SPI2 Receive Done Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 10 – SPI1RXIF SPI1 Receive Done Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 6 – INT4IF External Interrupt 4 bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 5 – INT3IF External Interrupt 3 bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 2 – MI2C2IF I2C2 Host Events Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 1 – SI2C2IF I2C2 Client Events Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

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8.3.10 Interrupt Request Flags 4 Register

Name: IFS4
Offset: 0x90

Bit	15	14	13	12	11	10	9	8
								HLVDIF
Access								R/W
Reset								0

Bit	7	6	5	4	3	2	1	0
					CRCIF	U2ERIF	U1ERIF	CCP2IF
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 8 – HLVDIF High/Low-Voltage Detect Interrupt bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 3 – CRCIF Cyclic Redundancy Check Interrupt bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 2 – U2ERIF UART2 Error Interrupt bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 1 – U1ERIF UART1 Error Interrupt bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 0 – CCP2IF Capture/Compare 2 Interrupt bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

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8.3.11 Interrupt Request Flags Register 5

Name: IFS5
Offset: 0x92

Bit	15	14	13	12	11	10	9	8
	CCP4IF	CCP3IF						
Access	R/W	R/W						
Reset	0	0						

Bit	7	6	5	4	3	2	1	0
		USB1IF	I2C2BCIF	I2C1BCIF				
Access		R/W	R/W	R/W				
Reset		0	0	0				

Bit 15 – CCP4IF Capture/Compare 4 Interrupt bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 14 – CCP3IF Capture/Compare 3 Interrupt bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 6 – USB1IF USB1 OTG Interrupt bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 5 – I2C2BCIF I2C2 Bus Collision Interrupt bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 4 – I2C1BCIF I2C1 Bus Collision Interrupt bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

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8.3.12 Interrupt Request Flags Register 6

Name: IFS6
Offset: 0x94

Bit	15	14	13	12	11	10	9	8
		RTCCTSIF				FSTIF		
Access		R/W				R/W		
Reset		0				0		

Bit	7	6	5	4	3	2	1	0
					CLC4IF	CLC3IF	CLC2IF	CLC1IF
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 14 – RTCCTSIF Real-Time Clock Timestamp Interrupt bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 10 – FSTIF FRC Self-Tuning Interrupt bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 3 – CLC4IF Configurable Logic Cell 4 Interrupt bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 2 – CLC3IF Configurable Logic Cell 3 Interrupt bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 1 – CLC2IF Configurable Logic Cell 2 Interrupt bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 0 – CLC1IF Configurable Logic Cell 1 Interrupt bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

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8.3.13 Interrupt Request Flags Register 7

Name: IFS7
Offset: 0x96

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			JTAGIF					
Access			R/W					
Reset			0					

Bit 5 – JTAGIF JTAG Interrupt Enable bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

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8.3.14 Interrupt Enable Register 0

Name: IEC0
Offset: 0x98

Bit	15	14	13	12	11	10	9	8
	NVMIE	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1TXIE	SPI1IE	T3IE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	T2IE			DMA0IE	T1IE	CCT2IE	CCT1IE	INT0IE
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bit 15 – NVMIE NVM Program/Erase Complete Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 14 – DMA1IE Direct Memory Access 1 Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 13 – AD1IE A/D Converter 1 Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 12 – U1TXIE UART1 Transmitter Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 11 – U1RXIE UART1 Receiver Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 10 – SPI1TXIE SPI1 Transfer Done Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 9 – SPI1IE SPI1 Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 8 – T3IE Timer3 Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

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Bit 7 – T2IE Timer2 Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 4 – DMA0IE Direct Memory Access 0 Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 3 – T1IE Timer1 Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 2 – CCT2IE Capture/Compare/Timer2 Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 1 – CCT1IE Capture/Compare/Timer1 Interrupt bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

Bit 0 – INT0IE External Interrupt 0 bit

Value	Description
1	Interrupt has occurred
0	Interrupt has not occurred

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8.3.15 Interrupt Enable Register 1

Name: IEC1
Offset: 0x9A

Bit	15	14	13	12	11	10	9	8
	U2TXIE	U2RXIE	INT2IE					
Access	R/W	R/W	R/W					
Reset	0	0	0					

Bit	7	6	5	4	3	2	1	0
		CCP5IE		INT1IE	IOCIE	CMIE	MI2C1IE	SI2C1IE
Access		R/W		R/W	R/W	R/W	R/W	R/W
Reset		0		0	0	0	0	0

Bit 15 – U2TXIE UART2 Transmitter Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 14 – U2RXIE UART2 Receiver Transmitter Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 13 – INT2IE External Interrupt 2 Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 6 – CCP5IE Capture/Compare 5 Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 4 – INT1IE External Interrupt 1 Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 3 – IOCIE Interrupt-on-Change Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 2 – CMIE Comparator Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 1 – MI2C1IE I2C1 Host Events Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

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Bit 0 – SI2C1IE I2C1 Client Events Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

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8.3.16 Interrupt Enable Register 2

Name: IEC2
Offset: 0x9C

Bit	15	14	13	12	11	10	9	8
	CCT5IE			CCT4IE	CCT3IE			
Access	R/W			R/W	R/W			
Reset	0			0	0			

Bit	7	6	5	4	3	2	1	0
							SPI2TXIE	SPI2IE
Access							R/W	R/W
Reset							0	0

Bit 15 – CCT5IE Capture/Compare/Timer5 Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 12 – CCT4IE Capture/Compare/Timer4 Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 11 – CCT3IE Capture/Compare/Timer3 Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 1 – SPI2TXIE SPI2 Transfer Done Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 0 – SPI2IE SPI2 General Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

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8.3.17 Interrupt Enable Register 3

Name: IEC3
Offset: 0x9E

Bit	15	14	13	12	11	10	9	8
	CCP1IE	RTCIE			SPI2RXIE	SPI1RXIE		
Access	R/W	R/W			R/W	R/W		
Reset	0	0			0	0		

Bit	7	6	5	4	3	2	1	0
		INT4IE	INT3IE			MI2C2IE	SI2C2IE	
Access		R/W	R/W			R/W	R/W	
Reset		0	0			0	0	

Bit 15 – CCP1IE Capture/Compare 1 Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 14 – RTCIE Real-Time Clock and Calendar Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 11 – SPI2RXIE SPI2 Receive Done Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 10 – SPI1RXIE SPI1 Receive Done Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 6 – INT4IE External Interrupt 4 Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 5 – INT3IE External Interrupt 4 Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 2 – MI2C2IE I2C2 Host Events Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 1 – SI2C2IE I2C2 Client Events Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

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8.3.18 Interrupt Enable Register 4

Name: IEC4
Offset: 0xA0

Bit	15	14	13	12	11	10	9	8
								HLVDIE
Access								R/W
Reset								0

Bit	7	6	5	4	3	2	1	0
					CRCIE	U2ERIE	U1ERIE	CCP2IE
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 8 – HLVDIE High/Low-Voltage Detect Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 3 – CRCIE Cyclic Redundancy Check Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 2 – U2ERIE UART2 Error Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 1 – U1ERIE UART1 Error Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 0 – CCP2IE Capture/Compare 2 Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

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8.3.19 Interrupt Enable Register 5

Name: IEC5
Offset: 0xA2

Bit	15	14	13	12	11	10	9	8
	CCP4IE	CCP3IE						
Access	R/W	R/W						
Reset	0	0						

Bit	7	6	5	4	3	2	1	0
		USB1IE	I2C2BCIE	I2C1BCIE				
Access		R/W	R/W	R/W				
Reset		0	0	0				

Bit 15 – CCP4IE Capture/Compare 4 Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 14 – CCP3IE Capture/Compare 4 Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 6 – USB1IE USB OTG 1 Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 5 – I2C2BCIE I2C2 Bus Collision Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 4 – I2C1BCIE I2C1 Bus Collision Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

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8.3.20 Interrupt Enable Register 6

Name: IEC6
Offset: 0xA4

Bit	15	14	13	12	11	10	9	8
		RTCCTSIE				FSTIE		
Access		R/W				R/W		
Reset		0				0		

Bit	7	6	5	4	3	2	1	0
					CLC4IE	CLC3IE	CLC2IE	CLC1IE
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 14 – RTCCTSIE Real-Time Clock Timestamp Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 10 – FSTIE FRC Self-Tuning Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 3 – CLC4IE Configurable Logic Cell 4 Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 2 – CLC3IE Configurable Logic Cell 3 Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 2 – CCT2IE Capture/Compare/Timer2 Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 1 – CLC2IE Configurable Logic Cell 2 Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

Bit 0 – CLC1IE Configurable Logic Cell 1 Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

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8.3.21 Interrupt Enable Register 7

Name: IEC7
Offset: 0xA6

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			JTAGIE					
Access			R/W					
Reset			0					

Bit 5 – JTAGIE JTAG Interrupt Enable bit

Value	Description
1	Interrupt enabled
0	Interrupt not enabled

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8.3.22 Interrupt Priority Register 0

Name: IPC0
Offset: 0xA8

Bit	15	14	13	12	11	10	9	8
		T1IP[2:0]				CCT2IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		CCT1IP[2:0]				INT0IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – T1IP[2:0] Timer1 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – CCT2IP[2:0] Capture/Compare/Timer2 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – CCT1IP[2:0] Capture/Compare/Timer1 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – INT0IP[2:0] External Interrupt 0 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3

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Value	Description
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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8.3.23 Interrupt Priority Register 1

Name: IPC1
Offset: 0xAA

Bit	15	14	13	12	11	10	9	8
		T2IP[2:0]						
Access		R/W	R/W	R/W				
Reset		1	0	0				

Bit	7	6	5	4	3	2	1	0
						DMA0IP[2:0]		
Access						R/W	R/W	R/W
Reset						1	0	0

Bits 14:12 – T2IP[2:0] Timer2 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – DMA0IP[2:0] Direct Memory Access 0 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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8.3.24 Interrupt Priority Register 2

Name: IPC2
Offset: 0xAC

Bit	15	14	13	12	11	10	9	8
		U1RXIP[2:0]				SPI1TXIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		SPI1IP[2:0]				T3IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – U1RXIP[2:0] UART1 Receiver Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – SPI1TXIP[2:0] SPI1 Transfer Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – SPI1IP[2:0] SPI1 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – T3IP[2:0] Timer3 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3

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Value	Description
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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8.3.25 Interrupt Priority Register 3

Name: IPC3
Offset: 0xAE

Bit	15	14	13	12	11	10	9	8
		NVMIP[2:0]				DMA1IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		AD1IP[2:0]				U1TXIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – NVMIP[2:0] NVM Program/Erase Complete Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – DMA1IP[2:0] Direct Memory Access 1 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – AD1IP[2:0] A/D Converter 1 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – U1TXIP[2:0] UART1 Transmitter Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3

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Value	Description
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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8.3.26 Interrupt Priority Register 4

Name: IPC4
Offset: 0xB0

Bit	15	14	13	12	11	10	9	8
		IOCIP[2:0]				CMIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		MI2C1IP[2:0]				SI2C1IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – IOCIP[2:0] Interrupt-on-Change Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – CMIP[2:0] Comparator Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – MI2C1IP[2:0] I2C1 Host Events Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – SI2C1IP[2:0] I2C1 Client Events Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3

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Value	Description
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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8.3.27 Interrupt Priority Register 5

Name: IPC5
Offset: 0xB2

Bit	15	14	13	12	11	10	9	8
						CCP5IP[2:0]		
Access						R/W	R/W	R/W
Reset						1	0	0

Bit	7	6	5	4	3	2	1	0
						INT1IP[2:0]		
Access						R/W	R/W	R/W
Reset						1	0	0

Bits 10:8 – CCP5IP[2:0] Capture/Compare 5 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – INT1IP[2:0] External Interrupt 1 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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8.3.28 Interrupt Priority Register 7

Name: IPC7
Offset: 0xB6

Bit	15	14	13	12	11	10	9	8
		U2TXIP[2:0]				U2RXIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		INT2IP[2:0]						
Access		R/W	R/W	R/W				
Reset		1	0	0				

Bits 14:12 – U2TXIP[2:0] UART2 Transmitter Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – U2RXIP[2:0] UART2 Receiver Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – INT2IP[2:0] External Interrupt 2 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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8.3.29 Interrupt Priority Register 8

Name: IPC8
Offset: 0xB8

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		SPI2TXIP[2:0]				SPI2IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 6:4 – SPI2TXIP[2:0] SPI2 Transfer Done Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – SPI2IP[2:0] SPI2 General Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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8.3.30 Interrupt Priority Register 10

Name: IPC10
Offset: 0xBC

Bit	15	14	13	12	11	10	9	8
		CCT3IP[2:0]						
Access		R/W	R/W	R/W				
Reset		1	0	0				

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 14:12 – CCT3IP[2:0] Capture/Compare/Timer3 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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8.3.31 Interrupt Priority Register 11

Name: IPC11
Offset: 0xBE

Bit	15	14	13	12	11	10	9	8
		CCT5IP[2:0]						
Access		R/W	R/W	R/W				
Reset		1	0	0				

Bit	7	6	5	4	3	2	1	0
						CCT4IP[2:0]		
Access						R/W	R/W	R/W
Reset						1	0	0

Bits 14:12 – CCT5IP[2:0] Capture/Compare/Timer5 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – CCT4IP[2:0] Capture/Compare/Timer4 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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8.3.32 Interrupt Priority Register 12

Name: IPC12
Offset: 0xC0

Bit	15	14	13	12	11	10	9	8
						MI2C2IP[2:0]		
Access						R/W	R/W	R/W
Reset						1	0	0

Bit	7	6	5	4	3	2	1	0
		SI2C2IP[2:0]						
Access		R/W	R/W	R/W				
Reset		1	0	0				

Bits 10:8 – MI2C2IP[2:0] I2C2 Host Events Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – SI2C2IP[2:0] I2C2 Client Events Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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8.3.33 Interrupt Priority Register 13

Name: IPC13
Offset: 0xC2

Bit	15	14	13	12	11	10	9	8
						INT4IP[2:0]		
Access						R/W	R/W	R/W
Reset						1	0	0

Bit	7	6	5	4	3	2	1	0
		INT3IP[2:0]						
Access		R/W	R/W	R/W				
Reset		1	0	0				

Bits 10:8 – INT4IP[2:0] External Interrupt 4 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – INT3IP[2:0] External Interrupt 3 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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8.3.34 Interrupt Priority Register 14

Name: IPC14
Offset: 0xC4

Bit	15	14	13	12	11	10	9	8
		SPI2RXIP[2:0]				SPI1RXIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 14:12 – SPI2RXIP[2:0] SPI2 Receive Done Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – SPI1RXIP[2:0] SPI1 Receive Done Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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8.3.35 Interrupt Priority Register 15

Name: IPC15
Offset: 0xC6

Bit	15	14	13	12	11	10	9	8
		CCP1IP[2:0]				RTCIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 14:12 – CCP1IP[2:0] Capture/Compare 1 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – RTCIP[2:0] Real-Time Clock and Calendar Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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8.3.36 Interrupt Priority Register 16

Name: IPC16
Offset: 0xC8

Bit	15	14	13	12	11	10	9	8
		CRCIP[2:0]				U2ERIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		U1ERIP[2:0]				CCP2IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – CRCIP[2:0] Cyclic Redundancy Check Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – U2ERIP[2:0] UART2 Error Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – U1ERIP[2:0] UART2 Error Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – CCP2IP[2:0] Capture/Compare 2 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3

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Value	Description
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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8.3.37 Interrupt Priority Register 18

Name: IPC18
Offset: 0xCC

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						HLVDIP[2:0]		
Access						R/W	R/W	R/W
Reset						1	0	0

Bits 2:0 – HLVDIP[2:0] High/Low-Voltage Detect Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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8.3.38 Interrupt Priority Register 21

Name: IPC21
Offset: 0xD2

Bit	15	14	13	12	11	10	9	8
						USB1IP[2:0]		
Access						R/W	R/W	R/W
Reset						1	0	0

Bit	7	6	5	4	3	2	1	0
		I2C2BCIP[2:0]				I2C1BCIP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 10:8 – USB1IP[2:0] USB OTG 1 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – I2C2BCIP[2:0] I2C2 Bus Collision Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – I2C1BCIP[2:0] I2C1 Bus Collision Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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8.3.39 Interrupt Priority Register 23

Name: IPC23
Offset: 0xD6

Bit	15	14	13	12	11	10	9	8
		CCP4IP[2:0]				CCP3IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 14:12 – CCP4IP[2:0] Capture/Compare 4 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – CCP3IP[2:0] Capture/Compare 3 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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8.3.40 Interrupt Priority Register 24

Name: IPC24
Offset: 0xD8

Bit	15	14	13	12	11	10	9	8
		CLC4IP[2:0]				CLC3IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bit	7	6	5	4	3	2	1	0
		CLC2IP[2:0]				CLC1IP[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	0	0		1	0	0

Bits 14:12 – CLC4IP[2:0] Configurable Logic Cell 4 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 10:8 – CLC3IP[2:0] Configurable Logic Cell 3 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 6:4 – CLC2IP[2:0] Configurable Logic Cell 2 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

Bits 2:0 – CLC1IP[2:0] Configurable Logic Cell 1 Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3

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Value	Description
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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8.3.41 Interrupt Priority Register 26

Name: IPC26
Offset: 0xDC

Bit	15	14	13	12	11	10	9	8
						FSTIP[2:0]		
Access						R/W	R/W	R/W
Reset						1	0	0

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 10:8 – FSTIP[2:0] FRC Self-Tuning Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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8.3.42 Interrupt Priority Register 27

Name: IPC27
Offset: 0xDE

Bit	15	14	13	12	11	10	9	8
						RTCCTSIP[2:0]		
Access						R/W	R/W	R/W
Reset						1	0	0

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 10:8 – RTCCTSIP[2:0] Real-Time Clock and Calendar Timestamp Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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8.3.43 Interrupt Priority Register 29

Name: IPC29
Offset: 0xE2

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		JTAGIP[2:0]						
Access		R/W	R/W	R/W				
Reset		1	0	0				

Bits 6:4 – JTAGIP[2:0] JTAG Interrupt Priority bits

Value	Description
7	Interrupt Priority Level 7 (highest)
6	Interrupt Priority Level 6
5	Interrupt Priority Level 5
4	Interrupt Priority Level 4 (default)
3	Interrupt Priority Level 3
2	Interrupt Priority Level 2
1	Interrupt Priority Level 1
0	Interrupt Priority Level 0 (lowest)

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8.3.44 Interrupt Control and Status Register

Name: INTTREG
Offset: 0xE4

Note:
1. See Table 8-1 and Table 8-2 for the vector numbers.

Bit	15	14	13	12	11	10	9	8
	CPUIRQ		VHOLD		ILR[3:0]			
Access	R		R/W		R	R	R	R
Reset	0		0		0	0	0	0

Bit	7	6	5	4	3	2	1	0
	VECNUM[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 15 – CPUIRQ Interrupt Request from Interrupt Controller to CPU bit

Value	Description
1	An interrupt request has occurred but has not yet been Acknowledged by the CPU; this happens when the CPU priority is higher than the interrupt priority
0	No interrupt request is unacknowledged

Bit 13 – VHOLD Vector Number Capture Configuration bit

Value	Description
1	The VECNUMx bits contain the value of the highest priority pending interrupt
0	The VECNUMx bits contain the value of the last Acknowledged interrupt (i.e., the last interrupt that has occurred with higher priority than the CPU, even if other interrupts are pending)

Bits 11:8 – ILR[3:0] New CPU Interrupt Priority Level bits

Value	Description
1111	New CPU Interrupt Priority Level bits
...	
0001	CPU Interrupt Priority Level is 1
0000	CPU Interrupt Priority Level is 0

Bits 7:0 – VECNUM[7:0] Vector Number of Pending Interrupt bits(1)

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9. Oscillator Configuration

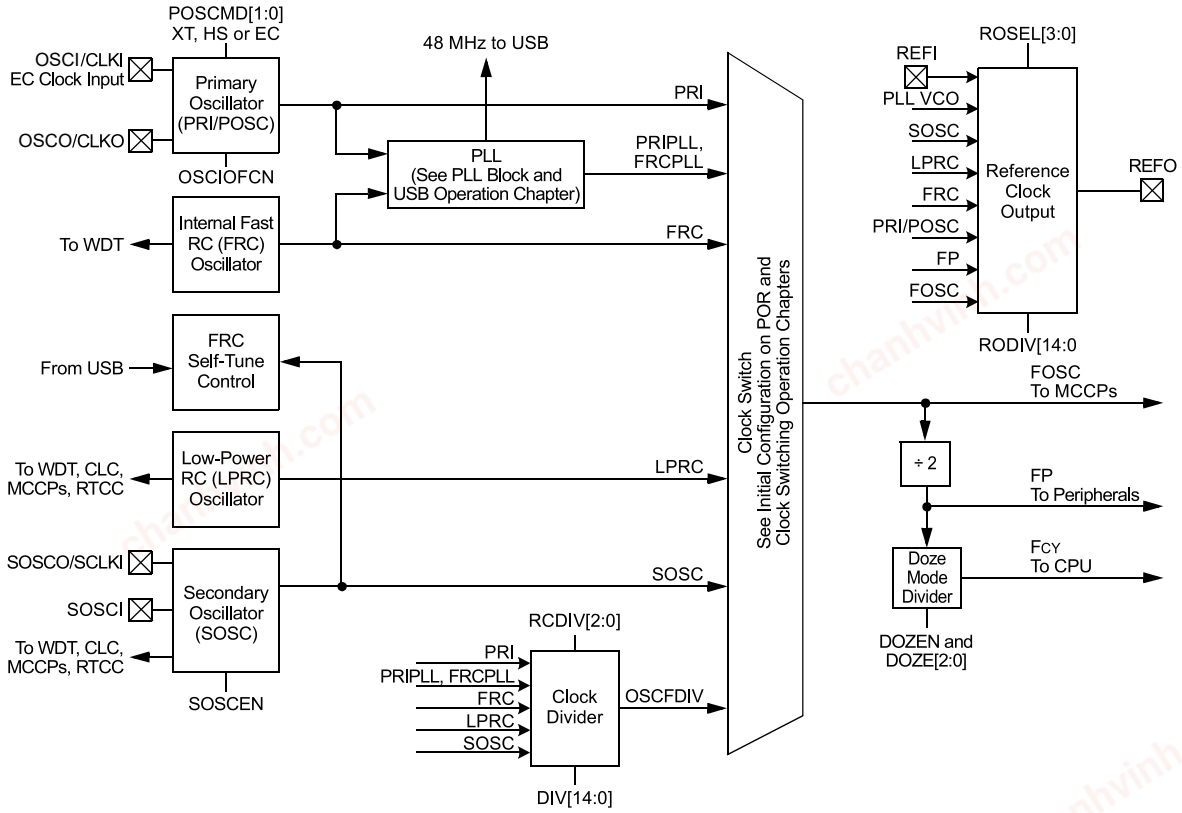
Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to **"Oscillator"** (www.microchip.com/DS39700) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

The oscillator system for the PIC24FJ64GP205/GU205 family devices has the following features:

- An On-Chip PLL Block to Provide a Range of Frequency Options for the System Clock
- Software-Controllable Switching between Various Clock Sources
- Software-Controllable Postscaler for Selective Clocking of CPU for System Power Savings
- A Fail-Safe Clock Monitor (FSCM) that Detects Clock Failure and Permits Safe Application Recovery or Shutdown
- A Separate and Independently Configurable System Clock Output for Synchronizing External Hardware

A simplified diagram of the oscillator system is shown in Figure 9-1.

Figure 9-1. PIC24FJ64GP205/GU205 Family Clock Diagram



The system clock source can be provided by one of the following sources:

- Primary Oscillator (PRI or POSC) on the OSCI and OSCO pins
- Fast Internal RC (FRC) Oscillator (8 MHz)
- Primary Oscillator with PLL (PRIPLL)
- Fast Internal RC Oscillator with PLL (FRCPLL)
- Secondary Oscillator (SOSC) on the SOSCI and SOSCO pins
- Low-Power Internal RC (LPRC) Oscillator (32 kHz)

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The Primary Oscillator and FRC sources have the option of using the internal PLL block, which can generate a 4x, 6x or 8x PLL clock. If the PLL is used, the PLL clocks can then be postscaled, if necessary, and used as the system clock. Refer to 9.8 PLL Block and USB Operation for additional information.

Each clock source (PRIPLL, FRCPLL, PRI, FRC, LPRC and SOSC) can be used as an input to an additional divider, which can then be used to produce a divided clock source for use as a system clock (OSCFDIV).

The selected clock source generates the processor and peripheral clock sources. The processor clock source is divided by two to produce the internal instruction cycle clock, F_{CY}. In this document, the instruction cycle clock is also denoted by Fosc/2. The internal instruction cycle clock, $F_{OSC}/2$, can be provided on the OSCO I/O pin for the EC operating mode of the Primary Oscillator.

9.1 Initial Configuration on POR

The oscillator source (and operating mode) that is used at a device Power-on Reset event is selected using Configuration bit settings. The Oscillator Configuration bit settings are located in the Configuration registers in the program memory (refer to 4.3 Configuration Bits Overview for further details). The Primary Oscillator Configuration bits, POSCMD[1:0] (FOSC[1:0]), and the Oscillator Select Configuration bits, FNOSC[2:0] (FOSCSEL[2:0]), select the oscillator source that is used at a Power-on Reset.

9.2 Clock Switching Operation

With few limitations, applications are free to switch between any of the clock sources under software control and at any time. To limit the possible side effects that could result from this flexibility, PIC24F devices have a safeguard lock built into the switching process.

Note: The Primary Oscillator mode has three different submodes (XT, HS and EC), which are determined by the POSCMD[1:0] Configuration bits. While an application can switch to and from Primary Oscillator mode in software, it cannot switch between the different Primary Oscillator submodes without reprogramming the device.

9.2.1 Enabling Clock Switching

To enable clock switching, the FCKSM[1:0] Configuration bits in FOSC must be programmed to '0x'. (Refer to 27.1 Configuration Bits for further details.) If the FCKSM[1:0] Configuration bits are programmed to '1x', the clock switching function is disabled; this is the default setting.

The NOSC[1:0] control bits (OSCCON[10:8]) do not control the clock selection when clock switching is disabled. However, the COSC[2:0] bits (OSCCON[14:12]) will reflect the clock source selected by the FOSC Configuration bits.

The OSWEN control bit (OSCCON[0]) has no effect when clock switching is disabled; it is held at '0' at all times.

9.2.2 Oscillator Switching Sequence

At a minimum, performing a clock switch requires this basic sequence:

1. If desired, read the COSC[2:0] bits (OSCCON[14:12]) to determine the current oscillator source.
2. Perform the unlock sequence to allow a write to the OSCCON register high byte.
3. Write the appropriate value to the NOSC[2:0] bits (OSCCON[10:8]) for the new oscillator source.
4. Perform the unlock sequence to allow a write to the OSCCON register low byte.
5. Set the OSWEN bit to initiate the oscillator switch.

Once the basic sequence is completed, the system clock hardware responds automatically as follows:

The clock switching hardware compares the COSC[2:0] bits with the new value of the NOSC[2:0] bits. If they are the same, then the clock switch is a redundant operation. In this case, the OSWEN bit is cleared automatically and the clock switch is aborted.

If a valid clock switch has been initiated, the LOCK (OSCCON[5]) and CF (OSCCON[3]) bits are cleared.

The new oscillator is turned on by the hardware if it is not currently running. If a crystal oscillator must be turned on, the hardware will wait until it is ready. If the new source is using the PLL, then the hardware waits until a PLL lock is detected (LOCK = 1).

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The hardware waits for ten clock cycles from the new clock source and then performs the clock switch.

The hardware clears the OSWEN bit to indicate a successful clock transition. In addition, the NOSC[2:0] bits value is transferred to the COSC[2:0] bits.

The old clock source is turned off at this time, unless this oscillator is needed for other modules.

The processor will continue to execute code throughout the clock switching sequence. Timing-sensitive code should not be executed during this time.

Direct clock switches between any Primary Oscillator mode with PLL and FRC with PLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.

A recommended code sequence for a clock switch includes the following:

1. Disable interrupts during the OSCCON register unlock and write sequence.
2. Execute the unlock sequence for the OSCCON high byte by writing 78h and 9Ah to OSCCON[15:8] in two back-to-back instructions.
3. Write the new oscillator source to the NOSCx bits in the instruction immediately following the unlock sequence.
4. Execute the unlock sequence for the OSCCON low byte by writing 46h and 57h to OSCCON[7:0] in two back-to-back instructions.
5. Set the OSWEN bit in the instruction immediately following the unlock sequence.
6. Continue to execute code that is not clock-sensitive (optional).
7. Invoke an appropriate amount of software delay (cycle counting) to allow the selected oscillator and/or PLL to start and stabilize.
8. Check to see if OSWEN is '0'; if it is, the switch was successful. If OSWEN is still set, then check the LOCK bit to determine the cause of the failure.

The assembler code sequence for unlocking the OSCCON register and initiating a clock switch is shown below:

Example 9-1. Unlocking OSCCON and Initiating a Clock Switch

```
; OSCCONH (high byte) Unlock Sequence
mov   #OSCCONH, w1
mov   #0x78, w2
mov   #0x9A, w3
mov.b w2, [w1]
mov.b w3, [w1]
; Set new oscillator selection
mov   #<New Clock Option Number>, w0
mov.b w0, OSCCONH
; OSCCONL (low byte) unlock sequence
mov   #OSCCONL, w1
mov   #0x46, w2
mov   #0x57, w3
mov.b w2, [w1]
mov.b w3, [w1]
; Start oscillator switch operation
bset  OSCCON, #0
```

The MPLAB® XC16 C compiler offers "built-in" functions for the clock switching as follows:

Example:

```
__builtin_write_OSCCONH(<New Clock Option Number>);
__builtin_write_OSCCONL(OSCCON | 0x01);     // Start oscillator switch operation
```

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9.3 Fail-Safe Clock Monitor (FSCM)

The Fail-Safe Clock Monitor (FSCM) detects clock failures. In case of a clock problem, the Fail-Safe Clock Monitor switches the clock to the on-chip Low-Power RC oscillator (LPRC) and generates the oscillator trap. To enable clock switching, the FCKSM[1:0] Configuration bits in FOSC must be programmed to '00'.

9.4 Internal Fast RC (FRC) Oscillator with Active Clock Tuning

The FRC includes an automatic mechanism to calibrate the frequency during run time. This system uses active clock tuning from a source of known accuracy to maintain the FRC within a very narrow margin of its nominal 8 MHz frequency. The TUN[5:0] bits in the OSCTUN register allow applications to fine-tune the FRC Oscillator over a range of approximately ±1.5%.

The self-tune system is controlled by the bits in the upper half of the OSCTUN register. Setting the STEN bit (OSCTUN[15]) enables the self-tuning feature, allowing the hardware to calibrate to a source selected by the STSRC bit (OSCTUN[12]).

When STSRC = 0, the system uses the crystal-controlled SOSC for its calibration source. Regardless of the source, the system uses the TUN[5:0] bits (OSCTUN[5:0]) to change the FRC Oscillator's frequency. Frequency monitoring and adjustment are dynamic, occurring continuously during run time. While the system is active, the TUN[5:0] bits cannot be written to by software.

The self-tune system can generate a hardware interrupt, FSTIF. The interrupt can result from a drift of the FRC from the reference, by greater than 0.2% in either direction, or whenever the frequency deviation is beyond the ability of the TUN[5:0] bits to correct (i.e., greater than 1.5%). The STLOCK and STOR status bits (OSCTUN[11,9]) are used to indicate these conditions.

The STLPOL and STORPOL bits (OSCTUN[10,8]) configure the FSTIF interrupt to occur in the presence or the absence of the conditions. It is the user's responsibility to monitor both the STLOCK and STOR bits to determine the exact cause of the interrupt.

Note: The STLPOL and STORPOL bits should be ignored when the self-tune system is disabled (STEN = 0).

9.5 Primary Oscillator (PRI or POSC)

The PIC24FJ64GP205/GU205 family devices feature a Primary Oscillator (POSC), which is available on the OSCI and OSCO pins. This connection enables an external crystal (or ceramic resonator) to provide the clock to the device. The Primary Oscillator provides three modes of operation:

- Medium Speed Oscillator (XT Mode): The XT mode is a Medium Gain, Medium Frequency mode used to work with crystal frequencies of 3.5 MHz to 10 MHz.
- High-Speed Oscillator (HS Mode): The HS mode is a High-Gain, High-Frequency mode used to work with crystal frequencies of 10 MHz to 32 MHz.
- External Clock Source Operation (EC Mode): If the crystal driver is disabled, the EC mode allows the internal oscillator to be bypassed. The device clocks are generated from an external source (0 MHz to up to 64 MHz) and input on the CLKI pin.

9.6 Low-Power RC (LPRC) Oscillator

The PIC24FJ64GP205/GU205 family devices contain one instance of the Low-Power RC (LPRC) Oscillator and provides a nominal clock frequency of 32 kHz. The LPRC Oscillator is the clock source for the Power-up Timer (PWRT), Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM) circuits in the clock subsystem. The LPRC Oscillator is enabled at power-on. The LPRC Oscillator remains enabled under these conditions:

- The FSCM is enabled
- The WDT is enabled
- The LPRC Oscillator is selected as the system clock

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If none of these conditions is true, the LPRC Oscillator shuts off after the PWRT expires. The LPRC Oscillator is shut off in Sleep mode.

9.7 Secondary Oscillator (SOSC)

9.7.1 Basic Operation

PIC24FJ64GP205/GU205 family devices do not have to set the SOSCEN bit to use the Secondary Oscillator. Any module requiring the SOSC (such as the RTCC or Timer1) will automatically turn on the SOSC when the clock signal is needed. The SOSC, however, has a long start-up time (as long as one second). To avoid delays for peripheral start-up, the SOSC can be manually started using the SOSCEN bit.

To use the Secondary Oscillator, the SOSCSEL bit (FOSC[3]) must be set to '1'. Programming the SOSCSEL bit to '0' configures the SOSC pins for Digital mode, enabling digital I/O functionality on the pins.

9.7.2 Crystal Selection

The 32.768 kHz crystal used for the SOSC must have the following specifications in order to properly start up and run at the correct frequency when the SOSC is in High-Power mode (default):

- 12.5 pF loading capacitance
- 1.0 pF shunt capacitance
- A typical ESR of 35k-50k; 70k maximum

In addition, the two external crystal loading capacitors should be in the range of 18 pF-22 pF, which will be based on the PC board layout. The capacitors should be C0G, 5% tolerance and rated 25V or greater.

The accuracy and duty cycle of the SOSC can be measured on the REFO pin, and is recommended to be in the range of 40-60% and accurate to ±0.65 Hz.

9.7.3 Low-Power Operation

The Secondary Oscillator can operate in two distinct levels of power consumption based on device configuration. In Low-Power mode, the oscillator operates in a low drive strength, low-power state. By default, the oscillator uses a higher drive strength, and therefore, requires more power. Low-Power mode is selected by Configuration bit, SOSCHP (FDEVOPT1[3]). The lower drive strength of this mode makes the SOSC more sensitive to noise and requires a longer start-up time. This mode can be used with lower load capacitance crystals (6 pF-9 pF) to reduce Sleep current in the RTCC. When Low-Power mode is used, care must be taken in the design and layout of the SOSC circuit to ensure that the oscillator starts up and oscillates properly. PC board layout issues, stray capacitance and other factors will need to be carefully controlled in order for the crystal to operate.

9.8 PLL Block and USB Operation

The PLL block, shown in Figure 9-2, can generate a wide range of clocks used for both parts with USB functionality (PIC24FJXXGU2XX devices) and non-USB functionality (PIC24FJXXGP2XXPIC24FJXXXGL4XX devices). All of the PLL modes are available regardless if USB is present or not.

The PLL input clock source (FRC or POSC) is controlled by the COSC[2:0] bits (OSCCON[14:12]) if the PLL output is used as a system clock. When COSC[2:0] = 001 (FRCPLL), the PLL is clocked from FRC. When COSC[2:0] = 011 (PRIPLL), the Primary Oscillator (POSC) is connected to the PLL. The default COSC[2:0] value is selected by the FNOSC[2:0] Configuration bits (FOSCSEL[2:0]). Also, REFO can use the PLL when it is not selected for the system clock (COSC[2:0] bits (OSCCON[14:12]) are not '001' or '011'). In this case, the PLL clock source is selected by the PLLSS Configuration bit (FOSC[4]). If PLLSS is cleared ('0'), the PLL is fed by the FRC Oscillator. If the PLLSS Configuration bit is not programmed ('1'), the PLL is clocked from the Primary Oscillator.

When used in a USB application, the 48 MHz internal clock must be running at all times, which requires the VCO of the PLL to run at 96 MHz. This, in turn, forces the system clock (that drives the CPU and peripherals) to route the 96 MHz through a fixed divide-by-3 block (generating 32 MHz) and then through a selection of four fixed divisors ('postscaler'). The postscaler controlled by the CPDIV[1:0] bits output becomes the system clock.

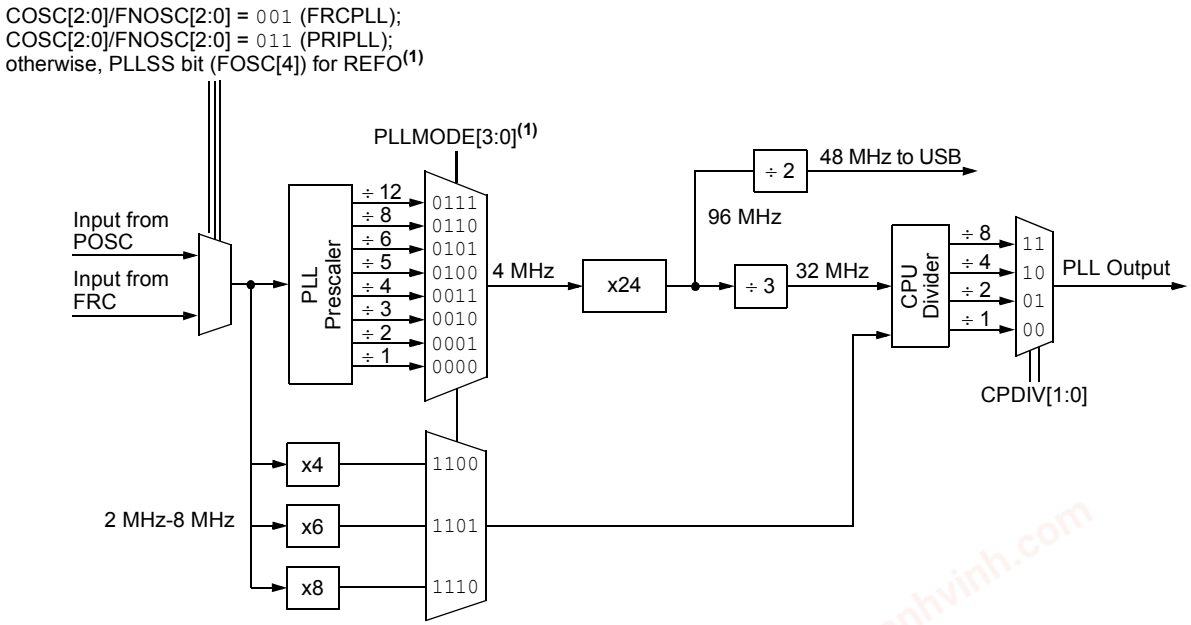
The input to the PLL must be 4 MHz when used in a USB application, which restricts the frequency input sources to be used with a small set of fixed frequency dividers (see Figure 9-2). The 96 MHz (USB) PLL prescaler is configured

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by the PLLMODE[3:0] Configuration bits. For example, if a 12 MHz crystal is used, the PLLMODE[3:0] Configuration bits must be set for divide-by-3 to generate the required 4 MHz. A popular baud rate crystal is 11.0592 MHz, but this value cannot be used for USB operation as there are no divisors available to generate 4 MHz exactly.

Non-USB operation allows a wider range of PLL input frequencies. The multiplier ratios can be selected as 4x, 6x or 8x. There is no clock prescaler. The postscaler (CPDIV[1:0]) is available and can be used to reduce the system clock to meet the 32 MHz maximum frequency specification. Note that the minimum input frequency to the PLL is 2 MHz, but the range is from 2 MHz to 8 MHz.

Figure 9-2. PLL Block



Note:

1. The FNOSC[2:0], PLLMODE[3:0] and PLLSS bits are in the configuration area. See the FOSC and FOSCSEL Configuration registers (27.1.6 FOSC and 27.1.5 FOSCSEL) for more information.

9.9 Reference Clock Output

In addition to the CLKO output ($F_{OSC}/2$), the device clock in the PIC24FJ64GP205/GU205 family devices can also be configured to provide a reference clock output signal to a port pin. This feature is available in all oscillator configurations and allows the user to select a greater range of clock submultiples to drive external devices in the application. CLKO is enabled by Configuration bit, OSCIOFCN, and is independent of the REFO reference clock. REFO is mappable to any I/O pin that has mapped output capability. Refer to Table 11-3 for more information.

This reference clock output is controlled by the REFOCONL and REFOCONH registers. Setting the ROEN bit (REFOCONL[15]) makes the clock signal available on the REFO pin. The RODIV[14:0] bits (REFOCONH[14:0]) enable the selection of different clock divide options. The ROSWEN bit (REFOCONL[9]) indicates that the clock divider has successfully switched. In order to change the divider, the user should wait until this bit has been cleared. Write the updated values to RODIV[14:0], set the ROSWEN bit and then wait until it is cleared before assuming that the REFO clock is valid.

The ROSEL[3:0] bits (REFOCONL[3:0]) determine which clock source is used for the reference clock output. The ROSLP bit (REFOCONL[11]) determines if the reference source is available on REFO when the device is in Sleep mode.

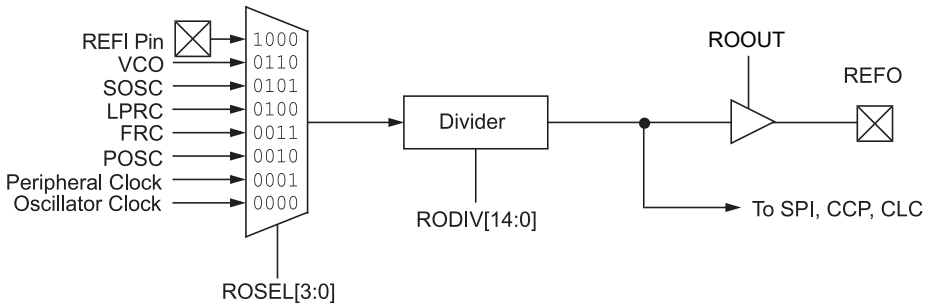
The ROOUT bit enables/disables the reference clock output on the REFO pin.

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The ROACTIVE bit (REFOCONL[8]) indicates that the module is active; it can be cleared by disabling the module (setting ROEN to '0'). The user must not change the reference clock source or adjust the divider when the ROACTIVE bit indicates that the module is active. To avoid glitches, the user should not disable the module until the ROACTIVE bit is '1'.

The PLLSS Configuration bit (FOSC[4]), when cleared, can be used to generate a REFO clock with the PLL that is independent of the system clock. For example, if the system clock is using FRC at 8 MHz, the PLL can use the FRC as the input and generate 32 MHz (PLL 4x mode) out of REFO.

Figure 9-3. Reference Clock Generator



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9.10 Oscillator Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0xFF	Reserved									
0x0100	OSCCON(1)	7:0	CLKLOCK	IOLOCK	LOCK		CF	POSCEN	SOSCEN	OSWEN
		15:8			COSC[2:0]				NOSC[2:0]	
0x0102	CLKDIV	7:0	CPDIV[1:0]		PLLEN					
		15:8	ROI		DOZE[2:0]		DOZEN		RCDIV[2:0]	
0x0104 ... 0x0105	Reserved									
0x0106	OSCTUN	7:0			TUN[5:0]					
		15:8	STEN		STSIDL	STSRC	STLOCK	STLPOL	STOR	STORPOL
0x0108 ... 0x010B	Reserved									
0x010C	OSCDIV	7:0	DIV[7:0]							
		15:8		DIV[14:8]						
0x010E	OSCFDIV(1)	7:0	TRIM[0]							
		15:8		TRIM[7:1]						
0x0110 ... 0x0167	Reserved									
0x0168	REFOCONL	7:0					ROSEL[3:0]			
		15:8	ROEN		ROSIDL	ROOUT	ROSLP		ROSWEN	ROACTIV
0x016A	REFOCONH	7:0	RODIV[7:0]							
		15:8		RODIV[14:8]						

9.10.1 Control Registers Overview

The OSCCON register is the main control register for the oscillator. It controls clock source switching and allows the monitoring of clock sources. OSCCON is protected by a write lock to prevent inadvertent clock switches. See 9.2 Clock Switching Operation for more information.

The CLKDIV register controls the features associated with Doze mode, as well as the postscalers for the OSCFDIV Clock mode and the PLL module.

The OSCDIV and OSCFDIV registers provide control for the system oscillator frequency divider.

The REFOCONL and REFOCONH registers control the reference clock feature.

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9.10.2 FRC Oscillator Tuning Register

Name: OSCTUN
Offset: 0x106

Note:

1. Use of either clock tuning reference source has specific application requirements. See 9.4 Internal Fast RC (FRC) Oscillator with Active Clock Tuning for details.
2. These bits are read-only when STEN = 1.

Bit	15	14	13	12	11	10	9	8
	STEN		STSIDL	STSRC	STLOCK	STLPOL	STOR	STORPOL
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			TUN[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit 15 – STEN FRC Self-Tune Enable bit

Value	Description
1	FRC self-tuning is enabled; TUNx bits are controlled by hardware
0	FRC self-tuning is disabled; application may optionally control the TUNx bits

Bit 13 – STSIDL FRC Self-Tune Stop in Idle bit

Value	Description
1	Self-tuning stops during Idle mode
0	Self-tuning continues during Idle mode

Bit 12 – STSRC FRC Self-Tune Reference Clock Source bit(1)

Value	Description
1	FRC approximately matches the USB host clock tolerance
0	FRC approximately matches the 32.768 kHz SOSC tolerance

Bit 11 – STLOCK FRC Self-Tune Lock Status bit

Value	Description
1	FRC accuracy is currently within ±0.2% of the STSRC reference accuracy
0	FRC accuracy may not be within ±0.2% of the STSRC reference accuracy

Bit 10 – STLPOL FRC Self-Tune Lock Interrupt Polarity bit

Value	Description
1	A self-tune lock interrupt is generated when STLOCK is '0'
0	A self-tune lock interrupt is generated when STLOCK is '1'

Bit 9 – STOR FRC Self-Tune Out of Range Status bit

Value	Description
1	STSRC reference clock error is beyond the range of TUN[5:0]; no tuning is performed
0	STSRC reference clock is within the tunable range; tuning is performed

Bit 8 – STORPOL FRC Self-Tune Out of Range Interrupt Polarity bit

Value	Description
1	A self-tune out of range interrupt is generated when STOR is '0'
0	A self-tune out of range interrupt is generated when STOR is '1'

Bits 5:0 – TUN[5:0] FRC Oscillator Tuning bits(2)

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Value	Description
011111	Maximum frequency deviation
011110	
...	
000001	
000000	Center frequency oscillator is running at factory calibrated frequency
111111	
...	
100001	
100000	Minimum frequency deviation

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9.10.3 Oscillator Control Register

Name: OSCCON(1)
Offset: 0x100

Notes:

1. OSCCON is protected by a write lock to prevent inadvertent clock switches. See 9.2 Clock Switching Operation for more information.
2. Reset values for these bits are determined by the FNOSCx Configuration bits.
3. The state of the IOLOCK bit can only be changed once an unlocking sequence has been executed. In addition, if the IOL1WAY Configuration bit is '1', once the IOLOCK bit is set, it cannot be cleared.
4. This bit also resets to '0' during any valid clock switch or whenever a non-PLL Clock mode is selected.

Legend: y = Value Set from Configuration bits on POR

Bit	15	14	13	12	11	10	9	8
		COSC[2:0]				NOSC[2:0]		
Access		R	R	R		R/W	R/W	R/W
Reset		0	0	x		y	y	y

Bit	7	6	5	4	3	2	1	0
	CLKLOCK	IOLOCK	LOCK		CF	POSCEN	SOSCEN	OSWEN
Access	R/W	R/W	R/W		R/W	R/W	R/W	R/W
Reset	0	0	0		0	0	0	0

Bits 14:12 – COSC[2:0] Current Oscillator Selection bits(2)

Value	Description
111	Oscillator with Frequency Divider (OSCFDIV)
110	Reserved
101	Low-Power RC Oscillator (LPRC)
100	Secondary Oscillator (SOSC)
011	Primary Oscillator with PLL module (XTPLL, ECPLL)
010	Primary Oscillator (XT, HS, EC)
001	Fast RC Oscillator with PLL module (FRCPLL)
000	Fast RC Oscillator (FRC)

Bits 10:8 – NOSC[2:0] New Oscillator Selection bits(2)

Value	Description
111	Oscillator with Frequency Divider (OSCFDIV)
110	Reserved
101	Low-Power RC Oscillator (LPRC)
100	Secondary Oscillator (SOSC)
011	Primary Oscillator with PLL module (XTPLL, ECPLL)
010	Primary Oscillator (XT, HS, EC)
001	Fast RC Oscillator with PLL module (FRCPLL)
000	Fast RC Oscillator (FRC)

Bit 7 – CLKLOCK Clock Lock Enable bit

Value	Description
	If FSCM is Enabled (FCKSM[1:0] = 00):
1	Clock and PLL selections are locked
0	Clock and PLL selections are not locked and may be modified by setting the OSWEN bit
	If FSCM is Disabled (FCKSM[1:0] = 1x):
	Clock and PLL selections are never locked and may be modified by setting the OSWEN bit.

Bit 6 – IOLOCK I/O Lock Enable bit(3)

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Value	Description
1	I/O lock is active
0	I/O lock is not active

Bit 5 – LOCK PLL Lock Status bit(4)

Value	Description
1	PLL module is in lock or PLL module start-up timer is satisfied
0	PLL module is out of lock, PLL start-up timer is running or PLL is disabled

Bit 3 – CF Clock Fail Detect bit

Value	Description
1	FSCM has detected a clock failure
0	FSCM has not detected a clock failure

Bit 2 – POSCEN Primary Oscillator Sleep Enable bit

Value	Description
1	Primary Oscillator continues to operate during Sleep mode
0	Primary Oscillator is disabled during Sleep mode

Bit 1 – SOSCEN 32 kHz Secondary Oscillator (SOSC) Enable bit

Value	Description
1	Enables Secondary Oscillator
0	Disables Secondary Oscillator

Bit 0 – OSWEN Oscillator Switch Enable bit

Value	Description
1	Initiates an oscillator switch to a clock source specified by the NOSC[2:0] bits
0	Oscillator switch is complete

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9.10.4 Clock Divider Register

Name: CLKDIV
Offset: 0x102

Note:

1. This bit is automatically cleared when the ROI bit is set and an interrupt occurs.

Bit	15	14	13	12	11	10	9	8
	ROI	DOZE[2:0]			DOZEN	RCDIV[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	1	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CPDIV[1:0]		PLLEN					
Access	R/W	R/W	R/W					
Reset	0	0	1					

Bit 15 – ROI Recover on Interrupt bit

Value	Description
1	Interrupts will clear the DOZEN bit and the processor clock, and the peripheral clock ratio is set to 1:1
0	Interrupts have no effect on the DOZEN bit

Bits 14:12 – DOZE[2:0] CPU Peripheral Clock Ratio Select bits

Value	Description
111	1:128
110	1:64
101	1:32
100	1:16
011	1:8 (default)
010	1:4
001	1:2
000	1:1

Bit 11 – DOZEN Doze Mode Enable bit(1)

Value	Description
1	DOZE[2:0] bits specify the CPU peripheral clock ratio
0	CPU peripheral clock ratio is set to 1:1

Bits 10:8 – RCDIV[2:0] System Frequency Divider Clock Source Select bits

Value	Description
111	Reserved; do not use
110	Reserved
101	Low-Power RC Oscillator (LPRC)
100	Secondary Oscillator (SOSC)
011	Primary Oscillator (XT, HS, EC) with PLL module (XTPLL, HSPLL, ECPLL)
010	Primary Oscillator (XT, HS, EC)
001	Fast RC Oscillator (FRC) with PLL module (FRCPLL)
000	Fast RC Oscillator (FRC)

Bits 7:6 – CPDIV[1:0] System Clock Select bits (postscaler select from PLL, 32 MHz clock branch)

Value	Description
11	Divide by 8
10	Divide by 4
01	Divide by 2
00	Divide by 1 (default)

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Bit 5 – PLLEN PLL Enable bit

Value	Description
1	PLL is always active (including Sleep modes)
0	PLL is only active when a PLL Oscillator mode is selected (OSCCON[14:12] = 001 or 011)

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9.10.5 Oscillator Divisor Register

Name: OSCDIV
Offset: 0x10C

Bit	15	14	13	12	11	10	9	8
		DIV[14:8]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DIV[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 14:0 – DIV[14:0] Reference Clock Divider bits
Specifies the 1/2 period of the reference clock in the source clocks
(ex: Period of ref_clk_output = [Reference Source * 2] * DIV[14:0]).

Value	Description
111111111111111	Oscillator frequency divided by 65,534 (32,767 * 2)
111111111111110	Oscillator frequency divided by 65,532 (32,766 * 2)
. . .	
000000000000011	Oscillator frequency divided by 6 (3 * 2)
000000000000010	Oscillator frequency divided by 4 (2 * 2)
000000000000001	Oscillator frequency divided by 2 (1 * 2) (default)
000000000000000	Oscillator frequency is unchanged (no divider)

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9.10.6 Oscillator Fractional Divisor Register

Name: OSCFDIV(1)
Offset: 0x10E

Note:

1. TRIMx values greater than zero are ONLY valid when DIVx values are greater than zero.

Bit	15	14	13	12	11	10	9	8
		TRIM[7:1]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRIM[0]							
Access	R/W							
Reset	0							

Bits 14:7 – TRIM[7:0] Trim bits
Provides fractional additive to the DIV[14:0] bits value for the 1/2 period of the oscillator clock.

Value	Description
000000000	0/512 (0.0) divisor added to DIVx value
000000001	1/512 (0.001953125) divisor added to DIVx value
000000010	2/512 (0.00390625) divisor added to DIVx value
. . .	
100000000	256/512 (0.5000) divisor added to DIVx value
111111110	510/512 (0.99609375) divisor added to DIVx value
111111111	511/512 (0.998046875) divisor added to DIVx value

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9.10.7 Reference Oscillator Control Register Low

Name: REFOCONL
Offset: 0x168

Legend: HC = Hardware Clearable bit

Bit	15	14	13	12	11	10	9	8
	ROEN		ROSIDL	ROOUT	ROSLP		ROSWEN	ROACTIV
Access	R/W		R/W	R/W	R/W		R/W/HC	R
Reset	0		0	0	0		0	0

Bit	7	6	5	4	3	2	1	0
					ROSEL[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – ROEN Reference Oscillator Output Enable bit

Value	Description
1	Reference Oscillator module is enabled
0	Reference Oscillator module is disabled

Bit 13 – ROSIDL REFO Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode
0	Continues module operation in Idle mode

Bit 12 – ROOUT Reference Clock Output Enable bit

Value	Description
1	Reference clock is driven out on the REFO pin
0	Reference clock is not driven out on the REFO pin

Bit 11 – ROSLP Reference Oscillator Output Stop in Sleep bit

Value	Description
1	Reference Oscillator continues to run in Sleep mode
0	Reference Oscillator is disabled in Sleep mode

Bit 9 – ROSWEN Reference Clock RODIVx Switch Enable bit

Value	Description
1	Switches clock divider; clock divider switching is currently in progress
0	Clock divider switch has been completed

Bit 8 – ROACTIV Reference Clock Request Status bit

Value	Description
1	Reference clock is active (user should not change the REFO settings)
0	Reference clock is inactive (user can update the REFO settings)

Bits 3:0 – ROSEL[3:0] Reference Clock Source Select bits

Value	Description
1111-1001	Reserved
1000	REFI pin
0111	Reserved
0110	PLL VCO (PLL output before postscaler)
0101	SOSC
0100	LPRC
0011	FRC

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Value	Description
0010	POSC
0001	System clock ($F_{OSC}/2$)
0000	F_{OSC}

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9.10.8 Reference Oscillator Control Register High

Name: REFOCONH
Offset: 0x16A

Bit	15	14	13	12	11	10	9	8
		RODIV[14:8]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RODIV[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 14:0 – RODIV[14:0] Reference Clock Divider bits
Specifies 1/2 period of the reference clock in the source clocks (ex: Period of Output = [Reference Source * 2] * RODIV[14:0]; this equation does not apply to RODIV[14:0] = 0).

Value	Description
111111111111111	REFO clock is the base clock frequency divided by 65,534 (32,767 * 2)
111111111111110	REFO clock is the base clock frequency divided by 65,532 (32,766 * 2)
...	
000000000000011	REFO clock is the base clock frequency divided by 6 (3 * 2)
000000000000010	REFO clock is the base clock frequency divided by 4 (2 * 2)
000000000000001	REFO clock is the base clock frequency divided by 2 (1 * 2)
000000000000000	REFO clock is the same frequency as the base clock (no divider)

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10. Power-Saving Features

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to **"Power-Saving Features with Deep Sleep"** (www.microchip.com/DS39727) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

The PIC24FJ64GP205/GU205 family of devices provides the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of circuits being clocked constitutes lower consumed power. All PIC24F devices manage power consumption in four different ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption, while still maintaining critical application features, such as timing-sensitive communications.

10.1 Clock Frequency and Clock Switching

PIC24F devices allow for a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSC[2:0] bits. The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in 9. Oscillator Configuration.

10.2 Instruction-Based Power-Saving Modes

PIC24F devices have two special power-saving modes that are entered through the execution of a special `PWRSAV` instruction. Sleep mode stops clock operation and halts all code execution; Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembly syntax of the `PWRSAV` instruction is shown below:

Example:

```
PWRSAV #1 ; places part in Idle
PWRSAV #0 ; places part in Sleep
```

The MPLAB® XC16 C compiler offers "built-in" functions for the power-saving modes as follows:

Example:

```
Idle();  // places part in Idle
Sleep(); // places part in Sleep
```

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

10.2.1 Sleep Mode

Sleep mode has these features:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption will be reduced to a minimum provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate during Sleep mode since the system clock source is disabled.
- The LPRC clock will continue to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.

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- Some device features or peripherals may continue to operate in Sleep mode. This includes items, such as the Input Change Notification (ICN) on the I/O ports or peripherals that use an external clock input. Any peripheral that requires the system clock source for its operation will be disabled in Sleep mode.

The device will wake-up from Sleep mode on any of these events:

- On any interrupt source that is individually enabled
- On any form of device Reset
- On a WDT time-out

On wake-up from Sleep, the processor will restart with the same clock source that was active when Sleep mode was entered. The instruction execution begins starting with the instruction following the `PWRSAV` instruction or the first instruction in the ISR.

10.2.2 Idle Mode

Idle mode has these features:

- The CPU will stop executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see 10.4 Selective Peripheral Module Control).
- If the WDT or FSCM is enabled, the LPRC will also remain active.

The device will wake from Idle mode on any of these events:

- Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle, the clock is reapplied to the CPU and instruction execution begins immediately, starting with the instruction following the `PWRSAV` instruction or the first instruction in the ISR.

10.2.3 Interrupts Coincident with Power Save Instructions

Any interrupt that coincides with the execution of a `PWRSAV` instruction will be held off until entry into Sleep or Idle mode has completed. The device will then wake-up from Sleep or Idle mode.

10.2.4 Low-Voltage Regulator Mode and Band Gap Power

PIC24FJ64GP205/GU205 family devices incorporate a Low-Power and Low-Voltage Regulator mode. This Regulator mode allows the data RAM and WDT to be maintained in power-saving modes at a low-voltage level, from 0.9V to 1.2V on the V_{CAP} pin.

Low-Voltage Sleep uses less power than standard Sleep mode, but takes more time to recover and begin the code execution. An additional 10-15 µs (typical) is required to charge V_{CAP} to 1.8V and start to execute instructions when exiting Low-Voltage Sleep.

The VREGS bit (RCON[8]) allows control of the band gap circuit power. It changes the speed to exit from the Sleep modes (Regular and Low-Voltage). When the VREGS bit is cleared (= `0`), the band gap is powered in Sleep mode. It increases the current but reduces time to recover from Sleep by ~10 µs.

The Low-Voltage Regulator mode is only available when Sleep mode is invoked. It is controlled by the $\overline{\text{LPREGEN}}$ Configuration bit (FPOR[2]) and in firmware by the RETEN bit (RCON[12]). $\overline{\text{LPREGEN}}$ must be programmed (= `0`) and the RETEN bit must be set (= `1`) for the Low-Voltage Regulator mode.

10.2.5 Summary of Low-Power Sleep Modes

The low-voltage RETEN bit (RCON[12]) and the standby VREGS bit (RCON[8]) allow for four different Sleep modes, which will vary by wake-up time and power consumption. Refer to Table 10-1 for a summary of these modes. Specific information about the current consumption and wake times can be found in 30. Electrical Characteristics.

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Table 10-1. Low-Power Sleep Modes

RETEN	VREGS	MODE	Relative Power
0	0	Standby Sleep	A Few µA Range
0	1	Sleep	100 µA Range
1	0	Low-Voltage Standby Sleep	Less than 1 µA
1	1	Low-Voltage Sleep	A Few µA Range

10.3 Doze Mode

Generally, changing clock speed and invoking one of the power-saving modes are the preferred strategies for reducing power consumption. There may be circumstances, however, where this is not practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed may introduce communication errors, while using a power-saving mode may stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV[11]). The ratio between peripheral and core clock speed is determined by the DOZE[2:0] bits (CLKDIV[14:12]). There are eight possible configurations, from 1:1 to 1:256, with 1:1 being the default.

It is also possible to use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU Idles, waiting for something to invoke an interrupt routine. Enabling the automatic return to full-speed CPU operation on interrupts is enabled by setting the ROI bit (CLKDIV[15]). By default, interrupt events have no effect on Doze mode operation.

Table 10-2. Power-Saving Operating Modes

Operating Mode	Active Clocks	Active Peripherals	Wake-up Sources
Low-Voltage/Retention Sleep	Refer to the respective peripheral for active clock source	Timer, REFO, MCCP, BOR, WDT, HLVD, RTCC, CMP, CV_{REF}, CLC, UART, SPI, I^2C	• Interrupt source that is individually enabled • Any form of device Reset • WDT time-out
Sleep	Refer to the respective peripheral for active clock source	Timer, REFO, MCCP, BOR, WDT, HLVD, ADC, RTCC, CMP, CV_{REF}, CLC, UART, SPI, I^2C	• Interrupt source that is individually enabled • Any form of device Reset • WDT time-out
Idle	All clocks	All peripherals	• Interrupt source that is individually enabled • Any form of device Reset • WDT time-out

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.....continued

Operating Mode	Active Clocks	Active Peripherals	Wake-up Sources
Doze	All clocks	All peripherals	• Interrupt source that is individually enabled (ROI bit (CLKDIV[15]) should be enabled) • Any form of device Reset

10.4 Selective Peripheral Module Control

Idle and Doze modes allow users to substantially reduce power consumption by slowing or stopping the CPU clock. Even so, peripheral modules still remain clocked, and thus, consume power. There may be cases where the application needs what these modes do not provide: the allocation of power resources to CPU processing with minimal power consumption from the peripherals.

PIC24F devices address this requirement by allowing peripheral modules to be selectively disabled, reducing or eliminating their power consumption. This can be done with two control bits:

- The Peripheral Enable bit, generically named, “XXXEN”, located in the module’s main control SFR.
- The Peripheral Module Disable (PMD) bit, generically named, “XXXMD”, located in one of the PMD Control registers.

Both bits have similar functions in enabling or disabling their associated module. Setting the PMD bit for a module disables all clock sources to that module, reducing its power consumption to an absolute minimum. In this state, the control and status registers associated with the peripheral will also be disabled, so writes to those registers will have no effect and read values will be invalid. Many peripheral modules have a corresponding PMD bit.

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In contrast, disabling a module by clearing its XXXEN bit disables its functionality, but leaves its registers available to be read and written to. This reduces power consumption, but not by as much as setting the PMD bit does. Most peripheral modules have an enable bit; exceptions include input capture, output compare and RTCC.

To achieve more selective power savings, peripheral modules can also be selectively disabled when the device enters Idle mode. This is done through the control bit of the generic name format, “XXXIDL”. By default, all modules that can operate during Idle mode will do so. Using the disable on Idle feature allows further reduction of power consumption during Idle mode, enhancing power savings for extremely critical power applications.

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10.5 Peripheral Module Disable Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x0177	Reserved									
0x0178	PMD1	7:0	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD			AD1MD
		15:8			T3MD	T2MD	T1MD			
0x017A ... 0x017B	Reserved									
0x017C	PMD3	7:0	CRCMD						I2C2MD	
		15:8						CMPMD	RTCCMD	
0x017E	PMD4	7:0					REFOMD		HLVDMD	USBMD
		15:8								
0x0180	PMD5	7:0				CCP5MD	CCP4MD	CCP3MD	CCP2MD	CCP1MD
		15:8								
0x0182 ... 0x0183	Reserved									
0x0184	PMD7	7:0				DMA03MD				
		15:8								
0x0186	PMD8	7:0			CLC4MD	CLC3MD	CLC2MD	CLC1MD		
		15:8								DMTMD

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10.5.1 Peripheral Module Disable Register 1

Name: PMD1
Offset: 0x178

Bit	15	14	13	12	11	10	9	8
			T3MD	T2MD	T1MD			
Access			R/W	R/W	R/W			
Reset			0	0	0			

Bit	7	6	5	4	3	2	1	0
	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD			AD1MD
Access	R/W	R/W	R/W	R/W	R/W			R/W
Reset	0	0	0	0	0			0

Bit 13 – T3MD Timer3 Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

Bit 12 – T2MD Timer2 Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

Bit 11 – T1MD Timer1 Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

Bit 7 – I2C1MD I2C1 Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

Bit 6 – U2MD UART2 Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

Bit 5 – U1MD UART1 Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

Bit 4 – SPI2MD SPI2 Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

Bit 3 – SPI1MD SPI1 Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

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Bit 0 – AD1MD A/D Converter Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

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10.5.2 Peripheral Module Disable Register 3

Name: PMD3
Offset: 0x17C

Bit	15	14	13	12	11	10	9	8
						CMPMD	RTCCMD	
Access						R/W	R/W	
Reset						0	0	

Bit	7	6	5	4	3	2	1	0
	CRCMD						I2C2MD	
Access	R/W						R/W	
Reset	0						0	

Bit 10 – CMPMD Triple Comparator Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

Bit 9 – RTCCMD RTCC Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

Bit 7 – CRCMD CRC Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

Bit 1 – I2C2MD I2C2 Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

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10.5.3 Peripheral Module Disable Register 4

Name: PMD4
Offset: 0x17E

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					REFOMD		HLVDMD	USBMD
Access					R/W		R/W	R/W
Reset					0		0	0

Bit 3 – REFOMD Reference Clock Output Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

Bit 1 – HLVDMD High/Low-Voltage Detect Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

Bit 0 – USBMD USB Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

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10.5.4 Peripheral Module Disable Register 5

Name: PMD5
Offset: 0x180

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				CCP5MD	CCP4MD	CCP3MD	CCP2MD	CCP1MD
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – CCP5MD MCCP5 Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

Bit 3 – CCP4MD MCCP4 Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

Bit 2 – CCP3MD MCCP3 Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

Bit 1 – CCP2MD MCCP2 Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

Bit 0 – CCP1MD MCCP1 Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

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10.5.5 Peripheral Module Disable Register 7

Name: PMD7
Offset: 0x184

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				DMA03MD				
Access				R/W				
Reset				0				

Bit 4 – DMA03MD DMA Controller (Channels 0 through 1) Disable bit

Value	Description
1	Controller is disabled
0	Controller power and clock sources are enabled

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10.5.6 Peripheral Module Disable Register 8

Name: PMD8
Offset: 0x186

Bit	15	14	13	12	11	10	9	8
								DMTMD
Access								R/W
Reset								0

Bit	7	6	5	4	3	2	1	0
			CLC4MD	CLC3MD	CLC2MD	CLC1MD		
Access			R/W	R/W	R/W	R/W		
Reset			0	0	0	0		

Bit 8 – DMTMD DMT Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

Bit 5 – CLC4MD CLC4 Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

Bit 4 – CLC3MD CLC3 Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

Bit 3 – CLC2MD CLC2 Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

Bit 2 – CLC1MD CLC1 Module Disable bit

Value	Description
1	Module is disabled
0	Module power and clock sources are enabled

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11. I/O Ports

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to **"I/O Ports with Interrupt-on-Change (IOC)"** (www.microchip.com/DS70005186) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

All of the device pins (except V_{DD}, V_{SS}, $\overline{MCLR}$ and OSCI/CLKI) are shared between the peripherals and the Parallel I/O (PIO) ports. All I/O input ports feature Schmitt Trigger (ST) inputs for improved noise immunity.

11.1 Parallel I/O (PIO) Ports

A Parallel I/O port that shares a pin with a peripheral is, in general, subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents "loop through", in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 11-1 shows how ports are shared with other peripherals and the associated I/O pin to which they are connected.

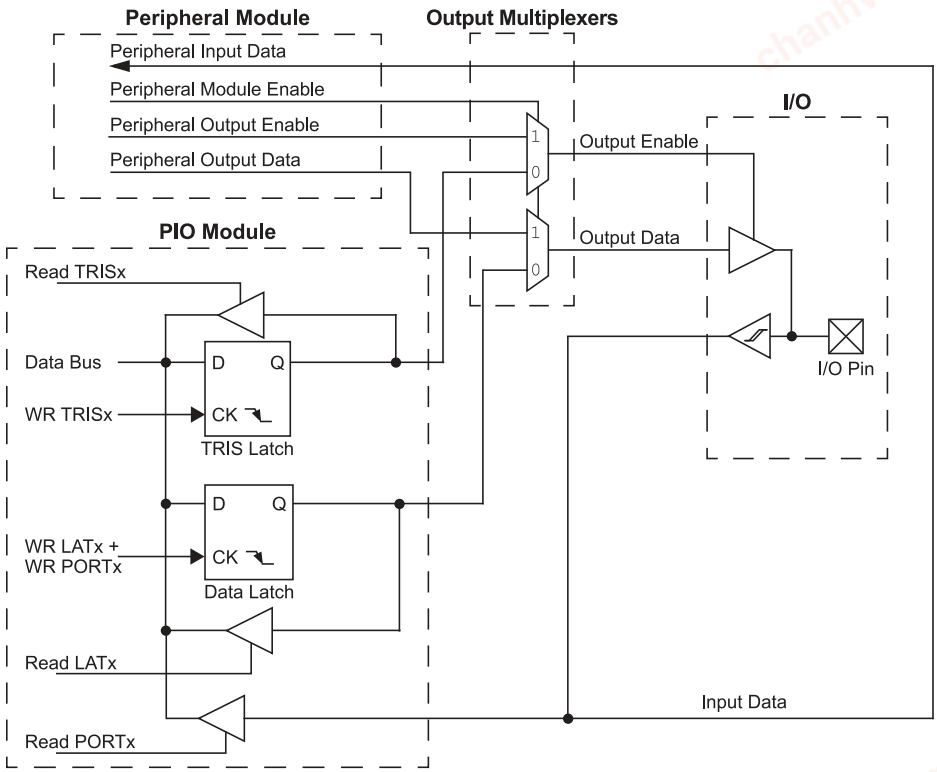
When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin may be read, but the output driver for the parallel port bit will be disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin may be driven by a port.

All port pins have three registers directly associated with their operation as digital I/Os and one register associated with their operation as analog inputs. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the Output Latch register (LATx), read the latch; writes to the latch, write the latch. Reads from the PORTx register, read the port pins; writes to the port pins, write the port pins.

Any bit and its associated data and control registers that are not valid for a particular device will be disabled. That means the corresponding LATx and TRISx registers, and the port pin, will read as zeros.

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Figure 11-1. Block Diagram of a Typical Shared Port Structure



11.1.1 I/O Port Write/Read Timing

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically, this instruction would be a `NOP`.

11.1.2 Open-Drain Configuration

In addition to the PORTx, LATx and TRISx registers for data control, each port pin can also be individually configured for either a digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than V_{DD} (e.g., 5V) on any desired digital only pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum V_{IH} specification.

Note: D+/D- pins on PIC24FJXXX**GU**XXX devices do not support open drain-configuration.

11.2 Configuring Analog Port Pins

The ANSx and TRISx registers control the operation of the pins with analog function. Each port pin with analog function is associated with one of the ANSx bits, which decide if the pin function should be analog or digital. Refer to Table 11-1 for detailed behavior of the pin for different ANSx and TRISx bit settings.

When reading the PORTx register, all pins configured as analog input channels will read as cleared (a low level).

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Table 11-1. Configuring Analog/Digital Function of an I/O Pin

Pin Function	ANSx Setting	TRISx Setting	Comments
Analog Input	1	1	
Analog Output	1	1	It is recommended to keep TRISx = 1.
Digital Input	0	1	Firmware must wait at least one instruction cycle after configuring a pin as a digital input before a valid input value can be read.
Digital Output	0	0	Make sure to disable the analog output function on the pin if any is present.

11.2.1 Analog Input Pins and Voltage Considerations

The voltage tolerance of pins used as device inputs is dependent on the pin's input function. Most input pins are able to handle DC voltages of up to 5.5V, a level typical for digital logic circuits. However, several pins can only tolerate voltages up to V_{DD}. Voltage excursions beyond V_{DD} on these pins should always be avoided.

For more information, refer to 30. Electrical Characteristics for more details.

11.3 Interrupt-on-Change (IOC)

The Interrupt-on-Change function of the I/O ports allows the PIC24FJ64GP205/GU205 family of devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature is capable of detecting input Change-of-States, even in Sleep mode, when the clocks are disabled.

Interrupt-on-Change functionality is enabled on a pin by setting the IOCPx and/or IOCNx register bit for that pin. For example, PORTC has register names, IOCPC and IOCNC, for these functions. Setting a value of '1' in the IOCPx register enables interrupts for low-to-high transitions, while setting a value of '1' in the IOCNx register enables interrupts for high-to-low transitions. Setting a value of '1' in both register bits will enable interrupts for either case (e.g., a pulse on the pin will generate two interrupts). In order for any IOC to be detected, the global IOC Interrupt Enable bit (IEC1[3]) must be set, the IOCON bit (PADCON[15]) set and the associated ISFx flag cleared.

When an interrupt request is generated for a pin, the corresponding status flag (IOCFx register bit) will be set, indicating that a Change-of-State occurred on that pin. The IOCFx register bit will remain set until cleared by writing a zero to it. When any IOCFx flag bit in a given port is set, the corresponding IOCPxF bit in the IOCSTAT register will be set. This flag indicates that a change was detected on one of the bits on the given port. The IOCPxF flag will be cleared when all IOCFx[15:0] bits are cleared.

Multiple individual status flags can be cleared by writing a zero to one or more bits using a Read-Modify-Write (RMW) operation. If another edge is detected on a pin whose status bit is being cleared during the Read-Modify-Write sequence, the associated change flag will still be set at the end of the Read-Modify-Write sequence.

The user should use the instruction sequence (or equivalent) shown in Example 11-1 to clear the Interrupt-on-Change Status registers.

At the end of this sequence, the W0 register will contain a zero for each bit for which the port pin had a change detected. In this way, any indication of a pin changing will not be lost.

Due to the asynchronous and real-time nature of the Interrupt-on-Change, the value read on the port pins may not indicate the state of the port when the change was detected, as a second change can occur during the interval between clearing the flag and reading the port. It is up to the user code to handle this case if it is a possibility in their application. To keep this interval to a minimum, it is recommended that any code modifying the IOCFx registers be run either in the interrupt handler or with interrupts disabled.

Each Interrupt-on-Change (IOC) pin has both a weak pull-up and a weak pull-down connected to it. The pull-ups act as a current source connected to the pin, while the pull-downs act as a current sink connected to the pin. These pull-ups eliminate the need for external resistors when push button or keypad devices are connected.

The pull-ups and pull-downs are separately enabled using the IOCPUx registers (for pull-ups) and the IOCPDx registers (for pull-downs). Each IOC pin has individual control bits for its pull-up and pull-down. Setting a control bit enables the weak pull-up or pull-down for the corresponding pin.

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Note: Pull-ups and pull-downs on pins should always be disabled whenever the pin is configured as a digital output.

Example 11-1. IOC Status Read/Clear In Assembly

```
MOV 0xFFFF, W0          ; Initial mask value 0xFFFF -> W0
XOR IOCFx, W0           ; W0 has '1' for each bit set in IOCFx
AND IOCFx               ; IOCFx & W0 ->IOCFx
```

Example 11-2. Port Read/Write in Assembly

```
MOV  0xFF00, W0         ; Configure PORTB[15:8] as inputs
MOV  W0, TRISB          ; and PORTB[7:0] as outputs
NOP                     ; Delay 1 cycle
BTSS PORTB, #13         ; Next Instruction
```

Example 11-3. Port Read/Write in 'C'

```
TRISB = 0xFF00;         // Configure PORTB[15:8] as inputs and PORTB[7:0] as
outputs
Nop();                  // Delay 1 cycle
If (PORTBbits.RB13){ }; // Next Instruction
```

11.4 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. In an application that needs to use more than one peripheral multiplexed on a single pin, inconvenient work arounds in application code, or a complete redesign may be the only option.

The Peripheral Pin Select (PPS) feature provides an alternative to these choices by enabling the user's peripheral set selection and its placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the microcontroller to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of any one of many digital peripherals to any one of these I/O pins. PPS is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.4.1 Available Pins

The number of available pins is dependent on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the designation, "RPn" or "RPIn", in their full pin designation, where "n" is the remappable pin number. "RP" is used to designate pins that support both remappable input and output functions, while "RPI" indicates pins that support remappable input functions only.

11.4.2 Available Peripherals and Peripheral Pin Select Function Priority

The peripherals managed by the PPS are all digital only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer related peripherals (input capture and output compare) and external interrupt inputs. Also included are the outputs of the comparator module, since these are discrete digital signals.

PPS is not available for these peripherals:

- I^2C (input and output)
- Input Change Notifications
- Analog (inputs and outputs)

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- INT0

A key difference between pin select and non-pin select peripherals is that pin select peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-pin select peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

Pin-selectable peripheral outputs (e.g., output compare, UART transmit) will take priority over general purpose digital functions on a pin, such as port I/Os. Specialized digital outputs will take priority over PPS outputs on the same pin. The pin diagrams list peripheral outputs in the order of priority. Refer to them for priority concerns on a particular pin.

Unlike PIC24F devices with fixed peripherals, pin-selectable peripheral inputs will never take ownership of a pin. The pin's output buffer will be controlled by the TRISx setting or by a fixed peripheral on the pin. If the pin is configured in Digital mode, then the PPS input will operate correctly. If an analog function is enabled on the pin, the PPS input will be disabled.

11.4.3 Controlling Peripheral Pin Select

PPS features are controlled through two sets of Special Function Registers (SFRs): one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on if an input or an output is being mapped.

11.4.3.1 Input Mapping

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral; that is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see 11.5 I/O Port and Peripheral Pin Select Registers).

Each register contains one or two sets of 6-bit fields, with each set associated with one of the pin-selectable peripherals. Programming a given peripheral's bit field with an appropriate 6-bit value maps the RPn/RPIn pin with that value to that peripheral. For any given device, the valid range of values for any of the bit fields corresponds to the maximum number of Peripheral Pin Selections supported by the device.

Table 11-2. Selectable Input Sources (Maps Input to Function)

Input Name	Function Name	Register	Function Mapping Bits
External Interrupt 1	INT1	RPINR0[13:8]	INT1R[5:0]
External Interrupt 2	INT2	RPINR1[5:0]	INT2R[5:0]
External Interrupt 3	INT3	RPINR1[13:8]	INT3R[5:0]
External Interrupt 4	INT4	RPINR2[5:0]	INT4R[5:0]
Timer2 External Clock	T2CK	RPINR3[5:0]	T2CKR[5:0]
Timer3 External Clock	T3CK	RPINR3[13:8]	T3CKR[5:0]
MCCP1 Input Capture	ICM1	RPINR5[5:0]	ICM1R[5:0]
MCCP2 Input Capture	ICM2	RPINR5[13:8]	ICM2R[5:0]
MCCP3 Input Capture	ICM3	RPINR6[5:0]	ICM3R[5:0]
MCCP4 Input Capture	ICM4	RPINR6[13:8]	ICM4R[5:0]
Output Compare Fault A	OCFA	RPINR11[5:0]	OCFAR[5:0]
Output Compare Fault B	OCFB	RPINR11[13:8]	OCFBR[5:0]
MCCP Clock Input A	TCKIA	RPINR12[5:0]	TCKIAR[5:0]
MCCP Clock Input B	TCKIB	RPINR12[13:8]	TCKIBR[5:0]
Reference Clock Input	REFI	RPINR13[5:0]	REFIR[5:0]

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Input Name	Function Name	Register	Function Mapping Bits
Tamper Detect	TMPRN	RPINR13[13:8]	TMPRNR[5:0]
MCCP5 Input Capture	ICM5	RPINR14[5:0]	ICM5R[5:0]
UART1 Receive	U1RX	RPINR18[5:0]	U1RXR[5:0]
UART1 Clear-to-Send	U1CTS	RPINR18[13:8]	U1CTSR[5:0]
UART2 Receive	U2RX	RPINR19[5:0]	U2RXR[5:0]
UART2 Clear-to-Send	U2CTS	RPINR19[13:8]	U2CTSR[5:0]
SPI1 Data	SDI1	RPINR20[5:0]	SDI1R[5:0]
SPI1 Clock	SCK1	RPINR20[13:8]	SCK1R[5:0]
SPI1 Slave Select	SS1	RPINR21[5:0]	SS1R[5:0]
SPI2 Data	SDI2	RPINR22[5:0]	SDI2R[5:0]
SPI2 Clock	SCK2	RPINR22[13:8]	SCK2R[5:0]
SPI2 Slave Select	SS2	RPINR23[5:0]	SS2R[5:0]
Generic Timer External Clock	TxCK	RPINR23[13:8]	TXCKR[5:0]
CLC Input A	CLCINA	RPINR25[5:0]	CLCINAR[5:0]
CLC Input B	CLCINB	RPINR25[13:8]	CLCINBR[5:0]
CLC Input C	CLCINC	RPINR26[5:0]	CLCINCR[5:0]
CLC Input D	CLCIND	RPINR26[13:8]	CLCINDR[5:0]

11.4.3.2 Output Mapping

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Each register contains two 6-bit fields, with each field being associated with one RPn pin (see 11.5 I/O Port and Peripheral Pin Select Registers). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 11-3).

Because of the mapping technique, the list of peripherals for output mapping also includes a null value of '000000'. This permits any given pin to remain disconnected from the output of any of the pin-selectable peripherals.

Table 11-3. Selectable Output Sources (Maps Function to Output)

Output Function Number	Function	Output Name
0	None (Pin Disabled)	—
1	C1OUT	Comparator 1 Output
2	C2OUT	Comparator 2 Output
3	U1TX	UART1 Transmit
4	U1RTS	UART1 Request-to-Send
5	U2TX	UART2 Transmit
6	U2RTS	UART2 Request-to-Send
7	SDO1	SPI1 Data
8	SCK1	SPI1 Clock

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Output Function Number	Function	Output Name
9	FSYNC1	SPI1 Synchronization
10	SDO2	SPI2 Data
11	SCK2	SPI2 Clock
12	FSYNC2	SPI2 Synchronization
13	OCM1A	MCCP1 Output A
14	OCM1B	MCCP1 Output B
15	OCM2A	MCCP2 Output A
16	OCM2B	MCCP2 Output B
17	OCM3A	MCCP3 Output A
18	OCM3B	MCCP3 Output B
19	PWRGT	RTCC Power Control
20	REFO	Reference Clock
21	CLC1OUT	CLC1 Output
22	CLC2OUT	CLC2 Output
23	CLC3OUT	CLC3 Output
24	CLC4OUT	CLC4 Output
25	RTCC	RTCC Clock
26	OCM4A	MCCP4 Output A
27	OCM4B	MCCP4 Output B
28	OCM5A	MCCP5 Output A
29	OCM5B	MCCP5 Output B
30	C3OUT	Comparator 3 Output

11.4.3.3 Mapping Limitations

The control schema of the Peripheral Pin Select is extremely flexible. Other than systematic blocks that prevent signal contention caused by two physical pins being configured as the same functional input, or two functional outputs configured as the same pin, there are no hardware enforced lockouts. The flexibility extends to the point of allowing a single input to drive multiple peripherals or a single functional output to drive multiple output pins.

MAPPING EXCEPTIONS FOR FAMILY DEVICES

The differences in available remappable pins are summarized in Table 11-3.

When developing applications that use remappable pins, users should also keep these things in mind:

- For the RPINRx registers, bit combinations corresponding to an unimplemented pin for a particular device are treated as invalid; the corresponding module will not have an input mapped to it.
- For RPORx registers, the bit fields corresponding to an unimplemented pin will also be unimplemented; writing to these fields will have no effect.

11.4.4 Controlling Configuration Changes

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC24F devices include three features to prevent alterations to the peripheral map:

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- Control register lock sequence
- Continuous state monitoring
- Configuration bit remapping lock

CONTROL REGISTER LOCK

Under normal operation, writes to the RPINRx and RPORx registers are not allowed. Attempted writes will appear to execute normally, but the contents of the registers will remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK bit (OSCCON[6]). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear IOLOCK, a specific command sequence must be executed:

- Write 46h to OSCCON[7:0].
- Write 57h to OSCCON[7:0].
- Clear (or set) IOLOCK as a single operation.

Unlike the similar sequence with the oscillator's LOCK bit, IOLOCK remains in one state until changed. This allows all of the Peripheral Pin Selects to be configured with a single unlock sequence, followed by an update to all control registers, then locked with a second lock sequence.

CONTINUOUS STATE MONITORING

In addition to being protected from direct writes, the contents of the RPINRx and RPORx registers are constantly monitored in hardware by shadow registers. If an unexpected change in any of the registers occurs (such as cell disturbances caused by ESD or other external events), a Configuration Mismatch Reset will be triggered.

CONFIGURATION BIT REMAPPING LOCK

As an additional level of safety, the device can be configured to prevent more than one write session to the RPINRx and RPORx registers. The IOL1WAY (FOSC[5]) Configuration bit blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure will not execute and the Peripheral Pin Select Control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session. Programming IOL1WAY allows users unlimited access (with the proper use of the unlock sequence) to the Peripheral Pin Select registers.

11.4.5 Considerations for Peripheral Pin Selection

The ability to control Peripheral Pin Selection introduces several considerations into application design that could be overlooked. This is particularly true for several common peripherals that are available only as remappable peripherals.

The main consideration is that the Peripheral Pin Selects are not available on default pins in the device's default (Reset) state. Since all RPINRx registers reset to '111111' and all RPORx registers reset to '000000', all Peripheral Pin Select inputs are tied to V_{SS}, and all Peripheral Pin Select outputs are disconnected.

This situation requires the user to initialize the device with the proper peripheral configuration before any other application code is executed. Since the IOLOCK bit resets in the unlocked state, it is not necessary to execute the unlock sequence after the device has come out of Reset. For application safety, however, it is best to set IOLOCK and lock the configuration after writing to the control registers.

Because the unlock sequence is timing-critical, it must be executed as an assembly language routine in the same manner as changes to the oscillator configuration. If the bulk of the application is written in 'C', or another high-level language, the unlock sequence should be performed by writing in-line assembly.

Choosing the configuration requires the review of all Peripheral Pin Selects and their pin assignments, especially those that will not be used in the application. In all cases, unused pin-selectable peripherals should be disabled completely. Unused peripherals should have their inputs assigned to an unused RPn/RPIn pin function. I/O pins with unused RPn functions should be configured with the null peripheral output.

The assignment of a peripheral to a particular pin does not automatically perform any other configuration of the pin's I/O circuitry. In theory, this means adding a pin-selectable output to a pin may mean inadvertently driving an existing peripheral input when the output is driven. Users must be familiar with the behavior of other fixed peripherals that

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share a remappable pin and know when to enable or disable them. To be safe, fixed digital peripherals that share the same pin should be disabled when not in use.

Along these lines, configuring a remappable pin for a specific peripheral does not automatically turn that feature on. The peripheral must be specifically configured for operation and enabled as if it were tied to a fixed pin. Where this happens in the application code (immediately following a device Reset and peripheral configuration or inside the main application routine) depends on the peripheral and its use in the application.

A final consideration is that Peripheral Pin Select functions neither override analog inputs nor reconfigure pins with analog functions for digital I/Os. If a pin is configured as an analog input on a device Reset, it must be explicitly reconfigured as a digital I/O when used with Peripheral Pin Select.

Example 11-4 shows a configuration for bidirectional communication with flow control using UART1. The following input and output functions are used:

- Input Functions: U1RX, $\overline{\text{U1CTS}}$
- Output Functions: U1TX, $\overline{\text{U1RTS}}$

Example 11-4. Configuring UART1 Input and Output Functions

```
//    Unlock Registers
asm volatile   ("MOV #OSCCON, w1 \n"
                "MOV #0x46, w2   \n"
                "MOV #0x57, w3   \n"
                "MOV.b w2, [w1]  \n"
                "MOV.b w3, [w1]  \n"
                "BCLR OSCCON, #6") ;
// or use XC16 built-in macro:
// __builtin_write_OSCCONL(OSCCON & 0xbf);

// Configure Input Functions (Table 11-2)
   // Assign U1RX To Pin RP0
   RPINR18bits.U1RXR = 0;

// Assign U1CTS To Pin RP1
RPINR18bits.U1CTSR = 1;

// Configure Output Functions (Table 11-3)
   // Assign U1TX To Pin RP2
   RPOR1bits.RP2R = 3;

   // Assign U1RTS To Pin RP3
   RPOR1bits.RP3R = 4;

// Lock Registers
asm volatile   ("MOV #OSCCON, w1 \n"
                "MOV #0x46, w2   \n"
                "MOV #0x57, w3   \n"
                "MOV.b w2, [w1]  \n"
                "MOV.b w3, [w1]  \n"
                "BSET OSCCON, #6") ;
// or use XC16 built-in macro:
// __builtin_write_OSCCONL(OSCCON | 0x40);
```

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11.5 I/O Port and Peripheral Pin Select Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x065B	Reserved									
0x065C	PADCON	7:0								
		15:8	IOCON							
0x065E	IOCSTAT	7:0						IOCPCF	IOCPBF	IOCPAF
		15:8								
0x0660 ... 0x0661	Reserved									
0x0662	TRISA	7:0	TRISA7			TRISA[4:0]				
		15:8		TRISA[14:8]						
0x0664	PORTA	7:0	RA7			RA[4:0]				
		15:8		RA[14:8]						
0x0666	LATA	7:0	LATA7			LATA[4:0]				
		15:8		LATA[14:8]						
0x0668	ODCA	7:0	ODCA7			ODCA[4:0]				
		15:8		ODCA[14:8]						
0x066A	ANSA	7:0				ANSA[4:0]				
		15:8								
0x066C	IOCPA	7:0	IOCPA7			IOCPA[4:0]				
		15:8		IOCPA[14:8]						
0x066E	IOCNA	7:0	IOCNA7			IOCNA[4:0]				
		15:8		IOCNA[14:8]						
0x0670	IOCFA	7:0	IOCFA7			IOCFA[4:0]				
		15:8		IOCFA[14:8]						
0x0672	IOCPUA	7:0	IOCPUA7			IOCPUA[4:0]				
		15:8		IOCPUA[14:8]						
0x0674	IOCPDA	7:0	IOCPDA7			IOCPDA[4:0]				
		15:8		IOCPDA[14:8]						
0x0676	TRISB	7:0	TRISB[7:0]							
		15:8	TRISB[15:8]							
0x0678	PORTB	7:0	RB[7:0]							
		15:8	RB[15:8]							
0x067A	LATB	7:0	LATB[7:0]							
		15:8	LATB[15:8]							
0x067C	ODCB	7:0	ODCB[7:0]							
		15:8	ODCB[15:8]							
0x067E	ANSB	7:0		ANSB6		ANSB[4:0]				
		15:8	ANSB[15:12]						ANSB9	
0x0680	IOCPB	7:0	IOCPB[7:0]							
		15:8	IOCPB[15:8]							
0x0682	IOCNB	7:0	IOCNB[7:0]							
		15:8	IOCNB[15:8]							
0x0684	IOCFB	7:0	IOCFB[7:0]							
		15:8	IOCFB[15:8]							
0x0686	IOCPUB	7:0	IOCPUB[7:0]							
		15:8	IOCPUB[15:8]							
0x0688	IOCPDB	7:0	IOCPDB[7:0]							
		15:8	IOCPDB[15:8]							
0x068A	TRISC	7:0	TRISC[7:0]							
		15:8							TRISC[9:8]	
0x068C	PORTC	7:0	RC[7:0]							
		15:8							RC[9:8]	
0x068E	LATC	7:0	LATC[7:0]							
		15:8							LATC[9:8]	

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0690	ODCC	7:0	ODCC[7:0]							
		15:8							ODCC[9:8]	
0x0692	ANSC	7:0					ANSC[3:0]			
		15:8								
0x0694	IOCPC	7:0	IOCPC[7:0]							
		15:8							IOCPC[9:8]	
0x0696	IOCNC	7:0	IOCNC[7:0]							
		15:8							IOCNC[9:8]	
0x0698	IOCFC	7:0	IOCFC[7:0]							
		15:8							IOCFC[9:8]	
0x069A	IOCPUC	7:0	IOCPUC[7:0]							
		15:8							IOCPUC[9:8]	
0x069C	IOCPDC	7:0	IOCPDC[7:0]							
		15:8							IOCPDC[9:8]	
0x069E ... 0x078F	Reserved									
0x0790	RPINR0	7:0								
		15:8			INT1R[5:0]					
0x0792	RPINR1	7:0			INT2R[5:0]					
		15:8			INT3R[5:0]					
0x0794	RPINR2	7:0			INT4R[5:0]					
		15:8								
0x0796	RPINR3	7:0			T2CKR[5:0]					
		15:8			T3CKR[5:0]					
0x0798 ... 0x0799	Reserved									
0x079A	RPINR5	7:0			ICM1R[5:0]					
		15:8			ICM2R[5:0]					
0x079C	RPINR6	7:0			ICM3R[5:0]					
		15:8			ICM4R[5:0]					
0x079E ... 0x07A5	Reserved									
0x07A6	RPINR11	7:0			OCFAR[5:0]					
		15:8			OCFBR[5:0]					
0x07A8	RPINR12	7:0			TCKIAR[5:0]					
		15:8			TCKIBR[5:0]					
0x07AA	RPINR13	7:0			REFIR[5:0]					
		15:8			TMPRNR[5:0]					
0x07AC	RPINR14	7:0			ICM5R[5:0]					
		15:8			ICM6R[5:0]					
0x07AE ... 0x07B3	Reserved									
0x07B4	RPINR18	7:0			U1RXR[5:0]					
		15:8			U1CTSR[5:0]					
0x07B6	RPINR19	7:0			U2RXR[5:0]					
		15:8			U2CTSR[5:0]					
0x07B8	RPINR20	7:0			SDI1R[5:0]					
		15:8			SCK1R[5:0]					
0x07BA	RPINR21	7:0			SS1R[5:0]					
		15:8								
0x07BC	RPINR22	7:0			SDI2R[5:0]					
		15:8			SCK2R[5:0]					
0x07BE	RPINR23	7:0			SS2R[5:0]					
		15:8			TXCKR[5:0]					

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x07C0 ... 0x07C1	Reserved									
0x07C2	RPINR25	7:0			CLCINAR[5:0]					
		15:8			CLCINBR[5:0]					
0x07C4	RPINR26	7:0			CLCINCR[5:0]					
		15:8			CLCINDR[5:0]					
0x07C6 ... 0x07D3	Reserved									
0x07D4	RPOR0	7:0		RP0R[6:0]						
		15:8		RP1R[6:0]						
0x07D6	RPOR1	7:0		RP2R[6:0]						
		15:8		RP3R[6:0]						
0x07D8	RPOR2	7:0		RP4R[6:0]						
		15:8		RP5R[6:0]						
0x07DA	RPOR3	7:0		RP6R[6:0]						
		15:8		RP7R[6:0]						
0x07DC	RPOR4	7:0		RP8R[6:0]						
		15:8		RP9R[6:0]						
0x07DE	RPOR5	7:0		RP10R[6:0]						
		15:8		RP11R[6:0]						
0x07E0	RPOR6	7:0		RP12R[6:0]						
		15:8		RP13R[6:0]						
0x07E2	RPOR7	7:0		RP14R[6:0]						
		15:8		RP15R[6:0]						
0x07E4	RPOR8	7:0		RP16R[6:0]						
		15:8		RP17R[6:0]						
0x07E6	RPOR9	7:0		RP18R[6:0]						
		15:8		RP19R[6:0]						
0x07E8	RPOR10	7:0		RP20R[6:0]						
		15:8		RP21R[6:0]						
0x07EA	RPOR11	7:0		RP22R[6:0]						
		15:8		RP23R[6:0]						
0x07EC	RPOR12	7:0		RP24R[6:0]						
		15:8		RP25R[6:0]						
0x07EE	RPOR13	7:0		RP26R[6:0]						
		15:8		RP27R[6:0]						
0x07F0	RPOR14	7:0		RP28R[6:0]						
		15:8		RP29R[6:0]						

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11.5.1 Port Configuration Register

Name: PADCON
Offset: 0x65C

Bit	15	14	13	12	11	10	9	8
	IOCON							
Access	R/W							
Reset	0							

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 15 – IOCON Interrupt-on-Change Enable bit

Value	Description
1	Interrupt-on-change functionality is enabled
0	Interrupt-on-change functionality is disabled

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11.5.2 Interrupt-on-Change Status Register

Name: IOCSTAT
Offset: 0x65E

Legend: HS = Hardware Settable bit; HC = Hardware Clearable bit

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						IOCPCF	IOCPBF	IOCPAF
Access						R/HS/HC	R/HS/HC	R/HS/HC
Reset						0	0	0

Bit 2 – IOCPCF Interrupt-on-Change PORTC Flag bit

Value	Description
1	A change was detected on an IOC-enabled pin on PORTC
0	No change was detected or the user has cleared all detected changes

Bit 1 – IOCPBF Interrupt-on-Change PORTB Flag bit

Value	Description
1	A change was detected on an IOC-enabled pin on PORTB
0	No change was detected or the user has cleared all detected changes

Bit 0 – IOCPAF Interrupt-on-Change PORTA Flag bit

Value	Description
1	A change was detected on an IOC-enabled pin on PORTA
0	No change was detected or the user has cleared all detected changes

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11.5.3 Output Enable for PORTA Register

Name: TRISA
Offset: 0x662

Bit	15	14	13	12	11	10	9	8
		TRISA[14:8]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	1	1

Bit	7	6	5	4	3	2	1	0
	TRISA7			TRISA[4:0]				
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	1			0	0	0	1	1

Bits 14:8 – TRISA[14:8] Output Enable bits

Value	Description
1	Pin is configured as input
0	Pin is configured as output

Bit 7 – TRISA7 Output Enable bit

Value	Description
1	Pin is configured as input
0	Pin is configured as output

Bits 4:0 – TRISA[4:0] Output Enable bits

Value	Description
1	Pin is configured as input
0	Pin is configured as output

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11.5.4 Input Data for PORTA Register

Name: PORTA
Offset: 0x664

Bit	15	14	13	12	11	10	9	8
		RA[14:8]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RA7			RA[4:0]				
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bits 14:8 – RA[14:8] Data Input Value bits

Bit 7 – RA7 Data Input Value bit

Bits 4:0 – RA[4:0] Data Input Value bits

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11.5.5 Output Data for PORTA Register

Name: LATA
Offset: 0x666

Bit	15	14	13	12	11	10	9	8
		LATA[14:8]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LATA7			LATA[4:0]				
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bits 14:8 – LATA[14:8] Output Data bits

Bit 7 – LATA7 Output Data bit

Bits 4:0 – LATA[4:0] Output Data bits

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11.5.6 Open-Drain Enable for PORTA Register

Name: ODCA
Offset: 0x668

Bit	15	14	13	12	11	10	9	8
		ODCA[14:8]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ODCA7			ODCA[4:0]				
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bits 14:8 – ODCA[14:8] Open-Drain Enable bits

Value	Description
1	Open-drain is enabled on the pin
0	Open-drain is disabled on the pin

Bit 7 – ODCA7 Open-Drain Enable bit

Value	Description
1	Open-drain is enabled on the pin
0	Open-drain is disabled on the pin

Bits 4:0 – ODCA[4:0] Open-Drain Enable bits

Value	Description
1	Open-drain is enabled on the pin
0	Open-drain is disabled on the pin

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11.5.7 Analog Select for PORTA Register

Name: ANSA
Offset: 0x66A

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				ANSA[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	1	1

Bits 4:0 – ANSA[4:0] Analog Input Select bits

Value	Description
1	Analog input is enabled and digital input is disabled on the pin
0	Analog input is disabled and digital input is enabled on the pin

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11.5.8 Interrupt-on-Change Positive Edge PORTA Register

Name: IOCPA
Offset: 0x66C

Bit	15	14	13	12	11	10	9	8
		IOCPA[14:8]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	IOCPA7			IOCPA[4:0]				
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bits 14:8 – IOCPA[14:8] Interrupt-on-Change Positive Edge Enable bits

Value	Description
1	Interrupt-on-change is enabled on the pin for a positive going edge; the associated status bit and interrupt flag will be set upon detecting an edge
0	Interrupt-on-change is disabled on the pin for a positive going edge

Bit 7 – IOCPA7 Interrupt-on-Change Positive Edge Enable bit

Value	Description
1	Interrupt-on-change is enabled on the pin for a positive going edge; the associated status bit and interrupt flag will be set upon detecting an edge
0	Interrupt-on-change is disabled on the pin for a positive going edge

Bits 4:0 – IOCPA[4:0] Interrupt-on-Change Positive Edge Enable bits

Value	Description
1	Interrupt-on-change is enabled on the pin for a positive going edge; the associated status bit and interrupt flag will be set upon detecting an edge
0	Interrupt-on-change is disabled on the pin for a positive going edge

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11.5.9 Interrupt-on-Change Negative Edge PORTA Register

Name: IOCNA
Offset: 0x66E

Bit	15	14	13	12	11	10	9	8
		IOCNA[14:8]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	IOCNA7			IOCNA[4:0]				
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bits 14:8 – IOCNA[14:8] Interrupt-on-Change Negative Edge Enable bits

Value	Description
1	Interrupt-on-change is enabled on the pin for a negative going edge; the associated status bit and interrupt flag will be set upon detecting an edge
0	Interrupt-on-change is disabled on the pin for a negative going edge

Bit 7 – IOCNA7 Interrupt-on-Change Negative Edge Enable bit

Value	Description
1	Interrupt-on-change is enabled on the pin for a negative going edge; the associated status bit and interrupt flag will be set upon detecting an edge
0	Interrupt-on-change is disabled on the pin for a negative going edge

Bits 4:0 – IOCNA[4:0] Interrupt-on-Change Negative Edge Enable bits

Value	Description
1	Interrupt-on-change is enabled on the pin for a negative going edge; the associated status bit and interrupt flag will be set upon detecting an edge
0	Interrupt-on-change is disabled on the pin for a negative going edge

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11.5.10 Interrupt-on-Change Flag PORTA Register

Name: IOCFA
Offset: 0x670

Bit	15	14	13	12	11	10	9	8
		IOCFA[14:8]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	IOCFA7			IOCFA[4:0]				
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bits 14:8 – IOCFA[14:8] Interrupt-on-Change Flag bits

Value	Description
1	An enabled change was detected on the associated pin
0	No change was detected or the user cleared the detected change

Bit 7 – IOCFA7 Interrupt-on-Change Flag bit

Value	Description
1	An enabled change was detected on the associated pin
0	No change was detected or the user cleared the detected change

Bits 4:0 – IOCFA[4:0] Interrupt-on-Change Flag bits

Value	Description
1	An enabled change was detected on the associated pin
0	No change was detected or the user cleared the detected change

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11.5.11 Interrupt-on-Change Pull-up Enable PORTA Register

Name: IOCPUA
Offset: 0x672

Bit	15	14	13	12	11	10	9	8
		IOCPUA[14:8]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	IOCPUA7			IOCPUA[4:0]				
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bits 14:8 – IOCPUA[14:8] Interrupt-on-Change Pull-up Enable bits

Value	Description
1	Pull-up is enabled
0	Pull-up is disabled

Bit 7 – IOCPUA7 Interrupt-on-Change Pull-up Enable bit

Value	Description
1	Pull-up is enabled
0	Pull-up is disabled

Bits 4:0 – IOCPUA[4:0] Interrupt-on-Change Pull-up Enable bits

Value	Description
1	Pull-up is enabled
0	Pull-up is disabled

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11.5.12 Interrupt-on-Change Pull-Down Enable PORTA Register

Name: IOCPDA
Offset: 0x674

Bit	15	14	13	12	11	10	9	8
		IOCPDA[14:8]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	IOCPDA7			IOCPDA[4:0]				
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bits 14:8 – IOCPDA[14:8] Interrupt-on-Change Pull-Down Enable bits

Value	Description
1	Pull-down is enabled
0	Pull-down is disabled

Bit 7 – IOCPDA7 Interrupt-on-Change Pull-Down Enable bit

Value	Description
1	Pull-down is enabled
0	Pull-down is disabled

Bits 4:0 – IOCPDA[4:0] Interrupt-on-Change Pull-Down Enable bits

Value	Description
1	Pull-down is enabled
0	Pull-down is disabled

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11.5.13 Output Enable for PORTB Register

Name: TRISB
Offset: 0x676

Bit	15	14	13	12	11	10	9	8
	TRISB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	TRISB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 15:0 – TRISB[15:0] Output Enable bits

Value	Description
1	Pin is configured as input
0	Pin is configured as output

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11.5.14 Input Data for PORTB Register

Name: PORTB
Offset: 0x678

Bit	15	14	13	12	11	10	9	8
	RB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – RB[15:0] Data Input Value bits

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11.5.15 Output Data for PORTB Register

Name: LATB
Offset: 0x67A

Bit	15	14	13	12	11	10	9	8
	LATB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LATB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – LATB[15:0] Output Data bits

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11.5.16 Open-Drain Enable for PORTB Register

Name: ODCB
Offset: 0x67C

Bit	15	14	13	12	11	10	9	8
	ODCB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ODCB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ODCB[15:0] Open-Drain Enable bits

Value	Description
1	Open-drain is enabled on the pin
0	Open-drain is disabled on the pin

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11.5.17 Analog Select for PORTB Register

Name: ANSB
Offset: 0x67E

Bit	15	14	13	12	11	10	9	8
	ANSB[15:12]						ANSB9	
Access	R/W	R/W	R/W	R/W			R/W	
Reset	1	1	1	1			1	

Bit	7	6	5	4	3	2	1	0
		ANSB6		ANSB[4:0]				
Access		R/W		R/W	R/W	R/W	R/W	R/W
Reset		1		1	1	1	1	1

Bits 15:12 – ANSB[15:12] Analog Input Select bits

Value	Description
1	Analog input is enabled and digital input is disabled on the pin
0	Analog input is disabled and digital input is enabled on the pin

Bit 9 – ANSB9 Analog Input Select bit

Value	Description
1	Analog input is enabled and digital input is disabled on the pin
0	Analog input is disabled and digital input is enabled on the pin

Bit 6 – ANSB6 Analog Input Select bit

Value	Description
1	Analog input is enabled and digital input is disabled on the pin
0	Analog input is disabled and digital input is enabled on the pin

Bits 4:0 – ANSB[4:0] Analog Input Select bits

Value	Description
1	Analog input is enabled and digital input is disabled on the pin
0	Analog input is disabled and digital input is enabled on the pin

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11.5.18 Interrupt-on-Change Positive Edge PORTB Register

Name: IOCPB
Offset: 0x680

Bit	15	14	13	12	11	10	9	8
	IOCPB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	IOCPB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – IOCPB[15:0] Interrupt-on-Change Positive Edge Enable bits

Value	Description
1	Interrupt-on-change is enabled on the pin for a positive going edge; the associated status bit and interrupt flag will be set upon detecting an edge
0	Interrupt-on-change is disabled on the pin for a positive going edge

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11.5.19 Interrupt-on-Change Negative Edge PORTB Register

Name: IOCNB
Offset: 0x682

Bit	15	14	13	12	11	10	9	8
	IOCNB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	IOCNB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – IOCNB[15:0] Interrupt-on-Change Negative Edge Enable bits

Value	Description
1	Interrupt-on-change is enabled on the pin for a negative going edge; the associated status bit and interrupt flag will be set upon detecting an edge
0	Interrupt-on-change is disabled on the pin for a negative going edge

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11.5.20 Interrupt-on-Change Flag PORTB Register

Name: IOCFB
Offset: 0x684

Bit	15	14	13	12	11	10	9	8
	IOCFB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	IOCFB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – IOCFB[15:0] Interrupt-on-Change Flag bits

Value	Description
1	An enabled change was detected on the associated pin
0	No change was detected or the user cleared the detected change

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11.5.21 Interrupt-on-Change Pull-up Enable PORTB Register

Name: IOCPUB
Offset: 0x686

Bit	15	14	13	12	11	10	9	8
	IOCPUB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	IOCPUB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – IOCPUB[15:0] Interrupt-on-Change Pull-up Enable bits

Value	Description
1	Pull-up is enabled
0	Pull-up is disabled

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11.5.22 Interrupt-on-Change Pull-Down Enable PORTB Register

Name: IOCPDB
Offset: 0x688

Bit	15	14	13	12	11	10	9	8
	IOCPDB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	IOCPDB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – IOCPDB[15:0] Interrupt-on-Change Pull-Down Enable bits

Value	Description
1	Pull-down is enabled
0	Pull-down is disabled

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11.5.23 Output Enable for PORTC Register

Name: TRISC
Offset: 0x68A

Bit	15	14	13	12	11	10	9	8
							TRISC[9:8]	
Access							R/W	R/W
Reset							1	1

Bit	7	6	5	4	3	2	1	0
	TRISC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	1	1	1

Bits 9:8 – TRISC[9:8] Output Enable bits

Value	Description
1	Pin is configured as input
0	Pin is configured as output

Bits 7:0 – TRISC[7:0] Output Enable bits

Value	Description
1	Pin is configured as input
0	Pin is configured as output

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11.5.24 Input Data for PORTC Register

Name: PORTC
Offset: 0x68C

Bit	15	14	13	12	11	10	9	8
							RC[9:8]	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	RC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 9:8 – RC[9:8] Data Input Value bits

Bits 7:0 – RC[7:0] Data Input Value bits

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11.5.25 Output Data for PORTC Register

Name: LATC
Offset: 0x68E

Bit	15	14	13	12	11	10	9	8
							LATC[9:8]	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	LATC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 9:8 – LATC[9:8] Output Data bits

Bits 7:0 – LATC[7:0] Output Data bits

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11.5.26 Open-Drain Enable for PORTC Register

Name: ODCC
Offset: 0x690

Bit	15	14	13	12	11	10	9	8
							ODCC[9:8]	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	ODCC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 9:8 – ODCC[9:8] Open-Drain Enable bits

Value	Description
1	Open-drain is enabled on the pin
0	Open-drain is disabled on the pin

Bits 7:0 – ODCC[7:0] Open-Drain Enable bits

Value	Description
1	Open-drain is enabled on the pin
0	Open-drain is disabled on the pin

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11.5.27 Analog Select for PORTC Register

Name: ANSC
Offset: 0x692

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					ANSC[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	1

Bits 3:0 – ANSC[3:0] Analog Input Select bit

Value	Description
1	Analog input is enabled and digital input is disabled on the pin
0	Analog input is disabled and digital input is enabled on the pin

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11.5.28 Interrupt-on-Change Positive Edge PORTC Register

Name: IOCPC
Offset: 0x694

Bit	15	14	13	12	11	10	9	8
							IOCPC[9:8]	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	IOCPC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 9:8 – IOCPC[9:8] Interrupt-on-Change Positive Edge Enable bits

Value	Description
1	Interrupt-on-change is enabled on the pin for a positive going edge; the associated status bit and interrupt flag will be set upon detecting an edge
0	Interrupt-on-change is disabled on the pin for a positive going edge

Bits 7:0 – IOCPC[7:0] Interrupt-on-Change Positive Edge Enable bits

Value	Description
1	Interrupt-on-change is enabled on the pin for a positive going edge; the associated status bit and interrupt flag will be set upon detecting an edge
0	Interrupt-on-change is disabled on the pin for a positive going edge

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11.5.29 Interrupt-on-Change Negative Edge PORTC Register

Name: IOCNC
Offset: 0x696

Bit	15	14	13	12	11	10	9	8
							IOCNC[9:8]	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	IOCNC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 9:8 – IOCNC[9:8] Interrupt-on-Change Negative Edge Enable bits

Value	Description
1	Interrupt-on-change is enabled on the pin for a negative going edge; the associated status bit and interrupt flag will be set upon detecting an edge
0	Interrupt-on-change is disabled on the pin for a negative going edge

Bits 7:0 – IOCNC[7:0] Interrupt-on-Change Negative Edge Enable bits

Value	Description
1	Interrupt-on-change is enabled on the pin for a negative going edge; the associated status bit and interrupt flag will be set upon detecting an edge
0	Interrupt-on-change is disabled on the pin for a negative going edge

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11.5.30 Interrupt-on-Change Flag PORTC Register

Name: IOCFC
Offset: 0x698

Bit	15	14	13	12	11	10	9	8
							IOCFC[9:8]	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	IOCFC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 9:8 – IOCFC[9:8] Interrupt-on-Change Flag bits

Value	Description
1	An enabled change was detected on the associated pin
0	No change was detected or the user cleared the detected change

Bits 7:0 – IOCFC[7:0] Interrupt-on-Change Flag bits

Value	Description
1	An enabled change was detected on the associated pin
0	No change was detected or the user cleared the detected change

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11.5.31 Interrupt-on-Change Pull-up Enable PORTC Register

Name: IOCPUC
Offset: 0x69A

Bit	15	14	13	12	11	10	9	8
							IOCPUC[9:8]	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	IOCPUC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 9:8 – IOCPUC[9:8] Interrupt-on-Change Pull-up Enable bits

Value	Description
1	Pull-up is enabled
0	Pull-up is disabled

Bits 7:0 – IOCPUC[7:0] Interrupt-on-Change Pull-up Enable bits

Value	Description
1	Pull-up is enabled
0	Pull-up is disabled

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11.5.32 Interrupt-on-Change Pull-Down Enable PORTC Register

Name: IOCPDC
Offset: 0x69C

Bit	15	14	13	12	11	10	9	8
							IOCPDC[9:8]	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	IOCPDC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 9:8 – IOCPDC[9:8] Interrupt-on-Change Pull-Down Enable bits

Value	Description
1	Pull-down is enabled
0	Pull-down is disabled

Bits 7:0 – IOCPDC[7:0] Interrupt-on-Change Pull-Down Enable bits

Value	Description
1	Pull-down is enabled
0	Pull-down is disabled

11.5.33 Peripheral Pin Select Registers

Note: Input and Output register values can only be changed if IOLOCK (OSCCON[6]) = 0. See 11.4.4 Controlling Configuration Changes for a specific command sequence.

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11.5.34 Peripheral Pin Select Input Register 0

Name: RPINR0
Offset: 0x790

Bit	15	14	13	12	11	10	9	8
			INT1R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 13:8 – INT1R[5:0] Refer to Table 11-2 for bit field definitions

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11.5.35 Peripheral Pin Select Input Register 1

Name: RPINR1
Offset: 0x792

Bit	15	14	13	12	11	10	9	8
			INT3R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			INT2R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – INT3R[5:0] Refer to Table 11-2 for bit field definitions

Bits 5:0 – INT2R[5:0] Refer to Table 11-2 for bit field definitions

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11.5.36 Peripheral Pin Select Input Register 2

Name: RPINR2
Offset: 0x794

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			INT4R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 5:0 – INT4R[5:0] Refer to Table 11-2 for bit field definitions

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11.5.37 Peripheral Pin Select Input Register 3

Name: RPINR3
Offset: 0x796

Bit	15	14	13	12	11	10	9	8
			T3CKR[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			T2CKR[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – T3CKR[5:0] Refer to Table 11-2 for bit field definitions

Bits 5:0 – T2CKR[5:0] Refer to Table 11-2 for bit field definitions

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11.5.38 Peripheral Pin Select Input Register 5

Name: RPINR5
Offset: 0x79A

Bit	15	14	13	12	11	10	9	8
			ICM2R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			ICM1R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – ICM2R[5:0] Refer to Table 11-2 for bit field definitions

Bits 5:0 – ICM1R[5:0] Refer to Table 11-2 for bit field definitions

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11.5.39 Peripheral Pin Select Input Register 6

Name: RPINR6
Offset: 0x79C

Bit	15	14	13	12	11	10	9	8
			ICM4R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			ICM3R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – ICM4R[5:0] Refer to Table 11-2 for bit field definitions

Bits 5:0 – ICM3R[5:0] Refer to Table 11-2 for bit field definitions

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11.5.40 Peripheral Pin Select Input Register 11

Name: RPINR11
Offset: 0x7A6

Bit	15	14	13	12	11	10	9	8
			OCFBR[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			OCFAR[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – OCFBR[5:0] Refer to Table 11-2 for bit field definitions

Bits 5:0 – OCFAR[5:0] Refer to Table 11-2 for bit field definitions

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11.5.41 Peripheral Pin Select Input Register 12

Name: RPINR12
Offset: 0x7A8

Bit	15	14	13	12	11	10	9	8
			TCKIBR[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			TCKIAR[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – TCKIBR[5:0] Refer to Table 11-2 for bit field definitions

Bits 5:0 – TCKIAR[5:0] Refer to Table 11-2 for bit field definitions

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11.5.42 Peripheral Pin Select Input Register 13

Name: RPINR13
Offset: 0x7AA

Bit	15	14	13	12	11	10	9	8
			TMPRNR[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			REFIR[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – TMPRNR[5:0] Refer to Table 11-2 for bit field definitions

Bits 5:0 – REFIR[5:0] Refer to Table 11-2 for bit field definitions

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11.5.43 Peripheral Pin Select Input Register 14

Name: RPINR14
Offset: 0x7AC

Bit	15	14	13	12	11	10	9	8
			ICM6R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			ICM5R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – ICM6R[5:0] Refer to Table 11-2 for bit field definitions

Bits 5:0 – ICM5R[5:0] Refer to Table 11-2 for bit field definitions

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11.5.44 Peripheral Pin Select Input Register 18

Name: RPINR18
Offset: 0x7B4

Bit	15	14	13	12	11	10	9	8
			U1CTSR[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			U1RXR[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – U1CTSR[5:0] Refer to Table 11-2 for bit field definitions

Bits 5:0 – U1RXR[5:0] Refer to Table 11-2 for bit field definitions

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11.5.45 Peripheral Pin Select Input Register 19

Name: RPINR19
Offset: 0x7B6

Bit	15	14	13	12	11	10	9	8
			U2CTSR[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			U2RXR[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – U2CTSR[5:0] Refer to Table 11-2 for bit field definitions

Bits 5:0 – U2RXR[5:0] Refer to Table 11-2 for bit field definitions

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11.5.46 Peripheral Pin Select Input Register 20

Name: RPINR20
Offset: 0x7B8

Bit	15	14	13	12	11	10	9	8
			SCK1R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			SDI1R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – SCK1R[5:0] Refer to Table 11-2 for bit field definitions

Bits 5:0 – SDI1R[5:0] Refer to Table 11-2 for bit field definitions

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11.5.47 Peripheral Pin Select Input Register 21

Name: RPINR21
Offset: 0x7BA

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			SS1R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 5:0 – SS1R[5:0] Refer to Table 11-2 for bit field definitions

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11.5.48 Peripheral Pin Select Input Register 22

Name: RPINR22
Offset: 0x7BC

Bit	15	14	13	12	11	10	9	8
			SCK2R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			SDI2R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – SCK2R[5:0] Refer to Table 11-2 for bit field definitions

Bits 5:0 – SDI2R[5:0] Refer to Table 11-2 for bit field definitions

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11.5.49 Peripheral Pin Select Input Register 23

Name: RPINR23
Offset: 0x7BE

Bit	15	14	13	12	11	10	9	8
			TXCKR[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			SS2R[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – TXCKR[5:0] Refer to Table 11-2 for bit field definitions

Bits 5:0 – SS2R[5:0] Refer to Table 11-2 for bit field definitions

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11.5.50 Peripheral Pin Select Input Register 25

Name: RPINR25
Offset: 0x7C2

Bit	15	14	13	12	11	10	9	8
			CLCINBR[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			CLCINAR[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – CLCINBR[5:0] Refer to Table 11-2 for bit field definitions

Bits 5:0 – CLCINAR[5:0] Refer to Table 11-2 for bit field definitions

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11.5.51 Peripheral Pin Select Input Register 26

Name: RPINR26
Offset: 0x7C4

Bit	15	14	13	12	11	10	9	8
			CLCINDR[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			CLCINCR[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 13:8 – CLCINDR[5:0] Refer to Table 11-2 for bit field definitions

Bits 5:0 – CLCINCR[5:0] Refer to Table 11-2 for bit field definitions

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11.5.52 Peripheral Pin Select Output Register 0

Name: RPOR0
Offset: 0x7D4

Bit	15	14	13	12	11	10	9	8
		RP1R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		RP0R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 14:8 – RP1R[6:0] Refer to Table 11-3 for bit field definitions

Bits 6:0 – RP0R[6:0] Refer to Table 11-3 for bit field definitions

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11.5.53 Peripheral Pin Select Output Register 1

Name: RPOR1
Offset: 0x7D6

Bit	15	14	13	12	11	10	9	8
		RP3R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		RP2R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 14:8 – RP3R[6:0] Refer to Table 11-3 for bit field definitions

Bits 6:0 – RP2R[6:0] Refer to Table 11-3 for bit field definitions

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11.5.54 Peripheral Pin Select Output Register 2

Name: RPOR2
Offset: 0x7D8

Bit	15	14	13	12	11	10	9	8
		RP5R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		RP4R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 14:8 – RP5R[6:0] Refer to Table 11-3 for bit field definitions

Bits 6:0 – RP4R[6:0] Refer to Table 11-3 for bit field definitions

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11.5.55 Peripheral Pin Select Output Register 3

Name: RPOR3
Offset: 0x7DA

Bit	15	14	13	12	11	10	9	8
		RP7R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		RP6R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 14:8 – RP7R[6:0] Refer to Table 11-3 for bit field definitions

Bits 6:0 – RP6R[6:0] Refer to Table 11-3 for bit field definitions

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11.5.56 Peripheral Pin Select Output Register 4

Name: RPOR4
Offset: 0x7DC

Bit	15	14	13	12	11	10	9	8
		RP9R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		RP8R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 14:8 – RP9R[6:0] Refer to Table 11-3 for bit field definitions

Bits 6:0 – RP8R[6:0] Refer to Table 11-3 for bit field definitions

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11.5.57 Peripheral Pin Select Output Register 5

Name: RPOR5
Offset: 0x7DE

Bit	15	14	13	12	11	10	9	8
		RP11R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		RP10R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 14:8 – RP11R[6:0] Refer to Table 11-3 for bit field definitions

Bits 6:0 – RP10R[6:0] Refer to Table 11-3 for bit field definitions

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11.5.58 Peripheral Pin Select Output Register 6

Name: RPOR6
Offset: 0x7E0

Bit	15	14	13	12	11	10	9	8
		RP13R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		RP12R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 14:8 – RP13R[6:0] Refer to Table 11-3 for bit field definitions

Bits 6:0 – RP12R[6:0] Refer to Table 11-3 for bit field definitions

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11.5.59 Peripheral Pin Select Output Register 7

Name: RPOR7
Offset: 0x7E2

Bit	15	14	13	12	11	10	9	8
		RP15R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		RP14R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 14:8 – RP15R[6:0] Refer to Table 11-3 for bit field definitions

Bits 6:0 – RP14R[6:0] Refer to Table 11-3 for bit field definitions

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11.5.60 Peripheral Pin Select Output Register 8

Name: RPOR8
Offset: 0x7E4

Bit	15	14	13	12	11	10	9	8
		RP17R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		RP16R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 14:8 – RP17R[6:0] Refer to Table 11-3 for bit field definitions

Bits 6:0 – RP16R[6:0] Refer to Table 11-3 for bit field definitions

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11.5.61 Peripheral Pin Select Output Register 9

Name: RPOR9
Offset: 0x7E6

Bit	15	14	13	12	11	10	9	8
		RP19R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		RP18R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 14:8 – RP19R[6:0] Refer to Table 11-3 for bit field definitions

Bits 6:0 – RP18R[6:0] Refer to Table 11-3 for bit field definitions

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11.5.62 Peripheral Pin Select Output Register 10

Name: RPOR10
Offset: 0x7E8

Bit	15	14	13	12	11	10	9	8
		RP21R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		RP20R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 14:8 – RP21R[6:0] Refer to Table 11-3 for bit field definitions

Bits 6:0 – RP20R[6:0] Refer to Table 11-3 for bit field definitions

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11.5.63 Peripheral Pin Select Output Register 11

Name: RPOR11
Offset: 0x7EA

Bit	15	14	13	12	11	10	9	8
		RP23R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		RP22R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 14:8 – RP23R[6:0] Refer to Table 11-3 for bit field definitions

Bits 6:0 – RP22R[6:0] Refer to Table 11-3 for bit field definitions

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11.5.64 Peripheral Pin Select Output Register 12

Name: RPOR12
Offset: 0x7EC

Bit	15	14	13	12	11	10	9	8
		RP25R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		RP24R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 14:8 – RP25R[6:0] Refer to Table 11-3 for bit field definitions

Bits 6:0 – RP24R[6:0] Refer to Table 11-3 for bit field definitions

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11.5.65 Peripheral Pin Select Output Register 13

Name: RPOR13
Offset: 0x7EE

Bit	15	14	13	12	11	10	9	8
		RP27R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		RP26R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 14:8 – RP27R[6:0] Refer to Table 11-3 for bit field definitions

Bits 6:0 – RP26R[6:0] Refer to Table 11-3 for bit field definitions

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11.5.66 Peripheral Pin Select Output Register 14

Name: RPOR14
Offset: 0x7F0

Bit	15	14	13	12	11	10	9	8
		RP29R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		RP28R[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 14:8 – RP29R[6:0] Refer to Table 11-3 for bit field definitions

Bits 6:0 – RP28R[6:0] Refer to Table 11-3 for bit field definitions

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12. Timer1

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to **"Timers"** (www.microchip.com/DS39704) in the *"dsPIC33/PIC24 Family Reference Manual"*). The information in this data sheet supersedes the information in the FRM.

Timer1 can operate in three modes:

- 16-Bit Timer
- 16-Bit Synchronous Counter
- 16-Bit Asynchronous Counter

Timer1 also supports these features:

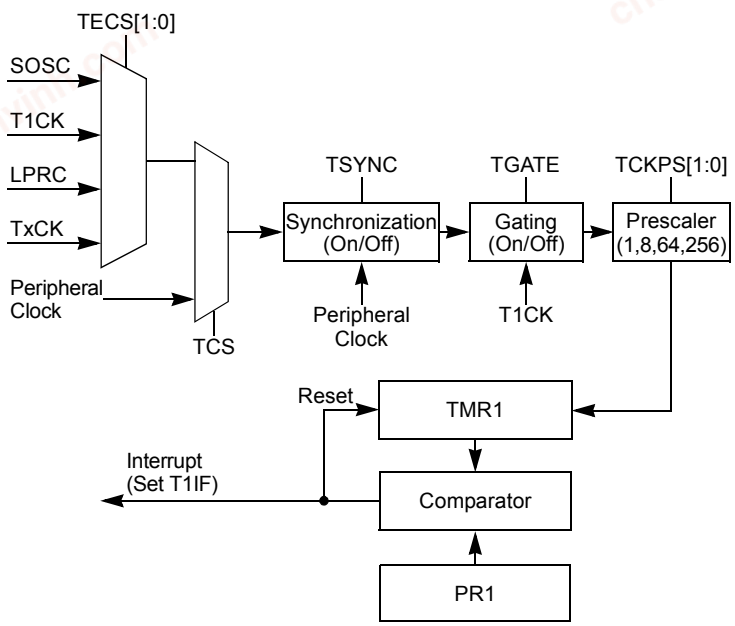
- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during CPU Idle and Sleep modes
- Interrupt on 16-Bit Period Register Match or Falling Edge of External Gate Signal

Figure 12-1 shows a block diagram of the 16-bit timer module.

To configure Timer1 for operation:

1. Select the timer prescaler ratio using the TCKPS[1:0] bits.
2. Set the Clock and Gating modes using the TCS, TECS[1:0] and TGATE bits.
3. Set or clear the TSYNC bit to configure synchronous or asynchronous operation.
4. Load the timer period value into the PR1 register.
5. If interrupts are required, set the Timer1 Interrupt Enable bit, T1IE. Use the Timer1 Interrupt Priority bits, T1IP[2:0], to set the interrupt priority.
6. Set the TON bit (= 1).

Figure 12-1. 16-Bit Timer1 Module Block Diagram



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12.1 Timer1 Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x018F	Reserved									
0x0190	TMR1	7:0	TMR1[7:0]							
		15:8	TMR1[15:8]							
0x0192	PR1	7:0	PR1[7:0]							
		15:8	PR1[15:8]							
0x0194	T1CON	7:0		TGATE	TCKPS[1:0]			TSYNC	TCS	
		15:8	TON		TSIDL				TECS[1:0]	

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12.1.1 Timer1 Counter Register

Name: TMR1
Offset: 0x190

Bit	15	14	13	12	11	10	9	8
	TMR1[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TMR1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TMR1[15:0] Timer1 Value bits

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12.1.2 Timer1 Period Register

Name: PR1
Offset: 0x192

Bit	15	14	13	12	11	10	9	8
	PR1[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PR1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PR1[15:0] Timer1 Period Value bits

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12.1.3 Timer1 Control Register

Name: T1CON
Offset: 0x194

Note:

1. Changing the value of T1CON while the timer is running (TON = 1) causes the timer prescale counter to reset and is not recommended.

Bit	15	14	13	12	11	10	9	8
	TON		TSIDL				TECS[1:0]	
Access	R/W		R/W				R/W	R/W
Reset	0		0				0	0

Bit	7	6	5	4	3	2	1	0
		TGATE	TCKPS[1:0]			TSYNC	TCS	
Access		R/W	R/W	R/W		R/W	R/W	
Reset		0	0	0		0	0	

Bit 15 – TON Timer1 On bit(1)

Value	Description
1	Starts 16-bit Timer1
0	Stops 16-bit Timer1

Bit 13 – TSIDL Timer1 Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode
0	Continues module operation in Idle mode

Bits 9:8 – TECS[1:0] Timer1 Extended Clock Select bits (selected when TCS = 1)

Value	Description
11	Generic timer (TxCK) external input
10	LPRC Oscillator
01	T1CK external clock input
00	SOSC

Bit 6 – TGATE Timer1 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:

Value	Description
1	Gated time accumulation is enabled
0	Gated time accumulation is disabled

Bits 5:4 – TCKPS[1:0] Timer1 Input Clock Prescale Select bits

Value	Description
11	1:256
10	1:64
01	1:8
00	1:1

Bit 2 – TSYNC Timer1 External Clock Input Synchronization Select bit
When TCS = 0:
This bit is ignored.
When TCS = 1:

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Value	Description
1	Synchronizes the external clock input
0	Does not synchronize the external clock input

Bit 1 – TCS Timer1 Clock Source Select bit

Value	Description
1	External clock source selected by TECS[1:0]
0	Internal peripheral clock (F_{OSC})

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13. Timer2/3

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to **"Timers"** (www.microchip.com/DS39704) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

The Timer2/3 modules are 32-bit timers, which can also be configured as independent, 16-bit timers with selectable operating modes.

As a 32-bit timer, Timer2/3 can operate in four modes:

- Two Independent 16-Bit Synchronous Timers
- Two Independent 16-Bit Synchronous Counters
- Single 32-Bit Synchronous Timer
- Single 32-Bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle mode
- Interrupt on a 32-Bit Period Register Match
- A/D Event Trigger

Individually, all of the timers can function as synchronous timers or counters. These timers cannot operate in Sleep mode. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON and T3CON registers.

For 32-bit timer/counter operation, Timer2 is the least significant word; Timer3 is the most significant word of the 32-bit timer.

Note: For 32-bit operation, T3CON control bits are ignored. Only T2CON control bits are used for setup and control. Timer2 clocks and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 interrupt flags.

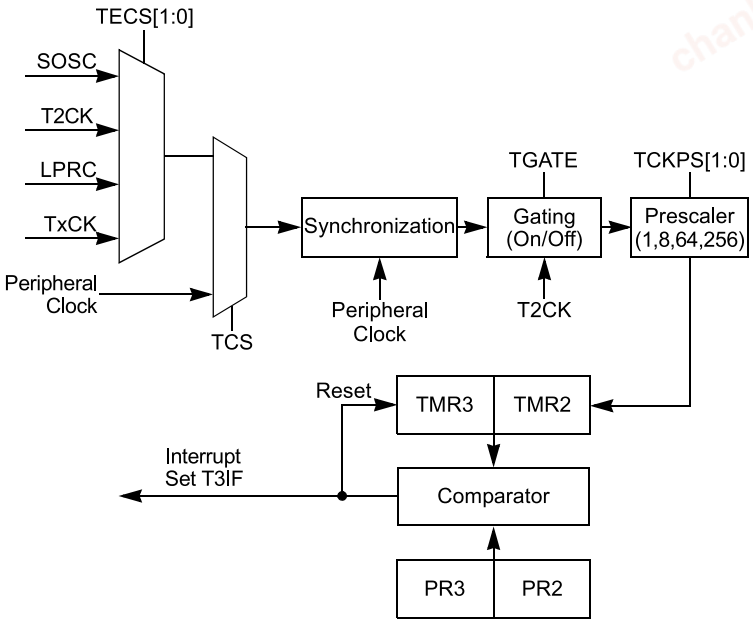
To configure Timer2/3 for 32-bit operation:

1. Set the T32 bit (T2CON[3] = `1`).
2. Select the prescaler ratio for Timer2 using the TCKPS[1:0] bits.
3. Set the Clock and Gating modes using the TCS and TGATE bits. If TCS is set to an external clock, RPINRx (TyCK) must be configured to an available RPn/RPIn pin. For more information, see 11.4 Peripheral Pin Select (PPS).
4. Load the timer period value. PR3 will contain the most significant word (msw) of the value, while PR2 contains the least significant word (lsw).
5. If interrupts are required, set the interrupt enable bit, T3IE. Use the priority bits, T3IP[2:0], to set the interrupt priority. Note that while Timer2 controls the timer, the interrupt appears as a Timer3 interrupt.
6. Set the TON bit (= `1`).

The timer value, at any point, is stored in the register pair, TMR3/2. TMR3 always contains the most significant word of the count, while TMR2 contains the least significant word. The 32-bit timer is shown in Figure 13-1.

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Figure 13-1. 32-Bit Timer Block Diagram



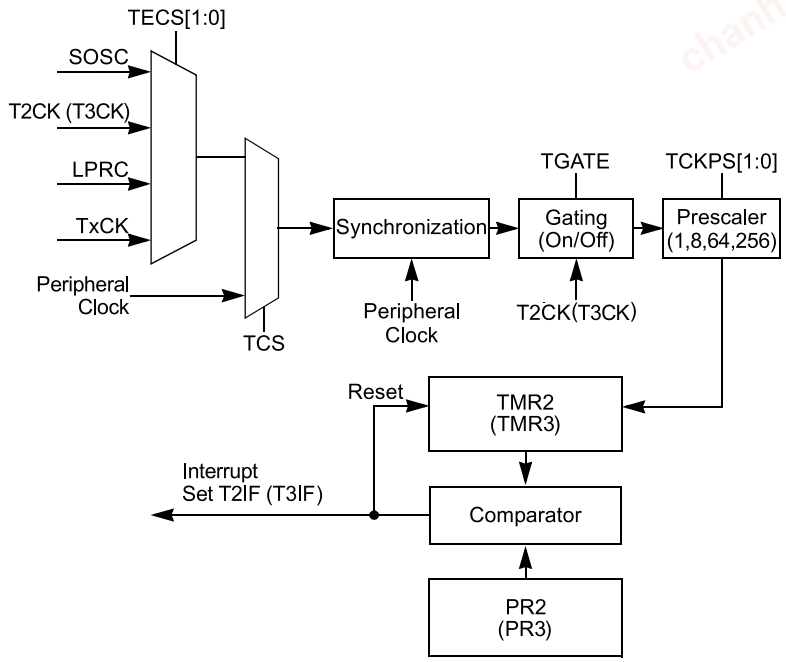
To configure any of the timers for individual 16-bit operation:

1. Clear the T32 bit (T2CON[3] for Timer2 and Timer3).
2. Select the timer prescaler ratio using the TCKPS[1:0] bits.
3. Set the Clock and Gating modes using the TCS and TGATE bits. See 11.4 Peripheral Pin Select (PPS) for more information.
4. Load the timer period value into the PRx register.
5. If interrupts are required, set the Timerx Interrupt Enable bit, TxIE. Use the Timerx Interrupt Priority bits, TxIP[2:0], to set the interrupt priority.
6. Set the TON bit (= 1).

The 16-bit timer is shown in Figure 13-2.

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Figure 13-2. 16-Bit Timer Block Diagram



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13.1 Timer2/3 and Timer4/5 Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x0195	Reserved									
0x0196	TMR2	7:0	TMR2[7:0]							
		15:8	TMR2[15:8]							
0x0198	TMR3HLD	7:0	TMR3HLD[7:0]							
		15:8	TMR3HLD[15:8]							
0x019A	TMR3	7:0	TMR3[7:0]							
		15:8	TMR3[15:8]							
0x019C	PR2	7:0	PR2[7:0]							
		15:8	PR2[15:8]							
0x019E	PR3	7:0	PR3[7:0]							
		15:8	PR3[15:8]							
0x01A0	T2CON	7:0		TGATE	TCKPS[1:0]		T32	TSYNC	TCS	
		15:8	TON		TSIDL				TECS[1:0]	
0x01A2	T3CON	7:0		TGATE	TCKPS[1:0]			TSYNC	TCS	
		15:8	TON		TSIDL				TECS[1:0]	

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13.1.1 Timer2 Counter Register

Name: TMR2
Offset: 0x196

Bit	15	14	13	12	11	10	9	8
	TMR2[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TMR2[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TMR2[15:0] Timer2 Value bits

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13.1.2 Timer3 Holding Register (for 32-bit timer operations only)

Name: TMR3HLD
Offset: 0x198

Bit	15	14	13	12	11	10	9	8
	TMR3HLD[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TMR3HLD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TMR3HLD[15:0] Timer3 Holding Value bits

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13.1.3 Timer3 Counter Register

Name: TMR3
Offset: 0x19A

Bit	15	14	13	12	11	10	9	8
	TMR3[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TMR3[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TMR3[15:0] Timer3 Value bits

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13.1.4 Timer2 Period Register

Name: PR2
Offset: 0x19C

Bit	15	14	13	12	11	10	9	8
	PR2[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PR2[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PR2[15:0] Timer2 Period Value bits

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13.1.5 Timer3 Period Register

Name: PR3
Offset: 0x19E

Bit	15	14	13	12	11	10	9	8
	PR3[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PR3[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PR3[15:0] Timer3 Period Value bits

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13.1.6 Timer2 Control Register

Name: T2CON
Offset: 0x1A0

Note:

1. Changing the value of T2CON while the timer is running (TON = 1) causes the timer prescale counter to reset and is not recommended.

Bit	15	14	13	12	11	10	9	8
	TON		TSIDL				TECS[1:0]	
Access	R/W		R/W				R/W	R/W
Reset	0		0				0	0

Bit	7	6	5	4	3	2	1	0
		TGATE	TCKPS[1:0]		T32	TSYNC	TCS	
Access		R/W	R/W	R/W	R/W	R/W	R/W	
Reset		0	0	0	0	0	0	

Bit 15 – TON Timer2 On bit(1)

Value	Description
1	Starts 16-bit Timer
0	Stops 16-bit Timer

Bit 13 – TSIDL Timer2 Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode
0	Continues module operation in Idle mode

Bits 9:8 – TECS[1:0] Timer2 Extended Clock Select bits (selected when TCS = 1)

Value	Description
11	Generic timer (TxCK) external input
10	LPRC Oscillator
01	T1CK external clock input
00	SOSC

Bit 6 – TGATE Timer2 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:

Value	Description
1	Gated time accumulation is enabled
0	Gated time accumulation is disabled

Bits 5:4 – TCKPS[1:0] Timer2 Input Clock Prescale Select bits

Value	Description
11	1:256
10	1:64
01	1:8
00	1:1

Bit 3 – T32 32-Bit Timer Mode Select bit
In 32-bit mode, T3CON control bits do not affect 32-bit timer operation.

Value	Description
1	Timer2 and Timer3 form a single 32-bit timer
0	Timer2 and Timer3 act as two 16-bit timers

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Bit 2 – TSYNC Timer2 External Clock Input Synchronization Select bit(1)

When TCS = 0:

This bit is ignored.

When TCS = 1:

Value	Description
1	Synchronizes the external clock input
0	Does not synchronize the external clock input

Bit 1 – TCS Timer2 Clock Source Select bit

Value	Description
1	External clock source selected by TECS[1:0]
0	Internal peripheral clock (F_{OSC})

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13.1.7 Timer3 Control Register

Name: T3CON
Offset: 0x1A2

Note:

1. Changing the value of T3CON while the timer is running (TON = 1) causes the timer prescale counter to reset and is not recommended.

Bit	15	14	13	12	11	10	9	8
	TON		TSIDL				TECS[1:0]	
Access	R/W		R/W				R/W	R/W
Reset	0		0				0	0

Bit	7	6	5	4	3	2	1	0
		TGATE	TCKPS[1:0]			TSYNC	TCS	
Access		R/W	R/W	R/W		R/W	R/W	
Reset		0	0	0		0	0	

Bit 15 – TON Timer3 On bit(1)

Value	Description
1	Starts 16-bit Timer
0	Stops 16-bit Timer

Bit 13 – TSIDL Timer3 Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode
0	Continues module operation in Idle mode

Bits 9:8 – TECS[1:0] Timer3 Extended Clock Select bits (selected when TCS = 1)

Value	Description
11	Generic timer (TxCK) external input
10	LPRC Oscillator
01	T1CK external clock input
00	SOSC

Bit 6 – TGATE Timer3 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:

Value	Description
1	Gated time accumulation is enabled
0	Gated time accumulation is disabled

Bits 5:4 – TCKPS[1:0] Timer3 Input Clock Prescale Select bits

Value	Description
11	1:256
10	1:64
01	1:8
00	1:1

Bit 2 – TSYNC Timer3 External Clock Input Synchronization Select bit(1)
When TCS = 0:
This bit is ignored.
When TCS = 1:

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Value	Description
1	Synchronizes the external clock input
0	Does not synchronize the external clock input

Bit 1 – TCS Timer3 Clock Source Select bit

Value	Description
1	External clock source selected by TECS[1:0]
0	Internal peripheral clock (F_{OSC})

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14. Capture/Compare/PWM/Timer Modules (MCCP)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to **"Capture/Compare/PWM/Timer (MCCP and SCCP)"** (www.microchip.com/DS30003035) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

PIC24FJ64GP205/GU205 family devices include several Capture/Compare/PWM/Timer base modules, which provide the functionality of three different peripherals of earlier PIC24F devices. The module can operate in one of three major modes:

- General Purpose Timer
- Input Capture
- Output Compare/PWM

This family of devices features five instances of the MCCP module. MCCP1-5 provide up to two outputs and an extended range of power control features.

The MCCPx modules can be operated only in one of the three major modes at any time. The other modes are not available unless the module is reconfigured for the new mode.

A conceptual block diagram for the module is shown in Figure 14-1. All three modules share a time base generator and a common Timer register pair (CCPxTMRH/L); other shared hardware components are added as a particular mode requires.

Each module has a total of seven control and status registers:

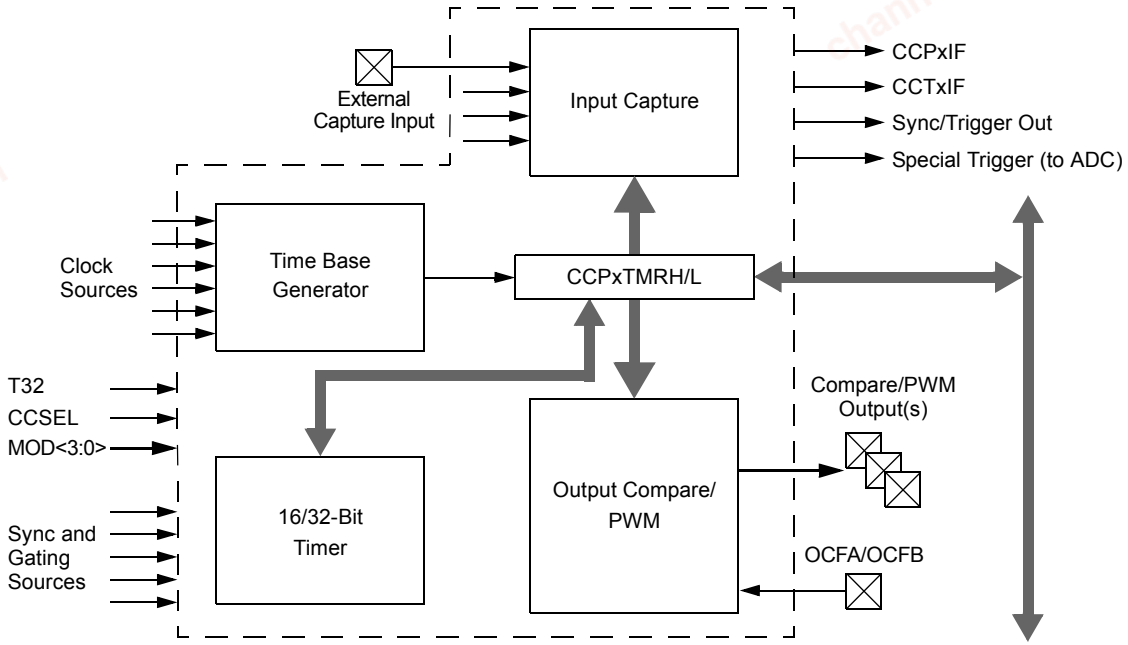
- CCPxCON1L
- CCPxCON1H
- CCPxCON2L
- CCPxCON2H
- CCPxCON3L
- CCPxCON3H
- CCPxSTATL

Each module also includes ten buffer/counter registers that serve as Timer Value registers or data holding buffers:

- CCPxTMRH/CCPxTMRL (Timer High/Low Counters)
- CCPxPRH/CCPxPRL (Timer Period High/Low)
- CCPxRAH/CCPxRAL (Primary Output Compare Data Buffer)
- CCPxRBH/CCPxRBL (Secondary Output Compare Data Buffer)
- CCPxBUFH/CCPxBUFL (Input Capture High/Low Buffers)

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Figure 14-1. MCCP Conceptual Block Diagram

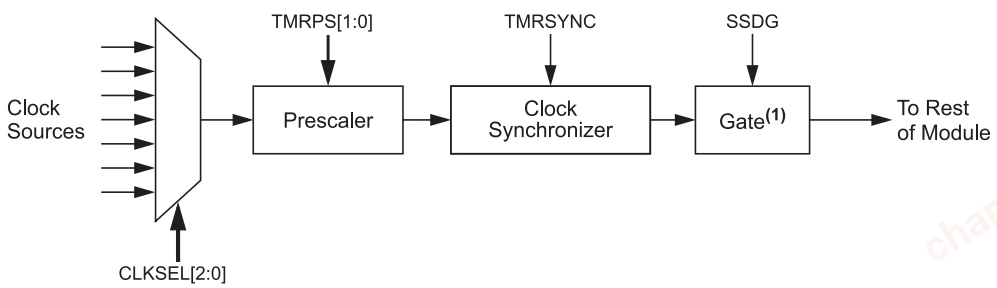


14.1 Time Base Generator

The Timer Clock Generator (TCG) generates a clock for the module's internal time base using one of the clock signals already available on the microcontroller. This is used as the time reference for the module in its three major modes. The internal time base is shown in Figure 14-2.

There are eight inputs available to the clock generator, which are selected using the CLKSEL[2:0] bits (CCPxCON1L[10:8]). Available sources include the FRC and LPRC, the Secondary Oscillator and the TCLKI external clock inputs. The system clock is the default source (CLKSEL[2:0] = 000). On PIC24FJ64GP205/GU205 family devices, clock sources to the MCCPx module can be synchronized with the system clock. As a result, when clock sources are selected, clock input timing restrictions or module operating restrictions may exist.

Figure 14-2. Timer Clock Generator



Note:

1. Gating available in Timer modes only.

14.2 General Purpose Timer

Timer mode is selected when CCSEL = 0 and MOD[3:0] = 0000. The timer can function as a 32-bit timer or a dual 16-bit timer, depending on the setting of the T32 bit (Table 14-1).

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Table 14-1. Timer Operation Mode

T32 (CCPxCON1L[5])	Operating Mode
0	Dual Timer Mode (16-bit)
1	Timer Mode (32-bit)

Dual 16-Bit Timer mode (Figure 14-3) provides a simple timer function with two independent 16-bit timer/counters. The primary timer uses the CCPxTMRL and CCPxPRL registers. Only the primary timer can interact with other modules on the device. It generates the MCCPx Sync out signals for use by other MCCPx modules. It can also use the SYNC[4:0] bits' signal generated by other modules.

The secondary timer uses the CCPxTMRH and CCPxPRH registers. It is intended to be used only as a periodic interrupt source for scheduling CPU events. It does not generate an output Sync/Trigger mode signal like the primary time base. In Dual Timer mode, the Timer Period High register, CCPxPRH, generates the MCCPx compare event (CCPxIF) used by many other modules on the device.

The 32-Bit Timer mode (Figure 14-4) uses the CCPxTMRL and CCPxTMRH registers, together, as a single 32-bit timer. When CCPxTMRL overflows, CCPxTMRH increments by one. This mode provides a simple timer function when it is important to track long time periods. Note that the T32 bit (CCPxCON1L[5]) should be set before the CCPxTMRL or CCPxPRH registers are written to initialize the 32-bit timer.

14.2.1 Sync and Trigger Operation

In both 16-bit and 32-bit modes, the timer can also function in either Synchronization ("Sync") or Trigger mode operation. Both use the SYNC[4:0] bits (CCPxCON1H[4:0]) to determine the input signal source. The difference is how that signal affects the timer.

In Sync mode operation, the Timer Reset or clear occurs when the input selected by SYNC[4:0] is asserted. The timer immediately begins to count again from zero unless it is held for some other reason. Sync operation is used whenever the TRIGEN bit (CCPxCON1H[7]) is cleared. The SYNC[4:0] bits can have any value except '11111'.

In Trigger mode operation, the timer is held in Reset until the input selected by SYNC[4:0] is asserted; when it occurs, the timer starts counting. Trigger operation is used whenever the TRIGEN bit is set. In Trigger mode, the timer will continue running after a trigger event as long as the CCPTRIG bit (CCPxSTATL[7]) is set. To clear CCPTRIG, the TRCLR bit (CCPxSTATL[5]) must be set to clear the trigger event, reset the timer and hold it at zero until another trigger event occurs. On PIC24FJ64GP205/GU205 family devices, Trigger mode operation can only be used when the peripheral clock is the time base source (CLKSEL[2:0] = 000).

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Figure 14-3. Dual 16-Bit Timer Mode

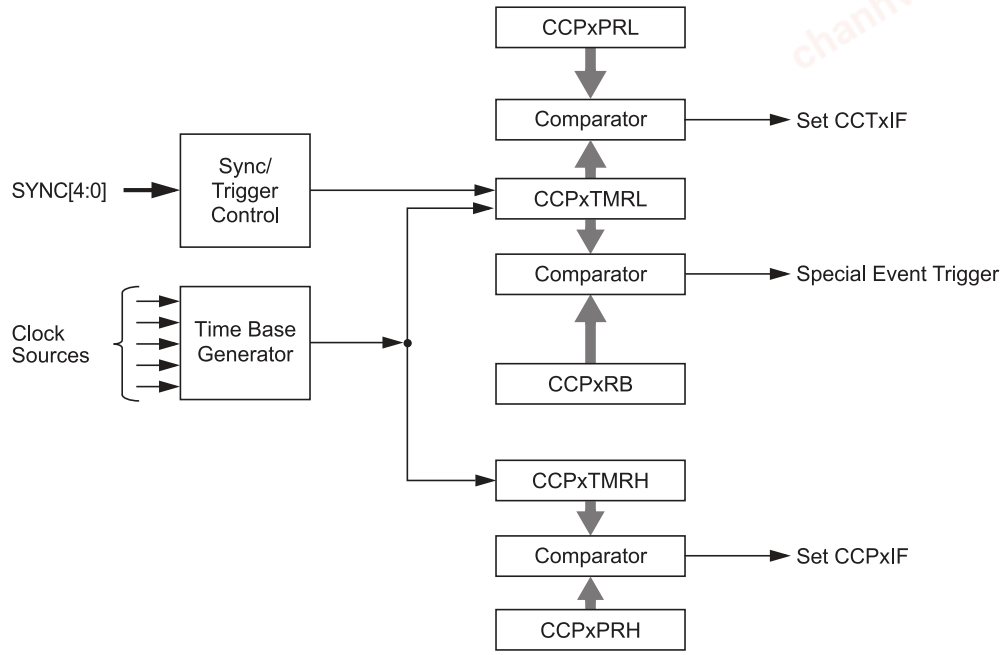
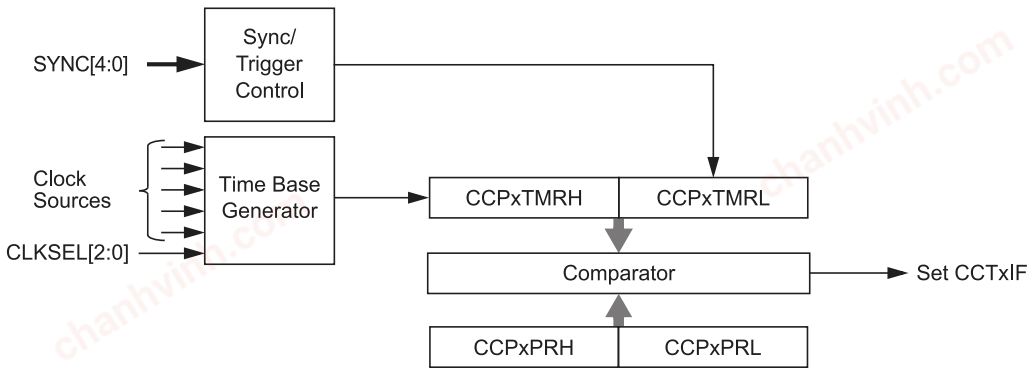


Figure 14-4. 32-Bit Timer Mode



14.3 Output Compare Mode

Output Compare mode compares the Timer register value with the value of one or two Compare registers, depending on its mode of operation. The output compare module, on compare match events, has the ability to generate a single output transition or a train of output pulses. Like most PIC® MCU peripherals, the output compare module can also generate interrupts on a compare match event.

Table 14-2 shows the various modes available in Output Compare modes. Figure 14-5 depicts a simplified block diagram of the Output Compare mode.

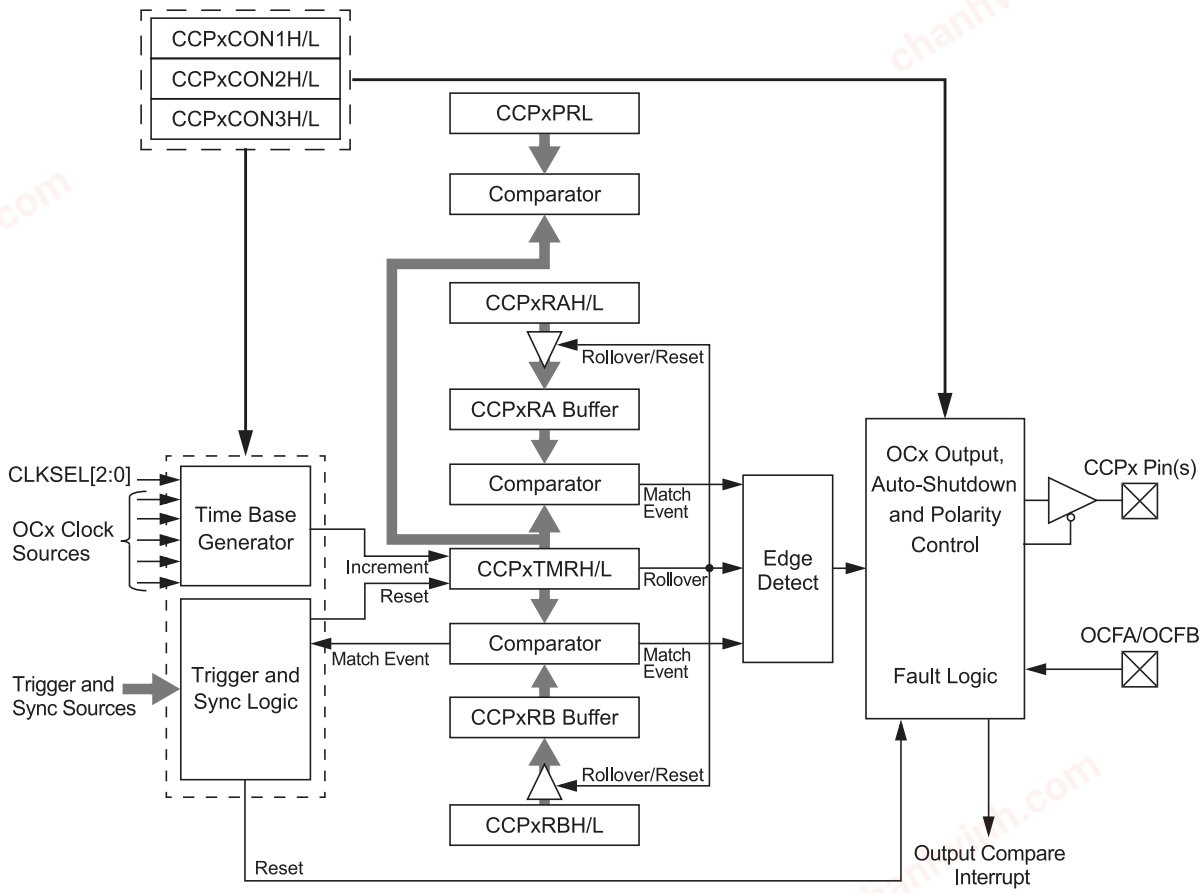
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Table 14-2. Output Compare/PWM Modes

MOD[3:0] (CCPxCON1L[3:0])	T32 (CCPxCON1L[5])	Operating Mode	
0001	0	Output High on Compare (16-bit)	Single Edge Mode
0001	1	Output High on Compare (32-bit)	
0010	0	Output Low on Compare (16-bit)	
0010	1	Output Low on Compare (32-bit)	
0011	0	Output Toggle on Compare (16-bit)	
0011	1	Output Toggle on Compare (32-bit)	
0100	0	Dual Edge Compare (16-bit)	Dual Edge Mode
0101	0	Dual Edge Compare (16-bit buffered)	PWM Mode
1111	0	External Input Source Mode (16-bit)	Center PWM Mode

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Figure 14-5. Output Compare Block Diagram



14.4 Input Capture Mode

Input Capture mode is used to capture a timer value from an independent timer base upon an event on an input pin or other internal trigger source. The input capture features are useful in applications requiring frequency (time period) and pulse measurement. Figure 14-6 depicts a simplified block diagram of the Input Capture mode.

Input Capture mode uses a dedicated 16/32-bit, synchronous, up counting timer for the capture function. The timer value is written to the FIFO when a capture event occurs. The internal value may be read (with a synchronization delay) using the CCPxTMRH/L registers.

To use Input Capture mode, the CCSEL bit (CCPxCON1L[4]) must be set. The T32 and MOD[3:0] bits are used to select the proper Capture mode, as shown in Table 14-3.

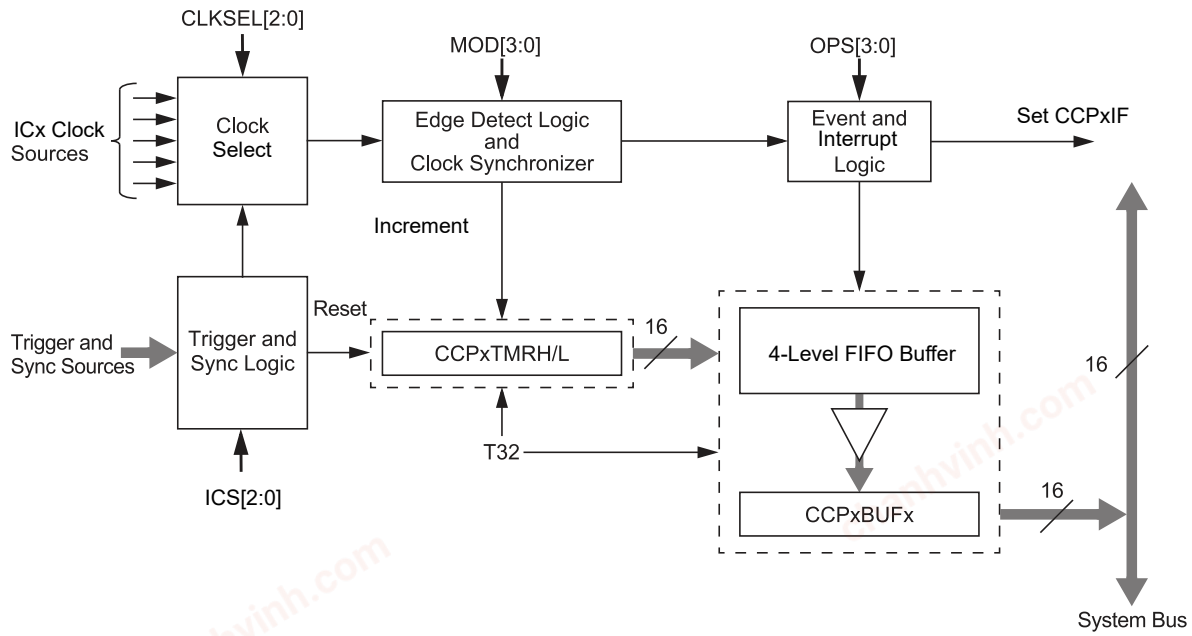
Table 14-3. Input Capture Modes

MOD[3:0] (CCPxCON1L[3:0])	T32 (CCPxCON1L[5])	Operating Mode
0000	0	Edge Detect (16-bit capture)
0000	1	Edge Detect (32-bit capture)
0001	0	Every Rising (16-bit capture)
0001	1	Every Rising (32-bit capture)
0010	0	Every Falling (16-bit capture)
0010	1	Every Falling (32-bit capture)

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.....continued		
MOD[3:0] (CCPxCON1L[3:0])	**T32 (CCPxCON1L[5])**	**Operating Mode**
0011	0	Every Rise/Fall (16-bit capture)
0011	1	Every Rise/Fall (32-bit capture)
0100	0	Every 4th Rising (16-bit capture)
0100	1	Every 4th Rising (32-bit capture)
0101	0	Every 16th Rising (16-bit capture)
0101	1	Every 16th Rising (32-bit capture)

Figure 14-6. Input Capture Block Diagram



14.5 Auxiliary Output

The MCCPx modules have an auxiliary (secondary) output that provides other peripherals access to internal module signals. The auxiliary output is intended to connect to other MCCPx modules, or other digital peripherals, to provide these types of functions:

- Time Base Synchronization
- Peripheral Trigger and Clock Inputs
- Signal Gating

The type of output signal is selected using the AUXOUT[1:0] control bits (CCPxCON2H[4:3]). The type of output signal is also dependent on the module operating mode, as shown in Table 14-4.

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Table 14-4. Auxiliary Output

AUXOUT[1:0]	CCSEL	MOD[3:0]	Comments	Signal Description
00	x	xxxx	Auxiliary Output Disabled	No Output
01	0	0000	Time Base Modes	Time Base Period Reset or Rollover
10				Special Event Trigger Output
11				No Output
01	0	0001 through 1111	Output Compare Modes	Time Base Period Reset or Rollover
10				Output Compare Event Signal
11				Output Compare Signal
01	1	xxxx	Input Capture Modes	Time Base Period Reset or Rollover
10				Reflects the Value of the ICDIS bit
11				Input Capture Event Signal

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14.6 MCCP Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x026B	Reserved									
0x026C	CCP1CON1L	7:0	TMRPS[1:0]		T32	CCSEL	MOD[3:0]			
		15:8	CCPON		CCPSIDL	CCPSLP	TMRSYNC	CLKSEL[2:0]		
0x026E	CCP1CON1H	7:0	TRIGEN	ONESHOT	ALTSYNC	SYNC[4:0]				
		15:8	OPSSRC	RTRGEN			OPS3[3:0]			
0x0270	CCP1CON2L	7:0	ASDG[7:0]							
		15:8	PWMRSEN	ASDGM		SSDG				
0x0272	CCP1CON2H	7:0	ICGSM[1:0]			AUXOUT[1:0]		ICS[2:0]		
		15:8	OENSYNC		OC[F:A]EN					
0x0274	CCP1CON3L	7:0				DT[4:0]				
		15:8								
0x0276	CCP1CON3H	7:0			POLACE	POLBDF	PSSACE[1:0]		PSSBDF[1:0]	
		15:8	OETRIG		OSCNT[2:0]			OUTM[2:0]		
0x0278	CCP1STATL	7:0	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE
		15:8						ICGARM		
0x027A ... 0x027B	Reserved									
0x027C	CCP1TMRL	7:0	TMRL[7:0]							
		15:8	TMRL[15:8]							
0x027E	CCP1TMRH	7:0	TMRH[23:16]							
		15:8	TMRH[31:24]							
0x0280	CCP1PRL	7:0	PRL[7:0]							
		15:8	PRL[15:8]							
0x0282	CCP1PRH	7:0	PRH[23:16]							
		15:8	PRH[31:24]							
0x0284	CCP1RA	7:0	CMP[7:0]							
		15:8	CMP[15:8]							
0x0286 ... 0x0287	Reserved									
0x0288	CCP1RB	7:0	CMP[7:0]							
		15:8	CMP[15:8]							
0x028A ... 0x028B	Reserved									
0x028C	CCP1BUFL	7:0	BUF[7:0]							
		15:8	BUF[15:8]							
0x028E	CCP1BUFH	7:0	BUF[23:16]							
		15:8	BUF[31:24]							
0x0290	CCP2CON1L	7:0	TMRPS[1:0]		T32	CCSEL	MOD[3:0]			
		15:8	CCPON		CCPSIDL	CCPSLP	TMRSYNC	CLKSEL[2:0]		
0x0292	CCP2CON1H	7:0	TRIGEN	ONESHOT	ALTSYNC	SYNC[4:0]				
		15:8	OPSSRC	RTRGEN			OPS3[3:0]			
0x0294	CCP2CON2L	7:0	ASDG[7:0]							
		15:8	PWMRSEN	ASDGM		SSDG				
0x0296	CCP2CON2H	7:0	ICGSM[1:0]			AUXOUT[1:0]		ICS[2:0]		
		15:8	OENSYNC		OC[F:A]EN					
0x0298	CCP2CON3L	7:0				DT[4:0]				
		15:8								
0x029A	CCP2CON3H	7:0			POLACE	POLBDF	PSSACE[1:0]		PSSBDF[1:0]	
		15:8	OETRIG		OSCNT[2:0]			OUTM[2:0]		
0x029C	CCP2STATL	7:0	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE
		15:8						ICGARM		

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x029E ... 0x029F	Reserved									
0x02A0	CCP2TMRL	7:0	TMRL[7:0]							
		15:8	TMRL[15:8]							
0x02A2	CCP2TMRH	7:0	TMRH[23:16]							
		15:8	TMRH[31:24]							
0x02A4	CCP2PRL	7:0	PRL[7:0]							
		15:8	PRL[15:8]							
0x02A6	CCP2PRH	7:0	PRH[23:16]							
		15:8	PRH[31:24]							
0x02A8	CCP2RA	7:0	CMP[7:0]							
		15:8	CMP[15:8]							
0x02AA ... 0x02AB	Reserved									
0x02AC	CCP2RB	7:0	CMP[7:0]							
		15:8	CMP[15:8]							
0x02AE ... 0x02B3	Reserved									
0x02B4	CCP3CON1L	7:0	TMRPS[1:0]		T32	CCSEL	MOD[3:0]			
		15:8	CCPON		CCPSIDL	CCPSLP	TMRSYNC	CLKSEL[2:0]		
0x02B6	CCP3CON1H	7:0	TRIGEN	ONESHOT	ALTSYNC	SYNC[4:0]				
		15:8	OPSSRC	RTRGEN			OPS3[3:0]			
0x02B8	CCP3CON2L	7:0	ASDG[7:0]							
		15:8	PWMRSEN	ASDGM		SSDG				
0x02BA	CCP3CON2H	7:0	ICGSM[1:0]			AUXOUT[1:0]		ICS[2:0]		
		15:8	OENSYNC		OC[F:A]EN					
0x02BC	CCP3CON3L	7:0				DT[4:0]				
		15:8								
0x02BE	CCP3CON3H	7:0			POLACE	POLBDF	PSSACE[1:0]		PSSBDF[1:0]	
		15:8	OETRIG		OSCNT[2:0]			OUTM[2:0]		
0x02C0	CCP3STATL	7:0	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE
		15:8						ICGARM		
0x02C2 ... 0x02C3	Reserved									
0x02C4	CCP3TMRL	7:0	TMRL[7:0]							
		15:8	TMRL[15:8]							
0x02C6	CCP3TMRH	7:0	TMRH[23:16]							
		15:8	TMRH[31:24]							
0x02C8	CCP3PRL	7:0	PRL[7:0]							
		15:8	PRL[15:8]							
0x02CA	CCP3PRH	7:0	PRH[23:16]							
		15:8	PRH[31:24]							
0x02CC	CCP3RA	7:0	CMP[7:0]							
		15:8	CMP[15:8]							
0x02CE ... 0x02CF	Reserved									
0x02D0	CCP3RB	7:0	CMP[7:0]							
		15:8	CMP[15:8]							
0x02D2 ... 0x02D3	Reserved									
0x02D4	CCP3BUFL	7:0	BUF[7:0]							
		15:8	BUF[15:8]							

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x02D6	CCP3BUFH	7:0	BUF[23:16]							
		15:8	BUF[31:24]							
0x02D8 ... 0x02FF	Reserved									
0x0300	CCP4CON1L	7:0	TMRPS[1:0]		T32	CCSEL	MOD[3:0]			
		15:8	CCPON		CCPSIDL	CCPSLP	TMRSYNC	CLKSEL[2:0]		
0x0302	CCP4CON1H	7:0	TRIGEN	ONESHOT	ALTSYNC	SYNC[4:0]				
		15:8	OPSSRC	RTRGEN			OPS3[3:0]			
0x0304	CCP4CON2L	7:0	ASDG[7:0]							
		15:8	PWMRSEN	ASDGM		SSDG				
0x0306	CCP4CON2H	7:0	ICGSM[1:0]			AUXOUT[1:0]		ICS[2:0]		
		15:8	OENSYNC		OC[F:A]EN					
0x0308	CCP4CON3L	7:0				DT[4:0]				
		15:8								
0x030A	CCP4CON3H	7:0			POLACE	POLBDF	PSSACE[1:0]		PSSBDF[1:0]	
		15:8	OETRIG		OSCNT[2:0]			OUTM[2:0]		
0x030C	CCP4STATL	7:0	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE
		15:8						ICGARM		
0x030E ... 0x030F	Reserved									
0x0310	CCP4TMRL	7:0	TMRL[7:0]							
		15:8	TMRL[15:8]							
0x0312	CCP4TMRH	7:0	TMRH[23:16]							
		15:8	TMRH[31:24]							
0x0314	CCP4PRL	7:0	PRL[7:0]							
		15:8	PRL[15:8]							
0x0316	CCP4PRH	7:0	PRH[23:16]							
		15:8	PRH[31:24]							
0x0318	CCP4RA	7:0	CMP[7:0]							
		15:8	CMP[15:8]							
0x031A ... 0x031B	Reserved									
0x031C	CCP4RB	7:0	CMP[7:0]							
		15:8	CMP[15:8]							
0x031E ... 0x031F	Reserved									
0x0320	CCP4BUFL	7:0	BUF[7:0]							
		15:8	BUF[15:8]							
0x0322	CCP4BUFH	7:0	BUF[23:16]							
		15:8	BUF[31:24]							
0x0324	CCP5CON1L	7:0	TMRPS[1:0]		T32	CCSEL	MOD[3:0]			
		15:8	CCPON		CCPSIDL	CCPSLP	TMRSYNC	CLKSEL[2:0]		
0x0326	CCP5CON1H	7:0	TRIGEN	ONESHOT	ALTSYNC	SYNC[4:0]				
		15:8	OPSSRC	RTRGEN			OPS3[3:0]			
0x0328	CCP5CON2L	7:0	ASDG[7:0]							
		15:8	PWMRSEN	ASDGM		SSDG				
0x032A	CCP5CON2H	7:0	ICGSM[1:0]			AUXOUT[1:0]		ICS[2:0]		
		15:8	OENSYNC		OC[F:A]EN					
0x032C	CCP5CON3L	7:0				DT[4:0]				
		15:8								
0x032E	CCP5CON3H	7:0			POLACE	POLBDF	PSSACE[1:0]		PSSBDF[1:0]	
		15:8	OETRIG		OSCNT[2:0]			OUTM[2:0]		
0x0330	CCP5STATL	7:0	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE
		15:8						ICGARM		

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0332 ... 0x0333	Reserved									
0x0334	CCP5TMRL	7:0	TMRL[7:0]							
		15:8	TMRL[15:8]							
0x0336	CCP5TMRH	7:0	TMRH[23:16]							
		15:8	TMRH[31:24]							
0x0338	CCP5PRL	7:0	PRL[7:0]							
		15:8	PRL[15:8]							
0x033A	CCP5PRH	7:0	PRH[23:16]							
		15:8	PRH[31:24]							
0x033C	CCP5RA	7:0	CMP[7:0]							
		15:8	CMP[15:8]							
0x033E ... 0x033F	Reserved									
0x0340	CCP5RB	7:0	CMP[7:0]							
		15:8	CMP[15:8]							
0x0342 ... 0x0343	Reserved									
0x0344	CCP5BUFL	7:0	BUF[7:0]							
		15:8	BUF[15:8]							
0x0346	CCP5BUFH	7:0	BUF[23:16]							
		15:8	BUF[31:24]							

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14.6.1 CCP1 Control 1 Low Register

Name: CCP1CON1L
Offset: 0x26C

Bit	15	14	13	12	11	10	9	8
	CCPON		CCPSIDL	CCPSLP	TMRSYNC	CLKSEL[2:0]		
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TMRPS[1:0]		T32	CCSEL	MOD[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – CCPON CCP Module Enable bit

Value	Description
1	Module is enabled with an operating mode specified by the MOD[3:0] control bits
0	Module is disabled

Bit 13 – CCPSIDL CCP Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode
0	Continues module operation in Idle mode

Bit 12 – CCPSLP CCP Sleep Mode Enable bit

Value	Description
1	Module continues to operate in Sleep modes
0	Module does not operate in Sleep modes

Bit 11 – TMRSYNC Time Base Clock Synchronization bit

Value	Description
1	Module time base clock is synchronized to the internal system clocks; timing restrictions apply
0	Module time base clock is not synchronized to the internal system clocks

Bits 10:8 – CLKSEL[2:0] CCP Time Base Clock Select bits

Value	Description
111	TCKIA pin
110	TCKIB pin
101	PLL clock
100	2x peripheral clock
011	CLC1
010	SOSC clock
001	Reference clock output
000	Peripheral clock

Bits 7:6 – TMRPS[1:0] Time Base Prescale Select bits

Value	Description
11	1:64 prescaler
10	1:16 prescaler
01	1:4 prescaler
00	1:1 prescaler

Bit 5 – T32 32-Bit Time Base Select bit

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Value	Description
1	Uses 32-bit time base for timer, single edge output compare or input capture function
0	Uses 16-bit time base for timer, single edge output compare or input capture function

Bit 4 – CCSEL Capture/Compare Mode Select bit

Value	Description
1	Input capture peripheral
0	Output Compare/PWM/Timer peripheral (exact function is selected by the MOD[3:0] bits)

Bits 3:0 – MOD[3:0] CCP Mode Select bits

For CCSEL = 1 (Input Capture modes):

Value	Description
1xxx	Reserved
011x	Reserved
0101	Capture every 16th rising edge
0100	Capture every 4th rising edge
0011	Capture every rising and falling edge
0010	Capture every falling edge
0001	Capture every rising edge
0000	Capture every rising and falling edge (Edge Detect mode)

For CCSEL = 0 (Output Compare/Timer modes):

Value	Description
1111	External Input mode: Pulse generator is disabled, source is selected by ICS[2:0]
1110	Reserved
110x	Reserved
10xx	Reserved
0101	Dual Edge Compare mode, buffered
0100	Dual Edge Compare mode
0011	16-Bit/32-Bit Single Edge mode, toggles output on compare match
0010	16-Bit/32-Bit Single Edge mode, drives output low on compare match
0001	16-Bit/32-Bit Single Edge mode, drives output high on compare match
0000	16-Bit/32-Bit Timer mode, output functions are disabled

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14.6.2 CCP1 Control 1 High Register

Name: CCP1CON1H
Offset: 0x26E

Notes:

1. This control bit has no function in Input Capture modes.
2. This control bit has no function when TRIGEN = 0.
3. Output postscale settings, from 1:5 to 1:16 (0100-1111), will result in a FIFO buffer overflow for Input Capture modes.

Bit	15	14	13	12	11	10	9	8
	OPSSRC	RTRGEN			OPS3[3:0]			
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRIGEN	ONESHOT	ALTSYNC	SYNC[4:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OPSSRC Output Postscaler Source Select bit(1)

Value	Description
1	Output postscaler scales module trigger output events
0	Output postscaler scales time base interrupt events

Bit 14 – RTRGEN Retrigger Enable bit(2)

Value	Description
1	Time base can be retriggered when TRIGEN bit = 1
0	Time base may not be retriggered when TRIGEN bit = 1

Bits 11:8 – OPS3[3:0] CCP Interrupt Output Postscale Select bits(3)

Value	Description
1111	Interrupt every 16th time base period match
1110	Interrupt every 15th time base period match
. . .	
0100	Interrupt every 5th time base period match
0011	Interrupt every 4th time base period match or 4th input capture event
0010	Interrupt every 3rd time base period match or 3rd input capture event
0001	Interrupt every 2nd time base period match or 2nd input capture event
0000	Interrupt after each time base period match or input capture event

Bit 7 – TRIGEN CCP Trigger Enable bit

Value	Description
1	Trigger operation of time base is enabled
0	Trigger operation of time base is disabled

Bit 6 – ONESHOT One-Shot Trigger Mode Enable bit

Value	Description
1	One-Shot Trigger mode is enabled; trigger duration is set by OSCNT[2:0]
0	One-Shot Trigger mode is disabled

Bit 5 – ALTSYNC CCP Clock Select bit

Value	Description
1	An alternate signal is used as the module synchronization output signal
0	The module synchronization output signal is the Time Base Reset/rollover event

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Bits 4:0 – SYNC[4:0] CCP Synchronization Source Select bits

SYNC[4:0]	Synchronization Source
11111	None; timer with rollover on CCP1PR match or FFFFh
11110	Reserved
11101	Reserved
11100	Reserved
11011	A/D start conversion
11010	CMP3 trigger
11001	CMP2 trigger
11000	CMP1 trigger
10111	Reserved
10110	Reserved
10101	Reserved
10100	Reserved
10011	CLC4 output
10010	CLC3 output
10001	CLC2 output
10000	CLC1 output
01111	Reserved
01101	INT4 pin
01100	INT3 pin
01011	INT2 pin
01010	INT1 pin
01001	INT0 pin
00110	MCCP5 sync output
00101	MCCP4 sync output
00100	MCCP3 sync output
00011	MCCP2 sync output
00010	MCCP1 sync output
00001	MCCPx sync output
00000	MCCP1 timer sync output

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14.6.3 CCP1 Control 2 Low Register

Name: CCP1CON2L
Offset: 0x270

Bit	15	14	13	12	11	10	9	8
	PWMRSEN	ASDGM		SSDG				
Access	R/W	R/W		R/W				
Reset	0	0		0				

Bit	7	6	5	4	3	2	1	0
	ASDG[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – PWMRSEN CCP PWM Restart Enable bit

Value	Description
1	ASEVT bit clears automatically at the beginning of the next PWM period, after the shutdown input has ended
0	ASEVT bit must be cleared in software to resume PWM activity on output pins

Bit 14 – ASDGM CCP Auto-Shutdown Gate Mode Enable bit

Value	Description
1	Waits until next Time Base Reset or rollover for shutdown to occur
0	Shutdown event occurs immediately

Bit 12 – SSDG CCP Software Shutdown/Gate Control bit

Value	Description
1	Manually forces auto-shutdown, timer clock gate or input capture signal gate event (setting of ASDGM bit still applies)
0	Normal module operation

Bits 7:0 – ASDG[7:0] CCP Auto-Shutdown/Gating Source Enable bits

Value	Description
10000000	OCFB
01000000	OCFA
00100000	CLC1
00010000	MCCP2
00001000	MCCP3
00000100	CMP3 out
00000010	CMP2 out
00000001	CMP1 out

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14.6.4 CCP1 Control 2 High Register

Name: CCP1CON2H
Offset: 0x272

Bit	15	14	13	12	11	10	9	8
	OENSYNC		OC[F:A]EN					
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ICGSM[1:0]			AUXOUT[1:0]		ICS[2:0]		
Access	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Reset	0	0		0	0	0	0	0

Bit 15 – OENSYNC Output Enable Synchronization bit

Value	Description
1	Update by output enable bits occurs on the next Time Base Reset or rollover
0	Update by output enable bits occurs immediately

Bits 13:8 – OC[F:A]EN Output Enable/Steering Control bits

Value	Description
1	OCx pin is controlled by the CCPx module and produces an output compare or PWM signal
0	OCx pin is not controlled by the CCPx module; the pin is available to the port logic or another peripheral multiplexed on the pin

Bits 7:6 – ICGSM[1:0] Input Capture Gating Source Mode Control bits

Value	Description
11	Reserved
10	One-Shot mode: Falling edge from gating source disables future capture events (ICDIS = 1)
01	One-Shot mode: Rising edge from gating source enables future capture events (ICDIS = 0)
00	Level-Sensitive mode: A high level from gating source will enable future capture events; a low level will disable future capture events

Bits 4:3 – AUXOUT[1:0] Auxiliary Output Signal on Event Selection bits

Value	Description
11	Input capture or output compare event; no signal in Timer mode
10	Signal output depends on module operating mode
01	Time base rollover event (all modes)
00	Disabled

Bits 2:0 – ICS[2:0] Input Capture Source Select bits

Value	Description
111	CLC4
110	CLC3
101	CLC2
100	CLC1
011	Comparator 3
010	Comparator 2
001	Comparator 1
000	Input capture pin (ICM1)

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14.6.5 CCP1 Control 3 Low Register

Name: CCP1CON3L
Offset: 0x274

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				DT[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – DT[4:0] PWM Dead-Time Select bits

Value	Description
111111	Inserts 63 dead-time delay periods between complementary output signals
111110	Inserts 62 dead-time delay periods between complementary output signals
...	
000010	Inserts 2 dead-time delay periods between complementary output signals
000001	Inserts 1 dead-time delay period between complementary output signals
000000	Dead-time logic is disabled

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14.6.6 CCP1 Control 3 High Register

Name: CCP1CON3H
Offset: 0x276

Bit	15	14	13	12	11	10	9	8
	OETRIG	OSCNT[2:0]				OUTM[2:0]		
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
			POLACE	POLBDF	PSSACE[1:0]		PSSBDF[1:0]	
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit 15 – OETRIG CCP Dead-Time Select bit

Value	Description
1	For Triggered mode (TRIGEN = 1): Module does not drive enabled output pins until triggered
0	Normal output pin operation

Bits 14:12 – OSCNT[2:0] One-Shot Event Count bits

Value	Description
111	Extends one-shot event by 7 time base periods (8 time base periods total)
110	Extends one-shot event by 6 time base periods (7 time base periods total)
101	Extends one-shot event by 5 time base periods (6 time base periods total)
100	Extends one-shot event by 4 time base periods (5 time base periods total)
011	Extends one-shot event by 3 time base periods (4 time base periods total)
010	Extends one-shot event by 2 time base periods (3 time base periods total)
001	Extends one-shot event by 1 time base period (2 time base periods total)
000	Does not extend one-shot trigger event

Bits 10:8 – OUTM[2:0] PWM Output Mode Control bits

Value	Description
111	Reserved
110	Output Scan mode
101	Brush DC Output mode, forward
100	Brush DC Output mode, reverse
011	Reserved
010	Half-Bridge Output mode
001	Push-Pull Output mode
000	Steerable Single Output mode

Bit 5 – POLACE CCP Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit

Value	Description
1	Output pin polarity is active-low
0	Output pin polarity is active-high

Bit 4 – POLBDF CCP Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit

Value	Description
1	Output pin polarity is active-low
0	Output pin polarity is active-high

Bits 3:2 – PSSACE[1:0] PWM Output Pins, OCMxA, OCMxC and OCMxE, Shutdown State Control bits

Value	Description
11	Pins are driven active when a shutdown event occurs

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Value	Description
10	Pins are driven inactive when a shutdown event occurs
0x	Pins are tri-stated when a shutdown event occurs

Bits 1:0 – PSSBDF[1:0] PWM Output Pins, OCMxB, OCMxD and OCMxF, Shutdown State Control bits

Value	Description
11	Pins are driven active when a shutdown event occurs
10	Pins are driven inactive when a shutdown event occurs
0x	Pins are in a high-impedance state when a shutdown event occurs

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14.6.7 CCP1 Status Register Low

Name: CCP1STATL
Offset: 0x278

Legend: C = Clearable bit; W1 = Write '1' Only bit

Bit	15	14	13	12	11	10	9	8
						ICGARM		
Access						W		
Reset						0		

Bit	7	6	5	4	3	2	1	0
	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE
Access	R	W1	W1	R/C	R/C	R/C	R/C	R/C
Reset	0	0	0	0	0	0	0	0

Bit 10 – ICGARM Input Capture Gate Arm bit
A write of '1' to this location will arm the Input Capture x module for a one-shot gating event when ICGSM[1:0] = 01 or 10; read as '0'.

Bit 7 – CCPTRIG CCP Trigger Status bit

Value	Description
1	Timer has been triggered and is running
0	Timer has not been triggered and is held in Reset

Bit 6 – TRSET CCP Trigger Set Request bit
Writes '1' to this location to trigger the timer when TRIGEN = 1 (location always reads as '0').

Bit 5 – TRCLR CCP Trigger Clear Request bit
Writes '1' to this location to cancel the timer trigger when TRIGEN = 1 (location always reads as '0').

Bit 4 – ASEVT CCP Auto-Shutdown Event Status/Control bit

Value	Description
1	A shutdown event is in progress; CCP outputs are in the shutdown state
0	CCP outputs operate normally

Bit 3 – SCEVT Single Edge Compare Event Status bit

Value	Description
1	A single edge compare event has occurred
0	A single edge compare event has not occurred

Bit 2 – ICDIS Input Capture Disable bit

Value	Description
1	Event on input capture pin (ICM1) does not generate a capture event
0	Event on input capture pin will generate a capture event

Bit 1 – ICOV Input Capture Buffer Overflow Status bit

Value	Description
1	The input capture FIFO buffer has overflowed
0	The input capture FIFO buffer has not overflowed

Bit 0 – ICBNE Input Capture Buffer Status bit

Value	Description
1	Input capture buffer has data available
0	Input capture buffer is empty

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14.6.8 CCP1 Time Base Low Register

Name: CCP1TMRL
Offset: 0x27C

Bit	15	14	13	12	11	10	9	8
	TMRL[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TMRL[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TMRL[15:0] CCP1 16-Bit Time Base Value bits

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14.6.9 CCP1 Time Base High Register

Name: CCP1TMRH
Offset: 0x27E

Bit	15	14	13	12	11	10	9	8
	TMRH[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TMRH[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – TMRH[31:24] CCP1 16-Bit Time Base Value bits

Bits 7:0 – TMRH[23:16] CCP1 16-Bit Time Base Value bits

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14.6.10 CCP1 Period Low Register

Name: CCP1PRL
Offset: 0x280

Bit	15	14	13	12	11	10	9	8
	PRL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PRL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PRL[15:0] CCP1 Period Low Register bits

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14.6.11 CCP1 Period High Register

Name: CCP1PRH
Offset: 0x282

Bit	15	14	13	12	11	10	9	8
	PRH[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PRH[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – PRH[31:24] CCP1 Period High Register bits

Bits 7:0 – PRH[23:16] CCP1 Period High Register bits

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14.6.12 CCP1 Primary Compare Register (Timer/Compare Modes Only)

Name: CCP1RA
Offset: 0x284

Bit	15	14	13	12	11	10	9	8
	CMP[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CMP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CMP[15:0] CCP1 Primary Compare Value bits
The 16-bit value to be compared against the CCP time base.

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14.6.13 CCP1 Secondary Compare Register (Timer/Compare Modes Only)

Name: CCP1RB
Offset: 0x288

Bit	15	14	13	12	11	10	9	8
	CMP[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CMP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CMP[15:0] CCP1 Secondary Compare Value bits
The 16-bit value to be compared against the CCP time base.

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14.6.14 CCP1 Capture Buffer Low Register (Capture Modes Only)

Name: CCP1BUFL
Offset: 0x28C

Bit	15	14	13	12	11	10	9	8
	BUF[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BUF[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – BUF[15:0] CCP1 Compare Buffer Value bits
Indicates the oldest captured time base value in the FIFO.

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14.6.15 CCP1 Capture Buffer High Register (Capture Modes Only)

Name: CCP1BUFH
Offset: 0x28E

Bit	15	14	13	12	11	10	9	8
	BUF[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BUF[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – BUF[31:24] CCP1 Compare Buffer Value bits

Bits 7:0 – BUF[23:16] CCP1 Compare Buffer Value bits

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14.6.16 CCP2 Control 1 Low Register

Name: CCP2CON1L
Offset: 0x290

Bit	15	14	13	12	11	10	9	8
	CCPON		CCPSIDL	CCPSLP	TMRSYNC	CLKSEL[2:0]		
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TMRPS[1:0]		T32	CCSEL	MOD[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – CCPON CCP Module Enable bit

Value	Description
1	Module is enabled with an operating mode specified by the MOD[3:0] control bits
0	Module is disabled

Bit 13 – CCPSIDL CCP Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode
0	Continues module operation in Idle mode

Bit 12 – CCPSLP CCP Sleep Mode Enable bit

Value	Description
1	Module continues to operate in Sleep modes
0	Module does not operate in Sleep modes

Bit 11 – TMRSYNC Time Base Clock Synchronization bit

Value	Description
1	Module time base clock is synchronized to the internal system clocks; timing restrictions apply
0	Module time base clock is not synchronized to the internal system clocks

Bits 10:8 – CLKSEL[2:0] CCP Time Base Clock Select bits

Value	Description
111	TCKIA pin
110	TCKIB pin
101	PLL clock
100	2x peripheral clock
011	CLC2
010	SOSC clock
001	Reference clock output
000	Peripheral clock

Bits 7:6 – TMRPS[1:0] Time Base Prescale Select bits

Value	Description
11	1:64 prescaler
10	1:16 prescaler
01	1:4 prescaler
00	1:1 prescaler

Bit 5 – T32 32-Bit Time Base Select bit

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Value	Description
1	Uses 32-bit time base for timer, single edge output compare or input capture function
0	Uses 16-bit time base for timer, single edge output compare or input capture function

Bit 4 – CCSEL Capture/Compare Mode Select bit

Value	Description
1	Input capture peripheral
0	Output Compare/PWM/Timer peripheral (exact function is selected by the MOD[3:0] bits)

Bits 3:0 – MOD[3:0] CCP Mode Select bits

For CCSEL = 1 (Input Capture modes):

Value	Description
1xxx	Reserved
011x	Reserved
0101	Capture every 16th rising edge
0100	Capture every 4th rising edge
0011	Capture every rising and falling edge
0010	Capture every falling edge
0001	Capture every rising edge
0000	Capture every rising and falling edge (Edge Detect mode)

For CCSEL = 0 (Output Compare/Timer modes):

Value	Description
1111	External Input mode: Pulse generator is disabled, source is selected by ICS[2:0]
1110	Reserved
110x	Reserved
10xx	Reserved
0101	Dual Edge Compare mode, buffered
0100	Dual Edge Compare mode
0011	16-Bit/32-Bit Single Edge mode, toggles output on compare match
0010	16-Bit/32-Bit Single Edge mode, drives output low on compare match
0001	16-Bit/32-Bit Single Edge mode, drives output high on compare match
0000	16-Bit/32-Bit Timer mode, output functions are disabled

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14.6.17 CCP2 Control 1 High Register

Name: CCP2CON1H
Offset: 0x292

Notes:

1. This control bit has no function in Input Capture modes.
2. This control bit has no function when TRIGEN = 0.
3. Output postscale settings, from 1:5 to 1:16 (0100-1111), will result in a FIFO buffer overflow for Input Capture modes.

Bit	15	14	13	12	11	10	9	8
	OPSSRC	RTRGEN			OPS3[3:0]			
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRIGEN	ONESHOT	ALTSYNC	SYNC[4:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OPSSRC Output Postscaler Source Select bit(1)

Value	Description
1	Output postscaler scales module trigger output events
0	Output postscaler scales time base interrupt events

Bit 14 – RTRGEN Retrigger Enable bit(2)

Value	Description
1	Time base can be retriggered when TRIGEN bit = 1
0	Time base may not be retriggered when TRIGEN bit = 1

Bits 11:8 – OPS3[3:0] CCP Interrupt Output Postscale Select bits(3)

Value	Description
1111	Interrupt every 16th time base period match
1110	Interrupt every 15th time base period match
. . .	
0100	Interrupt every 5th time base period match
0011	Interrupt every 4th time base period match or 4th input capture event
0010	Interrupt every 3rd time base period match or 3rd input capture event
0001	Interrupt every 2nd time base period match or 2nd input capture event
0000	Interrupt after each time base period match or input capture event

Bit 7 – TRIGEN CCP Trigger Enable bit

Value	Description
1	Trigger operation of time base is enabled
0	Trigger operation of time base is disabled

Bit 6 – ONESHOT One-Shot Trigger Mode Enable bit

Value	Description
1	One-Shot Trigger mode is enabled; trigger duration is set by OSCNT[2:0]
0	One-Shot Trigger mode is disabled

Bit 5 – ALTSYNC CCP Clock Select bit

Value	Description
1	An alternate signal is used as the module synchronization output signal
0	The module synchronization output signal is the Time Base Reset/rollover event

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Bits 4:0 – SYNC[4:0] CCP Synchronization Source Select bits

SYNC[4:0]	Synchronization Source
11111	None; timer with rollover on CCP2PR match or FFFFh
11110	Reserved
11101	Reserved
11100	Reserved
11011	A/D start conversion
11010	CMP3 trigger
11001	CMP2 trigger
11000	CMP1 trigger
10111	Reserved
10110	Reserved
10101	Reserved
10100	Reserved
10011	CLC4 output
10010	CLC3 output
10001	CLC2 output
10000	CLC1 output
01111	Reserved
01101	INT4 pin
01100	INT3 pin
01011	INT2 pin
01010	INT1 pin
01001	INT0 pin
00110	MCCP5 sync output
00101	MCCP4 sync output
00100	MCCP3 sync output
00011	MCCP2 sync output
00010	MCCP1 sync output
00001	MCCPx sync output
00000	MCCP2 timer sync output

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14.6.18 CCP2 Control 2 Low Register

Name: CCP2CON2L
Offset: 0x294

Bit	15	14	13	12	11	10	9	8
	PWMRSEN	ASDGM		SSDG				
Access	R/W	R/W		R/W				
Reset	0	0		0				

Bit	7	6	5	4	3	2	1	0
	ASDG[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – PWMRSEN CCP PWM Restart Enable bit

Value	Description
1	ASEVT bit clears automatically at the beginning of the next PWM period, after the shutdown input has ended
0	ASEVT bit must be cleared in software to resume PWM activity on output pins

Bit 14 – ASDGM CCP Auto-Shutdown Gate Mode Enable bit

Value	Description
1	Waits until next Time Base Reset or rollover for shutdown to occur
0	Shutdown event occurs immediately

Bit 12 – SSDG CCP Software Shutdown/Gate Control bit

Value	Description
1	Manually forces auto-shutdown, timer clock gate or input capture signal gate event (setting of ASDGM bit still applies)
0	Normal module operation

Bits 7:0 – ASDG[7:0] CCP Auto-Shutdown/Gating Source Enable bits

Value	Description
10000000	OCFB
01000000	OCFA
00100000	CLC2
00010000	MCCP1
00001000	MCCP3
00000100	CMP3 out
00000010	CMP2 out
00000001	CMP1 out

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14.6.19 CCP2 Control 2 High Register

Name: CCP2CON2H
Offset: 0x296

Note:
1. OCFEN through OCBEN (bits[13:9]) are implemented in MCCP modules only.

Bit	15	14	13	12	11	10	9	8
	OENSYNC		OC[F:A]EN					
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ICGSM[1:0]			AUXOUT[1:0]		ICS[2:0]		
Access	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Reset	0	0		0	0	0	0	0

Bit 15 – OENSYNC Output Enable Synchronization bit

Value	Description
1	Update by output enable bits occurs on the next Time Base Reset or rollover
0	Update by output enable bits occurs immediately

Bits 13:8 – OC[F:A]EN Output Enable/Steering Control bits(1)

Value	Description
1	OCx pin is controlled by the CCP module and produces an output compare or PWM signal
0	OCx pin is not controlled by the CCP module; the pin is available to the port logic or another peripheral multiplexed on the pin

Bits 7:6 – ICGSM[1:0] Input Capture Gating Source Mode Control bits

Value	Description
11	Reserved
10	One-Shot mode: Falling edge from gating source disables future capture events (ICDIS = 1)
01	One-Shot mode: Rising edge from gating source enables future capture events (ICDIS = 0)
00	Level-Sensitive mode: A high level from gating source will enable future capture events; a low level will disable future capture events

Bits 4:3 – AUXOUT[1:0] Auxiliary Output Signal on Event Selection bits

Value	Description
11	Input capture or output compare event; no signal in Timer mode
10	Signal output depends on module operating mode
01	Time base rollover event (all modes)
00	Disabled

Bits 2:0 – ICS[2:0] Input Capture Source Select bits

Value	Description
111	CLC4
110	CLC3
101	CLC2
100	CLC1
011	Comparator 3
010	Comparator 2
001	Comparator 1
000	Input capture pin (ICM2)

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14.6.20 CCP2 Control 3 Low Register

Name: CCP2CON3L
Offset: 0x298

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				DT[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – DT[4:0] PWM Dead-Time Select bits

Value	Description
111111	Inserts 63 dead-time delay periods between complementary output signals
111110	Inserts 62 dead-time delay periods between complementary output signals
...	
000010	Inserts 2 dead-time delay periods between complementary output signals
000001	Inserts 1 dead-time delay period between complementary output signals
000000	Dead-time logic is disabled

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14.6.21 CCP2 Control 3 High Register

Name: CCP2CON3H
Offset: 0x29A

Bit	15	14	13	12	11	10	9	8
	OETRIG	OSCNT[2:0]				OUTM[2:0]		
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
			POLACE	POLBDF	PSSACE[1:0]		PSSBDF[1:0]	
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit 15 – OETRIG CCP Dead-Time Select bit

Value	Description
1	For Triggered mode (TRIGEN = 1): Module does not drive enabled output pins until triggered
0	Normal output pin operation

Bits 14:12 – OSCNT[2:0] One-Shot Event Count bits

Value	Description
111	Extends one-shot event by 7 time base periods (8 time base periods total)
110	Extends one-shot event by 6 time base periods (7 time base periods total)
101	Extends one-shot event by 5 time base periods (6 time base periods total)
100	Extends one-shot event by 4 time base periods (5 time base periods total)
011	Extends one-shot event by 3 time base periods (4 time base periods total)
010	Extends one-shot event by 2 time base periods (3 time base periods total)
001	Extends one-shot event by 1 time base period (2 time base periods total)
000	Does not extend one-shot trigger event

Bits 10:8 – OUTM[2:0] PWM Output Mode Control bits

Value	Description
111	Reserved
110	Output Scan mode
101	Brush DC Output mode, forward
100	Brush DC Output mode, reverse
011	Reserved
010	Half-Bridge Output mode
001	Push-Pull Output mode
000	Steerable Single Output mode

Bit 5 – POLACE CCP Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit

Value	Description
1	Output pin polarity is active-low
0	Output pin polarity is active-high

Bit 4 – POLBDF CCP Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit

Value	Description
1	Output pin polarity is active-low
0	Output pin polarity is active-high

Bits 3:2 – PSSACE[1:0] PWM Output Pins, OCMxA, OCMxC and OCMxE, Shutdown State Control bits

Value	Description
11	Pins are driven active when a shutdown event occurs

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Value	Description
10	Pins are driven inactive when a shutdown event occurs
0x	Pins are tri-stated when a shutdown event occurs

Bits 1:0 – PSSBDF[1:0] PWM Output Pins, OCMxB, OCMxD and OCMxF, Shutdown State Control bits

Value	Description
11	Pins are driven active when a shutdown event occurs
10	Pins are driven inactive when a shutdown event occurs
0x	Pins are in a high-impedance state when a shutdown event occurs

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14.6.22 CCP2 Status Register Low

Name: CCP2STATL
Offset: 0x29C

Legend: C = Clearable bit; W1 = Write '1' Only bit

Bit	15	14	13	12	11	10	9	8
						ICGARM		
Access						W		
Reset						0		

Bit	7	6	5	4	3	2	1	0
	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE
Access	R	W1	W1	R/C	R/C	R/C	R/C	R/C
Reset	0	0	0	0	0	0	0	0

Bit 10 – ICGARM Input Capture Gate Arm bit
A write of '1' to this location will arm the Input Capture x module for a one-shot gating event when ICGSM[1:0] = 01 or 10; read as '0'.

Bit 7 – CCPTRIG CCP Trigger Status bit

Value	Description
1	Timer has been triggered and is running
0	Timer has not been triggered and is held in Reset

Bit 6 – TRSET CCP Trigger Set Request bit
Writes '1' to this location to trigger the timer when TRIGEN = 1 (location always reads as '0').

Bit 5 – TRCLR CCP Trigger Clear Request bit
Writes '1' to this location to cancel the timer trigger when TRIGEN = 1 (location always reads as '0').

Bit 4 – ASEVT CCP Auto-Shutdown Event Status/Control bit

Value	Description
1	A shutdown event is in progress; CCP outputs are in the shutdown state
0	CCP outputs operate normally

Bit 3 – SCEVT Single Edge Compare Event Status bit

Value	Description
1	A single edge compare event has occurred
0	A single edge compare event has not occurred

Bit 2 – ICDIS Input Capture Disable bit

Value	Description
1	Event on input capture pin (ICM2) does not generate a capture event
0	Event on input capture pin will generate a capture event

Bit 1 – ICOV Input Capture Buffer Overflow Status bit

Value	Description
1	The input capture FIFO buffer has overflowed
0	The input capture FIFO buffer has not overflowed

Bit 0 – ICBNE Input Capture Buffer Status bit

Value	Description
1	Input capture buffer has data available
0	Input capture buffer is empty

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14.6.23 CCP2 Time Base Low Register

Name: CCP2TMRL
Offset: 0x2A0

Bit	15	14	13	12	11	10	9	8
	TMRL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TMRL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TMRL[15:0] CCP2 16-Bit Time Base Value bits

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14.6.24 CCP2 Time Base High Register

Name: CCP2TMRH
Offset: 0x2A2

Bit	15	14	13	12	11	10	9	8
	TMRH[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TMRH[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – TMRH[31:24] CCP2 16-Bit Time Base Value bits

Bits 7:0 – TMRH[23:16] CCP2 16-Bit Time Base Value bits

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14.6.25 CCP2 Period Low Register

Name: CCP2PRL
Offset: 0x2A4

Bit	15	14	13	12	11	10	9	8
	PRL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PRL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PRL[15:0] CCP2 Period Low Register bits

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14.6.26 CCP2 Period High Register

Name: CCP2PRH
Offset: 0x2A6

Bit	15	14	13	12	11	10	9	8
	PRH[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PRH[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – PRH[31:24] CCP2 Period High Register bits

Bits 7:0 – PRH[23:16] CCP2 Period High Register bits

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14.6.27 CCP2 Primary Compare Register (Timer/Compare Modes Only)

Name: CCP2RA
Offset: 0x2A8

Bit	15	14	13	12	11	10	9	8
	CMP[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CMP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CMP[15:0] CCP2 Primary Compare Value bits
The 16-bit value to be compared against the CCP time base.

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14.6.28 CCP2 Secondary Compare Register (Timer/Compare Modes Only)

Name: CCP2RB
Offset: 0x2AC

Bit	15	14	13	12	11	10	9	8
	CMP[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CMP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CMP[15:0] CCP2 Secondary Compare Value bits
The 16-bit value to be compared against the CCP time base.

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14.6.29 CCP3 Capture Buffer Low Register (Capture Modes Only)

Name: CCP3BUFL
Offset: 0x2D4

Bit	15	14	13	12	11	10	9	8
	BUF[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BUF[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – BUF[15:0] CCP3 Compare Buffer Value bits
Indicates the oldest captured time base value in the FIFO.

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14.6.30 CCP3 Capture Buffer High Register (Capture Modes Only)

Name: CCP3BUFH
Offset: 0x2D6

Bit	15	14	13	12	11	10	9	8
	BUF[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BUF[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – BUF[31:24] CCP3 Compare Buffer Value bits

Bits 7:0 – BUF[23:16] CCP3 Compare Buffer Value bits

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14.6.31 CCP3 Control 1 Low Register

Name: CCP3CON1L
Offset: 0x2B4

Bit	15	14	13	12	11	10	9	8
	CCPON		CCPSIDL	CCPSLP	TMRSYNC	CLKSEL[2:0]		
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TMRPS[1:0]		T32	CCSEL	MOD[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – CCPON CCP Module Enable bit

Value	Description
1	Module is enabled with an operating mode specified by the MOD[3:0] control bits
0	Module is disabled

Bit 13 – CCPSIDL CCP Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode
0	Continues module operation in Idle mode

Bit 12 – CCPSLP CCP Sleep Mode Enable bit

Value	Description
1	Module continues to operate in Sleep modes
0	Module does not operate in Sleep modes

Bit 11 – TMRSYNC Time Base Clock Synchronization bit

Value	Description
1	Module time base clock is synchronized to the internal system clocks; timing restrictions apply
0	Module time base clock is not synchronized to the internal system clocks

Bits 10:8 – CLKSEL[2:0] CCP Time Base Clock Select bits

Value	Description
111	TCKIA pin
110	TCKIB pin
101	PLL clock
100	2x peripheral clock
011	CLC3
010	SOSC clock
001	Reference clock output
000	Peripheral clock

Bits 7:6 – TMRPS[1:0] Time Base Prescale Select bits

Value	Description
11	1:64 prescaler
10	1:16 prescaler
01	1:4 prescaler
00	1:1 prescaler

Bit 5 – T32 32-Bit Time Base Select bit

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Value	Description
1	Uses 32-bit time base for timer, single edge output compare or input capture function
0	Uses 16-bit time base for timer, single edge output compare or input capture function

Bit 4 – CCSEL Capture/Compare Mode Select bit

Value	Description
1	Input capture peripheral
0	Output Compare/PWM/Timer peripheral (exact function is selected by the MOD[3:0] bits)

Bits 3:0 – MOD[3:0] CCP Mode Select bits

For CCSEL = 1 (Input Capture modes):

Value	Description
1xxx	Reserved
011x	Reserved
0101	Capture every 16th rising edge
0100	Capture every 4th rising edge
0011	Capture every rising and falling edge
0010	Capture every falling edge
0001	Capture every rising edge
0000	Capture every rising and falling edge (Edge Detect mode)

For CCSEL = 0 (Output Compare/Timer modes):

Value	Description
1111	External Input mode: Pulse generator is disabled, source is selected by ICS[2:0]
1110	Reserved
110x	Reserved
10xx	Reserved
0101	Dual Edge Compare mode, buffered
0100	Dual Edge Compare mode
0011	16-Bit/32-Bit Single Edge mode, toggles output on compare match
0010	16-Bit/32-Bit Single Edge mode, drives output low on compare match
0001	16-Bit/32-Bit Single Edge mode, drives output high on compare match
0000	16-Bit/32-Bit Timer mode, output functions are disabled

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14.6.32 CCP3 Control 1 High Register

Name: CCP3CON1H
Offset: 0x2B6

Notes:

1. This control bit has no function in Input Capture modes.
2. This control bit has no function when TRIGEN = 0.
3. Output postscale settings, from 1:5 to 1:16 (0100-1111), will result in a FIFO buffer overflow for Input Capture modes.

Bit	15	14	13	12	11	10	9	8
	OPSSRC	RTRGEN			OPS3[3:0]			
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRIGEN	ONESHOT	ALTSYNC	SYNC[4:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OPSSRC Output Postscaler Source Select bit(1)

Value	Description
1	Output postscaler scales module trigger output events
0	Output postscaler scales time base interrupt events

Bit 14 – RTRGEN Retrigger Enable bit(2)

Value	Description
1	Time base can be retriggered when TRIGEN bit = 1
0	Time base may not be retriggered when TRIGEN bit = 1

Bits 11:8 – OPS3[3:0] CCP Interrupt Output Postscale Select bits(3)

Value	Description
1111	Interrupt every 16th time base period match
1110	Interrupt every 15th time base period match
. . .	
0100	Interrupt every 5th time base period match
0011	Interrupt every 4th time base period match or 4th input capture event
0010	Interrupt every 3rd time base period match or 3rd input capture event
0001	Interrupt every 2nd time base period match or 2nd input capture event
0000	Interrupt after each time base period match or input capture event

Bit 7 – TRIGEN CCP Trigger Enable bit

Value	Description
1	Trigger operation of time base is enabled
0	Trigger operation of time base is disabled

Bit 6 – ONESHOT One-Shot Trigger Mode Enable bit

Value	Description
1	One-Shot Trigger mode is enabled; trigger duration is set by OSCNT[2:0]
0	One-Shot Trigger mode is disabled

Bit 5 – ALTSYNC CCP Clock Select bit

Value	Description
1	An alternate signal is used as the module synchronization output signal
0	The module synchronization output signal is the Time Base Reset/rollover event

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Bits 4:0 – SYNC[4:0] CCP Synchronization Source Select bits

SYNC[4:0]	Synchronization Source
11111	None; timer with rollover on CCP3PR match or FFFFh
11110	Reserved
11101	Reserved
11100	Reserved
11011	A/D start conversion
11010	CMP3 trigger
11001	CMP2 trigger
11000	CMP1 trigger
10111	Reserved
10110	Reserved
10101	Reserved
10100	Reserved
10011	CLC4 output
10010	CLC3 output
10001	CLC2 output
10000	CLC1 output
01111	Reserved
01101	INT4 pin
01100	INT3 pin
01011	INT2 pin
01010	INT1 pin
01001	INT0 pin
00110	MCCP5 sync output
00101	MCCP4 sync output
00100	MCCP3 sync output
00011	MCCP2 sync output
00010	MCCP1 sync output
00001	MCCPx sync output
00000	MCCP3 timer sync output

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14.6.33 CCP3 Control 2 Low Register

Name: CCP3CON2L
Offset: 0x2B8

Bit	15	14	13	12	11	10	9	8
	PWMRSEN	ASDGM		SSDG				
Access	R/W	R/W		R/W				
Reset	0	0		0				

Bit	7	6	5	4	3	2	1	0
	ASDG[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – PWMRSEN CCP PWM Restart Enable bit

Value	Description
1	ASEVT bit clears automatically at the beginning of the next PWM period, after the shutdown input has ended
0	ASEVT bit must be cleared in software to resume PWM activity on output pins

Bit 14 – ASDGM CCP Auto-Shutdown Gate Mode Enable bit

Value	Description
1	Waits until next Time Base Reset or rollover for shutdown to occur
0	Shutdown event occurs immediately

Bit 12 – SSDG CCP Software Shutdown/Gate Control bit

Value	Description
1	Manually forces auto-shutdown, timer clock gate or input capture signal gate event (setting of ASDGM bit still applies)
0	Normal module operation

Bits 7:0 – ASDG[7:0] CCP Auto-Shutdown/Gating Source Enable bits

Value	Description
10000000	OCFB
01000000	OCFA
00100000	CLC3
00010000	MCCP1
00001000	MCCP4
00000100	CMP3 out
00000010	CMP2 out
00000001	CMP1 out

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14.6.34 CCP3 Control 2 High Register

Name: CCP3CON2H
Offset: 0x2BA

Bit	15	14	13	12	11	10	9	8
	OENSYNC		OC[F:A]EN					
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ICGSM[1:0]			AUXOUT[1:0]		ICS[2:0]		
Access	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Reset	0	0		0	0	0	0	0

Bit 15 – OENSYNC Output Enable Synchronization bit

Value	Description
1	Update by output enable bits occurs on the next Time Base Reset or rollover
0	Update by output enable bits occurs immediately

Bits 13:8 – OC[F:A]EN Output Enable/Steering Control bits

Value	Description
1	OCx pin is controlled by the CCP module and produces an output compare or PWM signal
0	OCx pin is not controlled by the CCP module; the pin is available to the port logic or another peripheral multiplexed on the pin

Bits 7:6 – ICGSM[1:0] Input Capture Gating Source Mode Control bits

Value	Description
11	Reserved
10	One-Shot mode: Falling edge from gating source disables future capture events (ICDIS = 1)
01	One-Shot mode: Rising edge from gating source enables future capture events (ICDIS = 0)
00	Level-Sensitive mode: A high level from gating source will enable future capture events; a low level will disable future capture events

Bits 4:3 – AUXOUT[1:0] Auxiliary Output Signal on Event Selection bits

Value	Description
11	Input capture or output compare event; no signal in Timer mode
10	Signal output depends on module operating mode
01	Time base rollover event (all modes)
00	Disabled

Bits 2:0 – ICS[2:0] Input Capture Source Select bits

Value	Description
111	CLC4
110	CLC3
101	CLC2
100	CLC1
011	Comparator 3
010	Comparator 2
001	Comparator 1
000	Input capture pin (ICM3)

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14.6.35 CCP3 Control 3 Low Register

Name: CCP3CON3L
Offset: 0x2BC

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				DT[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – DT[4:0] PWM Dead-Time Select bits

Value	Description
111111	Inserts 63 dead-time delay periods between complementary output signals
111110	Inserts 62 dead-time delay periods between complementary output signals
...	
000010	Inserts 2 dead-time delay periods between complementary output signals
000001	Inserts 1 dead-time delay period between complementary output signals
000000	Dead-time logic is disabled

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14.6.36 CCP3 Control 3 High Register

Name: CCP3CON3H
Offset: 0x2BE

Bit	15	14	13	12	11	10	9	8
	OETRIG	OSCNT[2:0]				OUTM[2:0]		
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
			POLACE	POLBDF	PSSACE[1:0]		PSSBDF[1:0]	
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit 15 – OETRIG CCP Dead-Time Select bit

Value	Description
1	For Triggered mode (TRIGEN = 1): Module does not drive enabled output pins until triggered
0	Normal output pin operation

Bits 14:12 – OSCNT[2:0] One-Shot Event Count bits

Value	Description
111	Extends one-shot event by 7 time base periods (8 time base periods total)
110	Extends one-shot event by 6 time base periods (7 time base periods total)
101	Extends one-shot event by 5 time base periods (6 time base periods total)
100	Extends one-shot event by 4 time base periods (5 time base periods total)
011	Extends one-shot event by 3 time base periods (4 time base periods total)
010	Extends one-shot event by 2 time base periods (3 time base periods total)
001	Extends one-shot event by 1 time base period (2 time base periods total)
000	Does not extend one-shot trigger event

Bits 10:8 – OUTM[2:0] PWM Output Mode Control bits

Value	Description
111	Reserved
110	Output Scan mode
101	Brush DC Output mode, forward
100	Brush DC Output mode, reverse
011	Reserved
010	Half-Bridge Output mode
001	Push-Pull Output mode
000	Steerable Single Output mode

Bit 5 – POLACE CCP Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit

Value	Description
1	Output pin polarity is active-low
0	Output pin polarity is active-high

Bit 4 – POLBDF CCP Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit

Value	Description
1	Output pin polarity is active-low
0	Output pin polarity is active-high

Bits 3:2 – PSSACE[1:0] PWM Output Pins, OCMxA, OCMxC and OCMxE, Shutdown State Control bits

Value	Description
11	Pins are driven active when a shutdown event occurs

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Value	Description
10	Pins are driven inactive when a shutdown event occurs
0x	Pins are tri-stated when a shutdown event occurs

Bits 1:0 – PSSBDF[1:0] PWM Output Pins, OCMxB, OCMxD and OCMxF, Shutdown State Control bits

Value	Description
11	Pins are driven active when a shutdown event occurs
10	Pins are driven inactive when a shutdown event occurs
0x	Pins are in a high-impedance state when a shutdown event occurs

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14.6.37 CCP3 Status Register Low

Name: CCP3STATL
Offset: 0x2C0

Legend: C = Clearable bit; W1 = Write '1' Only bit

Bit	15	14	13	12	11	10	9	8
						ICGARM		
Access						W		
Reset						0		

Bit	7	6	5	4	3	2	1	0
	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE
Access	R	W1	W1	R/C	R/C	R/C	R/C	R/C
Reset	0	0	0	0	0	0	0	0

Bit 10 – ICGARM Input Capture Gate Arm bit
A write of '1' to this location will arm the Input Capture x module for a one-shot gating event when ICGSM[1:0] = 01 or 10; read as '0'.

Bit 7 – CCPTRIG CCP Trigger Status bit

Value	Description
1	Timer has been triggered and is running
0	Timer has not been triggered and is held in Reset

Bit 6 – TRSET CCP Trigger Set Request bit
Writes '1' to this location to trigger the timer when TRIGEN = 1 (location always reads as '0').

Bit 5 – TRCLR CCP Trigger Clear Request bit
Writes '1' to this location to cancel the timer trigger when TRIGEN = 1 (location always reads as '0').

Bit 4 – ASEVT CCP Auto-Shutdown Event Status/Control bit

Value	Description
1	A shutdown event is in progress; CCP outputs are in the shutdown state
0	CCP outputs operate normally

Bit 3 – SCEVT Single Edge Compare Event Status bit

Value	Description
1	A single edge compare event has occurred
0	A single edge compare event has not occurred

Bit 2 – ICDIS Input Capture Disable bit

Value	Description
1	Event on input capture pin (ICM3) does not generate a capture event
0	Event on input capture pin will generate a capture event

Bit 1 – ICOV Input Capture Buffer Overflow Status bit

Value	Description
1	The input capture FIFO buffer has overflowed
0	The input capture FIFO buffer has not overflowed

Bit 0 – ICBNE Input Capture Buffer Status bit

Value	Description
1	Input capture buffer has data available
0	Input capture buffer is empty

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14.6.38 CCP3 Time Base Low Register

Name: CCP3TMRL
Offset: 0x2C4

Bit	15	14	13	12	11	10	9	8
	TMRL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TMRL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TMRL[15:0] CCP3 16-Bit Time Base Value bits

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14.6.39 CCP3 Time Base High Register

Name: CCP3TMRH
Offset: 0x2C6

Bit	15	14	13	12	11	10	9	8
	TMRH[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TMRH[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – TMRH[31:24] CCP3 16-Bit Time Base Value bits

Bits 7:0 – TMRH[23:16] CCP3 16-Bit Time Base Value bits

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14.6.40 CCP3 Period Low Register

Name: CCP3PRL
Offset: 0x2C8

Bit	15	14	13	12	11	10	9	8
	PRL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PRL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PRL[15:0] CCP3 Period Low Register bits

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14.6.41 CCP3 Period High Register

Name: CCP3PRH
Offset: 0x2CA

Bit	15	14	13	12	11	10	9	8
	PRH[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PRH[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – PRH[31:24] CCP3 Period High Register bits

Bits 7:0 – PRH[23:16] CCP3 Period High Register bits

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14.6.42 CCP3 Primary Compare Register (Timer/Compare Modes Only)

Name: CCP3RA
Offset: 0x2CC

Bit	15	14	13	12	11	10	9	8
	CMP[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CMP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CMP[15:0] CCP3 Primary Compare Value bits
The 16-bit value to be compared against the CCP time base.

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14.6.43 CCP3 Secondary Compare Register (Timer/Compare Modes Only)

Name: CCP3RB
Offset: 0x2D0

Bit	15	14	13	12	11	10	9	8
	CMP[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CMP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CMP[15:0] CCP3 Secondary Compare Value bits
The 16-bit value to be compared against the CCP time base.

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14.6.44 CCP4 Control 1 Low Register

Name: CCP4CON1L
Offset: 0x300

Bit	15	14	13	12	11	10	9	8
	CCPON		CCPSIDL	CCPSLP	TMRSYNC	CLKSEL[2:0]		
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TMRPS[1:0]		T32	CCSEL	MOD[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – CCPON CCP Module Enable bit

Value	Description
1	Module is enabled with an operating mode specified by the MOD[3:0] control bits
0	Module is disabled

Bit 13 – CCPSIDL CCP Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode
0	Continues module operation in Idle mode

Bit 12 – CCPSLP CCP Sleep Mode Enable bit

Value	Description
1	Module continues to operate in Sleep modes
0	Module does not operate in Sleep modes

Bit 11 – TMRSYNC Time Base Clock Synchronization bit

Value	Description
1	Module time base clock is synchronized to the internal system clocks; timing restrictions apply
0	Module time base clock is not synchronized to the internal system clocks

Bits 10:8 – CLKSEL[2:0] CCP Time Base Clock Select bits

Value	Description
111	TCKIA pin
110	TCKIB pin
101	PLL clock
100	2x peripheral clock
011	CLC4
010	SOSC clock
001	Reference clock output
000	Peripheral clock

Bits 7:6 – TMRPS[1:0] Time Base Prescale Select bits

Value	Description
11	1:64 prescaler
10	1:16 prescaler
01	1:4 prescaler
00	1:1 prescaler

Bit 5 – T32 32-Bit Time Base Select bit

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Value	Description
1	Uses 32-bit time base for timer, single edge output compare or input capture function
0	Uses 16-bit time base for timer, single edge output compare or input capture function

Bit 4 – CCSEL Capture/Compare Mode Select bit

Value	Description
1	Input capture peripheral
0	Output Compare/PWM/Timer peripheral (exact function is selected by the MOD[3:0] bits)

Bits 3:0 – MOD[3:0] CCP Mode Select bits

For CCSEL = 1 (Input Capture modes):

Value	Description
1xxx	Reserved
011x	Reserved
0101	Capture every 16th rising edge
0100	Capture every 4th rising edge
0011	Capture every rising and falling edge
0010	Capture every falling edge
0001	Capture every rising edge
0000	Capture every rising and falling edge (Edge Detect mode)

For CCSEL = 0 (Output Compare/Timer modes):

Value	Description
1111	External Input mode: Pulse generator is disabled, source is selected by ICS[2:0]
1110	Reserved
110x	Reserved
10xx	Reserved
0111	Reserved
0110	Reserved
0101	Dual Edge Compare mode, buffered
0100	Dual Edge Compare mode
0011	16-Bit/32-Bit Single Edge mode, toggles output on compare match
0010	16-Bit/32-Bit Single Edge mode, drives output low on compare match
0001	16-Bit/32-Bit Single Edge mode, drives output high on compare match
0000	16-Bit/32-Bit Timer mode, output functions are disabled

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14.6.45 CCP4 Control 1 High Register

Name: CCP4CON1H
Offset: 0x302

Notes:

1. This control bit has no function in Input Capture modes.
2. This control bit has no function when TRIGEN = 0.
3. Output postscale settings, from 1:5 to 1:16 (0100-1111), will result in a FIFO buffer overflow for Input Capture modes.

Bit	15	14	13	12	11	10	9	8
	OPSSRC	RTRGEN			OPS3[3:0]			
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRIGEN	ONESHOT	ALTSYNC	SYNC[4:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OPSSRC Output Postscaler Source Select bit(1)

Value	Description
1	Output postscaler scales module trigger output events
0	Output postscaler scales time base interrupt events

Bit 14 – RTRGEN Retrigger Enable bit(2)

Value	Description
1	Time base can be retriggered when TRIGEN bit = 1
0	Time base may not be retriggered when TRIGEN bit = 1

Bits 11:8 – OPS3[3:0] CCP Interrupt Output Postscale Select bits(3)

Value	Description
1111	Interrupt every 16th time base period match
1110	Interrupt every 15th time base period match
. . .	
0100	Interrupt every 5th time base period match
0011	Interrupt every 4th time base period match or 4th input capture event
0010	Interrupt every 3rd time base period match or 3rd input capture event
0001	Interrupt every 2nd time base period match or 2nd input capture event
0000	Interrupt after each time base period match or input capture event

Bit 7 – TRIGEN CCP Trigger Enable bit

Value	Description
1	Trigger operation of time base is enabled
0	Trigger operation of time base is disabled

Bit 6 – ONESHOT One-Shot Trigger Mode Enable bit

Value	Description
1	One-Shot Trigger mode is enabled; trigger duration is set by OSCNT[2:0]
0	One-Shot Trigger mode is disabled

Bit 5 – ALTSYNC CCP Clock Select bit

Value	Description
1	An alternate signal is used as the module synchronization output signal
0	The module synchronization output signal is the Time Base Reset/rollover event

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Bits 4:0 – SYNC[4:0] CCP Synchronization Source Select bits

SYNC[4:0]	Synchronization Source
11111	None; timer with rollover on CCP4PR match or FFFFh
11110	Reserved
11101	Reserved
11100	Reserved
11011	A/D start conversion
11010	CMP3 trigger
11001	CMP2 trigger
11000	CMP1 trigger
10111	Reserved
10110	Reserved
10101	Reserved
10100	Reserved
10011	CLC4 output
10010	CLC3 output
10001	CLC2 output
10000	CLC1 output
01111	Reserved
01101	INT4 pin
01100	INT3 pin
01011	INT2 pin
01010	INT1 pin
01001	INT0 pin
00110	MCCP5 sync output
00101	MCCP4 sync output
00100	MCCP3 sync output
00011	MCCP2 sync output
00010	MCCP1 sync output
00001	MCCPx sync output
00000	MCCP4 timer sync output

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14.6.46 CCP4 Control 2 Low Register

Name: CCP4CON2L
Offset: 0x304

Bit	15	14	13	12	11	10	9	8
	PWMRSEN	ASDGM		SSDG				
Access	R/W	R/W		R/W				
Reset	0	0		0				

Bit	7	6	5	4	3	2	1	0
	ASDG[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – PWMRSEN CCP PWM Restart Enable bit

Value	Description
1	ASEVT bit clears automatically at the beginning of the next PWM period, after the shutdown input has ended
0	ASEVT bit must be cleared in software to resume PWM activity on output pins

Bit 14 – ASDGM CCP Auto-Shutdown Gate Mode Enable bit

Value	Description
1	Waits until the next Time Base Reset or rollover for shutdown to occur
0	Shutdown event occurs immediately

Bit 12 – SSDG CCP Software Shutdown/Gate Control bit

Value	Description
1	Manually forces auto-shutdown, timer clock gate or input capture signal gate event (setting of ASDGM bit still applies)
0	Normal module operation

Bits 7:0 – ASDG[7:0] CCP Auto-Shutdown/Gating Source Enable bits

Value	Description
10000000	OCFB
01000000	OCFA
00100000	CLC4
00010000	MCCP1
00001000	MCCP5
00000100	CMP3 out
00000010	CMP2 out
00000001	CMP1 out

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14.6.47 CCP4 Control 2 High Register

Name: CCP4CON2H
Offset: 0x306

Bit	15	14	13	12	11	10	9	8
	OENSYNC		OC[F:A]EN					
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ICGSM[1:0]			AUXOUT[1:0]		ICS[2:0]		
Access	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Reset	0	0		0	0	0	0	0

Bit 15 – OENSYNC Output Enable Synchronization bit

Value	Description
1	Update by output enable bits occurs on the next Time Base Reset or rollover
0	Update by output enable bits occurs immediately

Bits 13:8 – OC[F:A]EN Output Enable/Steering Control bits

Value	Description
1	OCx pin is controlled by the CCPx module and produces an output compare or PWM signal
0	OCx pin is not controlled by the CCPx module; the pin is available to the port logic or another peripheral multiplexed on the pin

Bits 7:6 – ICGSM[1:0] Input Capture Gating Source Mode Control bits

Value	Description
11	Reserved
10	One-Shot mode: Falling edge from gating source disables future capture events (ICDIS = 1)
01	One-Shot mode: Rising edge from gating source enables future capture events (ICDIS = 0)
00	Level-Sensitive mode: A high level from gating source will enable future capture events; a low level will disable future capture events

Bits 4:3 – AUXOUT[1:0] Auxiliary Output Signal on Event Selection bits

Value	Description
11	Input capture or output compare event; no signal in Timer mode
10	Signal output depends on module operating mode
01	Time base rollover event (all modes)
00	Disabled

Bits 2:0 – ICS[2:0] Input Capture Source Select bits

Value	Description
111	CLC4
110	CLC3
101	CLC2
100	CLC1
011	Comparator 3
010	Comparator 2
001	Comparator 1
000	Input capture pin (ICM4)

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14.6.48 CCP4 Control 3 Low Register

Name: CCP4CON3L
Offset: 0x308

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				DT[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – DT[4:0] PWM Dead-Time Select bits

Value	Description
111111	Inserts 63 dead-time delay periods between complementary output signals
111110	Inserts 62 dead-time delay periods between complementary output signals
...	
000010	Inserts 2 dead-time delay periods between complementary output signals
000001	Inserts 1 dead-time delay period between complementary output signals
000000	Dead-time logic is disabled

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14.6.49 CCP4 Control 3 High Register

Name: CCP4CON3H
Offset: 0x30A

Bit	15	14	13	12	11	10	9	8
	OETRIG	OSCNT[2:0]				OUTM[2:0]		
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
			POLACE	POLBDF	PSSACE[1:0]		PSSBDF[1:0]	
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit 15 – OETRIG CCP Dead-Time Select bit

Value	Description
1	For Triggered mode (TRIGEN = 1): Module does not drive enabled output pins until triggered
0	Normal output pin operation

Bits 14:12 – OSCNT[2:0] One-Shot Event Count bits

Value	Description
111	Extends one-shot event by 7 time base periods (8 time base periods total)
110	Extends one-shot event by 6 time base periods (7 time base periods total)
101	Extends one-shot event by 5 time base periods (6 time base periods total)
100	Extends one-shot event by 4 time base periods (5 time base periods total)
011	Extends one-shot event by 3 time base periods (4 time base periods total)
010	Extends one-shot event by 2 time base periods (3 time base periods total)
001	Extends one-shot event by 1 time base period (2 time base periods total)
000	Does not extend one-shot trigger event

Bits 10:8 – OUTM[2:0] PWM Output Mode Control bits

Value	Description
111	Reserved
110	Output Scan mode
101	Brush DC Output mode, forward
100	Brush DC Output mode, reverse
011	Reserved
010	Half-Bridge Output mode
001	Push-Pull Output mode
000	Steerable Single Output mode

Bit 5 – POLACE CCP Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit

Value	Description
1	Output pin polarity is active-low
0	Output pin polarity is active-high

Bit 4 – POLBDF CCP Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit

Value	Description
1	Output pin polarity is active-low
0	Output pin polarity is active-high

Bits 3:2 – PSSACE[1:0] PWM Output Pins, OCMxA, OCMxC and OCMxE, Shutdown State Control bits

Value	Description
11	Pins are driven active when a shutdown event occurs

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Value	Description
10	Pins are driven inactive when a shutdown event occurs
0x	Pins are tri-stated when a shutdown event occurs

Bits 1:0 – PSSBDF[1:0] PWM Output Pins, OCMxB, OCMxD and OCMxF, Shutdown State Control bits

Value	Description
11	Pins are driven active when a shutdown event occurs
10	Pins are driven inactive when a shutdown event occurs
0x	Pins are in a high-impedance state when a shutdown event occurs

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14.6.50 CCP4 Status Register Low

Name: CCP4STATL
Offset: 0x30C

Legend: C = Clearable bit; W1 = Write '1' Only bit

Bit	15	14	13	12	11	10	9	8
						ICGARM		
Access						W		
Reset						0		

Bit	7	6	5	4	3	2	1	0
	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE
Access	R	W1	W1	R/C	R/C	R/C	R/C	R/C
Reset	0	0	0	0	0	0	0	0

Bit 10 – ICGARM Input Capture Gate Arm bit
A write of '1' to this location will arm the input capture module for a one-shot gating event when ICGSM[1:0] = 01 or 10; read as '0'.

Bit 7 – CCPTRIG CCP Trigger Status bit

Value	Description
1	Timer has been triggered and is running
0	Timer has not been triggered and is held in Reset

Bit 6 – TRSET CCP Trigger Set Request bit
Writes '1' to this location to trigger the timer when TRIGEN = 1 (location always reads as '0').

Bit 5 – TRCLR CCP Trigger Clear Request bit
Writes '1' to this location to cancel the timer trigger when TRIGEN = 1 (location always reads as '0').

Bit 4 – ASEVT CCP Auto-Shutdown Event Status/Control bit

Value	Description
1	A shutdown event is in progress; CCP outputs are in the shutdown state
0	CCP outputs operate normally

Bit 3 – SCEVT Single Edge Compare Event Status bit

Value	Description
1	A single edge compare event has occurred
0	A single edge compare event has not occurred

Bit 2 – ICDIS Input Capture Disable bit

Value	Description
1	Event on input capture pin (ICM4) does not generate a capture event
0	Event on input capture pin will generate a capture event

Bit 1 – ICOV Input Capture Buffer Overflow Status bit

Value	Description
1	The input capture FIFO buffer has overflowed
0	The input capture FIFO buffer has not overflowed

Bit 0 – ICBNE Input Capture Buffer Status bit

Value	Description
1	Input capture buffer has data available
0	Input capture buffer is empty

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14.6.51 CCP4 Time Base Low Register

Name: CCP4TMRL
Offset: 0x310

Bit	15	14	13	12	11	10	9	8
	TMRL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TMRL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TMRL[15:0] CCP4 16-Bit Time Base Value bits

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14.6.52 CCP4 Time Base High Register

Name: CCP4TMRH
Offset: 0x312

Bit	15	14	13	12	11	10	9	8
	TMRH[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TMRH[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – TMRH[31:24] CCP4 16-Bit Time Base Value bits

Bits 7:0 – TMRH[23:16] CCP4 16-Bit Time Base Value bits

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14.6.53 CCP4 Period Low Register

Name: CCP4PRL
Offset: 0x314

Bit	15	14	13	12	11	10	9	8
	PRL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PRL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PRL[15:0] CCP4 Period Low Register bits

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14.6.54 CCP4 Period High Register

Name: CCP4PRH
Offset: 0x316

Bit	15	14	13	12	11	10	9	8
	PRH[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PRH[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – PRH[31:24] CCP4 Period High Register bits

Bits 7:0 – PRH[23:16] CCP4 Period High Register bits

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14.6.55 CCP4 Primary Compare Register (Timer/Compare Modes Only)

Name: CCP4RA
Offset: 0x318

Bit	15	14	13	12	11	10	9	8
	CMP[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CMP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CMP[15:0] CCP4 Primary Compare Value bits
The 16-bit value to be compared against the CCP time base.

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14.6.56 CCP4 Secondary Compare Register (Timer/Compare Modes Only)

Name: CCP4RB
Offset: 0x31C

Bit	15	14	13	12	11	10	9	8
	CMP[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CMP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CMP[15:0] CCP4 Secondary Compare Value bits
The 16-bit value to be compared against the CCP time base.

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14.6.57 CCP4 Capture Buffer Low Register (Capture Modes Only)

Name: CCP4BUFL
Offset: 0x320

Bit	15	14	13	12	11	10	9	8
	BUF[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BUF[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – BUF[15:0] CCP4 Compare Buffer Value bits
Indicates the oldest captured time base value in the FIFO.

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14.6.58 CCP4 Capture Buffer High Register (Capture Modes Only)

Name: CCP4BUFH
Offset: 0x322

Bit	15	14	13	12	11	10	9	8
	BUF[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BUF[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – BUF[31:24] CCP4 Compare Buffer Value bits

Bits 7:0 – BUF[23:16] CCP4 Compare Buffer Value bits

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14.6.59 CCP5 Control 1 Low Register

Name: CCP5CON1L
Offset: 0x324

Bit	15	14	13	12	11	10	9	8
	CCPON		CCPSIDL	CCPSLP	TMRSYNC	CLKSEL[2:0]		
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TMRPS[1:0]		T32	CCSEL	MOD[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – CCPON CCP Module Enable bit

Value	Description
1	Module is enabled with an operating mode specified by the MOD[3:0] control bits
0	Module is disabled

Bit 13 – CCPSIDL CCP Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode
0	Continues module operation in Idle mode

Bit 12 – CCPSLP CCP Sleep Mode Enable bit

Value	Description
1	Module continues to operate in Sleep modes
0	Module does not operate in Sleep modes

Bit 11 – TMRSYNC Time Base Clock Synchronization bit

Value	Description
1	Module time base clock is synchronized to the internal system clocks; timing restrictions apply
0	Module time base clock is not synchronized to the internal system clocks

Bits 10:8 – CLKSEL[2:0] CCP Time Base Clock Select bits

Value	Description
111	TCKIA pin
110	TCKIB pin
101	PLL clock
100	2x peripheral clock
011	CLC1
010	SOSC clock
001	Reference clock output
000	Peripheral clock

Bits 7:6 – TMRPS[1:0] Time Base Prescale Select bits

Value	Description
11	1:64 prescaler
10	1:16 prescaler
01	1:4 prescaler
00	1:1 prescaler

Bit 5 – T32 32-Bit Time Base Select bit

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Value	Description
1	Uses 32-bit time base for timer, single edge output compare or input capture function
0	Uses 16-bit time base for timer, single edge output compare or input capture function

Bit 4 – CCSEL Capture/Compare Mode Select bit

Value	Description
1	Input capture peripheral
0	Output Compare/PWM/Timer peripheral (exact function is selected by the MOD[3:0] bits)

Bits 3:0 – MOD[3:0] CCP Mode Select bits

For CCSEL = 1 (Input Capture modes):

Value	Description
1xxx	Reserved
011x	Reserved
0101	Capture every 16th rising edge
0100	Capture every 4th rising edge
0011	Capture every rising and falling edge
0010	Capture every falling edge
0001	Capture every rising edge
0000	Capture every rising and falling edge (Edge Detect mode)

For CCSEL = 0 (Output Compare/Timer modes):

Value	Description
1111	External Input mode: Pulse generator is disabled, source is selected by ICS[2:0]
1110	Reserved
110x	Reserved
10xx	Reserved
0111	Reserved
0110	Reserved
0101	Dual Edge Compare mode, buffered
0100	Dual Edge Compare mode
0011	16-Bit/32-Bit Single Edge mode, toggles output on compare match
0010	16-Bit/32-Bit Single Edge mode, drives output low on compare match
0001	16-Bit/32-Bit Single Edge mode, drives output high on compare match
0000	16-Bit/32-Bit Timer mode, output functions are disabled

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14.6.60 CCP5 Control 1 High Register

Name: CCP5CON1H
Offset: 0x326

Notes:

1. This control bit has no function in Input Capture modes.
2. This control bit has no function when TRIGEN = 0.
3. Output postscale settings, from 1:5 to 1:16 (0100-1111), will result in a FIFO buffer overflow for Input Capture modes.

Bit	15	14	13	12	11	10	9	8
	OPSSRC	RTRGEN			OPS3[3:0]			
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRIGEN	ONESHOT	ALTSYNC	SYNC[4:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OPSSRC Output Postscaler Source Select bit(1)

Value	Description
1	Output postscaler scales module trigger output events
0	Output postscaler scales time base interrupt events

Bit 14 – RTRGEN Retrigger Enable bit(2)

Value	Description
1	Time base can be retriggered when TRIGEN bit = 1
0	Time base may not be retriggered when TRIGEN bit = 1

Bits 11:8 – OPS3[3:0] CCP Interrupt Output Postscale Select bits(3)

Value	Description
1111	Interrupt every 16th time base period match
1110	Interrupt every 15th time base period match
. . .	
0100	Interrupt every 5th time base period match
0011	Interrupt every 4th time base period match or 4th input capture event
0010	Interrupt every 3rd time base period match or 3rd input capture event
0001	Interrupt every 2nd time base period match or 2nd input capture event
0000	Interrupt after each time base period match or input capture event

Bit 7 – TRIGEN CCP Trigger Enable bit

Value	Description
1	Trigger operation of time base is enabled
0	Trigger operation of time base is disabled

Bit 6 – ONESHOT One-Shot Trigger Mode Enable bit

Value	Description
1	One-Shot Trigger mode is enabled; trigger duration is set by OSCNT[2:0]
0	One-Shot Trigger mode is disabled

Bit 5 – ALTSYNC CCP Clock Select bit

Value	Description
1	An alternate signal is used as the module synchronization output signal
0	The module synchronization output signal is the Time Base Reset/rollover event

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Bits 4:0 – SYNC[4:0] CCP Synchronization Source Select bits

SYNC[4:0]	Synchronization Source
11111	None; timer with rollover on CCP5PR match or FFFFh
11110	Reserved
11101	Reserved
11100	Reserved
11011	A/D start conversion
11010	CMP3 trigger
11001	CMP2 trigger
11000	CMP1 trigger
10111	Reserved
10110	Reserved
10101	Reserved
10100	Reserved
10011	CLC4 output
10010	CLC3 output
10001	CLC2 output
10000	CLC1 output
01111	Reserved
01101	INT4 pin
01100	INT3 pin
01011	INT2 pin
01010	INT1 pin
01001	INT0 pin
00110	MCCP5 sync output
00101	MCCP4 sync output
00100	MCCP3 sync output
00011	MCCP2 sync output
00010	MCCP1 sync output
00001	MCCPx sync output
00000	MCCP5 timer sync output

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14.6.61 CCP5 Control 2 Low Register

Name: CCP5CON2L
Offset: 0x328

Bit	15	14	13	12	11	10	9	8
	PWMRSEN	ASDGM		SSDG				
Access	R/W	R/W		R/W				
Reset	0	0		0				

Bit	7	6	5	4	3	2	1	0
	ASDG[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – PWMRSEN CCP PWM Restart Enable bit

Value	Description
1	ASEVT bit clears automatically at the beginning of the next PWM period, after the shutdown input has ended
0	ASEVT bit must be cleared in software to resume PWM activity on output pins

Bit 14 – ASDGM CCP Auto-Shutdown Gate Mode Enable bit

Value	Description
1	Waits until the next Time Base Reset or rollover for shutdown to occur
0	Shutdown event occurs immediately

Bit 12 – SSDG CCP Software Shutdown/Gate Control bit

Value	Description
1	Manually forces auto-shutdown, timer clock gate or input capture signal gate event (setting of ASDGM bit still applies)
0	Normal module operation

Bits 7:0 – ASDG[7:0] CCP Auto-Shutdown/Gating Source Enable bits

Value	Description
10000000	OCFB
01000000	OCFA
00100000	CLC1
00010000	MCCP1
00001000	MCCP2
00000100	CMP3 out
00000010	CMP2 out
00000001	CMP1 out

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14.6.62 CCP5 Control 2 High Register

Name: CCP5CON2H
Offset: 0x32A

Bit	15	14	13	12	11	10	9	8
	OENSYNC		OC[F:A]EN					
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ICGSM[1:0]			AUXOUT[1:0]		ICS[2:0]		
Access	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Reset	0	0		0	0	0	0	0

Bit 15 – OENSYNC Output Enable Synchronization bit

Value	Description
1	Update by output enable bits occurs on the next Time Base Reset or rollover
0	Update by output enable bits occurs immediately

Bits 13:8 – OC[F:A]EN Output Enable/Steering Control bits

Value	Description
1	OCx pin is controlled by the CCPx module and produces an output compare or PWM signal
0	OCx pin is not controlled by the CCPx module; the pin is available to the port logic or another peripheral multiplexed on the pin

Bits 7:6 – ICGSM[1:0] Input Capture Gating Source Mode Control bits

Value	Description
11	Reserved
10	One-Shot mode: Falling edge from gating source disables future capture events (ICDIS = 1)
01	One-Shot mode: Rising edge from gating source enables future capture events (ICDIS = 0)
00	Level-Sensitive mode: A high level from gating source will enable future capture events; a low level will disable future capture events

Bits 4:3 – AUXOUT[1:0] Auxiliary Output Signal on Event Selection bits

Value	Description
11	Input capture or output compare event; no signal in Timer mode
10	Signal output depends on module operating mode
01	Time base rollover event (all modes)
00	Disabled

Bits 2:0 – ICS[2:0] Input Capture Source Select bits

Value	Description
111	CLC4
110	CLC3
101	CLC2
100	CLC1
011	Comparator 3
010	Comparator 2
001	Comparator 1
000	Input capture pin (ICM5)

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14.6.63 CCP5 Control 3 Low Register

Name: CCP5CON3L
Offset: 0x32C

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				DT[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – DT[4:0] PWM Dead-Time Select bits

Value	Description
111111	Inserts 63 dead-time delay periods between complementary output signals
111110	Inserts 62 dead-time delay periods between complementary output signals
...	
000010	Inserts 2 dead-time delay periods between complementary output signals
000001	Inserts 1 dead-time delay period between complementary output signals
000000	Dead-time logic is disabled

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14.6.64 CCP5 Control 3 High Register

Name: CCP5CON3H
Offset: 0x32E

Bit	15	14	13	12	11	10	9	8
	OETRIG	OSCNT[2:0]				OUTM[2:0]		
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
			POLACE	POLBDF	PSSACE[1:0]		PSSBDF[1:0]	
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit 15 – OETRIG CCP Dead-Time Select bit

Value	Description
1	For Triggered mode (TRIGEN = 1): Module does not drive enabled output pins until triggered
0	Normal output pin operation

Bits 14:12 – OSCNT[2:0] One-Shot Event Count bits

Value	Description
111	Extends one-shot event by 7 time base periods (8 time base periods total)
110	Extends one-shot event by 6 time base periods (7 time base periods total)
101	Extends one-shot event by 5 time base periods (6 time base periods total)
100	Extends one-shot event by 4 time base periods (5 time base periods total)
011	Extends one-shot event by 3 time base periods (4 time base periods total)
010	Extends one-shot event by 2 time base periods (3 time base periods total)
001	Extends one-shot event by 1 time base period (2 time base periods total)
000	Does not extend one-shot trigger event

Bits 10:8 – OUTM[2:0] PWM Output Mode Control bits

Value	Description
111	Reserved
110	Output Scan mode
101	Brush DC Output mode, forward
100	Brush DC Output mode, reverse
011	Reserved
010	Half-Bridge Output mode
001	Push-Pull Output mode
000	Steerable Single Output mode

Bit 5 – POLACE CCP Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit

Value	Description
1	Output pin polarity is active-low
0	Output pin polarity is active-high

Bit 4 – POLBDF CCP Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit

Value	Description
1	Output pin polarity is active-low
0	Output pin polarity is active-high

Bits 3:2 – PSSACE[1:0] PWM Output Pins, OCMxA, OCMxC and OCMxE, Shutdown State Control bits

Value	Description
11	Pins are driven active when a shutdown event occurs

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Value	Description
10	Pins are driven inactive when a shutdown event occurs
0x	Pins are tri-stated when a shutdown event occurs

Bits 1:0 – PSSBDF[1:0] PWM Output Pins, OCMxB, OCMxD and OCMxF, Shutdown State Control bits

Value	Description
11	Pins are driven active when a shutdown event occurs
10	Pins are driven inactive when a shutdown event occurs
0x	Pins are in a high-impedance state when a shutdown event occurs

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14.6.65 CCP5 Status Register Low

Name: CCP5STATL
Offset: 0x330

Legend: C = Clearable bit; W1 = Write '1' Only bit

Bit	15	14	13	12	11	10	9	8
						ICGARM		
Access						W		
Reset						0		

Bit	7	6	5	4	3	2	1	0
	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE
Access	R	W1	W1	R/C	R/C	R/C	R/C	R/C
Reset	0	0	0	0	0	0	0	0

Bit 10 – ICGARM Input Capture Gate Arm bit
A write of '1' to this location will arm the Input Capture x module for a one-shot gating event when ICGSM[1:0] = 01 or 10; read as '0'.

Bit 7 – CCPTRIG CCP Trigger Status bit

Value	Description
1	Timer has been triggered and is running
0	Timer has not been triggered and is held in Reset

Bit 6 – TRSET CCP Trigger Set Request bit
Writes '1' to this location to trigger the timer when TRIGEN = 1 (location always reads as '0').

Bit 5 – TRCLR CCP Trigger Clear Request bit
Writes '1' to this location to cancel the timer trigger when TRIGEN = 1 (location always reads as '0').

Bit 4 – ASEVT CCP Auto-Shutdown Event Status/Control bit

Value	Description
1	A shutdown event is in progress; CCP outputs are in the shutdown state
0	CCP outputs operate normally

Bit 3 – SCEVT Single Edge Compare Event Status bit

Value	Description
1	A single edge compare event has occurred
0	A single edge compare event has not occurred

Bit 2 – ICDIS Input Capture Disable bit

Value	Description
1	Event on input capture pin (ICM5) does not generate a capture event
0	Event on input capture pin will generate a capture event

Bit 1 – ICOV Input Capture Buffer Overflow Status bit

Value	Description
1	The input capture FIFO buffer has overflowed
0	The input capture FIFO buffer has not overflowed

Bit 0 – ICBNE Input Capture Buffer Status bit

Value	Description
1	Input capture buffer has data available
0	Input capture buffer is empty

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14.6.66 CCP5 Time Base Low Register

Name: CCP5TMRL
Offset: 0x334

Bit	15	14	13	12	11	10	9	8
	TMRL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TMRL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TMRL[15:0] CCP5 16-Bit Time Base Value bits

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14.6.67 CCP5 Time Base High Register

Name: CCP5TMRH
Offset: 0x336

Bit	15	14	13	12	11	10	9	8
	TMRH[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TMRH[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – TMRH[31:24] CCP5 16-Bit Time Base Value bits

Bits 7:0 – TMRH[23:16] CCP5 16-Bit Time Base Value bits

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14.6.68 CCP5 Period Low Register

Name: CCP5PRL
Offset: 0x338

Bit	15	14	13	12	11	10	9	8
	PRL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PRL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PRL[15:0] CCP5 Period Low Register bits

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14.6.69 CCP5 Period High Register

Name: CCP5PRH
Offset: 0x33A

Bit	15	14	13	12	11	10	9	8
	PRH[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PRH[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – PRH[31:24] CCP5 Period High Register bits

Bits 7:0 – PRH[23:16] CCP5 Period High Register bits

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14.6.70 CCP5 Primary Compare Register (Timer/Compare Modes Only)

Name: CCP5RA
Offset: 0x33C

Bit	15	14	13	12	11	10	9	8
	CMP[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CMP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CMP[15:0] CCP5 Primary Compare Value bits
The 16-bit value to be compared against the CCP time base.

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14.6.71 CCP5 Secondary Compare Register (Timer/Compare Modes Only)

Name: CCP5RB
Offset: 0x340

Bit	15	14	13	12	11	10	9	8
	CMP[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CMP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CMP[15:0] CCP5 Secondary Compare Value bits
The 16-bit value to be compared against the CCP time base.

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14.6.72 CCP5 Capture Buffer Low Register (Capture Modes Only)

Name: CCP5BUFL
Offset: 0x344

Bit	15	14	13	12	11	10	9	8
	BUF[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BUF[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – BUF[15:0] CCP5 Compare Buffer Value bits
Indicates the oldest captured time base value in the FIFO.

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14.6.73 CCP5 Capture Buffer High Register (Capture Modes Only)

Name: CCP5BUFH
Offset: 0x346

Bit	15	14	13	12	11	10	9	8
	BUF[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BUF[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – BUF[31:24] CCP5 Compare Buffer Value bits

Bits 7:0 – BUF[23:16] CCP5 Compare Buffer Value bits

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15. Serial Peripheral Interface (SPI)

Note: This data sheet summarizes the features of the PIC24FJ64GP205/GU205 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Serial Peripheral Interface (SPI) with Audio Codec Support"** (www.microchip.com/DS70005136) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

The Serial Peripheral Interface (SPI) module is a synchronous serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D Converters, etc. The SPI module is compatible with the Motorola® SPI and SIOP interfaces. All devices in the PIC24FJ64GP205/GU205 family include two SPI modules.

The module supports operation in two buffer modes. In Standard Buffer mode, data are shifted through a single serial buffer. In Enhanced Buffer mode, data are shifted through a FIFO buffer. The FIFO level depends on the configured mode.

Note: FIFO depth for this device is 32 (in 8-Bit Data mode).

Variable length data can be transmitted and received from 2 to 32 bits.

Note: Do not perform Read-Modify-Write operations (such as bit-oriented instructions) on the SPIxBUF register in either Standard or Enhanced Buffer mode.

The module also supports a basic framed SPI protocol while operating in either Host or Client mode. A total of four framed SPI configurations are supported.

The module also supports Audio modes. Four different Audio modes are available:

- I^2S mode
- Left Justified mode
- Right Justified mode
- PCM/DSP mode

In each of these modes, the serial clock is free-running and audio data are always transferred.

If an audio protocol data transfer takes place between two devices, then usually one device is the Host and the other is the Client. However, audio data can be transferred between two Clients. Because the audio protocols require free-running clocks, the Host can be a third party controller. In either case, the Host generates two free-running clocks: SCKx and LRC (Left, Right Channel Clock is available on the $\overline{SSx}$/FSYNCx pin).

The SPI serial interface consists of four pins:

- SDIx: Serial Data Input
- SDOx: Serial Data Output
- SCKx: Shift Clock Input or Output
- $\overline{SSx}$: Active-Low Client Select or Frame Synchronization I/O Pulse

The SPI module can be configured to operate using two, three or four pins. In the 3-pin mode, $\overline{SSx}$ is not used. In the 2-pin mode, both SDOx and $\overline{SSx}$ are not used.

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The SPI module has the ability to generate three interrupts reflecting the events that occur during the data communication. The following types of interrupts can be generated:

1. Receive interrupts are signaled by SPIxRXIF. This event occurs when:
   – RX watermark interrupt
   – SPIROV = 1
   – SPIRBF = 1
   – SPIRBE = 1

   provided the respective mask bits are enabled in SPIxIMSKL/H.
2. Transmit interrupts are signaled by SPIxTXIF. This event occurs when:
   – TX watermark interrupt
   – SPITUR = 1
   – SPITBF = 1
   – SPITBE = 1

   provided the respective mask bits are enabled in SPIxIMSKL/H.
3. General interrupts are signaled by SPIxIF. This event occurs when:
   – FRMERR = 1
   – SPIBUSY = 1
   – SRMT = 1

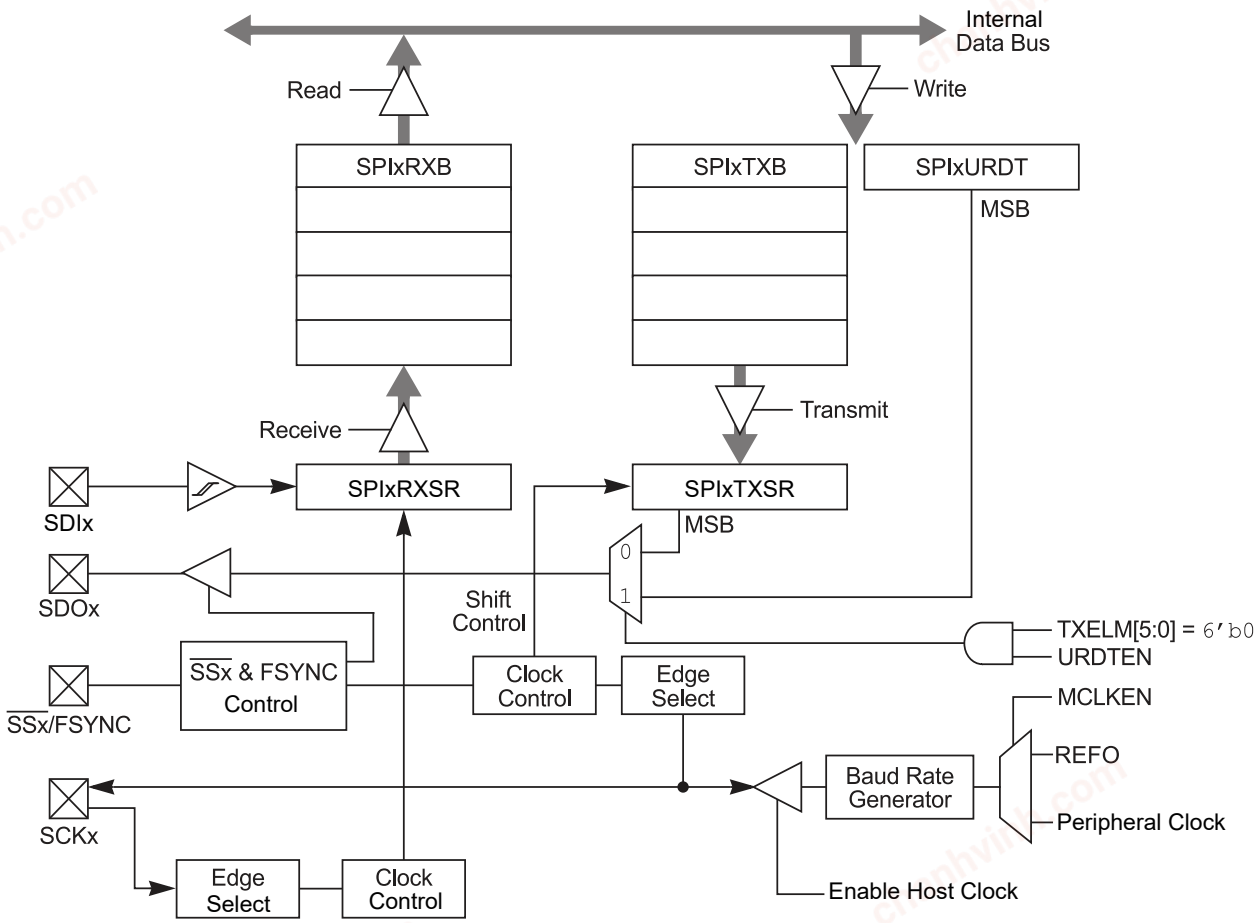
   provided the respective mask bits are enabled in SPIxIMSKL/H.

A block diagram of the module in Enhanced Buffer mode is shown in Figure 15-1.

Note: In this section, the SPI modules are referred to together as SPIx, or separately as SPI1 or SPI2. Special Function Registers will follow a similar notation. For example, SPIxCON1 and SPIxCON2 refer to the control registers for either of the two SPI modules.

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Figure 15-1. SPI Module Block Diagram (Enhanced Mode)



15.1 Host Mode Operation

Perform the following steps to set up the SPIx module for Host mode operation:

1. Disable the SPIx interrupts in the respective IECx register.
2. Stop and reset the SPIx module by clearing the SPIEN bit.
3. Clear the receive buffer.
4. Clear the ENHBUF bit (SPIxCON1L[0]) if using Standard Buffer mode or set the bit if using Enhanced Buffer mode.
5. Clear the SPIx interrupt flags/events in the respective IFSx register.
6. Write the SPIx interrupt priority and sub-priority bits in the respective IPCx register.
7. Set the SPIx interrupt enable bits in the respective IECx register.
8. Write the Baud Rate register, SPIxBRGL.
9. Clear the SPIROV bit (SPIxSTATL[6]).
10. Write the desired settings to the SPIxCON1L register with MSTEN (SPIxCON1L[5]) = 1.
11. Enable SPI operation by setting the SPIEN bit (SPIxCON1L[15]).
12. Write the data to be transmitted to the SPIxBUFL and SPIxBUFH registers. Transmission (and reception) will start as soon as data are written to the SPIxBUFL/H registers.

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15.2 Client Mode Operation

The following steps are used to set up the SPIx module for the Client mode of operation:

1. If using interrupts, disable the SPIx interrupts in the respective IECx register.
2. Stop and reset the SPIx module by clearing the SPIEN bit.
3. Clear the receive buffer.
4. Clear the ENHBUF bit (SPIxCON1L[0]) if using Standard Buffer mode or set the bit if using Enhanced Buffer mode.
5. Clear the SPIx interrupt flags/events in the respective IFSx register.
6. Write the SPIx interrupt priority and sub-priority bits in the respective IPCx register.
7. Set the SPIx interrupt enable bits in the respective IECx register.
8. Clear the SPIROV bit (SPIxSTATL[6]).
9. Write the desired settings to the SPIxCON1L register with MSTEN (SPIxCON1L[5]) = 0.
10. Enable SPI operation by setting the SPIEN bit (SPIxCON1L[15]).

Transmission (and reception) will start as soon as the Host provides the serial clock.

The following additional features are provided in Client mode:

- Client Select Synchronization:
  The $\overline{SSx}$ pin allows a Synchronous Client mode. If the SSEN bit (SPIxCON1L[7]) is set, transmission and reception are enabled in Client mode only if the $\overline{SSx}$ pin is driven to a low state. The port output, or other peripheral outputs, must not be driven in order to allow the $\overline{SSx}$ pin to function as an input. If the SSEN bit is set and the $\overline{SSx}$ pin is driven high, the SDOx pin is no longer driven and will tri-state, even if the module is in the middle of a transmission. An aborted transmission will be tried again the next time the $\overline{SSx}$ pin is driven low using the data held in the SPIxTXB register. If the SSEN bit is not set, the $\overline{SSx}$ pin does not affect the module operation in Client mode.
- SPITBE Status Flag Operation:
  The SPITBE bit (SPIxSTATL[3]) has a different function in the Client mode of operation. The following describes the function of SPITBE for various settings of the Client mode of operation:
  - If SSEN (SPIxCON1L[7]) is cleared, the SPITBE bit is cleared when SPIxBUF is loaded by the user code. It is set when the module transfers SPIxTXB to SPIxTXSR.
    This is similar to the SPITBE bit function in Host mode.
  - If SSEN is set, SPITBE is cleared when SPIxBUF is loaded by the user code. However, it is set only when the SPIx module completes data transmission. A transmission will be aborted when the $\overline{SSx}$ pin goes high and may be retried at a later time. So, each data word is held in SPIxTXB until all bits are transmitted to the receiver.

15.3 Audio Mode Operation

To initialize the SPIx module for Audio mode, follow the steps to initialize it for Host/Client mode, but also set the AUDEN bit (SPIxCON1H[15]).

In Host+Audio mode:

- This mode enables the device to generate SCKx and LRC pulses as long as the SPIEN bit (SPIxCON1L[15]) = 1.
- The SPIx module generates LRC and SCKx continuously in all cases, regardless of the transmit data, while in Host mode.
- The SPIx module drives the leading edge of LRC and SCKx within one SCKx period, and the serial data shift in and out continuously, even when the TX FIFO is empty.

In Client+Audio mode:

- This mode enables the device to receive SCKx and LRC pulses as long as the SPIEN bit (SPIxCON1L[15]) = 1.
- The SPIx module drives zeros out of SDOx, but does not shift data out or in (SDIx) until the module receives the LRC (i.e., the edge that precedes the left channel).

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- Once the module receives the leading edge of LRC, it starts receiving data if DISSDI (SPIxCON1L[4]) = 0 and the serial data shift out continuously, even when the TX FIFO is empty.

15.4 Relationship Between Device and SPI Clock Speed

Equation 15-1. Relationship Between Device and SPI Clock Speed

$$\text{Baud Rate} = \frac{F_{PB}}{(2 * (SPIxBRG + 1))}$$

Where: F_{PB} is the Peripheral Bus Clock Frequency.

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15.5 SPI Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x03F3	Reserved									
0x03F4	SPI1CON1L	7:0	SSEN	CKP	MSTEN	DISSDI	DISSCK	MCLKEN	SPIFE	ENHBUF
		15:8	SPIEN		SPISIDL	DISSDO	MODE[1:0]		SMP	CKE
0x03F6	SPI1CON1H	7:0	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT[2:0]		
		15:8	AUDEN	SPISGNEXT	IGNROV	IGNTUR	AUDMONO	URDTEN	AUDMOD[1:0]	
0x03F8	SPI1CON2L	7:0	WLENGTH[4:0]							
		15:8								
0x03FA ... 0x03FB	Reserved									
0x03FC	SPI1STATL	7:0	SRMT	SPIROV	SPIRBE		SPITBE		SPITBF	SPIRBF
		15:8				FRMERR	SPIBUSY			SPITUR
0x03FE	SPI1STATH	7:0	TXELM[5:0]							
		15:8	RXELM[5:0]							
0x0400	SPI1BUFL	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
0x0402	SPI1BUFH	7:0	DATA[23:16]							
		15:8	DATA[31:24]							
0x0404	SPI1BRGL	7:0	BRG[7:0]							
		15:8	BRG[12:8]							
0x0406 ... 0x0407	Reserved									
0x0408	SPI1IMSKL	7:0	SRMTEN	SPIROVEN	SPIRBEN		SPITBEN		SPITBFEN	SPIRBFEN
		15:8				FRMERREN	BUSYEN			SPITUREN
0x040A	SPI1IMSKH	7:0	TXWIEN		TXMSK[5:0]					
		15:8	RXWIEN		RXMSK[5:0]					
0x040C	SPI1URDTL	7:0	URDATA[7:0]							
		15:8	URDATA[15:8]							
0x040E	SPI1URDTH	7:0	URDATA[23:16]							
		15:8	URDATA[31:24]							
0x0410	SPI2CON1L	7:0	SSEN	CKP	MSTEN	DISSDI	DISSCK	MCLKEN	SPIFE	ENHBUF
		15:8	SPIEN		SPISIDL	DISSDO	MODE[1:0]		SMP	CKE
0x0412	SPI2CON1H	7:0	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT[2:0]		
		15:8	AUDEN	SPISGNEXT	IGNROV	IGNTUR	AUDMONO	URDTEN	AUDMOD[1:0]	
0x0414	SPI2CON2L	7:0	WLENGTH[4:0]							
		15:8								
0x0416 ... 0x0417	Reserved									
0x0418	SPI2STATL	7:0	SRMT	SPIROV	SPIRBE		SPITBE		SPITBF	SPIRBF
		15:8				FRMERR	SPIBUSY			SPITUR
0x041A	SPI2STATH	7:0	TXELM[5:0]							
		15:8	RXELM[5:0]							
0x041C	SPI2BUFL	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
0x041E	SPI2BUFH	7:0	DATA[23:16]							
		15:8	DATA[31:24]							
0x0420	SPI2BRGL	7:0	BRG[7:0]							
		15:8	BRG[12:8]							
0x0422 ... 0x0423	Reserved									

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.....continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0424	SPI2IMSKL	7:0	SRMTEN	SPIROVEN	SPIRBEN		SPITBEN		SPITBFEN	SPIRBFEN
		15:8				FRMERREN	BUSYEN			SPITUREN
0x0426	SPI2IMSKH	7:0	TXWIEN		TXMSK[5:0]					
		15:8	RXWIEN		RXMSK[5:0]					
0x0428	SPI2URDTL	7:0	URDATA[7:0]							
		15:8	URDATA[15:8]							
0x042A	SPI2URDTH	7:0	URDATA[23:16]							
		15:8	URDATA[31:24]							

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15.5.1 SPI1 Control Register 1 Low

Name: SPI1CON1L
Offset: 0x3F4

Note:

1. When AUDEN = 1, this module functions as if CKE = 0, regardless of its actual value.
2. When FRMEN = 1, SSEN is not used.
3. MCLKEN can only be written when the SPIEN bit = 0.
4. This channel is not meaningful for DSP/PCM mode as LRC follows the FRMSYPW bit.

Bit	15	14	13	12	11	10	9	8
	SPIEN		SPISIDL	DISSDO	MODE[1:0]		SMP	CKE
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SSEN	CKP	MSTEN	DISSDI	DISSCK	MCLKEN	SPIFE	ENHBUF
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – SPIEN SPI On bit

Value	Description
1	Enables module
0	Turns off and resets module, disables clocks, disables interrupt event generation, allows SFR modifications

Bit 13 – SPISIDL SPI Stop in Idle Mode bit

Value	Description
1	Halts in CPU Idle mode
0	Continues to operate in CPU Idle mode

Bit 12 – DISSDO Disable SDOx Output Port bit

Value	Description
1	SDOx pin is not used by the module; pin is controlled by the port function
0	SDOx pin is controlled by the module

Bits 11:10 – MODE[1:0] Serial Word Length bits(1,4)

AUDEN = 0:			
MODE32	MODE16	COMMUNICATION	FIFO DEPTH
1	x	32-Bit	8
0	1	16-Bit	16
0	0	8-Bit	32
AUDEN = 1:			
MODE32	MODE16	COMMUNICATION	
1	1	24-Bit Data, 32-Bit FIFO, 32-Bit Channel/64-Bit Frame	
1	0	32-Bit Data, 32-Bit FIFO, 32-Bit Channel/64-Bit Frame	
0	1	16-Bit Data, 16-Bit FIFO, 32-Bit Channel/64-Bit Frame	
0	0	16-Bit Data, 16-Bit FIFO, 16-Bit Channel/32-Bit Frame	

Bit 9 – SMP SPI Data Input Sample Phase bit
Client Mode:
Input data are always sampled at the middle of data output time, regardless of the SMP setting.
Host Mode:

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Value	Description
1	Input data are sampled at the end of data output time
0	Input data are sampled at the middle of data output time

Bit 8 – CKE SPI Clock Edge Select bit(1)

Value	Description
1	Transmit happens on transition from active clock state to Idle clock state
0	Transmit happens on transition from Idle clock state to active clock state

Bit 7 – SSEN Client Select Enable bit (Client mode)(2)

Value	Description
1	$\overline{SSx}$ pin is used by the macro in Client mode; $\overline{SSx}$ pin is used as the Client select input
0	$\overline{SSx}$ pin is not used by the macro ($\overline{SSx}$ pin will be controlled by the port I/O)

Bit 6 – CKP SPI Clock Polarity Select bit

Value	Description
1	Idle state for clock is a high level; active state is a low level
0	Idle state for clock is a low level; active state is a high level

Bit 5 – MSTEN Host Mode Enable bit

Value	Description
1	Host mode
0	Client mode

Bit 4 – DISSDI Disable SDIx Input Port bit

Value	Description
1	SDIx pin is not used by the module; pin is controlled by the port function
0	SDIx pin is controlled by the module

Bit 3 – DISSCK Disable SCKx Output Port bit

Value	Description
1	SCKx pin is not used by the module; pin is controlled by the port function
0	SCKx pin is controlled by the module

Bit 2 – MCLKEN Host Clock Enable bit(3)

Value	Description
1	Reference Clock Output (REFO) is used by the BRG
0	Peripheral clock is used by the BRG

Bit 1 – SPIFE Frame Sync Pulse Edge Select bit

Value	Description
1	Frame Sync pulse (Idle-to-active edge) coincides with the first bit clock
0	Frame Sync pulse (Idle-to-active edge) precedes the first bit clock

Bit 0 – ENHBUF Enhanced Buffer Mode Enable bit

Value	Description
1	Enhanced Buffer mode is enabled
0	Enhanced Buffer mode is disabled

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15.5.2 SPI1 Control Register 1 High

Name: SPI1CON1H
Offset: 0x3F6

Note:

1. AUDEN can only be written when the SPIEN bit = 0.
2. AUDMONO can only be written when the SPIEN bit = 0 and is only valid for AUDEN = 1.
3. URDTEN is only valid when IGNTUR = 1.
4. AUDMOD[1:0] bits can only be written when the SPIEN bit = 0 and are only valid when AUDEN = 1. When NOT in PCM/DSP mode, this module functions as if FRMSYPW = 1, regardless of its actual value.

Bit	15	14	13	12	11	10	9	8
	AUDEN	SPISGNEXT	IGNROV	IGNTUR	AUDMONO	URDTEN	AUDMOD[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – AUDEN Audio Codec Support Enable bit(1)

Value	Description
1	Audio protocol is enabled; MSTEN controls the direction of both the SCKx and frame (a.k.a. LRC), and this module functions as if FRMEN = 1, FRMSYNC = MSTEN, FRMCNT[2:0] = 001 and SMP = 0, regardless of their actual values
0	Audio protocol is disabled

Bit 14 – SPISGNEXT SPI Sign-Extend RX FIFO Read Data Enable bit

Value	Description
1	Data from RX FIFO are sign-extended
0	Data from RX FIFO are not sign-extended

Bit 13 – IGNROV Ignore Receive Overflow bit

Value	Description
1	A Receive Overflow (ROV) is NOT a critical error; during ROV, data in the FIFO are not overwritten by the receive data
0	A ROV is a critical error that stops SPI operation

Bit 12 – IGNTUR Ignore Transmit Underrun bit

Value	Description
1	A Transmit Underrun (TUR) is NOT a critical error and data indicated by URDTEN are transmitted until the SPI1TXB is not empty
0	A TUR is a critical error that stops SPI operation

Bit 11 – AUDMONO Audio Data Format Transmit bit(2)

Value	Description
1	Audio data are mono (i.e., each data word is transmitted on both left and right channels)
0	Audio data are stereo

Bit 10 – URDTEN Transmit Underrun Data Enable bit(3)

Value	Description
1	Transmits data out of SPI1URDTL/H register during Transmit Underrun conditions
0	Transmits the last received data during Transmit Underrun conditions

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Bits 9:8 – AUDMOD[1:0] Audio Protocol Mode Selection bits(4)

Value	Description
11	PCM/DSP mode
10	Right Justified mode: This module functions as if SPIFE = 1, regardless of its actual value
01	Left Justified mode: This module functions as if SPIFE = 1, regardless of its actual value
00	I^2S mode: This module functions as if SPIFE = 0, regardless of its actual value

Bit 7 – FRMEN Framed SPI Support bit

Value	Description
1	Framed SPI support is enabled ($\overline{SSx}$ pin is used as the FSYNC input/output)
0	Framed SPI support is disabled

Bit 6 – FRMSYNC Frame Sync Pulse Direction Control bit

Value	Description
1	Frame Sync pulse input (Client)
0	Frame Sync pulse output (Host)

Bit 5 – FRMPOL Frame Sync/Client Select Polarity bit

Value	Description
1	Frame Sync pulse/Client select is active-high
0	Frame Sync pulse/Client select is active-low

Bit 4 – MSSEN Host Mode Client Select Enable bit

Value	Description
1	SPI Client select support is enabled with polarity determined by FRMPOL ($\overline{SSx}$ pin is automatically driven during transmission in Host mode)
0	SPI Client select support is disabled ($\overline{SSx}$ pin will be controlled by port I/O)

Bit 3 – FRMSYPW Frame Sync Pulse-Width bit

Value	Description
1	Frame Sync pulse is one serial word length wide (as defined by MODE[32,16]/WLENGTH[4:0] bits)
0	Frame Sync pulse is one clock (SCKx) wide

Bits 2:0 – FRMCNT[2:0] Frame Sync Pulse Counter bits
Controls the number of serial words transmitted per Sync pulse.

Value	Description
111	Reserved
110	Reserved
101	Generates a Frame Sync pulse on every 32 serial words
100	Generates a Frame Sync pulse on every 16 serial words
011	Generates a Frame Sync pulse on every 8 serial words
010	Generates a Frame Sync pulse on every 4 serial words
001	Generates a Frame Sync pulse on every 2 serial words (value used by audio protocols)
000	Generates a Frame Sync pulse on each serial word

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15.5.3 SPI1 Control Register 2 Low

Name: SPI1CON2L
Offset: 0x3F8

Note:

1. These bits are effective when AUDEN = 0 only.
2. Varying the length by changing these bits does not affect the depth of the TX/RX FIFO.

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				WLENGTH[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – WLENGTH[4:0] Variable Word Length bits(1,2)

Value	Description
11111	32-bit data
11110	31-bit data
11101	30-bit data
11100	29-bit data
11011	28-bit data
11010	27-bit data
11001	26-bit data
11000	25-bit data
10111	24-bit data
10110	23-bit data
10101	22-bit data
10100	21-bit data
10011	20-bit data
10010	19-bit data
10001	18-bit data
10000	17-bit data
01111	16-bit data
01110	15-bit data
01101	14-bit data
01100	13-bit data
01011	12-bit data
01010	11-bit data
01001	10-bit data
01000	9-bit data
00111	8-bit data
00110	7-bit data
00101	6-bit data
00100	5-bit data
00011	4-bit data
00010	3-bit data
00001	2-bit data
00000	See MODE[32,16] bits in SPI1CON1L[11:10]

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15.5.4 SPI1 Status Register Low

Name: SPI1STATL
Offset: 0x3FC

Note:

1. SPITUR is cleared when SPIEN = 0. When IGNTUR = 1, SPITUR provides dynamic status of the Transmit Underrun condition, but does not stop RX/TX operation and does not need to be cleared by software.

Legend: C = Clearable bit; HS = Hardware Settable bit; HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
				FRMERR	SPIBUSY			SPITUR
Access				HS/R/C	HSC			HS/R/C
Reset				0	0			0

Bit	7	6	5	4	3	2	1	0
	SRMT	SPIROV	SPIRBE		SPITBE		SPITBF	SPIRBF
Access	HSC	HSC	HSC		HSC		HSC	HSC
Reset	0	0	0		0		0	0

Bit 12 – FRMERR SPI Frame Error Status bit

Value	Description
1	Frame error is detected
0	No frame error is detected

Bit 11 – SPIBUSY SPI Activity Status bit

Value	Description
1	Module is currently busy with some transactions
0	No ongoing transactions (at time of read)

Bit 8 – SPITUR SPI Transmit Underrun Status bit(1)

Value	Description
1	Transmit buffer has encountered a Transmit Underrun condition
0	Transmit buffer does not have a Transmit Underrun condition

Bit 7 – SRMT Shift Register Empty Status bit

Value	Description
1	No current or pending transactions (i.e., neither SPI1TXB or SPI1TXSR contains data to transmit)
0	Current or pending transactions

Bit 6 – SPIROV SPI Receive Overflow Status bit

Value	Description
1	A new byte/half-word/word has been completely received when the SPI1RXB is full
0	No overflow

Bit 5 – SPIRBE SPI RX Buffer Empty Status bit
Standard Buffer Mode:
Automatically set in hardware when SPI1BUF is read from, reading SPI1RXB. Automatically cleared in hardware when SPI transfers data from SPI1RXSR to SPI1RXB.
Enhanced Buffer Mode:
Indicates RXELM[5:0] = 000000.

Value	Description
1	RX buffer is empty
0	RX buffer is not empty

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Bit 3 – SPITBE SPI Transmit Buffer Empty Status bit
Standard Buffer Mode:
Automatically set in hardware when SPI1 transfers data from SPI1TXB to SPI1TXSR. Automatically cleared in hardware when SPI1BUF is written, loading SPI1TXB.
Enhanced Buffer Mode:
Indicates TXELM[5:0] = 000000.

Value	Description
1	SPI1TXB is empty
0	SPI1TXB is not empty

Bit 1 – SPITBF SPI Transmit Buffer Full Status bit
Standard Buffer Mode:
Automatically set in hardware when SPI1BUF is written, loading SPI1TXB. Automatically cleared in hardware when SPI transfers data from SPI1TXB to SPI1TXSR.
Enhanced Buffer Mode:
Indicates TXELM[5:0] = 111111.

Value	Description
1	SPI1TXB is full
0	SPI1TXB not full

Bit 0 – SPIRBF SPI Receive Buffer Full Status bit
Standard Buffer Mode:
Automatically set in hardware when SPI transfers data from SPI1RXSR to SPI1RXB. Automatically cleared in hardware when SPI1BUF is read from, reading SPI1RXB.
Enhanced Buffer Mode:
Indicates RXELM[5:0] = 111111.

Value	Description
1	SDIx pin is not used by the module; pin is controlled by the port function
0	SDIx pin is controlled by the module

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15.5.5 SPI1 Status Register High

Name: SPI1STATH
Offset: 0x3FE

Legend: C = Clearable bit; HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
			RXELM[5:0]					
Access			HSC/R/C	HSC/R/C	HSC/R/C	HSC/R/C	HSC/R/C	HSC/R/C
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			TXELM[5:0]					
Access			HSC/R/C	HSC/R/C	HSC/R/C	HSC/R/C	HSC/R/C	HSC/R/C
Reset			0	0	0	0	0	0

Bits 13:8 – RXELM[5:0] Receive Buffer Element Count bits (valid in Enhanced Buffer mode)

Bits 5:0 – TXELM[5:0] Transmit Buffer Element Count bits (valid in Enhanced Buffer mode)

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15.5.6 SPI1 Buffer Register Low

Name: SPI1BUFL
Offset: 0x400

Bit	15	14	13	12	11	10	9	8
	DATA[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DATA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – DATA[15:0] SPI FIFO Data bits
When the MODE[32,16] or WLENGTH[4:0] bits select 16 to 9-bit data, the SPI only uses DATA[15:0].
When the MODE[32,16] or WLENGTH[4:0] bits select 8 to 2-bit data, the SPI only uses DATA[7:0].

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15.5.7 SPI1 Buffer Register High

Name: SPI1BUFH
Offset: 0x402

Bit	15	14	13	12	11	10	9	8
	DATA[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DATA[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – DATA[31:24] SPI FIFO Data bits

Bits 7:0 – DATA[23:16] SPI FIFO Data bits

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15.5.8 SPI1 Baud Rate Generator Register Low

Name: SPI1BRGL
Offset: 0x404

Note:
1. Changing the BRG value when SPIEN = 1 causes undefined behavior.

Bit	15	14	13	12	11	10	9	8
				BRG[12:8]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BRG[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 12:0 – BRG[12:0] SPI Baud Rate Generator Divisor bits(1)

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15.5.9 SPI1 Interrupt Mask Register Low

Name: SPI1IMSKL
Offset: 0x408

Legend: C = Clearable bit

Bit	15	14	13	12	11	10	9	8
				FRMERREN	BUSYEN			SPITUREN
Access				R/W	R/W			R/C
Reset				0	0			0

Bit	7	6	5	4	3	2	1	0
	SRMTEN	SPIROVEN	SPIRBEN		SPITBEN		SPITBFEN	SPIRBFEN
Access	R/W	R/W	R/W		R/W		R/W	R/W
Reset	0	0	0		0		0	0

Bit 12 – FRMERREN Enable Interrupt Events via FRMERR bit

Value	Description
1	Frame error generates an interrupt event
0	Frame error does not generate an interrupt event

Bit 11 – BUSYEN Enable Interrupt Events via SPIBUSY bit

Value	Description
1	SPIBUSY generates an interrupt event
0	SPIBUSY does not generate an interrupt event

Bit 8 – SPITUREN Enable Interrupt Events via SPITUR bit

Value	Description
1	Transmit Underrun (TUR) generates an interrupt event
0	Transmit Underrun does not generate an interrupt event

Bit 7 – SRMTEN Enable Interrupt Events via SRMT bit

Value	Description
1	Shift Register Empty (SRMT) generates interrupt events
0	Shift Register Empty does not generate interrupt events

Bit 6 – SPIROVEN Enable Interrupt Events via SPIROV bit

Value	Description
1	SPI Receive Overflow generates an interrupt event
0	SPI Receive Overflow does not generate an interrupt event

Bit 5 – SPIRBEN Enable Interrupt Events via SPIRBE bit

Value	Description
1	SPI RX buffer empty generates an interrupt event
0	SPI RX buffer empty does not generate an interrupt event

Bit 3 – SPITBEN Enable Interrupt Events via SPITBE bit

Value	Description
1	SPI transmit buffer empty generates an interrupt event
0	SPI transmit buffer empty does not generate an interrupt event

Bit 1 – SPITBFEN Enable Interrupt Events via SPITBF bit

Value	Description
1	SPI transmit buffer full generates an interrupt event
0	SPI transmit buffer full does not generate an interrupt event

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Bit 0 – SPIRBFEN Enable Interrupt Events via SPIRBF bit

Value	Description
1	SPI receive buffer full generates an interrupt event
0	SPI receive buffer full does not generate an interrupt event

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15.5.10 SPI1 Interrupt Mask Register High

Name: SPI1IMSKH
Offset: 0x40A

Bit	15	14	13	12	11	10	9	8
	RXWIEN		RXMSK[5:0]					
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TXWIEN		TXMSK[5:0]					
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit 15 – RXWIEN Receive Watermark Interrupt Enable bit

Value	Description
1	Triggers receive buffer element watermark interrupt when RXMSK[5:0] ≤ RXELM[5:0]
0	Disables receive buffer element watermark interrupt

Bits 13:8 – RXMSK[5:0] RX Buffer Mask bits
RX mask bits; used in conjunction with the RXWIEN bit.

Bit 7 – TXWIEN Transmit Watermark Interrupt Enable bit

Value	Description
1	Triggers transmit buffer element watermark interrupt when TXMSK[5:0] = TXELM[5:0]
0	Disables transmit buffer element watermark interrupt

Bits 5:0 – TXMSK[5:0] TX Buffer Mask bits
TX mask bits; used in conjunction with the TXWIEN bit.

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15.5.11 SPI1 Underrun Data Register Low

Name: SPI1URDTL
Offset: 0x40C

Bit	15	14	13	12	11	10	9	8
	URDATA[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	URDATA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – URDATA[15:0] SPI Underrun Data bits
These bits are only used when URDTEN = 1. This register holds the data to transmit when a Transmit Underrun condition occurs.

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15.5.12 SPI1 Underrun Data Register High

Name: SPI1URDTH
Offset: 0x40

Bit	15	14	13	12	11	10	9	8
	URDATA[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	URDATA[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – URDATA[31:24] SPI Underrun Data bits
These bits are only used when URDTEN = 1. This register holds the data to transmit when a Transmit Underrun condition occurs.

Bits 7:0 – URDATA[23:16] SPI Underrun Data bits

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15.5.13 SPI2 Control Register 1 Low

Name: SPI2CON1L
Offset: 0x410

Note:

1. When AUDEN = 1, this module functions as if CKE = 0, regardless of its actual value.
2. When FRMEN = 1, SSEN is not used.
3. MCLKEN can only be written when the SPIEN bit = 0.
4. This channel is not meaningful for DSP/PCM mode as LRC follows the FRMSYPW bit.

Bit	15	14	13	12	11	10	9	8
	SPIEN		SPISIDL	DISSDO	MODE[1:0]		SMP	CKE
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SSEN	CKP	MSTEN	DISSDI	DISSCK	MCLKEN	SPIFE	ENHBUF
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – SPIEN SPI On bit

Value	Description
1	Enables module
0	Turns off and resets module, disables clocks, disables interrupt event generation, allows SFR modifications

Bit 13 – SPISIDL SPI Stop in Idle Mode bit

Value	Description
1	Halts in CPU Idle mode
0	Continues to operate in CPU Idle mode

Bit 12 – DISSDO Disable SDOx Output Port bit

Value	Description
1	SDOx pin is not used by the module; pin is controlled by the port function
0	SDOx pin is controlled by the module

Bits 11:10 – MODE[1:0] Serial Word Length bits(1,4)

AUDEN = 0:			
MODE32	MODE16	COMMUNICATION	FIFO DEPTH
1	x	32-Bit	8
0	1	16-Bit	16
0	0	8-Bit	32
AUDEN = 1:			
MODE32	MODE16	COMMUNICATION	
1	1	24-Bit Data, 32-Bit FIFO, 32-Bit Channel/64-Bit Frame	
1	0	32-Bit Data, 32-Bit FIFO, 32-Bit Channel/64-Bit Frame	
0	1	16-Bit Data, 16-Bit FIFO, 32-Bit Channel/64-Bit Frame	
0	0	16-Bit Data, 16-Bit FIFO, 16-Bit Channel/32-Bit Frame	

Bit 9 – SMP SPI Data Input Sample Phase bit
Client Mode:
Input data are always sampled at the middle of data output time, regardless of the SMP setting.
Host Mode:

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Value	Description
1	Input data are sampled at the end of data output time
0	Input data are sampled at the middle of data output time

Bit 8 – CKE SPI Clock Edge Select bit(1)

Value	Description
1	Transmit happens on transition from active clock state to Idle clock state
0	Transmit happens on transition from Idle clock state to active clock state

Bit 7 – SSEN Client Select Enable bit (Client mode)(2)

Value	Description
1	$\overline{SSx}$ pin is used by the macro in Client mode; $\overline{SSx}$ pin is used as the Client select input
0	$\overline{SSx}$ pin is not used by the macro ($\overline{SSx}$ pin will be controlled by the port I/O)

Bit 6 – CKP SPI Clock Polarity Select bit

Value	Description
1	Idle state for clock is a high level; active state is a low level
0	Idle state for clock is a low level; active state is a high level

Bit 5 – MSTEN Host Mode Enable bit

Value	Description
1	Host mode
0	Client mode

Bit 4 – DISSDI Disable SDIx Input Port bit

Value	Description
1	SDIx pin is not used by the module; pin is controlled by the port function
0	SDIx pin is controlled by the module

Bit 3 – DISSCK Disable SCKx Output Port bit

Value	Description
1	SCKx pin is not used by the module; pin is controlled by the port function
0	SCKx pin is controlled by the module

Bit 2 – MCLKEN Host Clock Enable bit(3)

Value	Description
1	Reference Clock Output (REFO) is used by the BRG
0	Peripheral clock is used by the BRG

Bit 1 – SPIFE Frame Sync Pulse Edge Select bit

Value	Description
1	Frame Sync pulse (Idle-to-active edge) coincides with the first bit clock
0	Frame Sync pulse (Idle-to-active edge) precedes the first bit clock

Bit 0 – ENHBUF Enhanced Buffer Mode Enable bit

Value	Description
1	Enhanced Buffer mode is enabled
0	Enhanced Buffer mode is disabled

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15.5.14 SPI2 Control Register 1 High

Name: SPI2CON1H
Offset: 0x412

Note:

1. AUDEN can only be written when the SPIEN bit = 0.
2. AUDMONO can only be written when the SPIEN bit = 0 and is only valid for AUDEN = 1.
3. URDTEN is only valid when IGNTUR = 1.
4. AUDMOD[1:0] bits can only be written when the SPIEN bit = 0 and are only valid when AUDEN = 1. When NOT in PCM/DSP mode, this module functions as if FRMSYPW = 1, regardless of its actual value.

Bit	15	14	13	12	11	10	9	8
	AUDEN	SPISGNEXT	IGNROV	IGNTUR	AUDMONO	URDTEN	AUDMOD[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – AUDEN Audio Codec Support Enable bit(1)

Value	Description
1	Audio protocol is enabled; MSTEN controls the direction of both the SCKx and frame (a.k.a. LRC), and this module functions as if FRMEN = 1, FRMSYNC = MSTEN, FRMCNT[2:0] = 001 and SMP = 0, regardless of their actual values
0	Audio protocol is disabled

Bit 14 – SPISGNEXT SPI Sign-Extend RX FIFO Read Data Enable bit

Value	Description
1	Data from RX FIFO are sign-extended
0	Data from RX FIFO are not sign-extended

Bit 13 – IGNROV Ignore Receive Overflow bit

Value	Description
1	A Receive Overflow (ROV) is NOT a critical error; during ROV, data in the FIFO are not overwritten by the receive data
0	A ROV is a critical error that stops SPI operation

Bit 12 – IGNTUR Ignore Transmit Underrun bit

Value	Description
1	A Transmit Underrun (TUR) is NOT a critical error and data indicated by URDTEN are transmitted until the SPI2TXB is not empty
0	A TUR is a critical error that stops SPI operation

Bit 11 – AUDMONO Audio Data Format Transmit bit(2)

Value	Description
1	Audio data are mono (i.e., each data word is transmitted on both left and right channels)
0	Audio data are stereo

Bit 10 – URDTEN Transmit Underrun Data Enable bit(3)

Value	Description
1	Transmits data out of SPI2URDTL/H register during Transmit Underrun conditions
0	Transmits the last received data during Transmit Underrun conditions

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Bits 9:8 – AUDMOD[1:0] Audio Protocol Mode Selection bits(4)

Value	Description
11	PCM/DSP mode
10	Right Justified mode: This module functions as if SPIFE = 1, regardless of its actual value
01	Left Justified mode: This module functions as if SPIFE = 1, regardless of its actual value
00	I^2S mode: This module functions as if SPIFE = 0, regardless of its actual value

Bit 7 – FRMEN Framed SPI Support bit

Value	Description
1	Framed SPI support is enabled ($\overline{SSx}$ pin is used as the FSYNC input/output)
0	Framed SPI support is disabled

Bit 6 – FRMSYNC Frame Sync Pulse Direction Control bit

Value	Description
1	Frame Sync pulse input (Client)
0	Frame Sync pulse output (Host)

Bit 5 – FRMPOL Frame Sync/Client Select Polarity bit

Value	Description
1	Frame Sync pulse/Client select is active-high
0	Frame Sync pulse/Client select is active-low

Bit 4 – MSSEN Host Mode Client Select Enable bit

Value	Description
1	SPI Client select support is enabled with polarity determined by FRMPOL ($\overline{SSx}$ pin is automatically driven during transmission in Host mode)
0	SPI Client select support is disabled ($\overline{SSx}$ pin will be controlled by port I/O)

Bit 3 – FRMSYPW Frame Sync Pulse-Width bit

Value	Description
1	Frame Sync pulse is one serial word length wide (as defined by MODE[32,16]/WLENGTH[4:0])
0	Frame Sync pulse is one clock (SCKx) wide

Bits 2:0 – FRMCNT[2:0] Frame Sync Pulse Counter bits
Controls the number of serial words transmitted per Sync pulse.

Value	Description
111	Reserved
110	Reserved
101	Generates a Frame Sync pulse on every 32 serial words
100	Generates a Frame Sync pulse on every 16 serial words
011	Generates a Frame Sync pulse on every 8 serial words
010	Generates a Frame Sync pulse on every 4 serial words
001	Generates a Frame Sync pulse on every 2 serial words (value used by audio protocols)
000	Generates a Frame Sync pulse on each serial word

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15.5.15 SPI2 Control Register 2 Low

Name: SPI2CON2L
Offset: 0x414

Note:

1. These bits are effective when AUDEN = 0 only.
2. Varying the length by changing these bits does not affect the depth of the TX/RX FIFO.

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				WLENGTH[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – WLENGTH[4:0] Variable Word Length bits(1,2)

Value	Description
11111	32-bit data
11110	31-bit data
11101	30-bit data
11100	29-bit data
11011	28-bit data
11010	27-bit data
11001	26-bit data
11000	25-bit data
10111	24-bit data
10110	23-bit data
10101	22-bit data
10100	21-bit data
10011	20-bit data
10010	19-bit data
10001	18-bit data
10000	17-bit data
01111	16-bit data
01110	15-bit data
01101	14-bit data
01100	13-bit data
01011	12-bit data
01010	11-bit data
01001	10-bit data
01000	9-bit data
00111	8-bit data
00110	7-bit data
00101	6-bit data
00100	5-bit data
00011	4-bit data
00010	3-bit data
00001	2-bit data
00000	See MODE[32,16] bits in SPI2CON1L[11:10]

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15.5.16 SPI2 Status Register Low

Name: SPI2STATL
Offset: 0x418

Note:

1. SPITUR is cleared when SPIEN = 0. When IGNTUR = 1, SPITUR provides dynamic status of the Transmit Underrun condition, but does not stop RX/TX operation and does not need to be cleared by software.

Legend: C = Clearable bit; HS = Hardware Settable bit; HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
				FRMERR	SPIBUSY			SPITUR
Access				HS/R/C	HSC			HS/R/C
Reset				0	0			0

Bit	7	6	5	4	3	2	1	0
	SRMT	SPIROV	SPIRBE		SPITBE		SPITBF	SPIRBF
Access	HSC	HSC	HSC		HSC		HSC	HSC
Reset	0	0	0		0		0	0

Bit 12 – FRMERR SPI Frame Error Status bit

Value	Description
1	Frame error is detected
0	No frame error is detected

Bit 11 – SPIBUSY SPI Activity Status bit

Value	Description
1	Module is currently busy with some transactions
0	No ongoing transactions (at time of read)

Bit 8 – SPITUR SPI Transmit Underrun Status bit(1)

Value	Description
1	Transmit buffer has encountered a Transmit Underrun condition
0	Transmit buffer does not have a Transmit Underrun condition

Bit 7 – SRMT Shift Register Empty Status bit

Value	Description
1	No current or pending transactions (i.e., neither SPI2TXB or SPI2TXSR contains data to transmit)
0	Current or pending transactions

Bit 6 – SPIROV SPI Receive Overflow Status bit

Value	Description
1	A new byte/half-word/word has been completely received when the SPI2RXB is full
0	No overflow

Bit 5 – SPIRBE SPI RX Buffer Empty Status bit
Standard Buffer Mode:
Automatically set in hardware when SPI2BUF is read from, reading SPI2RXB. Automatically cleared in hardware when SPI transfers data from SPI2RXSR to SPI2RXB.
Enhanced Buffer Mode:
Indicates RXELM[5:0] = 000000.

Value	Description
1	RX buffer is empty
0	RX buffer is not empty

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Bit 3 – SPITBE SPI Transmit Buffer Empty Status bit
Standard Buffer Mode:
Automatically set in hardware when SPI transfers data from SPI2TXB to SPI2TXSR. Automatically cleared in hardware when SPI2BUF is written, loading SPI2TXB.
Enhanced Buffer Mode:
Indicates TXELM[5:0] = 000000.

Value	Description
1	SPI2TXB is empty
0	SPI2TXB is not empty

Bit 1 – SPITBF SPI Transmit Buffer Full Status bit
Standard Buffer Mode:
Automatically set in hardware when SPI2BUF is written, loading SPI2TXB. Automatically cleared in hardware when SPI transfers data from SPI2TXB to SPI2TXSR.
Enhanced Buffer Mode:
Indicates TXELM[5:0] = 111111.

Value	Description
1	SPI2TXB is full
0	SPI2TXB not full

Bit 0 – SPIRBF SPI Receive Buffer Full Status bit
Standard Buffer Mode:
Automatically set in hardware when SPI transfers data from SPI2RXSR to SPI2RXB. Automatically cleared in hardware when SPI2BUF is read from, reading SPI2RXB.
Enhanced Buffer Mode:
Indicates RXELM[5:0] = 111111.

Value	Description
1	SDIx pin is not used by the module; pin is controlled by the port function
0	SDIx pin is controlled by the module

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15.5.17 SPI2 Status Register High

Name: SPI2STATH
Offset: 0x41A

Legend: C = Clearable bit, HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
			RXELM[5:0]					
Access			HSC/R/C	HSC/R/C	HSC/R/C	HSC/R/C	HSC/R/C	HSC/R/C
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			TXELM[5:0]					
Access			HSC/R/C	HSC/R/C	HSC/R/C	HSC/R/C	HSC/R/C	HSC/R/C
Reset			0	0	0	0	0	0

Bits 13:8 – RXELM[5:0] Receive Buffer Element Count bits (valid in Enhanced Buffer mode)

Bits 5:0 – TXELM[5:0] Transmit Buffer Element Count bits (valid in Enhanced Buffer mode)

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15.5.18 SPI2 Buffer Register Low

Name: SPI2BUFL
Offset: 0x41C

Bit	15	14	13	12	11	10	9	8
	DATA[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DATA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – DATA[15:0] SPI FIFO Data bits

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15.5.19 SPI2 Buffer Register High

Name: SPI2BUFH
Offset: 0x41E

Bit	15	14	13	12	11	10	9	8
	DATA[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DATA[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – DATA[31:24] SPI FIFO Data bits

Bits 7:0 – DATA[23:16] SPI FIFO Data bits

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15.5.20 SPI2 Baud Rate Generator Register Low

Name: SPI2BRGL
Offset: 0x420

Note:

1. Changing the BRG value when SPIEN = 1 causes undefined behavior.

Bit	15	14	13	12	11	10	9	8
				BRG[12:8]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BRG[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 12:0 – BRG[12:0] SPI Baud Rate Generator Divisor bits(1)

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15.5.21 SPI2 Interrupt Mask Register Low

Name: SPI2IMSKL
Offset: 0x424

Legend: C = Clearable bit

Bit	15	14	13	12	11	10	9	8
				FRMERREN	BUSYEN			SPITUREN
Access				R/W	R/W			R/C
Reset				0	0			0

Bit	7	6	5	4	3	2	1	0
	SRMTEN	SPIROVEN	SPIRBEN		SPITBEN		SPITBFEN	SPIRBFEN
Access	R/W	R/W	R/W		R/W		R/W	R/W
Reset	0	0	0		0		0	0

Bit 12 – FRMERREN Enable Interrupt Events via FRMERR bit

Value	Description
1	Frame error generates an interrupt event
0	Frame error does not generate an interrupt event

Bit 11 – BUSYEN Enable Interrupt Events via SPIBUSY bit

Value	Description
1	SPIBUSY generates an interrupt event
0	SPIBUSY does not generate an interrupt event

Bit 8 – SPITUREN Enable Interrupt Events via SPITUR bit

Value	Description
1	Transmit Underrun (TUR) generates an interrupt event
0	Transmit Underrun does not generate an interrupt event

Bit 7 – SRMTEN Enable Interrupt Events via SRMT bit

Value	Description
1	Shift Register Empty (SRMT) generates interrupt events
0	Shift Register Empty does not generate interrupt events

Bit 6 – SPIROVEN Enable Interrupt Events via SPIROV bit

Value	Description
1	SPI receive overflow generates an interrupt event
0	SPI receive overflow does not generate an interrupt event

Bit 5 – SPIRBEN Enable Interrupt Events via SPIRBE bit

Value	Description
1	SPI RX buffer empty generates an interrupt event
0	SPI RX buffer empty does not generate an interrupt event

Bit 3 – SPITBEN Enable Interrupt Events via SPITBE bit

Value	Description
1	SPI transmit buffer empty generates an interrupt event
0	SPI transmit buffer empty does not generate an interrupt event

Bit 1 – SPITBFEN Enable Interrupt Events via SPITBF bit

Value	Description
1	SPI transmit buffer full generates an interrupt event
0	SPI transmit buffer full does not generate an interrupt event

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Bit 0 – SPIRBFEN Enable Interrupt Events via SPIRBF bit

Value	Description
1	SPI receive buffer full generates an interrupt event
0	SPI receive buffer full does not generate an interrupt event

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15.5.22 SPI2 Interrupt Mask Register High

Name: SPI2IMSKH
Offset: 0x426

Bit	15	14	13	12	11	10	9	8
	RXWIEN		RXMSK[5:0]					
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TXWIEN		TXMSK[5:0]					
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit 15 – RXWIEN Receive Watermark Interrupt Enable bit

Value	Description
1	Triggers receive buffer element watermark interrupt when RXMSK[5:0] ≤ RXELM[5:0]
0	Disables receive buffer element watermark interrupt

Bits 13:8 – RXMSK[5:0] RX Buffer Mask bits
RX mask bits; used in conjunction with the RXWIEN bit.

Bit 7 – TXWIEN Transmit Watermark Interrupt Enable bit

Value	Description
1	Triggers transmit buffer element watermark interrupt when TXMSK[5:0] = TXELM[5:0]
0	Disables transmit buffer element watermark interrupt

Bits 5:0 – TXMSK[5:0] TX Buffer Mask bits
TX mask bits; used in conjunction with the TXWIEN bit.

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15.5.23 SPI2 Underrun Data Register Low

Name: SPI2URDTL
Offset: 0x428

Bit	15	14	13	12	11	10	9	8
	URDATA[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	URDATA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – URDATA[15:0] SPI Underrun Data bits
These bits are only used when URDTEN = 1. This register holds the data to transmit when a Transmit Underrun condition occurs.

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15.5.24 SPI2 Underrun Data Register High

Name: SPI2URDTH
Offset: 0x42A

Bit	15	14	13	12	11	10	9	8
	URDATA[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	URDATA[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – URDATA[31:24] SPI Underrun Data bits
These bits are only used when URDTEN = 1. This register holds the data to transmit when a Transmit Underrun condition occurs.

Bits 7:0 – URDATA[23:16] SPI Underrun Data bits

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16. Inter-Integrated Circuit (I²C)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to **"Inter-Integrated Circuit (I²C)"** (www.mcrochip.com/DS70000195) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

The Inter-Integrated Circuit (I²C) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, display drivers, A/D Converters, etc.

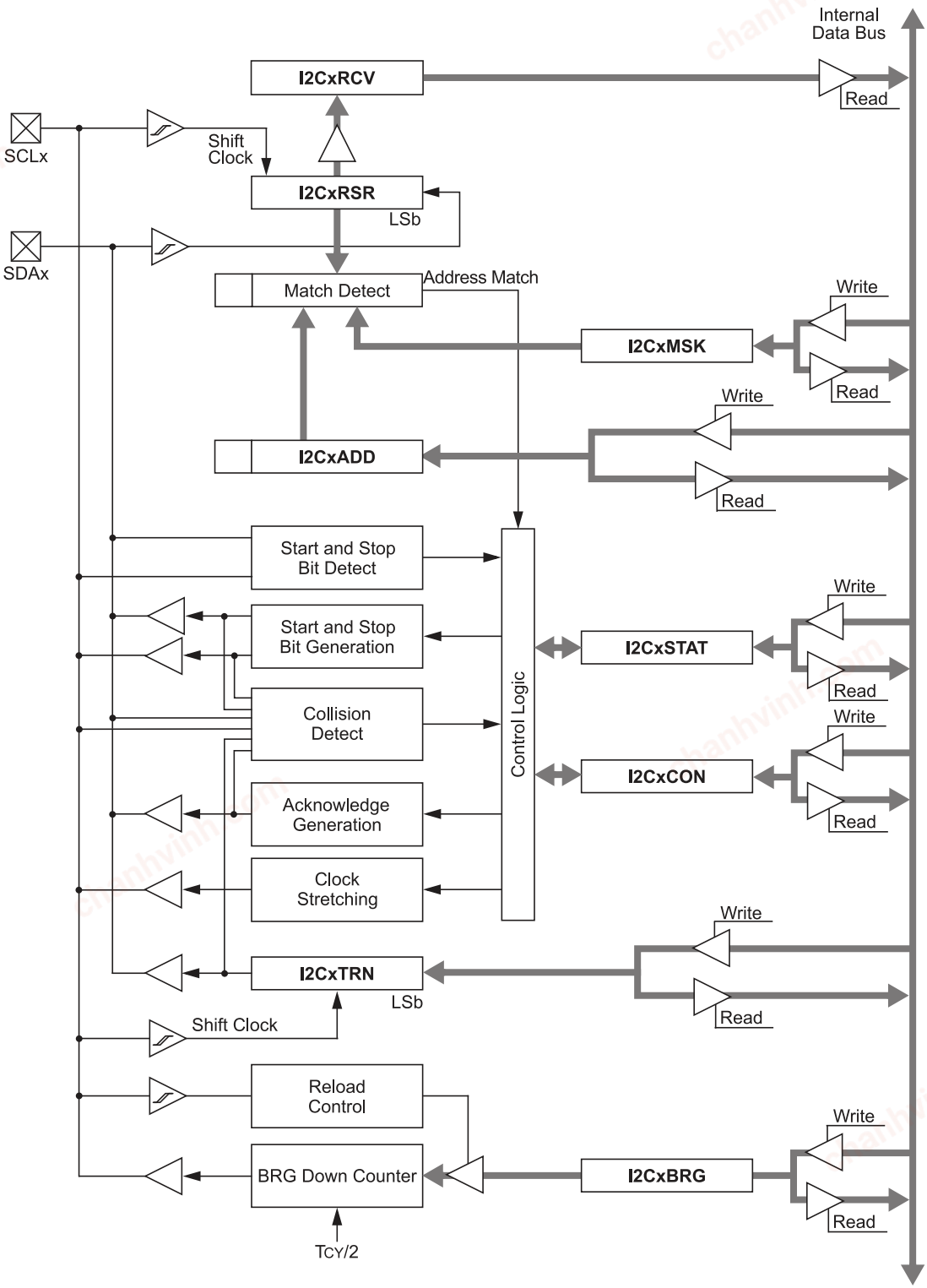
The I²C module supports these features:

- Independent Host and Client Logic
- 7-Bit and 10-Bit Device Addresses
- General Call Address as Defined in the I²C Protocol
- Clock Stretching to Provide Delays for the Processor to Respond to a Client Data Request
- Both 100 kHz, 400 kHz and 1 MHz Bus Specifications
- Configurable Address Masking
- Multi-Host modes to Prevent Loss of Messages in Arbitration
- Bus Repeater mode, Allowing the Acceptance of All Messages as a Client, regardless of the Address
- Automatic SCL
- PMBus™

A block diagram of the module is shown in Figure 16-1.

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Figure 16-1. I²C Block Diagram



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16.1 Communicating as a Host in a Single Host Environment

The details of sending a message in Host mode depends on the communications protocol for the device being communicated with. Typically, the sequence of events is as follows:

1. Assert a Start condition on SDAx and SCLx.
2. Send the I^2C device address byte to the Client with a write indication.
3. Wait for and verify an Acknowledge from the Client.
4. Send the first data byte (sometimes known as the command) to the Client.
5. Wait for and verify an Acknowledge from the Client.
6. Send the serial memory address low byte to the Client.
7. Repeat Steps 4 and 5 until all data bytes are sent.
8. Assert a Repeated Start condition on SDAx and SCLx.
9. Send the device address byte to the Client with a read indication.
10. Wait for and verify an Acknowledge from the Client.
11. Enable Host reception to receive serial memory data.
12. Generate an ACK or NACK condition at the end of a received byte of data.
13. Generate a Stop condition on SDAx and SCLx.

16.2 Setting Baud Rate When Operating as a Bus Host

To compute the Baud Rate Generator reload value, use Equation 16-1.

Equation 16-1. Computing Baud Rate Reload Value(1,2,3)

$$FSCL = \frac{FPB}{(I2CxBRG + 2) * 2}$$

or:

$$I2CxBRG = \left[\frac{FPB}{(FSCL * 2)} - 2\right]$$

Note:

1. Based on $F_{PB} = F_{OSC}/2$ (Peripheral Clock).
2. These clock rate values are for guidance only. The actual clock rate can be affected by various system-level parameters. The actual clock rate should be measured in its intended application.
3. BRG values of 0 to 3 are forbidden.

16.3 Host Address Masking

The I2CxMSK register designates address bit positions as “don’t care” for both 7-Bit and 10-Bit Addressing modes. Setting a particular bit location (= 1) in the I2CxMSK register causes the Client module to respond, whether the corresponding address bit value is a ‘0’ or a ‘1’. For example, when I2CxMSK is set to ‘0010000000’, the Client module will detect both addresses, ‘0000000000’ and ‘0010000000’.

To enable address masking, the Intelligent Peripheral Management Interface (IPMI) must be disabled by clearing the STRICT bit (I2CxCONL[11]).

Note: As a result of changes in the I^2C protocol, the addresses in Table 16-1 are reserved and will not be Acknowledged in Client mode. This includes any address mask settings that include any of these addresses.

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Table 16-1. I²C Reserved Addresses(1)

Client Address	R/$\overline{W}$ Bit	Description
0000 000	0	General Call Address(2)
0000 000	1	Start Byte
0000 001	x	C-Bus Address
0000 01x	x	Reserved
0000 1xx	x	HS Mode Host Code
1111 0xx	x	10-Bit Client Upper Byte(3)
1111 1xx	x	Reserved

Note:

1. The address bits listed here will never cause an address match independent of address mask settings.
2. This address will be Acknowledged only if GCEN = 1.
3. A match on this address can only occur on the upper byte in 10-Bit Addressing mode.

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16.4 I2C Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x0493	Reserved									
0x0494	I2C1RCV	7:0	I2CRXDATA[7:0]							
		15:8								
0x0496	I2C1TRN	7:0	I2CTXDATA[7:0]							
		15:8								
0x0498	I2C1BRG	7:0	I2CBRG[7:0]							
		15:8	I2CBRG[15:8]							
0x049A	I2C1CONL	7:0	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
		15:8	I2CEN		I2CSIDL	SCLREL	STRICT	A10M	DISSLW	SMEN
0x049C	I2C1CONH	7:0		PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
		15:8								
0x049E	I2C1STAT	7:0	IWCOL	I2COV	D/$\overline{A}$	P	S	R/$\overline{W}$	RBF	TBF
		15:8	ACKSTAT	TRSTAT	ACKTIM			BCL	GCSTAT	ADD10
0x04A0	I2C1ADD	7:0	ADD[7:0]							
		15:8							ADD[9:8]	
0x04A2	I2C1MSK	7:0	MSK[7:0]							
		15:8							MSK[9:8]	
0x04A4	I2C2RCV	7:0	I2CRXDATA[7:0]							
		15:8								
0x04A6	I2C2TRN	7:0	I2CTXDATA[7:0]							
		15:8								
0x04A8	I2C2BRG	7:0	I2CBRG[7:0]							
		15:8	I2CBRG[15:8]							
0x04AA	I2C2CONL	7:0	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
		15:8	I2CEN		I2CSIDL	SCLREL	STRICT	A10M	DISSLW	SMEN
0x04AC	I2C2CONH	7:0		PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
		15:8								
0x04AE	I2C2STAT	7:0	IWCOL	I2COV	D/$\overline{A}$	P	S	R/$\overline{W}$	RBF	TBF
		15:8	ACKSTAT	TRSTAT	ACKTIM			BCL	GCSTAT	ADD10
0x04B0	I2C2ADD	7:0	ADD[7:0]							
		15:8							ADD[9:8]	
0x04B2	I2C2MSK	7:0	MSK[7:0]							
		15:8							MSK[9:8]	

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16.4.1 I2C1 Receive Register

Name: I2C1RCV
Offset: 0x494

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	I2CRXDATA[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – I2CRXDATA[7:0] I2C1 Receive Data bits

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16.4.2 I2C1 Transmit Register

Name: I2C1TRN
Offset: 0x496

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	I2CTXDATA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – I2CTXDATA[7:0] I2C1 Transmit Data bits

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16.4.3 I2C1 Baud Rate Generator Register

Name: I2C1BRG
Offset: 0x498

Bit	15	14	13	12	11	10	9	8
	I2CBRG[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	I2CBRG[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – I2CBRG[15:0] I2C1 Baud Rate Generator bits

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16.4.4 I2C1 Control Register Low

Name: I2C1CONL
Offset: 0x49A

Note:

1. Automatically cleared to '0' at the beginning of Client transmission; automatically cleared to '0' at the end of Client reception. The user software must provide a delay between writing to the transmit buffer and setting the SCLREL bit. This delay must be greater than the minimum setup time for Client transmissions, as specified in 30. Electrical Characteristics.
2. Automatically cleared to '0' at the beginning of Client transmission.
3. *"SMBus 3.0 Specification"* input level can be selected by the SMB3EN Configuration bit (FDEVOPT1[10]).

Legend: HC = Hardware Clearable bit

Bit	15	14	13	12	11	10	9	8
	I2CEN		I2CSIDL	SCLREL	STRICT	A10M	DISSLW	SMEN
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
Access	R/W	R/W	R/W	HC/R/W	HC/R/W	HC/R/W	HC/R/W	HC/R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – I2CEN I2C1 Enable bit (writable from software only)

Value	Description
1	Enables the I^2C module and configures the SDA and SCL pins as serial port pins
0	Disables the I^2C module; all I^2C pins are controlled by port functions

Bit 13 – I2CSIDL I2C1 Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode
0	Continues module operation in Idle mode

Bit 12 – SCLREL SCL Release Control bit (I^2C Client mode only)(1)
If STREN = 1:

Value	Description
1	Releases clock
0	Holds clock low (clock stretch); user may program this bit to '0', clock stretch at next SCL low

If STREN = 0:(2)

Value	Description
1	Releases clock
0	Forces clock low (clock stretch)

Bit 11 – STRICT I2C1 Strict Reserved Address Rule Enable bit

Value	Description
1	Strict Reserved Addressing is enforced (for reserved addresses, refer to Table 16-1) In Client Mode: The device does not respond to reserved address space and addresses falling in that category are NACKed. In Host Mode: The device is allowed to generate addresses with reserved address space.

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Value	Description
0	Reserved Addressing would be Acknowledged In Client Mode: The device will respond to an address falling in the reserved address space. When there is a match with any of the reserved addresses, the device will generate an ACK. In Host Mode: Reserved.

Bit 10 – A10M 10-Bit Client Address Flag bit

Value	Description
1	I2C1ADD is a 10-bit Client address
0	I2C1ADD is a 7-bit Client address

Bit 9 – DISSLW Slew Rate Control Disable bit

Value	Description
1	Slew rate control is disabled for Standard Speed mode (100 kHz, also disabled for 1 MHz mode)
0	Slew rate control is enabled for High-Speed mode (400 kHz)

Bit 8 – SMEN SMBus Input Levels Enable bit(3)

Value	Description
1	Enables input logic so thresholds are compliant with the SMBus specification
0	Disables SMBus-specific inputs

Bit 7 – GCEN General Call Enable bit (I^2C Client mode only)

Value	Description
1	Enables interrupt when a general call address is received in I2C1RSR; module is enabled for reception
0	General call address is disabled

Bit 6 – STREN SCL Clock Stretch Enable bit
In I^2C Client mode only; used in conjunction with the SCLREL bit.

Value	Description
1	Enables clock stretching
0	Disables clock stretching

Bit 5 – ACKDT Acknowledge Data bit
In I^2C Host mode during Host Receive mode: The value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive.
In I^2C Client mode when AHEN = 1 or DHEN = 1: The value that the Client will transmit when it initiates an Acknowledge sequence at the end of an address or data reception.

Value	Description
1	NACK is sent
0	ACK is sent

Bit 4 – ACKEN Acknowledge Sequence Enable bit
In I^2C Host mode only; applicable during Host Receive mode.

Value	Description
1	Initiates Acknowledge sequence on SDA and SCL pins, and transmits the ACKDT data bit
0	Acknowledge sequence is Idle

Bit 3 – RCEN Receive Enable bit (I^2C Host mode only)

Value	Description
1	Enables Receive mode for I^2C; automatically cleared by hardware at the end of the 8-bit receive data byte
0	Receive sequence is not in progress

Bit 2 – PEN Stop Condition Enable bit (I^2C Host mode only)

Value	Description
1	Initiates Stop condition on the SDA and SCL pins

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Value	Description
0	Stop condition is Idle

Bit 1 – RSEN Restart Condition Enable bit (I^2C Host mode only)

Value	Description
1	Initiates Restart condition on the SDA and SCL pins
0	Restart condition is Idle

Bit 0 – SEN Start Condition Enable bit (I^2C Host mode only)

Value	Description
1	Initiates Start condition on the SDA and SCL pins
0	Start condition is Idle

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16.4.5 I2C1 Control Register High

Name: I2C1CONH
Offset: 0x49C

Note:

1. This bit must be set to '0' for 1 MHz operation.

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit 6 – PCIE Stop Condition Interrupt Enable bit (I^2C Client mode only)

Value	Description
1	Enables interrupt on detection of Stop condition
0	Stop detection interrupts are disabled

Bit 5 – SCIE Start Condition Interrupt Enable bit (I^2C Client mode only)

Value	Description
1	Enables interrupt on detection of Start or Restart conditions
0	Start detection interrupts are disabled

Bit 4 – BOEN Buffer Overwrite Enable bit (I^2C Client mode only)

Value	Description
1	I2C1RCV is updated and an ACK is generated for a received address/data byte, ignoring the state of the I2COV bit only if RBF bit = 0
0	I2C1RCV is only updated when I2COV is clear

Bit 3 – SDAHT SDA Hold Time Selection bit(1)

Value	Description
1	Minimum of 300 ns hold time on SDA after the falling edge of SCL
0	Minimum of 100 ns hold time on SDA after the falling edge of SCL

Bit 2 – SBCDE Client Mode Bus Collision Detect Enable bit (I^2C Client mode only)
If, on the rising edge of SCL, SDA is sampled low when the module is outputting a high state, the BCL bit is set and the bus goes Idle. This Detection mode is only valid during data and ACK transmit sequences.

Value	Description
1	Enables Client bus collision interrupts
0	Client bus collision interrupts are disabled

Bit 1 – AHEN Address Hold Enable bit (I^2C Client mode only)

Value	Description
1	Following the 8th falling edge of SCL for a matching received address byte; SCLREL bit (I2CxCONL[12]) will be cleared and SCL will be held low
0	Address holding is disabled

Bit 0 – DHEN Data Hold Enable bit (I^2C Client mode only)

Value	Description
1	Following the 8th falling edge of SCL for a received data byte; Client hardware clears the SCLREL bit (I2C1CONL[12]) and SCL is held low

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Value	Description
0	Data holding is disabled

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16.4.6 I2C1 Status Register

Name: I2C1STAT
Offset: 0x49E

Bit	15	14	13	12	11	10	9	8
	ACKSTAT	TRSTAT	ACKTIM			BCL	GCSTAT	ADD10
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bit	7	6	5	4	3	2	1	0
	IWCOL	I2COV	D/$\overline{A}$	P	S	R/$\overline{W}$	RBF	TBF
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – ACKSTAT Acknowledge Status bit (updated in all Host and Client modes)

Value	Description
1	Acknowledge was not received from Client
0	Acknowledge was received from Client

Bit 14 – TRSTAT Transmit Status bit (when operating as I^2C Host; applicable to Host transmit operation)

Value	Description
1	Host transmit is in progress (8 bits + ACK)
0	Host transmit is not in progress

Bit 13 – ACKTIM Acknowledge Time Status bit (valid in I^2C Client mode only)

Value	Description
1	Indicates I^2C bus is in an Acknowledge sequence, set on 8th falling edge of SCL clock
0	Not an Acknowledge sequence, cleared on 9th rising edge of SCL clock

Bit 10 – BCL Bus Collision Detect bit (Host/Client mode; cleared when I^2C module is disabled, I2CEN = 0)

Value	Description
1	A bus collision has been detected during a Host or Client transmit operation
0	No bus collision has been detected

Bit 9 – GCSTAT General Call Status bit (cleared after Stop detection)

Value	Description
1	General call address was received
0	General call address was not received

Bit 8 – ADD10 10-Bit Address Status bit (cleared after Stop detection)

Value	Description
1	10-bit address was matched
0	10-bit address was not matched

Bit 7 – IWCOL I2C1 Write Collision Detect bit

Value	Description
1	An attempt to write to the I2C1TRN register failed because the I^2C module is busy; must be cleared in software
0	No collision

Bit 6 – I2COV I2C1 Receive Overflow Flag bit

Value	Description
1	A byte was received while the I2C1RCV register was still holding the previous byte; I2COV is a “don’t care” in Transmit mode, must be cleared in software

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Value	Description
0	No overflow

Bit 5 – D/$\overline{A}$ Data/Address bit (when operating as I^2C Client)

Value	Description
1	Indicates that the last byte received was data
0	Indicates that the last byte received or transmitted was an address

Bit 4 – P I2C1 Stop bit
Updated when Start, Reset or Stop is detected; cleared when the I^2C module is disabled, I2CEN = 0.

Value	Description
1	Indicates that a Stop bit has been detected last
0	Stop bit was not detected last

Bit 3 – S I2C1 Start bit
Updated when Start, Reset or Stop is detected; cleared when the I^2C module is disabled, I2CEN = 0.

Value	Description
1	Indicates that a Start (or Repeated Start) bit has been detected last
0	Start (or Repeated Start) bit was not detected last

Bit 2 – R/$\overline{W}$ Read/Write Information bit (when operating as I^2C Client)
Updated when Start, Reset or Stop is detected; cleared when the I^2C module is disabled, I2CEN = 0.

Value	Description
1	Read: Indicates the data transfer is output from the Client
0	Write: Indicates the data transfer is input to the Client

Bit 1 – RBF Receive Buffer Full Status bit

Value	Description
1	Receive is complete, I2C1RCV is full
0	Receive is not complete, I2C1RCV is empty

Bit 0 – TBF Transmit Buffer Full Status bit

Value	Description
1	Transmit is in progress, I2C1TRN is full (eight bits of data)
0	Transmit is complete, I2C1TRN is empty

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16.4.7 I2C1 Address Register

Name: I2C1ADD
Offset: 0x4A0

Bit	15	14	13	12	11	10	9	8
							ADD[9:8]	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	ADD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – ADD[9:0] I2C1 Address bits

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16.4.8 I2C1 Slave Mode Address Mask Register

Name: I2C1MSK
Offset: 0x4A2

Bit	15	14	13	12	11	10	9	8
							MSK[9:8]	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	MSK[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – MSK[9:0] I2C1 Mask for Address bits

Value	Description
1	Enables masking for bit of the incoming message address; bit match is not required in this position
0	Disables masking for bit; bit match is required in this position

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16.4.9 I2C2 Receive Register

Name: I2C2RCV
Offset: 0x4A4

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	I2CRXDATA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – I2CRXDATA[7:0] I2C2 Receive Data bits

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16.4.10 I2C2 Transmit Register

Name: I2C2TRN
Offset: 0x4A6

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	I2CTXDATA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – I2CTXDATA[7:0] I2C2 Transmit Data bits

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16.4.11 I2C2 Baud Rate Generator Register

Name: I2C2BRG
Offset: 0x4A8

Bit	15	14	13	12	11	10	9	8
	I2CBRG[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	I2CBRG[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – I2CBRG[15:0] I2C2 Baud Rate Generator bits

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16.4.12 I2C2 Control Register Low

Name: I2C2CONL
Offset: 0x4AA

Note:

1. Automatically cleared to '0' at the beginning of Client transmission; automatically cleared to '0' at the end of Client reception. The user software must provide a delay between writing to the transmit buffer and setting the SCLREL bit. This delay must be greater than the minimum setup time for Client transmissions, as specified in 30. Electrical Characteristics.
2. Automatically cleared to '0' at the beginning of Client transmission.
3. *"SMBus 3.0 Specification"* input level can be selected by the SMB3EN Configuration bit (FDEVOPT1[10]).

Legend: HC = Hardware Clearable bit

Bit	15	14	13	12	11	10	9	8
	I2CEN		I2CSIDL	SCLREL	STRICT	A10M	DISSLW	SMEN
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
Access	R/W	R/W	R/W	HC/R/W	HC/R/W	HC/R/W	HC/R/W	HC/R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – I2CEN I2C2 Enable bit (writable from software only)

Value	Description
1	Enables the I2C2 module and configures the SDA and SCL pins as serial port pins
0	Disables the I2C2 module; all I^2C pins are controlled by port functions

Bit 13 – I2CSIDL I2C2 Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode
0	Continues module operation in Idle mode

Bit 12 – SCLREL SCL Release Control bit (I^2C Client mode only)(1)
If STREN = 1:

Value	Description
1	Releases clock
0	Holds clock low (clock stretch); user may program this bit to '0', clock stretch at next SCL low

If STREN = 0:(2)

Value	Description
1	Releases clock
0	Forces clock low (clock stretch)

Bit 11 – STRICT I2C2 Strict Reserved Address Rule Enable bit

Value	Description
1	Strict Reserved Addressing is enforced (for reserved addresses, refer to Table 16-1) In Client mode: The device does not respond to reserved address space and addresses falling in that category are NACKed. In Host mode: The device is allowed to generate addresses with reserved address space.

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Value	Description
0	Reserved addressing would be Acknowledged In Client mode: The device will respond to an address falling in the reserved address space. When there is a match with any of the reserved addresses, the device will generate an ACK. In Host mode: Reserved.

Bit 10 – A10M 10-Bit Client Address Flag bit

Value	Description
1	I2C2ADD is a 10-bit Client address
0	I2C2ADD is a 7-bit Client address

Bit 9 – DISSLW Slew Rate Control Disable bit

Value	Description
1	Slew rate control is disabled for Standard Speed mode (100 kHz, also disabled for 1 MHz mode)
0	Slew rate control is enabled for High-Speed mode (400 kHz)

Bit 8 – SMEN SMBus Input Levels Enable bit(3)

Value	Description
1	Enables input logic so thresholds are compliant with the SMBus specification
0	Disables SMBus-specific inputs

Bit 7 – GCEN General Call Enable bit (I^2C Client mode only)

Value	Description
1	Enables interrupt when a general call address is received in I2C2RSR; module is enabled for reception
0	General call address is disabled

Bit 6 – STREN SCL Clock Stretch Enable bit
In I^2C Client mode only; used in conjunction with the SCLREL bit.

Value	Description
1	Enables clock stretching
0	Disables clock stretching

Bit 5 – ACKDT Acknowledge Data bit
In I^2C Host mode during Host Receive mode: The value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive.
In I^2C Client mode when AHEN = 1 or DHEN = 1: The value that the Client will transmit when it initiates an Acknowledge sequence at the end of an address or data reception.

Value	Description
1	NACK is sent
0	ACK is sent

Bit 4 – ACKEN Acknowledge Sequence Enable bit
In I^2C Host mode only; applicable during Host Receive mode.

Value	Description
1	Initiates Acknowledge sequence on SDA and SCL pins, and transmits the ACKDT data bit
0	Acknowledge sequence is Idle

Bit 3 – RCEN Receive Enable bit (I^2C Host mode only)

Value	Description
1	Enables Receive mode for I^2C; automatically cleared by hardware at the end of the 8-bit receive data byte
0	Receive sequence is not in progress

Bit 2 – PEN Stop Condition Enable bit (I^2C Host mode only)

Value	Description
1	Initiates Stop condition on the SDA and SCL pins

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Value	Description
0	Stop condition is Idle

Bit 1 – RSEN Restart Condition Enable bit (I^2C Host mode only)

Value	Description
1	Initiates Restart condition on the SDA and SCL pins
0	Restart condition is Idle

Bit 0 – SEN Start Condition Enable bit (I^2C Host mode only)

Value	Description
1	Initiates Start condition on the SDA and SCL pins
0	Start condition is Idle

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16.4.13 I2C2 Control Register High

Name: I2C2CONH
Offset: 0x4AC

Note:

1. This bit must be set to '0' for 1 MHz operation.

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit 6 – PCIE Stop Condition Interrupt Enable bit (I^2C Client mode only)

Value	Description
1	Enables interrupt on detection of Stop condition
0	Stop detection interrupts are disabled

Bit 5 – SCIE Start Condition Interrupt Enable bit (I^2C Client mode only)

Value	Description
1	Enables interrupt on detection of Start or Restart conditions
0	Start detection interrupts are disabled

Bit 4 – BOEN Buffer Overwrite Enable bit (I^2C Client mode only)

Value	Description
1	I2C2RCV is updated and an ACK is generated for a received address/data byte, ignoring the state of the I2COV bit only if RBF bit = 0
0	I2C2RCV is only updated when I2COV is clear

Bit 3 – SDAHT SDA Hold Time Selection bit(1)

Value	Description
1	Minimum of 300 ns hold time on SDA after the falling edge of SCL
0	Minimum of 100 ns hold time on SDA after the falling edge of SCL

Bit 2 – SBCDE Client Mode Bus Collision Detect Enable bit (I^2C Client mode only)
If, on the rising edge of SCL, SDA is sampled low when the module is outputting a high state, the BCL bit is set and the bus goes Idle. This Detection mode is only valid during data and ACK transmit sequences.

Value	Description
1	Enables Client bus collision interrupts
0	Client bus collision interrupts are disabled

Bit 1 – AHEN Address Hold Enable bit (I^2C Client mode only)

Value	Description
1	Following the 8th falling edge of SCL for a matching received address byte; SCLREL bit (I2C2CONL[12]) will be cleared and SCL will be held low
0	Address holding is disabled

Bit 0 – DHEN Data Hold Enable bit (I^2C Client mode only)

Value	Description
1	Following the 8th falling edge of SCL for a received data byte; Client hardware clears the SCLREL bit (I2C2CONL[12]) and SCL is held low

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Value	Description
0	Data holding is disabled

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16.4.14 I2C2 Status Register

Name: I2C2STAT
Offset: 0x4AE

Bit	15	14	13	12	11	10	9	8
	ACKSTAT	TRSTAT	ACKTIM			BCL	GCSTAT	ADD10
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bit	7	6	5	4	3	2	1	0
	IWCOL	I2COV	D/$\overline{A}$	P	S	R/$\overline{W}$	RBF	TBF
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – ACKSTAT Acknowledge Status bit (updated in all Host and Client modes)

Value	Description
1	Acknowledge was not received from Client
0	Acknowledge was received from Client

Bit 14 – TRSTAT Transmit Status bit (when operating as I^2C Host; applicable to Host transmit operation)

Value	Description
1	Host transmit is in progress (8 bits + ACK)
0	Host transmit is not in progress

Bit 13 – ACKTIM Acknowledge Time Status bit (valid in I^2C Client mode only)

Value	Description
1	Indicates I^2C bus is in an Acknowledge sequence, set on 8th falling edge of SCL clock
0	Not an Acknowledge sequence, cleared on 9th rising edge of SCL clock

Bit 10 – BCL Bus Collision Detect bit (Host/Client mode; cleared when I^2C module is disabled, I2CEN = 0)

Value	Description
1	A bus collision has been detected during a Host or Client transmit operation
0	No bus collision has been detected

Bit 9 – GCSTAT General Call Status bit (cleared after Stop detection)

Value	Description
1	General call address was received
0	General call address was not received

Bit 8 – ADD10 10-Bit Address Status bit (cleared after Stop detection)

Value	Description
1	10-bit address was matched
0	10-bit address was not matched

Bit 7 – IWCOL I2C2 Write Collision Detect bit

Value	Description
1	An attempt to write to the I2C2TRN register failed because the I^2C module is busy; must be cleared in software
0	No collision

Bit 6 – I2COV I2C2 Receive Overflow Flag bit

Value	Description
1	A byte was received while the I2C2RCV register was still holding the previous byte; I2COV is a “don’t care” in Transmit mode, must be cleared in software

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Value	Description
0	No overflow

Bit 5 – D/$\overline{A}$ Data/Address bit (when operating as I^2C Client)

Value	Description
1	Indicates that the last byte received was data
0	Indicates that the last byte received or transmitted was an address

Bit 4 – P I2C2 Stop bit
Updated when Start, Reset or Stop is detected; cleared when the I^2C module is disabled, I2CEN = 0.

Value	Description
1	Indicates that a Stop bit has been detected last
0	Stop bit was not detected last

Bit 3 – S I2C2 Start bit
Updated when Start, Reset or Stop is detected; cleared when the I^2C module is disabled, I2CEN = 0.

Value	Description
1	Indicates that a Start (or Repeated Start) bit has been detected last
0	Start (or Repeated Start) bit was not detected last

Bit 2 – R/$\overline{W}$ Read/Write Information bit (when operating as I^2C Client)
Updated when Start, Reset or Stop is detected; cleared when the I^2C module is disabled, I2CEN = 0.

Value	Description
1	Read: Indicates the data transfer is output from the Client
0	Write: Indicates the data transfer is input to the Client

Bit 1 – RBF Receive Buffer Full Status bit

Value	Description
1	Receive is complete, I2C2RCV is full.
0	Receive is not complete, I2C2RCV is empty

Bit 0 – TBF Transmit Buffer Full Status bit

Value	Description
1	Transmit is in progress, I2C2TRN is full (eight bits of data)
0	Transmit is complete, I2C2TRN is empty

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16.4.15 I2C2 Address Register

Name: I2C2ADD
Offset: 0x4B0

Bit	15	14	13	12	11	10	9	8
							ADD[9:8]	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	ADD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – ADD[9:0] I2C2 Address bits

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16.4.16 I2C2 Slave Mode Address Mask Register

Name: I2C2MSK
Offset: 0x4B2

Bit	15	14	13	12	11	10	9	8
							MSK[9:8]	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	MSK[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – MSK[9:0] I2C2 Mask for Address bits

Value	Description
1	Enables masking for bit of the incoming message address; bit match is not required in this position
0	Disables masking for bit; bit match is required in this position

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17. Universal Asynchronous Receiver Transmitter (UART)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to **"Universal Asynchronous Receiver Transmitter (UART)"** (www.microchip.com/DS70000582) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the PIC24F device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins. The UART module includes an IrDA® encoder/decoder unit.

The PIC24FJ64GP205/GU205family devices are equipped with two UART modules, referred to as UART1 and UART2.

The primary features of the UARTx modules are:

- Full-Duplex, 8 or 9-Bit Data Transmission through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop bits
- Hardware Flow Control Option with the $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Pins
- Fully Integrated Baud Rate Generator with 16-Bit Prescaler
- Baud Rates Range from Up to 1 Mbps and Down to 15 Hz at 16 MIPS in 16x mode
- Baud Rates Range from Up to 4 Mbps and Down to 61 Hz at 16 MIPS in 4x mode
- 4-Deep, First-In First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-Bit mode with Address Detect (9th bit = 1)
- Separate Transmit and Receive Interrupts
- Loopback mode for Diagnostic Support
- Polarity Control for Transmit and Receive Lines
- Support for Sync and Break Characters
- Supports Automatic Baud Rate Detection
- IrDA® Encoder and Decoder Logic
- Includes DMA Support
- 16x Baud Clock Output for IrDA Support

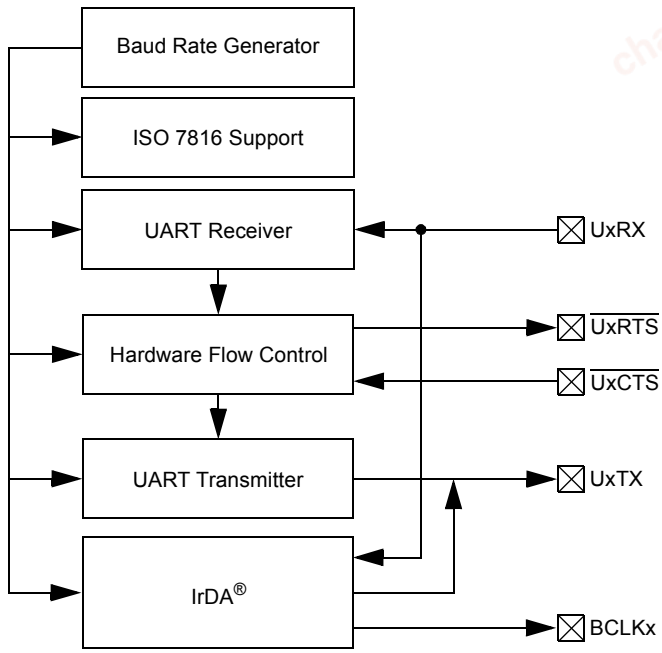
A simplified block diagram of the UARTx module is shown in Figure 17-1. The UARTx module consists of these key important hardware elements:

- Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

Note: Throughout this section, references to register and bit names that may be associated with a specific UART module are referred to generically by the use of 'x' in place of the specific module number. Thus, "UxSTA" might refer to the UART Status register for either UART module (UART1 or UART2).

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Figure 17-1. UART Simplified Block Diagram



Note: The UART inputs and outputs must all be assigned to available RPn/RPIn pins before use. See 11.4 Peripheral Pin Select (PPS) for more information.

17.1 UART Baud Rate Generator (BRG)

The UART module includes a dedicated, 16-bit Baud Rate Generator. The UxBRG register controls the period of a free-running, 16-bit timer. Equation 17-1 shows the formula for computation of the baud rate when BRGH = 0.

Equation 17-1. UART Baud Rate with BRGH = 0(1)

$$\text{Baud Rate} = \frac{F_{PB}}{16 \bullet (\text{UxBRG} + 1)}$$

$$\text{UxBRG} = \frac{F_{PB}}{16 \bullet \text{Baud Rate}} - 1$$

Note:

1. F_{PB} denotes the Peripheral Clock Frequency ($F_{OSC}/2$).

Equation 17-2 shows the formula for computation of the baud rate when BRGH = 1.

Equation 17-2. UART Baud Rate with BRGH = 1(1)

$$\text{Baud Rate} = \frac{F_{PB}}{4 \bullet (\text{UxBRG} + 1)}$$

$$\text{UxBRG} = \frac{F_{PB}}{4 \bullet \text{Baud Rate}} - 1$$

Note:

1. F_{PB} denotes the Peripheral Clock Frequency ($F_{OSC}/2$).

Writing a new value to the UxBRG register causes the BRG timer to be reset (cleared). This ensures the BRG does not wait for a timer overflow before generating the new baud rate.

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17.2 Transmitting in 8-Bit Data Mode

1. Write appropriate baud rate value to the UxBRG register.
2. Enable the UART.
3. Set the UTXEN bit (causes a transmit interrupt, two cycles after being set).
4. Write a data byte to the lower byte of the UxTXREG word. The value will be immediately transferred to the Transmit Shift Register (TSR) and the serial bit stream will start shifting out with the next rising edge of the baud clock.
5. Alternatively, the data byte may be transferred while UTXEN = 0 and then the user may set UTXEN. This will cause the serial bit stream to begin immediately because the baud clock will start from a cleared state.
6. A transmit interrupt will be generated as per interrupt control bits, UTXISEL[1:0].

17.3 Transmitting in 9-Bit Data Mode

1. Write appropriate baud rate value to the UxBRG register.
2. Enable the UART.
3. Set the UTXEN bit (causes a transmit interrupt).
4. Write UxTXREG as a 16-bit value only. A word write to UxTXREG triggers the transfer of the 9-bit data to the TSR. The serial bit stream will start shifting out with the first rising edge of the baud clock.
5. A transmit interrupt will be generated as per the setting of control bits, UTXISELx.

17.4 Break and Sync Transmit Sequence

The following sequence will send a message frame header, made up of a Break, followed by an auto-baud Sync byte.

1. Configure the UART for the desired mode.
2. Set UTXEN and UTXBRK to set up the Break character.
3. Load the UxTXREG with a dummy character to initiate transmission (value is ignored).
4. Write ‘55h’ to UxTXREG; this loads the Sync character into the transmit FIFO.
5. After the Break has been sent, the UTXBRK bit is reset by hardware. The Sync character now transmits.

17.5 Receiving in 8-Bit or 9-Bit Data Mode

1. Write appropriate baud rate value to the UxBRG register.
2. Enable the UART by setting the URXEN bit (UxSTA[12]).
3. A receive interrupt will be generated when one or more data characters have been received as per interrupt control bits, URXISEL[1:0].
4. Read the OERR bit to determine if an overrun error has occurred. The OERR bit must be reset in software.
5. Read UxRXREG.

The act of reading the UxRXREG character will move the next character to the top of the receive FIFO, including a new set of PERR and FERR values.

17.6 Operation of $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Control Pins

UARTx Clear-to-Send ($\overline{\text{UxCTS}}$) and Request-to-Send ($\overline{\text{UxRTS}}$) are the two hardware controlled pins that are associated with the UARTx modules. These two pins allow the UARTx to operate in Simplex and Flow Control mode. They are implemented to control the transmission and reception between the Data Terminal Equipment (DTE). The UEN[1:0] bits in the UxMODE register configure these pins.

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17.7 Infrared Support

The UART module provides two types of infrared UART support: one is the IrDA clock output to support an external IrDA encoder and decoder device (legacy module support), and the other is the full implementation of the IrDA encoder and decoder. Note that because the IrDA modes require a 16x baud clock, they will only work when the BRGH bit (UxMODE[3]) is '0'.

17.7.1 IrDA Clock Output for External IrDA Support

To support external IrDA encoder and decoder devices, the BCLKx pin (same as the $\overline{\text{UxRTS}}$ pin) can be configured to generate the 16x baud clock. When UEN[1:0] = 11, the BCLKx pin will output the 16x baud clock if the UARTx module is enabled; it can be used to support the IrDA codec chip.

17.7.2 Built-in IrDA Encoder and Decoder

The UARTx has full implementation of the IrDA encoder and decoder as part of the UARTx module. The built-in IrDA encoder and decoder functionality is enabled using the IREN bit (UxMODE[12]). When enabled (IREN = 1), the receive pin (UxRX) acts as the input from the infrared receiver. The transmit pin (UxTX) acts as the output to the infrared transmitter.

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17.8 UART Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x0397	Reserved									
0x0398	U1MODE	7:0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL[1:0]		STSEL
		15:8	UARTEN		USIDL	IREN	RTSMD		UEN[1:0]	
0x039A	U1STA	7:0	URXISEL[1:0]		ADDEN	RIDLE	PERR	FERR	OERR	URXDA
		15:8	UTXISEL1	UTXINV	UTXISEL0	URXEN	UTXBRK	UTXEN	UTXBF	TRMT
0x039C	U1TXREG	7:0	U1TXREG[7:0]							
		15:8								U1TXREG[8]
0x039E	U1RXREG	7:0	U1RXREG[7:0]							
		15:8								U1RXREG[8]
0x03A0	U1BRG	7:0	BRG[7:0]							
		15:8	BRG[15:8]							
0x03A2 ... 0x03AD	Reserved									
0x03AE	U2MODE	7:0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL[1:0]		STSEL
		15:8	UARTEN		USIDL	IREN	RTSMD		UEN[1:0]	
0x03B0	U2STA	7:0	URXISEL[1:0]		ADDEN	RIDLE	PERR	FERR	OERR	URXDA
		15:8	UTXISEL1	UTXINV	UTXISEL0	URXEN	UTXBRK	UTXEN	UTXBF	TRMT
0x03B2	U2TXREG	7:0	U2TXREG[7:0]							
		15:8								U2TXREG[8]
0x03B4	U2RXREG	7:0	U2RXREG[7:0]							
		15:8								U2RXREG[8]
0x03B6	U2BRG	7:0	BRG[7:0]							
		15:8	BRG[15:8]							

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17.8.1 UART1 Mode Register

Name: U1MODE
Offset: 0x398

Note:

1. If UARTEN = 1, the peripheral inputs and outputs must be configured to an available RPn/RPIn pin. For more information, see 11.4 Peripheral Pin Select (PPS).
2. This feature is only available for the 16x BRG mode (BRGH = 0).
3. This feature should be used only when PLLEN (CLKDIV[5]) = 1.

Bit	15	14	13	12	11	10	9	8
	UARTEN		USIDL	IREN	RTSMD		UEN[1:0]	
Access	R/W		R/W	R/W	R/W		R/W	R/W
Reset	0		0	0	0		0	0

Bit	7	6	5	4	3	2	1	0
	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL[1:0]		STSEL
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – UARTEN UART Enable bit(1)

Value	Description
1	UART is enabled; all UART pins are controlled by UART as defined by UEN[1:0]
0	UART is disabled; all UART pins are controlled by port latches, UART power consumption is minimal

Bit 13 – USIDL UART Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode
0	Continues module operation in Idle mode

Bit 12 – IREN IrDA® Encoder and Decoder Enable bit(2)

Value	Description
1	IrDA encoder and decoder are enabled
0	IrDA encoder and decoder are disabled

Bit 11 – RTSMD Mode Selection for $\overline{\text{U1RTS}}$ Pin bit

Value	Description
1	$\overline{\text{U1RTS}}$ pin is in Simplex mode
0	$\overline{\text{U1RTS}}$ pin is in Flow Control mode

Bits 9:8 – UEN[1:0] UART Enable bits

Value	Description
11	U1TX, U1RX and BCLK1 pins are enabled and used; $\overline{\text{U1CTS}}$ pin is controlled by port latches
10	U1TX, U1RX, $\overline{\text{U1CTS}}$ and $\overline{\text{U1RTS}}$ pins are enabled and used
01	U1TX, U1RX and $\overline{\text{U1RTS}}$ pins are enabled and used; $\overline{\text{U1CTS}}$ pin is controlled by port latches
00	U1TX and U1RX pins are enabled and used; $\overline{\text{U1CTS}}$ and $\overline{\text{U1RTS}}$/BCLK1 pins are controlled by port latches

Bit 7 – WAKE Wake-up on Start Bit Detect During Sleep Mode Enable bit(3)

Value	Description
1	UART continues to sample the U1RX pin; interrupt is generated on the falling edge, bit is cleared in hardware on the following rising edge
0	No wake-up is enabled

Bit 6 – LPBACK UART Loopback Mode Select bit

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Value	Description
1	Enables Loopback mode
0	Loopback mode is disabled

Bit 5 – ABAUD Auto-Baud Enable bit

Value	Description
1	Enables baud rate measurement on the next character – requires reception of a Sync field (55h); cleared in hardware upon completion
0	Baud rate measurement is disabled or completed

Bit 4 – URXINV UART Receive Polarity Inversion bit

Value	Description
1	U1RX Idle state is '0'
0	U1RX Idle state is '1'

Bit 3 – BRGH High Baud Rate Enable bit

Value	Description
1	High-Speed mode (4 BRG clock cycles per bit)
0	Standard Speed mode (16 BRG clock cycles per bit)

Bits 2:1 – PDSEL[1:0] Parity and Data Selection bits

Value	Description
11	9-bit data, no parity
10	8-bit data, odd parity
01	8-bit data, even parity
00	8-bit data, no parity

Bit 0 – STSEL Stop Bit Selection bit

Value	Description
1	Two Stop bits
0	One Stop bit

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17.8.2 UART1 Status and Control Register

Name: U1STA
Offset: 0x39A

C = Clearable bit; HSC = Hardware Settable/Clearable bit

Note:

1. The value of this bit only affects the transmit properties of the module when the IrDA® encoder is enabled (IREN = 1).
2. If UARTEN = 1, the peripheral inputs and outputs must be configured to an available RPn/RPIn pin. For more information, see 11.4 Peripheral Pin Select (PPS).

Legend: C = Clearable bit; HC = Hardware Clearable bit; HS = Hardware Settable bit; HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
	UTXISEL1	UTXINV	UTXISEL0	URXEN	UTXBRK	UTXEN	UTXBF	TRMT
Access	R/W	R/W	R/W	R/W	HC/R/W	R/W	HSC/R	HSC/R
Reset	0	0	0	0	0	0	0	1

Bit	7	6	5	4	3	2	1	0
	URXISEL[1:0]		ADDEN	RIDLE	PERR	FERR	OERR	URXDA
Access	R/W	R/W	R/W	HSC/R	HSC/R	HSC/R	HS/R/C	HSC/R
Reset	0	0	0	1	0	0	0	0

Bit 15 – UTXISEL1 UART Transmission Interrupt Mode Selection bit

Value of UTXISEL[1:0]	Description
11	Reserved; do not use
10	Interrupt when a character is transferred to the Transmit Shift Register (TSR), and as a result, the transmit buffer becomes empty
01	Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
00	Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)

Bit 14 – UTXINV UART IrDA® Encoder Transmit Polarity Inversion bit(1)

IREN = 1:

Value	Description
1	U1TX Idle state is '1'
0	U1TX Idle state is '0'

IREN = 0:

Value	Description
1	U1TX Idle state is '0'
0	U1TX Idle state is '1'

Bit 13 – UTXISEL0 UART Transmission Interrupt Mode Selection bit
See description of bit 15 – UTXISEL1.

Bit 12 – URXEN UART Receive Enable bit

Value	Description
1	Receive is enabled, U1RX pin is controlled by UART

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Value	Description
0	Receive is disabled, U1RX pin is controlled by the port

Bit 11 – UTXBRK UART Transmit Break bit

Value	Description
1	Sends Sync Break on next transmission – Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
0	Sync Break transmission is disabled or completed

Bit 10 – UTXEN UART Transmit Enable bit(2)

Value	Description
1	Transmit is enabled, U1TX pin is controlled by UART
0	Transmit is disabled, any pending transmission is aborted and the buffer is reset; U1TX pin is controlled by the port

Bit 9 – UTXBF UART Transmit Buffer Full Status bit (read-only)

Value	Description
1	Transmit buffer is full
0	Transmit buffer is not full, at least one more character can be written

Bit 8 – TRMT Transmit Shift Register Empty bit (read-only)

Value	Description
1	Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
0	Transmit Shift Register is not empty, a transmission is in progress or queued

Bits 7:6 – URXISEL[1:0] UART Receive Interrupt Mode Selection bits

Value	Description
11	Interrupt is set on an RSR transfer, making the receive buffer full (i.e., has four data characters)
10	Interrupt is set on an RSR transfer, making the receive buffer 3/4 full (i.e., has three data characters)
0x	Interrupt is set when any character is received and transferred from the RSR to the receive buffer; receive buffer has one or more characters

Bit 5 – ADDEN Address Character Detect bit (bit 8 of received data = 1)

Value	Description
1	Address Detect mode is enabled (if 9-bit mode is not selected, this does not take effect)
0	Address Detect mode is disabled

Bit 4 – RIDLE Receiver Idle bit (read-only)

Value	Description
1	Receiver is Idle
0	Receiver is active

Bit 3 – PERR Parity Error Status bit (read-only)

Value	Description
1	Parity error has been detected for the current character (the character at the top of the receive FIFO)
0	Parity error has not been detected

Bit 2 – FERR Framing Error Status bit (read-only)

Value	Description
1	Framing error has been detected for the current character (the character at the top of the receive FIFO)
0	Framing error has not been detected

Bit 1 – OERR Receive Buffer Overrun Error Status bit (clear/read-only)

Value	Description
1	Receive buffer has overflowed

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Value	Description
0	Receive buffer has not overflowed (clearing a previously set OERR bit ('1' to '0' transition) will reset the receive buffer and the RSR to the empty state)

Bit 0 – URXDA UART Receive Buffer Data Available bit (read-only)

Value	Description
1	Receive buffer has data, at least one more character can be read
0	Receive buffer is empty

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17.8.3 UART1 Transmit Register (Normally Write-Only)

Name: U1TXREG
Offset: 0x39C

Bit	15	14	13	12	11	10	9	8
								U1TXREG[8]
Access								W
Reset								0

Bit	7	6	5	4	3	2	1	0
	U1TXREG[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	x

Bits 8:0 – U1TXREG[8:0] UART1 Transmission Data bits

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17.8.4 UART1 Receive Register (Normally Read-Only)

Name: U1RXREG
Offset: 0x39E

Bit	15	14	13	12	11	10	9	8
								U1RXREG[8]
Access								R
Reset								0

Bit	7	6	5	4	3	2	1	0
	U1RXREG[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 8:0 – U1RXREG[8:0] UART1 Receive Data bits

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17.8.5 UART1 Baud Rate Generator Register

Name: U1BRG
Offset: 0x3A0

Bit	15	14	13	12	11	10	9	8
	BRG[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BRG[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – BRG[15:0] UART1 Baud Rate Divisor bits

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17.8.6 UART2 Mode Register

Name: U2MODE
Offset: 0x3AE

Note:

1. If UARTEN = 1, the peripheral inputs and outputs must be configured to an available RPn/RPIn pin. For more information, see 11.4 Peripheral Pin Select (PPS).
2. This feature is only available for the 16x BRG mode (BRGH = 0).
3. This feature should be used only when PLLEN (CLKDIV[5] = 1.

Bit	15	14	13	12	11	10	9	8
	UARTEN		USIDL	IREN	RTSMD		UEN[1:0]	
Access	R/W		R/W	R/W	R/W		R/W	R/W
Reset	0		0	0	0		0	0

Bit	7	6	5	4	3	2	1	0
	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL[1:0]		STSEL
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – UARTEN UART Enable bit(1)

Value	Description
1	UART is enabled; all UART pins are controlled by UART as defined by UEN[1:0]
0	UART is disabled; all UART pins are controlled by port latches, UART power consumption is minimal

Bit 13 – USIDL UART Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode
0	Continues module operation in Idle mode

Bit 12 – IREN IrDA® Encoder and Decoder Enable bit(2)

Value	Description
1	IrDA encoder and decoder are enabled
0	IrDA encoder and decoder are disabled

Bit 11 – RTSMD Mode Selection for $\overline{\text{U2RTS}}$ Pin bit

Value	Description
1	$\overline{\text{U2RTS}}$ pin is in Simplex mode
0	$\overline{\text{U2RTS}}$ pin is in Flow Control mode

Bits 9:8 – UEN[1:0] UART Enable bits

Value	Description
11	U2TX, U2RX and BCLK2 pins are enabled and used; $\overline{\text{U2CTS}}$ pin is controlled by port latches
10	U2TX, U2RX, $\overline{\text{U2CTS}}$ and $\overline{\text{U2RTS}}$ pins are enabled and used
01	U2TX, U2RX and $\overline{\text{U2RTS}}$ pins are enabled and used; $\overline{\text{U2CTS}}$ pin is controlled by port latches
00	U2TX and U2RX pins are enabled and used; $\overline{\text{U2CTS}}$ and $\overline{\text{U2RTS}}$/BCLK2 pins are controlled by port latches

Bit 7 – WAKE Wake-up on Start Bit Detect During Sleep Mode Enable bit(3)

Value	Description
1	UART continues to sample the U2RX pin; interrupt is generated on the falling edge, bit is cleared in hardware on the following rising edge
0	No wake-up is enabled

Bit 6 – LPBACK UART Loopback Mode Select bit

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Value	Description
1	Enables Loopback mode
0	Loopback mode is disabled

Bit 5 – ABAUD Auto-Baud Enable bit

Value	Description
1	Enables baud rate measurement on the next character – requires reception of a Sync field (55h); cleared in hardware upon completion
0	Baud rate measurement is disabled or completed

Bit 4 – URXINV UART Receive Polarity Inversion bit

Value	Description
1	U2RX Idle state is '0'
0	U2RX Idle state is '1'

Bit 3 – BRGH High Baud Rate Enable bit

Value	Description
1	High-Speed mode (4 BRG clock cycles per bit)
0	Standard Speed mode (16 BRG clock cycles per bit)

Bits 2:1 – PDSEL[1:0] Parity and Data Selection bits

Value	Description
11	9-bit data, no parity
10	8-bit data, odd parity
01	8-bit data, even parity
00	8-bit data, no parity

Bit 0 – STSEL Stop Bit Selection bit

Value	Description
1	Two Stop bits
0	One Stop bit

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17.8.7 UART2 Status and Control Register

Name: U2STA
Offset: 0x3B0

Note:

1. The value of this bit only affects the transmit properties of the module when the IrDA® encoder is enabled (IREN = 1).
2. If UARTEN = 1, the peripheral inputs and outputs must be configured to an available RPn/RPIn pin. For more information, see 11.4 Peripheral Pin Select (PPS).

Legend: C = Clearable bit; HC = Hardware Clearable bit; HS = Hardware Settable bit; HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
	UTXISEL1	UTXINV	UTXISEL0	URXEN	UTXBRK	UTXEN	UTXBF	TRMT
Access	R/W	R/W	R/W	R/W	HC/R/W	R/W	HSC/R	HSC/R
Reset	0	0	0	0	0	0	0	1

Bit	7	6	5	4	3	2	1	0
	URXISEL[1:0]		ADDEN	RIDLE	PERR	FERR	OERR	URXDA
Access	R/W	R/W	R/W	HSC/R	HSC/R	HSC/R	HS/R/C	HSC/R
Reset	0	0	0	1	0	0	0	0

Bit 15 – UTXISEL1 UART Transmission Interrupt Mode Selection bit

Value of UTXISEL[1:0]	Description
11	Reserved; do not use
10	Interrupt when a character is transferred to the Transmit Shift Register (TSR), and as a result, the transmit buffer becomes empty
01	Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
00	Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)

Bit 14 – UTXINV UART IrDA® Encoder Transmit Polarity Inversion bit(1)
IREN = 1:

Value	Description
1	U2TX Idle state is '1'
0	U2TX Idle state is '0'

IREN = 0:

Value	Description
1	U2TX Idle state is '0'
0	U2TX Idle state is '1'

Bit 13 – UTXISEL0 UART Transmission Interrupt Mode Selection bit
See description of bit 15 – UTXISEL1.

Bit 12 – URXEN UART Receive Enable bit

Value	Description
1	Receive is enabled, U2RX pin is controlled by UART
0	Receive is disabled, U2RX pin is controlled by the port

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Bit 11 – UTXBRK UART Transmit Break bit

Value	Description
1	Sends Sync Break on next transmission – Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
0	Sync Break transmission is disabled or completed

Bit 10 – UTXEN UART Transmit Enable bit(2)

Value	Description
1	Transmit is enabled, U2TX pin is controlled by UART
0	Transmit is disabled, any pending transmission is aborted and the buffer is reset; U2TX pin is controlled by the port

Bit 9 – UTXBF UART Transmit Buffer Full Status bit (read-only)

Value	Description
1	Transmit buffer is full
0	Transmit buffer is not full, at least one more character can be written

Bit 8 – TRMT Transmit Shift Register Empty bit (read-only)

Value	Description
1	Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
0	Transmit Shift Register is not empty, a transmission is in progress or queued

Bits 7:6 – URXISEL[1:0] UART Receive Interrupt Mode Selection bits

Value	Description
11	Interrupt is set on an RSR transfer, making the receive buffer full (i.e., has four data characters)
10	Interrupt is set on an RSR transfer, making the receive buffer 3/4 full (i.e., has three data characters)
0x	Interrupt is set when any character is received and transferred from the RSR to the receive buffer; receive buffer has one or more characters

Bit 5 – ADDEN Address Character Detect bit (bit 8 of received data = 1)

Value	Description
1	Address Detect mode is enabled (if 9-bit mode is not selected, this does not take effect)
0	Address Detect mode is disabled

Bit 4 – RIDLE Receiver Idle bit (read-only)

Value	Description
1	Receiver is Idle
0	Receiver is active

Bit 3 – PERR Parity Error Status bit (read-only)

Value	Description
1	Parity error has been detected for the current character (the character at the top of the receive FIFO)
0	Parity error has not been detected

Bit 2 – FERR Framing Error Status bit (read-only)

Value	Description
1	Framing error has been detected for the current character (the character at the top of the receive FIFO)
0	Framing error has not been detected

Bit 1 – OERR Receive Buffer Overrun Error Status bit (clear/read-only)

Value	Description
1	Receive buffer has overflowed
0	Receive buffer has not overflowed (clearing a previously set OERR bit ('1' to '0' transition) will reset the receive buffer and the RSR to the empty state)

Bit 0 – URXDA UART Receive Buffer Data Available bit (read-only)

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Value	Description
1	Receive buffer has data, at least one more character can be read
0	Receive buffer is empty

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17.8.8 UART2 Transmit Register (Normally Write-Only)

Name: U2TXREG
Offset: 0x3B2

Bit	15	14	13	12	11	10	9	8
								U2TXREG[8]
Access								W
Reset								0

Bit	7	6	5	4	3	2	1	0
	U2TXREG[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	x

Bits 8:0 – U2TXREG[8:0] UART2 Transmission Data bits

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17.8.9 UART2 Receive Register (Normally Read-Only)

Name: U2RXREG
Offset: 0x3B4

Bit	15	14	13	12	11	10	9	8
								U2RXREG[8]
Access								R
Reset								0

Bit	7	6	5	4	3	2	1	0
	U2RXREG[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 8:0 – U2RXREG[8:0] UART2 Receive Data bits

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17.8.10 UART2 Baud Rate Generator Register

Name: U2BRG
Offset: 0x3B6

Bit	15	14	13	12	11	10	9	8
	BRG[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BRG[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – BRG[15:0] UART2 Baud Rate Divisor bits

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18. Real-Time Clock and Calendar (RTCC) with Timestamp

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Real-Time Clock and Calendar, refer to **"RTCC with Timestamp"** (www.microchip.com/DS70005193) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

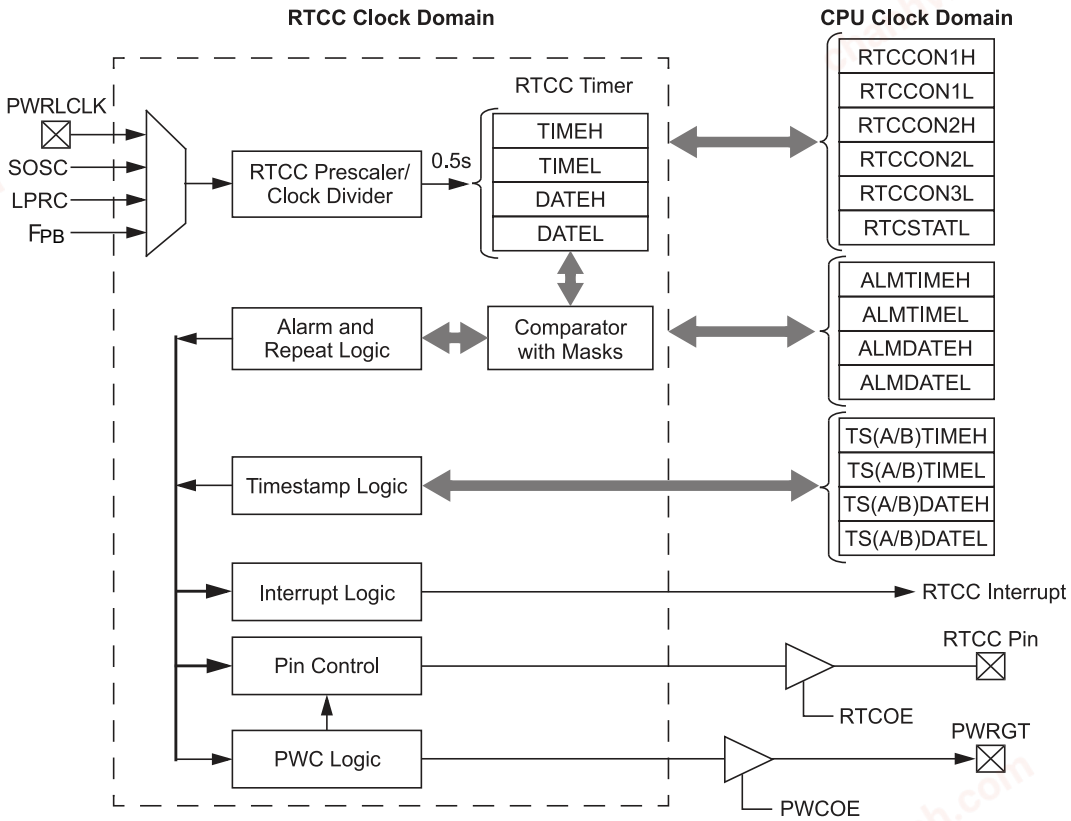
The RTCC provides the user with a Real-Time Clock and Calendar (RTCC) function that can be calibrated.

Key features of the RTCC module are:

- Selectable Clock Source
- Provides Hours, Minutes and Seconds Using 24-Hour Format
- Visibility of One Half Second Period
- Provides Calendar – Weekday, Date, Month and Year
- Alarm-Configurable for Half a Second, 1 Second, 10 Seconds, 1 Minute, 10 Minutes, 1 Hour, 1 Day, 1 Week, 1 Month or 1 Year
- Alarm Repeat with Decrementing Counter
- Alarm with Indefinite Repeat Chime
- Year 2000 to 2099 Leap Year Correction
- BCD Format for Smaller Software Overhead
- Optimized for Long-Term Battery Operation
- User Calibration of the 32.768 kHz Clock Crystal/32 kHz LPRC Frequency with Periodic Auto-Adjust
- Fractional Second Synchronization
- Calibration to within ±2.64 Seconds Error per Month
- Calibrates Up to 260 ppm of Crystal Error
- Ability to Periodically Wake-up External Devices without CPU Intervention (external power control)
- Power Control Output for External Circuit Control
- Calibration takes Effect Every 15 Seconds
- Timestamp Capture register for Time and Date
- Programmable Prescaler and Clock Divider Circuit allows Operation with Any Clock Source Up to 32 MHz, Including 32.768 kHz Crystal, 50/60 Hz Powerline Clock, External Real-Time Clock (RTC) or 32 kHz LPRC Clock

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Figure 18-1. RTCC Block Diagram



18.1 RTCC Source Clock

The RTCC clock divider block converts the incoming oscillator source into accurate 1/2 and 1 second clocks for the RTCC. The clock divider is optimized to work with three different oscillator sources:

- 32.768 kHz Crystal Oscillator
- 32 kHz Low-Power RC Oscillator (LPRC)
- External 50 Hz or 60 Hz Powerline Frequency

An asynchronous prescaler, PS[1:0] (RTCCON2L[5:4]), is provided that allows the RTCC to work with higher speed clock sources, such as the peripheral clock. Divide ratios of 1:16, 1:64 or 1:256 may be selected, allowing sources of up to 16 MHz to clock the RTCC.

18.1.1 Coarse Frequency Division

The clock divider block has a 16-bit counter used to divide the input clock frequency. The divide ratio is set by the DIV[15:0] register bits (RTCCON2H[15:0]). The DIV[15:0] bits should be programmed with a value to produce a nominal 1/2 second clock divider count period.

18.1.2 Fine Frequency Division

The fine frequency division is set using the FDIV[4:0] bits (RTCCON2L[15:11]). Increasing the FDIVx value will lengthen the overall clock divider period.

If FDIV[4:0] = `00000`, the fine frequency division circuit is effectively disabled. Otherwise, it will optionally remove a clock pulse from the input of the clock divider every 1/2 second. This functionality will allow the user to remove up to 31 pulses over a fixed period of 16 seconds, depending on the value of FDIVx.

The value for DIV[15:0] is calculated as shown in Equation 18-1. The fractional remainder of the DIV[15:0] calculation result can be used to calculate the value for FDIV[4:0].

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Equation 18-1. RTCC Clock Divider Output Frequency

$$FOUT = \frac{FIN}{2 \bullet (PS[1:0]\ Prescaler) \bullet (DIV[15:0] + 1) + \left(\frac{FDIV[4:0]}{32}\right)}$$

The DIV[15:0] value is the integer part of this calculation:

$$DIV[15:0] = \frac{FIN}{2 \bullet (PS[1:0]\ Prescaler)} - 1$$

The FDIV[4:0] value is the fractional part of the DIV[15:0] calculation, multiplied by 32.

18.2 RTCC Module Registers

The RTCC module registers are organized into four categories:

- RTCC Control Registers
- RTCC Value Registers
- Alarm Value Registers
- Timestamp Registers

18.2.1 Register Mapping

Previous RTCC implementations used a Register Pointer to access the RTCC Time and Date registers, as well as the Alarm Time and Date registers. These Registers are now mapped to memory and are individually addressable.

18.2.2 Write Lock

To prevent spurious changes to the Time Control or Time Value registers, the WRLOCK bit (RTCCON1L1[11]) must be cleared (‘0’). The POR default state is when the WRLOCK bit is ‘0’ and is cleared on any device Reset (POR, BOR, $\overline{\text{MCLR}}$). It is recommended that the WRLOCK bit be set to ‘1’ after the Date and Time registers are properly initialized, and after the RTCEN bit (RTCCON1L[15]) has been set.

Any attempt to write to the RTCEN bit, the RTCCON2L/H registers, or the Date or Time registers, will be ignored as long as WRLOCK is ‘1’. The Alarm, Power Control and Timestamp registers can be changed when WRLOCK is ‘1’.

Clearing the WRLOCK bit requires an unlock sequence after it has been written to a ‘1’, writing two bytes consecutively to the NVMKEY register. A sample assembly sequence is shown in Example 18-1. If WRLOCK is already cleared, it can be set to ‘1’ without using the unlock sequence.

Note: To avoid accidental writes to the timer, it is recommended that the WRLOCK bit (RTCCON1L[11]) is kept clear at any other time. For the WRLOCK bit to be set, there is only one instruction cycle time window allowed between the 55h/AA sequence and the setting of WRLOCK; therefore, it is recommended that code follow the procedure in Example 18-1.

Example 18-1. Setting the WRLOCK Bit

```
DISI #6                    ; disable interrupts for 6 instructions
MOV  #NVKEY, W1
MOV  #0x55, W2             ; first unlock code
MOV  W2, [W1]              ; write first unlock code
MOV  #0xAA, W3             ; second unlock sequence
MOV  W3, [W1]              ; write second unlock sequence
BCLR RTCCON1L, #WRLOCK     ; clear the WRLOCK bit
```

18.2.3 Selecting RTCC Clock Source

The clock source for the RTCC module can be selected using the CLKSEL[1:0] bits in the RTCCON2L register. When the bits are set to ‘00’, the Secondary Oscillator (SOSC) is used as the reference clock and when the bits are ‘01’, LPRC is used as the reference clock. When CLKSEL[1:0] = 10, the external powerline (50 Hz and 60 Hz) is used as the clock source. When CLKSEL[1:0] = 11, the system clock is used as the clock source.

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18.3 Calibration

18.3.1 Clock Source Calibration

A crystal oscillator that is connected to the RTCC may be calibrated to provide an accurate one second clock in two ways. First, coarse frequency adjustment is performed by adjusting the value written to the DIV[15:0] bits. Secondly, a 5-bit value can be written to the FDIV[4:0] control bits to perform a fine clock division.

The DIVx and FDIVx values can be concatenated and considered as a 21-bit prescaler value. If the oscillator source is slightly faster than ideal, the FDIV[4:0] value can be increased to make a small decrease in the RTC frequency. The value of DIV[15:0] should be increased to make larger decreases in the RTC frequency. If the oscillator source is slower than ideal, FDIV[4:0] may be decreased for small calibration changes and DIV[15:0] may need to be decreased to make larger calibration changes.

Before calibration, the user must determine the error of the crystal. This should be done using another timer resource on the device or an external timing reference. It is up to the user to include in the error value, the initial error of the crystal, drift due to temperature and drift due to crystal aging.

18.4 Alarm

- Configurable from half second to one year
- Enabled using the ALRMEN bit (RTCCON1H[15])
- One-time alarm and repeat alarm options are available

18.4.1 Configuring the Alarm

The alarm feature is enabled using the ALRMEN bit. This bit is cleared when an alarm is issued. Writes to the Alarm Value registers should only take place when ALRMEN = 0.

As shown in Figure 18-2, the interval selection of the alarm is configured through the AMASK[3:0] bits (RTCCON1H[11:8]). These bits determine which and how many digits of the alarm must match the clock value for the alarm to occur.

Figure 18-2. Alarm Mask Settings

Alarm Mask Setting (AMASK[3:0])	Day of the Week	Month	Day	Hours	Minutes	Seconds
0000 - Every half second 0001 - Every second						
0010 - Every 10 seconds						s
0011 - Every minute						s s
0100 - Every 10 minutes					m	s s
0101 - Every hour					m m	s s
0110 - Every day				h h	m m	s s
0111 - Every week	d			h h	m m	s s
1000 - Every month			d d	h h	m m	s s
1001 - Every year(1)		m m	d d	h h	m m	s s

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Note:

1. Annually, except when configured for February 29.

The alarm can also be configured to repeat based on a preconfigured interval. The amount of times this occurs, once the alarm is enabled, is stored in the ALMRPT[7:0] bits (RTCCON1H[7:0]). When the value of the ALMRPTx bits equals 00h and the CHIME bit (RTCCON1H[14]) is cleared, the repeat function is disabled and only a single alarm will occur. The alarm can be repeated, up to 255 times, by loading ALMRPT[7:0] with FFh.

After each alarm is issued, the value of the ALMRPTx bits is decremented by one. Once the value has reached 00h, the alarm will be issued one last time, after which, the ALRMEN bit will be cleared automatically and the alarm will turn off.

Indefinite repetition of the alarm can occur if the CHIME bit = 1. Instead of the alarm being disabled when the value of the ALMRPTx bits reaches 00h, it rolls over to FFh and continues counting indefinitely while CHIME is set.

18.4.2 Alarm Interrupt

At every alarm event, an interrupt is generated. This output is completely synchronous to the RTCC clock and can be used as a trigger clock to the other peripherals.

Note: Changing any of the register bits, other than the RTCOE bit (RTCCON1L[7]), the ALMRPT[7:0] bits (RTCCON1H[7:0] and the CHIME bit, while the alarm is enabled (ALRMEN = 1), can result in a false alarm event leading to a false alarm interrupt. To avoid a false alarm event, the timer and alarm values should only be changed while the alarm is disabled (ALRMEN = 0).

18.5 Power Control

The RTCC includes a power control feature that allows the device to periodically wake-up an external device, wait for the device to be stable before sampling wake-up events from that device and then shut down the external device. This can be done completely autonomously by the RTCC, without the need to wake-up from the current lower power mode.

To use this feature:

1. Enable the RTCC (RTCEN = 1).
2. Set the PWCEN bit (RTCCON1L[10]).
3. Configure the RTCC pin to drive the PWC control signal (RTCOE = 1 and OUTSEL[2:0] = 011).

The polarity of the PWC control signal may be chosen using the PWCPOL bit (RTCCON1L[9]). An active-low or active-high signal may be used with the appropriate external switch to turn on or off the power to one or more external devices. The active-low setting may also be used in conjunction with an open-drain setting on the RTCC pin, in order to drive the ground pin(s) of the external device directly (with the appropriate external V_{DD} pull-up device), without the need for external switches. Finally, the CHIME bit should be set to enable the PWC periodicity.

Once the RTCC and PWC are enabled and running, the PWC logic will generate a control output and a sample gate output. The control output is driven out on the RTCC pin (when RTCOE = 1 and OUTSEL[2:0] = 011) and is used to power up or down the device, as described above.

Once the control output is asserted, the stability window begins, in which the external device is given enough time to power up and provide a stable output.

Once the output is stable, the RTCC provides a sample gate during the sample window. The use of this sample gate depends on the external device being used, but typically, it is used to mask out one or more wake-up signals from the external device.

Finally, both the stability and the sample windows close after the expiration of the sample window and the external device is powered down.

18.5.1 Power Control Clock Source

The stability and sample windows are controlled by the PWCSAMPx and PWCSTABx bit fields in the RTCCON3L register (RTCCON3L[15:8] and [7:0], respectively). As both the stability and sample windows are defined in terms of the RTCC clock, their absolute values vary by the value of the PWC clock base period (T_{PWCCLK}). For example, using a 32.768 kHz SOSC input clock would produce a T_{PWCCLK} of 1/32768 = 30.518 µs. The 8-bit magnitude of

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PWCSTABx and PWCSAMPx allows for a window size of 0 to 255 T_{PWCCLK}. The period of the PWC clock can also be adjusted with a 1:1, 1:16, 1:64 or 1:256 prescaler, determined by the PWCPS[1:0] bits (RTCCON2L[7:6]).

In addition, certain values for the PWCSTABx and PWCSAMPx fields have specific control meanings in determining power control operations. If either bit field is 00h, the corresponding window is inactive. In addition, if the PWCSTABx field is FFh, the stability window remains active continuously, even if power control is disabled.

18.6 Event Timestamping

The RTCC includes a set of Timestamp registers that may be used for the capture of Time and Date register values when an external input signal is received. The RTCC will trigger a timestamp event when a low pulse occurs on the $\overline{\text{TMPRN}}$ pin.

18.6.1 Timestamp Operation

The event input is enabled for timestamping using the TSAEN bit (RTCCON1L[0]). When the timestamp event occurs, the present time and date values will be stored in the TSATIMEL/H and TSADATEL/H registers, the TSAEVT status bit (RTCSTATL[3]) will be set and an RTCC interrupt will occur. A new timestamp capture event cannot occur until the user clears the TSAEVT status bit.

The TSATIMEL/H and TSADATEL/H register pairs can be used for data storage when TSAEN = 0. The values of TSATIMEL/H and TSADATEL/H will be maintained throughout all types of non-Power-on Resets ($\overline{\text{MCLR}}$, WDT, etc).

18.6.2 Manual Timestamp Operation

The current time and date may be captured in the TSATIMEL/H and TSADATEL/H registers by writing a '1' to the TSAEVT bit location while the timestamp functionality is enabled (TSAEN = 1). This write will not set the TSAEVT bit, but it will initiate a timestamp capture. The TSAEVT bit will be set when the capture operation is complete. The user must poll the TSAEVT bit to determine when the capture operation is complete.

After the Timestamp registers have been read, the TSAEVT bit should be cleared to allow further hardware or software timestamp capture events.

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18.7 RTCC Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x01CB	Reserved									
0x01CC	RTCCON1L	7:0	RTCOE		OUTSEL[2:0]					TSAEN
		15:8	RTCEN				WRLOCK	PWCEN	PWCPOL	PWCPOE
0x01CE	RTCCON1H	7:0	ALMRPT[7:0]							
		15:8	ALRMEN	CHIME			AMASK[3:0]			
0x01D0	RTCCON2L	7:0	PWCPS[1:0]		PS[1:0]				CLKSEL[1:0]	
		15:8	FDIV[4:0]							
0x01D2	RTCCON2H	7:0	DIV[7:0]							
		15:8	DIV[15:8]							
0x01D4	RTCCON3L	7:0	PWCSTAB[7:0]							
		15:8	PWCSAMP[7:0]							
0x01D6 ... 0x01D7	Reserved									
0x01D8	RTCSTATL	7:0			ALMEVT		TSAEVT	SYNC	ALMSYNC	HALFSEC
		15:8								
0x01DA ... 0x01DB	Reserved									
0x01DC	TIMEL	7:0								
		15:8		SECTEN[2:0]			SECONE[3:0]			
0x01DE	TIMEH	7:0		MINTEN[2:0]			MINONE[3:0]			
		15:8			HRTEN[1:0]		HRONE[3:0]			
0x01E0	DATEL	7:0						WDAY[2:0]		
		15:8			DAYTEN[1:0]		DAYONE[3:0]			
0x01E2	DATEH	7:0				MTHTEN	MTHONE[3:0]			
		15:8	YRTEN[3:0]				YRONE[3:0]			
0x01E4	ALMTIMEL	7:0								
		15:8		SECTEN[2:0]			SECONE[3:0]			
0x01E6	ALMTIMEH	7:0		MINTEN[2:0]			MINONE[3:0]			
		15:8			HRTEN[1:0]		HRONE[3:0]			
0x01E8	ALMDATEL	7:0						WDAY[2:0]		
		15:8			DAYTEN[1:0]		DAYONE[3:0]			
0x01EA	ALMDATEH	7:0				MTHTEN	MTHONE[3:0]			
		15:8	YRTEN[3:0]				YRONE[3:0]			
0x01EC	TSATIMEL(1)	7:0								
		15:8		SECTEN[2:0]			SECONE[3:0]			
0x01EE	TSATIMEH(1)	7:0		MINTEN[2:0]			MINONE[3:0]			
		15:8			HRTEN[1:0]		HRONE[3:0]			
0x01F0	TSADATEL(1)	7:0						WDAY[2:0]		
		15:8			DAYTEN[1:0]		DAYONE[3:0]			
0x01F2	TSADATEH(1)	7:0				MTHTEN	MTHONE[3:0]			
		15:8	YRTEN[3:0]				YRONE[3:0]			

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18.7.1 RTCC Control Register 1 Low

Name: RTCCON1L
Offset: 0x1CC

Bit	15	14	13	12	11	10	9	8
	RTCEN				WRLOCK	PWCEN	PWCPOL	PWCPOE
Access	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RTCOE	OUTSEL[2:0]						TSAEN
Access	R/W	R/W	R/W	R/W				R/W
Reset	0	0	0	0				0

Bit 15 – RTCEN RTCC Enable bit

Value	Description
1	RTCC is enabled and counts from selected clock source
0	RTCC is not enabled

Bit 11 – WRLOCK RTCC Register Write Lock bit

Value	Description
1	RTCC registers are locked
0	RTCC registers may be written to by user

Bit 10 – PWCEN Power Control Enable bit

Value	Description
1	Power control is enabled
0	Power control is disabled

Bit 9 – PWCPOL Power Control Polarity bit

Value	Description
1	Power control output is active-high
0	Power control output is active-low

Bit 8 – PWCPOE Power Control Output Enable bit

Value	Description
1	Power control output pin is enabled
0	Power control output pin is disabled

Bit 7 – RTCOE RTCC Output Enable bit

Value	Description
1	RTCC output is enabled
0	RTCC output is disabled

Bits 6:4 – OUTSEL[2:0] RTCC Output Signal Selection bits

Value	Description
111	Unused
110	Unused
101	Unused
100	Timestamp A event
011	Power control
010	RTCC input clock
001	Second clock
000	Alarm event

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Bit 0 – TSAEN Timestamp A Enable bit

Value	Description
1	Timestamp event will occur when a low pulse is detected on the $\overline{\text{TMPRN}}$ pin
0	Timestamp is disabled

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18.7.2 RTCC Control Register 1 High

Name: RTCCON1H
Offset: 0x1CE

Bit	15	14	13	12	11	10	9	8
	ALRMEN	CHIME			AMASK[3:0]			
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ALMRPT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – ALRMEN Alarm Enable bit

Value	Description
1	Alarm is enabled (cleared automatically after an alarm event whenever ALMRPT[7:0] = 00h and CHIME = 0)
0	Alarm is disabled

Bit 14 – CHIME Chime Enable bit

Value	Description
1	Chime is enabled; ALMRPT[7:0] bits roll over from 00h to FFh
0	Chime is disabled; ALMRPT[7:0] bits stop once they reach 00h

Bits 11:8 – AMASK[3:0] Alarm Mask Configuration bits

Value	Description
11xx	Reserved – do not use
101x	Reserved – do not use
1001	Once a year (except when configured for February 29th, once every four years)
1000	Once a month
0111	Once a week
0110	Once a day
0101	Every hour
0100	Every ten minutes
0011	Every minute
0010	Every ten seconds
0001	Every second
0000	Every half second

Bits 7:0 – ALMRPT[7:0] Alarm Repeat Counter Value bits

Value	Description
11111111	Alarm will repeat 255 more times
. . .	
00000000	Alarm will repeat 0 more times The counter decrements on any alarm event. The counter is prevented from rolling over from '00' to 'FF' unless CHIME = 1.

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18.7.3 RTCC Control Register 2 Low

Name: RTCCON2L
Offset: 0x1D0

Bit	15	14	13	12	11	10	9	8
	FDIV[4:0]							
Access	R/W	R/W	R/W	R/W	R/W			
Reset	0	0	0	0	0			

Bit	7	6	5	4	3	2	1	0
	PWCPS[1:0]		PS[1:0]				CLKSEL[1:0]	
Access	R/W	R/W	R/W	R/W			R/W	R/W
Reset	0	0	0	0			0	0

Bits 15:11 – FDIV[4:0] Fractional Clock Divide bits

Value	Description
11111	Increase period by 31 RTCC input clock cycles every 16 seconds
11101	Increase period by 30 RTCC input clock cycles every 16 seconds
...	
00010	Increase period by 2 RTCC input clock cycles every 16 seconds
00001	Increase period by 1 RTCC input clock cycle every 16 seconds
00000	No fractional clock division

Bits 7:6 – PWCPS[1:0] Power Control Prescale Select bits

Value	Description
11	1:256
10	1:64
01	1:16
00	1:1

Bits 5:4 – PS[1:0] Prescale Select bits

Value	Description
11	1:256
10	1:64
01	1:16
00	1:1

Bits 1:0 – CLKSEL[1:0] Clock Select bits

Value	Description
11	Peripheral clock
10	PWRLCLK pin
01	LPRC
00	SOSC

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18.7.4 RTCC Control Register 2 High

Name: RTCCON2H
Offset: 0x1D2

Note:

1. A write to this register is only allowed when WRLOCK = 1.

Bit	15	14	13	12	11	10	9	8
	DIV[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DIV[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – DIV[15:0] Clock Divide bits(1)
Sets the period of the clock divider counter; value should cause a nominal 1/2 second underflow.

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18.7.5 RTCC Control Register 3 Low

Name: RTCCON3L
Offset: 0x1D4

Note:
1. The sample window always starts when the stability window timer expires, except when its initial value is 00h.

Bit	15	14	13	12	11	10	9	8
	PWCSAMP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PWCSTAB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – PWCSAMP[7:0] Power Control Sample Window Timer bits

Value	Description
11111111	Sample window is always enabled, even when PWCEN = 0
11111110	Sample window is 254 T_{PWCCLK} clock periods
...	
00000001	Sample window is 1 T_{PWCCLK} clock period
00000000	No sample window

Bits 7:0 – PWCSTAB[7:0] Power Control Stability Window Timer bits(1)

Value	Description
11111111	Stability window is 255 T_{PWCCLK} clock periods
11111110	Stability window is 254 T_{PWCCLK} clock periods
...	
00000001	Stability window is 1 T_{PWCCLK} clock period
00000000	No stability window; sample window starts when the alarm event triggers

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18.7.6 RTCC Status Register Low

Name: RTCSTATL
Offset: 0x1D8

Notes:

1. User software may write a '1' to this location to initiate a Timestamp A event; timestamp capture is not valid until TSAEVT reads as '1'.
2. This bit is read-only; it is cleared to '0' on a write to the SECONE[3:0] bits.

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			ALMEVT		TSAEVT	SYNC	ALMSYNC	HALFSEC
Access			R/W		R/W	R/W	R/W	R/W
Reset			0		0	0	0	0

Bit 5 – ALMEVT Alarm Event bit

Value	Description
1	An alarm event has occurred
0	An alarm event has not occurred

Bit 3 – TSAEVT Timestamp A Event bit(1)

Value	Description
1	A timestamp event has occurred
0	A timestamp event has not occurred

Bit 2 – SYNC Synchronization Status bit

Value	Description
1	TIME registers may change during software read
0	TIME registers may be read safely

Bit 1 – ALMSYNC Alarm Synchronization Status bit

Value	Description
1	Alarm registers (ALMTIME and ALMDATE) and Alarm bits (AMASK[3:0]) should not be modified, and Alarm Control bits (ALRMEN, ALMRPT[7:0]) may change during software read
0	Alarm registers and Alarm Control bits may be written/modified safely

Bit 0 – HALFSEC Half Second Status bit(2)

Value	Description
1	Second half period of a second
0	First half period of a second

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18.7.7 RTCC Time Register Low

Name: TIMEL
Offset: 0x1DC

Bit	15	14	13	12	11	10	9	8
		SECTEN[2:0]			SECONE[3:0]			
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 14:12 – SECTEN[2:0] Binary Coded Decimal Value of Seconds '10' Digit bits
Contains a value from 0 to 5.

Bits 11:8 – SECONE[3:0] Binary Coded Decimal Value of Seconds '1' Digit bits
Contains a value from 0 to 9.

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18.7.8 RTCC Time Register High

Name: TIMEH
Offset: 0x1DE

Bit	15	14	13	12	11	10	9	8
			HRTEN[1:0]		HRONE[3:0]			
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		MINTEN[2:0]			MINONE[3:0]			
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 13:12 – HRTEN[1:0] Binary Coded Decimal Value of Hours '10' Digit bits
Contains a value from 0 to 2.

Bits 11:8 – HRONE[3:0] Binary Coded Decimal Value of Hours '1' Digit bits
Contains a value from 0 to 9.

Bits 6:4 – MINTEN[2:0] Binary Coded Decimal Value of Minutes '10' Digit bits
Contains a value from 0 to 5.

Bits 3:0 – MINONE[3:0] Binary Coded Decimal Value of Minutes '1' Digit bits
Contains a value from 0 to 9.

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18.7.9 RTCC Date Register Low

Name: DATEL
Offset: 0x1E0

Bit	15	14	13	12	11	10	9	8
			DAYTEN[1:0]		DAYONE[3:0]			
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
						WDAY[2:0]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 13:12 – DAYTEN[1:0] Binary Coded Decimal Value of Days '10' Digit bits
Contains a value from 0 to 3.

Bits 11:8 – DAYONE[3:0] Binary Coded Decimal Value of Days '1' Digit bits
Contains a value from 0 to 9.

Bits 2:0 – WDAY[2:0] Binary Coded Decimal Value of Weekdays '1' Digit bits
Contains a value from 0 to 6.

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18.7.10 RTCC Date Register High

Name: DATEH
Offset: 0x1E2

Bit	15	14	13	12	11	10	9	8
	YRTEN[3:0]				YRONE[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	x

Bit	7	6	5	4	3	2	1	0
				MTHTEN	MTHONE[3:0]			
Access				R/W	R/W	R/W	R/W	R/W
Reset				x	0	0	0	x

Bits 15:12 – YRTEN[3:0] Binary Coded Decimal Value of Years '10' Digit bits

Bits 11:8 – YRONE[3:0] Binary Coded Decimal Value of Years '1' Digit bits

Bit 4 – MTHTEN Binary Coded Decimal Value of Months '10' Digit bits
Contains a value from 0 to 1.

Bits 3:0 – MTHONE[3:0] Binary Coded Decimal Value of Months '1' Digit bits
Contains a value from 0 to 9.

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18.7.11 RTCC Alarm Time Register Low

Name: ALMTIMEL
Offset: 0x1E4

Bit	15	14	13	12	11	10	9	8
		SECTEN[2:0]			SECONE[3:0]			
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 14:12 – SECTEN[2:0] Binary Coded Decimal Value of Seconds '10' Digit bits
Contains a value from 0 to 5.

Bits 11:8 – SECONE[3:0] Binary Coded Decimal Value of Seconds '1' Digit bits
Contains a value from 0 to 9.

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18.7.12 RTCC Alarm Time Register High

Name: ALMTIMEH
Offset: 0x1E6

Bit	15	14	13	12	11	10	9	8
			HRTEN[1:0]		HRONE[3:0]			
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		MINTEN[2:0]			MINONE[3:0]			
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 13:12 – HRTEN[1:0] Binary Coded Decimal Value of Hours '10' Digit bits
Contains a value from 0 to 2.

Bits 11:8 – HRONE[3:0] Binary Coded Decimal Value of Hours '1' Digit bits
Contains a value from 0 to 9.

Bits 6:4 – MINTEN[2:0] Binary Coded Decimal Value of Minutes '10' Digit bits
Contains a value from 0 to 5.

Bits 3:0 – MINONE[3:0] Binary Coded Decimal Value of Minutes '1' Digit bits
Contains a value from 0 to 9.

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18.7.13 RTCC Alarm Date Register Low

Name: ALMDATEL
Offset: 0x1E8

Bit	15	14	13	12	11	10	9	8
			DAYTEN[1:0]		DAYONE[3:0]			
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
						WDAY[2:0]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 13:12 – DAYTEN[1:0] Binary Coded Decimal Value of Days '10' Digit bits
Contains a value from 0 to 3.

Bits 11:8 – DAYONE[3:0] Binary Coded Decimal Value of Days '1' Digit bits
Contains a value from 0 to 9.

Bits 2:0 – WDAY[2:0] Binary Coded Decimal Value of Weekdays '1' Digit bits
Contains a value from 0 to 6.

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18.7.14 RTCC Alarm Date Register High

Name: ALMDATEH
Offset: 0x1EA

Bit	15	14	13	12	11	10	9	8
	YRTEN[3:0]				YRONE[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				MTHTEN	MTHONE[3:0]			
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 15:12 – YRTEN[3:0] Binary Coded Decimal Value of Years '10' Digit bits

Bits 11:8 – YRONE[3:0] Binary Coded Decimal Value of Years '1' Digit bits

Bit 4 – MTHTEN Binary Coded Decimal Value of Months '10' Digit bits
Contains a value from 0 to 1.

Bits 3:0 – MTHONE[3:0] Binary Coded Decimal Value of Months '1' Digit bits
Contains a value from 0 to 9.

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18.7.15 RTCC Timestamp A Time Register Low

Name: TSATIMEL(1)
Offset: 0x1EC

Note:
1. If TSAEN = 0, bits[15:0] can be used for persistent storage throughout a non-Power-on Reset (MCLR, WDT, etc.).

Bit	15	14	13	12	11	10	9	8
		SECTEN[2:0]			SECONE[3:0]			
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 14:12 – SECTEN[2:0] Binary Coded Decimal Value of Seconds '10' Digit bits
Contains a value from 0 to 5.

Bits 11:8 – SECONE[3:0] Binary Coded Decimal Value of Seconds '1' Digit bits
Contains a value from 0 to 9.

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18.7.16 RTCC Timestamp A Time Register High

Name: TSATIMEH(1)
Offset: 0x1EE

Note:
1. If TSAEN = 0, bits[15:0] can be used for persistent storage throughout a non-Power-on Reset (MCLR, WDT, etc.).

Bit	15	14	13	12	11	10	9	8
			HRTEN[1:0]		HRONE[3:0]			
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		MINTEN[2:0]			MINONE[3:0]			
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 13:12 – HRTEN[1:0] Binary Coded Decimal Value of Hours '10' Digit bits
Contains a value from 0 to 2.

Bits 11:8 – HRONE[3:0] Binary Coded Decimal Value of Hours '1' Digit bits
Contains a value from 0 to 9.

Bits 6:4 – MINTEN[2:0] Binary Coded Decimal Value of Minutes '10' Digit bits
Contains a value from 0 to 5.

Bits 3:0 – MINONE[3:0] Binary Coded Decimal Value of Minutes '1' Digit bits
Contains a value from 0 to 9.

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18.7.17 RTCC Timestamp A Date Register Low

Name: TSADATEL(1)
Offset: 0x1F0

Note:
1. If TSAEN = 0, bits[15:0] can be used for persistent storage throughout a non-Power-on Reset (MCLR, WDT, etc.).

Bit	15	14	13	12	11	10	9	8
			DAYTEN[1:0]		DAYONE[3:0]			
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
						WDAY[2:0]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 13:12 – DAYTEN[1:0] Binary Coded Decimal Value of Days '10' Digit bits
Contains a value from 0 to 3.

Bits 11:8 – DAYONE[3:0] Binary Coded Decimal Value of Days '1' Digit bits
Contains a value from 0 to 9.

Bits 2:0 – WDAY[2:0] Binary Coded Decimal Value of Weekdays '1' Digit bits
Contains a value from 0 to 6.

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18.7.18 RTCC Timestamp A Date Register High

Name: TSADATEH(1)
Offset: 0x1F2

Note:
1. If TSAEN = 0, bits[15:0] can be used for persistent storage throughout a non-Power-on Reset (MCLR, WDT, etc.).

Bit	15	14	13	12	11	10	9	8
	YRTEN[3:0]				YRONE[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				MTHTEN	MTHONE[3:0]			
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 15:12 – YRTEN[3:0] Binary Coded Decimal Value of Years '10' Digit bits

Bits 11:8 – YRONE[3:0] Binary Coded Decimal Value of Years '1' Digit bits

Bit 4 – MTHTEN Binary Coded Decimal Value of Months '10' Digit bits
Contains a value from 0 to 1.

Bits 3:0 – MTHONE[3:0] Binary Coded Decimal Value of Months '1' Digit bits
Contains a value from 0 to 9.

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19. 32-Bit Programmable Cyclic Redundancy Check (CRC) Generator

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to **"32-Bit Programmable Cyclic Redundancy Check (CRC)"** (www.microchip.com/DS30009729) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

The 32-bit programmable CRC generator provides a hardware implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-Programmable CRC Polynomial Equation, Up to 32 Bits
- Programmable Shift Direction (little or big-endian)
- Independent Data and Polynomial Lengths
- Configurable Interrupt Output
- Data FIFO

Figure 19-1 displays a simplified block diagram of the CRC generator. A simple version of the CRC shift engine is displayed in Figure 19-2.

Figure 19-1. CRC Block Diagram

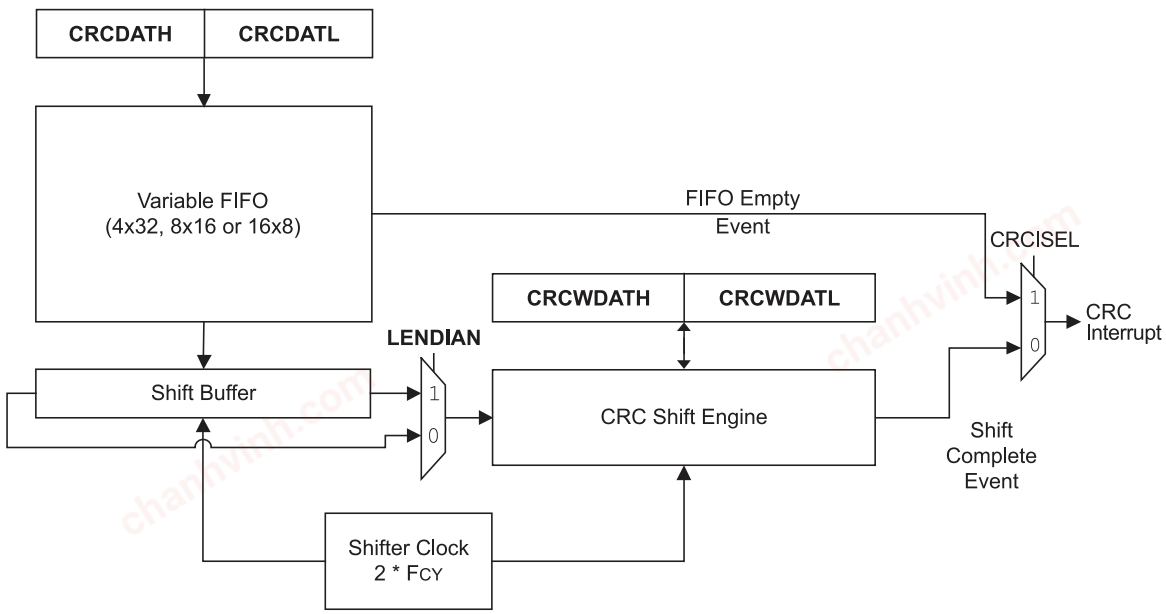
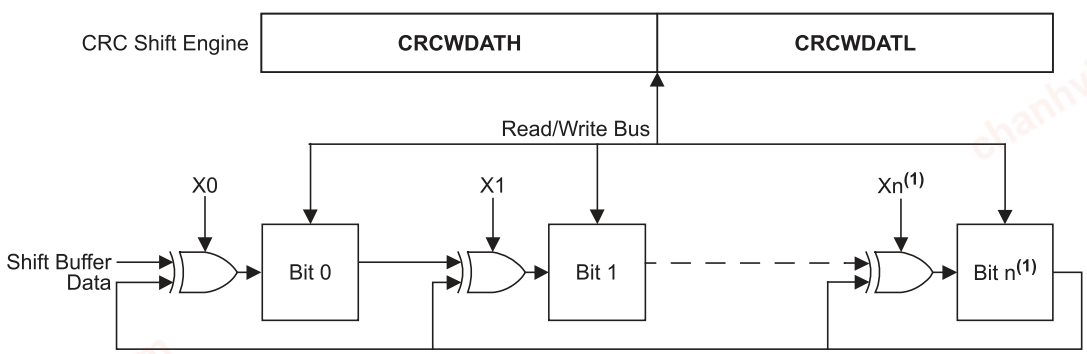


Figure 19-2. CRC Shift Engine Detail



Note:

1. n = PLEN[4:1] + 1.

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19.1 User Interface

19.1.1 Polynomial Interface

The CRC module can be programmed for CRC polynomials of up to the 32nd order, using up to 32 bits.

Polynomial length, which reflects the highest exponent in the equation, is selected by the PLEN[4:0] bits (CRCCON2[4:0]).

The CRCXORL and CRCXORH registers control which exponent terms are included in the equation. Setting a particular bit includes that exponent term in the equation. Functionally, this includes an XOR operation on the corresponding bit in the CRC engine. Clearing the bit disables the XOR.

For example, consider two CRC polynomials, one a 16-bit and the other a 32-bit equation.
$X^{16} + X^{12} + X^5 + 1$

AND
$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

To program these polynomials into the CRC generator, set the register bits, as shown in Table 19-1.

Table 19-1. CRC Setup Examples for 16 and 32-Bit Polynomials

CRC Control Bits	Bit Values	
	16-Bit Polynomial	32-Bit Polynomial
PLEN[4:0]	01111	11111
X[31:16]	0000 0000 0000 0001	0000 0100 1100 0001
X[15:1]	0001 0000 0010 000	0001 1101 1011 011

Note that the appropriate positions are set to '1' to indicate that they are used in the equation (for example, X26 and X23). The '0' bit required by the equation is always XORed; thus, X0 is a don't care. For a polynomial of length 32, it is assumed that the 32nd bit will be used; therefore, the X[31:1] bits do not have the 32nd bit.

19.1.2 Data Interface

The module incorporates a FIFO that works with a variable data width. Input data width can be configured to any value, between 1 and 32 bits, using the DWIDTH[4:0] bits (CRCCON2[12:8]). When the data width is greater than 15, the FIFO is four words deep. When the DWIDTHx bits are between 15 and 8, the FIFO is eight words deep. When the DWIDTHx bits are less than eight, the FIFO is 16 words deep.

The data for which the CRC is to be calculated must first be written into the FIFO. Even if the data width is less than eight, the smallest data element that can be written into the FIFO is 1 byte. For example, if the DWIDTHx bits are five, then the size of the data is DWIDTH[4:0] + 1 or 6. The data are written as a whole byte; the two unused upper bits are ignored by the module.

Once data are written into the MSb of the CRCDAT registers (that is, the MSb as defined by the data width), the value of the VWORD[4:0] bits (CRCCON1[12:8]) increments by one. For example, if the DWIDTHx bits are 24, the VWORDx bits will increment when bit 7 of CRCDATH is written. Therefore, CRCDATL must always be written to before CRCDATH.

The CRC engine starts shifting data when the CRCGO bit (CRCCON1[4]) is set and the value of the VWORDx bits is greater than zero.

Each word is copied out of the FIFO into a buffer register, which decrements the VWORDx bits. The data are then shifted out of the buffer. The CRC engine continues shifting at a rate of two bits per instruction cycle, until the VWORDx bits reach zero. This means that for a given data width, it takes half that number of instructions for each word to complete the calculation. For example, it takes 16 cycles to calculate the CRC for a single word of 32-bit data.

When the VWORDx bits reach the maximum value for the configured value of the DWIDTHx bits (4, 8 or 16), the CRCFUL bit (CRCCON1[7]) becomes set. When the VWORDx bits reach zero, the CRCMPT bit (CRCCON1[6]) becomes set. The FIFO is emptied and the VWORD[4:0] bits are set to '00000' whenever CRCEN is '0'.

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At least one instruction cycle must pass after a write to CRCWDAT before a read of the VWORDx bits is done.

19.1.3 Data Shift Direction

The LENDIAN bit (CRCCON1[3]) is used to control the shift direction. By default, the CRC will shift data through the engine, MSb first. Setting LENDIAN (= 1) causes the CRC to shift data, LSb first. This setting allows better integration with various communication schemes and removes the overhead of reversing the bit order in software. Note that this only changes the direction the data are shifted into the engine. The result of the CRC calculation will still be a normal CRC result, not a reverse CRC result.

19.1.4 Interrupt Operation

The module generates an interrupt that is configurable by the user for either of two conditions.

If CRCISEL is '0', an interrupt is generated when the VWORD[4:0] bits make a transition from a value of '1' to '0'. If CRCISEL is '1', an interrupt will be generated after the CRC operation finishes and the module sets the CRCGO bit to '0'. Manually setting CRCGO to '0' will not generate an interrupt. Note that when an interrupt occurs, the CRC calculation would not yet be complete. The module will still need (PLENx + 1)/2 clock cycles after the interrupt is generated until the CRC calculation is finished.

19.1.5 Typical Operation

To use the module for a typical CRC calculation:

1. Set the CRCEN bit to enable the module.
2. Configure the module for the desired operation.
   2.1. Program the desired polynomial using the CRCXOR registers and PLEN[4:0] bits.
   2.2. Configure the data width and shift direction using the DWIDTH[4:0] and LENDIAN bits.
3. Set the CRCGO bit to start the calculations.
4. Set the desired CRC non-direct initial value by writing to the CRCWDAT registers.
5. Load all data into the FIFO by writing to the CRCDAT registers as space becomes available (the CRCFUL bit must be zero before the next data loading).
6. Wait until the data FIFO is empty (CRCMPT bit is set).
7. Read the result:
   If the data width (DWIDTH[4:0] bits) is more than the polynomial length (PLEN[4:0] bits):
   7.1. Wait (DWIDTH[4:0] + 1)/2 instruction cycles to make sure that shifts from the shift buffer are finished.
   7.2. Change the data width to the polynomial length (DWIDTH[4:0] = PLEN[4:0]).
   7.3. Write one dummy data word to the CRCDAT registers.
   7.4. Wait two instruction cycles to move the data from the FIFO to the shift buffer and (PLEN[4:0] + 1)/2 instruction cycles to shift out the result.

Or, if the data width (DWIDTH[4:0] bits) is less than the polynomial length (PLEN[4:0] bits):

1. Clear the CRC Interrupt Selection bit (CRCISEL = 0) to get the interrupt when all shifts are done. Clear the CRC interrupt flag. Write dummy data in the CRCDAT registers and wait until the CRC interrupt flag is set.
2. Read the final CRC result from the CRCWDAT registers.
3. Restore the data width (DWIDTH[4:0] bits) for further calculations (Optional). If the data width (DWIDTH[4:0] bits) is equal to, or less than, the polynomial length (PLEN[4:0] bits):
   3.1. Clear the CRC Interrupt Selection bit (CRCISEL = 0) to get the interrupt when all shifts are done.
   3.2. Suspend the calculation by setting CRCGO = 0.
   3.3. Clear the CRC interrupt flag.
   3.4. Write the dummy data with the total data length equal to the polynomial length in the CRCDAT registers.
   3.5. Resume the calculation by setting CRCGO = 1.
   3.6. Wait until the CRC interrupt flag is set.
   3.7. Read the final CRC result from the CRCWDAT registers.

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19.2 CRC Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x0157	Reserved									
0x0158	CRCCON1	7:0	CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN			
		15:8	CRCEN		CSIDL	VWORD[4:0]				
0x015A	CRCCON2	7:0				PLEN[4:0]				
		15:8				DWIDTH[4:0]				
0x015C	CRCXORL	7:0	X[6:0]							
		15:8	X[14:7]							
0x015E	CRCXORH	7:0	X[23:16]							
		15:8	X[31:24]							
0x0160	CRCDATL	7:0	CRCDATL[7:0]							
		15:8	CRCDATL[15:8]							
0x0162	CRCDATH	7:0	CRCDATH[7:0]							
		15:8	CRCDATH[15:8]							
0x0164	CRCWDATL	7:0	CRCWDATL[7:0]							
		15:8	CRCWDATL[15:8]							
0x0166	CRCWDATH	7:0	CRCWDATH[7:0]							
		15:8	CRCWDATH[15:8]							

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19.2.1 CRC Control 1 Register

Name: CRCCON1
Offset: 0x158

Bit	15	14	13	12	11	10	9	8
	CRCEN		CSIDL	VWORD[4:0]				
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN			
Access	R/W	R/W	R/W	R/W	R/W			
Reset	0	0	0	0	0			

Bit 15 – CRCEN CRC Enable bit

Value	Description
1	Enables module
0	Disables module; all state machines, pointers and CRCWDAT/CRCDAT registers reset; other SFRs are NOT reset

Bit 13 – CSIDL CRC Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode
0	Continues module operation in Idle mode

Bits 12:8 – VWORD[4:0] Pointer Value bits
Indicates the number of valid words in the FIFO. Has a maximum value of 8 when PLEN[4:0] ≥ 7 or 16 when PLEN[4:0] ≤ 7.

Bit 7 – CRCFUL CRC FIFO Full bit

Value	Description
1	FIFO is full
0	FIFO is not full

Bit 6 – CRCMPT CRC FIFO Empty bit

Value	Description
1	FIFO is empty
0	FIFO is not empty

Bit 5 – CRCISEL CRC Interrupt Selection bit

Value	Description
1	Interrupt on FIFO is empty; the final word of data is still shifting through the CRC
0	Interrupt on shift is complete and results are ready

Bit 4 – CRCGO Start CRC bit

Value	Description
1	Starts CRC serial shifter
0	CRC serial shifter is turned off

Bit 3 – LENDIAN Data Shift Direction Select bit

Value	Description
1	Data word is shifted into the CRC, starting with the LSb (little-endian)
0	Data word is shifted into the CRC, starting with the MSb (big-endian)

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19.2.2 CRC Control 2 Register

Name: CRCCON2
Offset: 0x15A

Bit	15	14	13	12	11	10	9	8
				DWIDTH[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				PLEN[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 12:8 – DWIDTH[4:0] CRC Data Word Width Configuration bits
Configures the width of the data word (Data Word Width – 1).

Bits 4:0 – PLEN[4:0] Polynomial Length Configuration bits
Configures the length of the polynomial (Polynomial Length – 1).

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19.2.3 CRC XOR Polynomial Register Low

Name: CRCXORL
Offset: 0x15C

Bit	15	14	13	12	11	10	9	8
	X[14:7]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	X[6:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

Bits 15:1 – X[14:0] XOR of Polynomial Term X^n Enable bits

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19.2.4 CRC XOR Polynomial Register High

Name: CRCXORH
Offset: 0x15E

Bit	15	14	13	12	11	10	9	8
	X[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	X[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – X[31:24] XOR of Polynomial Term X^n Enable bits

Bits 7:0 – X[23:16] XOR of Polynomial Term X^n Enable bits

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19.2.5 CRC Data Register Low

Name: CRCDATL
Offset: 0x160

Bit	15	14	13	12	11	10	9	8
	CRCDATL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CRCDATL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CRCDATL[15:0] CRC Data Low bits

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19.2.6 CRC Data Register High

Name: CRCDATH
Offset: 0x162

Bit	15	14	13	12	11	10	9	8
	CRCDATH[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CRCDATH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CRCDATH[15:0] CRC Data High bits

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19.2.7 CRC Result Register Low

Name: CRCWDATL
Offset: 0x164

Bit	15	14	13	12	11	10	9	8
	CRCWDATL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CRCWDATL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CRCWDATL[15:0] CRC Result Low bits

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19.2.8 CRC Result Register High

Name: CRCWDATH
Offset: 0x166

Bit	15	14	13	12	11	10	9	8
	CRCWDATH[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CRCWDATH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CRCWDATH[15:0] CRC Result High bits

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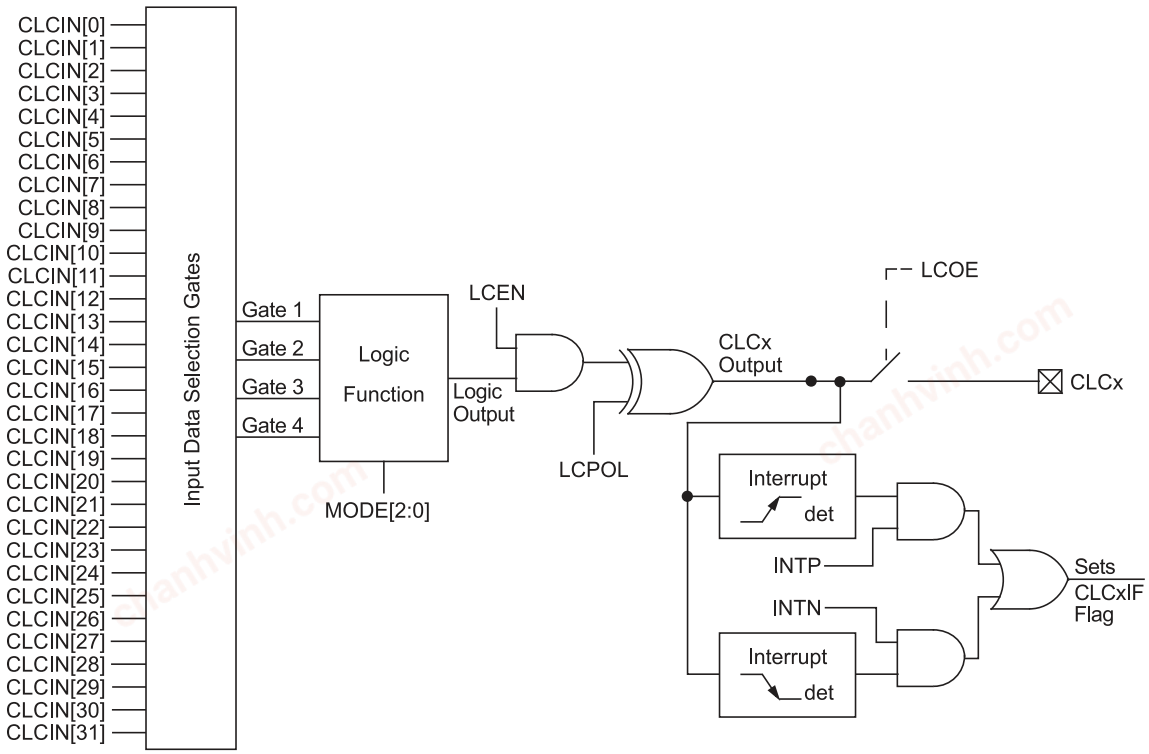
20. Configurable Logic Cell (CLC)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to **"Configurable Logic Cell (CLC)"** (www.microchip.com/DS70005298) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

The Configurable Logic Cell (CLC) module allows the user to specify combinations of signals as inputs to a logic function and to use the logic output to control other peripherals or I/O pins. This provides greater flexibility and potential in embedded designs, since the CLC module can operate outside the limitations of software execution and supports a vast amount of output designs.

There are four input gates to the selected logic function. These four input gates select from a pool of up to 32 signals that are selected using four data source selection multiplexers. Figure 20-1 shows an overview of the module. Figure 20-3 shows the details of the data source multiplexers and logic input gate connections.

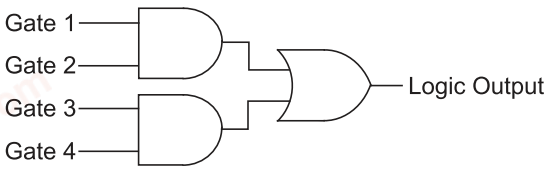
Figure 20-1. CLC Module

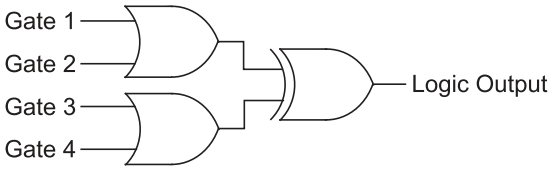


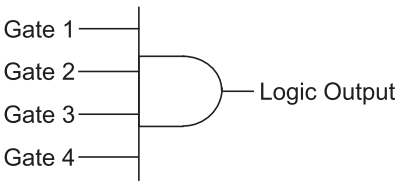
Note: All register bits shown in this figure can be found in the CLCxCONL register.

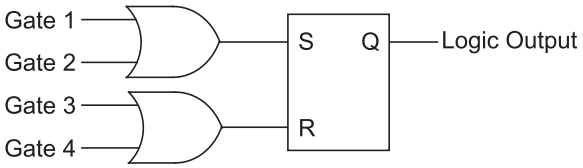
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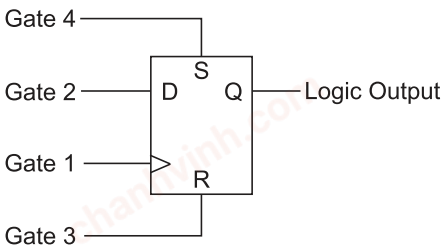
Figure 20-2. CLC Logic Function Combinatorial Options

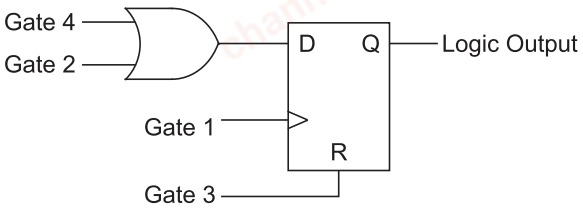
<table>
<tr>
<td>AND – OR


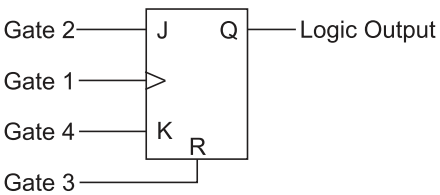
MODE[2:0] = 000</td>
<td>OR – XOR


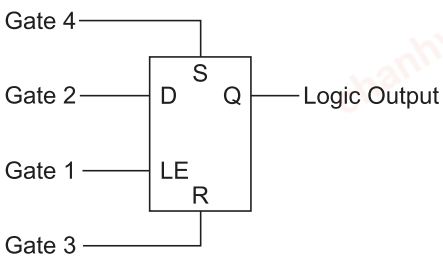
MODE[2:0] = 001</td>
</tr>
<tr>
<td>4-Input AND


MODE[2:0] = 010</td>
<td>S-R Latch


MODE[2:0] = 011</td>
</tr>
<tr>
<td>1-Input D Flip-Flop with S and R


MODE[2:0] = 100</td>
<td>2-Input D Flip-Flop with R


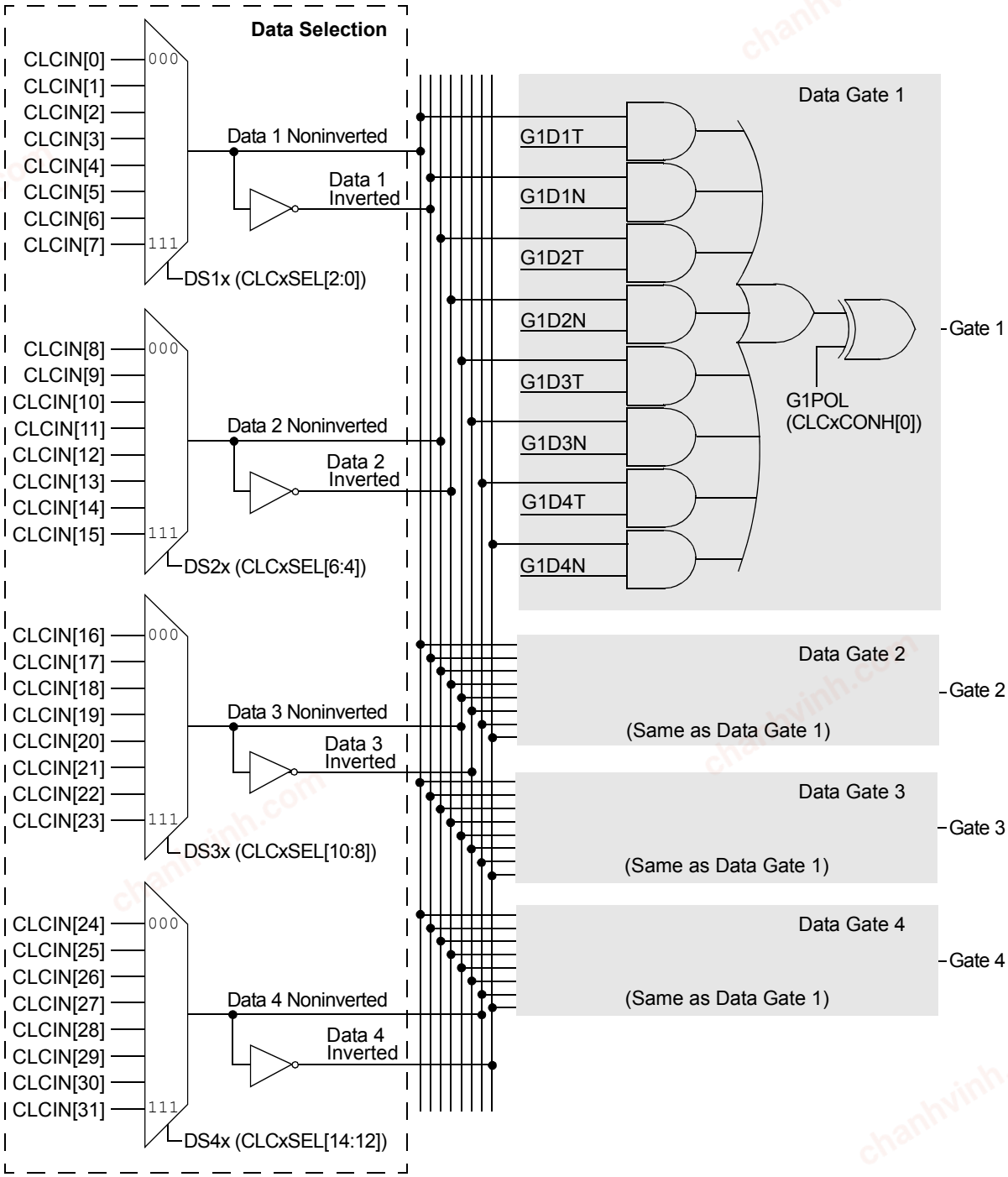
MODE[2:0] = 101</td>
</tr>
<tr>
<td>J-K Flip-Flop with R


MODE[2:0] = 110</td>
<td>1-Input Transparent Latch with S and R


MODE[2:0] = 111</td>
</tr>
</table>

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Figure 20-3. CLC Input Source Selection Diagram



Note: All controls are undefined at power-up.

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20.1 CLC Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x0463	Reserved									
0x0464	CLC1CONL	7:0	LCOE	LCOUT	LCPOL			MODE[2:0]		
		15:8	LCEN				INTP	INTN		
0x0466	CLC1CONH	7:0					G4POL	G3POL	G2POL	G1POL
		15:8								
0x0468	CLC1SEL	7:0		DS2[2:0]				DS1[2:0]		
		15:8		DS4[2:0]				DS3[2:0]		
0x046A ... 0x046B	Reserved									
0x046C	CLC1GLSL	7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
		15:8	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
0x046E	CLC1GLSH	7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
		15:8	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
0x0470	CLC2CONL	7:0	LCOE	LCOUT	LCPOL			MODE[2:0]		
		15:8	LCEN				INTP	INTN		
0x0472	CLC2CONH	7:0					G4POL	G3POL	G2POL	G1POL
		15:8								
0x0474	CLC2SEL	7:0		DS2[2:0]				DS1[2:0]		
		15:8		DS4[2:0]				DS3[2:0]		
0x0476 ... 0x0477	Reserved									
0x0478	CLC2GLSL	7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
		15:8	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
0x047A	CLC2GLSH	7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
		15:8	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
0x047C	CLC3CONL	7:0	LCOE	LCOUT	LCPOL			MODE[2:0]		
		15:8	LCEN				INTP	INTN		
0x047E	CLC3CONH	7:0					G4POL	G3POL	G2POL	G1POL
		15:8								
0x0480 ... 0x0483	Reserved									
0x0484	CLC3SEL	7:0		DS2[2:0]				DS1[2:0]		
		15:8		DS4[2:0]				DS3[2:0]		
0x0484	CLC3GLSL	7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
		15:8	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
0x0486	CLC3GLSH	7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
		15:8	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
0x0488	CLC4CONL	7:0	LCOE	LCOUT	LCPOL			MODE[2:0]		
		15:8	LCEN				INTP	INTN		
0x048A	CLC4CONH	7:0					G4POL	G3POL	G2POL	G1POL
		15:8								
0x048C	CLC4SEL	7:0		DS2[2:0]				DS1[2:0]		
		15:8		DS4[2:0]				DS3[2:0]		
0x048E ... 0x048F	Reserved									
0x0490	CLC4GLSL	7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
		15:8	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
0x0492	CLC4GLSH	7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
		15:8	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N

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20.1.1 Control Registers Overview

The CLCx module is controlled by the following registers:

- CLCxCONL
- CLCxCONH
- CLCxSEL
- CLCxGLSL
- CLCxGLSH

The CLCx Control registers (CLCxCONL and CLCxCONH) are used to enable the module and interrupts, control the output enable bit, select output polarity and select the logic function. The CLCx Control registers also allow the user to control the logic polarity of not only the cell output, but also some intermediate variables.

The CLCx Input MUX Select register (CLCxSEL) allows the user to select up to four data input sources using the four data input selection multiplexers. Each multiplexer has a list of eight data sources available.

The CLCx Gate Logic Input Select registers (CLCxGLSL and CLCxGLSH) allow the user to select which outputs from each of the selection MUXes are used as inputs to the input gates of the logic cell. Each data source MUX outputs both a true and a negated version of its output. All of these eight signals are enabled, ORed together by the logic cell input gates.

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20.1.2 CLC1 Control Register Low

Name: CLC1CONL
Offset: 0x464

Bit	15	14	13	12	11	10	9	8
	LCEN				INTP	INTN		
Access	R/W				R/W	R/W		
Reset	0				0	0		

Bit	7	6	5	4	3	2	1	0
	LCOE	LCOUT	LCPOL			MODE[2:0]		
Access	R/W	R	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bit 15 – LCEN CLC Enable bit

Value	Description
1	CLC is enabled and mixing input signals
0	CLC is disabled and has logic zero outputs

Bit 11 – INTP CLC Positive Edge Interrupt Enable bit

Value	Description
1	Interrupt will be generated when a rising edge occurs on LCOUT
0	Interrupt will not be generated

Bit 10 – INTN CLC Negative Edge Interrupt Enable bit

Value	Description
1	Interrupt will be generated when a falling edge occurs on LCOUT
0	Interrupt will not be generated

Bit 7 – LCOE CLC Port Enable bit

Value	Description
1	CLC port pin output is enabled
0	CLC port pin output is disabled

Bit 6 – LCOUT CLC Data Output Status bit

Value	Description
1	CLC output high
0	CLC output low

Bit 5 – LCPOL CLC Output Polarity Control bit

Value	Description
1	The output of the module is inverted
0	The output of the module is not inverted

Bits 2:0 – MODE[2:0] CLC Mode bits

Value	Description
111	Cell is a 1-input transparent latch with S and R
110	Cell is a JK flip-flop with R
101	Cell is a 2-input D flip-flop with R
100	Cell is a 1-input D flip-flop with S and R
011	Cell is an SR latch
010	Cell is a 4-input AND
001	Cell is an OR-XOR
000	Cell is an AND-OR

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20.1.3 CLC1 Control Register High

Name: CLC1CONH
Offset: 0x466

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					G4POL	G3POL	G2POL	G1POL
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – G4POL Gate 4 Polarity Control bit

Value	Description
1	The output of Channel 4 logic is inverted when applied to the logic cell
0	The output of Channel 4 logic is not inverted

Bit 2 – G3POL Gate 3 Polarity Control bit

Value	Description
1	The output of Channel 3 logic is inverted when applied to the logic cell
0	The output of Channel 3 logic is not inverted

Bit 1 – G2POL Gate 2 Polarity Control bit

Value	Description
1	The output of Channel 2 logic is inverted when applied to the logic cell
0	The output of Channel 2 logic is not inverted

Bit 0 – G1POL Gate 1 Polarity Control bit

Value	Description
1	The output of Channel 1 logic is inverted when applied to the logic cell
0	The output of Channel 1 logic is not inverted

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20.1.4 CLC1 Input MUX Select Register

Name: CLC1SEL
Offset: 0x468

Bit	15	14	13	12	11	10	9	8
		DS4[2:0]				DS3[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
		DS2[2:0]				DS1[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bits 14:12 – DS4[2:0] Data Selection MUX 4 Signal Selection bits

Value	Description
111	MCCP3 OCMP output
110	MCCP1 OCMP output
101	Unimplemented
100	Unimplemented
011	SPI1 Input (SDI1)
010	Comparator 3 output
001	CLC2 output
000	CLCIND pin

Bits 10:8 – DS3[2:0] Data Selection MUX 3 Signal Selection bits

Value	Description
111	MCCP3 OCMP output
110	MCCP2 OCMP output
101	DMA Channel 1 Interrupt
100	UART1 Input (U1RX)
011	SPI1 Output (SDO1)
010	Comparator 2 output
001	CLC1 output
000	CLCINC pin

Bits 6:4 – DS2[2:0] Data Selection MUX 2 Signal Selection bits

Value	Description
111	MCCP2 OCMP output
110	MCCP1 OCMP output
101	DMA Channel 0 Interrupt
100	A/D conversion done
011	UART1 Output (U1TX)
010	Comparator 1 output
001	CLC2 output
000	CLCINB pin

Bits 2:0 – DS1[2:0] Data Selection MUX 1 Signal Selection bits

Value	Description
111	Timer3 match event
110	Timer2 match event
101	Unimplemented
100	Reference Clock Output (REFO)
011	LPRC

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Value	Description
010	SOSC
001	Peripheral clock (F_{PB})
000	CLCINA pin

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20.1.5 CLC1 Gate Logic Input Select Low Register

Name: CLC1GLSL
Offset: 0x46C

Bit	15	14	13	12	11	10	9	8
	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – G2D4T Gate 2 Data Source 4 True Enable bit

Value	Description
1	The Data Source 4 signal is enabled for Gate 2
0	The Data Source 4 signal is disabled for Gate 2

Bit 14 – G2D4N Gate 2 Data Source 4 Negated Enable bit

Value	Description
1	The Data Source 4 inverted signal is enabled for Gate 2
0	The Data Source 4 inverted signal is disabled for Gate 2

Bit 13 – G2D3T Gate 2 Data Source 3 True Enable bit

Value	Description
1	The Data Source 3 signal is enabled for Gate 2
0	The Data Source 3 signal is disabled for Gate 2

Bit 12 – G2D3N Gate 2 Data Source 3 Negated Enable bit

Value	Description
1	The Data Source 3 inverted signal is enabled for Gate 2
0	The Data Source 3 inverted signal is disabled for Gate 2

Bit 11 – G2D2T Gate 2 Data Source 2 True Enable bit

Value	Description
1	The Data Source 2 signal is enabled for Gate 2
0	The Data Source 2 signal is disabled for Gate 2

Bit 10 – G2D2N Gate 2 Data Source 2 Negated Enable bit

Value	Description
1	The Data Source 2 inverted signal is enabled for Gate 2
0	The Data Source 2 inverted signal is disabled for Gate 2

Bit 9 – G2D1T Gate 2 Data Source 1 True Enable bit

Value	Description
1	The Data Source 1 signal is enabled for Gate 2
0	The Data Source 1 signal is disabled for Gate 2

Bit 8 – G2D1N Gate 2 Data Source 1 Negated Enable bit

Value	Description
1	The Data Source 1 inverted signal is enabled for Gate 2
0	The Data Source 1 inverted signal is disabled for Gate 2

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Bit 7 – G1D4T Gate 1 Data Source 4 True Enable bit

Value	Description
1	The Data Source 4 signal is enabled for Gate 1
0	The Data Source 4 signal is disabled for Gate 1

Bit 6 – G1D4N Gate 1 Data Source 4 Negated Enable bit

Value	Description
1	The Data Source 4 inverted signal is enabled for Gate 1
0	The Data Source 4 inverted signal is disabled for Gate 1

Bit 5 – G1D3T Gate 1 Data Source 3 True Enable bit

Value	Description
1	The Data Source 3 signal is enabled for Gate 1
0	The Data Source 3 signal is disabled for Gate 1

Bit 4 – G1D3N Gate 1 Data Source 3 Negated Enable bit

Value	Description
1	The Data Source 3 inverted signal is enabled for Gate 1
0	The Data Source 3 inverted signal is disabled for Gate 1

Bit 3 – G1D2T Gate 1 Data Source 2 True Enable bit

Value	Description
1	The Data Source 2 signal is enabled for Gate 1
0	The Data Source 2 signal is disabled for Gate 1

Bit 2 – G1D2N Gate 1 Data Source 2 Negated Enable bit

Value	Description
1	The Data Source 2 inverted signal is enabled for Gate 1
0	The Data Source 2 inverted signal is disabled for Gate 1

Bit 1 – G1D1T Gate 1 Data Source 1 True Enable bit

Value	Description
1	The Data Source 1 signal is enabled for Gate 1
0	The Data Source 1 signal is disabled for Gate 1

Bit 0 – G1D1N Gate 1 Data Source 1 Negated Enable bit

Value	Description
1	The Data Source 1 inverted signal is enabled for Gate 1
0	The Data Source 1 inverted signal is disabled for Gate 1

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20.1.6 CLC1 Gate Logic Input Select High Register

Name: CLC1GLSH
Offset: 0x46E

Bit	15	14	13	12	11	10	9	8
	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – G4D4T Gate 4 Data Source 4 True Enable bit

Value	Description
1	The Data Source 4 signal is enabled for Gate 4
0	The Data Source 4 signal is disabled for Gate 4

Bit 14 – G4D4N Gate 4 Data Source 4 Negated Enable bit

Value	Description
1	The Data Source 4 inverted signal is enabled for Gate 4
0	The Data Source 4 inverted signal is disabled for Gate 4

Bit 13 – G4D3T Gate 4 Data Source 3 True Enable bit

Value	Description
1	The Data Source 3 signal is enabled for Gate 4
0	The Data Source 3 signal is disabled for Gate 4

Bit 12 – G4D3N Gate 4 Data Source 3 Negated Enable bit

Value	Description
1	The Data Source 3 inverted signal is enabled for Gate 4
0	The Data Source 3 inverted signal is disabled for Gate 4

Bit 11 – G4D2T Gate 4 Data Source 2 True Enable bit

Value	Description
1	The Data Source 2 signal is enabled for Gate 4
0	The Data Source 2 signal is disabled for Gate 4

Bit 10 – G4D2N Gate 4 Data Source 2 Negated Enable bit

Value	Description
1	The Data Source 2 inverted signal is enabled for Gate 4
0	The Data Source 2 inverted signal is disabled for Gate 4

Bit 9 – G4D1T Gate 4 Data Source 1 True Enable bit

Value	Description
1	The Data Source 1 signal is enabled for Gate 4
0	The Data Source 1 signal is disabled for Gate 4

Bit 8 – G4D1N Gate 4 Data Source 1 Negated Enable bit

Value	Description
1	The Data Source 1 inverted signal is enabled for Gate 4
0	The Data Source 1 inverted signal is disabled for Gate 4

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Bit 7 – G3D4T Gate 3 Data Source 4 True Enable bit

Value	Description
1	The Data Source 4 signal is enabled for Gate 3
0	The Data Source 4 signal is disabled for Gate 3

Bit 6 – G3D4N Gate 3 Data Source 4 Negated Enable bit

Value	Description
1	The Data Source 4 inverted signal is enabled for Gate 3
0	The Data Source 4 inverted signal is disabled for Gate 3

Bit 5 – G3D3T Gate 3 Data Source 3 True Enable bit

Value	Description
1	The Data Source 3 signal is enabled for Gate 3
0	The Data Source 3 signal is disabled for Gate 3

Bit 4 – G3D3N Gate 3 Data Source 3 Negated Enable bit

Value	Description
1	The Data Source 3 inverted signal is enabled for Gate 3
0	The Data Source 3 inverted signal is disabled for Gate 3

Bit 3 – G3D2T Gate 3 Data Source 2 True Enable bit

Value	Description
1	The Data Source 2 signal is enabled for Gate 3
0	The Data Source 2 signal is disabled for Gate 3

Bit 2 – G3D2N Gate 3 Data Source 2 Negated Enable bit

Value	Description
1	The Data Source 2 inverted signal is enabled for Gate 3
0	The Data Source 2 inverted signal is disabled for Gate 3

Bit 1 – G3D1T Gate 3 Data Source 1 True Enable bit

Value	Description
1	The Data Source 1 signal is enabled for Gate 3
0	The Data Source 1 signal is disabled for Gate 3

Bit 0 – G3D1N Gate 3 Data Source 1 Negated Enable bit

Value	Description
1	The Data Source 1 inverted signal is enabled for Gate 3
0	The Data Source 1 inverted signal is disabled for Gate 3

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20.1.7 CLC2 Control Register Low

Name: CLC2CONL
Offset: 0x470

Bit	15	14	13	12	11	10	9	8
	LCEN				INTP	INTN		
Access	R/W				R/W	R/W		
Reset	0				0	0		

Bit	7	6	5	4	3	2	1	0
	LCOE	LCOUT	LCPOL			MODE[2:0]		
Access	R/W	R	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bit 15 – LCEN CLC Enable bit

Value	Description
1	CLC is enabled and mixing input signals
0	CLC is disabled and has logic zero outputs

Bit 11 – INTP CLC Positive Edge Interrupt Enable bit

Value	Description
1	Interrupt will be generated when a rising edge occurs on LCOUT
0	Interrupt will not be generated

Bit 10 – INTN CLC Negative Edge Interrupt Enable bit

Value	Description
1	Interrupt will be generated when a falling edge occurs on LCOUT
0	Interrupt will not be generated

Bit 7 – LCOE CLC Port Enable bit

Value	Description
1	CLC port pin output is enabled
0	CLC port pin output is disabled

Bit 6 – LCOUT CLC Data Output Status bit

Value	Description
1	CLC output high
0	CLC output low

Bit 5 – LCPOL CLC Output Polarity Control bit

Value	Description
1	The output of the module is inverted
0	The output of the module is not inverted

Bits 2:0 – MODE[2:0] CLC Mode bits

Value	Description
111	Cell is a 1-input transparent latch with S and R
110	Cell is a JK flip-flop with R
101	Cell is a 2-input D flip-flop with R
100	Cell is a 1-input D flip-flop with S and R
011	Cell is an SR latch
010	Cell is a 4-input AND
001	Cell is an OR-XOR
000	Cell is an AND-OR

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20.1.8 CLC2 Control Register High

Name: CLC2CONH
Offset: 0x472

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					G4POL	G3POL	G2POL	G1POL
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – G4POL Gate 4 Polarity Control bit

Value	Description
1	The output of Channel 4 logic is inverted when applied to the logic cell
0	The output of Channel 4 logic is not inverted

Bit 2 – G3POL Gate 3 Polarity Control bit

Value	Description
1	The output of Channel 3 logic is inverted when applied to the logic cell
0	The output of Channel 3 logic is not inverted

Bit 1 – G2POL Gate 2 Polarity Control bit

Value	Description
1	The output of Channel 2 logic is inverted when applied to the logic cell
0	The output of Channel 2 logic is not inverted

Bit 0 – G1POL Gate 1 Polarity Control bit

Value	Description
1	The output of Channel 1 logic is inverted when applied to the logic cell
0	The output of Channel 1 logic is not inverted

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20.1.9 CLC2 Input MUX Select Register

Name: CLC2SEL
Offset: 0x474

Bit	15	14	13	12	11	10	9	8
		DS4[2:0]				DS3[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
		DS2[2:0]				DS1[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bits 14:12 – DS4[2:0] Data Selection MUX 4 Signal Selection bits

Value	Description
111	MCCP3 OCMP output
110	MCCP1 OCMP Output
101	Unimplemented
100	Unimplemented
011	SPI2 Input (SDI2)
010	Comparator 3 output
001	CLC1 output
000	CLCIND pin

Bits 10:8 – DS3[2:0] Data Selection MUX 3 Signal Selection bits

Value	Description
111	MCCP3 OCMP output
110	MCCP2 OCMP output
101	DMA Channel 1 Interrupt
100	UART2 Input (U2RX)
011	SPI2 Output (SDO2)
010	Comparator 2 output
001	CLC2 output
000	CLCINC pin

Bits 6:4 – DS2[2:0] Data Selection MUX 2 Signal Selection bits

Value	Description
111	MCCP2 OCMP output
110	MCCP1 OCMP output
101	DMA Channel 0 Interrupt
100	A/D conversion done
011	UART2 Output (U2TX)
010	Comparator 1 output
001	CLC1 output
000	CLCINB pin

Bits 2:0 – DS1[2:0] Data Selection MUX 1 Signal Selection bits

Value	Description
111	Timer3 match event
110	Timer2 match event
101	Unimplemented
100	Reference Clock Output (REFO)
011	LPRC

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Value	Description
010	SOSC
001	Peripheral clock (F_{PB})
000	CLCINA pin

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20.1.10 CLC2 Gate Logic Input Select Low Register

Name: CLC2GLSL
Offset: 0x478

Bit	15	14	13	12	11	10	9	8
	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – G2D4T Gate 2 Data Source 4 True Enable bit

Value	Description
1	The Data Source 4 signal is enabled for Gate 2
0	The Data Source 4 signal is disabled for Gate 2

Bit 14 – G2D4N Gate 2 Data Source 4 Negated Enable bit

Value	Description
1	The Data Source 4 inverted signal is enabled for Gate 2
0	The Data Source 4 inverted signal is disabled for Gate 2

Bit 13 – G2D3T Gate 2 Data Source 3 True Enable bit

Value	Description
1	The Data Source 3 signal is enabled for Gate 2
0	The Data Source 3 signal is disabled for Gate 2

Bit 12 – G2D3N Gate 2 Data Source 3 Negated Enable bit

Value	Description
1	The Data Source 3 inverted signal is enabled for Gate 2
0	The Data Source 3 inverted signal is disabled for Gate 2

Bit 11 – G2D2T Gate 2 Data Source 2 True Enable bit

Value	Description
1	The Data Source 2 signal is enabled for Gate 2
0	The Data Source 2 signal is disabled for Gate 2

Bit 10 – G2D2N Gate 2 Data Source 2 Negated Enable bit

Value	Description
1	The Data Source 2 inverted signal is enabled for Gate 2
0	The Data Source 2 inverted signal is disabled for Gate 2

Bit 9 – G2D1T Gate 2 Data Source 1 True Enable bit

Value	Description
1	The Data Source 1 signal is enabled for Gate 2
0	The Data Source 1 signal is disabled for Gate 2

Bit 8 – G2D1N Gate 2 Data Source 1 Negated Enable bit

Value	Description
1	The Data Source 1 inverted signal is enabled for Gate 2
0	The Data Source 1 inverted signal is disabled for Gate 2

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Bit 7 – G1D4T Gate 1 Data Source 4 True Enable bit

Value	Description
1	The Data Source 4 signal is enabled for Gate 1
0	The Data Source 4 signal is disabled for Gate 1

Bit 6 – G1D4N Gate 1 Data Source 4 Negated Enable bit

Value	Description
1	The Data Source 4 inverted signal is enabled for Gate 1
0	The Data Source 4 inverted signal is disabled for Gate 1

Bit 5 – G1D3T Gate 1 Data Source 3 True Enable bit

Value	Description
1	The Data Source 3 signal is enabled for Gate 1
0	The Data Source 3 signal is disabled for Gate 1

Bit 4 – G1D3N Gate 1 Data Source 3 Negated Enable bit

Value	Description
1	The Data Source 3 inverted signal is enabled for Gate 1
0	The Data Source 3 inverted signal is disabled for Gate 1

Bit 3 – G1D2T Gate 1 Data Source 2 True Enable bit

Value	Description
1	The Data Source 2 signal is enabled for Gate 1
0	The Data Source 2 signal is disabled for Gate 1

Bit 2 – G1D2N Gate 1 Data Source 2 Negated Enable bit

Value	Description
1	The Data Source 2 inverted signal is enabled for Gate 1
0	The Data Source 2 inverted signal is disabled for Gate 1

Bit 1 – G1D1T Gate 1 Data Source 1 True Enable bit

Value	Description
1	The Data Source 1 signal is enabled for Gate 1
0	The Data Source 1 signal is disabled for Gate 1

Bit 0 – G1D1N Gate 1 Data Source 1 Negated Enable bit

Value	Description
1	The Data Source 1 inverted signal is enabled for Gate 1
0	The Data Source 1 inverted signal is disabled for Gate 1

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20.1.11 CLC2 Gate Logic Input Select High Register

Name: CLC2GLSH
Offset: 0x47A

Bit	15	14	13	12	11	10	9	8
	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – G4D4T Gate 4 Data Source 4 True Enable bit

Value	Description
1	The Data Source 4 signal is enabled for Gate 4
0	The Data Source 4 signal is disabled for Gate 4

Bit 14 – G4D4N Gate 4 Data Source 4 Negated Enable bit

Value	Description
1	The Data Source 4 inverted signal is enabled for Gate 4
0	The Data Source 4 inverted signal is disabled for Gate 4

Bit 13 – G4D3T Gate 4 Data Source 3 True Enable bit

Value	Description
1	The Data Source 3 signal is enabled for Gate 4
0	The Data Source 3 signal is disabled for Gate 4

Bit 12 – G4D3N Gate 4 Data Source 3 Negated Enable bit

Value	Description
1	The Data Source 3 inverted signal is enabled for Gate 4
0	The Data Source 3 inverted signal is disabled for Gate 4

Bit 11 – G4D2T Gate 4 Data Source 2 True Enable bit

Value	Description
1	The Data Source 2 signal is enabled for Gate 4
0	The Data Source 2 signal is disabled for Gate 4

Bit 10 – G4D2N Gate 4 Data Source 2 Negated Enable bit

Value	Description
1	The Data Source 2 inverted signal is enabled for Gate 4
0	The Data Source 2 inverted signal is disabled for Gate 4

Bit 9 – G4D1T Gate 4 Data Source 1 True Enable bit

Value	Description
1	The Data Source 1 signal is enabled for Gate 4
0	The Data Source 1 signal is disabled for Gate 4

Bit 8 – G4D1N Gate 4 Data Source 1 Negated Enable bit

Value	Description
1	The Data Source 1 inverted signal is enabled for Gate 4
0	The Data Source 1 inverted signal is disabled for Gate 4

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Bit 7 – G3D4T Gate 3 Data Source 4 True Enable bit

Value	Description
1	The Data Source 4 signal is enabled for Gate 3
0	The Data Source 4 signal is disabled for Gate 3

Bit 6 – G3D4N Gate 3 Data Source 4 Negated Enable bit

Value	Description
1	The Data Source 4 inverted signal is enabled for Gate 3
0	The Data Source 4 inverted signal is disabled for Gate 3

Bit 5 – G3D3T Gate 3 Data Source 3 True Enable bit

Value	Description
1	The Data Source 3 signal is enabled for Gate 3
0	The Data Source 3 signal is disabled for Gate 3

Bit 4 – G3D3N Gate 3 Data Source 3 Negated Enable bit

Value	Description
1	The Data Source 3 inverted signal is enabled for Gate 3
0	The Data Source 3 inverted signal is disabled for Gate 3

Bit 3 – G3D2T Gate 3 Data Source 2 True Enable bit

Value	Description
1	The Data Source 2 signal is enabled for Gate 3
0	The Data Source 2 signal is disabled for Gate 3

Bit 2 – G3D2N Gate 3 Data Source 2 Negated Enable bit

Value	Description
1	The Data Source 2 inverted signal is enabled for Gate 3
0	The Data Source 2 inverted signal is disabled for Gate 3

Bit 1 – G3D1T Gate 3 Data Source 1 True Enable bit

Value	Description
1	The Data Source 1 signal is enabled for Gate 3
0	The Data Source 1 signal is disabled for Gate 3

Bit 0 – G3D1N Gate 3 Data Source 1 Negated Enable bit

Value	Description
1	The Data Source 1 inverted signal is enabled for Gate 3
0	The Data Source 1 inverted signal is disabled for Gate 3

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20.1.12 CLC3 Control Register Low

Name: CLC3CONL
Offset: 0x47C

Bit	15	14	13	12	11	10	9	8
	LCEN				INTP	INTN		
Access	R/W				R/W	R/W		
Reset	0				0	0		

Bit	7	6	5	4	3	2	1	0
	LCOE	LCOUT	LCPOL			MODE[2:0]		
Access	R/W	R	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bit 15 – LCEN CLC Enable bit

Value	Description
1	CLC is enabled and mixing input signals
0	CLC is disabled and has logic zero outputs

Bit 11 – INTP CLC Positive Edge Interrupt Enable bit

Value	Description
1	Interrupt will be generated when a rising edge occurs on LCOUT
0	Interrupt will not be generated

Bit 10 – INTN CLC Negative Edge Interrupt Enable bit

Value	Description
1	Interrupt will be generated when a falling edge occurs on LCOUT
0	Interrupt will not be generated

Bit 7 – LCOE CLC Port Enable bit

Value	Description
1	CLC port pin output is enabled
0	CLC port pin output is disabled

Bit 6 – LCOUT CLC Data Output Status bit

Value	Description
1	CLC output high
0	CLC output low

Bit 5 – LCPOL CLC Output Polarity Control bit

Value	Description
1	The output of the module is inverted
0	The output of the module is not inverted

Bits 2:0 – MODE[2:0] CLC Mode bits

Value	Description
111	Cell is a 1-input transparent latch with S and R
110	Cell is a JK flip-flop with R
101	Cell is a 2-input D flip-flop with R
100	Cell is a 1-input D flip-flop with S and R
011	Cell is an SR latch
010	Cell is a 4-input AND
001	Cell is an OR-XOR
000	Cell is an AND-OR

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20.1.13 CLC3 Control Register High

Name: CLC3CONH
Offset: 0x47E

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					G4POL	G3POL	G2POL	G1POL
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – G4POL Gate 4 Polarity Control bit

Value	Description
1	The output of Channel 4 logic is inverted when applied to the logic cell
0	The output of Channel 4 logic is not inverted

Bit 2 – G3POL Gate 3 Polarity Control bit

Value	Description
1	The output of Channel 3 logic is inverted when applied to the logic cell
0	The output of Channel 3 logic is not inverted

Bit 1 – G2POL Gate 2 Polarity Control bit

Value	Description
1	The output of Channel 2 logic is inverted when applied to the logic cell
0	The output of Channel 2 logic is not inverted

Bit 0 – G1POL Gate 1 Polarity Control bit

Value	Description
1	The output of Channel 1 logic is inverted when applied to the logic cell
0	The output of Channel 1 logic is not inverted

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20.1.14 CLC3 Input MUX Select Register

Name: CLC3SEL
Offset: 0x484

Bit	15	14	13	12	11	10	9	8
		DS4[2:0]				DS3[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
		DS2[2:0]				DS1[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bits 14:12 – DS4[2:0] Data Selection MUX 4 Signal Selection bits

Value	Description
111	MCCP3 OCMP output
110	MCCP1 OCMP output
101	Unimplemented
100	Unimplemented
011	SPI1 Input (SDI1)
010	Comparator 3 output
001	CLC4 output
000	CLCIND pin

Bits 10:8 – DS3[2:0] Data Selection MUX 3 Signal Selection bits

Value	Description
111	MCCP3 OCMP output
110	MCCP2 OCMP output
101	DMA Channel 1 Interrupt
100	UART1 Input (U1RX)
011	SPI1 Output (SDO1)
010	Comparator 2 output
001	CLC1 output
000	CLCINC pin

Bits 6:4 – DS2[2:0] Data Selection MUX 2 Signal Selection bits

Value	Description
111	MCCP2 OCMP output
110	MCCP1 OCMP output
101	DMA Channel 0 Interrupt
100	A/D conversion done
011	UART1 Output (U1TX)
010	Comparator 1 output
001	CLC2 output
000	CLCINB pin

Bits 2:0 – DS1[2:0] Data Selection MUX 1 Signal Selection bits

Value	Description
111	Timer3 match event
110	Timer2 match event
101	Unimplemented
100	Reference Clock Output (REFO)
011	LPRC

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Value	Description
010	SOSC
001	Peripheral clock (F_{PB})
000	CLCINA pin

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20.1.15 CLC3 Gate Logic Input Select Low Register

Name: CLC3GLSL
Offset: 0x484

Bit	15	14	13	12	11	10	9	8
	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – G2D4T Gate 2 Data Source 4 True Enable bit

Value	Description
1	The Data Source 4 signal is enabled for Gate 2
0	The Data Source 4 signal is disabled for Gate 2

Bit 14 – G2D4N Gate 2 Data Source 4 Negated Enable bit

Value	Description
1	The Data Source 4 inverted signal is enabled for Gate 2
0	The Data Source 4 inverted signal is disabled for Gate 2

Bit 13 – G2D3T Gate 2 Data Source 3 True Enable bit

Value	Description
1	The Data Source 3 signal is enabled for Gate 2
0	The Data Source 3 signal is disabled for Gate 2

Bit 12 – G2D3N Gate 2 Data Source 3 Negated Enable bit

Value	Description
1	The Data Source 3 inverted signal is enabled for Gate 2
0	The Data Source 3 inverted signal is disabled for Gate 2

Bit 11 – G2D2T Gate 2 Data Source 2 True Enable bit

Value	Description
1	The Data Source 2 signal is enabled for Gate 2
0	The Data Source 2 signal is disabled for Gate 2

Bit 10 – G2D2N Gate 2 Data Source 2 Negated Enable bit

Value	Description
1	The Data Source 2 inverted signal is enabled for Gate 2
0	The Data Source 2 inverted signal is disabled for Gate 2

Bit 9 – G2D1T Gate 2 Data Source 1 True Enable bit

Value	Description
1	The Data Source 1 signal is enabled for Gate 2
0	The Data Source 1 signal is disabled for Gate 2

Bit 8 – G2D1N Gate 2 Data Source 1 Negated Enable bit

Value	Description
1	The Data Source 1 inverted signal is enabled for Gate 2
0	The Data Source 1 inverted signal is disabled for Gate 2

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Bit 7 – G1D4T Gate 1 Data Source 4 True Enable bit

Value	Description
1	The Data Source 4 signal is enabled for Gate 1
0	The Data Source 4 signal is disabled for Gate 1

Bit 6 – G1D4N Gate 1 Data Source 4 Negated Enable bit

Value	Description
1	The Data Source 4 inverted signal is enabled for Gate 1
0	The Data Source 4 inverted signal is disabled for Gate 1

Bit 5 – G1D3T Gate 1 Data Source 3 True Enable bit

Value	Description
1	The Data Source 3 signal is enabled for Gate 1
0	The Data Source 3 signal is disabled for Gate 1

Bit 4 – G1D3N Gate 1 Data Source 3 Negated Enable bit

Value	Description
1	The Data Source 3 inverted signal is enabled for Gate 1
0	The Data Source 3 inverted signal is disabled for Gate 1

Bit 3 – G1D2T Gate 1 Data Source 2 True Enable bit

Value	Description
1	The Data Source 2 signal is enabled for Gate 1
0	The Data Source 2 signal is disabled for Gate 1

Bit 2 – G1D2N Gate 1 Data Source 2 Negated Enable bit

Value	Description
1	The Data Source 2 inverted signal is enabled for Gate 1
0	The Data Source 2 inverted signal is disabled for Gate 1

Bit 1 – G1D1T Gate 1 Data Source 1 True Enable bit

Value	Description
1	The Data Source 1 signal is enabled for Gate 1
0	The Data Source 1 signal is disabled for Gate 1

Bit 0 – G1D1N Gate 1 Data Source 1 Negated Enable bit

Value	Description
1	The Data Source 1 inverted signal is enabled for Gate 1
0	The Data Source 1 inverted signal is disabled for Gate 1

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20.1.16 CLC3 Gate Logic Input Select High Register

Name: CLC3GLSH
Offset: 0x486

Bit	15	14	13	12	11	10	9	8
	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – G4D4T Gate 4 Data Source 4 True Enable bit

Value	Description
1	The Data Source 4 signal is enabled for Gate 4
0	The Data Source 4 signal is disabled for Gate 4

Bit 14 – G4D4N Gate 4 Data Source 4 Negated Enable bit

Value	Description
1	The Data Source 4 inverted signal is enabled for Gate 4
0	The Data Source 4 inverted signal is disabled for Gate 4

Bit 13 – G4D3T Gate 4 Data Source 3 True Enable bit

Value	Description
1	The Data Source 3 signal is enabled for Gate 4
0	The Data Source 3 signal is disabled for Gate 4

Bit 12 – G4D3N Gate 4 Data Source 3 Negated Enable bit

Value	Description
1	The Data Source 3 inverted signal is enabled for Gate 4
0	The Data Source 3 inverted signal is disabled for Gate 4

Bit 11 – G4D2T Gate 4 Data Source 2 True Enable bit

Value	Description
1	The Data Source 2 signal is enabled for Gate 4
0	The Data Source 2 signal is disabled for Gate 4

Bit 10 – G4D2N Gate 4 Data Source 2 Negated Enable bit

Value	Description
1	The Data Source 2 inverted signal is enabled for Gate 4
0	The Data Source 2 inverted signal is disabled for Gate 4

Bit 9 – G4D1T Gate 4 Data Source 1 True Enable bit

Value	Description
1	The Data Source 1 signal is enabled for Gate 4
0	The Data Source 1 signal is disabled for Gate 4

Bit 8 – G4D1N Gate 4 Data Source 1 Negated Enable bit

Value	Description
1	The Data Source 1 inverted signal is enabled for Gate 4
0	The Data Source 1 inverted signal is disabled for Gate 4

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Bit 7 – G3D4T Gate 3 Data Source 4 True Enable bit

Value	Description
1	The Data Source 4 signal is enabled for Gate 3
0	The Data Source 4 signal is disabled for Gate 3

Bit 6 – G3D4N Gate 3 Data Source 4 Negated Enable bit

Value	Description
1	The Data Source 4 inverted signal is enabled for Gate 3
0	The Data Source 4 inverted signal is disabled for Gate 3

Bit 5 – G3D3T Gate 3 Data Source 3 True Enable bit

Value	Description
1	The Data Source 3 signal is enabled for Gate 3
0	The Data Source 3 signal is disabled for Gate 3

Bit 4 – G3D3N Gate 3 Data Source 3 Negated Enable bit

Value	Description
1	The Data Source 3 inverted signal is enabled for Gate 3
0	The Data Source 3 inverted signal is disabled for Gate 3

Bit 3 – G3D2T Gate 3 Data Source 2 True Enable bit

Value	Description
1	The Data Source 2 signal is enabled for Gate 3
0	The Data Source 2 signal is disabled for Gate 3

Bit 2 – G3D2N Gate 3 Data Source 2 Negated Enable bit

Value	Description
1	The Data Source 2 inverted signal is enabled for Gate 3
0	The Data Source 2 inverted signal is disabled for Gate 3

Bit 1 – G3D1T Gate 3 Data Source 1 True Enable bit

Value	Description
1	The Data Source 1 signal is enabled for Gate 3
0	The Data Source 1 signal is disabled for Gate 3

Bit 0 – G3D1N Gate 3 Data Source 1 Negated Enable bit

Value	Description
1	The Data Source 1 inverted signal is enabled for Gate 3
0	The Data Source 1 inverted signal is disabled for Gate 3

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20.1.17 CLC4 Control Register Low

Name: CLC4CONL
Offset: 0x488

Bit	15	14	13	12	11	10	9	8
	LCEN				INTP	INTN		
Access	R/W				R/W	R/W		
Reset	0				0	0		

Bit	7	6	5	4	3	2	1	0
	LCOE	LCOUT	LCPOL			MODE[2:0]		
Access	R/W	R	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bit 15 – LCEN CLC Enable bit

Value	Description
1	CLC is enabled and mixing input signals
0	CLC is disabled and has logic zero outputs

Bit 11 – INTP CLC Positive Edge Interrupt Enable bit

Value	Description
1	Interrupt will be generated when a rising edge occurs on LCOUT
0	Interrupt will not be generated

Bit 10 – INTN CLC Negative Edge Interrupt Enable bit

Value	Description
1	Interrupt will be generated when a falling edge occurs on LCOUT
0	Interrupt will not be generated

Bit 7 – LCOE CLC Port Enable bit

Value	Description
1	CLC port pin output is enabled
0	CLC port pin output is disabled

Bit 6 – LCOUT CLC Data Output Status bit

Value	Description
1	CLC output high
0	CLC output low

Bit 5 – LCPOL CLC Output Polarity Control bit

Value	Description
1	The output of the module is inverted
0	The output of the module is not inverted

Bits 2:0 – MODE[2:0] CLC Mode bits

Value	Description
111	Cell is a 1-input transparent latch with S and R
110	Cell is a JK flip-flop with R
101	Cell is a 2-input D flip-flop with R
100	Cell is a 1-input D flip-flop with S and R
011	Cell is an SR latch
010	Cell is a 4-input AND
001	Cell is an OR-XOR
000	Cell is an AND-OR

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20.1.18 CLC4 Control Register High

Name: CLC4CONH
Offset: 0x48A

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					G4POL	G3POL	G2POL	G1POL
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – G4POL Gate 4 Polarity Control bit

Value	Description
1	The output of Channel 4 logic is inverted when applied to the logic cell
0	The output of Channel 4 logic is not inverted

Bit 2 – G3POL Gate 3 Polarity Control bit

Value	Description
1	The output of Channel 3 logic is inverted when applied to the logic cell
0	The output of Channel 3 logic is not inverted

Bit 1 – G2POL Gate 2 Polarity Control bit

Value	Description
1	The output of Channel 2 logic is inverted when applied to the logic cell
0	The output of Channel 2 logic is not inverted

Bit 0 – G1POL Gate 1 Polarity Control bit

Value	Description
1	The output of Channel 1 logic is inverted when applied to the logic cell
0	The output of Channel 1 logic is not inverted

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20.1.19 CLC4 Input MUX Select Register

Name: CLC4SEL
Offset: 0x48C

Bit	15	14	13	12	11	10	9	8
		DS4[2:0]				DS3[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
		DS2[2:0]				DS1[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bits 14:12 – DS4[2:0] Data Selection MUX 4 Signal Selection bits

Value	Description
111	MCCP3 OCMP output
110	MCCP1 OCMP output
101	Unimplemented
100	Unimplemented
011	SPI2 Input (SDI2)
010	Comparator 3 output
001	CLC3 output
000	CLCIND pin

Bits 10:8 – DS3[2:0] Data Selection MUX 3 Signal Selection bits

Value	Description
111	MCCP3 OCMP output
110	MCCP2 OCMP output
101	DMA Channel 1 Interrupt
100	UART2 Input (U2RX)
011	SPI2 Output (SDO2)
010	Comparator 2 output
001	CLC2 output
000	CLCINC pin

Bits 6:4 – DS2[2:0] Data Selection MUX 2 Signal Selection bits

Value	Description
111	MCCP2 OCMP output
110	MCCP1 OCMP output
101	DMA Channel 0 Interrupt
100	A/D conversion done
011	UART2 Output (U2TX)
010	Comparator 1 output
001	CLC1 output
000	CLCINB pin

Bits 2:0 – DS1[2:0] Data Selection MUX 1 Signal Selection bits

Value	Description
111	Timer3 match event
110	Timer2 match event
101	Unimplemented
100	Reference Clock Output (REFO)
011	LPRC

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Value	Description
010	SOSC
001	Peripheral clock (F_{PB})
000	CLCINA pin

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20.1.20 CLC4 Gate Logic Input Select Low Register

Name: CLC4GLSL
Offset: 0x490

Bit	15	14	13	12	11	10	9	8
	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – G2D4T Gate 2 Data Source 4 True Enable bit

Value	Description
1	The Data Source 4 signal is enabled for Gate 2
0	The Data Source 4 signal is disabled for Gate 2

Bit 14 – G2D4N Gate 2 Data Source 4 Negated Enable bit

Value	Description
1	The Data Source 4 inverted signal is enabled for Gate 2
0	The Data Source 4 inverted signal is disabled for Gate 2

Bit 13 – G2D3T Gate 2 Data Source 3 True Enable bit

Value	Description
1	The Data Source 3 signal is enabled for Gate 2
0	The Data Source 3 signal is disabled for Gate 2

Bit 12 – G2D3N Gate 2 Data Source 3 Negated Enable bit

Value	Description
1	The Data Source 3 inverted signal is enabled for Gate 2
0	The Data Source 3 inverted signal is disabled for Gate 2

Bit 11 – G2D2T Gate 2 Data Source 2 True Enable bit

Value	Description
1	The Data Source 2 signal is enabled for Gate 2
0	The Data Source 2 signal is disabled for Gate 2

Bit 10 – G2D2N Gate 2 Data Source 2 Negated Enable bit

Value	Description
1	The Data Source 2 inverted signal is enabled for Gate 2
0	The Data Source 2 inverted signal is disabled for Gate 2

Bit 9 – G2D1T Gate 2 Data Source 1 True Enable bit

Value	Description
1	The Data Source 1 signal is enabled for Gate 2
0	The Data Source 1 signal is disabled for Gate 2

Bit 8 – G2D1N Gate 2 Data Source 1 Negated Enable bit

Value	Description
1	The Data Source 1 inverted signal is enabled for Gate 2
0	The Data Source 1 inverted signal is disabled for Gate 2

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Bit 7 – G1D4T Gate 1 Data Source 4 True Enable bit

Value	Description
1	The Data Source 4 signal is enabled for Gate 1
0	The Data Source 4 signal is disabled for Gate 1

Bit 6 – G1D4N Gate 1 Data Source 4 Negated Enable bit

Value	Description
1	The Data Source 4 inverted signal is enabled for Gate 1
0	The Data Source 4 inverted signal is disabled for Gate 1

Bit 5 – G1D3T Gate 1 Data Source 3 True Enable bit

Value	Description
1	The Data Source 3 signal is enabled for Gate 1
0	The Data Source 3 signal is disabled for Gate 1

Bit 4 – G1D3N Gate 1 Data Source 3 Negated Enable bit

Value	Description
1	The Data Source 3 inverted signal is enabled for Gate 1
0	The Data Source 3 inverted signal is disabled for Gate 1

Bit 3 – G1D2T Gate 1 Data Source 2 True Enable bit

Value	Description
1	The Data Source 2 signal is enabled for Gate 1
0	The Data Source 2 signal is disabled for Gate 1

Bit 2 – G1D2N Gate 1 Data Source 2 Negated Enable bit

Value	Description
1	The Data Source 2 inverted signal is enabled for Gate 1
0	The Data Source 2 inverted signal is disabled for Gate 1

Bit 1 – G1D1T Gate 1 Data Source 1 True Enable bit

Value	Description
1	The Data Source 1 signal is enabled for Gate 1
0	The Data Source 1 signal is disabled for Gate 1

Bit 0 – G1D1N Gate 1 Data Source 1 Negated Enable bit

Value	Description
1	The Data Source 1 inverted signal is enabled for Gate 1
0	The Data Source 1 inverted signal is disabled for Gate 1

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20.1.21 CLC4 Gate Logic Input Select High Register

Name: CLC4GLSH
Offset: 0x492

Bit	15	14	13	12	11	10	9	8
	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – G4D4T Gate 4 Data Source 4 True Enable bit

Value	Description
1	The Data Source 4 signal is enabled for Gate 4
0	The Data Source 4 signal is disabled for Gate 4

Bit 14 – G4D4N Gate 4 Data Source 4 Negated Enable bit

Value	Description
1	The Data Source 4 inverted signal is enabled for Gate 4
0	The Data Source 4 inverted signal is disabled for Gate 4

Bit 13 – G4D3T Gate 4 Data Source 3 True Enable bit

Value	Description
1	The Data Source 3 signal is enabled for Gate 4
0	The Data Source 3 signal is disabled for Gate 4

Bit 12 – G4D3N Gate 4 Data Source 3 Negated Enable bit

Value	Description
1	The Data Source 3 inverted signal is enabled for Gate 4
0	The Data Source 3 inverted signal is disabled for Gate 4

Bit 11 – G4D2T Gate 4 Data Source 2 True Enable bit

Value	Description
1	The Data Source 2 signal is enabled for Gate 4
0	The Data Source 2 signal is disabled for Gate 4

Bit 10 – G4D2N Gate 4 Data Source 2 Negated Enable bit

Value	Description
1	The Data Source 2 inverted signal is enabled for Gate 4
0	The Data Source 2 inverted signal is disabled for Gate 4

Bit 9 – G4D1T Gate 4 Data Source 1 True Enable bit

Value	Description
1	The Data Source 1 signal is enabled for Gate 4
0	The Data Source 1 signal is disabled for Gate 4

Bit 8 – G4D1N Gate 4 Data Source 1 Negated Enable bit

Value	Description
1	The Data Source 1 inverted signal is enabled for Gate 4
0	The Data Source 1 inverted signal is disabled for Gate 4

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Bit 7 – G3D4T Gate 3 Data Source 4 True Enable bit

Value	Description
1	The Data Source 4 signal is enabled for Gate 3
0	The Data Source 4 signal is disabled for Gate 3

Bit 6 – G3D4N Gate 3 Data Source 4 Negated Enable bit

Value	Description
1	The Data Source 4 inverted signal is enabled for Gate 3
0	The Data Source 4 inverted signal is disabled for Gate 3

Bit 5 – G3D3T Gate 3 Data Source 3 True Enable bit

Value	Description
1	The Data Source 3 signal is enabled for Gate 3
0	The Data Source 3 signal is disabled for Gate 3

Bit 4 – G3D3N Gate 3 Data Source 3 Negated Enable bit

Value	Description
1	The Data Source 3 inverted signal is enabled for Gate 3
0	The Data Source 3 inverted signal is disabled for Gate 3

Bit 3 – G3D2T Gate 3 Data Source 2 True Enable bit

Value	Description
1	The Data Source 2 signal is enabled for Gate 3
0	The Data Source 2 signal is disabled for Gate 3

Bit 2 – G3D2N Gate 3 Data Source 2 Negated Enable bit

Value	Description
1	The Data Source 2 inverted signal is enabled for Gate 3
0	The Data Source 2 inverted signal is disabled for Gate 3

Bit 1 – G3D1T Gate 3 Data Source 1 True Enable bit

Value	Description
1	The Data Source 1 signal is enabled for Gate 3
0	The Data Source 1 signal is disabled for Gate 3

Bit 0 – G3D1N Gate 3 Data Source 1 Negated Enable bit

Value	Description
1	The Data Source 1 inverted signal is enabled for Gate 3
0	The Data Source 1 inverted signal is disabled for Gate 3

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21. 12-Bit A/D Converter with Threshold Detect

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the 12-Bit A/D Converter, refer to **"12-Bit A/D Converter with Threshold Detect"** (www.microchip.com/DS39739) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

The A/D Converter has the following key features:

- Successive Approximation Register (SAR) Conversion
- Selectable 10-Bit or 12-Bit (default) Conversion Resolution
- Up to 17 Analog Input Channels (internal and external)
- Multiple Internal Reference Input Channels
- External Voltage Reference Input Pins
- Unipolar Differential Sample-and-Hold (S/H) Amplifier
- Automated Threshold Scan and Compare Operation to Pre-Evaluate Conversion Results
- Selectable Conversion Trigger Source
- Fixed Length (one word per channel), Configurable Conversion Result Buffer
- Four Options for Results Alignment
- Configurable Interrupt Generation
- Enhanced DMA Operations with Indirect Address Generation
- Operation During CPU Sleep and Idle modes

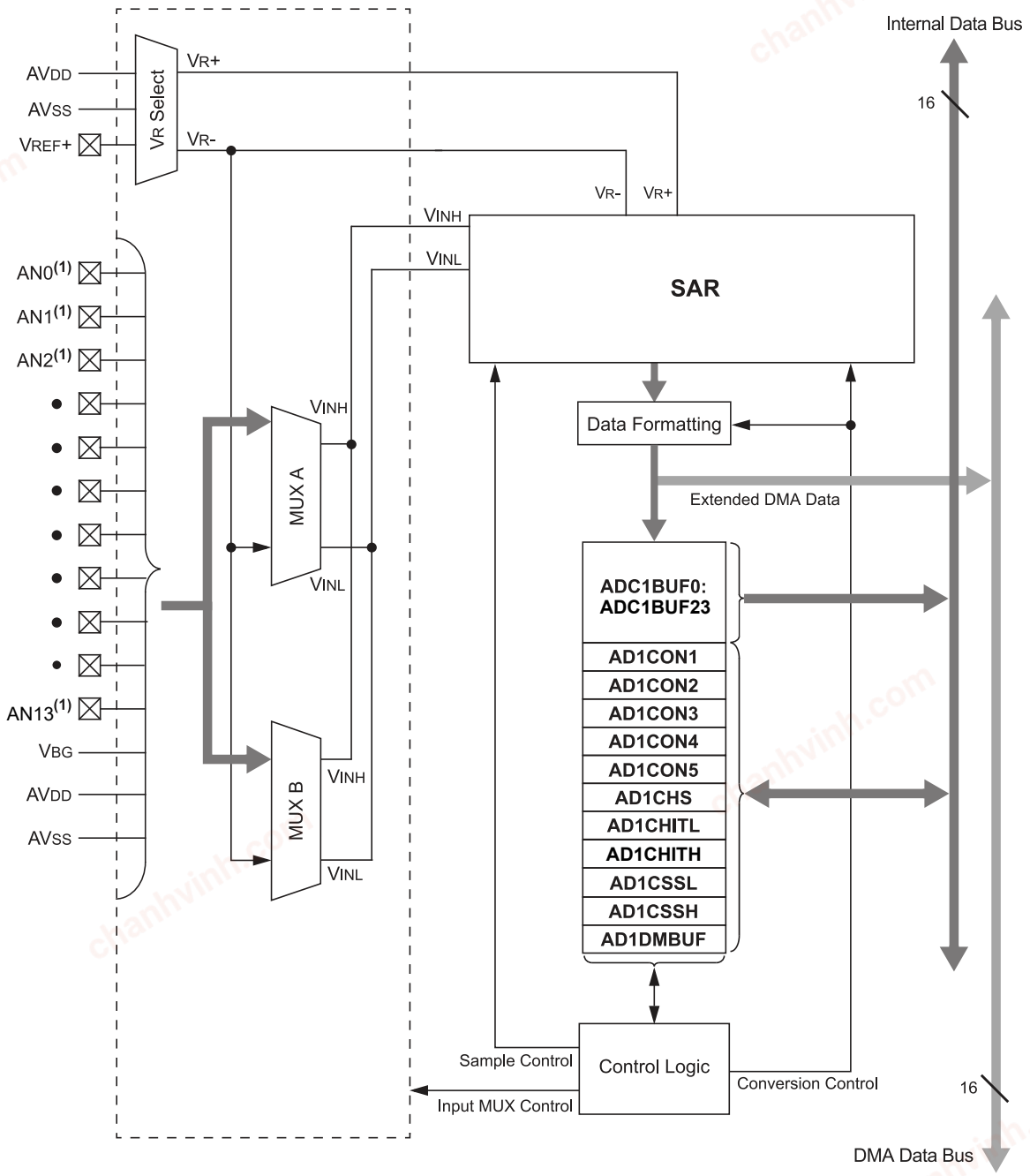
The 12-bit A/D Converter module is an enhanced version of the 10-bit module offered in earlier PIC24 devices. It is a Successive Approximation Register (SAR) Converter, enhanced with 12-bit resolution, a wide range of automatic sampling options, tighter integration with other analog modules and a configurable results buffer.

It also includes a unique Threshold Detect feature that allows the module itself to make simple decisions based on the conversion results, and enhanced operation with the DMA Controller through Peripheral Indirect Addressing (PIA).

A simplified block diagram for the module is shown in Figure 21-1.

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Figure 21-1. 12-Bit A/D Converter Block Diagram (PIC24FJ64GP205/GU205 Family)



Note:

1. Available ANx pins are package-dependent.

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21.1 Basic Operation

To perform a standard A/D conversion:

1. Configure the module:
   1.1. Configure port pins as analog inputs by setting the appropriate bits in the ANSx registers (see 11.2 Configuring Analog Port Pins for more information).
   1.2. Select the voltage reference source to match the expected range on analog inputs (AD1CON2[15:13]).
   1.3. Select the positive and negative multiplexer inputs for each channel (AD1CHS[15:0]).
   1.4. Select the analog conversion clock to match the desired data rate with the processor clock (AD1CON3[7:0]).
   1.5. Select the appropriate sample/conversion sequence (AD1CON1[7:4] and AD1CON3[12:8]).
   1.6. For Channel A scanning operations, select the positive channels to be included (AD1CSSH and AD1CSSL registers).
   1.7. Select how conversion results are presented in the buffer (AD1CON1[9:8] and AD1CON5 register).
   1.8. Select the interrupt rate (AD1CON2[6:2]).
   1.9. Turn on A/D module (AD1CON1[15]).
2. Configure the A/D interrupt (if required):
   2.1. Clear the AD1IF bit (IFS0[13]).
   2.2. Enable the AD1IE interrupt (IEC0[13]).
   2.3. Select the A/D interrupt priority (IPC3[6:4]).
3. If the module is configured for manual sampling, set the SAMP bit (AD1CON1[1]) to begin sampling.

21.2 Extended DMA Operations

In addition to the standard features available on all 12-bit A/D Converters, PIC24FJ64GP205/GU205 family devices implement a limited extension of DMA functionality. This extension adds features that work with the device's DMA Controller to expand the A/D module's data storage abilities beyond the module's built-in buffer.

The Extended DMA functionality is controlled by the DMAEN bit (AD1CON1[11]); setting this bit enables the functionality. The DMABM bit (AD1CON1[12]) configures how the DMA feature operates.

21.2.1 Extended Buffer Mode

Extended Buffer mode (DMABM = 1) maps the A/D Data Buffer registers and data from all channels, above 13, into a user-specified area of data RAM. This allows users to read the conversion results of channels above 13, which do not have their own memory-mapped A/D buffer locations, from data memory.

To accomplish this, the DMA must be configured in Peripheral Indirect Addressing mode and the DMA destination address must point to the beginning of the buffer. The DMA count must be set to generate an interrupt after the desired number of conversions.

In Extended Buffer mode, the A/D control bits will function similarly to non-DMA modes. The BUFREGEN bit will still select between FIFO mode and Channel-Aligned mode, but the number of words in the destination FIFO will be determined by the SMPI[4:0] bits in DMA mode. In FIFO mode, the BUFM bit will still split the output FIFO into two sets of 13 results (the SMPIx bits should be set accordingly) and the BUFS bit will still indicate which set of results is being written to and which can be read.

21.2.2 PIA Mode

When DMABM = 0, the A/D module is configured to function with the DMA Controller for Peripheral Indirect Addressing (PIA) mode operations. In this mode, the A/D module generates an 11-bit Indirect Address (IA). This is ORed with the destination address in the DMA Controller to define where the A/D conversion data will be stored.

In PIA mode, the buffer space is created as a series of contiguous smaller buffers, one per analog channel. The size of the channel buffer determines how many analog channels can be accommodated. The size of the buffer is selected by the DMABL[2:0] bits (AD1CON4[2:0]). The size options range from a single word per buffer to 128 words.

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Each channel is allocated a buffer of this size, regardless of whether or not the channel will actually have conversion data.

The IA is created by combining the base address within a channel buffer with three to five bits (depending on the buffer size) to identify the channel. The base address ranges from zero to seven bits wide, depending on the buffer size. The address is right-padded with a '0' in order to maintain address alignment in the Data Space. The concatenated channel and base address bits are then left-padded with zeros, as necessary, to complete the 11-bit IA.

The IA is configured to auto-increment which channel is written in each analog input's sub-buffer, during write operations, by using the SMPIx bits (AD1CON2[6:2]).

As with PIA operations for any DMA-enabled module, the base destination address in the DMADSTn register must be masked properly to accommodate the IA. Table 21-1 shows how complete addresses are formed. Note that the address masking varies for each buffer size option. Because of masking requirements, some address ranges may not be available for certain buffer sizes. Users should verify that the DMA base address is compatible with the buffer size selected.

Table 21-1. Indirect Address Generation in PIA Mode

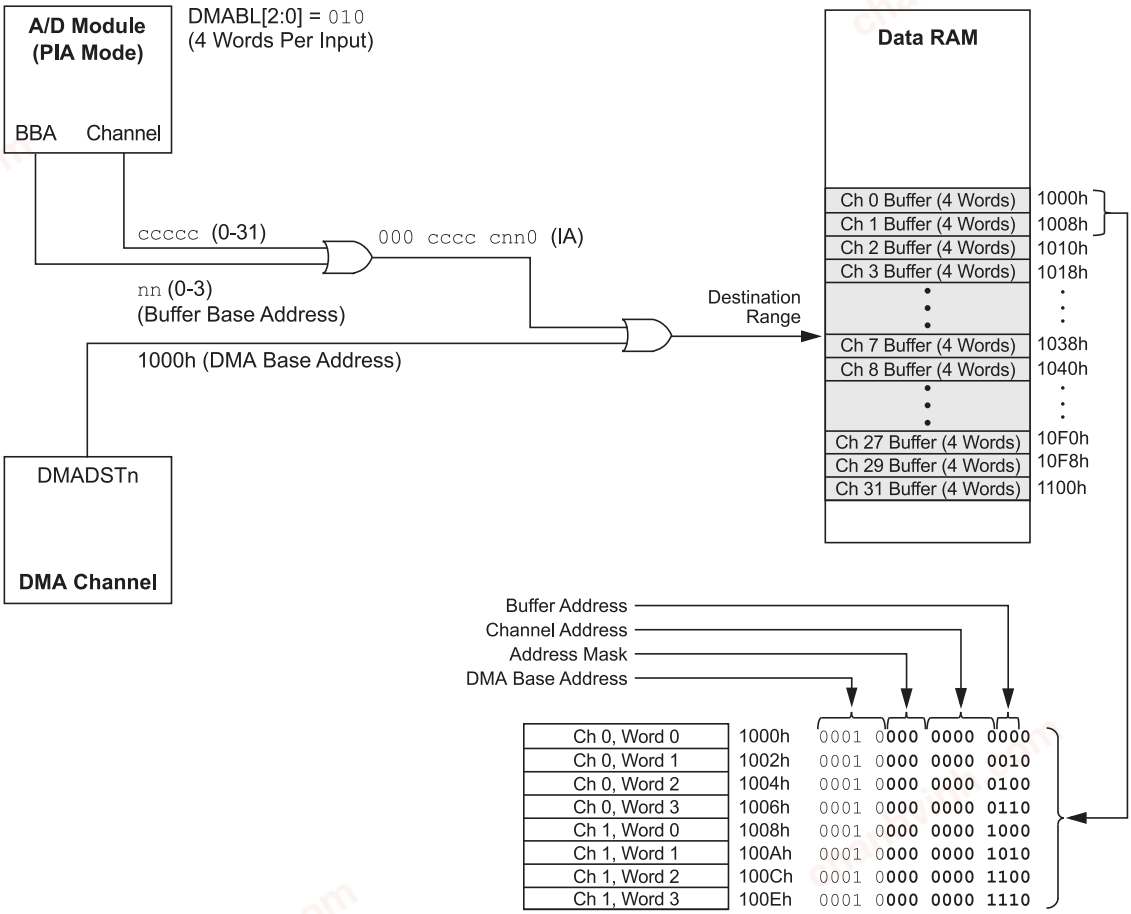
DMABL[2:0]	Buffer Size per Channel (words)	Generated Offset Address (lower 11 bits)	Available Input Channels	Allowable DMADSTn Addresses
000	1	000 00cc ccc0	32	xxxx xxxx xx00 0000
001	2	000 0ccc ccn0	32	xxxx xxxx x000 0000
010	4	000 cccc cnn0	32	xxxx xxxx 0000 0000
011	8	00c cccc nnn0	32	xxxx xxx0 0000 0000
100	16	0cc cccn nnn0	32	xxxx xx00 0000 0000
101	32	ccc ccnn nnn0	32	xxxx x000 0000 0000
110	64	ccc cnnn nnn0	16	xxxx x000 0000 0000
111	128	ccc nnnn nnn0	8	xxxx x000 0000 0000

Legend: ccc = Channel number (three to five bits), n = Base buffer address (zero to seven bits), x = User-definable range of DMADSTn for base address, 0 = Masked bits of DMADSTn for IA.

Figure 21-2 shows how the parts of the address define the buffer locations in data memory. In this case, the module "allocates" 256 bytes of data RAM (1000h to 1100h) for 32 buffers of four words each. However, this is not a hard allocation and nothing prevents these locations from being used for other purposes. For example, in the current case, if Analog Channels 1, 3 and 8 are being sampled and converted, conversion data will only be written to the channel buffers, starting at 1008h, 1018h and 1040h. The holes in the PIA buffer space can be used for any other purpose. It is the user's responsibility to keep track of buffer locations and prevent data overwrites.

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Figure 21-2. Example of Buffer Address Generation in PIA Mode (4-Word Buffers per Channel)

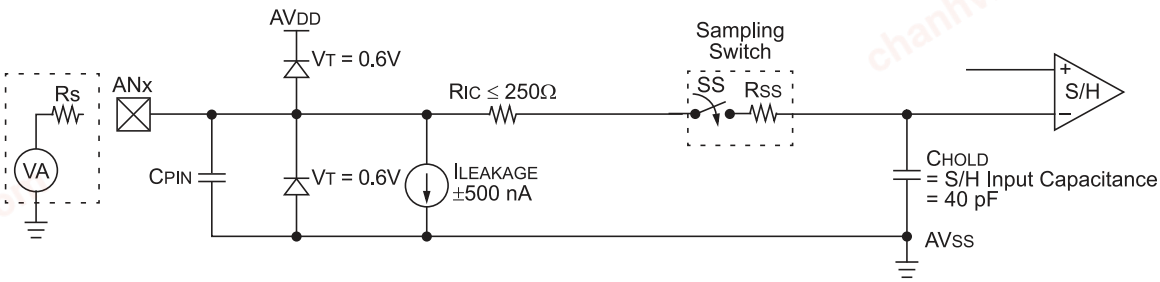


21.3 Sampling Time Requirements

The analog input model of the 12-Bit High-Speed, Multiple SARs ADC is illustrated in Figure 21-3. The total acquisition time for the Analog-to-Digital conversion is a function of the Holding Capacitor (C_{HOLD}) charge time. For the ADC module to meet its specified accuracy, the Holding Capacitor (C_{HOLD}) must be allowed to fully charge to the voltage level on the analog input pin. The analog output Source Impedance (R_S), the Interconnect Impedance (R_{IC}) and the internal Sampling Switch Impedance (R_{SS}) combine to directly affect the time required to charge the C_{HOLD}. The combined impedance of the analog sources must, therefore, be small enough to fully charge the Holding Capacitor within the selected sample time.

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Figure 21-3. 12-Bit A/D Converter Analog Input Model



Legend:	CPIN	= Input Capacitance
	VT	= Threshold Voltage
	ILEAKAGE	= Leakage Current at the pin due to Various Junctions
	RIC	= Interconnect Resistance
	RSS	= Sampling Switch Resistance
	CHOLD	= Sample/Hold Capacitance

Sampling Switch ($R_{SS} \leq 3\ k\Omega$)

Note: The C_{PIN} value depends on the device package and is not tested. The effect of C_{PIN} is negligible if Rs ≤ 2.5 kΩ.

To charge this capacitor to the input signal level with precision 0.5 LSB, the following sampling time is required:

$T_{SAMPLE} = R_{TOTAL} \times C_{HOLD} \times \ln(2_{Number\ Bits\ +1})$ or

$T_{SAMPLE} = R_{TOTAL} \times C_{HOLD} \times \ln(2048) = 7.6 \times 40\ pF \times R_{TOTAL}$ for 10-bit mode and

$T_{SAMPLE} = R_{TOTAL} \times C_{HOLD} \times \ln(8192) = 9 \times 40\ pF \times R_{TOTAL}$ for 12-bit mode,

where $R_{TOTAL} = R_S + R_{IC} + R_{SS}$

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21.4 12-Bit A/D Converter Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x02F3	Reserved									
0x02F4	ANCFG	7:0					VBGEN4	VBGEN3	VBGEN2	VBGEN1
		15:8								
0x02F6 ... 0x06FF	Reserved									
0x0700	ADC1BUF0	7:0	ADC1BUF0[7:0]							
		15:8	ADC1BUF0[15:8]							
0x0702	ADC1BUF1	7:0	ADC1BUF1[7:0]							
		15:8	ADC1BUF1[15:8]							
0x0704	ADC1BUF2	7:0	ADC1BUF2[7:0]							
		15:8	ADC1BUF2[15:8]							
0x0706	ADC1BUF3	7:0	ADC1BUF3[7:0]							
		15:8	ADC1BUF3[15:8]							
0x0708	ADC1BUF4	7:0	ADC1BUF4[7:0]							
		15:8	ADC1BUF4[15:8]							
0x070A	ADC1BUF5	7:0	ADC1BUF5[7:0]							
		15:8	ADC1BUF5[15:8]							
0x070C	ADC1BUF6	7:0	ADC1BUF6[7:0]							
		15:8	ADC1BUF6[15:8]							
0x070E	ADC1BUF7	7:0	ADC1BUF7[7:0]							
		15:8	ADC1BUF7[15:8]							
0x0710	ADC1BUF8	7:0	ADC1BUF8[7:0]							
		15:8	ADC1BUF8[15:8]							
0x0712	ADC1BUF9	7:0	ADC1BUF9[7:0]							
		15:8	ADC1BUF9[15:8]							
0x0714	ADC1BUF10	7:0	ADC1BUF10[7:0]							
		15:8	ADC1BUF10[15:8]							
0x0716	ADC1BUF11	7:0	ADC1BUF11[7:0]							
		15:8	ADC1BUF11[15:8]							
0x0718	ADC1BUF12	7:0	ADC1BUF12[7:0]							
		15:8	ADC1BUF12[15:8]							
0x071A	ADC1BUF13	7:0	ADC1BUF13[7:0]							
		15:8	ADC1BUF13[15:8]							
0x071C ... 0x0733	Reserved									
0x0734	AD1CON1	7:0	SSRC[3:0]					ASAM	SAMP	DONE
		15:8	ADON		ADSIDL	DMABM	DMAEN	MODE12	FORM[1:0]	
0x0736	AD1CON2	7:0	BUFS	SMPI[4:0]					BUFM	ALTS
		15:8	PVCFG[1:0]		NVCFG0	Reserved	BUFREGEN	CSCNA		
0x0738	AD1CON3	7:0	ADCS[7:0]							
		15:8	ADRC	EXTSAM	PUMPEN	SAMC[4:0]				
0x073A	AD1CHS	7:0	CH0NA[2:0]			CH0SA[4:0]				
		15:8	CH0NB[2:0]			CH0SB[2:0]				
0x073C	AD1CSSH	7:0								
		15:8		CSS[30:28]						
0x073E	AD1CSSL	7:0	CSS[7:0]							
		15:8				CSS[4:0]				
0x0740	AD1CON4	7:0						DMABL[2:0]		
		15:8								
0x0742	AD1CON5	7:0					WM[1:0]		CM[1:0]	
		15:8	ASEN	LPEN		BGREQ			ASINT[1:0]	

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.....continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0744 ... 0x0745	Reserved									
0x0746	AD1CHITL	7:0	CHH[7:0]							
		15:8			CHH[13:8]					
0x0748 ... 0x074B	Reserved									
0x074C	AD1DMBUF	7:0	AD1DMBUF[7:0]							
		15:8	AD1DMBUF[15:8]							

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21.4.1 ADC1 Buffer 0 Register

Name: ADC1BUF0
Offset: 0x700

Bit	15	14	13	12	11	10	9	8
	ADC1BUF0[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADC1BUF0[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ADC1BUF0[15:0] Buffer Data bits

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21.4.2 ADC1 Buffer 1 Register

Name: ADC1BUF1
Offset: 0x702

Bit	15	14	13	12	11	10	9	8
	ADC1BUF1[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADC1BUF1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ADC1BUF1[15:0] Buffer Data bits

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21.4.3 ADC1 Buffer 2 Register

Name: ADC1BUF2
Offset: 0x704

Bit	15	14	13	12	11	10	9	8
	ADC1BUF2[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADC1BUF2[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ADC1BUF2[15:0] Buffer Data bits

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21.4.4 ADC1 Buffer 3 Register

Name: ADC1BUF3
Offset: 0x706

Bit	15	14	13	12	11	10	9	8
	ADC1BUF3[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADC1BUF3[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ADC1BUF3[15:0] Buffer Data bits

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21.4.5 ADC1 Buffer 4 Register

Name: ADC1BUF4
Offset: 0x708

Bit	15	14	13	12	11	10	9	8
	ADC1BUF4[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADC1BUF4[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ADC1BUF4[15:0] Buffer Data bits

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21.4.6 ADC1 Buffer 5 Register

Name: ADC1BUF5
Offset: 0x70A

Bit	15	14	13	12	11	10	9	8
	ADC1BUF5[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADC1BUF5[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ADC1BUF5[15:0] Buffer Data bits

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21.4.7 ADC1 Buffer 6 Register

Name: ADC1BUF6
Offset: 0x70C

Bit	15	14	13	12	11	10	9	8
	ADC1BUF6[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADC1BUF6[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ADC1BUF6[15:0] Buffer Data bits

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21.4.8 ADC1 Buffer 7 Register

Name: ADC1BUF7
Offset: 0x70E

Bit	15	14	13	12	11	10	9	8
	ADC1BUF7[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADC1BUF7[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ADC1BUF7[15:0] Buffer Data bits

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21.4.9 ADC1 Buffer 8 Register

Name: ADC1BUF8
Offset: 0x710

Bit	15	14	13	12	11	10	9	8
	ADC1BUF8[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADC1BUF8[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ADC1BUF8[15:0] Buffer Data bits

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21.4.10 ADC1 Buffer 9 Register

Name: ADC1BUF9
Offset: 0x712

Bit	15	14	13	12	11	10	9	8
	ADC1BUF9[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADC1BUF9[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ADC1BUF9[15:0] Buffer Data bits

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21.4.11 ADC1 Buffer 10 Register

Name: ADC1BUF10
Offset: 0x714

Bit	15	14	13	12	11	10	9	8
	ADC1BUF10[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADC1BUF10[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ADC1BUF10[15:0] Buffer Data bits

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21.4.12 ADC1 Buffer 11 Register

Name: ADC1BUF11
Offset: 0x716

Bit	15	14	13	12	11	10	9	8
	ADC1BUF11[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADC1BUF11[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ADC1BUF11[15:0] Buffer Data bits

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21.4.13 ADC1 Buffer 12 Register

Name: ADC1BUF12
Offset: 0x718

Bit	15	14	13	12	11	10	9	8
	ADC1BUF12[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADC1BUF12[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ADC1BUF12[15:0] Buffer Data bits

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21.4.14 ADC1 Buffer 13 Register

Name: ADC1BUF13
Offset: 0x71A

Bit	15	14	13	12	11	10	9	8
	ADC1BUF13[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADC1BUF13[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ADC1BUF13[15:0] Buffer Data bits

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21.4.15 A/D Control Register 1

Name: AD1CON1
Offset: 0x734

Note:
1. This bit is only available when Extended DMA and buffer features are available (DMAEN = 1).

Bit	15	14	13	12	11	10	9	8
	ADON		ADSIDL	DMABM	DMAEN	MODE12	FORM[1:0]	
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SSRC[3:0]					ASAM	SAMP	DONE
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit 15 – ADON A/D Operating Mode bit

Value	Description
1	A/D Converter is operating
0	A/D Converter is off

Bit 13 – ADSIDL A/D Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode
0	Continues module operation in Idle mode

Bit 12 – DMABM Extended DMA Buffer Mode Select bit(1)

Value	Description
1	Extended Buffer mode: Buffer address is defined by the DMADSTn register
0	PIA mode: Buffer addresses are defined by the DMA Controller and AD1CON4[2:0]

Bit 11 – DMAEN Extended DMA/Buffer Enable bit

Value	Description
1	Extended DMA and buffer features are enabled
0	Extended features are disabled

Bit 10 – MODE12 A/D 12-Bit Operation Mode bit

Value	Description
1	12-bit A/D operation
0	10-bit A/D operation

Bits 9:8 – FORM[1:0] Data Output Format bits (see following formats)

Value	Description
11	Fractional result, signed, left-justified
10	Absolute fractional result, unsigned, left-justified
01	Decimal result, signed, right-justified
00	Absolute decimal result, unsigned, right-justified

Bits 7:4 – SSRC[3:0] Sample Clock Source Select bits

Value	Description
0111	Auto-Convert mode
0110	Timer1 (may trigger during Sleep mode)
0101	Timer1 (will not trigger during Sleep mode)
0011	Reserved

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Value	Description
0010	Timer3
0001	INT0
0000	SAMP is cleared by software

Bit 2 – ASAM A/D Sample Auto-Start bit

Value	Description
1	Sampling begins immediately after last conversion; SAMP bit is auto-set
0	Sampling begins when SAMP bit is manually set

Bit 1 – SAMP A/D Sample Enable bit

Value	Description
1	A/D Sample-and-Hold amplifiers are sampling
0	A/D Sample-and-Hold amplifiers are holding

Bit 0 – DONE A/D Conversion Status bit

Value	Description
1	A/D conversion cycle has completed
0	A/D conversion cycle has not started or is in progress

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21.4.16 A/D Control Register 2

Name: AD1CON2
Offset: 0x736

Legend: r = Reserved bit

Bit	15	14	13	12	11	10	9	8
	PVCFG[1:0]		NVCFG0	Reserved	BUFREGEN	CSCNA		
Access	R/W	R/W	R/W	r	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
	BUFS	SMPI[4:0]					BUFM	ALTS
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:14 – PVCFG[1:0] A/D Converter Positive Voltage Reference Configuration bits

Value	Description
1x	Unimplemented, do not use
01	External V_{REF}+
00	AV_{DD}

Bit 13 – NVCFG0 A/D Converter Negative Voltage Reference Configuration bit

Value	Description
1	Unimplemented
0	AV_{SS}

Bit 12 – Reserved Maintain as '0'

Bit 11 – BUFREGEN A/D Buffer Register Enable bit

Value	Description
1	Conversion result is loaded into the buffer location determined by the converted channel
0	A/D result buffer is treated as a FIFO

Bit 10 – CSCNA Scan Input Selections for CH0+ During Sample A bit

Value	Description
1	Scans inputs
0	Does not scan inputs

Bit 7 – BUFS Buffer Fill Status bit
When DMAEN = 1 and DMABM = 1:

Value	Description
1	A/D is currently filling the destination buffer from [buffer start + (buffer size/2)] to [buffer start + (buffer size – 1)]. User should access data located from [buffer start] to [buffer start + (buffer size/2) – 1].
0	A/D is currently filling the destination buffer from [buffer start] to [buffer start + (buffer size/2) – 1]. User should access data located from [buffer start + (buffer size/2)] to [buffer start + (buffer size – 1)].

When DMAEN = 0:

Value	Description
1	A/D is currently filling ADC1BUF12-ADC1BUF23; user should access data in ADC1BUF0-ADC1BUF11
0	A/D is currently filling ADC1BUF0-ADC1BUF11; user should access data in ADC1BUF12-ADC1BUF23

Bits 6:2 – SMPI[4:0] Interrupt Sample/DMA Increment Rate Select bits
When DMAEN = 1 and DMABM = 0:

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Value	Description
11111	Increments the DMA address after completion of the 32nd sample/conversion operation
11110	Increments the DMA address after completion of the 31st sample/conversion operation
...	
00001	Increments the DMA address after completion of the 2nd sample/conversion operation
00000	Increments the DMA address after completion of each sample/conversion operation

When DMAEN = 1 and DMABM = 1:

Value	Description
11111	Resets the DMA offset after completion of the 32nd sample/conversion operation
11110	Resets the DMA offset after completion of the 31st sample/conversion operation
...	
00001	Resets the DMA offset after completion of the 2nd sample/conversion operation
00000	Resets the DMA offset after completion of every sample/conversion operation

When DMAEN = 0:

Value	Description
11111	Interrupts at the completion of the conversion for each 32nd sample
11110	Interrupts at the completion of the conversion for each 31st sample
...	
00001	Interrupts at the completion of the conversion for every other sample
00000	Interrupts at the completion of the conversion for each sample

Bit 1 – BUFM Buffer Fill Mode Select bit

Value	Description
1	Starts buffer filling at ADC1BUF0 on first interrupt and ADC1BUF12 on next interrupt
0	Always starts filling buffer at ADC1BUF0

Bit 0 – ALTS Alternate Input Sample Mode Select bit

Value	Description
1	Uses channel input selects for Sample A on first sample and Sample B on next sample
0	Always uses channel input selects for Sample A

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21.4.17 A/D Control Register 3

Name: AD1CON3
Offset: 0x738

Notes:

1. Selecting the internal ADC RC clock requires that the ADCSx bits be '1' or greater. Setting ADCSx = 0 when ADRC = 1 will violate the T_{AD} (min) specification.
2. The user should enable the charge pump if AV_{DD} is < 2.7V. Longer sample times are required due to the increase of the internal resistance of the MUX if the charge pump is disabled.

Bit	15	14	13	12	11	10	9	8
	ADRC	EXTSAM	PUMPEN	SAMC[4:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADCS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – ADRC A/D Conversion Clock Source bit(1)

Value	Description
1	Dedicated ADC RC clock generator (4 MHz nominal)
0	Clock derived from system clock

Bit 14 – EXTSAM Extended Sampling Time bit

Value	Description
1	A/D is still sampling after SAMP = 0
0	A/D is finished sampling

Bit 13 – PUMPEN Charge Pump Enable bit(2)

Value	Description
1	Charge pump for switches is enabled
0	Charge pump for switches is disabled

Bits 12:8 – SAMC[4:0] Auto-Sample Time Select bits

Value	Description
11111	31 T_{AD}
...	
00001	1 T_{AD}
00000	0 T_{AD}

Bits 7:0 – ADCS[7:0] A/D Conversion Clock Select bits

Value	Description
11111111	256 * T_{PB} = T_{AD}
...	
00000001	2 * T_{PB} = T_{AD}
00000000	T_{PB} = T_{AD}

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21.4.18 A/D Sample Select Register

Name: AD1CHS
Offset: 0x73A

Note:
1. These input channels do not have corresponding memory-mapped result buffers.

Bit	15	14	13	12	11	10	9	8
	CH0NB[2:0]			CH0SB[2:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CH0NA[2:0]			CH0SA[4:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:13 – CH0NB[2:0] Sample B Channel 0 Negative Input Select bits

Value	Description
7-3	Unimplemented
2	AN1
1	Unimplemented
0	AV_{SS}

Bits 12:8 – CH0SB[2:0] Sample B Channel 0 Positive Input Select bits

Value	Description
31	Reserved
30	AV_{DD}(1)
29	AV_{SS}(1)
28	Band Gap Reference (1.2V)
27-14	Reserved
13	AN13
12	AN12
11	AN11
10	AN10
9	AN9
8	AN8
7	AN7
6	AN6
5	AN5
4	AN4
3	AN3
2	AN2
1	AN1
0	AN0

Bits 7:5 – CH0NA[2:0] Sample A Channel 0 Negative Input Select bits
Same definitions as for CHONB[2:0].

Bits 4:0 – CH0SA[4:0] Sample A Channel 0 Negative Input Select bits
Same definitions as for CHOSB[2:0].

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21.4.19 A/D Input Scan Select Register High

Name: AD1CSSH
Offset: 0x73C

Bit	15	14	13	12	11	10	9	8
		CSS[30:28]						
Access		R/W	R/W	R/W				
Reset		0	0	0				

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 14:12 – CSS[30:28] A/D Input Scan Selection bits

Value	Description
1	Includes corresponding channel for input scan
0	Skips channel for input scan

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21.4.20 A/D Input Scan Select Register Low

Name: AD1CSSL
Offset: 0x73E

Bit	15	14	13	12	11	10	9	8
				CSS[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CSS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 12:8 – CSS[4:0] A/D Input Scan Selection bits

Value	Description
1	Includes corresponding channel for input scan
0	Skips channel for input scan

Bits 7:0 – CSS[7:0] A/D Input Scan Selection bits

Value	Description
1	Includes corresponding channel for input scan
0	Skips channel for input scan

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21.4.21 A/D Control Register 4

Name: AD1CON4
Offset: 0x740

Note:

1. The DMABL[2:0] bits are only used when AD1CON1[11] = 1 and AD1CON1[12] = 0; otherwise, their value is ignored.

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						DMABL[2:0]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 2:0 – DMABL[2:0] DMA Buffer Size Select bits(1)

Value	Description
111	Allocates 128 words of buffer to each analog input
110	Allocates 64 words of buffer to each analog input
101	Allocates 32 words of buffer to each analog input
100	Allocates 16 words of buffer to each analog input
011	Allocates 8 words of buffer to each analog input
010	Allocates 4 words of buffer to each analog input
001	Allocates 2 words of buffer to each analog input
000	Allocates 1 word of buffer to each analog input

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21.4.22 A/D Control Register 5

Name: AD1CON5
Offset: 0x742

Bit	15	14	13	12	11	10	9	8
	ASEN	LPEN		BGREQ			ASINT[1:0]	
Access	R/W	R/W		R/W			R/W	R/W
Reset	0	0		0			0	0

Bit	7	6	5	4	3	2	1	0
					WM[1:0]		CM[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – ASEN Auto-Scan Enable bit

Value	Description
1	Auto-scan is enabled
0	Auto-scan is disabled

Bit 14 – LPEN Low-Power Enable bit

Value	Description
1	Low power is enabled after scan
0	Full power is enabled after scan

Bit 12 – BGREQ Band Gap Request bit

Value	Description
1	Band gap is enabled when the A/D is enabled and active
0	Band gap is not enabled by the A/D

Bits 9:8 – ASINT[1:0] Auto-Scan (Threshold Detect) Interrupt Mode bits

Value	Description
11	Interrupt after Threshold Detect sequence has completed and valid compare has occurred
10	Interrupt after valid compare has occurred
01	Interrupt after Threshold Detect sequence has completed
00	No interrupt

Bits 3:2 – WM[1:0] Write Mode bits

Value	Description
11	Reserved
10	Auto-compare only (conversion results are not saved, but interrupts are generated when a valid match occurs, as defined by the CMx and ASINTx bits)
01	Convert and save (conversion results are saved to locations as determined by the register bits when a match occurs, as defined by the CMx bits)
00	Legacy operation (conversion data are saved to a location determined by the Buffer register bits)

Bits 1:0 – CM[1:0] Compare Mode bits

Value	Description
11	Outside Window mode: Valid match occurs if the conversion result is outside of the window defined by the corresponding buffer pair
10	Inside Window mode: Valid match occurs if the conversion result is inside the window defined by the corresponding buffer pair
01	Greater Than mode: Valid match occurs if the result is greater than the value in the corresponding Buffer register
00	Less Than mode: Valid match occurs if the result is less than the value in the corresponding Buffer register

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21.4.23 A/D Scan Compare Hit Register Low

Name: AD1CHITL
Offset: 0x746

Bit	15	14	13	12	11	10	9	8
			CHH[13:8]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CHH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 13:0 – CHH[13:0] Compare Hit bits
If CM[1:0] = 11:

Value	Description
1	A/D Result Buffer n has been written with data or a match has occurred
0	A/D Result Buffer n has not been written with data

For All Other Values of CM[1:0]:

Value	Description
1	A match has occurred on A/D Result Channel n
0	No match has occurred on A/D Result Channel n

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21.4.24 A/D Conversion Result Register (for DMA PIA mode)

Name: AD1DMBUF
Offset: 0x74C

Bit	15	14	13	12	11	10	9	8
	AD1DMBUF[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	AD1DMBUF[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – AD1DMBUF[15:0] ADC Conversion Result bits

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21.4.25 A/D Band Gap Reference Configuration Register

Name: ANCFG
Offset: 0x2F4

Note:

1. When a module requests a band gap reference voltage, that reference will be enabled automatically after a brief start-up time. The user can manually enable the band gap references using the ANCFG register, before enabling the module requesting the band gap reference, to avoid this start-up time (~1 ms).

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					VBGEN4	VBGEN3	VBGEN2	VBGEN1
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – VBGEN4 USB Band Gap Buffer Control bit(1)

Value	Description
1	Band gap reference is enabled
0	Band gap reference is disabled

Bit 2 – VBGEN3 A/D Band Gap Reference Enable bit(1)

Value	Description
1	Band gap reference is enabled
0	Band gap reference is disabled

Bit 1 – VBGEN2 Comparator Band Gap Reference Enable bit(1)

Value	Description
1	Band gap reference is enabled
0	Band gap reference is disabled

Bit 0 – VBGEN1 V_{REG}, BOR, HLVD, FRC, NVM and A/D Boost Band Gap Reference Enable bit (1)

Value	Description
1	Band gap reference is enabled
0	Band gap reference is disabled

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22. Triple Comparator Module

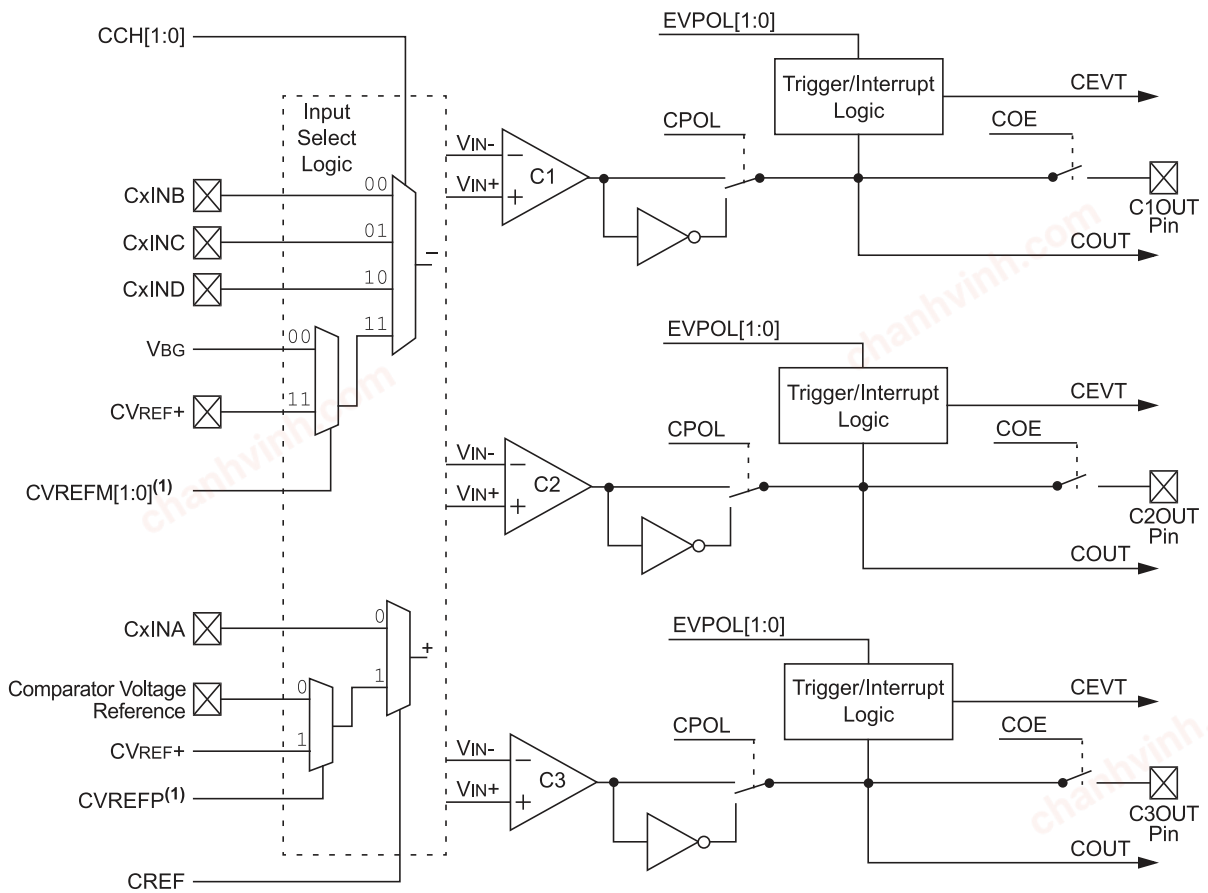
Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to **"Scalable Comparator Module"** (www.microchip.com/DS39734) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

The triple comparator module provides three dual input comparators. A simplified block diagram of the module in shown in Figure 22-1.

The comparator has the following features:

- Differential, Rail-to-Rail Inputs
- Power-Down mode for Power Savings
- Integrated Results Register
- Software-Selectable Comparator Output Polarity
- Software-Selectable Edge for Trigger/Interrupt Generation
- Software-Selectable Comparator Power mode

Figure 22-1. Triple Comparator Module Block Diagram



Note:

1. Refer to the CVRCON register (23.1.1 CVRCON) for bit details.

The inputs to the comparator can be configured to use any one of five external analog inputs (CxINA, CxINB, CxINC, CxIND and $CV_{REF}+$) and a voltage reference input from one of the internal band gap references or the comparator voltage reference generator (V_{BG} and CV_{REF}).

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The comparator outputs may be directly connected to the CxOUT pins. When the respective COE bit equals '1', the I/O pad logic makes the unsynchronized output of the comparator available on the pin.

Each comparator has its own control register, CMxCON, for enabling and configuring its operation. The output and event status of all three comparators is provided in the CMSTAT register.

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22.1 Triple Comparator Module Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x02E5	Reserved									
0x02E6	CMSTAT	7:0						C3OUT	C2OUT	C1OUT
		15:8	CMIDL					C3EVT	C2EVT	C1EVT
0x02E8 ... 0x02E9	Reserved									
0x02EA	CM1CON	7:0	EVPOL[1:0]			CREF			CCH[1:0]	
		15:8	CON	COE	CPOL				CEVT	COUT
0x02EC	CM2CON	7:0	EVPOL[1:0]			CREF			CCH[1:0]	
		15:8	CON	COE	CPOL				CEVT	COUT
0x02EE	CM3CON	7:0	EVPOL[1:0]			CREF			CCH[1:0]	
		15:8	CON	COE	CPOL				CEVT	COUT

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22.1.1 Comparator Module Status Register

Name: CMSTAT
Offset: 0x2E6

Legend: HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
	CMIDL					C3EVT	C2EVT	C1EVT
Access	R/W					HSC/R	HSC/R	HSC/R
Reset	0					0	0	0

Bit	7	6	5	4	3	2	1	0
						C3OUT	C2OUT	C1OUT
Access						HSC/R	HSC/R	HSC/R
Reset						0	0	0

Bit 15 – CMIDL Comparator Stop in Idle Mode bit

Value	Description
1	Discontinues operation of all comparators when device enters Idle mode
0	Continues operation of all enabled comparators in Idle mode

Bit 10 – C3EVT Comparator 3 Event Status bit (read-only)
Shows the current event status of Comparator 3 (CM3CON[9]).

Bit 9 – C2EVT Comparator 2 Event Status bit (read-only)
Shows the current event status of Comparator 2 (CM2CON[9]).

Bit 8 – C1EVT Comparator 1 Event Status bit (read-only)
Shows the current event status of Comparator 1 (CM1CON[9]).

Bit 2 – C3OUT Comparator 3 Output Status bit (read-only)
Shows the current output of Comparator 3 (CM3CON[8]).

Bit 1 – C2OUT Comparator 2 Output Status bit (read-only)
Shows the current output of Comparator 2 (CM2CON[8]).

Bit 0 – C1OUT Comparator 1 Output Status bit (read-only)
Shows the current output of Comparator 1 (CM1CON[8]).

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22.1.2 Comparator 1 Control Register

Name: CM1CON
Offset: 0x2EA

Legend: HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
	CON	COE	CPOL				CEVT	COUT
Access	R/W	R/W	R/W				R/W	HSC/R
Reset	0	0	0				0	0

Bit	7	6	5	4	3	2	1	0
	EVPOL[1:0]			CREF			CCH[1:0]	
Access	R/W	R/W		R/W			R/W	R/W
Reset	0	0		0			0	0

Bit 15 – CON Comparator Enable bit

Value	Description
1	Comparator is enabled
0	Comparator is disabled

Bit 14 – COE Comparator Output Enable bit

Value	Description
1	Comparator output is present on the C1OUT pin
0	Comparator output is internal only

Bit 13 – CPOL Comparator Output Polarity Select bit

Value	Description
1	Comparator output is inverted
0	Comparator output is not inverted

Bit 9 – CEVT Comparator Event bit

Value	Description
1	Comparator event that is defined by EVPOL[1:0] has occurred; subsequent triggers and interrupts are disabled until the bit is cleared
0	Comparator event has not occurred

Bit 8 – COUT Comparator Output bit

When CPOL = 1:

Value	Description
1	$V_{IN}+ < V_{IN}-$
0	$V_{IN}+ > V_{IN}-$

When CPOL = 0:

Value	Description
1	$V_{IN}+ > V_{IN}-$
0	$V_{IN}+ < V_{IN}-$

Bits 7:6 – EVPOL[1:0] Trigger/Event/Interrupt Polarity Select bits

Value	Description
11	Trigger/event/interrupt is generated on any change of the comparator output (while CEVT = 0)

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Value	Description
10	Trigger/event/interrupt is generated on transition of the comparator output: If CPOL = 1 (inverted polarity): Low-to-high transition only. If CPOL = 0 (noninverted polarity): High-to-low transition only.
01	Trigger/event/interrupt is generated on transition of comparator output: If CPOL = 1 (inverted polarity): High-to-low transition only. If CPOL = 0 (noninverted polarity): Low-to-high transition only.
00	Trigger/event/interrupt generation is disabled

Bit 4 – CREF DAC Reference Source Select bit

Value	Description
1	Noninverting input connects to the internal CV_{REF} voltage
0	Noninverting input connects to the C1INA pin

Bits 1:0 – CCH[1:0] Comparator Channel Select bits

Value	Description
11	Inverting input of the comparator connects to the internal selectable reference voltage specified by the CVREFM[1:0] bits in the CVRCON register
10	Inverting input of the comparator connects to the C1IND pin
01	Inverting input of the comparator connects to the C1INC pin
00	Inverting input of the comparator connects to the C1INB pin

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22.1.3 Comparator 2 Control Register

Name: CM2CON
Offset: 0x2EC

Legend: HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
	CON	COE	CPOL				CEVT	COUT
Access	R/W	R/W	R/W				R/W	HSC/R
Reset	0	0	0				0	0

Bit	7	6	5	4	3	2	1	0
	EVPOL[1:0]			CREF			CCH[1:0]	
Access	R/W	R/W		R/W			R/W	R/W
Reset	0	0		0			0	0

Bit 15 – CON Comparator Enable bit

Value	Description
1	Comparator is enabled
0	Comparator is disabled

Bit 14 – COE Comparator Output Enable bit

Value	Description
1	Comparator output is present on the C2OUT pin
0	Comparator output is internal only

Bit 13 – CPOL Comparator Output Polarity Select bit

Value	Description
1	Comparator output is inverted
0	Comparator output is not inverted

Bit 9 – CEVT Comparator Event bit

Value	Description
1	Comparator event that is defined by EVPOL[1:0] has occurred; subsequent triggers and interrupts are disabled until the bit is cleared
0	Comparator event has not occurred

Bit 8 – COUT Comparator Output bit
When CPOL = 1:

Value	Description
1	$V_{IN}+ < V_{IN}-$
0	$V_{IN}+ > V_{IN}-$

When CPOL = 0:

Value	Description
1	$V_{IN}+ > V_{IN}-$
0	$V_{IN}+ < V_{IN}-$

Bits 7:6 – EVPOL[1:0] Trigger/Event/Interrupt Polarity Select bits

Value	Description
11	Trigger/event/interrupt is generated on any change of the comparator output (while CEVT = 0)

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Value	Description
10	Trigger/event/interrupt is generated on transition of the comparator output: If CPOL = 1 (inverted polarity): Low-to-high transition only. If CPOL = 0 (noninverted polarity): High-to-low transition only.
01	Trigger/event/interrupt is generated on transition of comparator output: If CPOL = 1 (inverted polarity): High-to-low transition only. If CPOL = 0 (noninverted polarity): Low-to-high transition only.
00	Trigger/event/interrupt generation is disabled

Bit 4 – CREF DAC Reference Source Select bit

Value	Description
1	Noninverting input connects to the internal CV_{REF} voltage
0	Noninverting input connects to the C2INA pin

Bits 1:0 – CCH[1:0] Comparator Channel Select bits

Value	Description
11	Inverting input of the comparator connects to the internal selectable reference voltage specified by the CVREFM[1:0] bits in the CVRCON register
10	Inverting input of the comparator connects to the C2IND pin
01	Inverting input of the comparator connects to the C2INC pin
00	Inverting input of the comparator connects to the C2INB pin

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22.1.4 Comparator 3 Control Register

Name: CM3CON
Offset: 0x2EE

Legend: HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
	CON	COE	CPOL				CEVT	COUT
Access	R/W	R/W	R/W				R/W	HSC/R
Reset	0	0	0				0	0

Bit	7	6	5	4	3	2	1	0
	EVPOL[1:0]			CREF			CCH[1:0]	
Access	R/W	R/W		R/W			R/W	R/W
Reset	0	0		0			0	0

Bit 15 – CON Comparator Enable bit

Value	Description
1	Comparator is enabled
0	Comparator is disabled

Bit 14 – COE Comparator Output Enable bit

Value	Description
1	Comparator output is present on the C3OUT pin
0	Comparator output is internal only

Bit 13 – CPOL Comparator Output Polarity Select bit

Value	Description
1	Comparator output is inverted
0	Comparator output is not inverted

Bit 9 – CEVT Comparator Event bit

Value	Description
1	Comparator event that is defined by EVPOL[1:0] has occurred; subsequent triggers and interrupts are disabled until the bit is cleared
0	Comparator event has not occurred

Bit 8 – COUT Comparator Output bit
When CPOL = 1:

Value	Description
1	$V_{IN}+ < V_{IN}-$
0	$V_{IN}+ > V_{IN}-$

When CPOL = 0:

Value	Description
1	$V_{IN}+ > V_{IN}-$
0	$V_{IN}+ < V_{IN}-$

Bits 7:6 – EVPOL[1:0] Trigger/Event/Interrupt Polarity Select bits

Value	Description
11	Trigger/event/interrupt is generated on any change of the comparator output (while CEVT = 0)

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Value	Description
10	Trigger/event/interrupt is generated on transition of the comparator output: If CPOL = 1 (inverted polarity): Low-to-high transition only. If CPOL = 0 (noninverted polarity): High-to-low transition only.
01	Trigger/event/interrupt is generated on transition of comparator output: If CPOL = 1 (inverted polarity): High-to-low transition only. If CPOL = 0 (noninverted polarity): Low-to-high transition only.
00	Trigger/event/interrupt generation is disabled

Bit 4 – CREF DAC Reference Source Select bit

Value	Description
1	Noninverting input connects to the internal CV_{REF} voltage
0	Noninverting input connects to the C3INA pin

Bits 1:0 – CCH[1:0] Comparator Channel Select bits

Value	Description
11	Inverting input of the comparator connects to the internal selectable reference voltage specified by the CVREFM[1:0] bits in the CVRCON register
10	Inverting input of the comparator connects to the C3IND pin
01	Inverting input of the comparator connects to the C3INC pin
00	Inverting input of the comparator connects to the C3INB pin

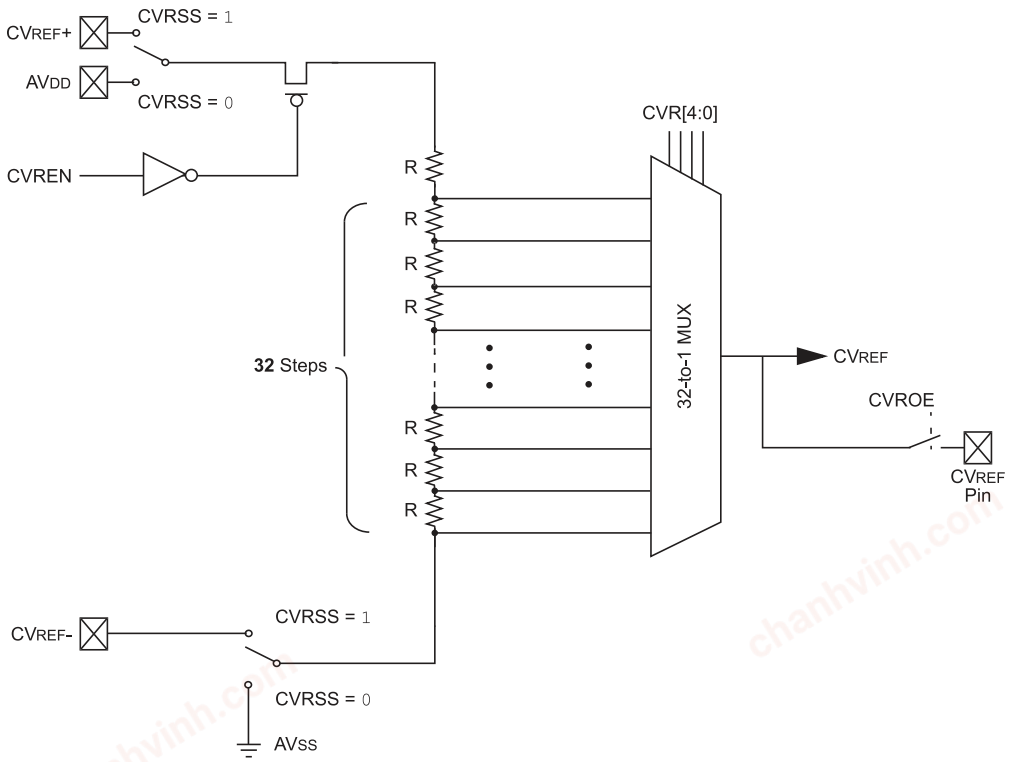
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23. Comparator Voltage Reference

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to **"Dual Comparator Module"** (www.microchip.com/DS39710) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

The comparator voltage reference diagram is shown in Figure 23-1.

Figure 23-1. Comparator Voltage Reference Block Diagram



The voltage reference module is controlled through the CVRCON register. The comparator voltage reference provides two ranges of output voltage, each with 16 distinct levels. The primary difference between the ranges is the size of the steps selected by the CV_{REF} Value Selection bits (CVR[4:0]), with one range offering finer resolution.

The comparator reference supply voltage can come from either AV_{DD} and AV_{SS}, or the external CV_{REF}+ and CV_{REF}- pins. The voltage source is selected by the CVRSS bit (CVRCON[5]).

The settling time of the comparator voltage reference must be considered when changing the CV_{REF} output.

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23.1 Comparator Voltage Reference Register

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x02E7	Reserved									
0x02E8	CVRCON	7:0	CVREN	CVROE	CVRSS			CVR[4:0]		
		15:8						CVREFP	CVREFM[1:0]	

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23.1.1 Comparator Voltage Reference Control Register

Name: CVRCON
Offset: 0x2E8

Bit	15	14	13	12	11	10	9	8
						CVREFP	CVREFM[1:0]	
Access						R/W	R/W	R/W
Reset						0	0	0

Bit	7	6	5	4	3	2	1	0
	CVREN	CVROE	CVRSS	CVR[4:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 10 – CVREFP Comparator Voltage Reference Select bit (valid only when CREF is '1')

Value	Description
1	$CV_{REF}+$ is used as a reference voltage to the comparators
0	The CVR[4:0] bits (5-bit DAC) within this module provide the reference voltage to the comparators

Bits 9:8 – CVREFM[1:0] Comparator Band Gap Reference Source Select bits(valid only when CCH[1:0] = 11)

Value	Description
11	$CV_{REF}+$ is provided as an input to the comparators
10	Reserved
01	Reserved
00	Band gap voltage is provided as an input to the comparators

Bit 7 – CVREN Comparator Voltage Reference Enable bit

Value	Description
1	CV_{REF} circuit is powered on
0	CV_{REF} circuit is powered down

Bit 6 – CVROE Comparator V_{REF} Output Enable bit

Value	Description
1	CV_{REF} voltage level is output on the CV_{REF} pin
0	CV_{REF} voltage level is disconnected from the CV_{REF} pin

Bit 5 – CVRSS Comparator V_{REF} Source Selection bit

Value	Description
1	Comparator reference source, $CV_{RSRC} = CV_{REF}+ - CV_{REF}-$
0	Comparator reference source, $CV_{RSRC} = AV_{DD} - AV_{SS}$

Bits 4:0 – CVR[4:0] Comparator V_{REF} Value Selection bits ($0 \le CVR[4:0] \le 31$)
When CVRSS = 1:
$CV_{REF} = (CV_{REF}-) + (CVR[4:0]/32) \times (CV_{REF}+ - CV_{REF}-)$
When CVRSS = 0:
$CV_{REF} = (AV_{SS}) + (CVR[4:0]/32) \times (AV_{DD} - AV_{SS})$

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24. High/Low-Voltage Detect (HLVD)

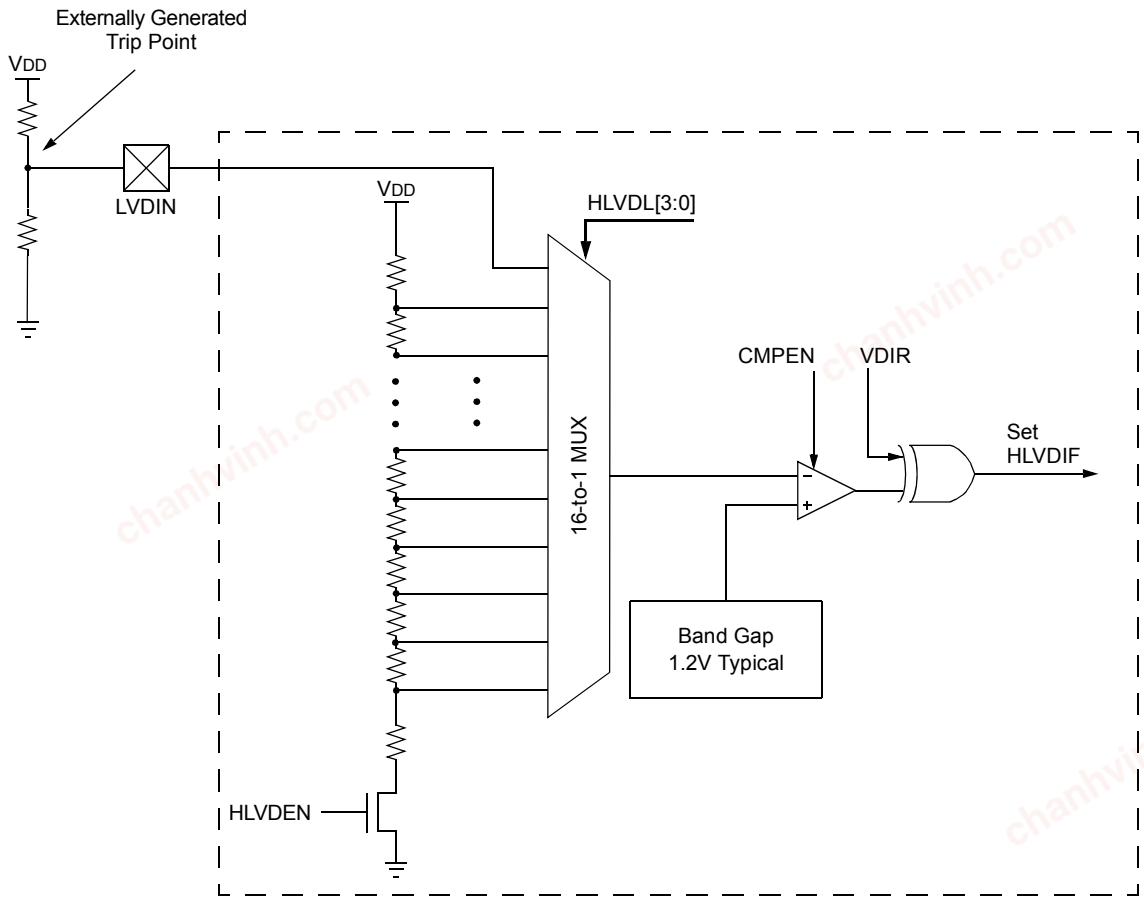
Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the High/Low-Voltage Detect, refer to **"High-Level Integration with Programmable High/Low-Voltage Detect (HLVD)"** (www.microchip.com/DS39725) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

The High/Low-Voltage Detect (HLVD) module is a programmable circuit that allows the user to specify both the device voltage trip point and the direction of change. The module block diagram is shown in Figure 24-1.

An interrupt flag is set if the device experiences an excursion past the trip point in the direction of change. If the interrupt is enabled, the program execution will branch to the interrupt vector address and the software can then respond to the interrupt. The HLVDIF flag may be set during a POR or BOR event. The firmware should clear the flag before the application uses it for the first time, even if the interrupt was disabled.

The HLVDCON register completely controls the operation of the HLVD module. This allows the circuitry to be "turned off" by the user under software control, which minimizes the current consumption for the device. To enable the High/Low-Voltage Detect, the HLVDEN (HLVDCON[15]) and CMPEN (HLVDCON[7]) bits must be set.

Figure 24-1. High/Low-Voltage Detect (HLVD) Module Block Diagram



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24.1 High/Low-Voltage Detect (HLVD) Register

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x0113	Reserved									
0x0114	HLVDCON	7:0	CMPEN				HLVDL[3:0]			
		15:8	HLVDEN		LSIDL		VDIR	BGVST	IRVST	HLVDEVT

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24.1.1 High/Low-Voltage Detect Control Register

Name: HLVDCON
Offset: 0x114

Notes:

1. For the actual trip point, see 30. Electrical Characteristics.
2. The HLVDIF flag cannot be cleared by software unless HLVDEVT = 0. The voltage must be monitored so that the HLVD condition (as set by VDIR and HLVDL[3:0]) is not asserted.

Bit	15	14	13	12	11	10	9	8
	HLVDEN		LSIDL		VDIR	BGVST	IRVST	HLVDEVT
Access	R/W		R/W		R/W	R/W	R/W	R/W
Reset	0		0		0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CMPEN				HLVDL[3:0]			
Access	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

Bit 15 – HLVDEN High/Low-Voltage Detect Power Enable bit

Value	Description
1	HLVD is enabled
0	HLVD is disabled

Bit 13 – LSIDL HLVD Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode
0	Continues module operation in Idle mode

Bit 11 – VDIR Voltage Change Direction Select bit

Value	Description
1	Event occurs when voltage equals or exceeds the trip point (HLVDL[3:0])
0	Event occurs when voltage equals or falls below the trip point (HLVDL[3:0])

Bit 10 – BGVST Band Gap Voltage Stable Flag bit

Value	Description
1	Indicates that the band gap voltage is stable
0	Indicates that the band gap voltage is unstable

Bit 9 – IRVST Internal Reference Voltage Stable Flag bit

Value	Description
1	Internal reference voltage is stable; the High-Voltage Detect logic generates the interrupt flag at the specified voltage range
0	Internal reference voltage is unstable; the High-Voltage Detect logic will not generate the interrupt flag at the specified voltage range and the HLVD interrupt should not be enabled

Bit 8 – HLVDEVT High or Low-Voltage Event Status bit(2)

Value	Description
1	HLVD event is true during current instruction cycle
0	HLVD event is not true during current instruction cycle

Bit 7 – CMPEN High/Low-Voltage Detect Comparator Enable bit

Value	Description
1	HLVD comparator is enabled
0	HLVD comparator is disabled

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Bits 3:0 – HLVDL[3:0] High/Low-Voltage Detection Limit bits(1)

Value	Description
15	Voltage on external LVDIN pin is compared with band gap (1.2V)
14	2.1V
13	2.2V
12	2.3V
11	2.4V
10	2.5V
9	2.6V
8	2.8V
7	2.9V
6	3.1V
5	3.4V
4-0	Reserved

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25. Deadman Timer (DMT)

Note: This data sheet summarizes the features of the PIC24FJ64GP205/GU205 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Deadman Timer (DMT)"** (www.microchip.com/DS70005155) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

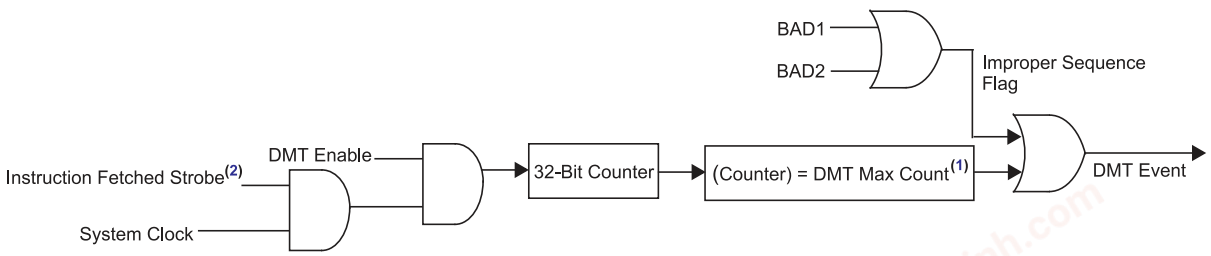
The primary function of the Deadman Timer (DMT) is to interrupt the processor in the event of a software malfunction. The DMT, which works on the system clock, is a free-running instruction fetch timer, which is clocked whenever an instruction fetch occurs, until a count match occurs. Instructions are not fetched when the processor is in Sleep mode.

DMT can be enabled in the Configuration fuse or by software in the DMTCON register by setting the ON bit. The DMT consists of a 32-bit counter with a time-out count match value, as specified by the two 16-bit Configuration Fuse registers: FDMTCNTL and FDMTCNTH.

A DMT is typically used in mission-critical and safety-critical applications, where any single failure of software functionality and sequencing must be detected.

Figure 25-1 shows a block diagram of the Deadman Timer module.

Figure 25-1. Deadman Timer Block Diagram



Notes:

1. DMT Max Count is controlled by the initial value of the FDMTCNTL and FDMTCNTH Configuration registers.
2. DMT window interval is controlled by the value of the FDMTIVTL and FDMTIVTH Configuration registers.

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25.1 Deadman Timer (DMT) Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x5B	Reserved									
0x5C	DMTCON	7:0								
		15:8	ON							
0x5E ... 0x5F	Reserved									
0x60	DMTPRECLR	7:0								
		15:8	STEP1[7:0]							
0x62 ... 0x63	Reserved									
0x64	DMTCLR	7:0	STEP2[7:0]							
		15:8								
0x66 ... 0x67	Reserved									
0x68	DMTSTAT	7:0	BAD1	BAD2	DMTEVENT					WINOPN
		15:8								
0x6A ... 0x6B	Reserved									
0x6C	DMTCNTL	7:0	COUNTER[7:0]							
		15:8	COUNTER[15:8]							
0x6E	DMTCNTH	7:0	COUNTER[23:16]							
		15:8	COUNTER[31:24]							
0x70	DMTHOLDREG(1)	7:0	UPRCNT[7:0]							
		15:8	UPRCNT[15:8]							
0x72 ... 0x73	Reserved									
0x74	DMTPSCNTL	7:0	PSCNT[7:0]							
		15:8	PSCNT[15:8]							
0x76	DMTPSCNTH	7:0	PSCNT[23:16]							
		15:8	PSCNT[31:24]							
0x78	DMTPSINTVL	7:0	PSINTV[7:0]							
		15:8	PSINTV[15:8]							
0x7A	DMTPSINTVH	7:0	PSINTV[23:16]							
		15:8	PSINTV[31:24]							

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25.1.1 Deadman Timer Control Register

Name: DMTCON
Offset: 0x5C

Note:

1. This bit has control only when DMTDIS = 0 in the FDMT Configuration Word.

Bit	15	14	13	12	11	10	9	8
	ON							
Access	R/W							
Reset	0							

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 15 – ON DMT Module Enable bit(1)

Value	Description
1	Deadman Timer module is enabled
0	Deadman Timer module is not enabled

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25.1.2 Deadman Timer Preclear Register

Name: DMTPRECLR
Offset: 0x60

Bit	15	14	13	12	11	10	9	8
	STEP1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 15:8 – STEP1[7:0] DMT Preclear Enable bits
These bits must be set to 40h to enable the Deadman Timer prescaler. All other values (improper sequence) generate the DMT event and set the BAD1 flag. These bits are cleared when a DMT Reset event occurs. STEP1[7:0] bits are also cleared if the STEP2[7:0] bits are loaded with the correct value in the correct sequence.

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25.1.3 Deadman Timer Clear Register

Name: DMTCLR
Offset: 0x64

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	STEP2[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – STEP2[7:0] DMT Clear Enable bits
If the correct (40h) value was loaded in the STEP1[7:0] bits, the 04h value written into the STEP2[7:0] bits resets the Deadman Timer and clears the STEP1[7:0] bits. All other values (improper sequence) generate the DMT event and set the BAD2 flag.

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25.1.4 Deadman Timer Status Register

Name: DMTSTAT
Offset: 0x68

Legend: HC = Hardware Clearable bit

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	BAD1	BAD2	DMTEVENT					WINOPN
Access	HC/R	HC/R	HC/R					R
Reset	0	0	0					0

Bit 7 – BAD1 Deadman Timer Bad STEP1[7:0] Value Detect bit

Value	Description
1	Incorrect STEP1[7:0] value was detected
0	Incorrect STEP1[7:0] value was not detected

Bit 6 – BAD2 Deadman Timer Bad STEP2[7:0] Value Detect bit

Value	Description
1	Incorrect STEP2[7:0] value was detected
0	Incorrect STEP2[7:0] value was not detected

Bit 5 – DMTEVENT Deadman Timer Event bit

Value	Description
1	Deadman Timer event was detected (counter expired or improper Reset sequence)
0	Deadman Timer event was not detected

Bit 0 – WINOPN Deadman Timer Clear Window bit

Value	Description
1	Deadman Timer clear window is open
0	Deadman Timer clear window is not open

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25.1.5 Deadman Timer Count Register Low

Name: DMTCNTL
Offset: 0x6C

Bit	15	14	13	12	11	10	9	8
	COUNTER[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	COUNTER[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – COUNTER[15:0] Read Current Contents of Lower DMT Counter bits

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25.1.6 Deadman Timer Count Register High

Name: DMTCNTH
Offset: 0x6E

Bit	15	14	13	12	11	10	9	8
	COUNTER[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	COUNTER[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – COUNTER[31:24] Read Current Contents of Higher DMT Counter bits

Bits 7:0 – COUNTER[23:16] Read Current Contents of Higher DMT Counter bits

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25.1.7 DMT Post-Configure Count Status Register Low

Name: DMTPSCNTL
Offset: 0x74

Legend: y = Value from Configuration bit on POR

Bit	15	14	13	12	11	10	9	8
	PSCNT[15:8]							
Access	R-y	R-y	R-y	R-y	R-y	R-y	R-y	R-y
Reset								

Bit	7	6	5	4	3	2	1	0
	PSCNT[7:0]							
Access	R-y	R-y	R-y	R-y	R-y	R-y	R-y	R-y
Reset								

Bits 15:0 – PSCNT[15:0] Lower DMT Instruction Count Value Configuration Status bits
This is always the value of the FDMTCNTL Configuration register.

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25.1.8 DMT Post-Configure Count Status Register High

Name: DMTPSCNTH
Offset: 0x76

Legend: y = Value from Configuration bit on POR

Bit	15	14	13	12	11	10	9	8
	PSCNT[31:24]							
Access	R-y	R-y	R-y	R-y	R-y	R-y	R-y	R-y
Reset								

Bit	7	6	5	4	3	2	1	0
	PSCNT[23:16]							
Access	R-y	R-y	R-y	R-y	R-y	R-y	R-y	R-y
Reset								

Bits 15:8 – PSCNT[31:24] Higher DMT Instruction Count Value Configuration Status bits
This is always the value of the FDMTCNTH Configuration register.

Bits 7:0 – PSCNT[23:16] Higher DMT Instruction Count Value Configuration Status bits
This is always the value of the FDMTCNTH Configuration register.

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25.1.9 DMT Post-Configure Interval Status Register Low

Name: DMTPSINTVL
Offset: 0x78

Legend: y = Value from Configuration bit on POR

Bit	15	14	13	12	11	10	9	8
	PSINTV[15:8]							
Access	R-y	R-y	R-y	R-y	R-y	R-y	R-y	R-y
Reset								

Bit	7	6	5	4	3	2	1	0
	PSINTV[7:0]							
Access	R-y	R-y	R-y	R-y	R-y	R-y	R-y	R-y
Reset								

Bits 15:0 – PSINTV[15:0] Lower DMT Window Interval Configuration Status bits
This is always the value of the FDMTIVTL Configuration register.

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25.1.10 DMT Post-Configure Interval Status Register High

Name: DMTPSINTVH
Offset: 0x7A

Legend: y = Value from Configuration bit on POR

Bit	15	14	13	12	11	10	9	8
	PSINTV[31:24]							
Access	R-y	R-y	R-y	R-y	R-y	R-y	R-y	R-y
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSINTV[23:16]							
Access	R-y	R-y	R-y	R-y	R-y	R-y	R-y	R-y
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – PSINTV[31:24] Higher DMT Window Interval Configuration Status bits
This is always the value of the FDMTIVTH Configuration register.

Bits 7:0 – PSINTV[23:16] Higher DMT Window Interval Configuration Status bits
This is always the value of the FDMTIVTH Configuration register.

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25.1.11 DMT Hold Register

Name: DMTHOLDREG(1)
Offset: 0x70

Note:

1. The DMTHOLDREG register is initialized to '0' on Reset, and is only loaded when the DMTCNTL and DMTCNTH registers are read.

Bit	15	14	13	12	11	10	9	8
	UPRCNT[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	UPRCNT[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – UPRCNT[15:0] DMTCNTH Register Value When DMTCNTL or DMTCNTH were Last Read bits

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26. USB with On-The-Go (USB OTG) Support

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to **"USB On-The-Go (OTG)"** (www.microchip.com/DS39721) in the *"dsPIC33/PIC24 Family Reference Manual"*. The information in this data sheet supersedes the information in the FRM.

PIC24FJ64GP205/GU205 family devices contain a full-speed and low-speed compatible, On-The-Go (OTG) USB Serial Interface Engine (SIE). The OTG capability allows the device to act as either a USB peripheral device or as a USB embedded host with limited host capabilities. The OTG capability allows the device to dynamically switch from device to host operation using OTG's Host Negotiation Protocol (HNP).

For more details on OTG operation, refer to the *"On-The-Go Supplement"* to the *"USB 2.0 Specification"* published by the USB-IF. For more details on USB operation, refer to the *"Universal Serial Bus Specification, v2.0"*.

The USB OTG module offers these features:

- USB Functionality in Device and Host modes, and OTG Capabilities for Application-Controlled mode Switching
- Software-Selectable module Speeds of Full Speed (12 Mbps) or Low Speed (1.5 Mbps available in Host mode only)
- Support for All Four USB Transfer Types: Control, Interrupt, Bulk and Isochronous
- 16 Bidirectional Endpoints for a Total of 32 Unique Endpoints
- DMA Interface for Data RAM Access
- Queues Up to 16 Unique Endpoint Transfers without Servicing
- Integrated, On-Chip USB Transceiver with Support for Off-Chip Transceivers via a Digital Interface
- Integrated V_{BUS} Generation with On-Chip Comparators and Boost Generation, and Support of External V_{BUS} Comparators and Regulators through a Digital Interface
- Configurations for On-Chip Bus Pull-up and Pull-Down Resistors

A simplified block diagram of the USB OTG module is shown in Figure 26-1.

The USB OTG module can function as a USB peripheral device or as a USB host, and may dynamically switch between Device and Host modes under software control. In either mode, the same data paths and Buffer Descriptors (BDs) are used for the transmission and reception of data.

In discussing USB operation, this section will use a controller-centric nomenclature for describing the direction of the data transfer between the microcontroller and the USB. RX (Receive) will be used to describe transfers that move data from the USB to the microcontroller and TX (Transmit) will be used to describe transfers that move data from the microcontroller to the USB. Table 26-1 shows the relationship between data direction in this nomenclature and the USB tokens exchanged.

Table 26-1. Controller-Centric Data Direction for USB Host or Target

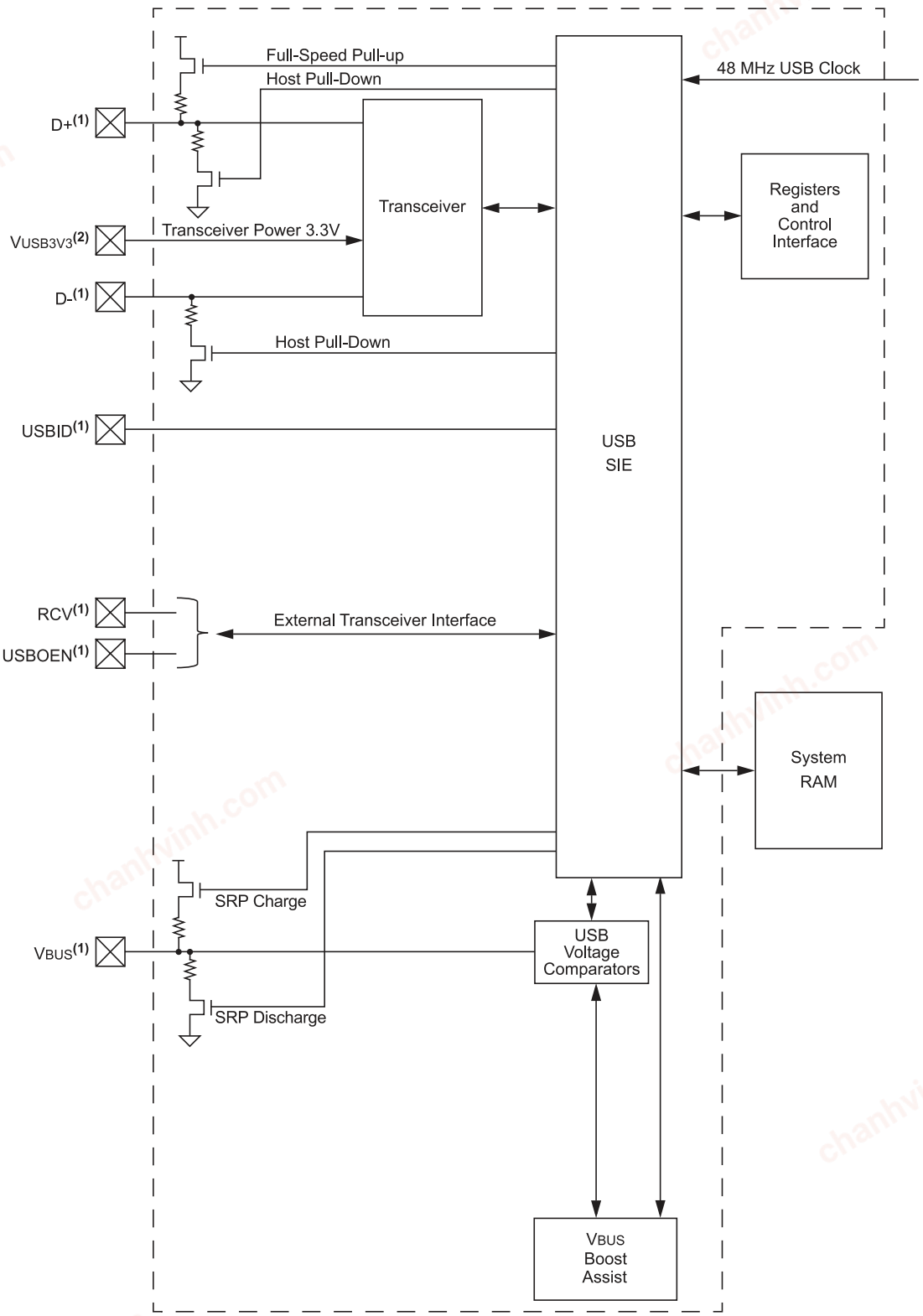
USB Mode	Direction	
	RX	TX
Device	OUT or SETUP	IN
Host	IN	OUT or SETUP

This chapter presents the most basic operations needed to implement USB OTG functionality in an application. A complete and detailed discussion of the USB protocol and its OTG supplement are beyond the scope of this data sheet. It is assumed that the user already has a basic understanding of USB architecture and the latest version of the protocol.

Not all steps for proper USB operation (such as device enumeration) are presented here. It is recommended that application developers use an appropriate device driver to implement all of the necessary features. Microchip provides a number of application-specific resources, such as USB firmware and driver support. Refer to www.microchip.com/usb for the latest firmware and driver support.

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Figure 26-1. USB OTG Module Block Diagram



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Notes:

1. Pins are multiplexed with digital I/Os and other device features.
2. Connecting V_{BUS3V3} to V_{DD} is highly recommended, as floating this input can cause increased I_{PD} currents. The pin should be tied to V_{DD} when the USB functions are not used.

26.1 Hardware Configuration

26.1.1 Device Mode

26.1.1.1 D+ Pull-up Resistor

PIC24FJ64GP205/GU205 family devices have a built-in 1.5 kΩ resistor on the D+ line that is available when the microcontroller is operating in Device mode. This is used to signal an external host that the device is operating in Full-Speed Device mode. It is engaged by setting the USBEN bit (U1CON[0]) and powering up the USB module (USBPWR = 1). If the OTGEN bit (U1OTGCON[2]) is set, then the D+ pull-up is enabled through the DPPULUP bit (U1OTGCON[7]).

26.1.1.2 The V_{BUS} Pin

In order to meet the *"USB 2.0 Specification"* requirement, relating to the back drive voltage on the D+/D- pins, the USB module incorporates V_{BUS}-level sensing comparators. When the comparators detect the V_{BUS} level below the V_{A_SESS}_V_{LD} level, the hardware will automatically disable the D+ pull-up resistor described in 26.1.1.1 D+ Pull-up Resistor. This allows the device to automatically meet the back drive requirement for D+ and D-, even if the application firmware does not explicitly monitor the V_{BUS} level. Therefore, the V_{BUS} microcontroller pin should not be left floating in USB Device mode application designs and should normally be connected to the V_{BUS} pin on the USB connector/cable (either directly or through a small resistance ≤ 100 ohms).

26.1.1.3 Power Modes

Many USB applications will likely have several different sets of power requirements and configuration. The most common power modes encountered are:

- Bus Power Only mode
- Self-Power Only mode
- Suspend mode
- Dual Power with Self-Power Dominance mode

Bus Power Only mode (Figure 26-2) is effectively the simplest method. All power for the application is drawn from the USB.

To meet the inrush current requirements of the *"USB 2.0 Specification"*, the total effective capacitance, appearing across V_{BUS} and ground, must be no more than 10 µF.

In the USB Suspend mode, devices must consume no more than 2.5 mA from the 5V V_{BUS} line of the USB cable. During the USB Suspend mode, the D+ or D- pull-up resistor must remain active, which will consume some of the allowed suspend current.

In Self-Power Only mode (Figure 26-3), the USB application provides its own power, with very little power being pulled from the USB. Note that an attach indication is added to indicate when the USB has been connected and the host is actively powering V_{BUS}.

To meet compliance specifications, the USB module (and the D+ or D- pull-up resistor) should not be enabled until the host actively drives V_{BUS} high. One of the 5.5V tolerant I/O pins may be used for this purpose.

The application should never source any current onto the 5V V_{BUS} pin of the USB cable when the USB module is operated in USB Device mode.

The Dual Power with Self-Power Dominance mode (Figure 26-4) allows the application to use internal power primarily, but switch to power from the USB when no internal power is available. Dual power devices must also meet all of the special requirements for inrush current and Suspend mode current previously described, and must not enable the USB module until V_{BUS} is driven high.

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Figure 26-2. Bus-Powered Interface Example

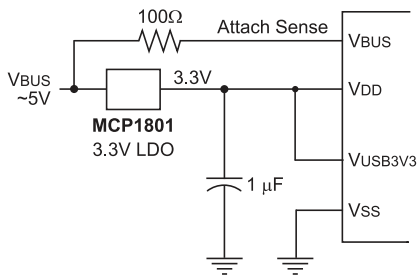


Figure 26-3. Self-Power Only

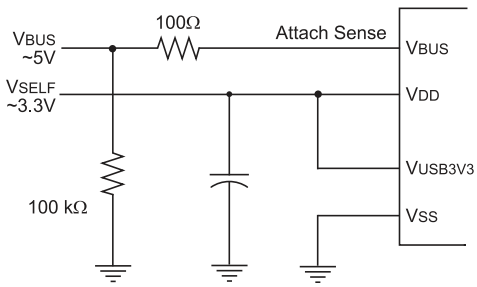
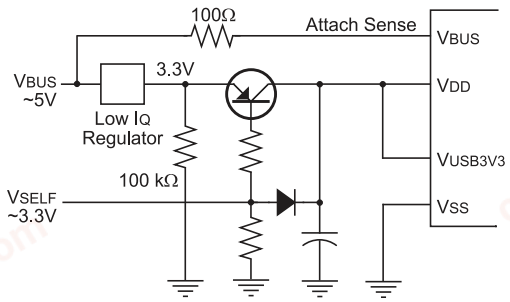


Figure 26-4. Dual Power Example



26.1.2 Host and OTG Modes

26.1.2.1 D+ and D- Pull-Down Resistors

PIC24FJ64GP205/GU205 family devices have built-in 15 kΩ pull-down resistors on the D+ and D- lines. These resistors are used in tandem to signal to the bus that the microcontroller is operating in Host mode. They are engaged by setting the HOSTEN bit (U1CON[3]). If the OTGEN bit (U1OTGCON[2]) is set, then these pull-downs are enabled by setting the DPPULDWN and DMPULDWN bits (U1OTGCON[5:4]).

26.1.2.2 Power Configurations

In Host mode, as well as Host mode in On-The-Go operation, the *"USB 2.0 Specification"* requires that the host application should supply power on V_{BUS}. Since the microcontroller is running below V_{BUS}, and is not able to source sufficient current, a separate power supply must be provided.

When the application is always operating in Host mode, a simple circuit can be used to supply V_{BUS} and regulate current on the bus (Figure 26-5). For OTG operation, it is necessary to be able to turn V_{BUS} on or off as needed, as the microcontroller switches between Device and Host modes. A typical example using an external charge pump is shown in Figure 26-6.

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Figure 26-5. Host Interface Example

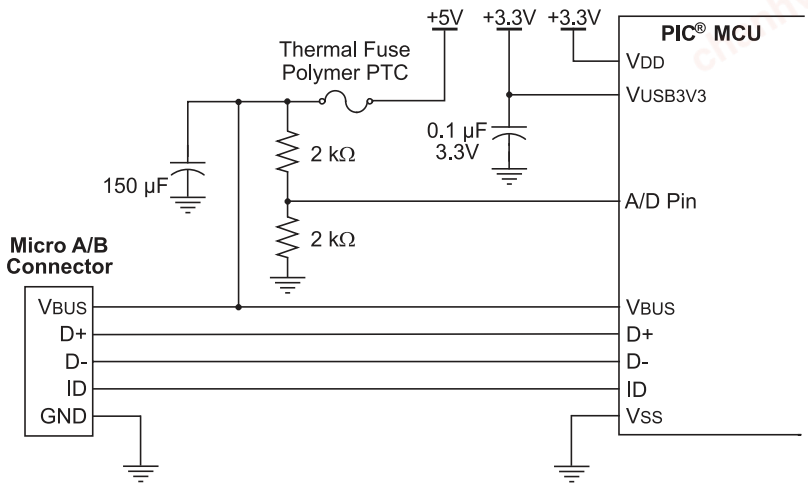
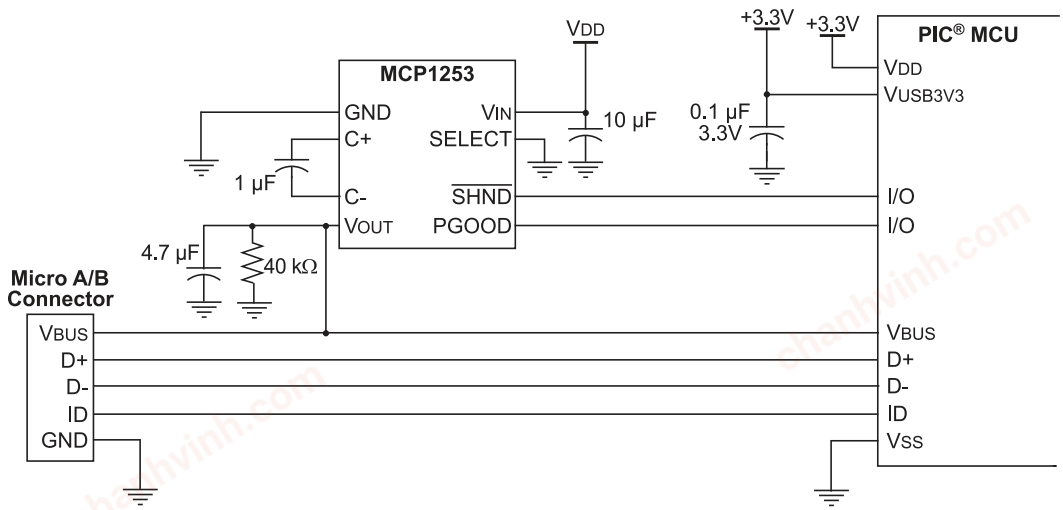


Figure 26-6. OTG Interface Example



26.1.3 Calculating Transceiver Power Requirements

The USB transceiver consumes a variable amount of current depending on the characteristic impedance of the USB cable, the length of the cable, the V_{USB} supply voltage and the actual data patterns moving across the USB cable. Longer cables have larger capacitances and consume more total energy when switching output states. The total transceiver current consumption will be application-specific. Equation 26-1 can help estimate how much current actually may be required in full-speed applications.

Refer to **"USB On-The-Go (OTG)"** (www.microchip.com/DS39721) in the *"dsPIC33/PIC24 Family Reference Manual"* for a complete discussion on transceiver power consumption.

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Equation 26-1. Estimating USB Transceiver Current Consumption

$$IXCVR = \frac{40\ mA \bullet V_{USB} \bullet P_{ZERO} \bullet P_{IN} \bullet L_{CABLE}}{3.3V \bullet 5m} + I_{PULLUP}$$

Legend: V_{USB} – Voltage applied to the V_{USB3V3} pin in volts (3.0V to 3.6V).

P_{ZERO} – Percentage (in decimal) of the IN traffic bits sent by the PIC® microcontroller that are a value of '0'.

P_{IN} – Percentage (in decimal) of total bus bandwidth that is used for IN traffic.

L_{CABLE} – Length (in meters) of the USB cable. The *"USB 2.0 Specification"* requires that full-speed applications use cables no longer than 5m.

I_{PULLUP} – Current which the nominal, 1.5 kΩ pull-up resistor (when enabled) must supply to the USB cable.

26.2 USB Buffer Descriptors and the BDT

Endpoint buffer control is handled through a structure called the Buffer Descriptor Table (BDT). This provides a flexible method for users to construct and control endpoint buffers of various lengths and configurations.

The BDT can be located in any available 512-byte, aligned block of data RAM. The BDT Pointer (U1BDTP1) contains the upper address byte of the BDT and sets the location of the BDT in RAM. The user must set this pointer to indicate the table's location.

The BDT is composed of Buffer Descriptors (BDs), which are used to define and control the actual buffers in the USB RAM space. Each BD consists of two 16-bit, "soft" (non-fixed address) registers, BDnSTAT and BDnADR, where n represents one of the 64 possible BDs (range of 0 to 63). BDnSTAT is the status register for BDn, while BDnADR specifies the starting address for the buffer associated with BDn.

Note: Since BDnADR is a 16-bit register, only the first 64 Kbytes of RAM can be accessed by the USB module.

Depending on the endpoint buffering configuration used, there are up to 64 sets of Buffer Descriptors, for a total of 256 bytes. At a minimum, the BDT must be at least eight bytes long. This is because the *"USB 2.0 Specification"* mandates that every device must have Endpoint 0 with both input and output for initial setup.

Endpoint mapping in the BDT is dependent on three variables:

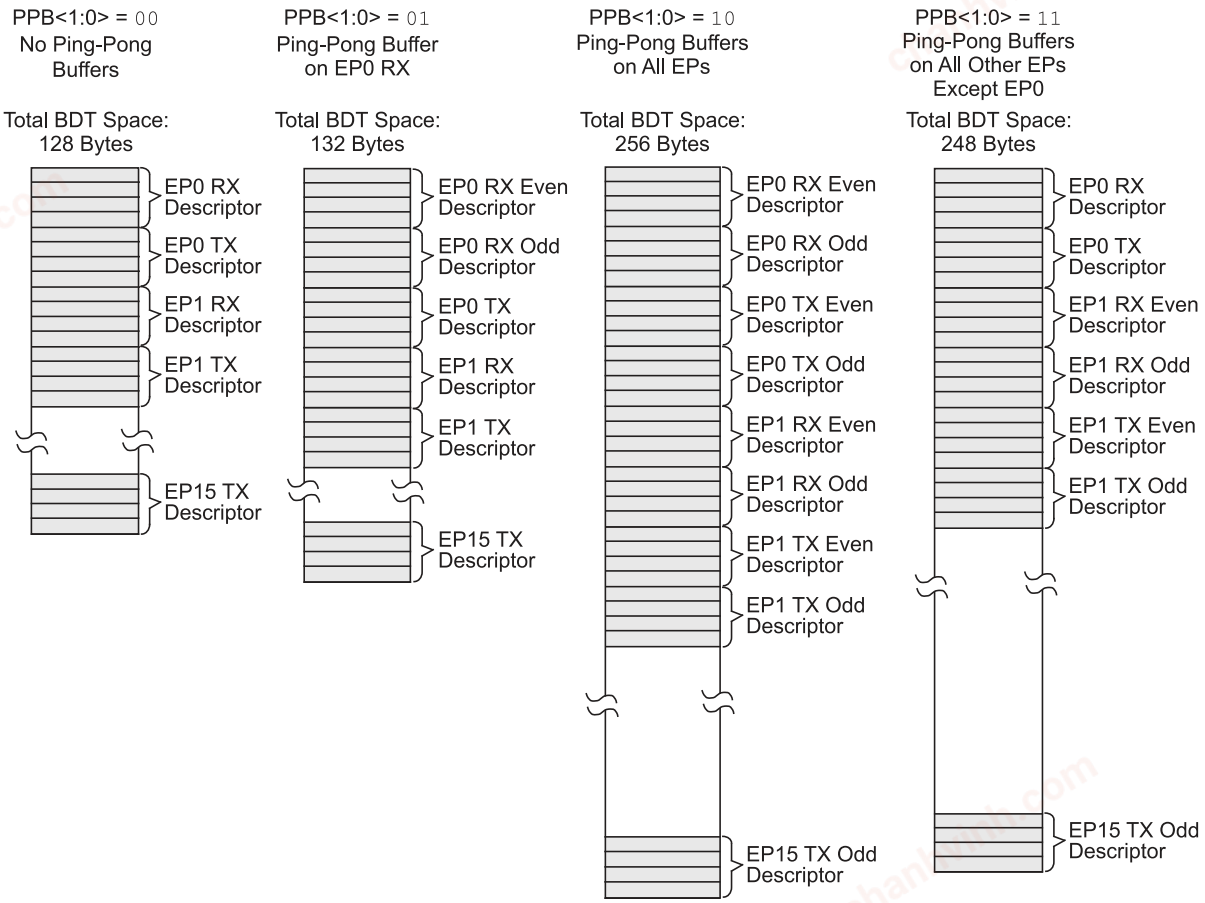
- Endpoint number (0 to 15)
- Endpoint direction (RX or TX)
- Ping-pong settings (U1CNFG1[1:0])

Figure 26-7 illustrates how these variables are used to map endpoints in the BDT.

In Host mode, only Endpoint 0 Buffer Descriptors are used. All transfers utilize the Endpoint 0 Buffer Descriptor and Endpoint Control register (U1EP0). For received packets, the attached device's source endpoint is indicated by the value of ENDPT[3:0] in the USB Status register (U1STAT[7:4]). For transmitted packets, the attached device's destination endpoint is indicated by the value written to the USB Token register (U1TOK).

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Figure 26-7. BDT Mapping for Endpoint Buffering Modes



Note: Memory area is not shown to scale.

BDs have a fixed relationship to a particular endpoint, depending on the buffering configuration. Table 26-2 provides the mapping of BDs to endpoints. This relationship also means that gaps may occur in the BDT if endpoints are not enabled contiguously. This, theoretically, means that the BDs for disabled endpoints could be used as buffer space. In practice, users should avoid using such spaces in the BDT unless a method of validating BD addresses is implemented.

Table 26-2. Assignment of Buffer Descriptors for the Different Buffering Modes

Endpoint	BDs Assigned to Endpoint							
	Mode 0 (No Ping-Pong)		Mode 1 (Ping-Pong on EP0 RX)		Mode 2 (Ping-Pong on All EPs)		Mode 3 (Ping-Pong on All Other EPs, Except EP0)	
	RX	TX	RX	TX	RX	TX	RX	TX
0	0	1	0 (E), 1 (O)	2	0 (E), 1 (O)	2 (E), 3 (O)	0	1
1	2	3	3	4	4 (E), 5 (O)	6 (E), 7 (O)	2 (E), 3 (O)	4 (E), 5 (O)
2	4	5	5	6	8 (E), 9 (O)	10 (E), 11 (O)	6 (E), 7 (O)	8 (E), 9 (O)
3	6	7	7	8	12 (E), 13 (O)	14 (E), 15 (O)	10 (E), 11 (O)	12 (E), 13 (O)
4	8	9	9	10	16 (E), 17 (O)	18 (E), 19 (O)	14 (E), 15 (O)	16 (E), 17 (O)
5	10	11	11	12	20 (E), 21 (O)	22 (E), 23 (O)	18 (E), 19 (O)	20 (E), 21 (O)

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Endpoint	BDs Assigned to Endpoint							
	Mode 0 (No Ping-Pong)		Mode 1 (Ping-Pong on EP0 RX)		Mode 2 (Ping-Pong on All EPs)		Mode 3 (Ping-Pong on All Other EPs, Except EP0)	
	RX	TX	RX	TX	RX	TX	RX	TX
6	12	13	13	14	24 (E), 25 (O)	26 (E), 27 (O)	22 (E), 23 (O)	24 (E), 25 (O)
7	14	15	15	16	28 (E), 29 (O)	30 (E), 31 (O)	26 (E), 27 (O)	28 (E), 29 (O)
8	16	17	17	18	32 (E), 33 (O)	34 (E), 35 (O)	30 (E), 31 (O)	32 (E), 33 (O)
9	18	19	19	20	36 (E), 37 (O)	38 (E), 39 (O)	34 (E), 35 (O)	36 (E), 37 (O)
10	20	21	21	22	40 (E), 41 (O)	42 (E), 43 (O)	38 (E), 39 (O)	40 (E), 41 (O)
11	22	23	23	24	44 (E), 45 (O)	46 (E), 47 (O)	42 (E), 43 (O)	44 (E), 45 (O)
12	24	25	25	26	48 (E), 49 (O)	50 (E), 51 (O)	46 (E), 47 (O)	48 (E), 49 (O)
13	26	27	27	28	52 (E), 53 (O)	54 (E), 55 (O)	50 (E), 51 (O)	52 (E), 53 (O)
14	28	29	29	30	56 (E), 57 (O)	58 (E), 59 (O)	54 (E), 55 (O)	56 (E), 57 (O)
15	30	31	31	32	60 (E), 61 (O)	62 (E), 63 (O)	58 (E), 59 (O)	60 (E), 61 (O)

Legend: (E) = Even transaction buffer, (O) = Odd transaction buffer

26.2.1 Buffer Ownership

Because the buffers and their BDs are shared between the CPU and the USB module, a simple semaphore mechanism is used to distinguish which is allowed to update the BD and associated buffers in memory. This is done by using the UOWN bit as a semaphore to distinguish which is allowed to update the BD and associated buffers in memory. UOWN is the only bit that is shared between the two configurations of BDnSTAT.

When UOWN is clear, the BD entry is “owned” by the microcontroller core. When the UOWN bit is set, the BD entry and the buffer memory are “owned” by the USB peripheral. The core should not modify the BD or its corresponding data buffer during this time. Note that the microcontroller core can still read BDnSTAT while the SIE owns the buffer and vice versa.

The Buffer Descriptors have a different meaning based on the source of the register update. 26.3.1 BDnSTAT and 26.3.2 BDnSTAT show the differences in BDnSTAT depending on its current “ownership”.

When UOWN is set, the user can no longer depend on the values that were written to the BDs. From this point, the USB module updates the BDs as necessary, overwriting the original BD values. The BDnSTAT register is updated by the SIE with the token PID and the transfer count is updated.

26.2.2 DMA Interface

The USB OTG module uses a dedicated DMA to access both the BDT and the endpoint data buffers. Since part of the address space of the DMA is dedicated to the Buffer Descriptors, a portion of the memory connected to the DMA must comprise a contiguous address space, properly mapped for the access by the module.

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26.3 USB On-The-Go Registers

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
00 ... 05FF	Reserved									
0x0600	U1OTGIR(2)	7:0	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF		VBUSVDIF
		15:8								
0x0602	U1OTGIE	7:0	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE		VBUSVDIE
		15:8								
0x0604	U1OTGSTAT	7:0	ID		LSTATE		SESVD	SESEND		VBUSVD
		15:8								
0x0606	U1OTGCON	7:0	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	Reserved	OTGEN	Reserved	VBUSDIS
		15:8								
0x0608	U1PWRC	7:0	UACTPND			USLPGRD			USUSPND	USBPWR
		15:8								
0x060A	U1IR(1)	7:0	STALLIF		RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF
		15:8								
0x060A	U1IR(1)	7:0	STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	DETACHIF
		15:8								
0x060C	U1IE	7:0	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE or DETACHIE
		15:8								
0x060E	U1EIR(1)	7:0	BTSEF		DMAEF	BTOEF	DFN8EF	CRC16EF	CRC5EF or EOFEE	PIDEF
		15:8								
0x0610	U1EIE	7:0	BTSEE		DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE or EOFEE	PIDEE
		15:8								
0x0612	U1STAT	7:0	ENDPT[3:0]				DIR	PPBI		
		15:8								
0x0614	U1CON	7:0		SE0	PKTDIS		HOSTEN	RESUME	PPBRST	USBEN
		15:8								
0x0614	U1CON	7:0	JSTATE	SE0	TOKBUSY	USBRST	HOSTEN	RESUME	PPBRST	SOFEN
		15:8								
0x0616	U1ADDR	7:0	LSPDEN	DEVADDR[6:0]						
		15:8								
0x0618	U1BDTP1	7:0	BDTPTRL[6:0]							
		15:8								
0x061A	U1FRML	7:0	FRM[7:0]							
		15:8								
0x061C	U1FRMH	7:0						FRM[10:8]		
		15:8								
0x061E	U1TOK	7:0	PID[3:0]				EP[3:0]			
		15:8								
0x0620	U1SOF	7:0	CNT[7:0]							
		15:8								
0x0622	U1BDTP2	7:0	BDTPTRH[7:0]							
		15:8								
0x0624	U1BDTP3	7:0	BDTPTRU[7:0]							
		15:8								
0x0626	U1CNFG1	7:0	UTEYE	UOEMON		USBSIDL			PPB[1:0]	
		15:8								
0x0628	U1CNFG2	7:0				PUVBUS	EXTI2CEN			
		15:8								
0x062A	U1EP0	7:0	LSPD	RETRYDIS		EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
0x062C	U1EP1	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								

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.....continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x062E	U1EP2	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
0x0630	U1EP3	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
0x0632	U1EP4	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
0x0634	U1EP5	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
0x0636	U1EP6	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
0x0638	U1EP7	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
0x063A	U1EP8	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
0x063C	U1EP9	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
0x063E	U1EP10	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
0x0640	U1EP11	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
0x0642	U1EP12	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
0x0644	U1EP13	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
0x0646	U1EP14	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
0x0648	U1EP15	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								

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26.3.1 Buffer Descriptor n Status Register Prototype, USB Mode (BD0STAT through BD63STAT)

Name: BDnSTAT
Offset: User Defined

Legend: HSC = Hardware Settable/Clearable bit; x = Bit state is unknown

Bit	15	14	13	12	11	10	9	8
	UOWN	DTS	PID[3:0]				BC[9:8]	
Access	HSC/R/W	HSC/R/W	HSC/R/W	HSC/R/W	HSC/R/W	HSC/R/W	HSC/R/W	HSC/R/W
Reset	x	x	x	x	x	x	x	x

Bit	7	6	5	4	3	2	1	0
	BC[7:0]							
Access	HSC/R/W	HSC/R/W	HSC/R/W	HSC/R/W	HSC/R/W	HSC/R/W	HSC/R/W	HSC/R/W
Reset	x	x	x	x	x	x	x	x

Bit 15 – UOWN USB Own bit

Value	Description
1	The USB module owns the BD and its corresponding buffer; the CPU must not modify the BD or the buffer

Bit 14 – DTS Data Toggle Packet bit

Value	Description
1	Data 1 packet
0	Data 0 packet

Bits 13:10 – PID[3:0] Packet Identifier bits (written by the USB module)
In Device mode:
Represents the PID of the received token during the last transfer.
In Host mode:
Represents the last returned PID or the transfer status indicator.

Bits 9:0 – BC[9:0] Byte Count bits
This represents the number of bytes to be transmitted or the maximum number of bytes to be received during a transfer. Upon completion, the byte count is updated by the USB module with the actual number of bytes transmitted or received.

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26.3.2 Buffer Descriptor n Status Register Prototype, CPU Mode (BD0STAT through BD63STAT)

Name: BDnSTAT
Offset: User Defined

Note:
1. This bit is ignored unless DTSEN = 1.

Legend: HSC = Hardware Settable/Clearable bit; x = Bit state is unknown

Bit	15	14	13	12	11	10	9	8
	UOWN	DTS			DTSEN	BSTALL	BC[9:8]	
Access	HSC/R/W	HSC/R/W			HSC/R/W	HSC/R/W	HSC/R/W	HSC/R/W
Reset	x	x			x	x	x	x

Bit	7	6	5	4	3	2	1	0
	BC[7:0]							
Access	HSC/R/W	HSC/R/W	HSC/R/W	HSC/R/W	HSC/R/W	HSC/R/W	HSC/R/W	HSC/R/W
Reset	x	x	x	x	x	x	x	x

Bit 15 – UOWN USB Own bit

Value	Description
1	The microcontroller core owns the BD and its corresponding buffer; the USB module ignores all other fields in the BD

Bit 14 – DTS Data Toggle Packet bit(1)

Value	Description
1	Data 1 packet
0	Data 0 packet

Bit 11 – DTSEN Data Toggle Synchronization Enable bit

Value	Description
1	Data toggle synchronization is enabled; data packets with incorrect Sync value will be ignored
0	No data toggle synchronization is performed

Bit 10 – BSTALL Buffer Stall Enable bit

Value	Description
1	Buffer STALL is enabled; STALL handshake issued if a token is received that would use the BD in the given location (UOWN bit remains set, BD value is unchanged), corresponding EPSTALL bit will get set on any STALL handshake
0	Buffer STALL is disabled

Bits 9:0 – BC[9:0] Byte Count bits
This represents the number of bytes to be transmitted or the maximum number of bytes to be received during a transfer. Upon completion, the byte count is updated by the USB module with the actual number of bytes transmitted or received.

26.4 USB Interrupts

The USB OTG module has many conditions that can be configured to cause an interrupt. All interrupt sources use the same interrupt vector.

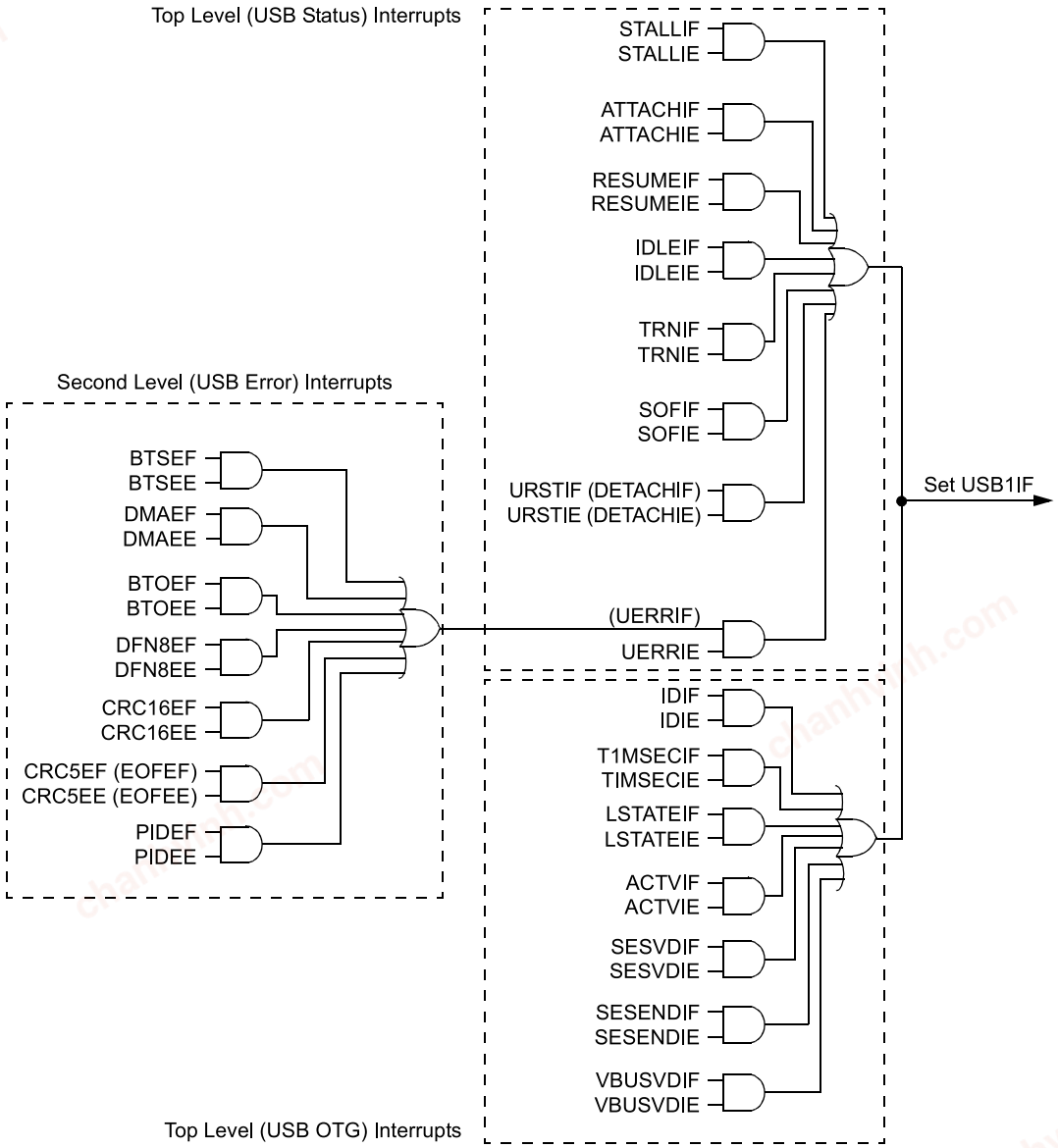
Figure 26-8 shows the interrupt logic for the USB module. There are two layers of interrupt registers in the USB module. The top level consists of overall USB status interrupts; these are enabled and flagged in the U1IE and U1IR registers, respectively. The second level consists of USB error conditions, which are enabled and flagged in the U1EIR and U1EIE registers. An interrupt condition in any of these triggers a USB Error Interrupt Flag (UERRIF) in the

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top level. Unlike the device-level interrupt flags in the IFSx registers, USB interrupt flags in the U1IR registers can only be cleared by writing a '1' to the bit position.

Interrupts may be used to trap routine events in a USB transaction. Figure 26-8 provides some common events within a USB frame and their corresponding interrupts.

Figure 26-8. USB OTG Interrupt Funnel



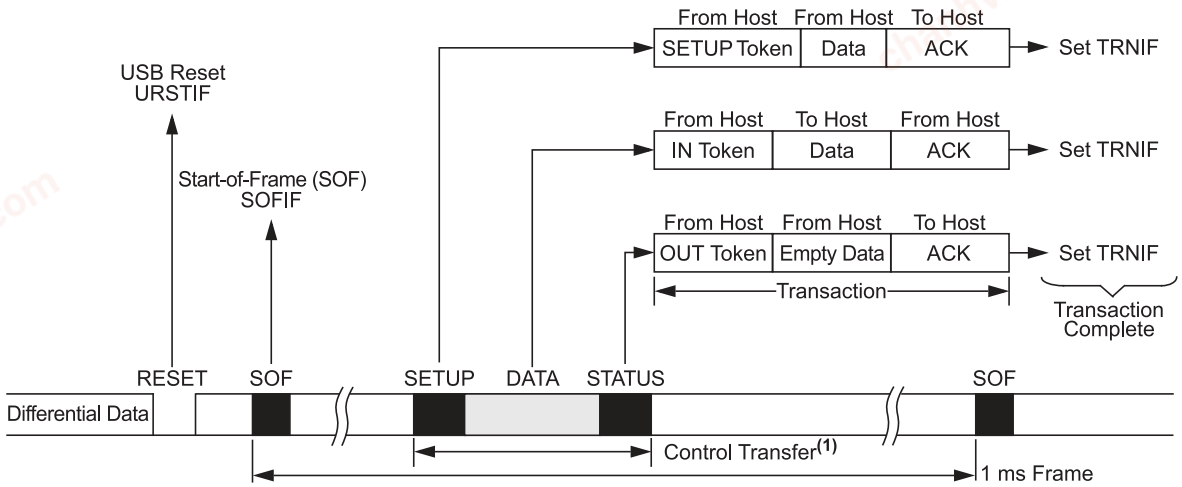
26.4.1 Clearing USB OTG Interrupts

Unlike device-level interrupts, the USB OTG interrupt status flags are not freely writable in software. All USB OTG flag bits are implemented as hardware set only bits. Additionally, these bits can only be cleared in software by writing a '1' to their locations (i.e., performing a MOV type instruction). Writing a '0' to a flag bit (i.e., a BCLR instruction) has no effect.

Note: Throughout this data sheet, a bit that can only be cleared by writing a '1' to its location is referred to as "Write '1' to Clear". In register descriptions; this function is indicated by the descriptor, "K".

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Figure 26-9. Example of a USB Transaction and Interrupt Events



Note:

1. The control transfer shown here is only an example showing events that can occur for every transaction. Typical control transfers will spread across multiple frames.

26.5 Device Mode Operation

The following section describes how to perform a common Device mode task. In Device mode, USB transfers are performed at the transfer level. The USB module automatically performs the status phase of the transfer.

26.5.1 Enabling Device Mode

1. Reset the Ping-Pong Buffer Pointers by setting, then clearing, the Ping-Pong Buffer Reset bit, PPBRST (U1CON[1]).
2. Disable all interrupts (U1IE and U1EIE = 00h).
3. Clear any existing interrupt flags by writing FFh to U1IR and U1EIR.
4. Verify that V_{BUS} is present (non-OTG devices only).
5. Enable the USB module by setting the USBEN bit (U1CON[0]).
6. Set the OTGEN bit (U1OTGCON[2]) to enable OTG operation.
7. Enable the Endpoint 0 buffer to receive the first setup packet by setting the EPRXEN and EPHSHK bits for Endpoint 0 (U1EP0[3,0] = 1).
8. Power up the USB module by setting the USBPWR bit (U1PWRC[0]).
9. Enable the D+ pull-up resistor to signal an attach by setting the DPPULUP bit (U1OTGCON[7]).

26.5.2 Receiving an IN Token in Device Mode

1. Attach to a USB host and enumerate as described in Chapter 9 of the *"USB 2.0 Specification"*.
2. Create a data buffer and populate it with the data to send to the host.
3. In the appropriate (even or odd) TX BD for the desired endpoint:
   - 3.1. Set up the status register (BDnSTAT) with the correct data toggle (DATA0/1) value and the byte count of the data buffer.
   - 3.2. Set up the address register (BDnADR) with the starting address of the data buffer.
   - 3.3. Set the UOWN bit of the status register to '1'.
4. When the USB module receives an IN token, it automatically transmits the data in the buffer. Upon completion, the module updates the status register (BDnSTAT) and sets the Token Processing Complete Interrupt Flag, TRNIF (U1IR[3]).

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26.5.3 Receiving an OUT Token in Device Mode

1. Attach to a USB host and enumerate as described in Chapter 9 of the *"USB 2.0 Specification"*.
2. Create a data buffer with the amount of data you are expecting from the host.
3. In the appropriate (even or odd) TX BD for the desired endpoint:
   3.1. Set up the status register (BDnSTAT) with the correct data toggle (DATA0/1) value and the byte count of the data buffer.
   3.2. Set up the address register (BDnADR) with the starting address of the data buffer.
   3.3. Set the UOWN bit of the status register to '1'.
4. When the USB module receives an OUT token, it automatically receives the data sent by the host to the buffer. Upon completion, the module updates the status register (BDnSTAT) and sets the Token Processing Complete Interrupt Flag, TRNIF (U1IR[3]).

26.6 Host Mode Operation

The following sections describe how to perform common Host mode tasks. In Host mode, USB transfers are invoked explicitly by the host software. The host software is responsible for the Acknowledge portion of the transfer. Also, all transfers are performed using the Endpoint 0 Control register (U1EP0) and Buffer Descriptors.

26.6.1 Enable Host Mode and Discover a Connected Device

1. Enable Host mode by setting the HOSTEN bit (U1CON[3]). This causes the Host mode control bits in other USB OTG registers to become available.
2. Enable the D+ and D- pull-down resistors by setting the DPPULDWN and DMPULDWN bits (U1OTGCON[5:4]). Disable the D+ and D- pull-up resistors by clearing the DPPULUP and DMPULUP bits (U1OTGCON[7:6]).
3. At this point, SOF generation begins with the SOF counter loaded with 12,000. Eliminate noise on the USB by clearing the SOFEN bit (U1CON[0]) to disable Start-of-Frame (SOF) packet generation.
4. Enable the device attached interrupt by setting the ATTACHIE bit (U1IE[6]).
5. Wait for the device attached interrupt (U1IR[6] = 1). This is signaled by the USB device changing the state of D + or D- from '0' to '1' (SE0 to J-state). After it occurs, wait 100 ms for the device power to stabilize.
6. Check the state of the JSTATE and SE0 bits in U1CON. If the JSTATE bit (U1CON[7]) is '0', the connecting device is low speed. If the connecting device is low speed, set the LSPDEN and LSPD bits (U1ADDR[7] and U1EP0[7]) to enable low-speed operation.
7. Reset the USB device by setting the USBRST bit (U1CON[4]) for at least 50 ms, sending Reset signaling on the bus. After 50 ms, terminate the Reset by clearing USBRST.
8. In order to keep the connected device from going into suspend, enable the SOF packet generation by setting the SOFEN bit.
9. Wait 10 ms for the device to recover from Reset.
10. Perform enumeration as described by Chapter 9 of the *"USB 2.0 Specification"*.

26.6.2 Complete a Control Transaction to a Connected Device

1. Follow the procedure described in 26.6.1 Enable Host Mode and Discover a Connected Device to discover a device.
2. Set up the Endpoint Control register for bidirectional control transfers by writing 0Dh to U1EP0 (this sets the EPCONDIS, EPTXEN and EPHSHK bits).
3. Place a copy of the device framework setup command in a memory buffer. See Chapter 9 of the *"USB 2.0 Specification"* for information on the device framework command set.
4. Initialize the Buffer Descriptor (BD) for the current (even or odd) TX EP0 to transfer the eight bytes of command data for a device framework command (i.e., GET DEVICE DESCRIPTOR):
   4.1. Set the BD Data Buffer Address (BD0ADR) to the starting address of the 8-byte memory buffer containing the command.
   4.2. Write 8008h to BD0STAT (this sets the UOWN bit and sets a byte count of eight).

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5. Set the USB device address of the target device in the USB Address register (U1ADDR[6:0]). After a USB bus Reset, the device USB address will be zero. After enumeration, it will be set to another value between 1 and 127.
6. Write D0h to U1TOK; this is a SETUP token to Endpoint 0, the target device's default control pipe. This initiates a SETUP token on the bus, followed by a data packet. The device handshake is returned in the PID field of BD0STAT after the packets are complete. When the USB module updates BD0STAT, a Token Processing Complete Interrupt Flag is asserted (the TRNIF flag is set). This completes the setup phase of the setup transaction, as referenced in Chapter 9 of the *"USB 2.0 Specification"*.
7. To initiate the data phase of the setup transaction (i.e., get the data for the `GET DEVICE DESCRIPTOR` command), set up a buffer in memory to store the received data.
8. Initialize the current (even or odd) RX or TX (RX for IN, TX for OUT) EP0 BD to transfer the data:
   8.1. Write C040h to BD0STAT. This sets the UOWN bit, configures the Data Toggle Packet bit (DTS) to DATA1 and sets the byte count to the length of the data buffer (64 or 40h in this case).
   8.2. Set BD0ADR to the starting address of the data buffer.
9. Write the Token register with the appropriate IN or OUT token to Endpoint 0, the target device's default control pipe (e.g., write 90h to U1TOK for an IN token for a `GET DEVICE DESCRIPTOR` command). This initiates an IN token on the bus, followed by a data packet from the device to the host. When the data packet completes, the BD0STAT is written and a Token Processing Complete Interrupt Flag is asserted (the TRNIF flag is set). For control transfers with a single packet data phase, this completes the data phase of the setup transaction, as referenced in Chapter 9 of the *"USB 2.0 Specification"*. If more data need to be transferred, return to Step 8.
10. To initiate the status phase of the setup transaction, set up a buffer in memory to receive or send the zero length status phase data packet.
11. Initialize the current (even or odd) TX EP0 BD to transfer the status data:
    11.1. Set the BDT buffer address field to the start address of the data buffer.
    11.2. Write 8000h to BD0STAT (set UOWN bit, configure DTS to DATA0 and set byte count to 0).
12. Write the Token register with the appropriate IN or OUT token to Endpoint 0, the target device's default control pipe (e.g., write 01h to U1TOK for an OUT token for a `GET DEVICE DESCRIPTOR` command). This initiates an OUT token on the bus, followed by a zero length data packet from the host to the device. When the data packet completes, the BD is updated with the handshake from the device and a Token Processing Complete Interrupt Flag is asserted (the TRNIF flag is set). This completes the status phase of the setup transaction, as described in Chapter 9 of the *"USB 2.0 Specification"*.

Note: Only one control transaction can be performed per frame.

26.6.3 Send a Full-Speed Bulk Data Transfer to a Target Device

1. Follow the procedure described in 26.6.1 Enable Host Mode and Discover a Connected Device and 26.6.2 Complete a Control Transaction to a Connected Device to discover and configure a device.
2. To enable transmit and receive transfers with handshaking enabled, write 1Dh to U1EP0. If the target device is a low-speed device, also set the LSPD (U1EP0[7]) bit. If you want the hardware to automatically retry indefinitely if the target device asserts a NAK on the transfer, clear the Retry Disable bit, RETRYDIS (U1EP0[6]).
3. Set up the BD for the current (even or odd) TX EP0 to transfer up to 64 bytes.
4. Set the USB device address of the target device in the address register (U1ADDR[6:0]).
5. Write an OUT token to the desired endpoint to U1TOK. This triggers the module's transmit state machines to begin transmitting the token and the data.
6. Wait for the Token Processing Complete Interrupt Flag, TRNIF. This indicates that the BD has been released back to the microprocessor and the transfer has completed. If the Retry Disable bit (RETRYDIS) is set, the handshake (ACK, NAK, STALL or ERROR (0Fh)) is returned in the BD PID field. If a STALL interrupt occurs, the pending packet must be dequeued and the error condition in the target device cleared. If a detach interrupt occurs (SE0 for more than 2.5 µs), then the target has detached (U1IR[0] is set).
7. Once the Token Processing Complete Interrupt Flag occurs (TRNIF is set), the BD can be examined and the next data packet queued by returning to Step 2.

Note: USB speed, transceiver and pull-ups should only be configured during the module setup phase. It is not recommended to change these settings while the module is enabled.

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26.6.4 OTG Operation

26.6.4.1 Session Request Protocol (SRP)

An OTG A-device may decide to power down the V_{BUS} supply when it is not using the USB link through the Session Request Protocol (SRP). SRP can only be initiated at full speed. Software may do this by configuring a GPIO pin to disable an external power transistor, or voltage regulator enable signal, which controls the V_{BUS} supply. When the V_{BUS} supply is powered down, the A-device is said to have ended a USB session.

An OTG A-device or embedded host may repower the V_{BUS} supply at any time (initiate a new session). An OTG B-device may also request that the OTG A-device repower the V_{BUS} supply (initiate a new session). This is accomplished via Session Request Protocol (SRP).

Prior to requesting a new session, the B-device must first check that the previous session has definitely ended. To do this, the B-device must check for two conditions:

- V_{BUS} supply is below the session valid voltage.
- Both D+ and D- have been low for at least 2 ms.

The B-device will be notified of Condition 1 by the SESENDIF (U1OTGIR[2]) interrupt. Software will have to manually check for Condition 2.

Note: When the A-device powers down the V_{BUS} supply, the B-device must disconnect its pull-up resistor from power. If the device is self-powered, it can do this by clearing DPPULUP (U1OTGCON[7]) and DMPULUP (U1OTGCON[6]).

The B-device may aid in achieving Condition 1 by discharging the V_{BUS} supply through a resistor. Software may do this by setting VBUSDIS (U1OTGCON[0]).

After these initial conditions are met, the B-device may begin requesting the new session. The B-device begins by pulsing the D+ data line. Software should do this by setting DPPULUP (U1OTGCON[7]). The data line should be held high for 5 to 10 ms.

The B-device then proceeds by pulsing the V_{BUS} supply. Software should do this by setting PUVBUS (U1CNFG2[4]). When an A-device detects SRP signaling (either via the ATTACHIF (U1IR[6]) interrupt or via the SESVDIF (U1OTGIR[3]) interrupt), the A-device must restore the V_{BUS} supply by properly configuring the general purpose I/O port pin controlling the external power source.

The B-device should not monitor the state of the V_{BUS} supply while performing V_{BUS} supply pulsing. When the B-device does detect that the V_{BUS} supply has been restored (via the SESVDIF (U1OTGIR[3]) interrupt), the B-device must reconnect to the USB link by pulling up D+ or D- (via the DPPULUP or DMPULUP bit).

The A-device must complete the SRP by driving USB Reset signaling.

26.6.4.2 Host Negotiation Protocol (HNP)

In USB OTG applications, a Dual Role Device (DRD) is a device that is capable of being either a host or a peripheral. Any OTG DRD must support Host Negotiation Protocol (HNP).

HNP allows an OTG B-device to temporarily become the USB host. The A-device must first enable the B-device to follow HNP. Refer to the *"On-The-Go Supplement"* to the *"USB 2.0 Specification"* for more information regarding HNP. HNP may only be initiated at full speed.

After being enabled for HNP by the A-device, the B-device requests being the host any time that the USB link is in the suspend state, by simply indicating a disconnect. This can be done in software by clearing DPPULUP and DMPULUP. When the A-device detects the disconnect condition (via the URSTIF (U1IR[0]) interrupt), the A-device may allow the B-device to take over as host. The A-device does this by signaling connect as a full-speed function. Software may accomplish this by setting DPPULUP.

If the A-device responds instead with resume signaling, the A-device remains as host. When the B-device detects the connect condition (via ATTACHIF, U1IR[6]), the B-device becomes host. The B-device drives Reset signaling prior to using the bus.

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When the B-device has finished in its role as host, it stops all bus activity and turns on its D+ pull-up resistor by setting DPPULUP. When the A-device detects a suspend condition (Idle for 3 ms), the A-device turns off its D+ pull-up. The A-device may also power down the V_{BUS} supply to end the session. When the A-device detects the connect condition (via ATTACHIF), the A-device resumes host operation and drives Reset signaling.

26.6.5 USB OTG Module Registers

The USB OTG module registers can be divided into four general categories:

- USB OTG Module Control
- USB Interrupt
- USB Endpoint Management
- USB V_{BUS} Power Control

This total does not include the (up to) 128 BD registers in the BDT. Their prototypes, described in 26.3.1 BDnSTAT and 26.3.2 BDnSTAT, are shown separately in 26.2 USB Buffer Descriptors and the BDT.

All USB OTG registers are implemented in the Least Significant Byte (LSB) of the register. Bits in the upper byte are unimplemented and have no function. Note that some registers are instantiated only in Host mode, while other registers have different bit instantiations and functions in Device and Host modes.

The registers described in the following sections are those that have bits with specific control and configuration features. The following registers are used for data or address values only:

- U1BDTP1, U1BDTP2 and U1BDTP3: Specify the 256-word page in data RAM used for the BDT; 8-bit value with bit 0 fixed as '0' for boundary alignment.
- U1FRML and U1FRMH: Contain the 11-bit byte counter for the current data frame.

26.7 USB Interrupt Registers

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26.7.1 USB OTG Interrupt Status Register (Host Mode Only)

Name: U1OTGIR(2)
Offset: 0x600

Notes:
1. V_{BUS} threshold crossings may either be rising or falling.
2. Individual bits can only be cleared by writing a '1' to the bit position as part of a word write operation on the entire register. Using Boolean instructions or bitwise operations to write to a single bit position will cause all set bits, at the moment of the write, to become cleared.

Legend: HS = Hardware Settable bit; K = Write '1' to Clear bit

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF		VBUSVDIF
Access	HS/R/K	HS/R/K	HS/R/K	HS/R/K	HS/R/K	HS/R/K		HS/R/K
Reset	0	0	0	0	0	0		0

Bit 7 – IDIF ID State Change Indicator bit

Value	Description
1	Change in ID state is detected
0	No ID state change is detected

Bit 6 – T1MSECIF 1 Millisecond Timer bit

Value	Description
1	The 1 millisecond timer has expired
0	The 1 millisecond timer has not expired

Bit 5 – LSTATEIF Line State Stable Indicator bit

Value	Description
1	USB line state (as defined by the SE0 and JSTATE bits) has been stable for 1 ms, but different from the last time
0	USB line state has not been stable for 1 ms

Bit 4 – ACTVIF Bus Activity Indicator bit

Value	Description
1	Activity on the D+/D- lines or V_{BUS} is detected
0	No activity on the D+/D- lines or V_{BUS} is detected

Bit 3 – SESVDIF Session Valid Change Indicator bit

Value	Description
1	V_{BUS} has crossed $V_{A_SESS_END}$ (as defined in the *"USB 2.0 Specification"*)(1)
0	V_{BUS} has not crossed $V_{A_SESS_END}$

Bit 2 – SESENDIF B-Device V_{BUS} Change Indicator bit

Value	Description
1	V_{BUS} change on B-device is detected; V_{BUS} has crossed $V_{B_SESS_END}$ (as defined in the *"USB 2.0 Specification"*)(1)
0	V_{BUS} has not crossed $V_{B_SESS_END}$

Bit 0 – VBUSVDIF A-Device V_{BUS} Change Indicator bit

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Value	Description
1	V_{BUS} change on A-device is detected; V_{BUS} has crossed $V_{A_VBUS}_V_{LD}$ (as defined in the *"USB 2.0 Specification"*)(1)
0	No V_{BUS} change on A-device is detected

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26.7.2 USB OTG Interrupt Enable Register (Host Mode Only)

Name: U1OTGIE
Offset: 0x602

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE		VBUSVDIE
Access	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	0		0

Bit 7 – IDIE ID Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 6 – T1MSECIE 1 Millisecond Timer Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 5 – LSTATEIE Line State Stable Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 4 – ACTVIE Bus Activity Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 3 – SESVDIE Session Valid Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 2 – SESENDIE B-Device Session End Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 0 – VBUSVDIE A-Device V_{BUS} Valid Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

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26.7.3 USB Interrupt Status Register (Device Mode Only)

Name: U1IR(1)
Offset: 0x60A

Note:

1. Individual bits can only be cleared by writing a '1' to the bit position as part of a word write operation on the entire register. Using Boolean instructions or bitwise operations to write to a single bit position will cause all set bits, at the moment of the write, to become cleared.

Legend: HS = Hardware Settable bit; K = Write '1' to Clear bit

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	STALLIF		RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF
Access	HS/R/K		HS/R/K	HS/R/K	HS/R/K	HS/R/K	HS/R/K	HS/R/K
Reset	0		0	0	0	0	0	0

Bit 7 – STALLIF STALL Handshake Interrupt bit

Value	Description
1	A STALL handshake was sent by the peripheral during the handshake phase of the transaction in Device mode
0	A STALL handshake has not been sent

Bit 5 – RESUMEIF Resume Interrupt bit

Value	Description
1	A K-state is observed on the D+ or D- pin for 2.5 µs (differential '1' for low speed, differential '0' for full speed)
0	No K-state is observed

Bit 4 – IDLEIF Idle Detect Interrupt bit

Value	Description
1	Idle condition is detected (constant Idle state of 3 ms or more)
0	No Idle condition is detected

Bit 3 – TRNIF Token Processing Complete Interrupt bit

Value	Description
1	Processing of the current token is complete; read the U1STAT register for endpoint information
0	Processing of the current token is not complete; clear the U1STAT register or load the next token from STAT (clearing this bit causes the STAT FIFO to advance)

Bit 2 – SOFIF Start-of-Frame Token Interrupt bit

Value	Description
1	A Start-of-Frame token is received by the peripheral or the Start-of-Frame threshold is reached by the host
0	No Start-of-Frame token is received or threshold reached

Bit 1 – UERRIF USB Error Condition Interrupt bit

Value	Description
1	An unmasked error condition has occurred; only error states enabled in the U1EIE register can set this bit
0	No unmasked error condition has occurred

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Bit 0 – URSTIF USB Reset Interrupt bit

Value	Description
1	Valid USB Reset has occurred for at least 2.5 µs; Reset state must be cleared before this bit can be reasserted
0	No USB Reset has occurred; individual bits can only be cleared by writing a '1' to the bit position as part of a word write operation on the entire register. Using Boolean instructions or bitwise operations to write to a single bit position will cause all set bits, at the moment of the write, to become cleared.

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26.7.4 USB Interrupt Status Register (Host Mode Only)

Name: U1IR(1)
Offset: 0x60A

Note:

1. Individual bits can only be cleared by writing a '1' to the bit position as part of a word write operation on the entire register. Using Boolean instructions or bitwise operations to write to a single bit position will cause all set bits, at the moment of the write, to become cleared.

Legend: HS = Hardware Settable bit; K = Write '1' to Clear bit

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	DETACHIF
Access	HS/R/K	HS/R/K	HS/R/K	HS/R/K	HS/R/K	HS/R/K	HS/R/K	HS/R/K
Reset	0	0	0	0	0	0	0	0

Bit 7 – STALLIF STALL Handshake Interrupt bit

Value	Description
1	A STALL handshake was sent by the peripheral during the handshake phase of the transaction in Device mode
0	A STALL handshake has not been sent

Bit 6 – ATTACHIF Peripheral Attach Interrupt bit

Value	Description
1	A peripheral attachment has been detected by the module; it is set if the bus state is not SE0 and there has been no bus activity for 2.5 µs
0	No peripheral attachment has been detected

Bit 5 – RESUMEIF Resume Interrupt bit

Value	Description
1	A K-state is observed on the D+ or D- pin for 2.5 µs (differential '1' for low speed, differential '0' for full speed)
0	No K-state is observed

Bit 4 – IDLEIF Idle Detect Interrupt bit

Value	Description
1	Idle condition is detected (constant Idle state of 3 ms or more)
0	No Idle condition is detected

Bit 3 – TRNIF Token Processing Complete Interrupt bit

Value	Description
1	Processing of the current token is complete; read the U1STAT register for endpoint information
0	Processing of the current token is not complete; clear the U1STAT register or load the next token from STAT (clearing this bit causes the STAT FIFO to advance)

Bit 2 – SOFIF Start-of-Frame Token Interrupt bit

Value	Description
1	A Start-of-Frame token is received by the peripheral or the Start-of-Frame threshold is reached by the host
0	No Start-of-Frame token is received or threshold reached

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Bit 1 – UERRIF USB Error Condition Interrupt bit

Value	Description
1	An unmasked error condition has occurred; only error states enabled in the U1EIE register can set this bit
0	No unmasked error condition has occurred

Bit 0 – DETACHIF Detach Interrupt bit

Value	Description
1	A peripheral detachment has been detected by the module; Reset state must be cleared before this bit can be reasserted
0	No peripheral detachment is detected. Individual bits can only be cleared by writing a '1' to the bit position as part of a word write operation on the entire register. Using Boolean instructions or bitwise operations to write to a single bit position will cause all set bits, at the moment of the write, to become cleared.

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26.7.5 USB Interrupt Enable Register (All USB Modes)

Name: U1IE
Offset: 0x60C

Note:
1. This bit is unimplemented in Device mode, read as '0'.

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE or DETACHIE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – STALLIE STALL Handshake Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 6 – ATTACHIE Peripheral Attach Interrupt bit (Host mode only)(1)

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 5 – RESUMEIE Resume Interrupt bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 4 – IDLEIE Idle Detect Interrupt bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 3 – TRNIE Token Processing Complete Interrupt bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 2 – SOFIE Start-of-Frame Token Interrupt bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 1 – UERRIE USB Error Condition Interrupt bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 0 – URSTIE or DETACHIE USB Reset Interrupt (Device mode) or USB Detach Interrupt (Host mode) Enable bit

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Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

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26.7.6 USB Error Interrupt Status Register

Name: U1EIR(1)
Offset: 0x60E

Note:

1. Individual bits can only be cleared by writing a '1' to the bit position as part of a word write operation on the entire register. Using Boolean instructions or bitwise operations to write to a single bit position will cause all set bits, at the moment of the write, to become cleared.

Legend: K = Write '1' to Clear bit; HS = Hardware Settable bit

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	BTSEF		DMAEF	BTOEF	DFN8EF	CRC16EF	CRC5EF or EOFEE	PIDEF
Access	HS/R/K		HS/R/K	HS/R/K	HS/R/K	HS/R/K	HS/R/K	HS/R/K
Reset	0		0	0	0	0	0	0

Bit 7 – BTSEF Bit Stuff Error Flag bit

Value	Description
1	Bit stuff error has been detected
0	No bit stuff error has been detected

Bit 5 – DMAEF DMA Error Flag bit

Value	Description
1	A USB DMA error condition is detected; the data size indicated by the BD byte count field is less than the number of received bytes, the received data are truncated
0	No DMA error

Bit 4 – BTOEF Bus Turnaround Time-out Error Flag bit

Value	Description
1	Bus turnaround time-out has occurred
0	No bus turnaround time-out has occurred

Bit 3 – DFN8EF Data Field Size Error Flag bit

Value	Description
1	Data field was not an integral number of bytes
0	Data field was an integral number of bytes

Bit 2 – CRC16EF CRC16 Failure Flag bit

Value	Description
1	CRC16 failed
0	CRC16 passed

Bit 1 – CRC5EF or EOFEE CRC5 Host Error Flag bit **(For Device Mode Only)**

Value	Description
1	Token packet is rejected due to CRC5 error
0	Token packet is accepted (no CRC5 error)

Bit 1 – EOFEF End-of-Frame (EOF) Error Flag bit **(For Host Mode Only)**

Value	Description
1	End-of-Frame error has occurred

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Value	Description
0	End-of-Frame interrupt is disabled

Bit 0 – PIDEF PID Check Failure Flag bit

Value	Description
1	PID check failed
0	PID check passed

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26.7.7 USB Error Interrupt Enable Register

Name: U1EIE
Offset: 0x610

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	BTSEE		DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE or EOFEE	PIDEE
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit 7 – BTSEE Bit Stuff Error Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 5 – DMAEE DMA Error Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 4 – BTOEE Bus Turnaround Time-out Error Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 3 – DFN8EE Data Field Size Error Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 2 – CRC16EE CRC16 Failure Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 1 – CRC5EE or EOFEE CRC5 Host Error Interrupt Enable bit **(For Device Mode Only)**

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 1 – EOFEE End-of-Frame (EOF) Error interrupt Enable bit **(For Host Mode Only)**

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 0 – PIDEE PID Check Failure Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

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26.8 USB OTG Registers

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26.8.1 USB OTG Status Register (Host Mode Only)

Name: U1OTGSTAT
Offset: 0x604

Legend: HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	ID		LSTATE		SESVD	SESEND		VBUSVD
Access	HSC/R		HSC/R		HSC/R	HSC/R		HSC/R
Reset	0		0		0	0		0

Bit 7 – ID ID Pin State Indicator bit

Value	Description
1	No plug is attached or a Type B cable has been plugged into the USB receptacle
0	A Type A plug has been plugged into the USB receptacle

Bit 5 – LSTATE Line State Stable Indicator bit

Value	Description
1	The USB line state (as defined by SE0 and JSTATE) has been stable for the previous 1 ms
0	The USB line state has not been stable for the previous 1 ms

Bit 3 – SESVD Session Valid Indicator bit

Value	Description
1	The V_{BUS} voltage is above $V_{A_SESS_VLD}$ (as defined in the *"USB 2.0 Specification"*) on the A or B-device
0	The V_{BUS} voltage is below $V_{A_SESS_VLD}$ on the A or B-device

Bit 2 – SESEND B Session End Indicator bit

Value	Description
1	The V_{BUS} voltage is below $V_{B_SESS_END}$ (as defined in the *"USB 2.0 Specification"*) on the B-device
0	The V_{BUS} voltage is above $V_{B_SESS_END}$ on the B-device

Bit 0 – VBUSVD A V_{BUS} Valid Indicator bit

Value	Description
1	The V_{BUS} voltage is above $V_{A_VBUS_VLD}$ (as defined in the *"USB 2.0 Specification"*) on the A-device
0	The V_{BUS} voltage is below $V_{A_VBUS_VLD}$ on the A-device

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26.8.2 USB On-The-Go Control Register

Name: U1OTGCON
Offset: 0x606

Note:
1. These bits are only used in Host mode; do not use in Device mode.

Legend: r = Reserved bit

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	Reserved	OTGEN	Reserved	VBUSDIS
Access	R/W	R/W	R/W	R/W	r	R/W	r	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – DPPULUP D+ Pull-up Enable bit

Value	Description
1	D+ data line pull-up resistor is enabled
0	D+ data line pull-up resistor is disabled

Bit 6 – DMPULUP D- Pull-up Enable bit

Value	Description
1	D- data line pull-up resistor is enabled
0	D- data line pull-up resistor is disabled

Bit 5 – DPPULDWN D+ Pull-Down Enable bit(1)

Value	Description
1	D+ data line pull-down resistor is enabled
0	D+ data line pull-down resistor is disabled

Bit 4 – DMPULDWN D- Pull-Down Enable bit(1)

Value	Description
1	D- data line pull-down resistor is enabled
0	D- data line pull-down resistor is disabled

Bit 3 – Reserved Maintain as '0'

Bit 2 – OTGEN OTG Features Enable bit(1)

Value	Description
1	USB OTG is enabled; all D+/D- pull-up and pull-down bits are enabled
0	USB OTG is disabled; D+/D- pull-up and pull-down bits are controlled in hardware by the settings of the HOSTEN and USBEN (U1CON[3:0]) bits

Bit 1 – Reserved Maintain as '0'

Bit 0 – VBUSDIS V_{BUS} Discharge Enable bit(1)

Value	Description
1	V_{BUS} line is discharged through a resistor
0	V_{BUS} line is not discharged

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26.8.3 USB Power Control Register

Name: U1PWRC
Offset: 0x608

Note:

1. Do not clear this bit unless the HOSTEN, USBEN and OTGEN bits (U1CON[3,0] and U1OTGCON[2]) are all cleared.

Legend: HC = Hardware Clearable bit; HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	UACTPND			USLPGRD			USUSPND	USBPWR
Access	HSC/R			R/W			HC/R/W	R/W
Reset	x			0			0	0

Bit 7 – UACTPND USB Activity Pending bit

Value	Description
1	Module should not be suspended at the moment (requires the USLPGRD bit to be set)
0	Module may be suspended or powered down

Bit 4 – USLPGRD USB Sleep/Suspend Guard bit

Value	Description
1	Indicates to the USB module that it is about to be suspended or powered down
0	No suspend

Bit 1 – USUSPND USB Suspend Mode Enable bit

Value	Description
1	USB OTG module is in Suspend mode; USB clock is gated and the transceiver is placed in a low-power state
0	Normal USB OTG operation

Bit 0 – USBPWR USB Operation Enable bit

Value	Description
1	USB OTG module is enabled
0	USB OTG module is disabled(1)

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26.8.4 USB Status Register

Name: U1STAT
Offset: 0x612

Note:
1. This bit is only valid for endpoints with available even and odd BD registers.

Legend: HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	ENDPT[3:0]				DIR	PPBI		
Access	HSC/R	HSC/R	HSC/R	HSC/R	HSC/R	HSC/R		
Reset	0	0	0	0	0	0		

Bits 7:4 – ENDPT[3:0] USB Activity Pending bits
Number of the last endpoint activity bits.
(Represents the number of the BDT updated by the last USB transfer.)

Value	Description
1111	Endpoint 15
1110	Endpoint 14
...	
0001	Endpoint 1
0000	Endpoint 0

Bit 3 – DIR Last BD Direction Indicator bit

Value	Description
1	The last transaction was a transmit transfer (TX)
0	The last transaction was a receive transfer (RX)

Bit 2 – PPBI Ping-Pong BD Pointer Indicator bit(1)

Value	Description
1	The last transaction was to the odd BD bank
0	The last transaction was to the even BD bank

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26.8.5 USB Control Register (Device Mode)

Name: U1CON
Offset: 0x614

Legend: HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		SE0	PKTDIS		HOSTEN	RESUME	PPBRST	USBEN
Access		HSC/R	R/W		R/W	R/W	R/W	R/W
Reset		x	0		0	0	0	0

Bit 6 – SE0 Live Single-Ended Zero Flag bit

Value	Description
1	Single-ended zero is active on the USB bus
0	No single-ended zero is detected

Bit 5 – PKTDIS Packet Transfer Disable bit

Value	Description
1	SIE token and packet processing are disabled; automatically set when a SETUP token is received
0	SIE token and packet processing are enabled

Bit 3 – HOSTEN Host Mode Enable bit

Value	Description
1	USB host capability is enabled; pull-downs on D+ and D- are activated in hardware
0	USB host capability is disabled

Bit 2 – RESUME Resume Signaling Enable bit

Value	Description
1	Resume signaling is activated
0	Resume signaling is disabled

Bit 1 – PPBRST Ping-Pong Buffers Reset bit

Value	Description
1	Resets all Ping-Pong Buffer Pointers to the even BD banks
0	Ping-Pong Buffer Pointers are not reset

Bit 0 – USBEN USB Module Enable bit

Value	Description
1	USB module and supporting circuitry are enabled (device attached); D+ pull-up is activated in hardware
0	USB module and supporting circuitry are disabled (device detached)

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26.8.6 USB Control Register (Host Mode Only)

Name: U1CON
Offset: 0x614

Legend: HSC = Hardware Settable/Clearable bit

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	JSTATE	SE0	TOKBUSY	USBRST	HOSTEN	RESUME	PPBRST	SOFEN
Access	HSC/R	HSC/R	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	0	0	0	0	0	0

Bit 7 – JSTATE Live Differential Receiver J-State Flag bit

Value	Description
1	J-state (differential '0' in low speed, differential '1' in full speed) is detected on the USB
0	No J-state is detected

Bit 6 – SE0 Live Single-Ended Zero Flag bit

Value	Description
1	Single-ended zero is active on the USB bus
0	No single-ended zero is detected

Bit 5 – TOKBUSY Token Busy Status bit

Value	Description
1	Token is being executed by the USB module in On-The-Go state
0	No token is being executed

Bit 4 – USBRST USB Module Reset bit

Value	Description
1	USB Reset has been generated for a software Reset; application must set this bit for 50 ms, then clear it
0	USB Reset is terminated

Bit 3 – HOSTEN Host Mode Enable bit

Value	Description
1	USB host capability is enabled; pull-downs on D+ and D- are activated in hardware
0	USB host capability is disabled

Bit 2 – RESUME Resume Signaling Enable bit

Value	Description
1	Resume signaling is activated; software must set bit for 10 ms and then clear to enable remote wake-up
0	Resume signaling is disabled

Bit 1 – PPBRST Ping-Pong Buffers Reset bit

Value	Description
1	Resets all Ping-Pong Buffer Pointers to the even BD banks
0	Ping-Pong Buffer Pointers are not reset

Bit 0 – SOFEN Start-of-Frame Enable bit

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Value	Description
1	Start-of-Frame token is sent every one 1 ms
0	Start-of-Frame token is disabled

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26.8.7 USB Address Register

Name: U1ADDR
Offset: 0x616

Note:

1. Host mode only. In Device mode, this bit is unimplemented and read as '0'.

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	LSPDEN	DEVADDR[6:0]						
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – LSPDEN Low-Speed Enable Indicator bit(1)

Value	Description
1	USB module operates at low speed
0	USB module operates at full speed

Bits 6:0 – DEVADDR[6:0] USB Device Address bits

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26.8.8 BDT Address Low Bits Register

Name: U1BDTP1
Offset: 0x618

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	BDTPTRL[6:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

Bits 7:1 – BDTPTRL[6:0] BDT Address Low bits

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26.8.9 Current Data Frame Counter Register Low

Name: U1FRML
Offset: 0x61A

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	FRM[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – FRM[7:0] Data Frame Counter bits

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26.8.10 Current Data Frame Counter Register High

Name: U1FRMH
Offset: 0x61C

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						FRM[10:8]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 2:0 – FRM[10:8] Data Frame Counter bits

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26.8.11 USB Token Register (Host Mode Only)

Name: U1TOK
Offset: 0x61E

Note:
1. All other combinations are reserved and are not to be used.

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	PID[3:0]				EP[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:4 – PID[3:0] Token Type Identifier bits

Value	Description
1101	SETUP (TX) token type transaction(1)
1001	IN (RX) token type transaction(1)
0001	OUT (TX) token type transaction(1)

Bits 3:0 – EP[3:0] Token Command Endpoint Address bits
This value must specify a valid endpoint on the attached device.

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26.8.12 USB OTG Start of Token Threshold Register (Host Mode Only)

Name: U1SOF
Offset: 0x620

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	CNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – CNT[7:0] Start-of-Frame Size bits
Value represents 10 + (packet size of n bytes). For example:

Value	Description
01001010	64-byte packet
00101010	32-byte packet
00010010	8-byte packet

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26.8.13 BDT Address High Bits Register

Name: U1BDTP2
Offset: 0x622

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	BDTPTRH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – BDTPTRH[7:0] BDT Address High bits

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26.8.14 BDT Address Upper Bits Register

Name: U1BDTP3
Offset: 0x624

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	BDTPTRU[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – BDTPTRU[7:0] BDT Address Upper bits

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26.8.15 USB Configuration Register 1

Name: U1CNFG1
Offset: 0x626

Note:
1. This bit is only active when the UTRDIS bit (U1CNFG2[0]) is set.

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	UTEYE	UOEMON		USBSIDL			PPB[1:0]	
Access	R/W	R/W		R/W			R/W	R/W
Reset	0	0		0			0	0

Bit 7 – UTEYE USB Eye Pattern Test Enable bit

Value	Description
1	Eye pattern test is enabled
0	Eye pattern test is disabled

Bit 6 – UOEMON USB $\overline{OE}$ Monitor Enable bit(1)

Value	Description
1	$\overline{OE}$ signal is active; it indicates intervals during which the D+/D- lines are driving
0	$\overline{OE}$ signal is inactive

Bit 4 – USBSIDL USB OTG Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when the device enters Idle mode
0	Continues module operation in Idle mode

Bits 1:0 – PPB[1:0] Ping-Pong Buffers Configuration bits

Value	Description
11	Even/Odd Ping-Pong Buffers are enabled for Endpoints 1 to 15
10	Even/Odd Ping-Pong Buffers are enabled for all endpoints
01	Even/Odd Ping-Pong Buffers are enabled for RX Endpoint 0
00	Even/Odd Ping-Pong Buffers are disabled

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26.8.16 USB Configuration Register 2

Name: U1CNFG2
Offset: 0x628

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				PUVBUS	EXTI2CEN			
Access				R/W	R/W			
Reset				0	0			

Bit 4 – PUVBUS V_{BUS} Pull-up Enable bit

Value	Description
1	Pull-up on V_{BUS} pin is enabled
0	Pull-up on V_{BUS} pin is disabled

Bit 3 – EXTI2CEN I^2C Interface for External Module Control Enable bit

Value	Description
1	External module(s) is controlled via the I^2C interface
0	External module(s) is controlled via the dedicated pins

26.9 USB Endpoint Management Registers

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26.9.1 USB Endpoint 0 Control Register

Name: U1EP0
Offset: 0x62A

Note:

1. These bits are available only for U1EP0 and only in Host mode. For all other U1EPn registers, these bits are always unimplemented and read as '0'.

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	LSPD	RETRYDIS		EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
Access	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Reset	0	0		0	0	0	0	0

Bit 7 – LSPD Low-Speed Direct Connection Enable bit (U1EP0 only)(1)

Value	Description
1	Direct connection to a low-speed device is enabled
0	Direct connection to a low-speed device is disabled

Bit 6 – RETRYDIS Retry Disable bit (U1EP0 only)(1)

Value	Description
1	Retry NAK transactions are disabled
0	Retry NAK transactions are enabled; retry is done in hardware

Bit 4 – EPCONDIS Bidirectional Endpoint Control bit
For All Other Combinations of EPTXEN and EPRXEN:
This bit is ignored.
If EPTXEN and EPRXEN = 1:

Value	Description
1	Disables Endpoint n from control transfers; only TX and RX transfers are allowed
0	Enables Endpoint n for control (SETUP) transfers; TX and RX transfers are also allowed

Bit 3 – EPRXEN Endpoint Receive Enable bit

Value	Description
1	Endpoint n receive is enabled
0	Endpoint n receive is disabled

Bit 2 – EPTXEN Endpoint Transmit Enable bit

Value	Description
1	Endpoint n transmit is enabled
0	Endpoint n transmit is disabled

Bit 1 – EPSTALL Endpoint STALL Status bit

Value	Description
1	Endpoint n was stalled
0	Endpoint n was not stalled

Bit 0 – EPHSHK Endpoint Handshake Enable bit

Value	Description
1	Endpoint handshake is enabled
0	Endpoint handshake is disabled (typically used for isochronous endpoints)

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26.9.2 USB Endpoint 1 Control Register

Name: U1EP1
Offset: 0x62C

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – EPCONDIS Bidirectional Endpoint Control bit
For All Other Combinations of EPTXEN and EPRXEN:
This bit is ignored.
If EPTXEN and EPRXEN = 1:

Value	Description
1	Disables Endpoint n from control transfers; only TX and RX transfers are allowed
0	Enables Endpoint n for control (SETUP) transfers; TX and RX transfers are also allowed

Bit 3 – EPRXEN Endpoint Receive Enable bit

Value	Description
1	Endpoint n receive is enabled
0	Endpoint n receive is disabled

Bit 2 – EPTXEN Endpoint Transmit Enable bit

Value	Description
1	Endpoint n transmit is enabled
0	Endpoint n transmit is disabled

Bit 1 – EPSTALL Endpoint STALL Status bit

Value	Description
1	Endpoint n was stalled
0	Endpoint n was not stalled

Bit 0 – EPHSHK Endpoint Handshake Enable bit

Value	Description
1	Endpoint handshake is enabled
0	Endpoint handshake is disabled (typically used for isochronous endpoints)

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26.9.3 USB Endpoint 2 Control Register

Name: U1EP2
Offset: 0x62E

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – EPCONDIS Bidirectional Endpoint Control bit
For All Other Combinations of EPTXEN and EPRXEN:
This bit is ignored.
If EPTXEN and EPRXEN = 1:

Value	Description
1	Disables Endpoint n from control transfers; only TX and RX transfers are allowed
0	Enables Endpoint n for control (SETUP) transfers; TX and RX transfers are also allowed

Bit 3 – EPRXEN Endpoint Receive Enable bit

Value	Description
1	Endpoint n receive is enabled
0	Endpoint n receive is disabled

Bit 2 – EPTXEN Endpoint Transmit Enable bit

Value	Description
1	Endpoint n transmit is enabled
0	Endpoint n transmit is disabled

Bit 1 – EPSTALL Endpoint STALL Status bit

Value	Description
1	Endpoint n was stalled
0	Endpoint n was not stalled

Bit 0 – EPHSHK Endpoint Handshake Enable bit

Value	Description
1	Endpoint handshake is enabled
0	Endpoint handshake is disabled (typically used for isochronous endpoints)

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26.9.4 USB Endpoint 3 Control Register

Name: U1EP3
Offset: 0x630

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – EPCONDIS Bidirectional Endpoint Control bit
For All Other Combinations of EPTXEN and EPRXEN:
This bit is ignored.
If EPTXEN and EPRXEN = 1:

Value	Description
1	Disables Endpoint n from control transfers; only TX and RX transfers are allowed
0	Enables Endpoint n for control (SETUP) transfers; TX and RX transfers are also allowed

Bit 3 – EPRXEN Endpoint Receive Enable bit

Value	Description
1	Endpoint n receive is enabled
0	Endpoint n receive is disabled

Bit 2 – EPTXEN Endpoint Transmit Enable bit

Value	Description
1	Endpoint n transmit is enabled
0	Endpoint n transmit is disabled

Bit 1 – EPSTALL Endpoint STALL Status bit

Value	Description
1	Endpoint n was stalled
0	Endpoint n was not stalled

Bit 0 – EPHSHK Endpoint Handshake Enable bit

Value	Description
1	Endpoint handshake is enabled
0	Endpoint handshake is disabled (typically used for isochronous endpoints)

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26.9.5 USB Endpoint 4 Control Register

Name: U1EP4
Offset: 0x632

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – EPCONDIS Bidirectional Endpoint Control bit
For All Other Combinations of EPTXEN and EPRXEN:
This bit is ignored.
If EPTXEN and EPRXEN = 1:

Value	Description
1	Disables Endpoint n from control transfers; only TX and RX transfers are allowed
0	Enables Endpoint n for control (SETUP) transfers; TX and RX transfers are also allowed

Bit 3 – EPRXEN Endpoint Receive Enable bit

Value	Description
1	Endpoint n receive is enabled
0	Endpoint n receive is disabled

Bit 2 – EPTXEN Endpoint Transmit Enable bit

Value	Description
1	Endpoint n transmit is enabled
0	Endpoint n transmit is disabled

Bit 1 – EPSTALL Endpoint STALL Status bit

Value	Description
1	Endpoint n was stalled
0	Endpoint n was not stalled

Bit 0 – EPHSHK Endpoint Handshake Enable bit

Value	Description
1	Endpoint handshake is enabled
0	Endpoint handshake is disabled (typically used for isochronous endpoints)

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26.9.6 USB Endpoint 5 Control Register

Name: U1EP5
Offset: 0x634

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – EPCONDIS Bidirectional Endpoint Control bit
For All Other Combinations of EPTXEN and EPRXEN:
This bit is ignored.
If EPTXEN and EPRXEN = 1:

Value	Description
1	Disables Endpoint n from control transfers; only TX and RX transfers are allowed
0	Enables Endpoint n for control (SETUP) transfers; TX and RX transfers are also allowed

Bit 3 – EPRXEN Endpoint Receive Enable bit

Value	Description
1	Endpoint n receive is enabled
0	Endpoint n receive is disabled

Bit 2 – EPTXEN Endpoint Transmit Enable bit

Value	Description
1	Endpoint n transmit is enabled
0	Endpoint n transmit is disabled

Bit 1 – EPSTALL Endpoint STALL Status bit

Value	Description
1	Endpoint n was stalled
0	Endpoint n was not stalled

Bit 0 – EPHSHK Endpoint Handshake Enable bit

Value	Description
1	Endpoint handshake is enabled
0	Endpoint handshake is disabled (typically used for isochronous endpoints)

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26.9.7 USB Endpoint 6 Control Register

Name: U1EP6
Offset: 0x636

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – EPCONDIS Bidirectional Endpoint Control bit
For All Other Combinations of EPTXEN and EPRXEN:
This bit is ignored.
If EPTXEN and EPRXEN = 1:

Value	Description
1	Disables Endpoint n from control transfers; only TX and RX transfers are allowed
0	Enables Endpoint n for control (SETUP) transfers; TX and RX transfers are also allowed

Bit 3 – EPRXEN Endpoint Receive Enable bit

Value	Description
1	Endpoint n receive is enabled
0	Endpoint n receive is disabled

Bit 2 – EPTXEN Endpoint Transmit Enable bit

Value	Description
1	Endpoint n transmit is enabled
0	Endpoint n transmit is disabled

Bit 1 – EPSTALL Endpoint STALL Status bit

Value	Description
1	Endpoint n was stalled
0	Endpoint n was not stalled

Bit 0 – EPHSHK Endpoint Handshake Enable bit

Value	Description
1	Endpoint handshake is enabled
0	Endpoint handshake is disabled (typically used for isochronous endpoints)

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26.9.8 USB Endpoint 7 Control Register

Name: U1EP7
Offset: 0x638

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – EPCONDIS Bidirectional Endpoint Control bit
For All Other Combinations of EPTXEN and EPRXEN:
This bit is ignored.
If EPTXEN and EPRXEN = 1:

Value	Description
1	Disables Endpoint n from control transfers; only TX and RX transfers are allowed
0	Enables Endpoint n for control (SETUP) transfers; TX and RX transfers are also allowed

Bit 3 – EPRXEN Endpoint Receive Enable bit

Value	Description
1	Endpoint n receive is enabled
0	Endpoint n receive is disabled

Bit 2 – EPTXEN Endpoint Transmit Enable bit

Value	Description
1	Endpoint n transmit is enabled
0	Endpoint n transmit is disabled

Bit 1 – EPSTALL Endpoint STALL Status bit

Value	Description
1	Endpoint n was stalled
0	Endpoint n was not stalled

Bit 0 – EPHSHK Endpoint Handshake Enable bit

Value	Description
1	Endpoint handshake is enabled
0	Endpoint handshake is disabled (typically used for isochronous endpoints)

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26.9.9 USB Endpoint 8 Control Register

Name: U1EP8
Offset: 0x63A

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – EPCONDIS Bidirectional Endpoint Control bit
For All Other Combinations of EPTXEN and EPRXEN:
This bit is ignored.
If EPTXEN and EPRXEN = 1:

Value	Description
1	Disables Endpoint n from control transfers; only TX and RX transfers are allowed
0	Enables Endpoint n for control (SETUP) transfers; TX and RX transfers are also allowed

Bit 3 – EPRXEN Endpoint Receive Enable bit

Value	Description
1	Endpoint n receive is enabled
0	Endpoint n receive is disabled

Bit 2 – EPTXEN Endpoint Transmit Enable bit

Value	Description
1	Endpoint n transmit is enabled
0	Endpoint n transmit is disabled

Bit 1 – EPSTALL Endpoint STALL Status bit

Value	Description
1	Endpoint n was stalled
0	Endpoint n was not stalled

Bit 0 – EPHSHK Endpoint Handshake Enable bit

Value	Description
1	Endpoint handshake is enabled
0	Endpoint handshake is disabled (typically used for isochronous endpoints)

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26.9.10 USB Endpoint 9 Control Register

Name: U1EP9
Offset: 0x63C

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – EPCONDIS Bidirectional Endpoint Control bit
For All Other Combinations of EPTXEN and EPRXEN:
This bit is ignored.
If EPTXEN and EPRXEN = 1:

Value	Description
1	Disables Endpoint n from control transfers; only TX and RX transfers are allowed
0	Enables Endpoint n for control (SETUP) transfers; TX and RX transfers are also allowed

Bit 3 – EPRXEN Endpoint Receive Enable bit

Value	Description
1	Endpoint n receive is enabled
0	Endpoint n receive is disabled

Bit 2 – EPTXEN Endpoint Transmit Enable bit

Value	Description
1	Endpoint n transmit is enabled
0	Endpoint n transmit is disabled

Bit 1 – EPSTALL Endpoint STALL Status bit

Value	Description
1	Endpoint n was stalled
0	Endpoint n was not stalled

Bit 0 – EPHSHK Endpoint Handshake Enable bit

Value	Description
1	Endpoint handshake is enabled
0	Endpoint handshake is disabled (typically used for isochronous endpoints)

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26.9.11 USB Endpoint 10 Control Register

Name: U1EP10
Offset: 0x63E

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – EPCONDIS Bidirectional Endpoint Control bit
For All Other Combinations of EPTXEN and EPRXEN:
This bit is ignored.
If EPTXEN and EPRXEN = 1:

Value	Description
1	Disables Endpoint n from control transfers; only TX and RX transfers are allowed
0	Enables Endpoint n for control (SETUP) transfers; TX and RX transfers are also allowed

Bit 3 – EPRXEN Endpoint Receive Enable bit

Value	Description
1	Endpoint n receive is enabled
0	Endpoint n receive is disabled

Bit 2 – EPTXEN Endpoint Transmit Enable bit

Value	Description
1	Endpoint n transmit is enabled
0	Endpoint n transmit is disabled

Bit 1 – EPSTALL Endpoint STALL Status bit

Value	Description
1	Endpoint n was stalled
0	Endpoint n was not stalled

Bit 0 – EPHSHK Endpoint Handshake Enable bit

Value	Description
1	Endpoint handshake is enabled
0	Endpoint handshake is disabled (typically used for isochronous endpoints)

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26.9.12 USB Endpoint 11 Control Register

Name: U1EP11
Offset: 0x640

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – EPCONDIS Bidirectional Endpoint Control bit
For All Other Combinations of EPTXEN and EPRXEN:
This bit is ignored.
If EPTXEN and EPRXEN = 1:

Value	Description
1	Disables Endpoint n from control transfers; only TX and RX transfers are allowed
0	Enables Endpoint n for control (SETUP) transfers; TX and RX transfers are also allowed

Bit 3 – EPRXEN Endpoint Receive Enable bit

Value	Description
1	Endpoint n receive is enabled
0	Endpoint n receive is disabled

Bit 2 – EPTXEN Endpoint Transmit Enable bit

Value	Description
1	Endpoint n transmit is enabled
0	Endpoint n transmit is disabled

Bit 1 – EPSTALL Endpoint STALL Status bit

Value	Description
1	Endpoint n was stalled
0	Endpoint n was not stalled

Bit 0 – EPHSHK Endpoint Handshake Enable bit

Value	Description
1	Endpoint handshake is enabled
0	Endpoint handshake is disabled (typically used for isochronous endpoints)

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26.9.13 USB Endpoint 12 Control Register

Name: U1EP12
Offset: 0x642

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – EPCONDIS Bidirectional Endpoint Control bit
For All Other Combinations of EPTXEN and EPRXEN:
This bit is ignored.
If EPTXEN and EPRXEN = 1:

Value	Description
1	Disables Endpoint n from control transfers; only TX and RX transfers are allowed
0	Enables Endpoint n for control (SETUP) transfers; TX and RX transfers are also allowed

Bit 3 – EPRXEN Endpoint Receive Enable bit

Value	Description
1	Endpoint n receive is enabled
0	Endpoint n receive is disabled

Bit 2 – EPTXEN Endpoint Transmit Enable bit

Value	Description
1	Endpoint n transmit is enabled
0	Endpoint n transmit is disabled

Bit 1 – EPSTALL Endpoint STALL Status bit

Value	Description
1	Endpoint n was stalled
0	Endpoint n was not stalled

Bit 0 – EPHSHK Endpoint Handshake Enable bit

Value	Description
1	Endpoint handshake is enabled
0	Endpoint handshake is disabled (typically used for isochronous endpoints)

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26.9.14 USB Endpoint 13 Control Register

Name: U1EP13
Offset: 0x644

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – EPCONDIS Bidirectional Endpoint Control bit
For All Other Combinations of EPTXEN and EPRXEN:
This bit is ignored.
If EPTXEN and EPRXEN = 1:

Value	Description
1	Disables Endpoint n from control transfers; only TX and RX transfers are allowed
0	Enables Endpoint n for control (SETUP) transfers; TX and RX transfers are also allowed

Bit 3 – EPRXEN Endpoint Receive Enable bit

Value	Description
1	Endpoint n receive is enabled
0	Endpoint n receive is disabled

Bit 2 – EPTXEN Endpoint Transmit Enable bit

Value	Description
1	Endpoint n transmit is enabled
0	Endpoint n transmit is disabled

Bit 1 – EPSTALL Endpoint STALL Status bit

Value	Description
1	Endpoint n was stalled
0	Endpoint n was not stalled

Bit 0 – EPHSHK Endpoint Handshake Enable bit

Value	Description
1	Endpoint handshake is enabled
0	Endpoint handshake is disabled (typically used for isochronous endpoints)

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26.9.15 USB Endpoint 14 Control Register

Name: U1EP14
Offset: 0x646

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – EPCONDIS Bidirectional Endpoint Control bit
For All Other Combinations of EPTXEN and EPRXEN:
This bit is ignored.
If EPTXEN and EPRXEN = 1:

Value	Description
1	Disables Endpoint n from control transfers; only TX and RX transfers are allowed
0	Enables Endpoint n for control (SETUP) transfers; TX and RX transfers are also allowed

Bit 3 – EPRXEN Endpoint Receive Enable bit

Value	Description
1	Endpoint n receive is enabled
0	Endpoint n receive is disabled

Bit 2 – EPTXEN Endpoint Transmit Enable bit

Value	Description
1	Endpoint n transmit is enabled
0	Endpoint n transmit is disabled

Bit 1 – EPSTALL Endpoint STALL Status bit

Value	Description
1	Endpoint n was stalled
0	Endpoint n was not stalled

Bit 0 – EPHSHK Endpoint Handshake Enable bit

Value	Description
1	Endpoint handshake is enabled
0	Endpoint handshake is disabled (typically used for isochronous endpoints)

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26.9.16 USB Endpoint 15 Control Register

Name: U1EP15
Offset: 0x648

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – EPCONDIS Bidirectional Endpoint Control bit
For All Other Combinations of EPTXEN and EPRXEN:
This bit is ignored.
If EPTXEN and EPRXEN = 1:

Value	Description
1	Disables Endpoint n from control transfers; only TX and RX transfers are allowed
0	Enables Endpoint n for control (SETUP) transfers; TX and RX transfers are also allowed

Bit 3 – EPRXEN Endpoint Receive Enable bit

Value	Description
1	Endpoint n receive is enabled
0	Endpoint n receive is disabled

Bit 2 – EPTXEN Endpoint Transmit Enable bit

Value	Description
1	Endpoint n transmit is enabled
0	Endpoint n transmit is disabled

Bit 1 – EPSTALL Endpoint STALL Status bit

Value	Description
1	Endpoint n was stalled
0	Endpoint n was not stalled

Bit 0 – EPHSHK Endpoint Handshake Enable bit

Value	Description
1	Endpoint handshake is enabled
0	Endpoint handshake is disabled (typically used for isochronous endpoints)

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27. Special Features

Notes: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the following sections of the *"dsPIC33/PIC24 Family Reference Manual"*, which are available from the Microchip website (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

- **"Watchdog Timer (WDT)"** (www.microchip.com/DS39697)
- **"High-Level Device Integration"** (www.microchip.com/DS39719)
- **"Programming and Diagnostics"** (www.microchip.com/DS39716)

PIC24FJ64GP205/GU205 family devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation

27.1 Configuration Bits

The Configuration bits are stored in the last page location of implemented program memory. These bits can be set or cleared to select various device configurations. There are two types of Configuration bits: system operation bits and code-protect bits. The system operation bits determine the power-on settings for system-level components, such as the oscillator and the Watchdog Timer. The code-protect bits prevent program memory from being read and written.

27.1.1 Considerations for Configuring PIC24FJ64GP205/GU205 Family Devices

In PIC24FJ64GP205/GU205 family devices, the Configuration bytes are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data are stored in the three words at the top of the on-chip program memory space, known as the Flash Configuration Words. Their specific locations are shown in Table 27-1. The configuration data are automatically loaded from the Flash Configuration Words to the proper Configuration registers during device Resets.

Note: Configuration data are reloaded on all types of device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration Word for configuration data. This is to make certain that program code is not stored in this address when the code is compiled.

The upper byte of all Flash Configuration Words in program memory should always be '0000 0000'. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since Configuration bits are not implemented in the corresponding locations, writing '0's to these locations has no effect on device operation.

Table 27-1. Configuration Word Addresses

Configuration Register	PIC24FJ64GP20X/GU20X	PIC24FJ32GP20X/GU20X
FSEC	0x00AF00	0x005700
FBSLIM	0x00AF10	0x005710
FSIGN	0x00AF14	0x005714
FOSCSEL	0x00AF18	0x005718
FOSC	0x00AF1C	0x00571C
FWDT	0x00AF20	0x005720

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.....continued

Configuration Register	PIC24FJ64GP20X/GU20X	PIC24FJ32GP20X/GU20X
FPOR	0x00AF24	0x005724
FICD	0x00AF28	0x005728
FDMTIVT_L	0x00AF2C	0x00572C
FDMTIVT_H	0x00AF30	0x005730
FDMTCNT_L	0x00AF34	0x005734
FDMTCNT_H	0x00AF38	0x005738
FDMT	0x00AF3C	0x00573C
FDEVOPT1	0x00AF40	0x005740

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27.1.2 FSEC Configuration Register

Name: FSEC

Legend: PO = Program Once bit

Bit	15	14	13	12	11	10	9	8
	AIVTDIS				CSS[2:0]			CWRP
Access	R/PO				R/PO	R/PO	R/PO	R/PO
Reset	1				1	1	1	1

Bit	7	6	5	4	3	2	1	0
	GSS[1:0]		GWRP		BSEN	BSS[1:0]		BWRP
Access	R/PO	R/PO	R/PO		R/PO	R/PO	R/PO	R/PO
Reset	1	1	1		1	1	1	1

Bit 15 – AIVTDIS Alternate Interrupt Vector Table Disable bit

Value	Description
1	Disables AIVT; INTCON2[8] (AIVTEN) bit is not available
0	Enables AIVT; INTCON2[8] (AIVTEN) bit is available

Bits 11:9 – CSS[2:0] Configuration Segment (CS) Code Protection Level bits

Value	Description
111	No protection (other than CWRP)
110	Standard security
10x	Enhanced security
0xx	High security

Bit 8 – CWRP Configuration Segment Program Write Protection bit

Value	Description
1	Configuration Segment is not write-protected
0	Configuration Segment is write-protected

Bits 7:6 – GSS[1:0] General Segment (GS) Code Protection Level bits

Value	Description
11	No protection (other than GWRP)
10	Standard security
0x	High security

Bit 5 – GWRP General Segment Program Write Protection bit

Value	Description
1	General Segment is not write-protected
0	General Segment is write-protected

Bit 3 – BSEN Boot Segment (BS) Control bit

Value	Description
1	No Boot Segment is enabled
0	Boot Segment size is determined by BSLIM[12:0]

Bits 2:1 – BSS[1:0] Boot Segment Code Protection Level bits

Value	Description
11	No protection (other than BWRP)
10	Standard security
0x	High security

Bit 0 – BWRP Boot Segment Program Write Protection bit

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Value	Description
1	Boot Segment can be written
0	Boot Segment is write-protected

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27.1.3 FBSLIM Configuration Register

Name: FBSLIM

Note:

1. The BSLIMx bits are a ‘write-once’ element. If, after the Reset sequence, they are not erased (all ‘1’s), then programming of the FBSLIM bits is prohibited. An attempt to do so will fail to set the WR bit (NVMCON[15]), and consequently, have no effect.

Legend: PO = Program Once bit

PO = Program Once bit

Bit	15	14	13	12	11	10	9	8
				BSLIM[12:8]				
Access				R/PO	R/PO	R/PO	R/PO	R/PO
Reset				1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	BSLIM[7:0]							
Access	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO
Reset	1	1	1	1	1	1	1	1

Bits 12:0 – BSLIM[12:0] Active Boot Segment Code Flash Page Address Limit (Inverted) bits(1)
This bit field contains the last active Boot Segment Page + 1 (i.e., first page address of GS). The value is stored as an inverted page address, such that programming additional ‘0’s can only increase the size of BS. If BSLIM[12:0] is set to all ‘1’s (unprogrammed default), the active Boot Segment size is zero.

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27.1.4 FSIGN Configuration Register

Name: FSIGN

Legend: PO = Program Once bit

Bit	15	14	13	12	11	10	9	8
	SIGN							
Access	R/PO							
Reset	0							

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 15 – SIGN Valid Configuration bit
This bit must be maintained as '0'.

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27.1.5 FOSCSEL Configuration Register

Name: FOSCSEL

Legend: PO = Program Once bit; r = Reserved bit

Bit	15	14	13	12	11	10	9	8
							Reserved[1:0]	
Access							r	r
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	IESO	PLLMODE[3:0]				FNOSC[2:0]		
Access	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO
Reset	1	1	1	1	1	1	1	1

Bits 9:8 – Reserved[1:0] Maintain as '0'

Bit 7 – IESO Two-Speed Oscillator Start-up Enable bit

Value	Description
1	Starts up the device with FRC, then automatically switches to the user-selected oscillator when ready
0	Starts up the device with the user-selected oscillator source

Bits 6:3 – PLLMODE[3:0] Frequency Multiplier Select bits

Value	Description
1111	No PLL is used (PLLEN bit is unavailable)
1110	8x PLL is selected
1101	6x PLL is selected
1100	4x PLL is selected
0111	96 MHz PLL is selected (Input Frequency = 48 MHz)
0110	96 MHz PLL is selected (Input Frequency = 32 MHz)
0101	96 MHz PLL is selected (Input Frequency = 24 MHz)
0100	96 MHz PLL is selected (Input Frequency = 20 MHz)
0011	96 MHz PLL is selected (Input Frequency = 16 MHz)
0010	96 MHz PLL is selected (Input Frequency = 12 MHz)
0001	96 MHz PLL is selected (Input Frequency = 8 MHz)
0000	96 MHz PLL is selected (Input Frequency = 4 MHz)

Bits 2:0 – FNOSC[2:0] Oscillator Selection bits

Value	Description
111	Oscillator with Frequency Divider (OSCFDIV)
110	Reserved
101	Low-Power RC Oscillator (LPRC)
100	Secondary Oscillator (SOSC)
011	Primary Oscillator with PLL (XTPLL, HSPLL, ECPLL)
010	Primary Oscillator (XT, HS, EC)
001	Fast RC Oscillator with PLL (FRCPLL)
000	Fast RC Oscillator (FRC)

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27.1.6 FOSC Configuration Register

Name: FOSC

Legend: PO = Program Once bit

Note:

1. PLSS is set to PRI by default. If POSC is disabled/not present, PLLSS = PRI is an invalid configuration. PLLSS should be set to FRC in such condition.

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	FCKSM[1:0]		IOL1WAY	PLLSS	SOSCSEL	OSCIOFCN	POSCMD[1:0]	
Access	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO
Reset	1	1	1	1	1	1	1	1

Bits 7:6 – FCKSM[1:0] Clock Switching and Monitor Selection bits

Value	Description
1x	Clock switching and the Fail-Safe Clock Monitor are disabled
01	Clock switching is enabled, Fail-Safe Clock Monitor is disabled
00	Clock switching and the Fail-Safe Clock Monitor are enabled

Bit 5 – IOL1WAY Peripheral Pin Select Configuration bit

Value	Description
1	The IOLOCK bit can be set only once (with unlock sequence)
0	The IOLOCK bit can be set and cleared as needed (with unlock sequence)

Bit 4 – PLLSS PLL Secondary Selection Configuration bit(1)

This Configuration bit only takes effect when the PLL is NOT being used by the system (i.e., not selected as part of the system clock source). Used to generate an independent clock out of REFO.

Value	Description
1	PLL is fed by the Primary Oscillator
0	PLL is fed by the on-chip Fast RC (FRC) Oscillator

Bit 3 – SOSCSEL SOSC Selection Configuration bit

Value	Description
1	Crystal (SOSCI/SOSCO) mode
0	Digital (SCLKI) Externally Supplied Clock mode

Bit 2 – OSCIOFCN CLKO Enable Configuration bit

Value	Description
1	CLKO output signal is active on the OSCO pin (when the Primary Oscillator is disabled or configured for EC mode)
0	CLKO output is disabled

Bits 1:0 – POSCMD[1:0] Primary Oscillator Configuration bits

Value	Description
11	Primary Oscillator mode is disabled
10	HS Oscillator mode is selected (10 MHz-32 MHz)
01	XT Oscillator mode is selected (1.5 MHz-10 MHz)
00	External Clock mode is selected

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27.1.7 FWDT Configuration Register

Name: FWDT

Legend: PO = Program Once bit

Bit	15	14	13	12	11	10	9	8
		WDTCLK[1:0]			WDTCMX		WDTWIN[1:0]	
Access		R/PO	R/PO		R/PO		R/PO	R/PO
Reset		1	1		1		1	1

Bit	7	6	5	4	3	2	1	0
	WINDIS	FWDTEN[1:0]		FWPSA	WDTPS[3:0]			
Access	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO
Reset	1	1	1	1	1	1	1	1

Bits 14:13 – WDTCLK[1:0] Watchdog Timer Clock Select bits (when WDTCMX = 1)

Value	Description
11	Always uses LPRC
10	Uses FRC when WINDIS = 0, system clock is not LPRC and device is not in Sleep; otherwise, uses LPRC
01	Always uses SOSC
00	Uses peripheral clock when system clock is not LPRC and device is not in Sleep; otherwise, uses LPRC

Bit 11 – WDTCMX WDT Clock MUX Control bit

Value	Description
1	Enables WDT clock MUX, WDT clock is selected by WDTCLK[1:0]
0	WDT clock is LPRC

Bits 9:8 – WDTWIN[1:0] Watchdog Timer Window Width bits

Value	Description
11	WDT window is 25% of the WDT period
10	WDT window is 37.5% of the WDT period
01	WDT window is 50% of the WDT period
00	WDT window is 75% of the WDT period

Bit 7 – WINDIS Windowed Watchdog Timer Disable bit

Value	Description
1	Windowed WDT is disabled
0	Windowed WDT is enabled

Bits 6:5 – FWDTEN[1:0] Watchdog Timer Enable bits

Value	Description
11	WDT is enabled
10	WDT is disabled (control is placed on the SWDTEN bit)
01	WDT is enabled only while device is active and disabled in Sleep; SWDTEN bit is disabled
00	WDT and SWDTEN are disabled

Bit 4 – FWPSA Watchdog Timer Prescaler bit

Value	Description
1	WDT prescaler ratio of 1:128
0	WDT prescaler ratio of 1:32

Bits 3:0 – WDTPS[3:0] Watchdog Timer Postscale Select bits

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Value	Description
1111	1:32,768
1110	1:16,384
1101	1:8,192
1100	1:4,096
1011	1:2,048
1010	1:1,024
1001	1:512
1000	1:256
0111	1:128
0110	1:64
0101	1:32
0100	1:16
0011	1:8
0010	1:4
0001	1:2
0000	1:1

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27.1.8 FPOR Configuration Register

Name: FPOR

Legend: PO = Program Once bit

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					LPBOREN	LPREGEN	BOREN[1:0]	
Access					R/PO	R/PO	R/PO	R/PO
Reset					1	1	1	1

Bit 3 – LPBOREN Low-Power Brown-out Reset Enable bit

Value	Description
1	Low-power BOR is enabled and active when main BOR is inactive
0	Low-power BOR is disabled

Bit 2 – LPREGEN Low-Voltage Regulator Control bit

Value	Description
1	Low-voltage and low-power regulator are not available
0	Low-voltage and low-power regulator are available and controlled by the RETEN bit during Sleep mode

Bits 1:0 – BOREN[1:0] Brown-out Reset Enable bits

Value	Description
11	Brown-out Reset is enabled in hardware; SBOREN bit is disabled
10	Brown-out Reset is enabled only while device is active and is disabled in Sleep; SBOREN bit is disabled
01	Brown-out Reset is controlled with the SBOREN bit setting
00	Brown-out Reset is disabled in hardware; SBOREN bit is disabled

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27.1.9 FICD Configuration Register

Name: FICD

Legend: PO = Program Once bit; r = Reserved bit

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	Reserved		$\overline{\text{JTAGEN}}$				ICS[1:0]	
Access	r		R/PO				R/PO	R/PO
Reset	1		1				1	1

Bit 7 – Reserved Maintain as '1'

Bit 5 – $\overline{\text{JTAGEN}}$ JTAG Port Enable bit

Value	Description
1	JTAG port is enabled
0	JTAG port is disabled

Bits 1:0 – ICS[1:0] ICD Communication Channel Select bits

Value	Description
11	Communicates on PGEC1/PGED1
10	Communicates on PGEC2/PGED2
01	Communicates on PGEC3/PGED3
00	Reserved; do not use

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27.1.10 FDMTIVTL Configuration Register

Name: FDMTIVTL

Legend: PO = Program Once bit

Bit	15	14	13	12	11	10	9	8
	DMTIVTL[15:8]							
Access	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	DMTIVTL[7:0]							
Access	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO
Reset	1	1	1	1	1	1	1	1

Bits 15:0 – DMTIVTL[15:0] DMT Window Interval Lower 16 bits

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27.1.11 FDMTIVTH Configuration Register

Name: FDMTIVTH

Legend: PO = Program Once bit

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DMTIVTH[31:24]							
Access	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	DMTIVTH[23:16]							
Access	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO
Reset	1	1	1	1	1	1	1	1

Bits 15:8 – DMTIVTH[31:24] DMT Window Interval Higher 16 bits

Bits 7:0 – DMTIVTH[23:16] DMT Window Interval Higher 16 bits

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27.1.12 FDMTCNTL Configuration Register

Name: FDMTCNTL

Legend: PO = Program Once bit

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DMTCNTL[15:8]							
Access	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	DMTCNTL[7:0]							
Access	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO
Reset	1	1	1	1	1	1	1	1

Bits 15:0 – DMTCNTL[15:0] DMT Instruction Count Time-out Value Lower 16 bits

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27.1.13 FDMTCNTH Configuration Register

Name: FDMTCNTH

Legend: PO = Program Once bit

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DMTCNTH[31:24]							
Access	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	DMTCNTH[23:16]							
Access	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO	R/PO
Reset	1	1	1	1	1	1	1	1

Bits 15:8 – DMTCNTH[31:24] DMT Instruction Count Time-out Value Higher 16 bits

Bits 7:0 – DMTCNTH[23:16] DMT Instruction Count Time-out Value Higher 16 bits

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27.1.14 FDMT Configuration Register

Name: FDMT

Legend: PO = Program Once bit

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
Access								R/PO
Reset								1

Bit 0 – DMTDIS DMT Disable bit

Value	Description
1	DMT is disabled
0	DMT is enabled

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27.1.15 FDEVOPT1 Configuration Register

Name: FDEVOPT1

Note:
1. SMBus mode is enabled by the SMEN bit (I2CxCONL[8]).

Legend: PO = Program Once bit

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
						SMB3EN		
Access						R/PO		
Reset						1		

Bit	7	6	5	4	3	2	1	0
			ALTCMP2	ALTI2C1	SOSCHP	TMPRPIN	ALTCMP1	
Access			R/PO	R/PO	R/PO	R/PO	R/PO	
Reset			1	1	1	1	1	

Bit 10 – SMB3EN SMBus 3.0 Levels Enable bit(1)

Value	Description
1	SMBus 3.0 input levels
0	Normal SMBus input levels

Bit 5 – ALTCMP2 Alternate Comparator Input Enable bit 2

Value	Description
1	C2INC and C2IND are on RA4 and RB4
0	AC2INC and AC2IND are on RB9 and RA3

Bit 4 – ALTI2C1 Alternate I2C1 bit

Value	Description
1	SDA1 and SCL1 are on RB8 and RB9
0	ASDA1 and ASCL1 are on RB5 and RB6

Bit 3 – SOSCHP SOSC High-Power Enable bit (valid only when SOSCSEL = 1)

Value	Description
1	SOSC High-Power mode is enabled
0	SOSC Low-Power mode is enabled (see 9.7.3 Low-Power Operation for more information)

Bit 2 – TMPRPIN Tamper Pin Enable bit

Value	Description
1	$\overline{\text{TMPRN}}$ pin function is disabled
0	$\overline{\text{TMPRN}}$ pin function is enabled

Bit 1 – ALTCMP1 Alternate Comparator Input Enable bit 1

Value	Description
1	C1INC and C3INC are on RB13 and RA0
0	AC1INC and AC3INC are on RB9

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27.2 Device Identification

The PIC24FJ64GP205/GU205 devices have two Identification registers near the end of configuration memory space that store the Device ID (DEVID) and Device Revision (DEVREV). These registers are used to determine the variant and manufacturing information about the device. These registers are read-only and are shown in 27.2.2 DEVID and 27.2.1 DEVREV.

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27.2.1 Device Revision Register

Name: DEVREV

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					DEVREV[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – DEVREV[3:0] Device Revision bits

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27.2.2 DEVID Device ID Register

Name: DEVID

Note:
1. See 27.2.3 Device IDs for the list of Device Identifier bits.

Bit	15	14	13	12	11	10	9	8
	FAMID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEV[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – FAMID[7:0] Device Family Identifier bits
(23h = PIC24FJ64GU205 family)

Bits 7:0 – DEV[7:0] Individual Device Identifier bits(1)

27.2.3 Device IDs

Table 27-2. Device IDs

Device	DEVID	Device	DEVID
PIC24FJ64GP205	9A18	PIC24FJ64GU205	9A19
PIC24FJ32GP205	9A08	PIC24FJ32GU205	9A09
PIC24FJ64GP203	9A14	PIC24FJ64GU203	9A15
PIC24FJ32GP203	9A04	PIC24FJ32GU203	9A05
PIC24FJ64GP202	9A10	PIC24FJ64GU202	9A11
PIC24FJ32GP202	9A00	PIC24FJ32GU202	9A01

27.3 Unique Device Identifier (UDID)

All PIC24FJ64GP205/GU205 family devices are individually encoded during final manufacturing with a Unique Device Identifier or UDID. The UDID cannot be erased by a bulk erase command or any other user-accessible means. This feature allows for manufacturing traceability of Microchip Technology devices in applications where this is a requirement. It may also be used by the application manufacturer for any number of things that may require unique identification, such as:

- Tracking the device
- Unique serial number
- Unique security key

The UDID comprises five 24-bit program words. When taken together, these fields form a unique 120-bit identifier.

The UDID is stored in five read-only locations, located between 0x801600 and 0x801608 in the device Configuration space. Table 27-3 lists the addresses of the Identifier Words and shows their contents.

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Table 27-3. UDID Addresses

UDID	Address	Description
UDID1	0x80 1600	UDID Word 1
UDID2	0x80 1602	UDID Word 2
UDID3	0x80 1604	UDID Word 3
UDID4	0x80 1606	UDID Word 4
UDID5	0x80 1608	UDID Word 5

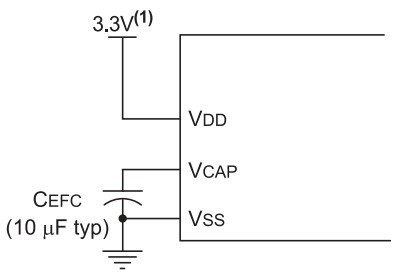
27.4 On-Chip Voltage Regulator

All PIC24FJ64GP205/GU205 family devices power their core digital logic at a nominal 1.8V. This may create an issue for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the PIC24FJ64GP205/GU205 family incorporate an on-chip regulator that allows the device to run its core logic from V_{DD}.

This regulator is always enabled. It provides a constant voltage (1.8V nominal) to the digital core logic, from a V_{DD} of 2.0V, all the way up to the device's V_{DDMAX}. It does not have the capability to boost V_{DD} levels. In order to prevent "brown-out" conditions when the voltage drops too low for the regulator, the Brown-out Reset occurs. Then, the regulator output follows V_{DD} with a typical voltage drop of 200 mV.

A low-ESR capacitor (such as ceramic) must be connected to the V_{CAP} pin (Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the Filter Capacitor (C_{EFC}) is provided in 30. Electrical Characteristics.

Figure 27-1. Connections for the On-Chip Regulator



Note:

1. This is a typical operating voltage. Refer to 30. Electrical Characteristics for the full operating ranges of V_{DD}.

27.4.1 On-Chip Regulator and POR

The voltage regulator takes approximately 10 µs for it to generate output. During this time, designated as T_{VREG}, code execution is disabled. T_{VREG} is applied every time the device resumes operation after any power-down, including Sleep mode. T_{VREG} is determined by the status of the VREGS bit (RCON[8]) and the WDTWIN[1:0] Configuration bits (FWDT[9:8]).

27.4.2 Voltage Regulator Standby Mode

The on-chip regulator always consumes a small incremental amount of current over I_{DD}/I_{PD}, including when the device is in Sleep mode, even though the core digital logic does not require power. To provide additional savings in applications where power resources are critical, the regulator can be made to enter Standby mode, on its own, whenever the device goes into Sleep mode. This feature is controlled by the VREGS bit (RCON[8]). Clearing the VREGS bit enables the Standby mode. When waking up from Standby mode, the regulator needs to wait for T_{VREG} to expire before wake-up.

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27.4.3 Low-Voltage Regulator

When in Sleep mode, PIC24FJ64GP205/GU205 family devices may use a separate low-power, low-voltage regulator to power critical circuits. This regulator, which operates from 0.9V to 1.2V, maintains power to data RAM and the RTCC while all other core digital logic is powered down. The low-voltage regulator is described in more detail in 10.2.4 Low-Voltage Regulator Mode and Band Gap Power.

27.5 Watchdog Timer (WDT)

For PIC24FJ64GP205/GU205 family devices, the WDT is driven by the LPRC Oscillator, the Secondary Oscillator (SOSC) or the system timer. When the device is in Sleep mode, the LPRC Oscillator will be used. When the WDT is enabled, the clock source is also enabled.

The nominal WDT clock source from LPRC is 32 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the FWPSA Configuration bit. With a 32 kHz input, the prescaler yields a nominal WDT Time-out (T_{WDT}) period of 1 ms in 5-bit mode or 4 ms in 7-bit mode.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPS[3:0] Configuration bits (FWDT[3:0]), which allows the selection of a total of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler time-out periods, ranges from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSCx bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a `PWRSAV` instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a `CLRWDT` instruction during normal execution

If the WDT is enabled, it will continue to run during Sleep or Idle modes. When the WDT time-out occurs, the device will wake-up and code execution will continue from where the `PWRSAV` instruction was executed. The corresponding SLEEP or IDLE (RCON[3:2]) bits will need to be cleared in software after the device wakes up.

The WDT Flag bit, WDTO (RCON[4]), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

Note: The `CLRWDT` and `PWRSAV` instructions clear the prescaler and postscaler counts when executed.

27.5.1 Windowed Operation

The Watchdog Timer has an optional Fixed Window mode of operation. In this Windowed mode, `CLRWDT` instructions can only reset the WDT during the last 1/4 of the programmed WDT period. A `CLRWDT` instruction executed before that window causes a WDT Reset, similar to a WDT time-out.

Windowed WDT mode is enabled by programming the WINDIS Configuration bit (FWDT[7]) to '`0`'.

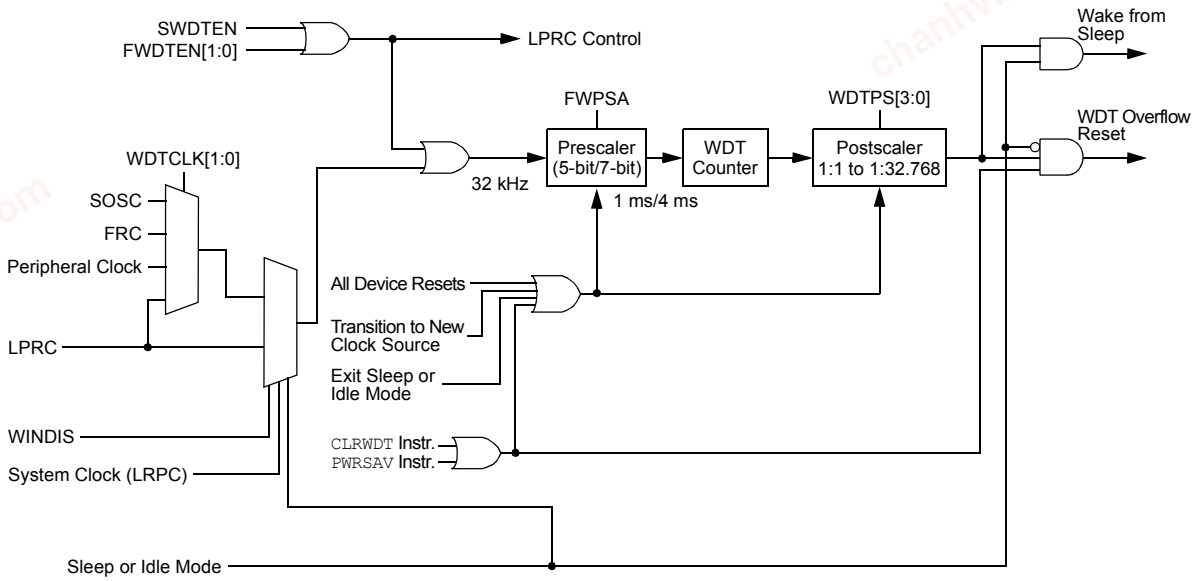
27.5.2 Control Register

The WDT is enabled or disabled by the FWDTEN[1:0] Configuration bits (FWDT[6:5]). When the Configuration bits, FWDTEN[1:0] = `11`, the WDT is always enabled.

The WDT can be optionally controlled in software when the Configuration bits, FWDTEN[1:0] = `10`. When FWDTEN[1:0] = `00`, the Watchdog Timer is always disabled. The WDT is enabled in software by setting the SWDTEN control bit (RCON[5]). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user to enable the WDT for critical code segments and disable the WDT during non-critical code segments for maximum power savings.

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Figure 27-2. WDT Block Diagram



27.6 Program Verification and Code Protection

PIC24FJ64GP205/GU205 family devices offer basic implementation of CodeGuard™ Security that supports General Segment (GS) security and Boot Segment (BS) security. This feature helps protect individual intellectual property.

Note: For more information on usage, configuration and operation, refer to **"CodeGuard™ Intermediate Security"** (www.microchip.com/DS70005182) in the *"dsPIC33/PIC24 Family Reference Manual"*.

27.7 JTAG Interface

PIC24FJ64GP205/GU205 family devices implement a JTAG interface, which supports boundary scan device testing.

27.8 In-Circuit Serial Programming™ (ICSP)™

PIC24FJ64GP205/GU205 family microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock (PGECx) and data (PGEDx), and three other lines for power (V_{DD}), ground (V_{SS}) and $\overline{MCLR}$. This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

27.9 Customer OTP Memory

PIC24FJ64GP205/GU205 family devices provide 256 bytes of One-Time-Programmable (OTP) memory, located at addresses, 801700h through 8017FEh. This memory can be used for persistent storage of application-specific information that will not be erased by reprogramming the device. This includes many types of information, such as (but not limited to):

- Application checksums
- Code revision information
- Product information
- Serial numbers

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- System manufacturing dates
- Manufacturing lot numbers

Customer OTP memory may be programmed in any mode, including user RTSP mode, but it cannot be erased. Data are not cleared by a chip erase.

Note: Do not write the OTP memory more than once. Writing to the OTP memory more than once may result in an ECC Double-Bit Error (ECCDBE).

27.10 In-Circuit Debugger

This function allows simple debugging functions when used with MPLAB® IDE. Debugging functionality is controlled through the PGECx (Emulation/Debug Clock) and PGEDx (Emulation/Debug Data) pins.

To use the in-circuit debugger function of the device, the design must implement ICSP connections to $\overline{MCLR}$, V_{DD}, V_{SS} and the PGECx/PGEDx pin pair, designated by the ICS[1:0] Configuration bits. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins.

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28. Development Support

Move a design from concept to production in record time with Microchip's award-winning development tools. Microchip tools work together to provide state of the art debugging for any project with easy-to-use Graphical User Interfaces (GUIs) in our free MPLAB® X and Atmel Studio Integrated Development Environments (IDEs), and our code generation tools. Providing the ultimate ease-of-use experience, Microchip's line of programmers, debuggers and emulators work seamlessly with our software tools. Microchip development boards help evaluate the best silicon device for an application, while our line of third party tools round out our comprehensive development tool solutions.

Microchip's MPLAB X and Atmel Studio ecosystems provide a variety of embedded design tools to consider, which support multiple devices, such as PIC® MCUs, AVR® MCUs, SAM MCUs and dsPIC® DSCs. MPLAB X tools are compatible with Windows®, Linux® and Mac® operating systems while Atmel Studio tools are compatible with Windows.

Go to the following website for more information and details:

https://www.microchip.com/development-tools/

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29. Instruction Set Summary

Note: This chapter is a brief summary of the PIC24F Instruction Set Architecture (ISA) and is not intended to be a comprehensive reference source.

The PIC24F instruction set adds many enhancements to the previous PIC® MCU instruction sets, while maintaining an easy migration from previous PIC MCU instruction sets. Most instructions are a single program memory word. Only three instructions require two program memory locations.

Each single-word instruction is a 24-bit word divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction. The instruction set is highly orthogonal and is grouped into four basic categories:

- Word or byte-oriented operations
- Bit-oriented operations
- Literal operations
- Control operations

Table 29-1 shows the general symbols used in describing the instructions. The PIC24F instruction set summary in Table 29-2 lists all the instructions, along with the status flags affected by each instruction.

Most word or byte-oriented W register instructions (including barrel shift instructions) have three operands:

- The first source operand, which is typically a register, ‘Wb’, without any address modifier
- The second source operand, which is typically a register, ‘Ws’, with or without an address modifier
- The destination of the result, which is typically a register, ‘Wd’, with or without an address modifier

However, word or byte-oriented file register instructions have two operands:

- The file register specified by the value, ‘f’
- The destination, which could either be the file register, ‘f’, or the W0 register, which is denoted as ‘WREG’

Most bit-oriented instructions (including simple rotate/shift instructions) have two operands:

- The W register (with or without an address modifier) or file register (specified by the value of ‘Ws’ or ‘f’)
- The bit in the W register or file register (specified by a literal value or indirectly by the contents of register, ‘Wb’)

The literal instructions that involve data movement may use some of the following operands:

- A literal value to be loaded into a W register or file register (specified by the value of ‘k’)
- The W register or file register where the literal value is to be loaded (specified by ‘Wb’ or ‘f’)

However, literal instructions that involve arithmetic or logical operations use some of the following operands:

- The first source operand, which is a register, ‘Wb’, without any address modifier
- The second source operand, which is a literal value
- The destination of the result (only if not the same as the first source operand), which is typically a register, ‘Wd’, with or without an address modifier

The control instructions may use some of the following operands:

- A program memory address
- The mode of the Table Read and Table Write instructions

All instructions are a single word, except for certain double-word instructions, which were made double-word instructions so that all the required information is available in these 48 bits. In the second word, the eight MSbs are ‘0’s. If this second word is executed as an instruction (by itself), it will execute as a NOP.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true or the Program Counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles, with the additional instruction cycle(s) executed as a NOP. Notable exceptions are the BRA (unconditional/computed branch), indirect CALL/GOTO, all Table Reads and Table Writes, and RETURN/RETFIE instructions, which are single-word instructions but take two or three cycles.

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Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles. The double-word instructions execute in two instruction cycles.

Table 29-1. Symbols Used In Opcode Descriptions

Field	Description
#text	Means literal defined by "text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{ }	Optional field or operation
[n:m]	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.w	Word mode selection (default)
bit4	4-bit Bit Selection field (used in word-addressed instructions) ∈ {0...15}
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address ∈ {0000h...1FFFh}
lit1	1-bit unsigned literal ∈ {0,1}
lit4	4-bit unsigned literal ∈ {0...15}
lit5	5-bit unsigned literal ∈ {0...31}
lit8	8-bit unsigned literal ∈ {0...255}
lit10	10-bit unsigned literal ∈ {0...255} for Byte mode, {0...1023} for Word mode
lit14	14-bit unsigned literal ∈ {0...16383}
lit16	16-bit unsigned literal ∈ {0...65535}
lit23	23-bit unsigned literal ∈ {0...8388607}; LSb must be '0'
None	Field does not require an entry, may be blank
PC	Program Counter
Slit10	10-bit signed literal ∈ {-512...511}
Slit16	16-bit signed literal ∈ {-32768...32767}
Slit6	6-bit signed literal ∈ {-16...16}
Wb	Base W register ∈ {W0..W15}
Wd	Destination W register ∈ { Wd, [Wd], [Wd++], [Wd--], [++Wd], [--Wd] }
Wdo	Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] }
Wm,Wn	Dividend, Divisor Working register pair (direct addressing)
Wn	One of 16 Working registers ∈ {W0..W15}

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Field	Description
Wnd	One of 16 destination Working registers ∈ {W0..W15}
Wns	One of 16 source Working registers ∈ {W0..W15}
WREG	W0 (Working register used in file register instructions)
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws--], [++Ws], [--Ws] }
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns--], [++Wns], [--Wns], [Wns+Wb] }

Table 29-2. Instruction Set Overview

Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
ADD	ADD	f	f = f + WREG	1	1	C, DC, N, OV, Z
	ADD	f,WREG	WREG = f + WREG	1	1	C, DC, N, OV, Z
	ADD	#lit10,Wn	Wd = lit10 + Wd	1	1	C, DC, N, OV, Z
	ADD	Wb,Ws,Wd	Wd = Wb + Ws	1	1	C, DC, N, OV, Z
	ADD	Wb,#lit5,Wd	Wd = Wb + lit5	1	1	C, DC, N, OV, Z
ADDC	ADDC	f	f = f + WREG + (C)	1	1	C, DC, N, OV, Z
	ADDC	f,WREG	WREG = f + WREG + (C)	1	1	C, DC, N, OV, Z
	ADDC	#lit10,Wn	Wd = lit10 + Wd + (C)	1	1	C, DC, N, OV, Z
	ADDC	Wb,Ws,Wd	Wd = Wb + Ws + (C)	1	1	C, DC, N, OV, Z
	ADDC	Wb,#lit5,Wd	Wd = Wb + lit5 + (C)	1	1	C, DC, N, OV, Z
AND	AND	f	f = f .AND. WREG	1	1	N, Z
	AND	f,WREG	WREG = f .AND. WREG	1	1	N, Z
	AND	#lit10,Wn	Wd = lit10 .AND. Wd	1	1	N, Z
	AND	Wb,Ws,Wd	Wd = Wb .AND. Ws	1	1	N, Z
	AND	Wb,#lit5,Wd	Wd = Wb .AND. lit5	1	1	N, Z
ASR	ASR	f	f = Arithmetic Right Shift f	1	1	C, N, OV, Z
	ASR	f,WREG	WREG = Arithmetic Right Shift f	1	1	C, N, OV, Z
	ASR	Ws,Wd	Wd = Arithmetic Right Shift Ws	1	1	C, N, OV, Z
	ASR	Wb,Wns,Wnd	Wnd = Arithmetic Right Shift Wb by Wns	1	1	N, Z
	ASR	Wb,#lit5,Wnd	Wnd = Arithmetic Right Shift Wb by lit5	1	1	N, Z
BCLR	BCLR	f,#bit4	Bit Clear f	1	1	None
	BCLR	Ws,#bit4	Bit Clear Ws	1	1	None

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Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
BRA	BRA	C,Expr	Branch if Carry	1	1 (2)	None
	BRA	GE,Expr	Branch if Greater Than or Equal	1	1 (2)	None
	BRA	GEU,Expr	Branch if Unsigned Greater Than or Equal	1	1 (2)	None
	BRA	GT,Expr	Branch if Greater Than	1	1 (2)	None
	BRA	GTU,Expr	Branch if Unsigned Greater Than	1	1 (2)	None
	BRA	LE,Expr	Branch if Less Than or Equal	1	1 (2)	None
	BRA	LEU,Expr	Branch if Unsigned Less Than or Equal	1	1 (2)	None
	BRA	LT,Expr	Branch if Less Than	1	1 (2)	None
	BRA	LTU,Expr	Branch if Unsigned Less Than	1	1 (2)	None
	BRA	N,Expr	Branch if Negative	1	1 (2)	None
	BRA	NC,Expr	Branch if Not Carry	1	1 (2)	None
	BRA	NN,Expr	Branch if Not Negative	1	1 (2)	None
	BRA	NOV,Expr	Branch if Not Overflow	1	1 (2)	None
	BRA	NZ,Expr	Branch if Not Zero	1	1 (2)	None
	BRA	OV,Expr	Branch if Overflow	1	1 (2)	None
	BRA	Expr	Branch Unconditionally	1	2	None
	BRA	Z,Expr	Branch if Zero	1	1 (2)	None
	BRA	Wn	Computed Branch	1	2	None
BSET	BSET	f,#bit4	Bit Set f	1	1	None
	BSET	Ws,#bit4	Bit Set Ws	1	1	None
BSW	BSW.C	Ws,Wb	Write C bit to Ws[Wb]	1	1	None
	BSW.Z	Ws,Wb	Write Z bit to Ws[Wb]	1	1	None
BTG	BTG	f,#bit4	Bit Toggle f	1	1	None
	BTG	Ws,#bit4	Bit Toggle Ws	1	1	None
BTSC	BTSC	f,#bit4	Bit Test f, Skip if Clear	1	1 (2 or 3)	None
	BTSC	Ws,#bit4	Bit Test Ws, Skip if Clear	1	1 (2 or 3)	None
BTSS	BTSS	f,#bit4	Bit Test f, Skip if Set	1	1 (2 or 3)	None
	BTSS	Ws,#bit4	Bit Test Ws, Skip if Set	1	1 (2 or 3)	None

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Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
BTST	BTST	f,#bit4	Bit Test f	1	1	Z
	BTST.C	Ws,#bit4	Bit Test Ws to C	1	1	C
	BTST.Z	Ws,#bit4	Bit Test Ws to Z	1	1	Z
	BTST.C	Ws,Wb	Bit Test Ws[Wb] to C	1	1	C
	BTST.Z	Ws,Wb	Bit Test Ws[Wb] to Z	1	1	Z
BTSTS	BTSTS	f,#bit4	Bit Test, then Set f	1	1	Z
	BTSTS.C	Ws,#bit4	Bit Test Ws to C, then Set	1	1	C
	BTSTS.Z	Ws,#bit4	Bit Test Ws to Z, then Set	1	1	Z
CALL	CALL	lit23	Call Subroutine	2	2	None
	CALL	Wn	Call Indirect Subroutine	1	2	None
CLR	CLR	f	f = 0x0000	1	1	None
	CLR	WREG	WREG = 0x0000	1	1	None
	CLR	Ws	Ws = 0x0000	1	1	None
CLRWDT	CLRWDT		Clear Watchdog Timer	1	1	WDTO, Sleep
COM	COM	f	$f = \bar{f}$	1	1	N, Z
	COM	f,WREG	$WREG = \bar{f}$	1	1	N, Z
	COM	Ws,Wd	$Wd = \overline{Ws}$	1	1	N, Z
CP	CP	f	Compare f with WREG	1	1	C, DC, N, OV, Z
	CP	Wb,#lit5	Compare Wb with lit5	1	1	C, DC, N, OV, Z
	CP	Wb,Ws	Compare Wb with Ws (Wb – Ws)	1	1	C, DC, N, OV, Z
CP0	CP0	f	Compare f with 0x0000	1	1	C, DC, N, OV, Z
	CP0	Ws	Compare Ws with 0x0000	1	1	C, DC, N, OV, Z
CPB	CPB	f	Compare f with WREG, with Borrow	1	1	C, DC, N, OV, Z
	CPB	Wb,#lit5	Compare Wb with lit5, with Borrow	1	1	C, DC, N, OV, Z
	CPB	Wb,Ws	Compare Wb with Ws, with Borrow (Wb – Ws – $\overline{C}$)	1	1	C, DC, N, OV, Z
CPSEQ	CPSEQ	Wb,Wn	Compare Wb with Wn, Skip if =	1	1 (2 or 3)	None
CPSGT	CPSGT	Wb,Wn	Compare Wb with Wn, Skip if >	1	1 (2 or 3)	None
CPSLT	CPSLT	Wb,Wn	Compare Wb with Wn, Skip if <	1	1 (2 or 3)	None

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Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
CPSNE	CPSNE	Wb,Wn	Compare Wb with Wn, Skip if ≠	1	1 (2 or 3)	None
DAW	DAW.B	Wn	Wn = Decimal Adjust Wn	1	1	C
DEC	DEC	f	f = f – 1	1	1	C, DC, N, OV, Z
	DEC	f,WREG	WREG = f – 1	1	1	C, DC, N, OV, Z
	DEC	Ws,Wd	Wd = Ws – 1	1	1	C, DC, N, OV, Z
DEC2	DEC2	f	f = f – 2	1	1	C, DC, N, OV, Z
	DEC2	f,WREG	WREG = f – 2	1	1	C, DC, N, OV, Z
	DEC2	Ws,Wd	Wd = Ws – 2	1	1	C, DC, N, OV, Z
DISI	DISI	#lit14	Disable Interrupts for k Instruction Cycles	1	1	None
DIV	DIV.SW	Wm,Wn	Signed 16/16-bit Integer Divide	1	18	N, Z, C, OV
	DIV.SD	Wm,Wn	Signed 32/16-bit Integer Divide	1	18	N, Z, C, OV
	DIV.UW	Wm,Wn	Unsigned 16/16-bit Integer Divide	1	18	N, Z, C, OV
	DIV.UD	Wm,Wn	Unsigned 32/16-bit Integer Divide	1	18	N, Z, C, OV
EXCH	EXCH	Wns,Wnd	Swap Wns with Wnd	1	1	None
FF1L	FF1L	Ws,Wnd	Find First One from Left (MSb) Side	1	1	C
FF1R	FF1R	Ws,Wnd	Find First One from Right (LSb) Side	1	1	C
GOTO	GOTO	Expr	Go to Address	2	2	None
	GOTO	Wn	Go to Indirect	1	2	None
INC	INC	f	f = f + 1	1	1	C, DC, N, OV, Z
	INC	f,WREG	WREG = f + 1	1	1	C, DC, N, OV, Z
	INC	Ws,Wd	Wd = Ws + 1	1	1	C, DC, N, OV, Z
INC2	INC2	f	f = f + 2	1	1	C, DC, N, OV, Z
	INC2	f,WREG	WREG = f + 2	1	1	C, DC, N, OV, Z
	INC2	Ws,Wd	Wd = Ws + 2	1	1	C, DC, N, OV, Z
IOR	IOR	f	f = f .IOR. WREG	1	1	N, Z
	IOR	f,WREG	WREG = f .IOR. WREG	1	1	N, Z
	IOR	#lit10,Wn	Wd = lit10 .IOR. Wd	1	1	N, Z
	IOR	Wb,Ws,Wd	Wd = Wb .IOR. Ws	1	1	N, Z
	IOR	Wb,#lit5,Wd	Wd = Wb .IOR. lit5	1	1	N, Z

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Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
LNK	LNK	#lit14	Link Frame Pointer	1	1	None
LSR	LSR	f	f = Logical Right Shift f	1	1	C, N, OV, Z
	LSR	f,WREG	WREG = Logical Right Shift f	1	1	C, N, OV, Z
	LSR	Ws,Wd	Wd = Logical Right Shift Ws	1	1	C, N, OV, Z
	LSR	Wb,Wns,Wnd	Wnd = Logical Right Shift Wb by Wns	1	1	N, Z
	LSR	Wb,#lit5,Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N, Z
MOV	MOV	f,Wn	Move f to Wn	1	1	None
	MOV	[Wns +Slit10],Wnd	Move [Wns + Slit10] to Wnd	1	1	None
	MOV	f	Move f to f	1	1	N, Z
	MOV	f,WREG	Move f to WREG	1	1	N, Z
	MOV	#lit16,Wn	Move 16-Bit Literal to Wn	1	1	None
	MOV.b	#lit8,Wn	Move 8-Bit Literal to Wn	1	1	None
	MOV	Wn,f	Move Wn to f	1	1	None
	MOV	Wns,[Wns +Slit10]	Move Wns to [Wns + Slit10]	1	1	None
	MOV	Wso,Wdo	Move Ws to Wd	1	1	None
	MOV	WREG,f	Move WREG to f	1	1	N, Z
	MOV.D	Wns,Wd	Move Double from W(ns):W(ns + 1) to Wd	1	2	None
	MOV.D	Ws,Wnd	Move Double from Ws to W(nd + 1):W(nd)	1	2	None
MUL	MUL.SS	Wb,Ws,Wnd	{Wnd + 1, Wnd} = Signed(Wb) * Signed(Ws)	1	1	None
	MUL.SU	Wb,Ws,Wnd	{Wnd + 1, Wnd} = Signed(Wb) * Unsigned(Ws)	1	1	None
	MUL.US	Wb,Ws,Wnd	{Wnd + 1, Wnd} = Unsigned(Wb) * Signed(Ws)	1	1	None
	MUL.UU	Wb,Ws,Wnd	{Wnd + 1, Wnd} = Unsigned(Wb) * Unsigned(Ws)	1	1	None
	MUL.SU	Wb,#lit5,Wnd	{Wnd + 1, Wnd} = Signed(Wb) * Unsigned(lit5)	1	1	None
	MUL.UU	Wb,#lit5,Wnd	{Wnd + 1, Wnd} = Unsigned(Wb) * Unsigned(lit5)	1	1	None
	MUL	f	W3:W2 = f * WREG	1	1	None

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Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
NEG	NEG	f	f = $\bar{f}$ + 1	1	1	C, DC, N, OV, Z
	NEG	f,WREG	WREG = $\bar{f}$ + 1	1	1	C, DC, N, OV, Z
	NEG	Ws,Wd	Wd = $\overline{Ws}$ + 1	1	1	C, DC, N, OV, Z
NOP	NOP		No Operation	1	1	None
	NOPR		No Operation	1	1	None
POP	POP	f	Pop f from Top-of-Stack (TOS)	1	1	None
	POP	Wdo	Pop from Top-of-Stack (TOS) to Wdo	1	1	None
	POP.D	Wnd	Pop from Top-of-Stack (TOS) to W(nd):W(nd + 1)	1	2	None
	POP.S		Pop Shadow Registers	1	1	All
PUSH	PUSH	f	Push f to Top-of-Stack (TOS)	1	1	None
	PUSH	Wso	Push Wso to Top-of-Stack (TOS)	1	1	None
	PUSH.D	Wns	Push W(ns):W(ns + 1) to Top-of-Stack (TOS)	1	2	None
	PUSH.S		Push Shadow Registers	1	1	None
PWRSAV	PWRSAV	#lit1	Go into Sleep or Idle mode	1	1	WDTO, Sleep
RCALL	RCALL	Expr	Relative Call	1	2	None
	RCALL	Wn	Computed Call	1	2	None
REPEAT	REPEAT	#lit14	Repeat Next Instruction lit14 + 1 times	1	1	None
	REPEAT	Wn	Repeat Next Instruction (Wn) + 1 times	1	1	None
RESET	RESET		Software Device Reset	1	1	None
RETFIE	RETFIE		Return from Interrupt	1	3 (2)	None
RETLW	RETLW	#lit10,Wn	Return with Literal in Wn	1	3 (2)	None
RETURN	RETURN		Return from Subroutine	1	3 (2)	None
RLC	RLC	f	f = Rotate Left through Carry f	1	1	C, N, Z
	RLC	f,WREG	WREG = Rotate Left through Carry f	1	1	C, N, Z
	RLC	Ws,Wd	Wd = Rotate Left through Carry Ws	1	1	C, N, Z

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Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
RLNC	RLNC	f	f = Rotate Left (No Carry) f	1	1	N, Z
	RLNC	f,WREG	WREG = Rotate Left (No Carry) f	1	1	N, Z
	RLNC	Ws,Wd	Wd = Rotate Left (No Carry) Ws	1	1	N, Z
RRC	RRC	f	f = Rotate Right through Carry f	1	1	C, N, Z
	RRC	f,WREG	WREG = Rotate Right through Carry f	1	1	C, N, Z
	RRC	Ws,Wd	Wd = Rotate Right through Carry Ws	1	1	C, N, Z
RRNC	RRNC	f	f = Rotate Right (No Carry) f	1	1	N, Z
	RRNC	f,WREG	WREG = Rotate Right (No Carry) f	1	1	N, Z
	RRNC	Ws,Wd	Wd = Rotate Right (No Carry) Ws	1	1	N, Z
SE	SE	Ws,Wnd	Wnd = Sign-Extended Ws	1	1	C, N, Z
SETM	SETM	f	f = FFFFh	1	1	None
	SETM	WREG	WREG = FFFFh	1	1	None
	SETM	Ws	Ws = FFFFh	1	1	None
SL	SL	f	f = Left Shift f	1	1	C, N, OV, Z
	SL	f,WREG	WREG = Left Shift f	1	1	C, N, OV, Z
	SL	Ws,Wd	Wd = Left Shift Ws	1	1	C, N, OV, Z
	SL	Wb,Wns,Wnd	Wnd = Left Shift Wb by Wns	1	1	N, Z
	SL	Wb,#lit5,Wnd	Wnd = Left Shift Wb by lit5	1	1	N, Z
SUB	SUB	f	f = f – WREG	1	1	C, DC, N, OV, Z
	SUB	f,WREG	WREG = f – WREG	1	1	C, DC, N, OV, Z
	SUB	#lit10,Wn	Wn = Wn – lit10	1	1	C, DC, N, OV, Z
	SUB	Wb,Ws,Wd	Wd = Wb – Ws	1	1	C, DC, N, OV, Z
	SUB	Wb,#lit5,Wd	Wd = Wb – lit5	1	1	C, DC, N, OV, Z
SUBB	SUBB	f	f = f – WREG – ($\overline{C}$)	1	1	C, DC, N, OV, Z
	SUBB	f,WREG	WREG = f – WREG – ($\overline{C}$)	1	1	C, DC, N, OV, Z
	SUBB	#lit10,Wn	Wn = Wn – lit10 – ($\overline{C}$)	1	1	C, DC, N, OV, Z
	SUBB	Wb,Ws,Wd	Wd = Wb – Ws – ($\overline{C}$)	1	1	C, DC, N, OV, Z
	SUBB	Wb,#lit5,Wd	Wd = Wb – lit5 – ($\overline{C}$)	1	1	C, DC, N, OV, Z

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Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
SUBR	SUBR	f	f = WREG – f	1	1	C, DC, N, OV, Z
	SUBR	f,WREG	WREG = WREG – f	1	1	C, DC, N, OV, Z
	SUBR	Wb,Ws,Wd	Wd = Ws – Wb	1	1	C, DC, N, OV, Z
	SUBR	Wb,#lit5,Wd	Wd = lit5 – Wb	1	1	C, DC, N, OV, Z
SUBBR	SUBBR	f	f = WREG – f – ($\overline{C}$)	1	1	C, DC, N, OV, Z
	SUBBR	f,WREG	WREG = WREG – f – ($\overline{C}$)	1	1	C, DC, N, OV, Z
	SUBBR	Wb,Ws,Wd	Wd = Ws – Wb – ($\overline{C}$)	1	1	C, DC, N, OV, Z
	SUBBR	Wb,#lit5,Wd	Wd = lit5 – Wb – ($\overline{C}$)	1	1	C, DC, N, OV, Z
SWAP	SWAP.b	Wn	Wn = Nibble Swap Wn	1	1	None
	SWAP	Wn	Wn = Byte Swap Wn	1	1	None
TBLRDH	TBLRDH	Ws,Wd	Read Prog[23:16] to Wd[7:0]	1	2	None
TBLRDL	TBLRDL	Ws,Wd	Read Prog[15:0] to Wd	1	2	None
TBLWTH	TBLWTH	Ws,Wd	Write Ws[7:0] to Prog[23:16]	1	2	None
TBLWTL	TBLWTL	Ws,Wd	Write Ws to Prog[15:0]	1	2	None
ULNK	ULNK		Unlink Frame Pointer	1	1	None
XOR	XOR	f	f = f .XOR. WREG	1	1	N, Z
	XOR	f,WREG	WREG = f .XOR. WREG	1	1	N, Z
	XOR	#lit10,Wn	Wd = lit10 .XOR. Wd	1	1	N, Z
	XOR	Wb,Ws,Wd	Wd = Wb .XOR. Ws	1	1	N, Z
	XOR	Wb,#lit5,Wd	Wd = Wb .XOR. lit5	1	1	N, Z
ZE	ZE	Ws,Wnd	Wnd = Zero-Extend Ws	1	1	C, Z, N

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30. Electrical Characteristics

This section provides an overview of the PIC24FJ64GP205/GU205 family electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC24FJ64GP205/GU205 family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these, or any other conditions above the parameters indicated in the operation listings of this specification, is not implied.

30.1 Absolute Maximum Ratings(1)

Parameter	Rating
Ambient temperature under bias	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on V_{DD} with respect to V_{SS}	-0.3V to +4.0V
Voltage on any general purpose digital/analog pin (not 5.5V tolerant) with respect to V_{SS}	-0.3V to (V_{DD} + 0.3V)
Voltage on any general purpose digital/ analog pin (5.5V tolerant, including $\overline{MCLR}$) with respect to V_{SS}:	
When V_{DD} = 0V:	-0.3V to +4.0V
When V_{DD} ≥ 2.0V:	-0.3V to +6.0V
Voltage on AV_{DD} with respect to V_{SS}	(V_{DD} – 0.3V) to (lesser of: 4.0V or (V_{DD} + 0.3V))
Voltage on AV_{SS} with respect to V_{SS}	-0.3V to +0.3V
Maximum current out of V_{SS} pin	300 mA
Maximum current into V_{DD} pin(2)	250 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by all ports	200 mA
Maximum current sourced by all ports(2)	200 mA

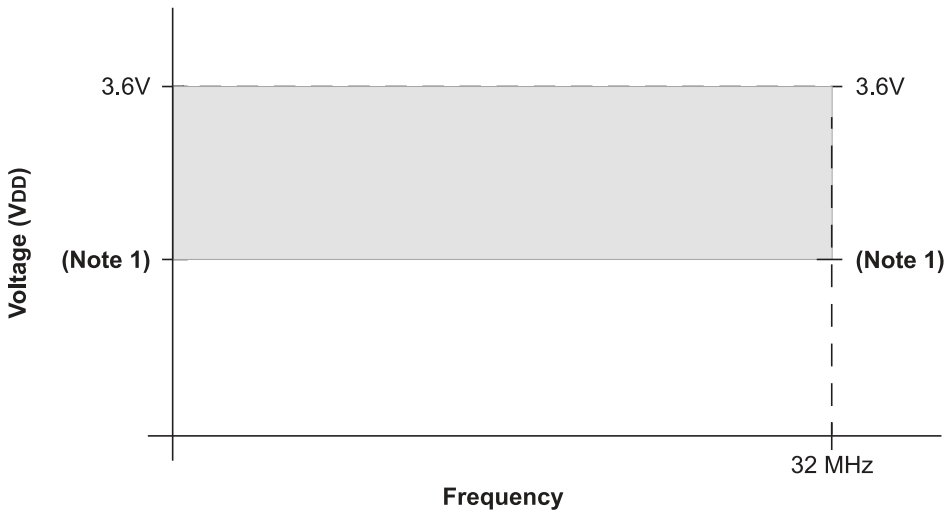
Notes:

1. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those, or any other conditions above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Maximum allowable current is a function of device maximum power dissipation (see Table 30-1).

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30.2 DC Characteristics

Figure 30-1. PIC24FJ64GP205/GU205 Family Voltage-Frequency Graph (Industrial)



Note:

1. Lower operating boundary is 2.0V or V_{BOR} (when BOR is enabled), whichever is lower. For best analog performance, operate above 2.2V.

Table 30-1. Thermal Operating Conditions

Rating	Symbol	Min	Typ	Max	Unit
PIC24FJ128GU410:					
Operating Junction Temperature Range	T_J	-40	—	+135	°C
Operating Ambient Temperature Range	T_A	-40	—	+125	°C
Power Dissipation: Internal Chip Power Dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \Sigma I_{OH})$	P_D	$P_{INT} + P_{I/O}$			W
I/O Pin Power Dissipation: $P_{I/O} = \Sigma (\{V_{DD} - V_{OH}\} \times I_{OH}) + \Sigma (V_{OL} \times I_{OL})$					
Maximum Allowed Power Dissipation	P_{DMAX}	$(T_J - T_A)/\Theta_{JA}$			W

Table 30-2. Package Thermal Resistance

Characteristic(1)	Symbol	Typ	Unit
28-Pin QFN	θ_{JA}	38.4	°C/W
28-Pin UQFN	θ_{JA}	38.7	°C/W
28-Pin SOIC	θ_{JA}	79.0	°C/W
28-Pin SSOP	θ_{JA}	67.1	°C/W
36-Pin UQFN	θ_{JA}	35.4	°C/W
48-Pin UQFN	θ_{JA}	28.3	°C/W
48-Pin TQFP	θ_{JA}	71.0	°C/W

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Note:

1. Junction to ambient thermal resistance; Theta-$_{JA}$ (θ_{JA}) numbers are achieved by package simulations.

Table 30-3. Temperature and Voltage Specifications

Operating Conditions (unless otherwise stated): 2.0V ≤ V_{DD} ≤ 3.6V -40° ≤ T_A ≤ +85°C						
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**
DC10	V_{DD}	Supply Voltage	2.0	—	3.6	V
DC16	V_{POR}(1)	V_{DD} Start Voltage to Ensure Internal Power-on Reset Signal	V_{SS}	—	—	V
DC17A	SV_{DD}(1,3)	Recommended V_{DD} Rise Rate to Ensure Internal Power-on Reset Signal	1V/20 ms	—	1V/10 µS	sec
DC17B	V_{BOR}(2)	Brown-out Reset Voltage on V_{DD} Transition, High-to-Low	2.0	2.1	2.2	V

Notes:

1. If the V_{POR} or SV_{DD} parameters are not met, or the application experiences slow power-down V_{DD} ramp rates, it is recommended to enable and use BOR.
2. On a rising V_{DD} power-up sequence, application firmware execution begins at the higher of the V_{PORREL} or V_{BOR} level (when BOREN = 1).
3. V_{DD} rise times outside this window may not internally reset the processor and are not parametrically tested.

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Table 30-4. Operating Current (I_{DD})

Operating Conditions (unless otherwise stated): -40° ≤ T_A ≤ +125°C					
Param No.	**Typ**	**Max**	**Units**	**V_{DD}**	**Conditions(2)**
DC19	187	340	µA	2.0V	0.5 MIPS, F_{OSC} = 1 MHz
	196	340	µA	3.3V	
DC20	339	530	µA	2.0V	1 MIPS, F_{OSC} = 2 MHz
	351	530	µA	3.3V	
DC23	1.23	1.58	mA	2.0V	4 MIPS, F_{OSC} = 8 MHz
	1.25	1.58	mA	3.3V	
DC24	5.78	6.2	mA	2.0V	16 MIPS, F_{OSC} = 32 MHz
	5.86	6.2	mA	3.3V	
DC31	45	200	µA	2.0V	LPRC (16 KIPS), F_{OSC} = 32 kHz
	51	200	µA	3.3V	
DC32	1.25	1.64	mA	2.0V	FRC (4 MIPS), F_{OSC} = 8 MHz
	1.26	1.64	mA	3.3V	

Notes:

1. Data in the “Typ” column are at +25°C. Typical parameters are for design guidance only and are not tested.
2. Base I_{DD} current is measured with:
   - Oscillator is configured in EC mode without PLL (FNOSC[2:0] (FOSCSEL[2:0]) = 010, PLLMODE[3:0] (FOSCSEL[6:3]) = 1111 and POSCMOD[1:0] (FOSC[1:0]) = 00)
   - OSCI pin is driven with external square wave with levels from 0.3V to V_{DD} – 0.3V
   - OSCO is configured as an I/O in the Configuration Words (OSCIOFCN (FOSC[2]) = 0)
   - FSCM is disabled (FCKSM[1:0] (FOSC[7:6]) = 11)
   - Secondary Oscillator circuit is disabled (SOSCSEL (FOSC[3]) = 0)
   - Main and low-power BOR circuits are disabled (BOREN[1:0] (FPOR[1:0]) = 00 and LPBOREN (FPOR[3]) = 0)
   - Watchdog Timer is disabled (FWDTEN[1:0] (FWDT[6:5]) = 00)
   - All I/O pins (except OSCI) are configured as outputs and driving low
   - No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
   - JTAG is disabled ($\overline{\text{JTAGEN}}$ (FICD[5]) = 0)
   - NOP instructions are executed

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Table 30-5. Idle Current (I_{IDLE})

Operating Conditions (unless otherwise stated): -40° ≤ T_A ≤ +125°C					
Param No.	**Typ**	**Max**	**Units**	**V_{DD}**	**Conditions(2)**
DC40	111	270	µA	2.0V	1 MIPS, F_{OSC} = 2 MHz
	122	270	µA	3.3V	
DC43	329	520	µA	2.0V	4 MIPS, F_{OSC} = 8 MHz
	356	520	µA	3.3V	
DC47	1.17	1.8	mA	2.0V	16 MIPS, F_{OSC} = 32 MHz
	1.26	1.8	mA	3.3V	
DC50	370	570	µA	2.0V	FRC (4 MIPS), F_{OSC} = 8 MHz
	380	570	µA	3.0V	
DC51	41	290	µA	2.0V	LPRC (16 KIPS), F_{OSC} = 32 kHz
	47	290	µA	3.3V	

Notes:

1. Data in the “Typ” column are at +25°C. Parameters are for design guidance only and are not tested.
2. Base I_{IDLE} current is measured with:
   - Oscillator is configured in EC mode without PLL (FNOSC[2:0] (FOSCSEL[2:0]) = 010, PLLMODE[3:0] (FOSCSEL[6:3]) = 1111 and POSCMOD[1:0] (FOSC[1:0]) = 00)
   - OSCI pin is driven with external square wave with levels from 0.3V to V_{DD} – 0.3V
   - OSCO is configured as an I/O in Configuration Words (OSCIOFCN (FOSC[2]) = 0)
   - FSCM is disabled (FCKSM[1:0] (FOSC[7:6]) = 11)
   - Secondary Oscillator circuit is disabled (SOSCSEL (FOSC[3]) = 0)
   - Main and low-power BOR circuits are disabled (BOREN[1:0] (FPOR[1:0]) = 00 and LPBOREN (FPOR[3]) = 0)
   - Watchdog Timer is disabled (FWDTEN[1:0] (FWDT[6:5]) = 00)
   - All I/O pins (except OSCI) are configured as outputs and driving low
   - No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
   - JTAG is disabled ($\overline{\text{JTAGEN}}$ (FICD[5]) = 0)
   - `pwrsav #1 (IDLE)` instruction is executed

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Table 30-6. Power-Down Current (I_{PD})

Param No.	Typ	Max	Units	Operating Temperature	V_{DD}	Conditions(2)
DC60	1.98	10	µA	-40°C	2.0V	Sleep with main voltage regulator in Standby mode (VREGS (RCON[8]) = 0, RETEN (RCON[12]) = 0, LPREGEN (FPOR[2]) = 1)
	3.1	12	µA	+25°C		
	4	18	µA	+85°C		
	8.31	150	µA	+125°C		
	4.3	10	µA	-40°C	3.3V	
	5.1	12	µA	+25°C		
	6.15	18	µA	+85°C		
	11.22	150	µA	+125°C		
DC61	0.17	—	µA	-40°C	2.0V	Sleep with enabled low-voltage retention regulator (VREGS (RCON[8]) = 0, RETEN (RCON[12]) = 1, LPREGEN (FPOR[2]) = 0)
	0.51	—	µA	+25°C		
	0.80	—	µA	+85°C		
	4.79	—	µA	+125°C		
	0.33	—	µA	-40°C	3.3V	
	0.7	—	µA	+25°C		
	1.09	—	µA	+85°C		
	5.77	—	µA	+125°C		

Notes:

1. Data in the “Typ” column are at +25°C. Parameters are for design guidance only and are not tested.
2. Base I_{PD} current is measured with:
   - Oscillator is configured in FRC mode without PLL (FNOSC[2:0] (FOSCSEL[2:0]) = 000, PLLMODE[3:0] (FOSCSEL[6:3]) = 1111 and POSCMOD[1:0] (FOSC[1:0]) = 11)
   - OSCO is configured as an I/O in Configuration Words (OSCIOFCN (FOSC[2]) = 0)
   - FSCM is disabled (FCKSM[1:0] (FOSC[7:6]) = 11)
   - Secondary Oscillator circuit is disabled (SOSCSEL (FOSC[3]) = 0)
   - Main and low-power BOR circuits are disabled (BOREN[1:0] (FPOR[1:0]) = 00 and LPBOREN (FPOR[3]) = 0)
   - Watchdog Timer is disabled (FWDTEN[1:0] (FWDT[6:5]) = 00)
   - All I/O pins are configured as outputs and driving low
   - No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
   - JTAG is disabled ($\overline{\text{JTAGEN}}$ (FICD[5]) = 0)
   - The currents are measured on the device containing the most memory in this family
   - `pwrsav #0 (SLEEP)` instruction is executed.

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Table 30-7. Incremental Peripheral Δ Current

Operating Conditions (unless otherwise stated): -40°C ≤ T_A ≤ +125°C						
Param No.	**Typ**	**Max**	**Units**	**Operating Temperature**	**V_{DD}**	**Conditions**
Incremental Current Brown-out Reset (ΔBOR)(2)						
DC25	2.22	5	µA	-40°C to +85°C	2.0V	ΔBOR
	2.80	5	µA	-40°C to +85°C	3.3V	
	2.23	10	µA	-40°C to +125°C	2.0V	
	2.81	10	µA	-40°C to +125°C	3.3V	
Incremental Current Watchdog Timer (ΔWDT)(2)						
DC71	0.35	1	µA	-40°C to +85°C	2.0V	ΔWDT
	0.38	1	µA	-40°C to +85°C	3.3V	
	0.61	5	µA	-40°C to +125°C	2.0V	
	0.63	5	µA	-40°C to +125°C	3.3V	
Incremental Current High/Low-Voltage Detect (ΔHLVD)(2)						
DC75	1.93	5	µA	-40°C to +85°C	2.0V	ΔHLVD
	2.58	5	µA	-40°C to +85°C	3.3V	
	2.10	10	µA	-40°C to +125°C	2.0V	
	2.82	10	µA	-40°C to +125°C	3.3V	
Incremental Current Analog-to-Digital Converter (ΔADC)(2)						
	363.1	700	µA	-40°C to +85°C	2.0V	ΔADC (with internal RC Clock)
	429.6	700	µA	-40°C to +85°C	3.3V	
	381.3	750	µA	-40°C to +125°C	2.0V	
	451.6	750	µA	-40°C to +125°C	3.3V	
Incremental Current Deadman Timer (ΔDMT)(2)						
	212.9	1000	nA	-40°C to +85°C	2.0V	ΔDMT(2)
	215.4	1000	nA	-40°C to +85°C	3.3V	
	668	1500	nA	-40°C to +125°C	2.0V	
	636.5	1500	nA	-40°C to +125°C	3.3V	
Incremental Current Real-Time Clock and Calendar (ΔRTCC)(2)						
DC77	0.63	—	µA	-40°C to +85°C	2.0V	With SOSC enabled in Low-Power mode
	0.83	—	µA	-40°C to +85°C	3.3V	
	0.85	—	µA	-40°C to +125°C	2.0V	
	1	—	µA	-40°C to +125°C	3.3V	

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Operating Conditions (unless otherwise stated): -40°C ≤ T_A ≤ +125°C						
Param No.	**Typ**	**Max**	**Units**	**Operating Temperature**	**V_{DD}**	**Conditions**
DC77A	381.6	1000	nA	-40°C to +85°C	2.0V	With LPRC enabled
	407.1	1000	nA	-40°C to +85°C	3.3V	
	392.8	1300	nA	-40°C to +125°C	2.0V	
	473.3	1300	nA	-40°C to +125°C	3.3V	
Incremental Current PLL Enable (Δ PLLEN)(2)						
	662.4	—	µA	-40°C to +85°C	2.0V	PLL Enabled
	662.5	—	µA	-40°C to +85°C	3.3V	CLKDIV[PLLEN] = 1
	676.7	—	µA	-40°C to +125°C	2.0V	
	677.2	—	µA	-40°C to +125°C	3.3V	

Notes:

1. Data in the “Typ” column are at +25°C. Parameters are for design guidance only and are not tested.
2. Incremental current while the module is enabled and running. This current should be added to the base I_{PD} current.

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Table 30-8. I/O Pin Input Specifications

Operating Conditions (unless otherwise stated): 2.0V < V_{DD} < 3.6V -40°C < T_A < +85°C						
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
	V_{IL}	Input Low Voltage(2)				
DI10		I/O Pins with ST Buffer	V_{SS}	0.2 V_{DD}	V	
DI11		I/O Pins with TTL Buffer	V_{SS}	0.15 V_{DD}	V	
DI15		$\overline{MCLR}$	V_{SS}	0.2 V_{DD}	V	
DI16		OSCI (XT mode)	V_{SS}	0.2 V_{DD}	V	
DI17		OSCI (HS mode)	V_{SS}	0.2 V_{DD}	V	
DI18		I/O Pins with I^2C Buffer	V_{SS}	0.3 V_{DD}	V	
DI19		I/O Pins with SMBus Buffer	—	0.8	V	SMBus is enabled
	V_{IH}	Input High Voltage(3)				
DI20		I/O Pins with ST Buffer: with Analog Functions, Digital Only	0.8 V_{DD} 0.8 V_{DD}	V_{DD} 5.5	V V	
DI21		I/O Pins with TTL Buffer: with Analog Functions, Digital Only	0.25 V_{DD} + 0.8 0.25 V_{DD} + 0.8	V_{DD} 5.5	V V	
DI25		$\overline{MCLR}$	0.8 V_{DD}	V_{DD}	V	
DI26		OSCI (XT mode)	0.7 V_{DD}	V_{DD}	V	
DI27		OSCI (HS mode)	0.7 V_{DD}	V_{DD}	V	
DI28		I/O Pins with I^2C Buffer: with Analog Functions, Digital Only	0.7 V_{DD} 0.7 V_{DD}	V_{DD} 5.5	V V	
DI29		I/O Pins with SMBus Buffer: with Analog Functions, Digital Only	1.35	—	V	2.5V ≤ V_{PIN} ≤ V_{DD}
DI30	I_{CNPU}	**CNx Pull-up Current**	100	450	µA	V_{DD} = 3.3V, V_{PIN} = V_{SS}
DI30A	I_{CNPD}	**CNx Pull-Down Current**	150	550	µA	V_{DD} = 3.3V, V_{PIN} = V_{DD}

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Operating Conditions (unless otherwise stated): 2.0V < V_{DD} < 3.6V -40°C < T_A < +85°C						
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
	I_{IL}	**Input Leakage Current(1)**				
DI50		I/O Ports	—	±1	µA	$V_{SS} \le V_{PIN} \le V_{DD}$, pin at high-impedance
DI51		Analog Input Pins	—	±1	µA	$V_{SS} \le V_{PIN} \le V_{DD}$, pin at high-impedance
DI55		$\overline{MCLR}$	—	±1	µA	$V_{SS} \le V_{PIN} \le V_{DD}$
DI56		OSCI/CLKI	—	±1	µA	$V_{SS} \le V_{PIN} \le V_{DD}$, EC, XT and HS modes

Notes:

1. Negative current is defined as current sourced by the pin.
2. Refer to Table 1-1 for I/O pin buffer types.

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Table 30-9. I/O Pin Output Specifications

Operating Conditions (unless otherwise stated): -40°C < T_A < +85°C						
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
	V_{OL}	**Output Low Voltage**				
DO10		I/O Ports	—	0.4	V	I_{OL} = 3 mA, V_{DD} = 3.6V
			—	0.8	V	I_{OL} = 6 mA, V_{DD} = 3.6V
DO16		OSCO/CLKO	—	0.18	V	I_{OL} = 3 mA, V_{DD} = 3.6V
			—	0.2	V	I_{OL} = 6 mA, V_{DD} = 3.6V
	V_{OH}	**Output High Voltage**				
DO20		I/O Ports	3.4	—	V	I_{OL} = -3.0 mA, V_{DD} = 3.6V
			3.25	—	V	I_{OL} = -6.0 mA, V_{DD} = 3.6V
DO26		OSCO/CLKO	3.3	—	V	I_{OL} = -3 mA, V_{DD} = 3.6V
			1.85	—	V	I_{OL} = -6 mA, V_{DD} = 3.6V

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Table 30-10. Program Memory

Operating Conditions (unless otherwise stated): 2.0V < V_{DD} < 3.6V -40°C < T_A < +85°C					
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**
		Program Flash Memory			
D130	E_P	Cell Endurance	10000	—	E/W
D133A	T_{IW}	Self-Timed Double-Word Write Cycle Time	—	30	µs
		Self-Timed Row Write Cycle Time	—	2	ms
D133B	T_{IE}	Self-Timed Page Erase Time	—	40	ms
D134	T_{RETD}	Characteristic Retention	20	—	Year

Table 30-11. Internal Voltage Regulator Specifications

Operating Conditions (unless otherwise stated): -40°C< T_A < +85°C							
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
DVR	T_{VREG}	Voltage Regulator Start-up Time	—	10	—	µs	VREGS = 0 with any POR or BOR
DVR10	V_{BG}	Internal Band Gap Reference	1.14	1.2	1.26	V	
DVR11	T_{BG}	Band Gap Reference Start-up Time	—	1	—	ms	
DVR20	V_{RGOUT}	Regulator Output Voltage	—	1.8	—	V	V_{DD} > 1.9V
DVR21	C_{EFC}	External Filter Capacitor Value	10	—	—	µF	Series resistance < 3Ω recommended; < 5Ω required
DVR30	V_{LVR}	Low-Voltage Regulator Output Voltage	0.9	—	1.2	V	RETEN = 1, $\overline{\text{LPREGEN}}$ = 0

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Table 30-12. High/Low-Voltage Detect Characteristics

Operating Conditions (unless otherwise stated): -40°C < T_A < +85°C							
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ**	**Max**	**Units**
DC18	V_{HLVD}	HLVD Voltage on V_{DD} Transition	HLVDL[3:0] = 0110	2.93	—	3.39	V
			HLVDL[3:0] = 0111	2.73	—	3.17	V
			HLVDL[3:0] = 1000	2.62	—	3.06	V
			HLVDL[3:0] = 1001	2.39	—	2.8	V
			HLVDL[3:0] = 1010	2.29	—	2.68	V
			HLVDL[3:0] = 1011	2.18	—	2.56	V
			HLVDL[3:0] = 1100	2.08	—	2.45	V
			HLVDL[3:0] = 1101	1.98	—	2.34	V
			HLVDL[3:0] = 1110	1.88	—	2.23	V
DC101	V_{THL}	HLVD Voltage on LVDIN Pin Transition	HLVDL[3:0] = 1111	—	1.2	—	V
DC105	T_{ONLVD}	HLVD Module Enable Time		—	5	—	µs

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Table 30-13. Comparator DC Specifications

Operating Conditions (unless otherwise stated): 2.0V < V_{DD} < 3.6V -40°C < T_A < +85°C						
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ**	**Max**	**Units**
D300	V_{IOFF}	Input Offset Voltage	—	12	50	mV
D301	V_{ICM}	Input Common-Mode Voltage	0	—	V_{DD}	V
D302	CMRR	Common-Mode Rejection Ratio	55	—	—	dB
D306	I_{QCMP}	AV_{DD} Quiescent Current per Comparator	—	27	—	µA
D307	T_{RESP}	Response Time(2)	—	300	—	ns
D308	T_{MC2OV}	Comparator Mode Change to Valid Output	—	—	10	µs
D309	I_{DD}	Operating Supply Current	—	30	—	µA

Notes:

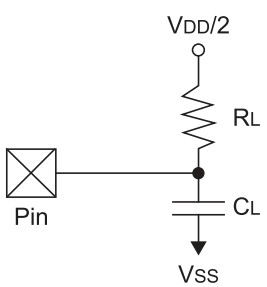
1. Parameters are characterized but not tested.
2. Measured with one input at $V_{DD}/2$ and the other transitioning from V_{SS} to V_{DD}, 40 mV step, 15 mV overdrive.

Table 30-14. Comparator Voltage Reference DC Specifications

Operating Conditions (unless otherwise stated): 2.0V < V_{DD} < 3.6V -40°C < T_A < +85°C					
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**
VR310	T_{SET}	Settling Time	—	10	µs
VRD311	CV_{RAA}	Absolute Accuracy	-100	+100	mV

30.3 AC Characteristics and Timing Parameters

Figure 30-2. Load Conditions for I/O Specifications



R_L = 464Ω
C_L = 50 pF

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Figure 30-3. CLKO and I/O Timing Characteristics

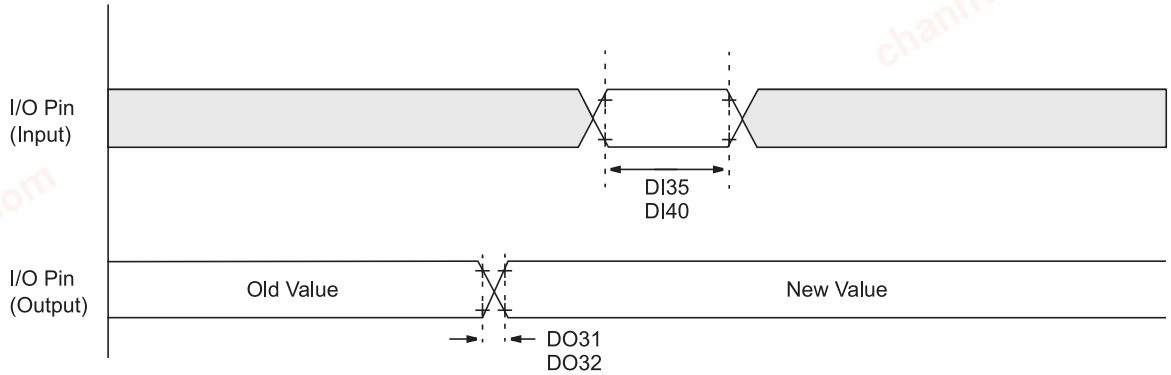
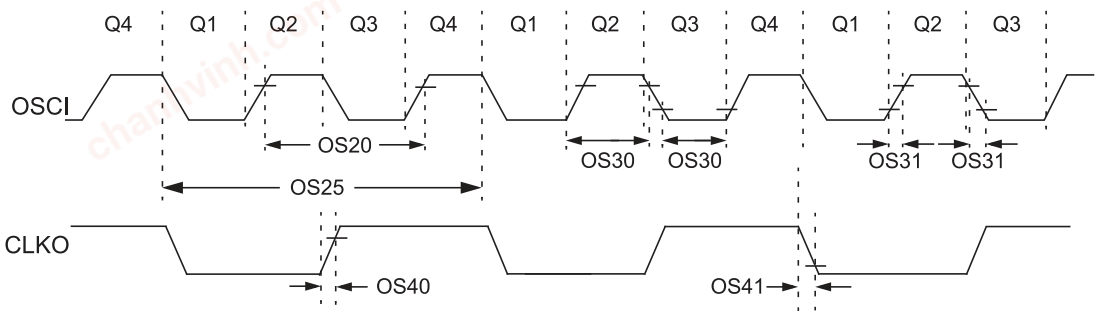


Table 30-15. I/O Timing Requirements

Operating Conditions 2.0V to 3.6V (unless otherwise stated): 2.0V < V_{DD} < 3.6V -40°C < T_A < +85°C					
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**
DO31	$T_{IO}R$	Port Output Rise Time	—	25	ns
DO32	$T_{IO}F$	Port Output Fall Time	—	25	ns
DI35	T_{INP}	INTx Pin High or Low Time (input)	1	—	T_{CY}
DI40	T_{RBP}	CNx High or Low Time (input)	1	—	T_{CY}

Figure 30-4. External Clock Timing



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Table 30-16. External Clock Timing Requirements

Operating Conditions (unless otherwise stated): 2.0V < V_{DD} < 3.6V -40°C < T_A < +85°C							
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
OS10	F_{OSC}	External CLKI Frequency (External clocks allowed only in EC mode)(2)	— 4	— —	32 48	MHz MHz	EC
		Oscillator Frequency	3.5 4 10 12 31	— — — — —	10 8 32 24 33	MHz MHz MHz MHz kHz	XT XTPLL HS HSPLL SOSC
OS25	T_{CY}	Instruction Cycle Time(3)	62.5	—	DC	ns	
OS30	$T_{OS}L$, $T_{OS}H$	External Clock in (OSCI) High or Low Time	0.45 x T_{OSC}	—	—	ns	EC
OS31	$T_{OS}R$, $T_{OS}F$	External Clock in (OSCI) Rise or Fall Time	—	—	20	ns	EC
OS40	$T_{CK}R$	CLKO Rise Time(4)	—	15	30	ns	
OS41	$T_{CK}F$	CLKO Fall Time(4)	—	15	30	ns	

Notes:

1. Data in the “Typ” column are at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
2. Represents input to the system clock prescaler. PLL dividers and postscalers must still be configured so that the system clock frequency does not exceed the maximum frequency shown in Figure 30-1.
3. Instruction cycle period (T_{CY}) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type, under standard operating conditions, with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “Min.” values with an external clock applied to the OSCI/CLKI pin. When an external clock input is used, the “Max.” cycle time limit is “DC” (no clock) for all devices.
4. Measurements are taken in EC mode. The CLKO signal is measured on the OSCO pin. CLKO is low for the Q1-Q2 period (1/2 T_{CY}) and high for the Q3-Q4 period (1/2 T_{CY}).

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Table 30-17. PLL Clock Timing Specifications

Operating Conditions 2.0V to 3.6V (unless otherwise stated): 2.0V < V_{DD} < 3.6V -40°C < T_A < +85°C					
Sym	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
F_{IN}	Input Frequency Range	2	24	MHz	
F_{MIN}	Minimum Output Frequency from the Frequency Multiplier	—	16	MHz	4 MHz F_{IN} with 4x feedback ratio, 2 MHz F_{IN} with 8x feedback ratio
F_{MAX}	Maximum Output Frequency from the Frequency Multiplier	96	—	MHz	4 MHz F_{IN} with 24x net multiplication ratio, 24 MHz F_{IN} with 4x net multiplication ratio
F_{SLEW}	Maximum Step Function of F_{IN} at which the PLL will be Ensured to Maintain Lock	-4	+4	%	Full input range of F_{IN}
T_{LOCK}	Lock Time for VCO	—	24	µs	With the specified minimum, T_{REF}, and a lock timer count of one cycle, this is the maximum VCO lock time supported
J_{FM8}	Cumulative Jitter of Frequency Multiplier Over Voltage and Temperature during Any Eight Consecutive Cycles of the PLL Output	—	±0.12	%	4 MHz F_{IN} with 4x feedback ratio

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Table 30-18. FRC Oscillator Specifications

Operating Conditions (unless otherwise stated): 2.0V < V_{DD} < 3.6V -40°C < T_A < +85°C							
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(3)**	**Max**	**Units**	**Conditions**
F20	A_{FRC}	FRC Accuracy @ 8 MHz(1)	-1.5	+0.15	1.5	%	-20°C ≤ T_A ≤ +85°C
			-2.5	—	2.5	%	-40°C ≤ T_A ≤ -20°C
			-2.5	—	2.5	%	85°C ≤ T_A ≤ +125°C
F20A	$A_{FRCTUNE}$	FRC Accuracy @ 8 MHz with Enabled Self-Tune Feature	-0.20	+0.05	-0.20	%	0°C ≤ T_A ≤ +85°C
FR0	T_{FRC}	FRC Oscillator Start-up Time	—	2	—	µS	
F22	S_{TUNE}	OSCTUN Step-Size	—	0.05	—	%/bit	
F23	T_{LOCK}	FRC Self-Tune Lock Time(2)	—	5	8	ms	

Notes:

1. To achieve this accuracy, physical stress applied to the microcontroller package (ex., by flexing the PCB) must be kept to a minimum.
2. Time from reference clock stable, and in range, to FRC tuned with range specified by F20 (with self-tune).
3. Data in the “Typ” column are 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

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Table 30-19. LPRC Oscillator Specifications

Operating Conditions (unless otherwise stated): 2.0V < V_{DD} < 3.6V -40°C < T_A < +85°C						
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**
FR21	A_{LPRC}	LPRC Accuracy @ 32 kHz	-20	—	20	%
FR1	T_{LPRC}	Low-Power RC Oscillator Start-up Time	—	50	—	µs

Note:

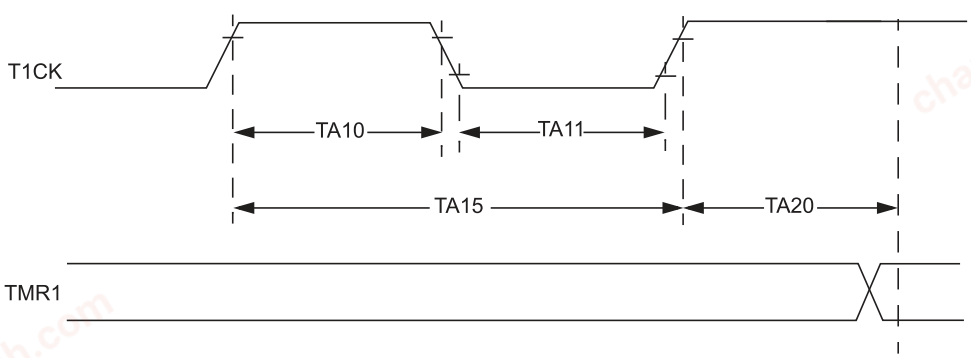
1. Data in the “Typ” column are 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

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Table 30-20. Reset and Brown-out Reset Requirements

Operating Conditions (unless otherwise stated): 2.0V < V_{DD} < 3.6V -40°C < T_A < +85°C							
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
SY10	T_{MCL}	$\overline{MCLR}$ Pulse Width (Low)	2	—	—	µs	
SY12	T_{POR}	Power-on Reset Delay	—	2	—	µs	
SY13	T_{IOZ}	I/O High-Impedance from $\overline{MCLR}$ Low or Watchdog Timer Reset	Lesser of: (3 T_{CY} + 2) or 700	—	(3 T_{CY} + 2)	µs	
SY25	T_{BOR}	Brown-out Reset Pulse Width	1	—	—	µs	$V_{DD} \leq V_{BOR}$
SY45	T_{RST}	Internal State Reset Time	—	50	—	µs	
SY71	T_{WAKEUP}	Wake-up Time from Sleep Mode	—	7	—	µs	VREGS (RCON[8]) = 1, RETEN (RCON[12]) = 0 $\overline{LPCFG}$ (FPOR[2]) = 1
			—	35	—	µs	VREGS (RCON[8]) = 0, RETEN (RCON[12]) = 0 $\overline{LPCFG}$ (FPOR[2]) = 1
			—	195		µs	VREGS (RCON[8]) = 1, RETEN (RCON[12]) = 1 $\overline{LPCFG}$ (FPOR[2]) = 0
			—	315		µs	VREGS (RCON[8]) = 0, RETEN (RCON[12]) = 1 $\overline{LPCFG}$ (FPOR[2]) = 0

Figure 30-5. Timer1 External Clock Timing Characteristics



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Table 30-21. Timer1 External Clock Timing Characteristics

Operating Conditions (unless otherwise stated): 2.0V < V_{DD} < 3.6V -40°C < T_A < +85°C							
Param No.	**Symbol**	**Characteristics(1)**		**Min**	**Max**	**Units**	**Conditions**
TA10	T_{CKH}	T1CK High Time	Synchronous	1	—	T_{CY}	Must also meet Parameter TA15
			Asynchronous	10	—	ns	
TA11	T_{CKL}	T1CK Low Time	Synchronous	1	—	T_{CY}	Must also meet Parameter TA15
			Asynchronous	10	—	ns	
TA15	T_{CKP}	T1CK Input Period	Synchronous	2	—	T_{CY}	
			Asynchronous	20	—	ns	
TA20	$T_{CKEXTMRL}$	Delay from External T1CK Clock Edge to Timer Increment		—	3	T_{CY}	Synchronous mode

Note:

1. These parameters are characterized but not tested in manufacturing.

Figure 30-6. MCCP Timer Mode External Clock Timing Characteristics

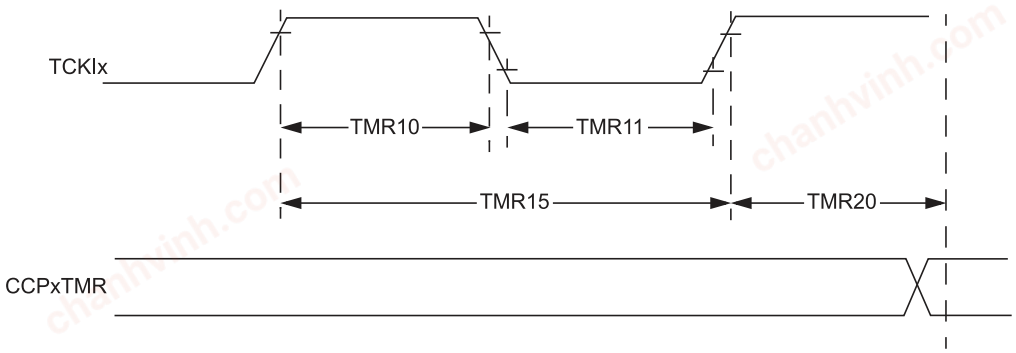


Table 30-22. MCCP Timer Mode Timing Requirements

Operation Conditions (unless otherwise stated): 2.0V < V_{DD} < 3.6V -40°C < T_A < +85°C							
Param No.	**Symbol**	**Characteristics(1)**		**Min**	**Max**	**Units**	**Conditions**
TMR10	T_{CKH}	TCKIx High Time	Synchronous	1	—	T_{CY}	Must also meet Parameter TMR15
			Asynchronous	10	—	ns	
TMR11	T_{CKL}	TCKIx Low Time	Synchronous	1	—	T_{CY}	Must also meet Parameter TMR15
			Asynchronous	10	—	ns	

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.....continued							
Operation Conditions (unless otherwise stated): **2.0V < V_{DD} < 3.6V** **-40°C < T_A < +85°C**							
TMR15	T_{CKP}	TCKIx Input Period	Synchronous	2	—	T_{CY}	
			Asynchronous	20	—	ns	
TMR20	$T_{CKEXTMRL}$	Delay from External TCKIx Clock Edge to Timer Increment		—	1	T_{CY}	

Note:

1. These parameters are characterized but not tested in manufacturing.

Figure 30-7. MCCP Input Capture Mode Timing Characteristics

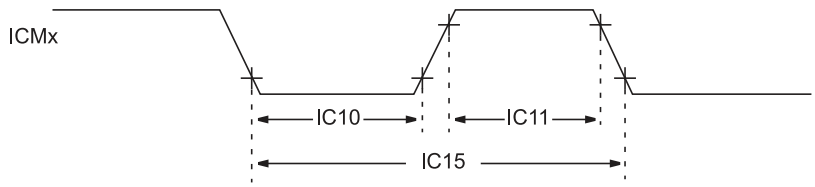


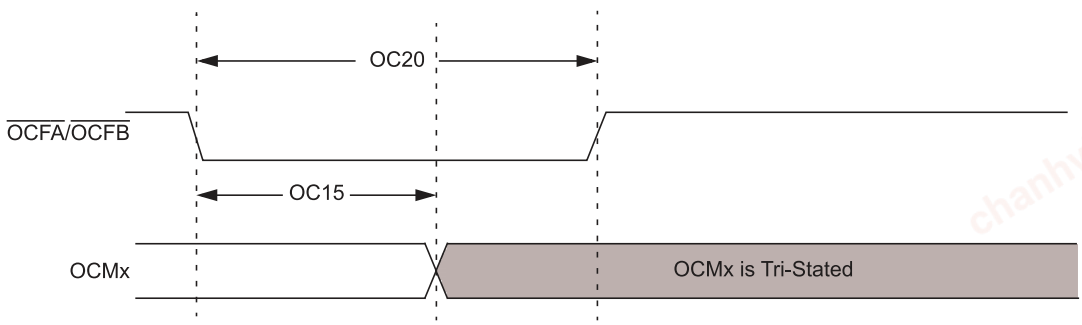
Table 30-23. MCCP Input Capture Mode Timing Requirements

Operation Conditions (unless otherwise stated): **2.0V < V_{DD} < 3.6V** **-40°C < T_A < +85°C**						
Param No.	**Symbol**	**Characteristics(1)**	**Min**	**Max**	**Units**	**Conditions**
IC10	T_{ICL}	ICMx Input Low Time	25	—	ns	Must also meet Parameter IC15
IC11	T_{ICH}	ICMx Input High Time	25	—	ns	Must also meet Parameter IC15
IC15	T_{ICP}	ICMx Input Period	50	—	ns	

Note:

1. These parameters are characterized but not tested in manufacturing.

Figure 30-8. MCCP PWM Mode Timing Characteristics



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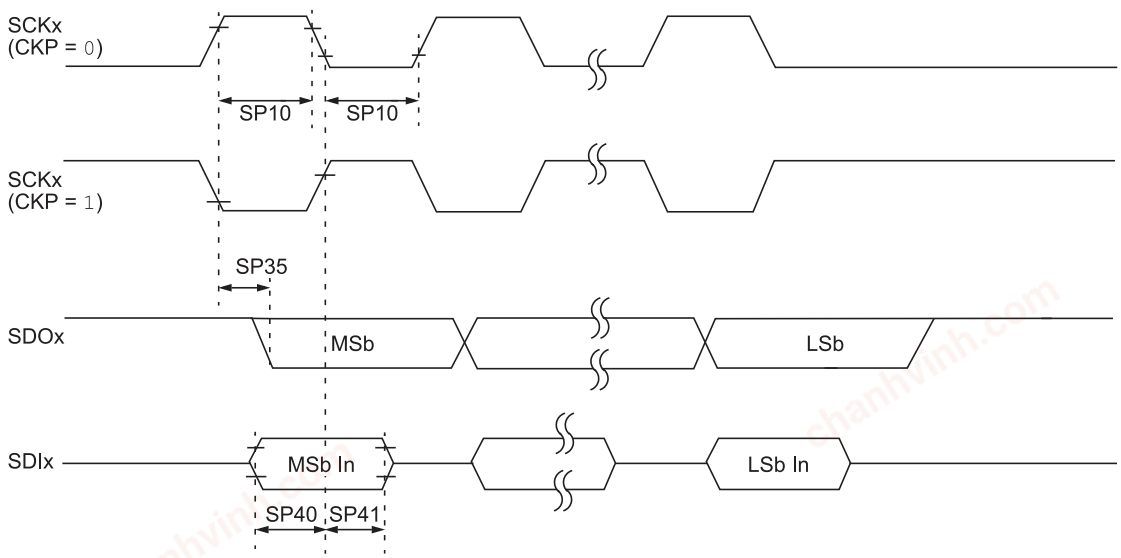
Table 30-24. MCCP PWM Mode Timing Requirements

Operation Conditions (unless otherwise stated): 2.0V < V_{DD} < 3.6V -40°C < T_A < +85°C					
Param No.	**Symbol**	**Characteristics(1)**	**Min**	**Max**	**Units**
OC15	T_{FD}	Fault Input to PWM I/O Change	—	30	ns
OC20	T_{FLT}	Fault Input Pulse Width	10	—	ns

Note:

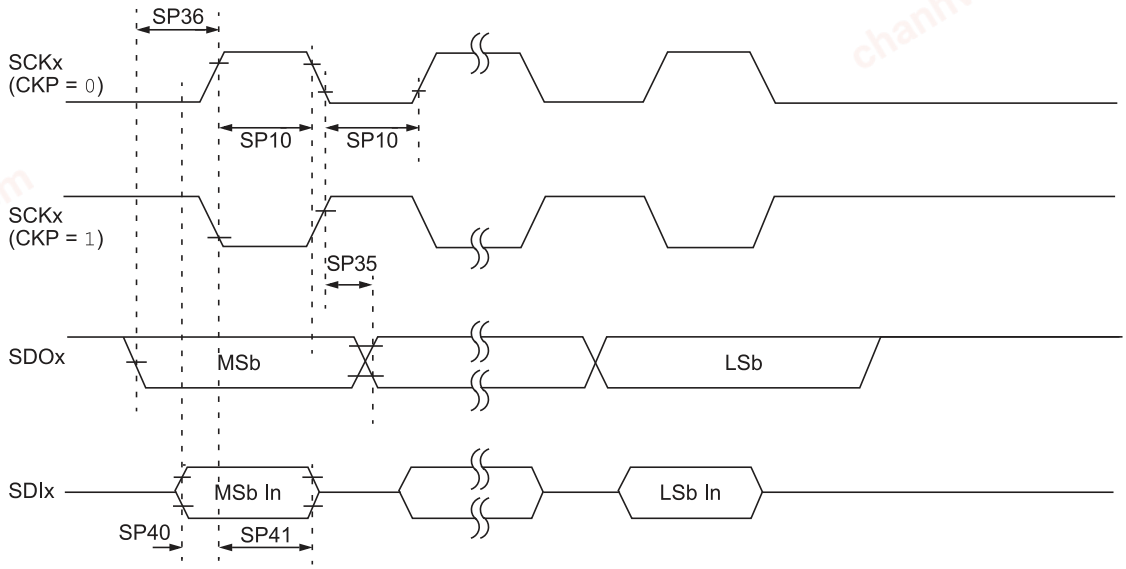
1. These parameters are characterized but not tested in manufacturing.

Figure 30-9. SPI Module Host Mode (CKE = 0) Timing Characteristics



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Figure 30-10. SPI Module Host Mode (CKE = 1) Timing Characteristics



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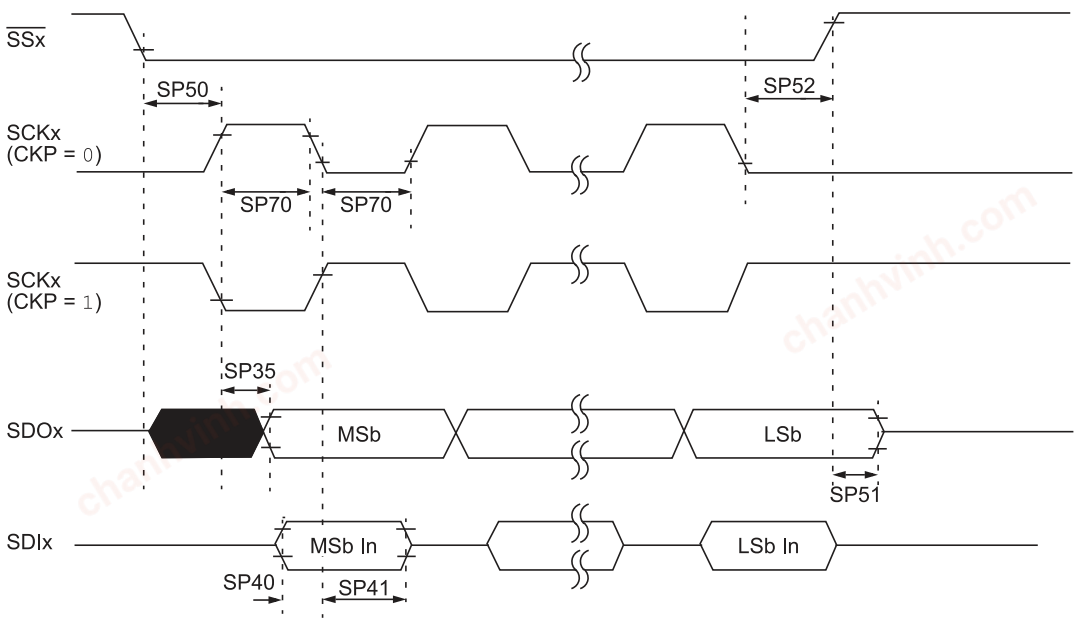
Table 30-25. SPI Module Host Mode Timing Requirements

Operation Conditions (unless otherwise stated): 2.0V < V_{DD} < 3.6V -40°C < T_A < +85°C					
Param No.	**Symbol**	**Characteristics(1)**	**Min**	**Max**	**Units**
SP10	$T_{SC}L$, TscH	SCKx Output Low or High Time	20	—	ns
SP35	$T_{SCH2DO}V$, $T_{SCL2DO}V$	SDOx Data Output Valid after SCKx Edge	—	7	ns
SP36	$T_{DO}V2_{SC}$, $T_{DO}V2_{SC}L$	SDOx Data Output Setup to First SCKx Edge	7	—	ns
SP40	$T_{DI}V2_{SC}H$, $T_{DI}V2_{SC}L$	Setup Time of SDIx Data Input to SCKx Edge	7	—	ns
SP41	$T_{SC}H2_{DI}L$, $T_{SC}L2_{DI}L$	Hold Time of SDIx Data Input to SCKx Edge	7	—	ns

Note:

1. These parameters are characterized but not tested in manufacturing.

Figure 30-11. SPI Module Client Mode (CKE = 0) Timing Characteristics



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Figure 30-12. SPI Module Client Mode (CKE = 1) Timing Characteristics

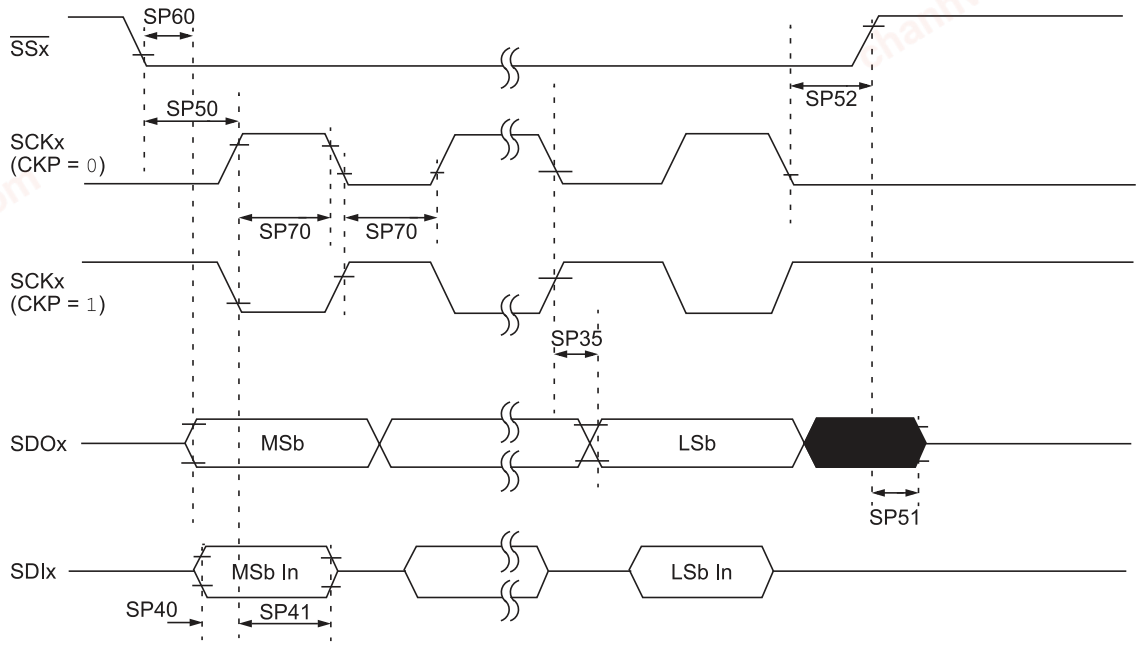


Table 30-26. SPI Module Client Mode Timing Requirements

Operation Conditions (unless otherwise stated): 2.0V < V_{DD} < 3.6V -40°C < T_A < +85°C					
Param No.	**Symbol**	**Characteristics(1)**	**Min**	**Max**	**Units**
SP70	$T_{SC}L$, $T_{SC}H$	SCKx Input Low Time or High Time	20	—	ns
SP35	$T_{SC}H2_{DO}V$, $T_{SC}L2_{DO}V$	SDOx Data Output Valid after SCKx Edge	—	10	ns
SP40	$T_{DI}V2_{SC}H$, $T_{DI}V2_{SC}L$	Setup Time of SDIx Data Input to SCKx Edge	0	—	ns
SP41	$T_{SC}H2_{DI}L$, $T_{SC}L2_{DI}L$	Hold Time of SDIx Data Input to SCKx Edge	7	—	ns
SP50	$T_{SS}L2_{SC}H$, $T_{SS}L2_{SC}L$	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	40	—	ns
SP51	$T_{SS}H2S_{DO}Z$	$\overline{SSx}$ ↑ to SDOx Output High-Impedance	2.5	12	ns
SP52	$T_{SC}H2_{SS}H$, $T_{SC}L2_{SS}H$	$\overline{SSx}$ ↑ after SCKx Edge	10	—	ns
SP60	$T_{SS}L2_{DO}V$	SDOx Data Output Valid after $\overline{SSx}$ Edge	—	12.5	ns

Note:

1. These parameters are characterized but not tested in manufacturing.

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Figure 30-13. I²C Bus Start/Stop Bits Timing Characteristics (Host Mode)

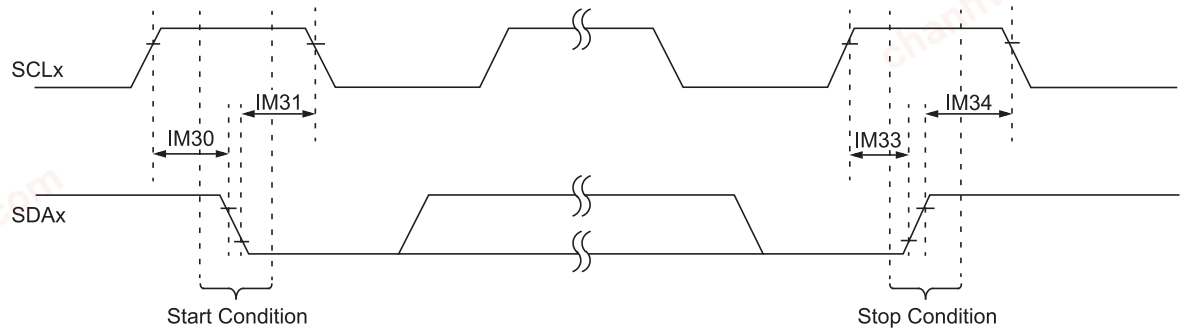


Figure 30-14. I²C Bus Data Timing Characteristics (Host Mode)

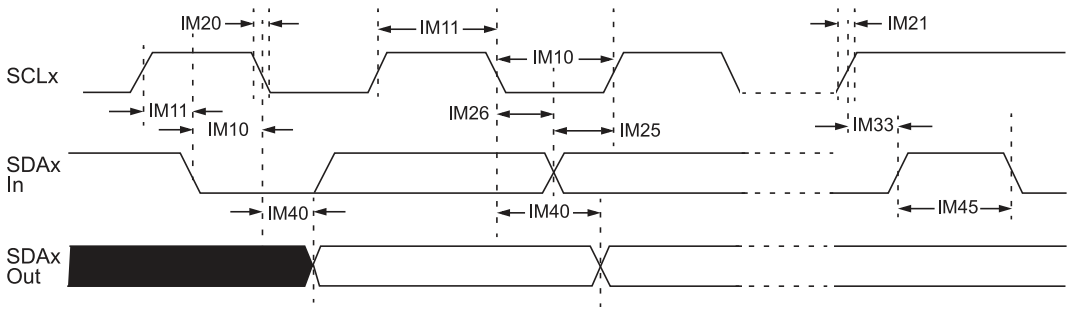


Table 30-27. I²C Bus Data Timing Requirements (Host Mode)

Operation Conditions (unless otherwise stated): 2.0V < V_{DD} < 3.6V -40°C < T_A < +85°C							
Param No.	**Symbol**	**Characteristics(1)**		**Min.**	**Max.**	**Units**	**Conditions**
IM10	$T_{LO:SCL}$	Clock Low Time	100 kHz mode	T_{CY} * (BRG + 2)	—	µs	
			400 kHz mode	T_{CY} * (BRG + 2)	—	µs	
			1 MHz mode	T_{CY} * (BRG + 2)	—	µs	
IM11	$T_{HI:SCL}$	Clock High Time	100 kHz mode	T_{CY} * (BRG + 2)	—	µs	
			400 kHz mode	T_{CY} * (BRG + 2)	—	µs	
			1 MHz mode	T_{CY} * (BRG + 2)	—	µs	
IM20	$T_{F:SCL}$	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1 C_B	300	ns	
			1 MHz mode	—	100	ns	
IM21	$T_{R:SCL}$	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1 C_B	300	ns	
			1 MHz mode	—	300	ns	
IM25	$T_{SU:DAT}$	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode	100	—	ns	

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.....continued

Operation Conditions (unless otherwise stated): 2.0V < V_{DD} < 3.6V -40°C < T_A < +85°C							
Param No.	**Symbol**	**Characteristics(1)**		**Min.**	**Max.**	**Units**	**Conditions**
IM26	$T_{HD:DAT}$	Data Input Hold Time	100 kHz mode	0	—	µs	
			400 kHz mode	0	0.9	µs	
			1 MHz mode	0	0.3	µs	
IM30	$T_{SU:STA}$	Start Condition Setup Time	100 kHz mode	T_{CY} * (BRG + 2)	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	T_{CY} * (BRG + 2)	—	µs	
			1 MHz mode	T_{CY} * (BRG + 2)	—	µs	
IM31	$T_{HD:STA}$	Start Condition Hold Time	100 kHz mode	T_{CY} * (BRG + 2)	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	T_{CY} * (BRG + 2)	—	µs	
			1 MHz mode	T_{CY} * (BRG + 2)	—	µs	
IM33	$T_{SU:STO}$	Stop Condition Setup Time	100 kHz mode	T_{CY} * (BRG + 2)	—	µs	
			400 kHz mode	T_{CY} * (BRG + 2)	—	µs	
			1 MHz mode	T_{CY} * (BRG + 2)	—	µs	
IM34	$T_{HD:STO}$	Stop Condition Hold Time	100 kHz mode	T_{CY} * (BRG + 2)	—	ns	
			400 kHz mode	T_{CY} * (BRG + 2)	—	ns	
			1 MHz mode	T_{CY} * (BRG + 2)	—	ns	
IM40	$T_{AA:SCL}$	Output Valid from Clock	100 kHz mode	—	3500	ns	
			400 kHz mode	—	1000	ns	
			1 MHz mode	—	350	ns	
IM45	$T_{BF:SDA}$	Bus Free Time	100 kHz mode	4.7	—	µs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode	0.5	—	µs	
IM50	C_B	Bus Capacitive Loading	100 kHz mode	—	400	pF	
			400 kHz mode	—	400	pF	
			1 MHz mode	—	10	pF	
IM51	T_{PGD}	Pulse Gobbler Delay		52	312	ns	

Note:

1. These parameters are characterized but not tested in manufacturing.

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Figure 30-15. I²C Bus Start/Stop Bits Timing Characteristics (Client Mode)

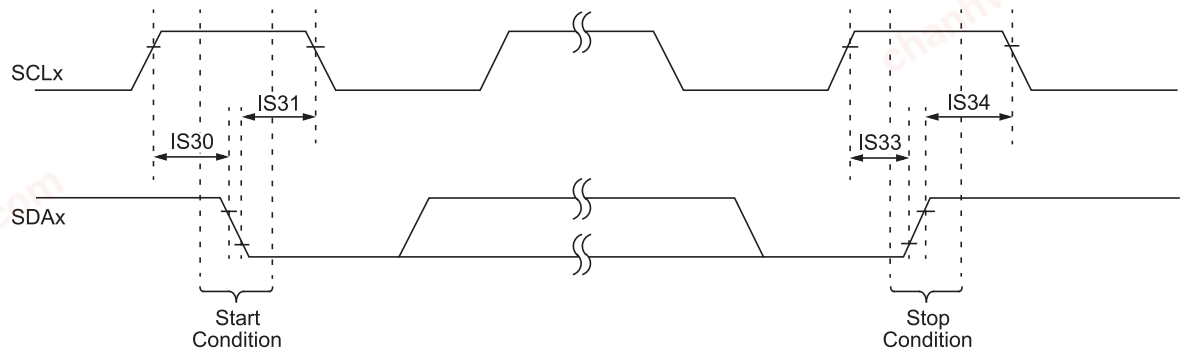


Figure 30-16. I²C Bus Data Timing Characteristics (Client Mode)

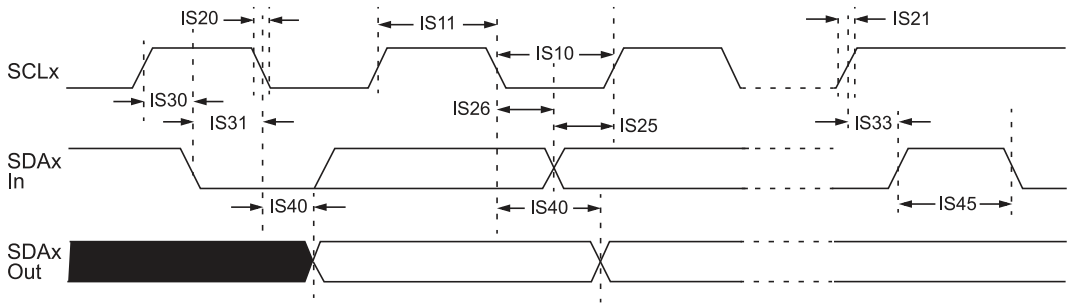


Table 30-28. I²C Bus Data Timing Requirements (Client Mode)

Operation Conditions (unless otherwise stated): 2.0V < V_{DD} < 3.6V -40°C < T_A < +85°C							
Param No.	**Symbol**	**Characteristics**		**Min.**	**Max.**	**Units**	**Conditions**
IS10	$T_{LO:SCL}$	Clock Low Time	100 kHz mode	4.7	—	µs	CPU clock must be a minimum of 800 kHz
			400 kHz mode	1.3	—	µs	CPU clock must be a minimum of 3.2 MHz
			1 MHz mode	0.5	—	µs	
IS11	$T_{HI:SCL}$	Clock High Time	100 kHz mode	4.0	—	µs	CPU clock must be a minimum of 800 kHz
			400 kHz mode	0.6	—	µs	CPU clock must be a minimum of 3.2 MHz
			1 MHz mode	0.5	—	µs	
IS20	$T_{F:SCL}$	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1 C_B	300	ns	
			1 MHz mode	—	100	ns	

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.....continued

Operation Conditions (unless otherwise stated):
2.0V < V_{DD} < 3.6V
-40°C < T_A < +85°C

Param No.	Symbol	Characteristics		Min.	Max.	Units	Conditions
IS21	$T_{R:SCL}$	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1 C_B	300	ns	
			1 MHz mode	—	300	ns	
IS25	$T_{SU:DAT}$	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode	100	—	ns	
IS26	$T_{HD:DAT}$	Data Input Hold Time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	µs	
			1 MHz mode	0	0.3	µs	
IS30	$T_{SU:STA}$	Start Condition Setup Time	100 kHz mode	4700	—	ns	Only relevant for Repeated Start condition
			400 kHz mode	600	—	ns	
			1 MHz mode	250	—	ns	
IS31	$T_{HD:STA}$	Start Condition Hold Time	100 kHz mode	4000	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	600	—	ns	
			1 MHz mode	250	—	ns	
IS33	$T_{SU:STO}$	Stop Condition Setup Time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	
			1 MHz mode	600	—	ns	
IS34	$T_{HD:STO}$	Stop Condition Hold Time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	
			1 MHz mode	250	—	ns	
IS40	$T_{AA:SCL}$	Output Valid from Clock	100 kHz mode	0	3500	ns	
			400 kHz mode	0	1000	ns	
			1 MHz mode	0	350	ns	
IS45	$T_{BF:SDA}$	Bus Free Time	100 kHz mode	4.7	—	µs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode	0.5	—	µs	
IS50	C_B	Bus Capacitive Loading	100 kHz mode	—	400	pF	
			400 kHz mode	—	400	pF	
			1 MHz mode	—	10	pF	

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Table 30-29. A/D Module Specifications

Operation Conditions (unless otherwise stated): 2.0V < V_{DD} < 3.6V -40°C < T_A < +85°C							
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
Device Supply							
AD01	AV_{DD}	Module V_{DD} Supply	Greater of: V_{DD} – 0.3 or 2.2	—	Lesser of: V_{DD} + 0.3 or 3.6	V	
AD02	AV_{SS}	Module V_{SS} Supply	V_{SS} – 0.3	—	V_{SS} + 0.3	V	
Reference Inputs							
AD05	V_{REFH}	Reference Voltage High	AV_{SS} + 1.7	—	AV_{DD}	V	
AD06	V_{REFL}	Reference Voltage Low	AV_{SS}	—	AV_{DD} – 1.7	V	
AD07	V_{REF}	Absolute Reference Voltage	AV_{SS} – 0.3	—	AV_{DD} + 0.3	V	
Analog Inputs							
AD10	V_{INH}-V_{INL}	Full-Scale Input Span	V_{REFL}	—	V_{REFH}	V	**(Note 2)**
AD11	V_{IN}	Absolute Input Voltage	AV_{SS} – 0.3	—	AV_{DD} + 0.3	V	
AD12	V_{INL}	Absolute V_{INL} Input Voltage	AV_{SS} – 0.3	—	AV_{DD}/3	V	
AD13		Leakage Current	—	±1.0	±610	nA	V_{INL} = AV_{SS} = V_{REFL} = 0V, AV_{DD} = V_{REFH} = 3V, Source Impedance = 2.5 kΩ
AD17	R_{IN}	Recommended Impedance of Analog Voltage Source	—	—	2.5k	Ω	10-bit
A/D Accuracy							
AD20B	N_R	Resolution	—	12	—	bits	
AD21B	INL	Integral Nonlinearity	—	±1	< ±2	LSb	V_{INL} = AV_{SS} = V_{REFL} = 0V, AV_{DD} = V_{REFH} = 3V
AD22B	DNL	Differential Nonlinearity	—	—	< ±1(3)	LSb	V_{INL} = AV_{SS} = V_{REFL} = 0V, AV_{DD} = V_{REFH} = 3V
AD23B	G_{ERR}	Gain Error	-2	±1	+4	LSb	V_{INL} = AV_{SS} = V_{REFL} = 0V, AV_{DD} = V_{REFH} = 3V
AD24B	E_{OFF}	Offset Error	-2	±1	+5	LSb	V_{INL} = AV_{SS} = V_{REFL} = 0V, AV_{DD} = V_{REFH} = 3V
AD25B		Monotonicity(1)	—	—	—	—	Guaranteed

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Notes:

1. The A/D conversion result never decreases with an increase in the input voltage.
2. Measurements are taken with the external $V_{REF}+$ and $V_{REF}-$ used as the A/D voltage reference.
3. Codes 511, 1023, 1535, 2559 and 3583 can have a DNL error of -1 LSB to <+1 LSB, code 2047 can have a DNL error of -1 LSB to <+2 LSB and code 3071 can have a DNL error of -1 LSB to < +2.5 LSB.

Table 30-30. A/D Conversion Timing Requirements(1)

Operation Conditions (unless otherwise stated): 2.0V < V_{DD} < 3.6V -40°C < T_A < +85°C							
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	T_{AD}	A/D Clock Period	178	—	—	ns	
AD51	t_{RC}	A/D Internal RC Oscillator Period	—	269.18	—	ns	
Conversion Rate							
AD55	t_{CONV}	SAR Conversion Time, 12-Bit Mode	—	14	—	T_{AD}	
AD55A		SAR Conversion Time, 10-Bit Mode is Typical 12 T_{AD}	—	12	—	T_{AD}	
AD56	F_{CNV}	Throughput Rate	—	—	400	ksps	AV_{DD} > 2.7V(2)
AD57	t_{SAMP}	Sample Time	—	1	—	T_{AD}	
Clock Synchronization							
AD61	t_{PSS}	Sample Start Delay from Setting Sample bit (SAMP)	1.5	—	2.5	T_{AD}	

Notes:

1. Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.
2. Throughput rate is based on AD55 + AD57 + AD61 and the period of T_{AD}.

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Table 30-31. USB OTG Electrical Specifications

Operation Conditions (unless otherwise stated): 2.0V < V_{DD} < 3.6V -40°C < T_A < +85°C						
Param No.	**Symbol**	**Characteristics(1)**	**Min.**	**Max.**	**Units**	**Conditions**
USB313	V_{USB3V3}	USB Voltage	3.0	3.6	V	Voltage on V_{USB3V3} must be in this range for proper USB operation
USB315	V_{ILUSB}	Input Low Voltage for USB Buffer	—	0.8	V	
USB316	V_{IHUSB}	Input High Voltage for USB Buffer	2.0	—	V	
USB318	V_{DIFS}	Differential Input Sensitivity	—	0.2	V	The difference between D+ and D- must exceed this value while VCM is met
USB319	VCM	Differential Common-Mode Range	0.8	2.5	V	
USB320	Z_{OUT}	Driver Output Impedance	28.0	44.0	Ω	
USB321	V_{OL}	Voltage Output Low	0.0	0.3	V	14.25 kΩ load connected to 3.6V
USB322	V_{OH}	Voltage Output High	2.8	3.6	V	14.25 kΩ load connected to ground

Note:

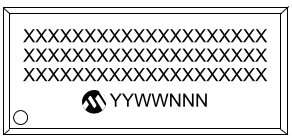
1. These parameters are characterized but not tested in manufacturing.

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31. Package Information

31.1 Package Marking Information

28-Lead SOIC



Example



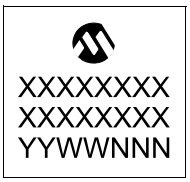
28-Lead SSOP



Example



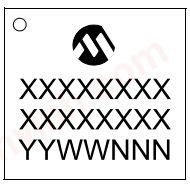
28-Lead QFN (6 x 6 mm)



Example



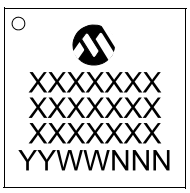
28-Lead UQFN (4x4 mm)



Example



36-Lead UQFN (5x5 mm)



Example



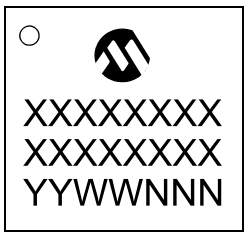
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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31.2 Package Marking Information (Continued)

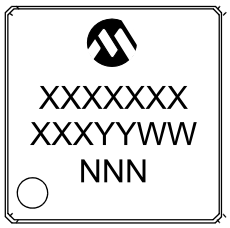
48-Lead UQFN (6x6 mm)



Example



48-Lead TQFP (7x7x1.0 mm)



Example

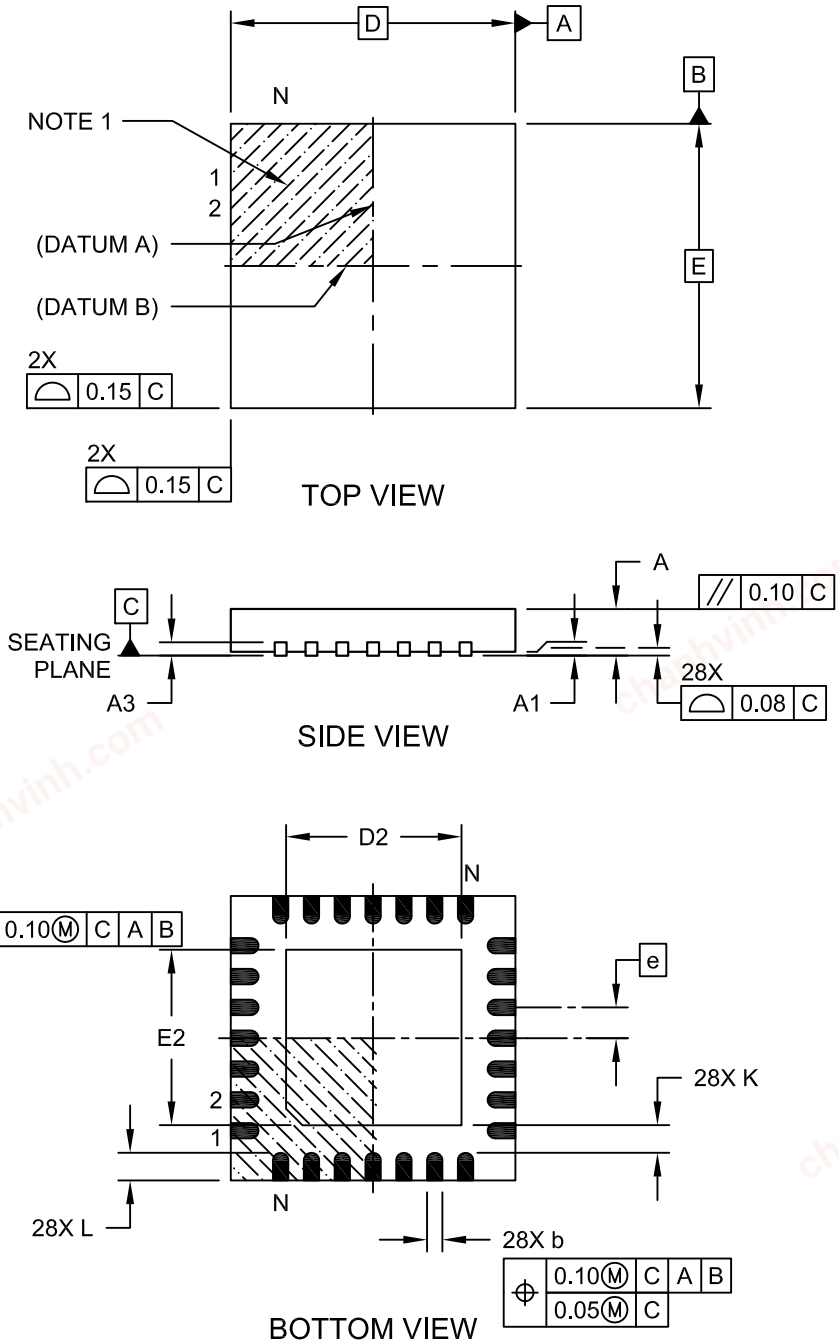


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31.3 Package Details

28-Lead Plastic Quad Flat, No Lead Package (ML) - 6x6 mm Body [QFN] With 0.55 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

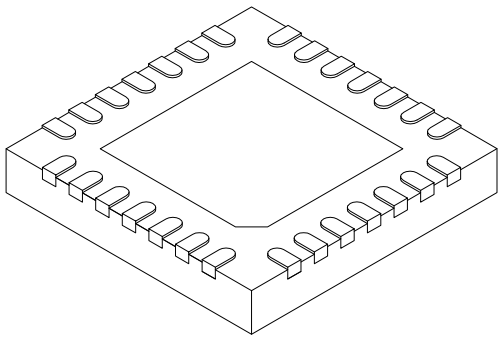


Microchip Technology Drawing C04-105C Sheet 1 of 2

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28-Lead Plastic Quad Flat, No Lead Package (ML) - 6x6 mm Body [QFN] With 0.55 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.65	3.70	4.20
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.65	3.70	4.20
Terminal Width	b	0.23	0.30	0.35
Terminal Length	L	0.50	0.55	0.70
Terminal-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

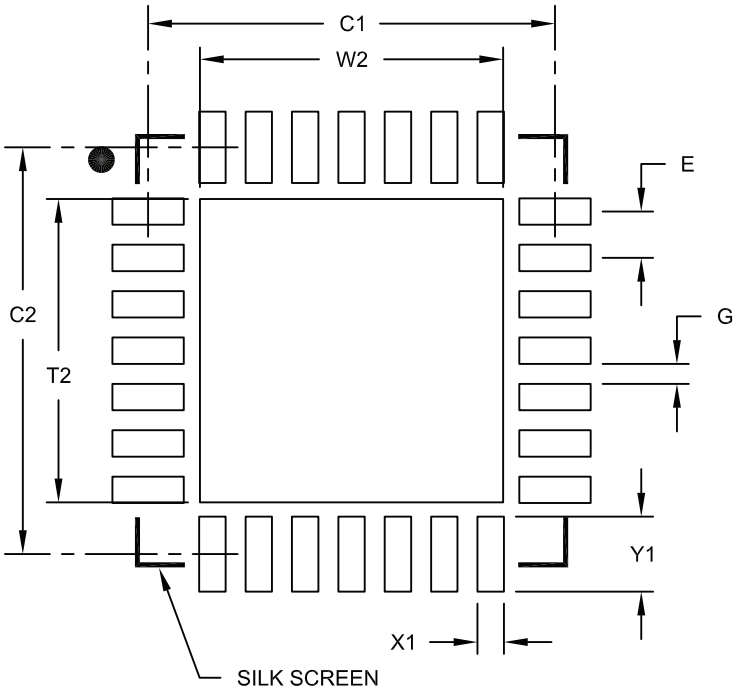
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105C Sheet 2 of 2

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28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

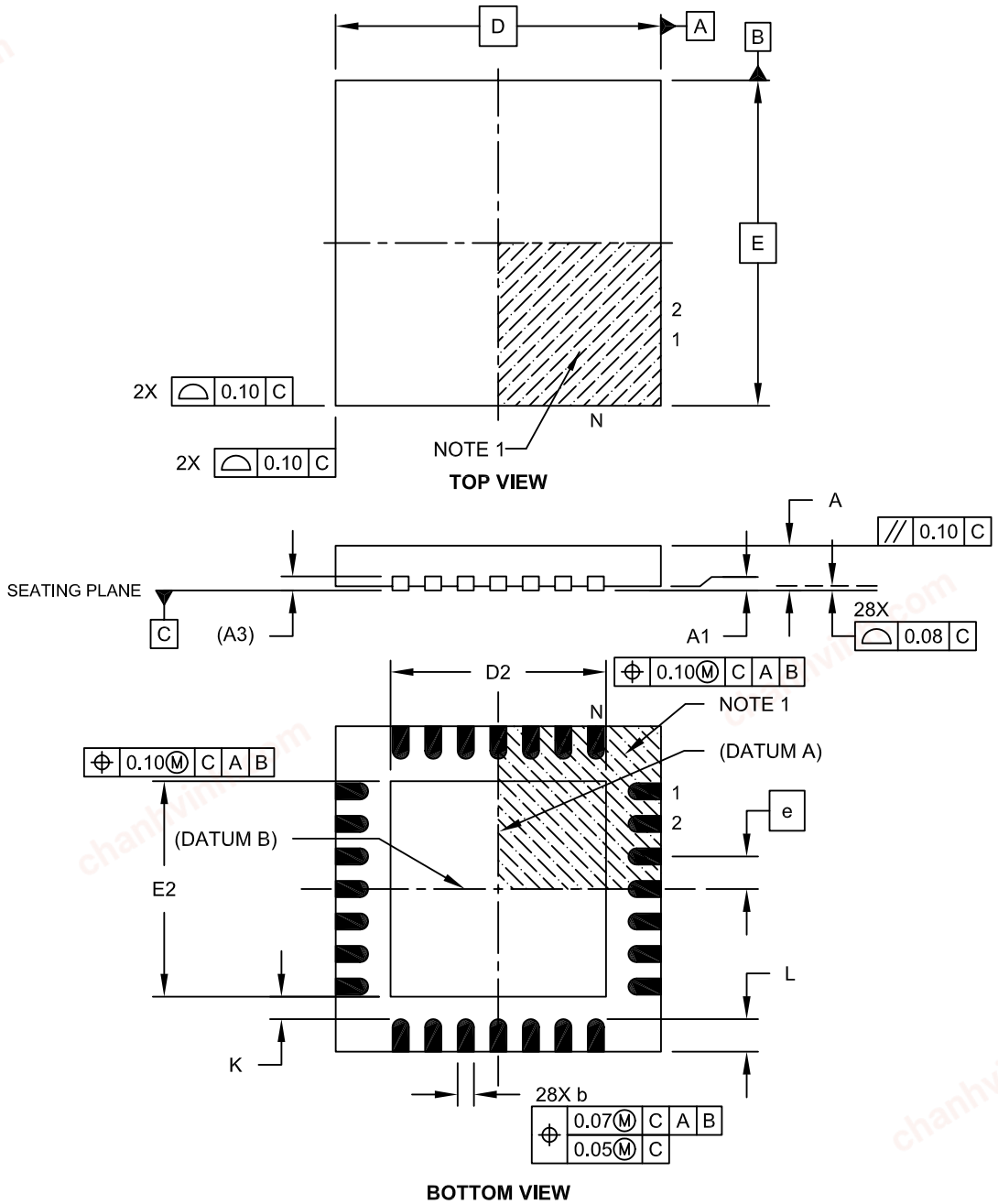
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

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28-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

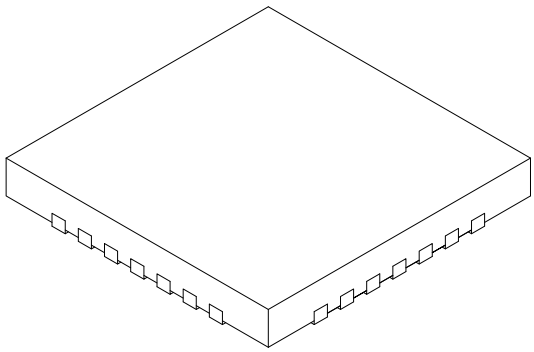


Microchip Technology Drawing C04-152A Sheet 1 of 2

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28-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.40 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.127 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.55	2.65	2.75
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.55	2.65	2.75
Contact Width	b	0.15	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

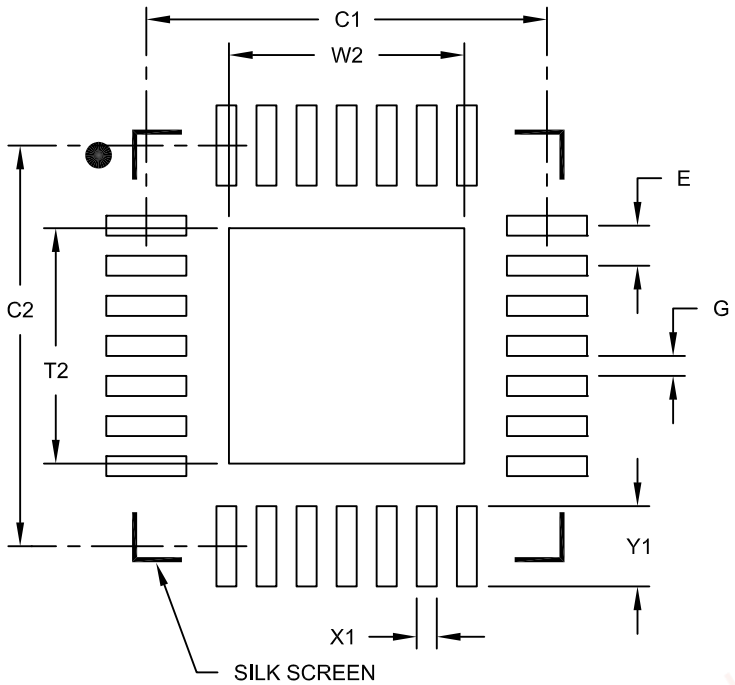
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-152A Sheet 2 of 2

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28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 4x4 mm Body [UQFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	W2			2.35
Optional Center Pad Length	T2			2.35
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X28)	X1			0.20
Contact Pad Length (X28)	Y1			0.80
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

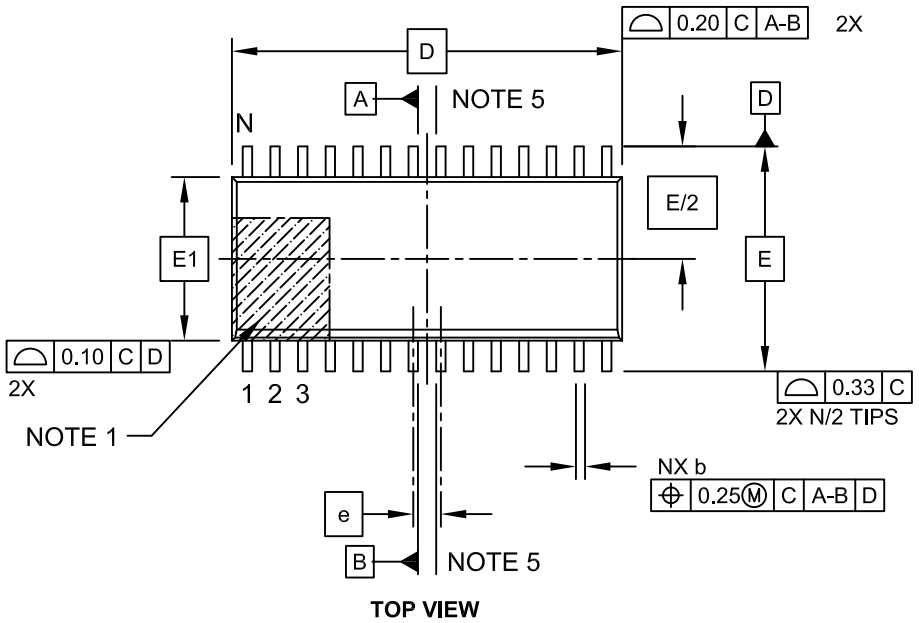
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2152A

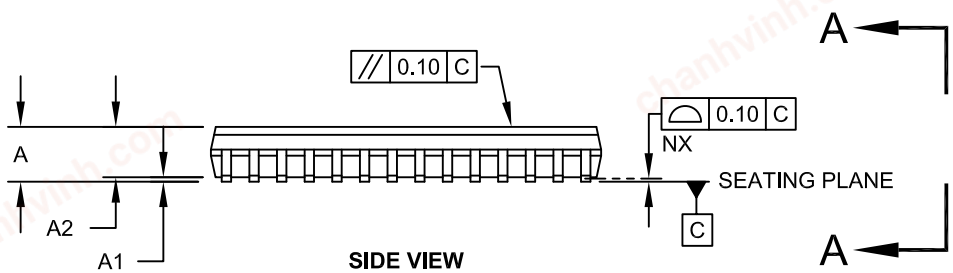
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28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

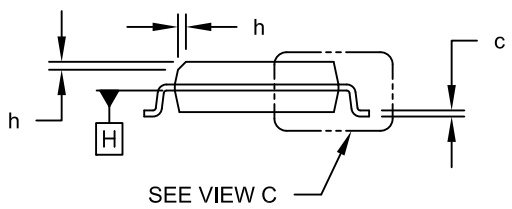
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



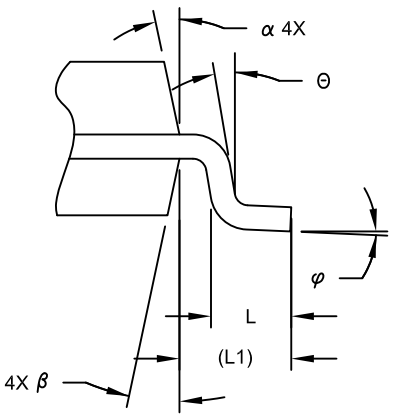
VIEW A-A

Microchip Technology Drawing C04-052C Sheet 1 of 2

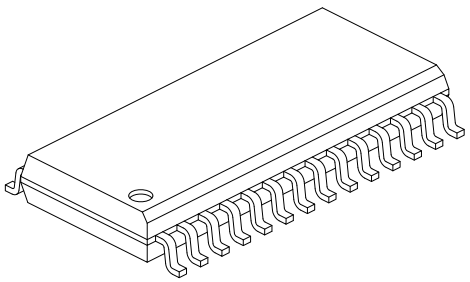
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28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		17.90 BSC	
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1		1.40 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

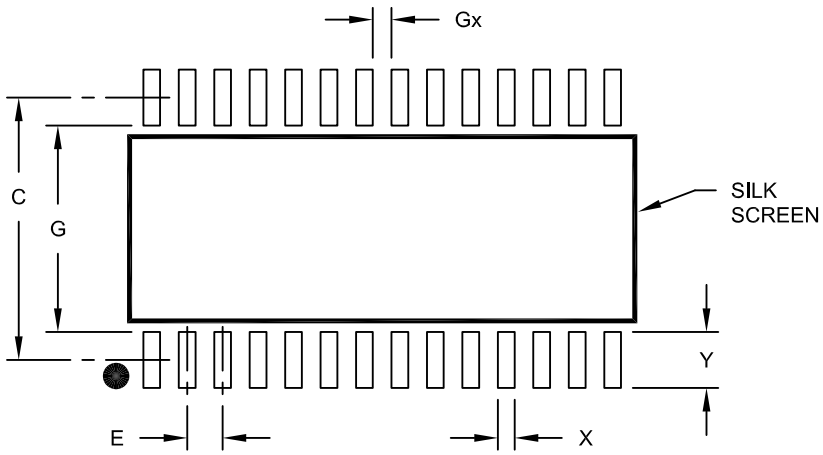
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

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28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

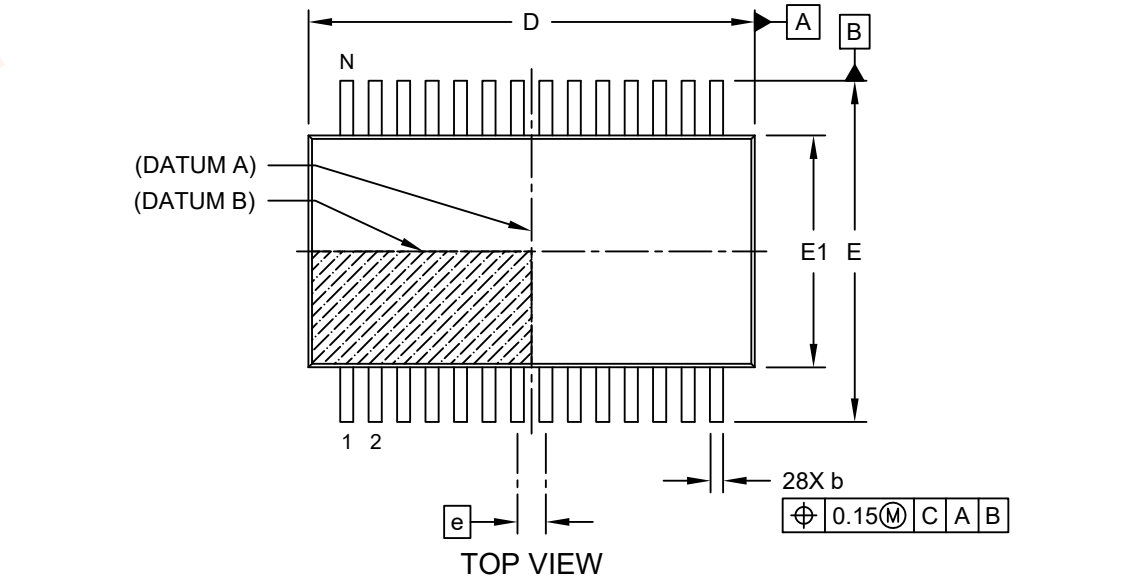
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

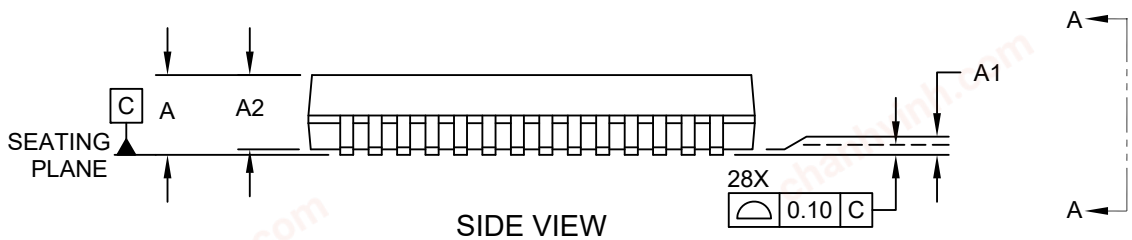
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28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

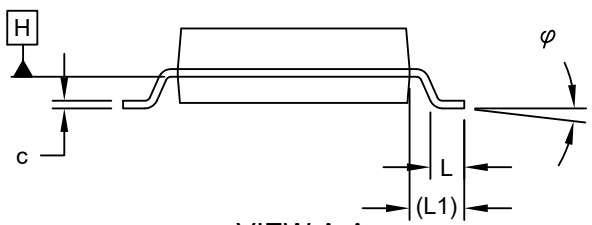
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



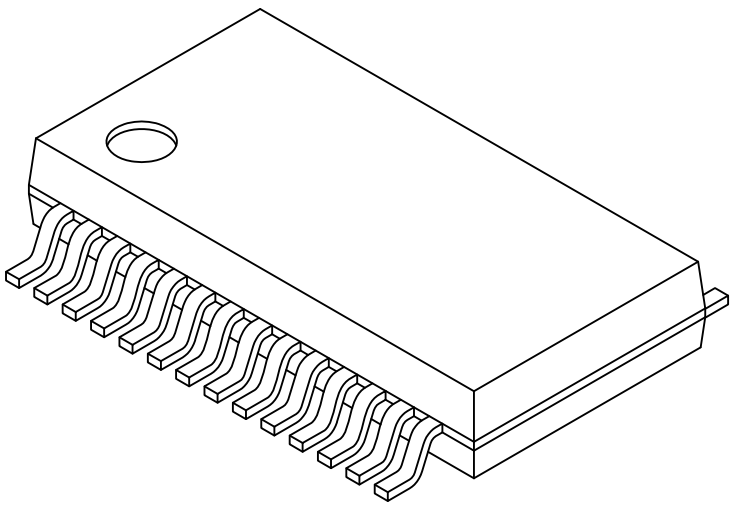
VIEW A-A

Microchip Technology Drawing C04-073 Rev C Sheet 1 of 2

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28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	-	-
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	-	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	-	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

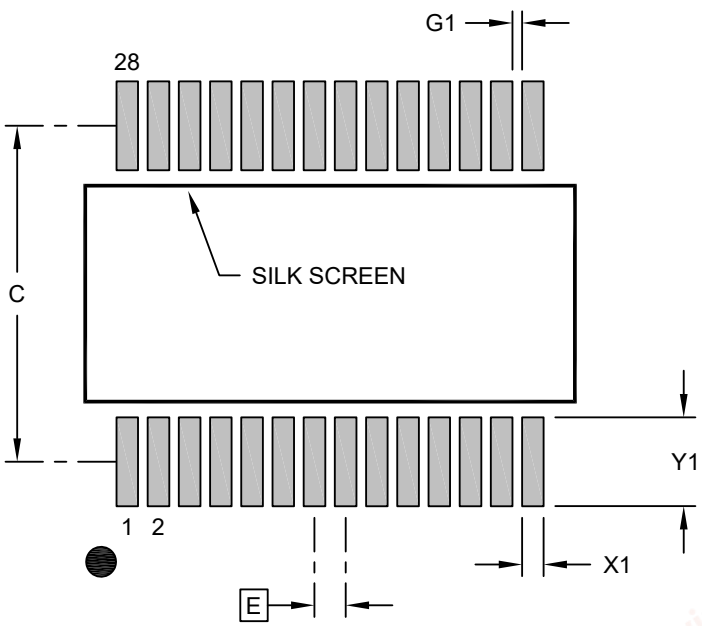
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073 Rev C Sheet 2 of 2

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28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.00	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.85
Contact Pad to Center Pad (X26)	G1	0.20		

Notes:

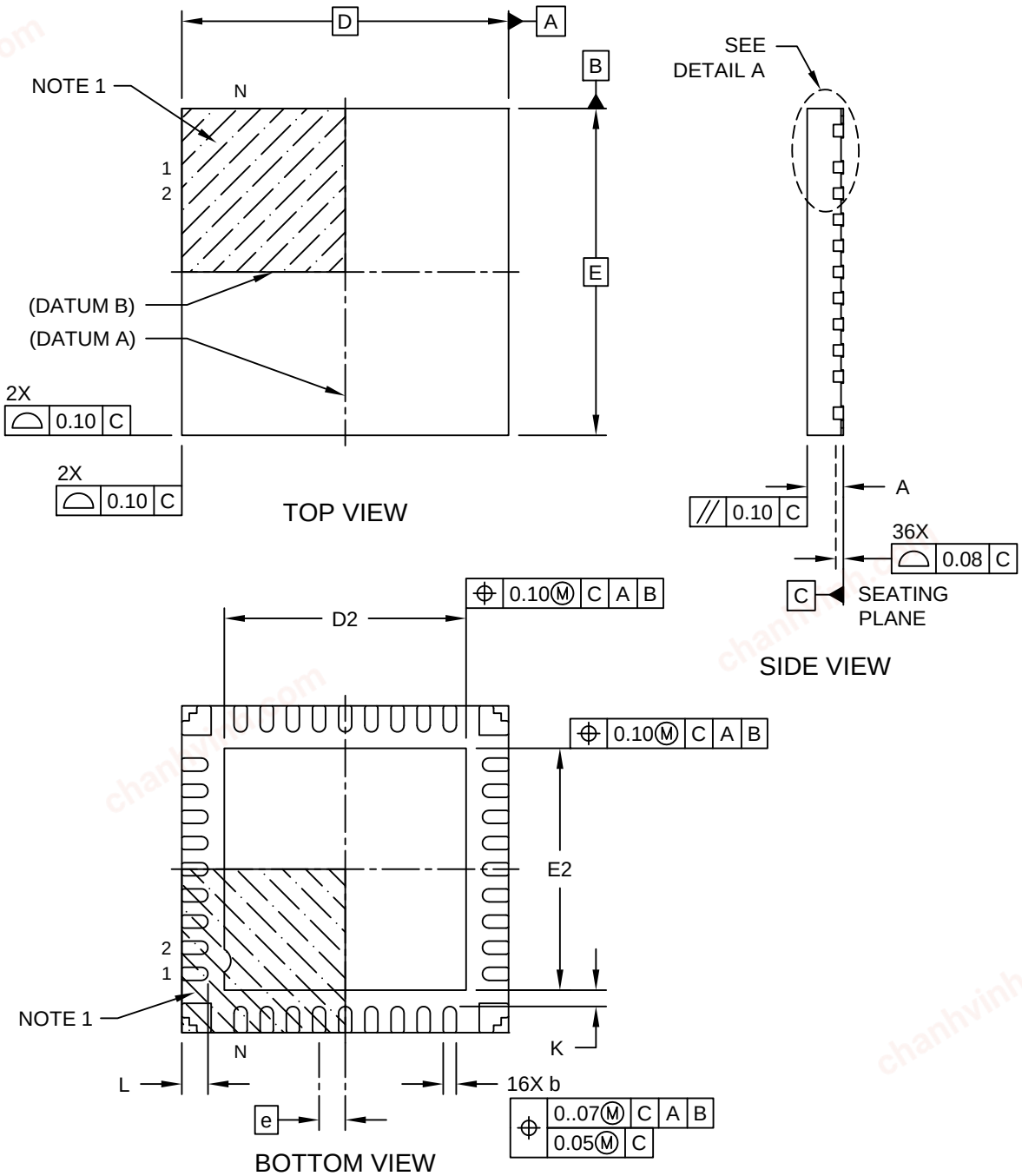
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2073 Rev B

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36-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M5) - 5x5 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

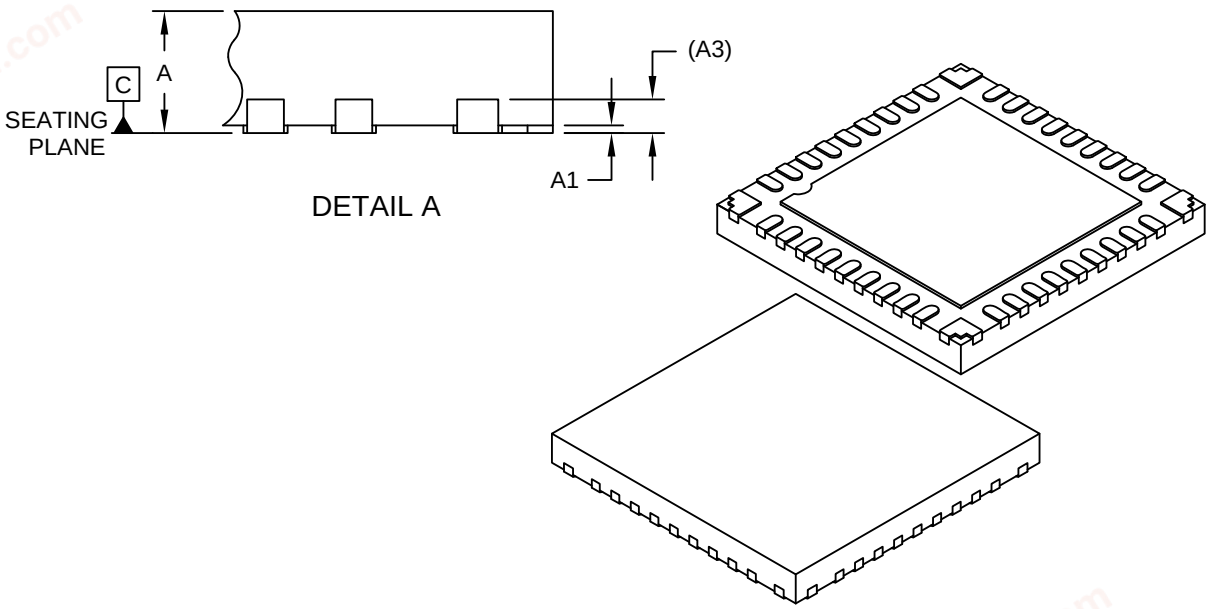


Microchip Technology Drawing C04-436–M5 Rev B Sheet 1 of 2

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36-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M5) - 5x5 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		36	
Pitch	e		0.40 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.60	3.70	3.80
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.60	3.70	3.80
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K		0.25 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

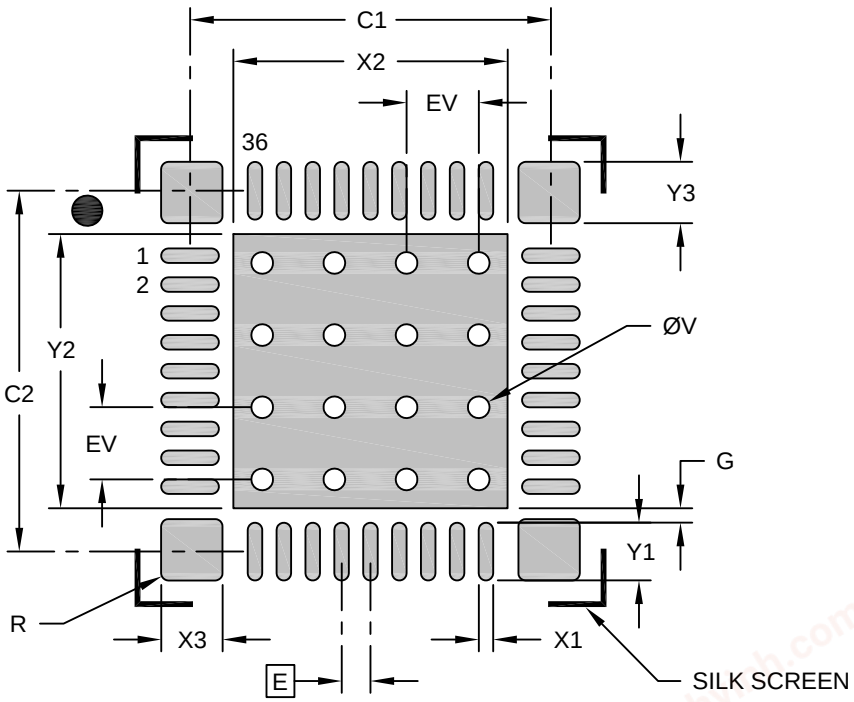
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-436–M5 Rev B Sheet 2 of 2

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36-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M5) - 5x5 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Center Pad Width	X2			3.80
Center Pad Length	Y2			3.80
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X36)	X1			0.20
Contact Pad Length (X36	Y1			0.80
Corner Pad Width (X4)	X3			0.85
Corner Pad Length (X4)	Y3			0.85
Corner Pad Radius	R		0.10	
Contact Pad to Center Pad (X36)	G	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

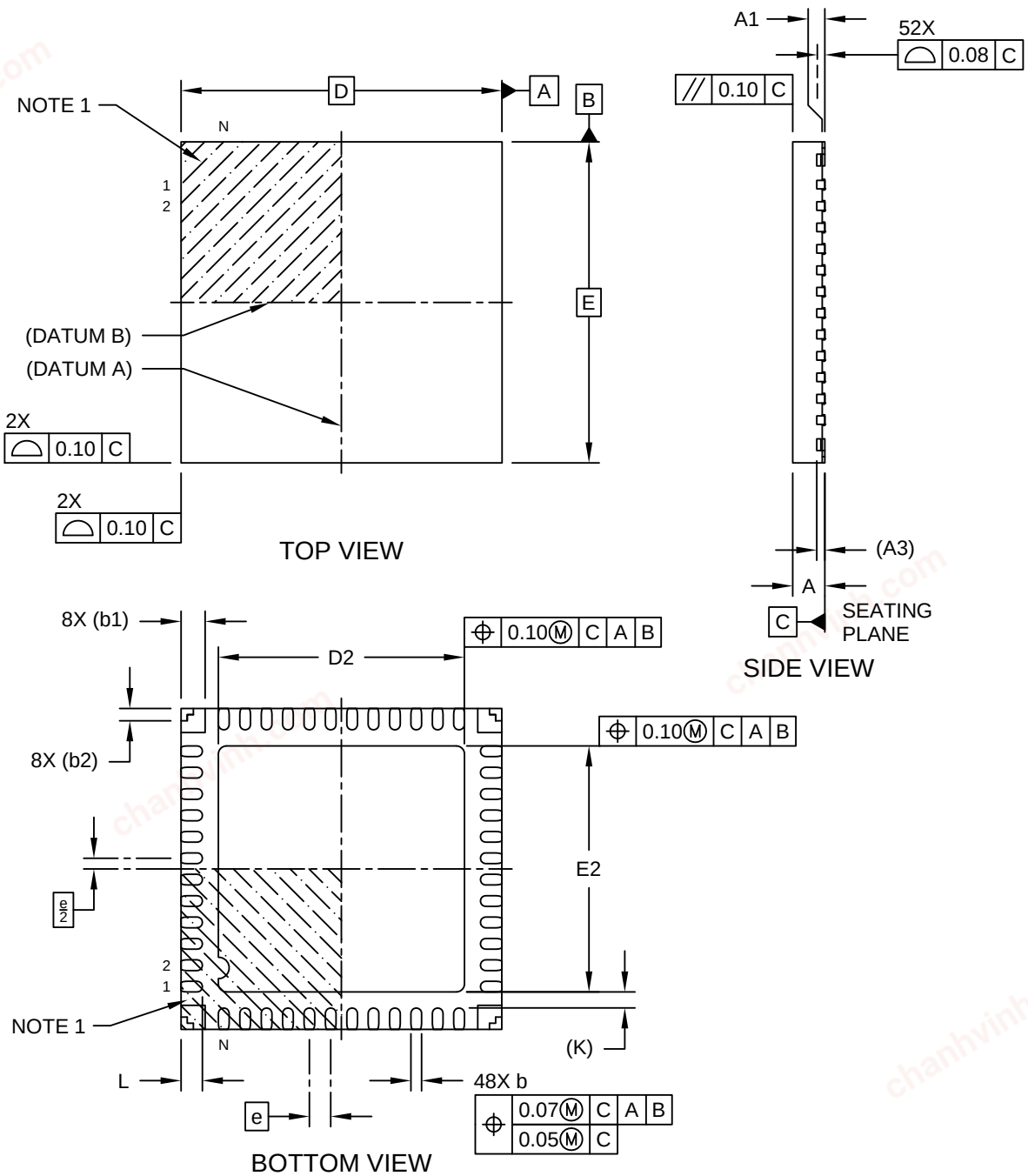
Microchip Technology Drawing C04-2436–M5 Rev B

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48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M4) - 6x6 mm Body [UQFN] With Corner Anchors and 4.6x4.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

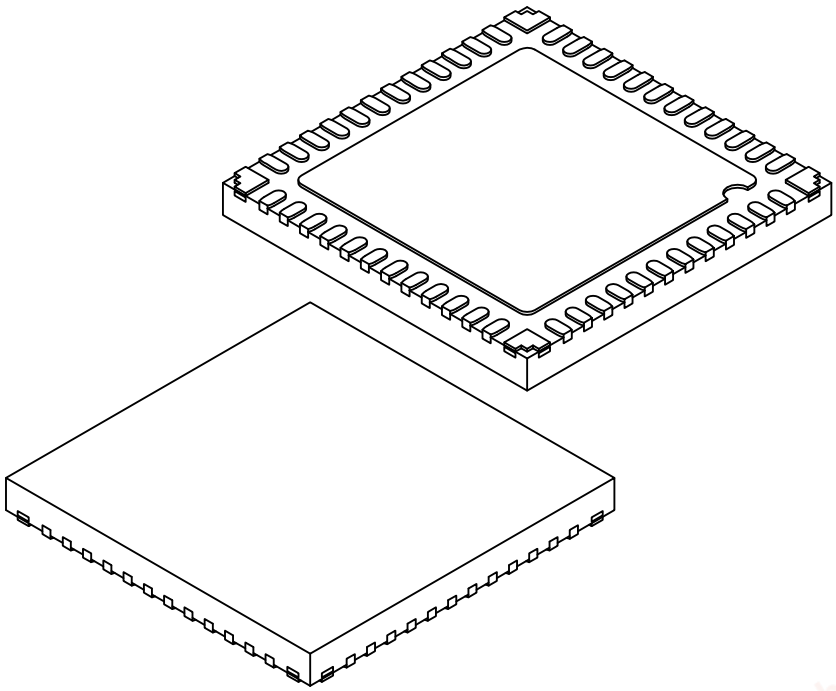


Microchip Technology Drawing C04-442A-M4 Sheet 1 of 2

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48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M4) - 6x6 mm Body [UQFN] With Corner Anchors and 4.6x4.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		48	
Pitch	e		0.40 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.15 REF	
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	4.50	4.60	4.70
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	4.50	4.60	4.70
Terminal Width	b	0.15	0.20	0.25
Corner Anchor Pad	b1		0.45 REF	
Corner Anchor Pad, Metal-free Zone	b2		0.23 REF	
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.30 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

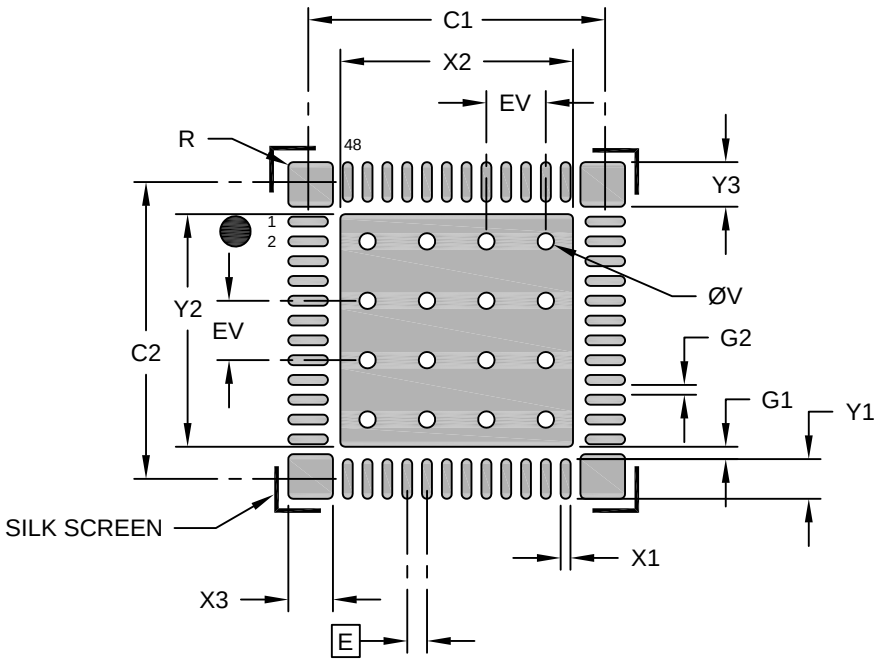
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-442A-M4 Sheet 2 of 2

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48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M4) - 6x6 mm Body [UQFN] With Corner Anchors and 4.6x4.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Center Pad Width	X2			4.70
Center Pad Length	Y2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X48)	X1			0.20
Contact Pad Length (X48)	Y1			0.80
Corner Anchor Pad Width (X4)	X3			0.90
Corner Anchor Pad Length (X4)	Y3			0.90
Pad Corner Radius (X 20)	R			0.10
Contact Pad to Center Pad (X48)	G1	0.25		
Contact Pad to Contact Pad	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

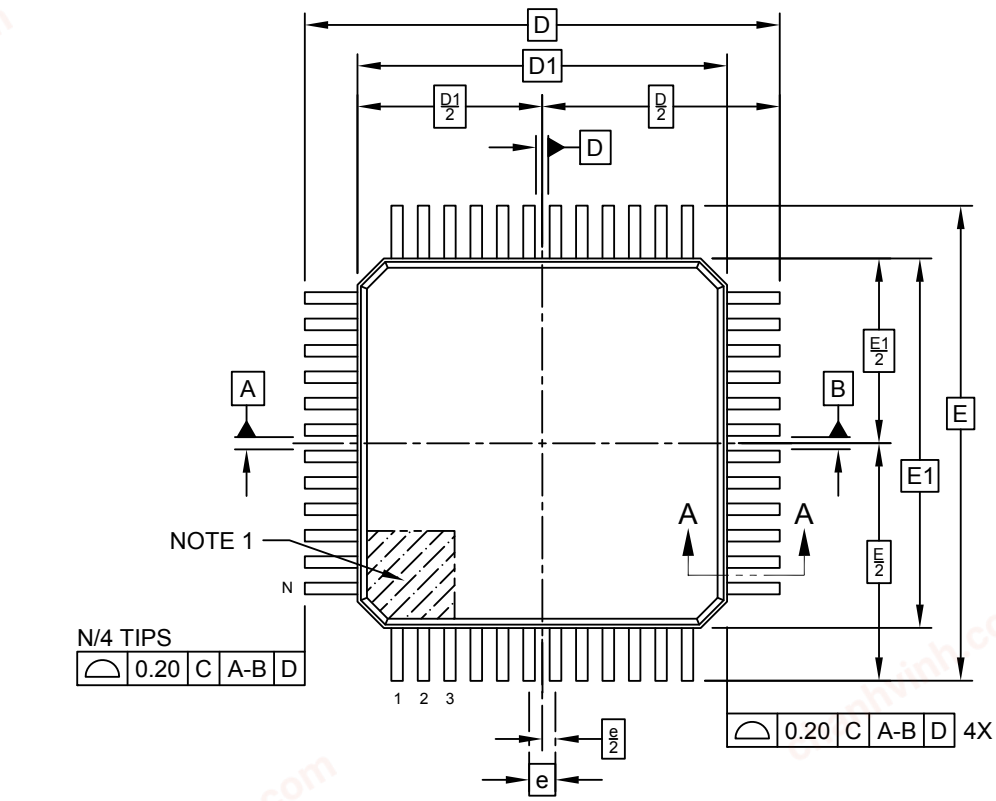
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2442A-M4

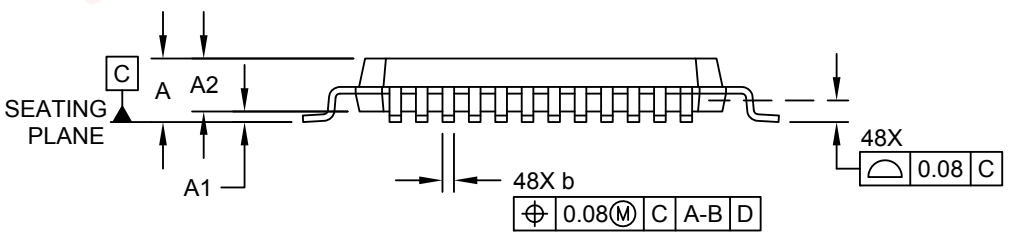
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48-Lead Plastic Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



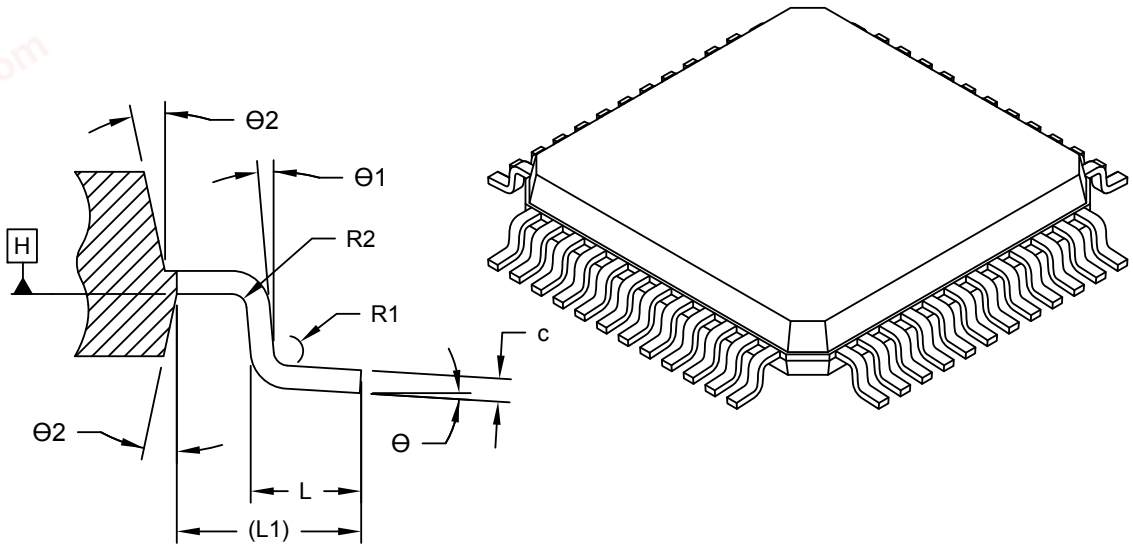
SIDE VIEW

Microchip Technology Drawing C04-300-PT Rev D Sheet 1 of 2

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48-Lead Plastic Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		48	
Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Length	D		9.00 BSC	
Molded Package Length	D1		7.00 BSC	
Overall Width	E		9.00 BSC	
Molded Package Width	E1		7.00 BSC	
Terminal Width	b	0.17	0.22	0.27
Terminal Thickness	c	0.09	-	0.16
Terminal Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Lead Bend Radius	R1	0.08	-	-
Lead Bend Radius	R2	0.08	-	0.20
Foot Angle	Θ	0°	3.5°	7°
Lead Angle	Θ1	0°	-	-
Mold Draft Angle	Θ2	11°	12°	13°

Notes:

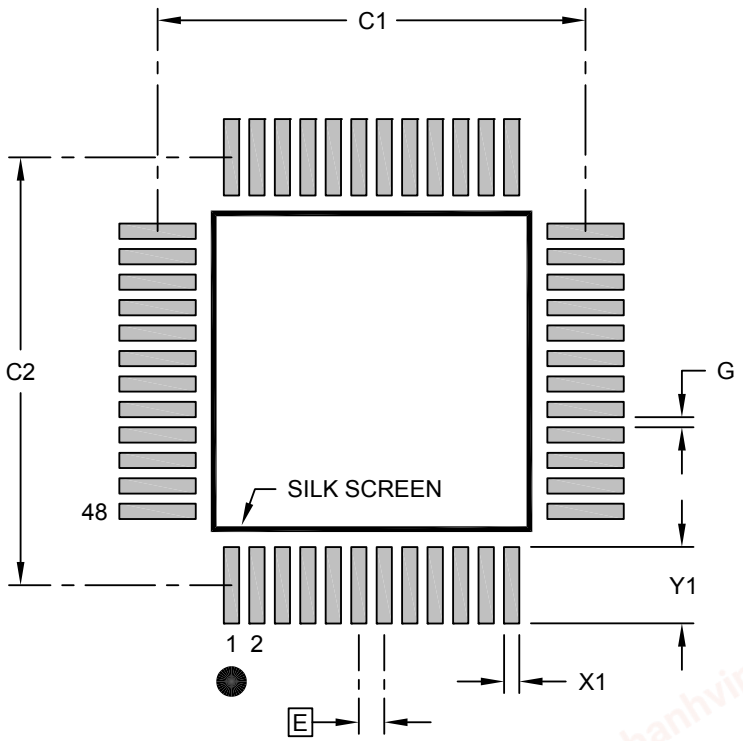
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-300-PT Rev D Sheet 2 of 2

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48-Lead Plastic Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		8.40	
Contact Pad Spacing	C2		8.40	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2300-PT Rev D

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32. Revision History

32.1 Revision A (April 2020)

This is the initial version of the document.

32.2 Revision B (August 2020)

This revision incorporates the following updates:

- Sections:
  - Updates 2.1 Basic Connection Requirements and 10.3 Doze Mode.
  -
- Registers:
  - Updates 8.3.9 IFS3, 8.3.10 IFS4, 8.3.11 IFS5, 8.3.12 IFS6, 8.3.13 IFS7, 8.3.27 IPC5, 8.3.16 IEC2, 8.3.17 IEC3, 8.3.18 IEC4, 8.3.19 IEC5, 8.3.13 IFS7, 8.3.27 IPC5 , 8.3.28 IPC7, 8.3.31 IPC11, 8.3.32 IPC12, 8.3.33 IPC13, 8.3.34 IPC14, 8.3.35 IPC15, 8.3.37 IPC18, 8.3.38 IPC21, 8.3.39 IPC23, 8.3.42 IPC27, 8.3.43 IPC29, 8.3.44 INTTREG, 9.10.2 OSCTUN, 10.5.1 PMD1, 10.5.2 PMD3, 10.5.3 PMD4, 10.5.4 PMD5, 10.5.5 PMD7, 10.5.6 PMD8, 14.6.1 CCP1CON1L, 14.6.2 CCP1CON1H, 14.6.16 CCP2CON1L, 14.6.17 CCP2CON1H, 14.6.18 CCP2CON2L, 14.6.31 CCP3CON1L, 14.6.32 CCP3CON1H, 14.6.31 CCP3CON1L, 14.6.45 CCP4CON1H, 14.6.46 CCP4CON2L, 14.6.60 CCP5CON1H, 14.6.61 CCP5CON2L, 15.5.2 SPI1CON1H, 15.5.14 SPI2CON1H, 16.4.1 I2C1RCV, 20.1.4 CLC1SEL, 20.1.5 CLC1GLSL, 20.1.9 CLC2SEL, 20.1.14 CLC3SEL, 20.1.19 CLC4SEL, 21.4.16 AD1CON2 and 22.1.1 CMSTAT.
  - Adds 21.4.25 ANCFG.
  - Removes IPC6, IPC19, IPC20, IPC22, IPC25, IPC28 and PMD6.
- Tables:
  - Updates Table 1-1, Table 11-3, Table 14-2, Table 30-4, Table 30-5, Table 30-6, Table 30-7 and Table 30-20.
  - Removes 10-Bit DAC Specifications
- Figures:
  - Updates Figure 5-1 and Figure 9-1.

32.3 Revision C (December 2020)

This revision incorporates the following updates:

- Sections:
  - The I^2C and SPI standard uses the terminology “Master” and “Slave”. The equivalent Microchip terminology used in this document is “Host” and “Client”, respectively.
  - Updates Analog Features.
  - Updates all 28-Pin, 36-Pin and 48-Pin Package information.
- Registers:
  - Updates 17.8.1 U1MODE, 17.8.6 U2MODE and 27.1.6 FOSC.
- Tables:
  - Updates Table 30-3, Table 30-4, Table 30-5, Table 30-6, Table 30-7, Table 30-9, Table 30-11, Table 30-12, Table 30-13, Table 30-14 and Table 30-29.

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- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO. [X](1) –X /XX

Device — Tape and Reel — Temperature Range — Package

Device:	PIC24FJ64GU205, PIC24FJ64GU203, PIC24FJ64GU202, PIC24FJ32GU205, PIC24FJ32GU203, PIC24FJ32GU202, PIC24FJ64GP205, PIC24FJ64GP203, PIC24FJ64GP202, PIC24FJ32GP205, PIC24FJ32GP203, PIC24FJ32GP202	
Tape & Reel Option:	Blank	= Tube
	T	= Tape & Reel
Temperature Range:	I	= -40°C to +85°C (Industrial)
	E	= -40°C to +125°C (Extended)
Package:	PT	= 48-Lead TQFP
	M4	= 48-Lead UQFN
	M5	= 36-Lead UQFN
	SS	= 28-Lead SSOP
	SO	= 28-Lead SOIC
	ML	= 28-Lead QFN
	MV	= 28-Lead UQFN

Examples:

- PIC24FJ64GU205-I/PT: Industrial Temperature, 48-Lead TQFP Package

Notes:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.

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- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
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ISBN: 978-1-5224-7350-3

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