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PIC18F24/25Q10 Silicon Errata and Data Sheet Clarifications

PIC18F24/25Q10

Product Page Links

Introduction

The PIC18F24/25Q10 devices that you have received conform functionally to the current device data sheet (DS40001945**F**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F24/25Q10 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID	
		A8	B2
PIC18F24Q10	0x71C0	0xA008	0xA082
PIC18F25Q10	0x71A0	0xA008	0xA082

Important: Refer to the **Device/Revision ID** section in the current **"PIC18F2X/4XQ10 Memory Programming Specification"** (DS40001874) for more detailed information on Device Identification and Revision IDs for your specific device.

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Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions	
				A8	B2
Electrical Specifications	Temperature Range	1.1.1	Industrial Temperature Range Only	X	
I/O Ports	Ext $\overline{MCLR}$	1.2.1	Internal Pull-Up Enabled Late	X	X
Resets	LPBOR	1.3.1	Trip Point Rises with Temperature	X	
Resets	$\overline{RMCLR}$ Flag	1.3.2	POR may Clear the $\overline{RMCLR}$ bit by Mistake	X	X
Oscillator	HFINTOSC	1.4.1	5% Variation Over Temperature Range	X	
Oscillator	XT Mode	1.4.2	Maximum Clock Frequency Limited to 2 MHz for XT Mode	X	
ADCC	FVR Reference	1.5.1	Missing Codes when FVR is Used as Reference	X	X
WWDT	Window Operation	1.6.1	Window Feature of WWDT does not Operate Correctly in DOZE Mode	X	
NVM	NVMERR	1.7.1	The NVMERR bit is set by Device Reset after being Cleared by Software	X	
MSSP	SPI	1.8.1	SSPBUF may be Corrupted by Writes to Other GPR/SFRs	X	
In-Circuit Debug	Software Breakpoints	1.9.1	Software Breakpoints are not Available	X	X
PFM-Program Flash Memory	Self-Write	1.10.1	The First Instruction Following a Self-write Instruction may not Execute	X	X

Note: Only those issues indicated in the last column apply to the current silicon revision.

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1. Silicon Errata Issues

NOTICE This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1. Module: Electrical Specifications

1.1.1. Industrial Temperature Range Only

Extended temperature range devices are not released.

Work around

Operate at temperatures below 85 degrees C.

Affected Silicon Revisions

A8	B2
X	

1.2. Module: I/O Ports

1.2.1. Internal Pull-up on $\overline{\text{MCLR}}$ Pin Enabled Late

When the external master clear is selected, an internal pull-up feature is enabled. Because the internal pull-up feature happens later in the initialization sequence than expected, it can cause the device to become stuck in an initialization-Reset loop.

Work around

Use an external pull-up resistor on the $\overline{\text{MCLR}}$ pin when the external master clear configuration is selected.

Affected Silicon Revisions

A8	B2
X	X

1.3. Module: Resets

1.3.1. Low-Power Brown-out Reset (LPBOR) Mode

The Brown-out Reset trip level increases proportionally with temperature to a level where BOR is never released. LPBOR cannot be used reliably because the trip level relative to temperature is indeterminate.

Work around

Use the Normal-Power BOR mode.

Affected Silicon Revisions

A8	B2
X	

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1.3.2. The $\overline{\text{RMCLR}}$ Flag in the PCON0 Register Cleared by Mistake

On an initial power-up of the device or when executing a software Reset, the $\overline{\text{RMCLR}}$ flag in the PCON0 register may be improperly cleared by a Power-on Reset (POR) or software Reset ($\overline{\text{RI}}$), thereby indicating a false $\overline{\text{MCLR}}$ event.

Work around

None.

Affected Silicon Revisions

A8	B2
X	X

1.4. Module: Oscillator (OSC)

1.4.1. Internal HFINTOSC Oscillator Varies up to 5%

The internal HFINTOSC oscillator frequency varies up to 5% over the voltage and temperature range.

Work around

For systems requiring more precision, use an external crystal or ceramic resonator in one of the external oscillator modes.

Affected Silicon Revisions

A8	B2
X	

1.4.2. Maximum Clock Frequency Limited to 2 MHz for XT Mode

The maximum clock frequency for the intermediate gain setting that supports quartz crystal and ceramic resonator operation (XT mode) is being reduced from 4 MHz to 2 MHz.

Work around

For crystal or resonator frequencies above 2 MHz, use HS mode.

Affected Silicon Revisions

A8	B2
X	

1.5. Module: Analog-to-Digital Converter with Computation (ADCC)

1.5.1. Missing Codes with FVR Reference

Using the FVR as the positive voltage reference for the ADC can cause an increase in missing codes.

Work around

Method 1:

Increase the bit conversion time, known as T_{AD}, to 8 µs or higher.

Method 2:

Use V_{DD} as the positive voltage reference to the ADC.

Affected Silicon Revisions

A8	B2
X	X

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1.6. Module: Windowed Watchdog Timer (WWDT)

1.6.1. Window Operation in Doze Mode

When enabling the Windowed operation mode in Doze mode, a window violation error is issued even though the window is open and armed. This condition occurs only when the window size is set to a value other than 100% open.

Work around

Method 1:

Use the Windowed operation mode in any mode other than Doze. If disabling Doze mode is not an option, use the WWDT module without enabling the window.

Method 2:

If the device is in Doze mode, perform the arming process for the window in Normal mode and return to Doze mode.

Method 3:

If there is an Interrupt Service Routine (ISR) in the application code, the arming within the window can be done inside the ISR with the ROI bit of the CPUDOZE register being set.

Affected Silicon Revisions

A8	B2
X	

1.7. Module: Nonvolatile Memory (NVM)

1.7.1. NVMERR

When a Reset is issued while an NVM high-voltage operation is in progress, the NVMERR bit in the NVMCON0 register is set as expected. After clearing the NVMERR bit, if a Reset reoccurs, the NVMERR bit is set again regardless of whether an NVM operation is in progress or not. A successful write operation will clear the NVMERR condition.

Work around

None.

Affected Silicon Revisions

A8	B2
X	

1.8. Module: Host Synchronous Serial Port (MSSP)

1.8.1. MSSP SPI Client Mode

When operating in SPI Client mode, if the incoming SCK clock signal arrives during any of the conditions below, the SSPBUF Transmit Shift Register (TSR) may become corrupted. The byte transmitted to the client cannot be ensured to be correct, and the state of the WCOL bit may or may not indicate a write collision.

These conditions include:

- A write to an SFR
- A write to RAM following an SFR read
- A write to RAM before an SFR read

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Work around

Method 1 (Interrupt based using $\overline{SS}$):

1. Connect the $\overline{SS}$ line to both the $\overline{SS}$ input and either an INT or IOC input pin.
2. Enable INT or IOC interrupts (interrupt on falling edge if available, otherwise, check that $\overline{SS}$ == 0 when the interrupt occurs).
3. Load SSPBUF with the data to be transmitted.
4. Continue program execution.
5. When invoking the Interrupt Service Routine (ISR), do either of the following:
   a. Add a delay that ensures the first SCK clock will be complete, or
   b. Poll SSPSTAT.BF (while(BF == 0)) and wait for the transmission/reception to complete.

Method 2 (Bit polling based using $\overline{SS}$):

1. Load SSPBUF with the data to be transmitted.
2. Poll the $\overline{SS}$ line and wait for the $\overline{SS}$ to go active (while(!PORTx.$\overline{SS}$ == 0)).
3. When $\overline{SS}$ is active ($\overline{SS}$ == 0), do either of the following:
   a. Add a delay that ensures the first SCK clock will be complete, or
   b. Poll SSPSTAT.BF (while(BF == 0)) and wait for the transmission/reception to complete.

Once one of these two methods is complete, it is safe to return to program execution.

Method 3 ($\overline{SS}$ not available):

1. Load SSPBUF with the data to be transmitted.
2. Poll SSPSTAT.BF (while(BF == 0)) and wait for the transmission/reception to complete.

Affected Silicon Revisions

A8	B2
X	

1.9. Module: In-Circuit Debug

1.9.1. Software Breakpoints Are Not Available

When debugging code, software breakpoints will not be available.

Work around

None.

Affected Silicon Revisions

A8	B2
X	X

1.10. Module: Program Flash Memory (PFM)

1.10.1. The First Instruction Following a Self-Write Instruction May Not Execute

When performing a self-write operation to Program Flash Memory, the first instruction following a self-write instruction may not execute.

Work around

Add two all-zero `NOP()` macros immediately after the self-write instruction. The all-zero `NOP()` macros are included automatically when the `#include <xc.h>` directive is used in user software.

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Affected Silicon Revisions

A8	B2
X	X

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2. Data Sheet Clarifications

Note the following typographic corrections and clarifications for the latest version of the device data sheet (DS40001945**F**):

Note:

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1. Pin Diagrams

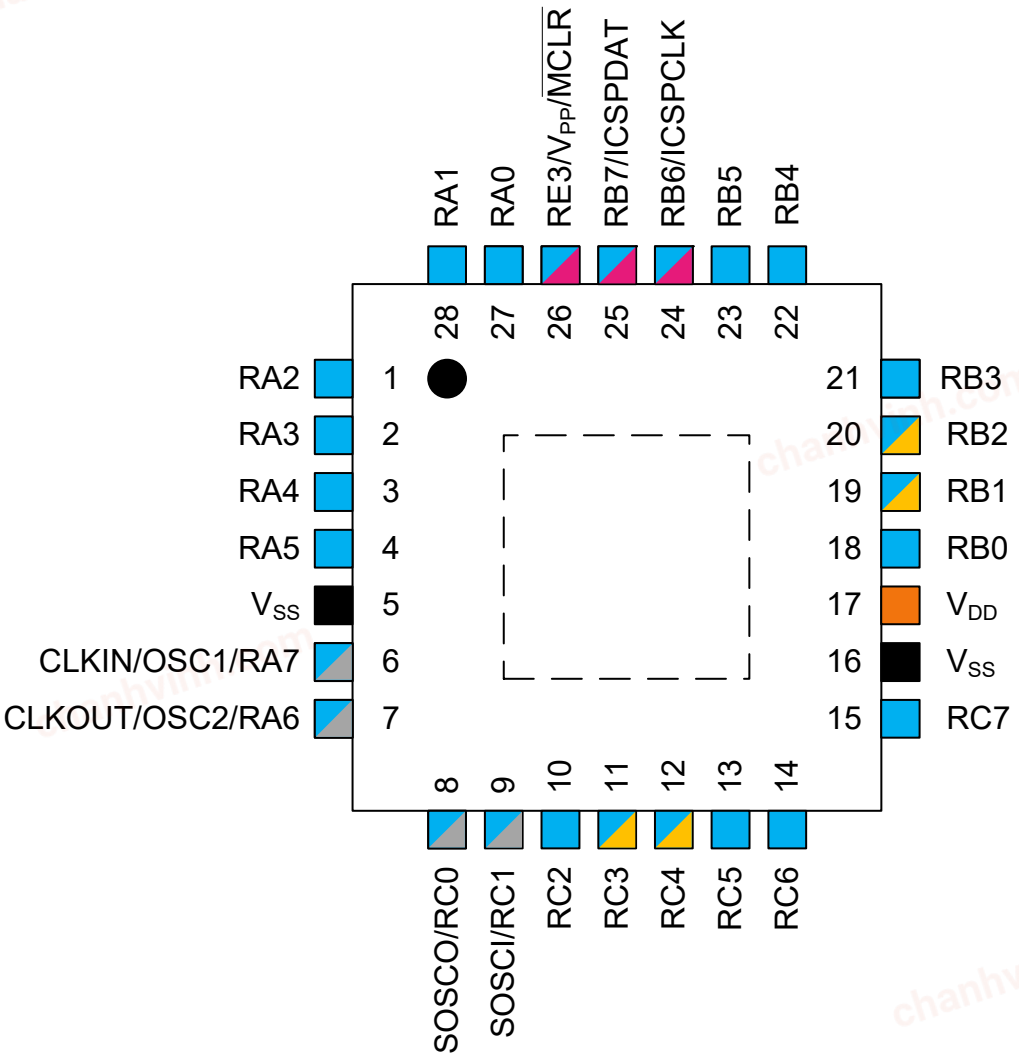
The pin diagrams for the 28-pin packages have changed. Figures 1-1 and 1-2 in the data sheet have been updated as follows:

28-Pin VQFN

28-Pin UQFN

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Power

- Power Supply
- Ground
- Pin on V_{DD} Power Domain

Functionality

- Programming/Debug
- Clock/Crystal
- I^2C/SMBus-compatible

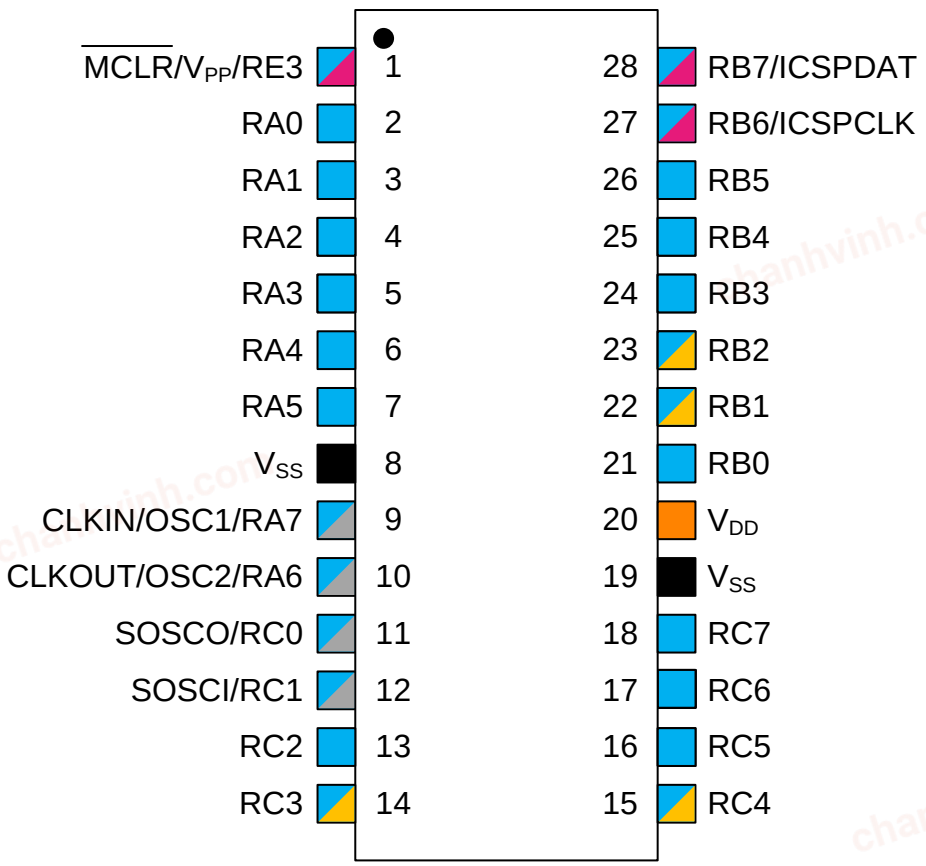
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28-Pin SPDIP

28-Pin SSOP

28-Pin SOIC



Power

- Power Supply
- Ground
- Pin on V_{DD} Power Domain

Functionality

- Programming/Debug
- Clock/Crystal
- I^2C/SMBus-compatible

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3. Appendix A: Revision History

Doc Rev.	Date	Comments
I	05/2026	Updated data sheet revision letter. Added data sheet clarification 2.1 for the 28-pin diagrams.
H	04/2024	Updated data sheet revision letter.
G	11/2022	Added silicon issue 1.10.1.
F	07/2021	Removed silicon issue 1.5.1. Minor editorial corrections.
E	02/2021	Added CVD issue for Rev B2 in Silicon Issue Summary table and Affected Silicon Revision in section 1.5.1.
D	01/2021	Added silicon erratum item 1.9.1.
C	11/2020	Added silicon revision B2. Minor editorial corrections.
B	08/2020	Updated Table 1. Added silicon errata items 1.3.2 and 1.4.2. Minor editorial corrections.
A	05/2018	Initial document release.

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