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PIC18F06/16Q20 Silicon Errata and Data Sheet Clarifications

PIC18F06/16Q20

Product Page Links

Introduction

The PIC18F06/16Q20 devices you have received conform functionally to the current device data sheet (DS40002387**E**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F06/16Q20 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID	
		B2	C0
PIC18F06Q20	0x7A60	0xA042	0xA080
PIC18F16Q20	0x7A40	0xA042	0xA080

Important: Refer to the **Device/Revision ID** section in the current **"PIC18FXXQ20 Family Programming Specification"** (DS40002327) for more detailed information on Device Identification and Revision IDs for your specific device.

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Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions	
				B2	C0
I²C	Bus Time-Out	1.1.1	CSTR Bit Is Not Cleared after Bus Time-Out	X	
	Bus Time-Out	1.1.2	MDR Bit Is Not Cleared after Bus Time-Out	X	
	Bus Time-Out	1.1.3	Bus Time-Out Not Detected Properly When External Host Clock Stretches	X	
	Bus Time-Out	1.1.4	Bus Time-Out Causes False Start/Stop	X	
	Clock Stretch	1.1.5	Clock Stretch Disable Not Working Properly	X	
	Clock Stretch	1.1.6	Clock Stretching Does Not Work When the I²C and I3C Modules Share the Same Pins	X	
	Bus Collision	1.1.7	Bus Collision Followed by a Stop Condition during a Transaction by an External Host Device May Hang the Bus	X	
	Multi-Host Arbitration	1.1.8	I²C Module May Hang the Bus during Multi-Host Arbitration	X	
I3C	Bus Available and Idle Timer	1.2.1	I3C Bus Available/Idle Timer Does Not Start Counting until IBI/HJREQ Is set	X	
	Static Address SDR Mode	1.2.2	Static Address Match Sets DADRIF Bit in Static Address SDR Mode	X	
	Device Status	1.2.3	Activity Mode and Protocol Error Bits Are Not Implemented in DSTAT0	X	
	Dynamic Address Assignment	1.2.4	Incorrect Dynamic Address Change Interrupt Operation	X	
	HDR Exit	1.2.5	Force HDR Exit Feature Is Not Functional	X	
	In-Band Interrupt/Hot-Join	1.2.6	In-Band Interrupt/Hot-Join NACK Causes the IBI/HJ Request to Be Canceled When a Bus Time-Out Occurs	X	
	In-Band Interrupt/Hot-Join	1.2.7	Passive Hot-Join/In-Band Interrupt may cause race condition to happen	X	
	Hot-Join	1.2.8	Hot-Join Does Not Work Properly When RETRY = 1	X	
	Hot-Join	1.2.9	Incorrect Hot-Join Operation after Controller ACKs and Sends Stop	X	
	Private Transaction One-Shot	1.2.10	Incorrect ACKPOS Operation with Direct CCC Write Transactions	X	
	Read/Write RNW Status Bits	1.2.11	RNW Status Bits Are Not Sticky and Are Set for Both ACK and NACK	X	
	Address Match Flags	1.2.12	DADRIF and SADRIF Flags Are Incorrectly Set for Direct CCCs and Private/I²C NACKs	X	
	Private/I²C Transaction Acknowledge	1.2.13	ACKP and ACKPOS Bits Are Not Functional for Private Read and I²C Read/Write Transactions	X	
	Target Reset	1.2.14	Target Reset Pattern Is Not Detected without a Preceding Start Condition	X	
	Target Reset	1.2.15	Unexpected RSTACT CCC Behavior with Certain Defining Bytes	X	
	Target Reset	1.2.16	Target Reset Pattern May Be Detected before a Stop Condition Occurs	X	
	Target Reset	1.2.17	BFREE Bit Not Set after Target Reset Pattern	X	
	CCC	1.2.18	Direct CCCs Read/Write from FIFO in I²C Mode	X	
	Transmit/Receive FIFO	1.2.19	TXFIFO and RXFIFO Are Not Cleared When the Module Is Enabled	X	
	Error Detection and Recovery	1.2.20	TE4 error not detected when module operates in I3C mode	X	
	Error Detection and Recovery	1.2.21	TE0/TE1 Error Detection cannot be turned off in I²C mode	X	
	Error Detection and Recovery	1.2.22	TE0 Error Detection does not take R/W bit into consideration	X	
ICSP™	Low-Voltage Programming	1.3.1	Low-Voltage Programming Not Possible	X	

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Table 2. Silicon Issue Summary (continued)

Module	Feature	Item No.	Issue Summary	Affected Revisions	
				B2	C0
UART	UART	1.4.1	UART TXDE Signal May Go Low before the STOP Bit Has Been Entirely Transmitted	X	
UTMR	Level-Triggered ERS Start/ Reset Condition	1.5.1	Dead Zone Exists in Level-Triggered Start/ Reset Condition When an ERS Signal Is Generated Due to an SFR Access	X	X
	Interrupts	1.5.2	Interrupts Do Not Work When Leaving Debug Mode	X	X
Electrical Specifications	Multi-Voltage I/O	1.6.1	Maximum MVIO Supply Voltage Is 3.63V	X	

Note: Only those issues indicated in the last column apply to the current silicon revision.

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1. Silicon Errata Issues

NOTICE This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1. Module: Inter-Integrated Circuit (I^2C)

1.1.1. CSTR Bit Is Not Cleared after Bus Time-Out

When the module is operating in Client mode and TOREC = 1, and a bus time-out occurs during clock stretching, the CSTR bit will not be cleared, and the module continues to clock stretch and hang the bus.

Work around

Reset the I^2C module by toggling the EN bit.

Affected Silicon Revisions

B2	C0
X	

1.1.2. MDR Bit Is Not Cleared after Bus Time-Out

In the Host mode of the I^2C module, when a bus time-out occurs during clock stretching and TOREC = 1, the MDR bit will not be cleared and a Stop will not be transmitted on the bus.

Work around

Force a Stop on the bus by setting the P bit upon bus time-out in Host mode. Forcing a Stop on the bus clears the MDR bit.

Affected Silicon Revisions

B2	C0
X	

1.1.3. Bus Time-Out Not Detected Properly When External Host Clock Stretches

When the module is operating in Client mode and an external Host device is clock stretching after the 8th SCL clock and a bus time-out occurs, the bus time-out is not detected properly. When the external Host times out before the Client and releases SCL to generate a Stop condition, the module continues to stretch SDA as if to generate an ACK and hangs the bus, and a Stop is never seen on the bus.

Work around

Reset the module by toggling the EN bit.

Affected Silicon Revisions

B2	C0
X	

1.1.4. Bus Time-Out Causes False Start/Stop

When the module is operating in Client mode and an external Host device is clock stretching, and a bus time-out occurs in the Client, the Client releases SDA and goes into the idle state. After the

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external Host generates a Stop condition on the bus by releasing SCL, the module can erroneously drive a low pulse on the SDA line, which acts as a false Start and Stop on the bus.

Work around

None.

Affected Silicon Revisions

B2	C0
X	

1.1.5. Clock Stretch Disable Not Working Properly

When the CSD bit is set between a Start condition and the 8th falling SCL edge, the I^{2}C module enters a state where the module clock stretches indefinitely after the next Start until a bus time-out occurs.

Work around

Force a reset of the module by toggling the EN bit.

Affected Silicon Revisions

B2	C0
X	

1.1.6. Clock Stretching Does Not Work When the I^{2}C and I3C Modules Share the Same Pins

When the I^{2}C module is used in conjunction with the I3C module using the same set of SDA and SCL pins, the I^{2}C module is unable to perform clock stretching in Client mode.

Work around

If clock stretching is desired, the I^{2}C module can use a different set of SDA/SCL pins.

Affected Silicon Revisions

B2	C0
X	

1.1.7. Bus Collision Followed by a Stop Condition During a Transaction by an External Host Device May Hang the Bus

In a Multi-Host environment, when another Host device on the bus causes a collision (BCLIF bit) and forces a Stop during a transaction, the I^{2}C module may not respond appropriately and may hang the bus.

Work around

When a Bus Collision (BCLIF) is detected along with a Stop condition (PCIF), reset the I^{2}C module by toggling the EN bit.

Affected Silicon Revisions

B2	C0
X	

1.1.8. I^{2}C Module May Hang the Bus During Multi-Host Arbitration

The I^{2}C module may hang the bus in a Multi-Host environment when another Host device initiates a transaction on the bus by issuing the Start condition before the I^{2}C module pulls down the SDA line, and the most significant bit of the address header starts with a '0' in FME = 0 or FME = 1 mode.

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Work around

When using FME = 0 or FME = 1 modes, the user can choose to assign addresses such that the most significant bit of the address header starts with a '1'. Alternatively, the user can select the FME = 2 mode of operation.

Affected Silicon Revisions

B2	C0
X	

1.2. Module: Improved Inter-Integrated Circuit (I3C)

1.2.1. I3C Bus Available/Idle Timer Does Not Start Counting until IBI/HJREQ Is Set

The internal Bus Available and Idle timers do not start counting after a Stop or Module Reset. The counter begins counting only after an In-Band Interrupt or Hot-Join is requested.

Work around

None.

Affected Silicon Revisions

B2	C0
X	

1.2.2. Static Address Match Sets DADRIF Bit in Static Address SDR Mode

When operating in Static Address SDR mode (SASDRMD = 1) and the module has been assigned a Dynamic Address, the module incorrectly sets DADRIF bit upon Static Address match.

Work around

None.

Affected Silicon Revisions

B2	C0
X	

1.2.3. Activity Mode and Protocol Error Bits Are Not Implemented

The Activity Mode ACTMODE bits and the Protocol Error PERR bit in the I3CxDSTAT0 register are read-only hardcoded to 0, which does not align with the MIPI I3C specification for GETSTATUS CCC.

Work around

None.

Affected Silicon Revisions

B2	C0
X	

1.2.4. Incorrect Dynamic Address Change Interrupt Operation

When the module does not have a Dynamic Address assigned and a RSTDAA CCC is received, the Dynamic Address Changed DACHIF bit is set incorrectly.

Work around

None.

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Affected Silicon Revisions

B2	C0
X	

1.2.5. Force HDR Exit Feature Is Not Functional

The Software Force HDR Exit FHDRE bit is not functional.

Work around

The module can exit HDR mode and go back to operating in SDR mode when the controller sends an HDR Exit Pattern on the bus.

Affected Silicon Revisions

B2	C0
X	

1.2.6. In-Band Interrupt/Hot-Join NACK Causes the IBI/HJ Request to Be Canceled When a Bus Time-Out Occurs

When the bus time-out is enabled (BTOEN = 1) and an In-Band Interrupt/Hot-Join request is NACK'd by the controller, an unexpected behavior is observed. When the controller does not follow the NACK with a Stop and a bus time-out happens, the BTOIF bit is set as expected. However, alongside the BTOIF, the IBIEIF/HJEIF error bit is also set erroneously, which clears the IBIREQ/HJREQ bit.

Work around

None.

Affected Silicon Revisions

B2	C0
X	

1.2.7. Passive Hot-Join/In-Band Interrupt May Cause Race Condition to Happen

When an external device on the bus requests a Hot-Join or In-Band Interrupt simultaneously when the I3C module requests arbitration (both devices pull the SDA line low very close to one another), a race condition may occur. When this happens, the module sends the first bit of the address, then releases the SDA line and does not continue to participate in arbitration.

Work around

None.

Affected Silicon Revisions

B2	C0
X	

1.2.8. Hot-Join Does Not Work Properly When RETRY = 1

If a Hot-Join request is NACK'd when the retry limit is 1 (I3CxRETRY = 1), the module may not exit the Hot-Join state and continue making more Hot-Join requests until the request is ACK'd by the controller. This behavior is similar to an unlimited retry limit (I3CxRETRY = 0).

Work around

The user should set a retry limit value greater than 1 (I3CxRETRY > 1).

Affected Silicon Revisions

B2	C0

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X	

1.2.9. Incorrect Hot-Join Operation after Controller ACKs and Sends Stop

The module behaves in an unexpected manner when the Controller ACKs a Hot-Join request and does not immediately follow up with an ENTDAA CCC in the same frame before a Stop occurs on the bus.

Work around

The Controller should send an ENTDAA immediately after it ACKs a Hot-Join request.

Affected Silicon Revisions

B2	C0
X	

1.2.10. Incorrect ACKPOS Operation with Direct CCC Write Transactions

A CCC Transaction should have no effect on the One-shot Private Transaction Acknowledge ACKPOS bit; however, a Direct CCC Write transaction incorrectly clears the ACKPOS bit. In addition, when ACKP = 0 and ACKPOS = 0, a Direct Write CCC request is incorrectly NACK'd by the module.

Work around

Re-arm the ACKPOS bit each time a Dynamic Address Match (DADRIF = 1) occurs.

Affected Silicon Revisions

B2	C0
X	

1.2.11. RNW Status Bits Are Not Sticky and Are Set for Both ACK and NACK

The RNW status bits should only be set when an address match occurs, and the module responds with an ACK. However, the RNW bits are being set for both ACK and NACK following an address match. In addition, the RNW bits should be sticky and maintain their values even after a Restart/Stop occurs on the bus, but they are being cleared at the end of a Private/I^2C transaction when a Restart/Stop occurs.

Work around

None.

Affected Silicon Revisions

B2	C0
X	

1.2.12. DADRIF and SADRIF Flags Are Incorrectly Set for Direct CCCs and Private/I^2C NACKs

The Static and Dynamic Address Match SADRIF/DADRIF flags should only be set when a Private/I^2C transaction is ACK'd by the module. However, the flags are also being set for Direct CCC transactions and when a Private/I^2C transaction is NACK'd by the module.

Work around

None.

Affected Silicon Revisions

B2	C0
X	

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1.2.13. ACKP and ACKPOS Bits Are Not Functional for Private Read and I²C Read/Write Transactions

The ACKP and ACKPOS bits are operational only for I3C Private Write transactions. The bits are not functional for I3C Private Read transactions or I²C Read/Write transactions.

Work around

None.

Affected Silicon Revisions

B2	C0
X	

1.2.14. Target Reset Pattern Is Not Detected without a Preceding Start Condition

When the bus is Idle (BFREE = 1), a Target Reset Pattern that is not preceded by a Start condition will not be detected on the bus.

Work around

None.

Affected Silicon Revisions

B2	C0
X	

1.2.15. Unexpected RSTACT CCC Behavior with Certain Defining Bytes

The RSTACT CCC behaves unexpectedly with certain defining bytes:

1. A Direct Read of the RSTACT CCC returns the contents of bits 1 and 0 only (two least significant bits) from the I3CxRSTACT register instead of returning all eight bits.
2. A Direct Read of the RSTACT CCC with defining bytes 0x80-0xFF returns 0xFF for 0x81-0x82 only and remains undefined for others.
3. A Direct Write of the RSTACT CCC with defining bytes 0x80-0xFF should be ignored, but the module incorrectly writes the defining byte to the I3CxRSTACT CCC register.
4. A Direct/Broadcast RSTACT CCC with defining bytes 0x03-0x04 should be NACK'd, but the module responds with an ACK.

Work around

None.

Affected Silicon Revisions

B2	C0
X	

1.2.16. Target Reset Pattern May Be Detected Before a Stop Condition Occurs

When a Target Reset Pattern occurs on the bus, the RSTDET and I3CxRIF bits should be set after the pattern ends with a Stop condition; however, the bits may be set after 14 SDA transitions but before the Stop condition occurs.

Work around

None.

Affected Silicon Revisions

B2	C0
X	

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1.2.17. BFREE Bit Not Set after Target Reset Pattern

The BFREE bit is cleared by hardware during a Target Reset Pattern; however, the module fails to set the bit after the Stop condition following the Target Reset Pattern, which causes the next transaction to be NACK'd. The BFREE bit is set after the Stop following the next transaction.

Work around

None.

Affected Silicon Revisions

B2	C0
X	

1.2.18. Direct CCCs Read/Write from FIFO in I²C Mode

When the module is operating in I²C mode (OPMD = `00`), a Direct CCC write using the static address erroneously writes data to the RXFIFO, and Direct CCC read erroneously reads data from the TXFIFO, if any; otherwise underflow error is set.

Work around

None.

Affected Silicon Revisions

B2	C0
X	

1.2.19. TXFIFO and RXFIFO Are Not Cleared When the Module Is Enabled

The TXFIFO and RXFIFO are not reset when the module is enabled. If there is any rogue data present in the FIFO, it will continue to be there even after the user disables/enables the module.

Work around

The user can explicitly clear the TXFIFO/RXFIFO using the CLRTXB and CLRRXB bits before enabling the module.

Affected Silicon Revisions

B2	C0
X	

1.2.20. TE4 Error Not Detected When Module Operates in I3C Mode

The module does not flag a TE4 error when it receives an ENTDAA CCC with a 7'h7E/W (instead of 7'h7E/R) when it is already operating in I3C mode (OPMD = `0bx1`).

Work around

None.

Affected Silicon Revisions

B2	C0
X	

1.2.21. TE0/TE1 Error Detection Cannot be Turned Off in I²C Mode

When the Bus Error Detection bit is set (BERRDET = `1`), the module is expected to detect TE0/TE1 errors in I3C mode only (OPMD = `0bx1`), however, the module detects TE0/TE1 in both I3C and I²C modes of operation.

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Work around

None. However, the I3C Controller on the bus can send an HDR Exit Pattern for error recovery if the target device appears unresponsive on the bus.

Affected Silicon Revisions

B2	C0
X	

1.2.22. TE0 Error Detection Does Not Take R/W Bit Into Consideration

An I3C Target should detect TE0 error by monitoring the bus for any of the following invalid combinations of Broadcast Address/W:

- 7'h3E/W
- 7'h5E/W
- 7'h6E/W
- 7'h76/W
- 7'h7A/W
- 7'h7C/W
- 7'h7F/W
- 7'h7E/R

With the exception of 7'h7E/R, the module flags a TE0 error immediately after the 7-bit address match happens, regardless of the status of the R/W bit.

Work around

None. However, the I3C Controller on the bus can send an HDR Exit Pattern for error recovery if the target device appears unresponsive on the bus.

Affected Silicon Revisions

B2	C0
X	

1.3. Module: Low-Voltage Programming (LVP)

1.3.1. Low-Voltage Programming Not Possible

Low-Voltage Programming is not possible when V_{DD} is below the selected BORV voltage level while BOR is enabled.

Work Around

Method 1:

Disable BOR to use Low-Voltage Programming.

Method 2:

Raise V_{DD} above the selected BORV level while using Low-Voltage Programming.

Affected Silicon Revisions

B2	C0
X	

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1.4. Module: Universal Asynchronous Receiver Transmitter (UART)

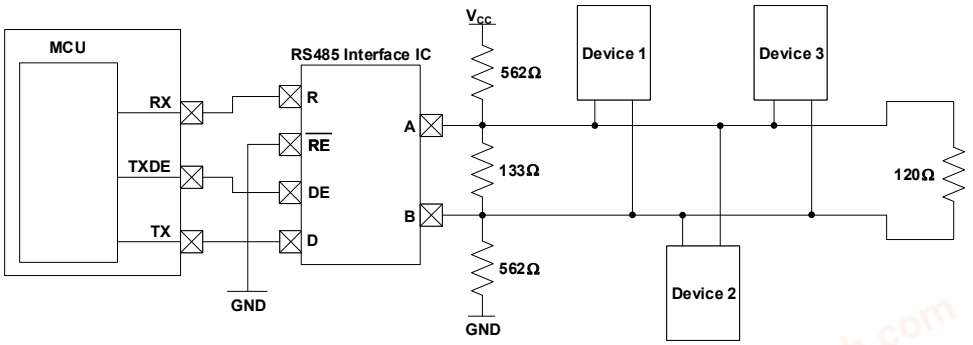
1.4.1. UART TXDE Signal May Go Low Before the STOP Bit Has Been Entirely Transmitted

The UART Transmit Drive Enable (TXDE) signal could potentially transition into a low state before the UART Stop bit has been entirely transmitted due to the effects of parasitic capacitance on the TX line. In some applications, this could result in communication being prematurely terminated due to the TXDE signal going low before the STOP bit has had enough time to settle.

Work Around

To ensure that the Stop bit settles into its final logic state before the TXDE signal transitions low, a biasing circuit can be implemented. A biasing circuit allows the TX line to either be driven high or low, rather than being left in a floating tri-state mode, where prolonged rise or fall times could lead to communication being disrupted. This bias circuit must only be implemented on one end of the serial bus, and a termination resistor must be used on the other end. The figure below shows an example of a bias circuit that can be used to achieve this.

Please note that the resistor values used in this circuit are recommendations and that the actual resistor values required may vary based on the application.



Affected Silicon Revisions

B2	C0
X	

1.5. Module: Universal Timer (UTMR) Module

1.5.1. Dead Zone Exists in Level-Triggered Start/Reset Condition When an ERS Signal Is Generated Due to an SFR Access

When a level-triggered Start/Reset condition (START = `'b11` or RESET = `'b01`) is triggered by an ERS signal generated by an SFR access, such as TUxyPRL_Write or TUxyTMRL_Read or TUxyCRL_Read (TUxyERS = 0x3E or 0x3F), there exists a dead zone in which subsequent SFR accesses will be missed. This dead zone is the period between the ZIF flag being set and the timer starting to count again. This can be monitored by checking either the RUN status bit or the level output of the timer.

Work Around

The user must wait for the timer to start counting before accessing the period, counter and capture registers again.

Affected Silicon Revisions

B2	C0
X	X

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1.5.2. Interrupts Do Not Work When Leaving Debug Mode

The Universal Timer interrupts do not work after the user exits a debug session.

Work around

Toggle the PMD bit for the corresponding instance of UTMR at the beginning of `main()` before initializing the module.

Affected Silicon Revisions

B2	C0
X	X

1.6. Module: Electrical Specifications

1.6.1. Maximum MVIO Supply Voltage Is 3.63V

MVIO power supply on V_{DDIOx} pin is limited to a maximum of 3.63V

Work around

None.

Affected Silicon Revisions

B2	C0
X	

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2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002387**E**):

Note:

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1. None

There are no known data sheet clarifications as of this publication date.

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3. Appendix A: Revision History

Doc. Rev.	Date	Comments
D	10/2025	Updated data sheet revision to E; minor grammatical corrections.
C	7/2024	Correct Revision IDs. Added silicon revision C0.
B	3/2024	Adds new I3C silicon issues 1.2.7 and 1.2.20 through 1.22; items 1.2.7 through 1.2.18 in revision A renumbered as 1.2.8 through 1.2.19. Minor editorial corrections.
A	9/2023	Initial document release.

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