chanhvinh.com

PIC18F04/05/14/15Q20 Silicon Errata and Data Sheet Clarifications

PIC18F04/05/14/15Q20

Product Page Links

Introduction

The PIC18F04/05/14/56Q20 devices you have received conform functionally to the current device data sheet (DS40002570**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F04/05/14/15Q20 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID
		A0
PIC18F04Q20	0x7AE0	0xA000
PIC18F05Q20	0x7AA0	0xA000
PIC18F14Q20	0x7AC0	0xA000
PIC18F15Q20	0x7A80	0xA000

Important: Refer to the **Device/Revision ID** section in the current **"PIC18FXXQ20 Family Programming Specification"** (DS40002327) for more detailed information on Device Identification and Revision IDs for your specific device.

© 2024-2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions
				A0
I3C	Error Detection and Recovery	1.1.1	TE4 error not detected when module operates in I3C mode	X
	Error Detection and Recovery	1.1.2	TE0/TE1 Error Detection cannot be turned off in I^2C mode	X
	Error Detection and Recovery	1.1.3	TE0 Error Detection does not take R/W bit into consideration	X
	In-Band Interrupt/Hot-Join	1.1.4	Passive Hot-Join/In-Band Interrupt may cause race condition to happen	X
UTMR	Level-Triggered ERS Start/Reset Condition	1.2.1	Dead Zone Exists in Level-Triggered Start/Reset Condition When an ERS Signal Is Generated Due to an SFR Access	X
	Interrupts	1.2.2	Interrupts Do Not Work When Leaving Debug Mode	X

Note: Only those issues indicated in the last column apply to the current silicon revision.

© 2024-2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

1. Silicon Errata Issues

NOTICE This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1. Module: Improved Inter-Integrated Circuit (I3C)

1.1.1. TE4 Error Not Detected When Module Operates in I3C Mode

The module does not flag a TE4 error when it receives an ENTDAA CCC with a 7'h7E/W (instead of 7'h7E/R) when it is already operating in I3C mode (OPMD = `0bx1`).

Work around

None.

Affected Silicon Revisions

A0
X

1.1.2. TE0/TE1 Error Detection Cannot be Turned Off in I^2C Mode

When the Bus Error Detection bit is set (BERRDET = `1`), the module is expected to detect TE0/TE1 errors in I3C mode only (OPMD = `0bx1`), however, the module detects TE0/TE1 in both I3C and I^2C modes of operation.

Work around

None. However, the I3C Controller on the bus can send an HDR Exit Pattern for error recovery if the target device appears unresponsive on the bus.

Affected Silicon Revisions

A0
X

1.1.3. TE0 Error Detection Does Not Take R/W Bit Into Consideration

An I3C Target should detect TE0 error by monitoring the bus for any of the following invalid combinations of Broadcast Address/W:

- 7'h3E/W
- 7'h5E/W
- 7'h6E/W
- 7'h76/W
- 7'h7A/W
- 7'h7C/W
- 7'h7F/W
- 7'h7E/R

With the exception of 7'h7E/R, the module flags a TE0 error immediately after the 7-bit address match happens, regardless of the status of the R/W bit.

© 2024-2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

Work around

None. However, the I3C Controller on the bus can send an HDR Exit Pattern for error recovery if the target device appears unresponsive on the bus.

Affected Silicon Revisions

A0
X

1.1.4. Passive Hot-Join/In-Band Interrupt May Cause Race Condition to Happen

When an external device on the bus requests a Hot-Join or In-Band Interrupt simultaneously when the I3C module requests arbitration (both devices pull the SDA line low very close to one another), a race condition may occur. When this happens, the module sends the first bit of the address, then releases the SDA line and does not continue to participate in arbitration.

Work around

None.

Affected Silicon Revisions

A0
X

1.2. Module: Universal Timer (UTMR) Module

1.2.1. Dead Zone Exists in Level-Triggered Start/Reset Condition When an ERS Signal Is Generated Due to an SFR Access

When a level-triggered Start/Reset condition (START = `'b11` or RESET = `'b01`) is triggered by an ERS signal generated by an SFR access, such as TUxyPRL_Write or TUxyTMRL_Read or TUxyCRL_Read (TUxyERS = 0x3E or 0x3F), there exists a dead zone in which subsequent SFR accesses will be missed. This dead zone is the period between the ZIF flag being set and the timer starting to count again. This can be monitored by checking either the RUN status bit or the level output of the timer.

Work Around

The user must wait for the timer to start counting before accessing the period, counter and capture registers again.

Affected Silicon Revisions

A0
X

1.2.2. Interrupts Do Not Work When Leaving Debug Mode

The Universal Timer interrupts do not work after the user exits a debug session.

Work around

Toggle the PMD bit for the corresponding instance of UTMR at the beginning of `main()` before initializing the module.

Affected Silicon Revisions

A0
X

© 2024-2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002570**B**):

Note:

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1. None

There are no known data sheet clarifications as of this publication date.

© 2024-2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

3. Appendix A: Revision History

Doc Rev.	Date	Comments
B	10/2025	Updated data sheet revision to B; minor grammatical corrections.
A	5/2024	Initial document release. Includes silicon issues 1.1.1 through 1.1.4 (I3C) and 1.2.1 and 1.2.2 (UTMR).

© 2024-2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

Microchip Information

Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at https://www.microchip.com/en-us/about/legal-information/microchip-trademarks.

ISBN: 979-8-3371-1808-6

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP “AS IS”. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP’S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip products are strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

© 2024-2025 Microchip Technology Inc. and its subsidiaries

chanhvinh.com

Product Page Links

PIC18F04Q20, PIC18F05Q20, PIC18F14Q20, PIC18F15Q20

© 2024-2025 Microchip Technology Inc. and its subsidiaries