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PIC18F27/47/57Q83 Silicon Errata and Data Sheet Clarifications

PIC18F27/47/57Q83

Product Page Links

Introduction

The PIC18F27/47/57Q83 devices that you have received conform functionally to the current device data sheet (DS40002265**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F27/47/57Q83 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID			
		B3	B4	B5	C0
PIC18F27Q83	0x9909	0xA043	0xA044	0xA045	0xA080
PIC18F47Q83	0x990A	0xA043	0xA044	0xA045	0xA080
PIC18F57Q83	0x990B	0xA043	0xA044	0xA045	0xA080

Important: Refer to the **Device/Revision ID** section in the current **"PIC18-Q83/84 Family Programming Specification"** (DS40002137) for more detailed information on Device Identification and Revision IDs for a specific device.

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Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions			
				B3	B4	B5	C0
UTMR	Hardware Reset condition	1.1.1	Reset does not happen at period match when the prescaler > 0	X			
	Level-triggered ERS Start/Reset condition	1.1.2	Dead zone exists in level-triggered Start/Reset condition when an ERS signal is generated due to an SFR access	X	X	X	X
	Hardware Reset condition	1.1.3	Reset does not happen at period match when the prescaler > 0 and the timer stops at period match (includes One Shot mode)	X	X	X	X
	Pulse output	1.1.4	Pulse output does not occur at period match when the prescaler = 1		X	X	X
	Clear command	1.1.5	Clear Command may not work properly	X	X	X	X
I^2C	Start and Stop interrupt function	1.2.1	The I^2C Start and/or Stop flags may be set when I^2C is enabled	X	X	X	X
	Clock Stretching	1.2.3	CSTR bit will not clear after a bus time-out	X	X	X	X
	Bus free divider ratio	1.2.2	BFREDR =1 mode is nonfunctional	X	X	X	X
	Host data request	1.2.4	MDR bit will not clear after a bus time-out	X	X	X	X
	Clock stretching	1.2.5	Bus time-out not detected during clock stretching	X	X	X	X
	Clock stretching	1.2.6	Disabling clock stretching can fail with specific timing	X	X	X	X
	Multi-Host mode	1.2.7	Bus collisions can hang the bus in mult-host mode	X	X	X	X
	Clock Stretching	1.2.8	I2CCNT value may be corrupted if written to during clock stretching	X	X	X	X
SMT	Reset bit	1.3.1	SMT stops working if RST is set while the prescaler setting is not zero	X	X	X	X
ADCC with Context	Double sample conversions	1.4.1	An unexpected acquisition time is added between the first and second conversion	X	X	X	X
PIC18 Core	FSR shadow registers	1.5.1	FSR shadow registers are not writable	X	X	X	X
UART	Stop bit	1.6.1	TXDE signal may go low before the Stop bit has been entirely transmitted	X	X	X	X
ICD	Single-Step (SSTEP) function	1.7.1	Single Step function does not execute at Software Breakpoint	X	X	X	X
PWM	PWM mode	1.8.1	Wrong duty cycle for the CCP module	X	X	X	X
ICSP™	Low-Voltage Programming (LVP)	1.9.1	Low-Voltage Programming is not possible when V_{DD} is below BORV while BOR is enabled	X	X	X	X
CAN	Masks/Filters	1.10.1	Filters 8–11 will erroneously accept incoming messages with SID of 0x000	X	X	X	
Instruction Set	`PUSHL` instruction	1.11.1	The `PUSHL` instruction executes incorrectly	X	X	X	X
Timer 1	Gate Interrupt	1.12.1	Writing to the gate source select may set the gate interrupt flag	X	X	X	X
Memory	DIA	1.13.1	The TSLR2 and TSHR2 Values Stored in the DIA Table are Incorrect	X	X	X	X

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Table 2. Silicon Issue Summary (continued)

Module	Feature	Item No.	Issue Summary	Affected Revisions			
				B3	B4	B5	C0
Capture/ Compare/ PWM (CCP)	Compare Toggle Mode	1.14.1	CCP Compare Toggle Output Mode Does Not Work as Expected	X	X	X	X
Power-Saving Modes	XLP Power Mode	1.15.1	XLP Power Mode Does Not Work as Expected	X	X	X	X

Note: Only issues indicated in the last column apply to the current silicon revision.

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1. Silicon Errata Issues

NOTICE This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1. Module: Universal Timer (UTMR) Module

1.1.1. Reset Does Not Happen at Period Match When the Prescaler > 0

When the prescaler > 0 and a hardware-based Reset event is selected (RESET = 'b01 or 'b10 or 'b11), the timer does not reset at period match.

Work Around

1. Use prescaler = 0, or
2. When using prescaler > 0, clear the timer in software using the CLR command at every PR match interrupt.

Affected Silicon Revisions

B3	B4	B5	**C0**				
X							

1.1.2. Dead Zone Exists in Level-Triggered Start/Reset Condition When an ERS Signal Is Generated Due to an SFR Access

When a level-triggered Start/Reset condition (START = 'b11 or RESET = 'b01) is triggered by an ERS signal generated by an SFR access, such as TUxyPRL_Write or TUxyTMRL_Read or TUxyCRL_Read (TUxyERS = 0x3E or 0x3F), there exists a dead zone in which subsequent SFR accesses will be missed. This dead zone is the period between the ZIF flag being set and the timer starting to count again. This can be monitored by checking either the RUN status bit or the level output of the timer.

Work Around

The user must wait for the timer to start counting before accessing the period, counter and capture registers again.

Affected Silicon Revisions

B3	B4	B5	**C0**				
X	X	X	**X**				

1.1.3. Reset Does Not Happen at Period Match When the Prescaler > 0 and the Timer Stops at Period Match

When the prescaler > 0 and the timer is configured to reset at a hardware-based event (RESET = 'b01 or 'b10 or 'b11) and stop at period match (STOP = 'b11), the timer stops at period match but does not reset (no pulse output occurs and the ZIF interrupt is not generated).

Work Around

1. Use prescaler = 0, or
2. When using prescaler > 0, clear the timer in software using the CLR command at every PR match interrupt.

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Affected Silicon Revisions

B3	B4	B5	**C0**				
X	X	X	**X**				

1.1.4. Pulse Output Does Not Occur at Period Match When the Prescaler = 1

The timer output pulse will not occur at period match when prescaler = 1.

Work Around

Use prescaler = 0 or prescaler > 1 when a pulse output is desired.

Affected Silicon Revisions

B3	B4	B5	**C0**				
	X	X	**X**				

1.1.5. Clear Command May Not Work Properly in Asynchronous Mode

When operating in Asynchronous mode (CSYNC = `0`), setting the Clear Command bit (CLR= `1`) may not clear the Timer Counter register value.

Work Around

Use the Universal Timer module in Synchronous mode (CSYNC = `1`) when the Clear Command bit (CLR) is being used.

Affected Silicon Revisions

B3	B4	B5	**C0**				
X	X	X	**X**				

1.1.6. Interrupts Do Not Work When Leaving Debug Mode

The Universal Timer interrupts do not work after the user exits a debug session.

Work around

Toggle the PMD bit for the corresponding instance of UTMR at the beginning of `main()` before initializing the module.

Affected Silicon Revisions

B3	B4	B5	**C0**				
X	X	X	**X**				

1.2. Module: Inter-Integrated Circuit (I^2C)

1.2.1. The I^2C Start and/or Stop Flags May Be Set When I^2C Is Enabled

When I^2C is enabled, erroneous Start and/or Stop conditions may be detected. This can generate erroneous I^2C interrupts, if enabled.

Work Around

Use the following procedure to correctly detect the Start and Stop conditions:

1. Disable the Start and Stop conditions interrupt functions.
2. Enable the I^2C module.
3. Wait 250 ns + six instruction cycles ($F_{OSC}/4$).
4. Clear the Start and Stop conditions interrupt flags.

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5. Enable the Start and Stop conditions interrupt functions, if used.

```
I2CxPIEbits.SCIE = 0;         // Disable Start condition interrupt
I2CxPIEbits.PCIE = 0;         // Disable Stop condition interrupt
I2CxCON0bits.EN = 1;          // Enable I2C
Delay();                      // Wait for 250 ns + 6 instruction cycles (FOSC/4)
I2CxPIRbits.SCIF = 0;         // Clear the Start condition interrupt flags
I2CxPIRbits.PCIF = 0;         // Clear the Stop condition interrupt flags
I2CxPIEbits.SCIE = 1;         // Enable Start condition interrupt if used
I2CxPIEbits.PCIE = 1;         // Enable Stop condition interrupt if used
```

Affected Silicon Revisions

B3	B4	B5	**C0**				
X	X	X	**X**				

1.2.2. The Bus Free Divider Ratio BFREDR = 1 Value Is Not Functional

Setting the Bus Free Divider Ratio bit (BFREDR = 1) has no effect on the Bus Free Time Divider ratio.

Work around

Maintain BFREDR = 0 at all times.

Affected Silicon Revisions

B3	B4	B5	**C0**				
X	X	X	**X**				

1.2.3. CSTR Bit Is Not Cleared after Bus Time-Out

When the module is operating in Client mode and TOREC = 1, and a bus time-out occurs during clock stretching, the CSTR bit will not be cleared, and the module continues to clock stretch and hang the bus.

Work around

Reset the I^2C module by toggling the EN bit.

Affected Silicon Revisions

B3	B4	B5	**C0**				
X	X	X	**X**				

1.2.4. MDR Bit Is Not Cleared after Bus Time-Out

In the Host mode of the I^2C module, when a bus time-out occurs during clock stretching and TOREC = 1, the MDR bit will not be cleared and a Stop will not be transmitted on the bus.

Work around

Force a Stop on the bus by setting the P bit upon bus time-out in Host mode. Forcing a Stop on the bus clears the MDR bit.

Affected Silicon Revisions

B3	B4	B5	**C0**				
X	X	X	**X**				

1.2.5. Bus Time-Out Not Detected Properly When External Host Clock Stretches

When the module is operating in Client mode and an external Host device is clock stretching after the 8th SCL clock and a bus time-out occurs, the bus time-out is not detected properly. When the external Host times out before the Client and releases SCL to generate a Stop condition, the module continues to stretch SDA as if to generate an ACK and hangs the bus, and a Stop is never seen on the bus.

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Work around

Reset the module by toggling the EN bit.

Affected Silicon Revisions

B3	B4	B5	**C0**				
X	X	X	**X**				

1.2.6. Clock Stretch Disable Not Working Properly

When the CSD bit is set between a Start condition and the 8th falling SCL edge, the I^2C module enters a state where the module clock stretches indefinitely after the next Start until a bus time-out occurs.

Work around

Force a reset of the module by toggling the EN bit.

Affected Silicon Revisions

B3	B4	B5	**C0**				
X	X	X	**X**				

1.2.7. Bus Collision Followed by a Stop Condition During a Transaction by an External Host Device May Hang the Bus

In a Multi-Host environment, when another Host device on the bus causes a collision (BCLIF bit) and forces a Stop during a transaction, the I^2C module may not respond appropriately and may hang the bus.

Work around

When a Bus Collision (BCLIF) is detected along with a Stop condition (PCIF), reset the I^2C module by toggling the EN bit.

Affected Silicon Revisions

B3	B4	B5	**C0**				
X	X	X	**X**				

1.2.8. Writing to the I2CCNT Register During Clock Stretching May Corrupt the I2CCNT Value

The I2CCNT register value may be corrupted when user software writes to the I2CCNT register during clock stretching triggered by the one of the following conditions:

- Host transmission (MMA = `1`; TXBE = `1`; I2CCNT != `0`)
- Host reception (MMA = `1`; RXBF = `1`)
- Client transmission (SMA = `1`; TXBE = `1`; I2CCNT != `0`)
- Client reception (SMA = `1`; RXBF = `1`)

Work around

User software should not write to the I2CCNT register during clock stretching triggered by the above-mentioned conditions.

Affected Silicon Revisions

B3	B4	B5	**C0**				
X	X	X	**X**				

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1.3. Module: Signal Measurement Timer (SMT)

1.3.1. Reset Bit

If the SMT clock prescaler is set to any value other than '00', setting the RST bit will cause the module to stop working. The RST bit will remain at the value '1', the counter will not increment, and no interrupts will be generated. The problem is cleared by turning the module off and on or by performing a device reset.

Work Around
Method 1:

Do not set the RST bit; manual reset is usually not required for typical operation because the measurement logic will reset the counter automatically.

Method 2:

Write zero to the counter manually. Either disable the module or the clock before using this method.

Method 3:

Use 1:1 prescaler (PS = 00).

Method 4:

Use the CLKREF subsystem to provide a prescaled clock and set PS = 00.

Affected Silicon Revisions

B3	B4	B5	**C0**				
X	X	X	**X**				

1.4. Module: Analog-to-Digital (ADC) With Computation and Context Switching

1.4.1. An Unexpected Acquisition Time is Added Between the First and Second Conversions

When enabling a Double Sample Conversion (DSEN = 1) with no precharge time (ADPRE = 0) and no acquisition time (ADACQ = 0), the maximum number of cycles of acquisition time is inserted prior to the second conversion. The first conversion will be performed as expected with no precharge time and no acquisition time. It is only between the first and second conversions where a maximum number of cycles of acquisition time are performed unexpectedly.

Work Around
Method 1:

Disable Double Sample Conversion (DSEN = 0) and perform two single conversions back to back.

Method 2:

If adding acquisition time is acceptable, then select no precharge time along with the desired acquisition time.

Affected Silicon Revisions

B3	B4	B5	**C0**				
X	X	X	**X**				

1.5. Module: PIC18 Core

1.5.1. FSR Shadow Registers Are Not Writable

Writing to the FSR shadow registers does not result in accurate values being stored in the registers. Consequently, reading the FSR shadow registers after they have been written will return inaccurate data.

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Work Around

Writes to the FSR shadow registers can be performed safely using the following steps:

1. Save regular FSR2 value into RAM.
2. Write the regular FSR2 with the targeted value minus the computed offset (IR[6:0] + 1, see below).
3. Write the shadow FSRxL (data doesn't matter); this will clock the shadow FSR with the FSR computed offset value.
4. Decrement FSR2 value by 1, since FSRxH increments the address by 1 (IR[6:0]).
5. Write FSRxH.
6. Restore the regular FSR2 from the stored RAM value.

The FSR shadow will have the desired value and the regular FSR will have the original value.

Affected Silicon Revisions

B3	B4	B5	**C0**				
X	X	X	**X**				

1.6. Module: Universal Asynchronous Receiver Transmitter (UART)

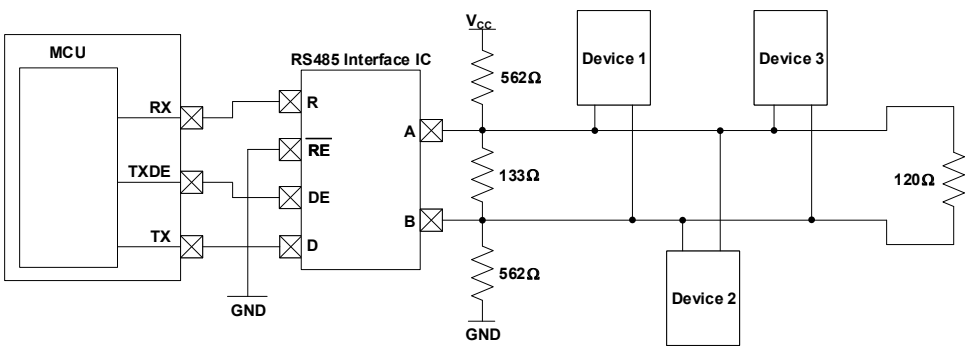
1.6.1. UART TXDE Signal May Go Low Before the STOP Bit Has Been Entirely Transmitted

The UART Transmit Drive Enable (TXDE) signal could potentially transition into a low state before the UART Stop bit has been entirely transmitted due to the effects of parasitic capacitance on the TX line. In some applications, this could result in communication being prematurely terminated due to the TXDE signal going low before the STOP bit has had enough time to settle.

Work Around

To ensure that the Stop bit settles into its final logic state before the TXDE signal transitions low, a biasing circuit can be implemented. A biasing circuit allows the TX line to either be driven high or low, rather than being left in a floating tri-state mode, where prolonged rise or fall times could lead to communication being disrupted. This bias circuit must only be implemented on one end of the serial bus, and a termination resistor must be used on the other end. The figure below shows an example of a bias circuit that can be used to achieve this.

Please note that the resistor values used in this circuit are recommendations and that the actual resistor values required may vary based on the application.



Affected Silicon Revisions

B3	B4	B5	**C0**				
X	X	X	**X**				

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1.7. Module: In-Circuit Debug

1.7.1. Single-Step Function Does Not Execute at SW Breakpoint

The SW breakpoint occurs, but the SSTEP function does not execute at the breakpoint.

Work Around

None.

Affected Silicon Revisions

B3	B4	B5	**C0**				
X	X	X	**X**				

1.8. Module: Pulse-Width Modulation (PWM)

1.8.1. Wrong Duty Cycle for CCP Module

While in PWM mode and with the Timer2 prescaler configured to 1:1, the duty cycle of the PWM output is as expected. When the Timer2 prescaler is changed to a value other than 1:1 while T2PR = 0 (PWM resolution of two bits), the expected duty cycle is wrong. The corrected duty cycle values are shown in the table below.

Table 1-1. Corrected Duty Cycle Values

Prescaler/CCPR	0	1	2	3	4
1:1	0%	25%	50%	75%	100%
1:2	50%	75%	50%	75%	100%
1:4...1:128	75%	75%	75%	75%	100%

Work Around

None.

Affected Silicon Revisions

B3	B4	B5	**C0**				
X	X	X	**X**				

1.9. Module: Low-Voltage Programming (LVP)

1.9.1. Low-Voltage Programming Not Possible

Low-Voltage Programming is not possible when V_{DD} is below the selected BORV voltage level while BOR is enabled.

Work Around

Method 1:

Disable BOR to use Low-Voltage Programming.

Method 2:

Raise V_{DD} above the selected BORV level while using Low-Voltage Programming.

Affected Silicon Revisions

B3	B4	B5	**C0**				
X	X	X	**X**				

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1.10. Module: Controller Area Network (CAN) Module

1.10.1. Filters 8–11 Will Erroneously Accept Incoming Messages With SID of 0x000

When using the CAN RX filters 8–11, any messages where the incoming message (after masking) is SID 0x000 will trigger a filter match, regardless of the filter ID settings. For example: an incoming message with ID of 0x350 and a mask setting of 0x00F will trigger a filter match regardless of other mask/filter settings. This will occur even if the filter is set to only accept extended IDs.

Work Around

If using CAN RX filters 8–11, check the FILHIT bits of C1VECH (or the received message object) upon message reception. If the value of FILHIT is greater than 11, then this error has occurred and the message can be ignored and discarded.

Affected Silicon Revisions

B3	B4	B5	**C0**				
X	X	X					

1.11. Module: Instruction Set

1.11.1. The PUSHL Instruction Executes Incorrectly

The PUSHL instruction of the PIC18 Extended Instruction Set incorrectly executes when FSR2 is loaded with certain values.

Work Around

Do not use PUSHL when FSR2 is loaded with any of the following values:

- 0xDB
- 0xDC
- 0xDE
- 0xE3
- 0xE4
- 0xE6
- 0xEB
- 0xEC
- 0xEE

Affected Silicon Revisions

B3	B4	B5	**C0**				
X	X	X	**X**				

1.12. Module: Timer1

1.12.1. Changing the Timer1 Gate Source May Cause Unexpected Interrupts

When a new value is written into the Timer1 Gate Source Select (GSS) bits of the TxGATE register, the TMRxGIF interrupt flag may be set unexpectedly. If the TMRxGIE bit is set, an unexpected interrupt will occur.

Work around

User software must clear the TMRxGIF bit immediately after writing the new value to the GSS bits.

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Affected Silicon Revisions

B3	B4	B5	C0				
X	X	X	X				

1.13. Module: Memory

1.13.1. The TSLR2 and TSHR2 Values Stored in the DIA Table Are Incorrect

The Temperature Indicator Low Range (TSLR2) and Temperature Indicator High Range (TSHR2) measurement values stored in the Device Information Area (DIA) in Program Memory are incorrect and should not be used to calculate the device die temperature.

Work Around

The following steps can be used to measure the die temperature (T_{MEAS}):

1. Place the device in a temperature-controlled environment and allow the device to reach the desired steady-state temperature.
2. Ensure that the device operating voltage (V_{DD}) is 3.0V, and the ADC positive reference voltage ($V_{REF}+$) is 2.048V (the Gain and Offset values of the DIA table are measured with these parameters).
3. Obtain the ADC count value of the measured analog voltage: The analog output voltage, V_{MEAS}, is converted to a digital count value by the Analog-to-Digital Converter (ADC) and is referred to as ADC_{MEAS}.
4. Obtain the Gain value from the DIA table. This parameter is TSLR1 for the low range setting or TSHR1 for the high range setting of the temperature indicator module.
5. Obtain the Offset value from the DIA table. This parameter is TSLR3 for the low range setting or TSHR3 for the high range setting of the temperature indicator module.

The following equation provides an estimate for the die temperature based on the above parameters:

Equation 1-1. Die Temperature (in °C)

$$T_{MEAS} = \frac{\frac{(ADC_{MEAS} \times Gain)}{256} + Offset}{10}$$

Where:

ADC_{MEAS} = ADC reading at temperature being measured

Gain = Gain value stored in the DIA table

Offset = Offset value stored in the DIA table

Note: It is recommended to take the average of ten measurements of ADC_{MEAS} to reduce noise and improve accuracy.

Affected Silicon Revisions

B3	B4	B5	C0				
X	X	X	X				

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1.14. Module: Capture/Compare/PWM Module (CCP)

1.14.1. CCP Compare Toggle Output Mode Does Not Work as Expected

The CCP module's Compare Toggle Output Mode (MODE[3:0] = 'b0001) does not work as expected. When the TMRx resource matches the value in the CCPRx registers, the output may toggle randomly or not at all.

Work Around

None

Affected Silicon Revisions

B3	B4	B5	**C0**				
X	X	X	X				

1.15. Module: Power-Saving Modes

1.15.1. XLP Power Mode Does Not Work as Expected

Extended Ultra Low-Power Mode (VREGPM[1:0] = 'b11), which is recommended for applications operating above 85°C, does not work as expected.

Work Around

Use the Ultra Low-Power Mode (VREGPM[1:0] = 'b10) for the operating temperature range of -40°C to 125°C.

Affected Silicon Revisions

B3	B4	B5	**C0**				
X	X	X	**X**				

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2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002265**C**):

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1. CONFIG11 $\overline{\text{DATASCEN}}$ Bit

The Non-Boot Block Area CRC Data EEPROM Scan Enable ($\overline{\text{DATASCEN}}$) bit of CONFIG11 is incorrectly labeled in the data sheet. The correct labeling is shown in the register below in **bold**:

Bit	7	6	5	4	3	2	1	0
	$\overline{\text{BOOTPOR}}$	$\overline{\text{COE}}$	$\overline{\text{CFGSCEN}}$	**$\overline{\text{DATASCEN}}$**	$\overline{\text{SAFSCEN}}$	$\overline{\text{APPSCEN}}$	$\overline{\text{BOOTCOE}}$	$\overline{\text{BOOTSCEN}}$
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

2.2. I2CxCNT Register Note Addition

Note 3 has been added to the I2CxCNT register description as shown below in **bold**:

Bit	15	14	13	12	11	10	9	8
	CNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 - CNT[15:0] Byte Count

Condition	Description
If receiving data:	Count value decremented on 8th falling SCL edge when a new byte is loaded into I2CxRXB
If transmitting data:	Count value decremented on 9th falling SCL edge when a new byte is moved into I2CxTXB

Notes:

1. It is recommended to write this register only when the module is Idle (MMA = 0 or SMA = 0) or when the module is clock stretching (CSTR = 1 or MDR = 1).

2. CNTIF is set on the 9th falling SCL edge when I2CxCNT = 0.

3. I2CxCNTH is double-buffered for writing and must be written to before writing to I2CxCNTL. The counter value is updated when I2CxCNTL is written.

2.3. RxyPPS Register Bit-Field Length

The RxyPPS register incorrectly shows a 6-bit-wide bit-field (RxyPPS[5:0]). Bit 6 has been added to the bit-field as shown below in **bold**:

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Bit	7	6	5	4	3	2	1	0
		RxyPPS[**6:0**]						
Access		**R/W**	R/W	R/W	R/W	R/W	R/W	R/W
Reset		**0**	0	0	0	0	0	0

Bits **6**:0 - RxyPPS[**6:0**] Pin Rxy Output Source Selection

2.4. UART Checksum Error Interrupt Flag (CERIF) Bit

The UART Checksum Error Interrupt Flag (CERIF) bit description of the UxERRIR register incorrectly refers to DALI mode, when this bit is only used in LIN mode. The corrected description is shown below in **bold**:

Bit 4 - CERIF Checksum Error Interrupt Flag

Value	Condition	Description
1	**MODE = LIN**	**Indicates a checksum error in received data**
0	**MODE = LIN**	**No checksum error**
x	**MODE = not LIN**	**Not used**

2.5. TUIN0PPS/TUIN1PPS Register Addresses

Table 21-9 (PPS Register Summary) incorrectly lists the Universal Timer PPS Inputs (TUIN0PPS/ TUIN1PPS) register addresses. The correct addresses are shown in the table snippet below in **bold**:

Address	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x024B	TUIN0PPS	7:0			PORT[2:0]			PIN[2:0]		
0x024C	TUIN1PPS	7:0			PORT[2:0]			PIN[2:0]		

2.6. 48-Lead TQFP Package Drawing

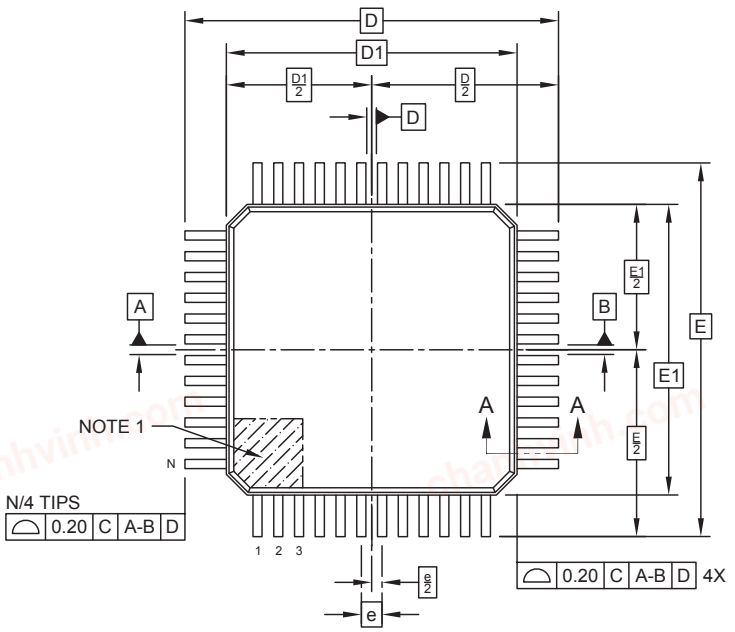
The data sheet lists the incorrect package drawing for the 48-lead TQFP package. The correct package drawings are shown below:

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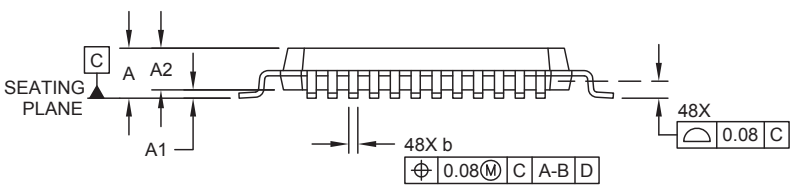
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48-Lead Plastic Thin Quad Flatpack (Y8X) - 7x7x1.0 mm Body [TQFP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

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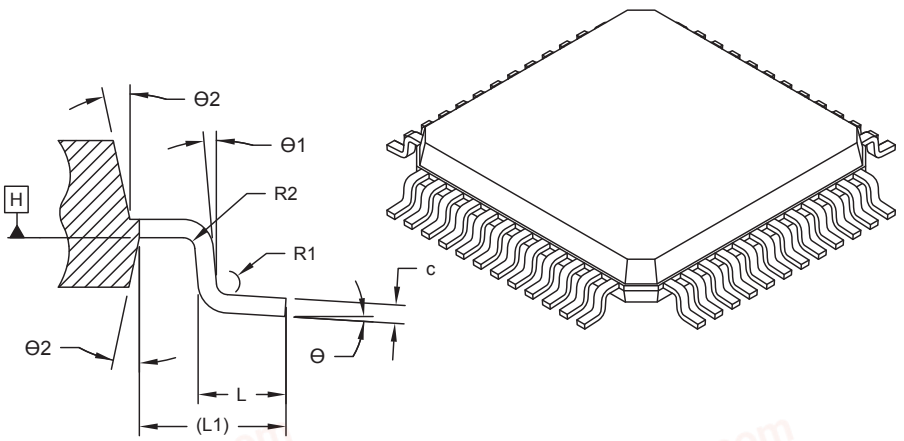
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48-Lead Plastic Thin Quad Flatpack (Y8X) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		48	
Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Length	D		9.00 BSC	
Molded Package Length	D1		7.00 BSC	
Overall Width	E		9.00 BSC	
Molded Package Width	E1		7.00 BSC	
Terminal Width	b	0.17	0.22	0.27
Terminal Thickness	c	0.09	-	0.16
Terminal Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Lead Bend Radius	R1	0.08	-	-
Lead Bend Radius	R2	0.08	-	0.20
Foot Angle	Θ	0°	3.5°	7°
Lead Angle	Θ1	0°	-	-
Mold Draft Angle	Θ2	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-300-Y8X Rev D Sheet 2 of 2

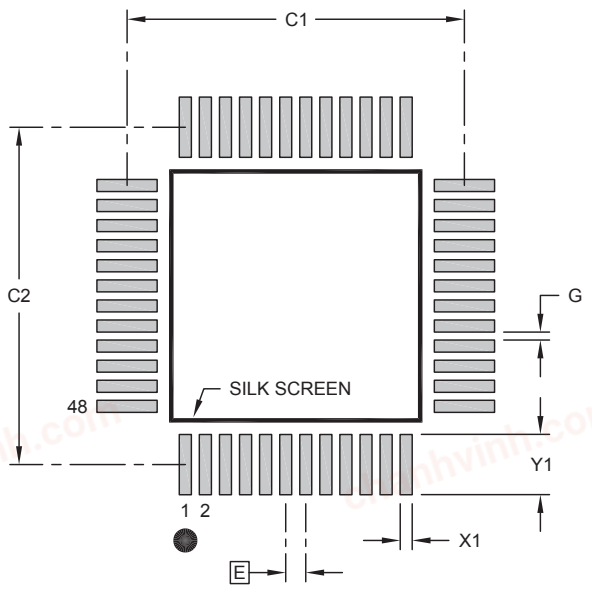
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48-Lead Plastic Thin Quad Flatpack (Y8X) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		8.40	
Contact Pad Spacing	C2		8.40	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2300-Y8X Rev D

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2.7. IVTBASE and IVTAD Register Reset Values

The IVTBASE and IVTAD register Reset values are incorrect in the data sheet. The correct Reset values are shown below (changes in **bold**):

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Bit	7	6	5	4	3	2	1	0
	IVTBASEL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	**1**	0	0	0

Bit	7	6	5	4	3	2	1	0
	IVTADL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	**1**	0	0	0

2.8. FVR Independent Gain Amplifiers

The following note is added to the section **"Independent Gain Amplifiers"**:

Important: Changing an analog peripheral's reference voltage while the peripheral is enabled may cause undesirable behavior, including device resets, oscillator drift, or reliability issues. If the analog peripheral's reference voltage must be changed, disable the peripheral, update the reference voltage, and then re-enable the peripheral. This applies to all analog peripherals, such as the ADC, DAC, Comparator, etc..

2.9. ADACT Register

In the ADACT register, the description of two ADC Auto-Conversion Trigger Sources have been clarified. Corrections are shown in the table excerpt (below) in **bold**; all other values in the original table remain unchanged.

Table 2-1. ADC Auto-Conversion Trigger Sources (Excerpt)

ACT	Auto-Conversion Trigger Source
111110	Software read of**/write to** ADRESH
111101	Software read of**/write to** ADERRH

2.10. CAN Receive Message Object

The Receive Message Object table shown in the section **"Reading a Receive Message Object"** has bytes 4 and 5 erroneously swapped. Corrections are shown in the table except (below) in **bold**; all other bytes and table footnotes remain unchanged.

Table 2-2. Receive Message Object (Excerpt)

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	SID[7:0]							
1	EID[4:0]					SID[10:8]		
2	EID[12:5]							
3	-	-	-	EID[17:13]				
4	-	-	**RTR**	**IDE**	**DLC[3:0]**			
5	**FILHIT[4:0]**				-	-	**ESI**	

2.11. Interrupt Vector Priority Table Incorrect PWM Interrupt Source Labels

The PWMx interrupt source labels in the Interrupt Vector Priority table have been corrected as shown in the table below (changes from the data sheet in **bold**).

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Table 2-3. Interrupt Vector Priority Table

Vector Number	Interrupt source
0x26	**PWM1P (PWM Period Interrupt)**
0x27	**PWM1 (PWM Parameter Interrupt)**
0x2E	**PWM2P**
0x2F	**PWM2**
0x3E	**PWM3P**
0x3F	**PWM3**
0x4E	**PWM4P**
0x4F	**PWM4**

2.12. DMAxSIRQ/DMAxAIRQ Interrupt Source Table Incorrect PWM Interrupt Labels

The PWMx interrupt source labels in the DMAxSIRQ and DMAxAIRQ Interrupt Sources table have been corrected as shown in the table below (changes from the data sheet in **bold**).

Table 2-4. DMAxSIRQ and DMAxAIRQ Interrupt Sources

Vector Number	Interrupt Source
0x26	**PWM1P (PWM Period Interrupt)**
0x27	**PWM1 (PWM Parameter Interrupt)**
0x2E	**PWM2P**
0x2F	**PWM2**
0x3E	**PWM3P**
0x3F	**PWM3**
0x4E	**PWM4P**
0x4F	**PWM4**

2.13. Resets: Windowed Watchdog Timer (WWDT) Reset Section

The text of the **"Windowed Watchdog Timer (WWDT) Reset"** section of the **"Resets"** chapter has been replaced with the following text:

Windowed Watchdog Timer (WWDT) Reset

The Windowed Watchdog Timer generates a Reset if the firmware does not issue a `CLRWDT` instruction within the time-out period or window set. When a WDT Time-out Reset occurs, the $\overline{TO}$ bit of the STATUS register and the $\overline{RWDT}$ bit are cleared. If the `CLRWDT` instruction was issued while the WDT Reset window was closed, the $\overline{WDTWV}$ bit is cleared, indicating a WDT Window violation occurred.

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3. Appendix A: Revision History

Doc. Rev.	Date	Comments
G	08/2026	Added silicon issues 1.1.6, 1.2.2 through 1.2.8, 1.11.1, 1.12.1, 1.13.1, 1.14.1 and 1.15.1; added DS Clarifications 2.1 through 2.13.
F	04/2024	Added silicon revision C0
E	12/2023	Added silicon erratum 1.1.5 to UTMR module as well as new errata 1.2.1-1.10.1. Added new errata entry to UTMR module.
D	07/2022	Added Data Sheet Clarification 2.1
C	03/2021	Adding silicon erratum item 1.1.4
B	01/2021	Adding silicon erratum item 1.1.3
A	11/2020	Initial document release

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