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PIC16F15225/45 Silicon Errata and Data Sheet Clarifications

PIC16F15225/45

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Introduction

The PIC16F15225/45 devices that you have received conform functionally to the current device data sheet (DS20006389**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC16F15225/45 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID				
		B0	B1	B2	B3	B4
PIC16F15225	0x30E9	0x2100	0x2101	0x2102	0x2103	0x2104
PIC16F15245	0x30EA	0x2100	0x2101	0x2102	0x2103	0x2104

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Silicon Issue Summary

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions				
				B0	B1	B2	B3	B4
Capture/ Compare/PWM (CCP)	PWM mode	1.1.1	Duty cycle values are incorrect	X	X	X	X	X
Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)	Transmit mode	1.2.1	Possible duplicate byte transmitted	X	X	X	X	X
Host Synchronous Serial Port (MSSP)	Start and Stop interrupt function	1.3.1	A race condition can cause the Start and/or Stop flags to be set when I^2C is enabled	X	X	X	X	X
In-Circuit Serial Programming™	Low-Voltage Programming	1.4.1	Low-Voltage Programming is not possible when V_{DD} is below BORV while BOR is enabled	X	X	X	X	X
Watchdog Timer (WDT)	Watchdog Timer Reset	1.5.1	WDT reset may not work properly while device is not in Sleep	X	X			
Configuration Words (CONFIG)	Sleep	1.6.1	Waking from Sleep may cause unexpected behavior.	X	X	X		
NVM - Non-Volatile Memory	NVM Programming	1.7.1	NVM programming does not work below 2.7V.	X	X	X	X	
Timer1	Timer1 Gate Source	1.8.1	Changing the Timer1 Gate Source may cause unexpected interrupts.	X	X	X	X	X
PFM - Program Flash Memory	Back to Back Writes	1.9.1	Repetitive writes may cause write/erase failures.	X	X	X	X	X

Note: Only those issues indicated in the last column apply to the current silicon revision.

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1. Silicon Errata Issues

NOTICE This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1. Module: Capture/Compare/PWM Module (CCP)

1.1.1. Wrong Duty Cycle for CCP Module

While in PWM mode and with the Timer2 prescaler configured to 1:1, the duty cycle of the PWM output is as expected. When the Timer2 prescaler is changed to a value other than 1:1 while T2PR = 0 (PWM resolution of two bits), the expected duty cycle is wrong. The corrected duty cycle values are shown in the table below.

Table 1-1. Corrected Duty Cycle Values

Prescaler/CCPR	0	1	2	3	4
1:1	0%	25%	50%	75%	100%
1:2	50%	75%	50%	75%	100%
1:4...1:128	75%	75%	75%	75%	100%

Work Around

None.

Affected Silicon Revisions

B0	B1	B2	B3	**B4**			
X	X	X	X	**X**			

1.2. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

1.2.1. Double Byte Transmit

Under certain conditions, a byte written to the TXREG register can be transmitted twice. This happens when a byte is written to TXREG just as the TSR register becomes empty. This new byte is immediately transferred to the TSR register but also remains in the TXREG register until the completion of the current instruction cycle. If the new byte in the TSR register is transmitted before this instruction cycle has completed, the duplicate in the TXREG register will subsequently be transferred to the TSR register on the following instruction clock cycle and transmitted.

Work around

Method 1:

Monitor the Transmit Interrupt Flag (TXIF) bit. Writes to the TXREG register can be performed once the TXIF bit is set, indicating that the TXREG register is empty. If using this method, ensure that the second byte is filled in the TXREG before bit 6 of the first byte is transmitted. If the delay is more than six bit times, there is a possibility of double byte transmission.

Method 2:

Monitor the TMRT bit of the TXxSTA register. Writes to the TXREG register can be performed once the TMRT bit is set, indicating that the Transmit Shift Register (TSR) is empty. This work around can be applied if back-to-back transmissions are not necessary.

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Affected Silicon Revisions

B0	B1	B2	B3	**B4**			
X	X	X	X	**X**			

1.3. Module: Host Synchronous Serial Port (MSSP)

1.3.1. The I²C Start and/or Stop Flags May Be Set When I²C Is Enabled

When I²C is enabled, erroneous Start and/or Stop conditions may be detected. This can generate erroneous I²C interrupts, if enabled.

Work Around

Use the following procedure to correctly detect the Start and Stop conditions:

1. Disable the Start and Stop conditions interrupt functions.
2. Enable the I²C module.
3. Wait 250 ns + six instruction cycles ($F_{OSC}/4$).
4. Clear the Start and Stop conditions interrupt flags.
5. Enable the Start and Stop conditions interrupt functions, if used.

```
SSPxCON3bits.SCIE = 0;          // Disable Start condition interrupt
SSPxCON3bits.PCIE = 0;          // Disable Stop condition interrupt
SSPxCON1bits.SSPEN = 1;         // Enable I2C
Delay();                        // Wait for 250 ns + 6 instruction cycles (FOSC/4)
PIRxbits.SSPxIF = 0;            // Clear the MSSP interrupt flag
SSPxCON3bits.SCIE = 1;          // Enable Start condition interrupt if used
SSPxCON3bits.PCIE = 1;          // Enable Stop condition interrupt if used
```

Affected Silicon Revisions

B0	B1	B2	B3	**B4**			
X	X	X	X	**X**			

1.4. Module: Low-Voltage Programming (LVP)

1.4.1. Low-Voltage Programming Not Possible

Low-Voltage Programming is not possible when V_{DD} is below the selected BORV voltage level while BOR is enabled.

Work Around

Method 1:

Disable BOR to use Low-Voltage Programming.

Method 2:

Raise V_{DD} above the selected BORV level while using Low-Voltage Programming.

Affected Silicon Revisions

B0	B1	B2	B3	**B4**			
X	X	X	X	**X**			

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1.5. Module: Watchdog Timer (WDT)

1.5.1. Watchdog Timer Reset

The Watchdog Timer (WDT) Reset feature may not work properly outside of Sleep mode. Reliance on WDT Reset while executing a program is not recommended. Operation in Sleep is not impacted by this errata.

Work around

Use an independent timer to emulate a watchdog feature, outside of Sleep mode, using the following steps:

1. Configure the chosen timer for the desired timeout period.
2. Enable the timer interrupt.
3. Enable Peripheral and Global interrupts.
4. Enable the timer, which starts the count.
5. At the end of the Main loop, restore the timer values.
6. If the timer interrupt occurs, issue a `RESET` command.

A code example using Timer1 is shown below.

```
void __interrupt() isr(void)
{
    if( TMR1IF && TMR1IE )
    {
        asm("RESET");
    }
}

void main(void)
{
    configure_TMR1();
    GIE = 1;
    PEIE = 1;

    T1CONbits.ON = 1;

    while(1)
    {
        // user code here
        restore_TMR1();
    }
}
```

Affected Silicon Revisions

B0	B1	B2	B3	**B4**			
X	X						

1.6. Module: Configuration Words (CONFIG)

1.6.1. Waking from Sleep May Cause Unexpected Behavior

Waking from Sleep may cause unexpected behavior.

Work around

Do not use the `SLEEP` instruction. If clock switching is available and there is a need for reduced current consumption, switch to the slowest system clock.

Affected Silicon Revisions

B0	B1	B2	B3	**B4**			
X	X	X					

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1.7. Module: Nonvolatile Memory (NVM)

1.7.1. NMV Programming Does Not Work Below 2.7V

Performing an erase or write operation when V_{DD} is below 2.7V may fail. It is recommended to ensure that V_{DD} is above 2.7V before performing an erase or write operation.

Work around

None.

Affected Silicon Revisions

B0	B1	B2	B3	**B4**			
X	X	X	X				

1.8. Module: Timer1

1.8.1. Changing the Timer1 Gate Source May Cause Unexpected Interrupts

When a new value is written into the Timer1 Gate Source Select (GSS) bits of the TxGATE register, the TMRxGIF interrupt flag may be set unexpectedly, and if the TMRxGIE bit is set, an unexpected interrupt will occur.

Work around

User software must clear the TMRxGIF bit immediately after writing the new value to the GSS bits.

Affected Silicon Revisions

B0	B1	B2	B3	**B4**			
X	X	X	X	**X**			

1.9. Module: Program Flash Memory (PFM)

1.9.1. PFM Back-to-Back Writes

When repetitive writes to non-volatile memory (Program Flash Memory) are performed, it could result in write/erase failures at some locations. The issue is due to latent timing in the non-volatile memory controller which can cause the write instruction to fail under certain conditions.

Work around

To avoid the issue, the customer needs to wait an additional 100 µs after the WR bit of the NVMCON1 register has been set, allowing for the last word to be loaded into the latch. This delay is added only when the LWLO bit of the NVMCON1 register is cleared in the software.

```
if(i == (WRITE_FLASH_BLOCKSIZE-1))
        {
            // Start Flash program memory write
            NVMCON1bits.LWLO = 0;
        }
         NVMCON2 = 0x55;
        NVMCON2 = 0xAA;
        NVMCON1bits.WR = 1;
         if (NVMCON1bits.LWLO==0)
        {
        __delay_us(100);
        }
        NOP();
        NOP();

    writeAddr++;
    }
```


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Note: The `__delay_us()` function uses a `#define` macro definition. For the intrinsic `__delay_us()` function to work correctly, the value of the _XTAL_FREQ must be clearly defined. This macro is defined in the `device_config.h` file if the code is generated using MCC. The value of XTAL_FREQ is equal to the system clock frequency.

Affected Silicon Revisions

B0	B1	B2	B3	**B4**			
X	X	X	X	**X**			

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2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS20006389**D**):

Note:
Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1. TMR0

A note box has been added to the section **"Timer0 Output"**. The entire section now reads as follows:

TMR0_out toggles on every match between TMR0L and TMR0H in 8-bit mode or when TMR0H:TMR0L rolls over in 16-bit mode. If the output postscaler is used, the output is scaled by the ratio selected. The Timer0 output can be routed to an I/O pin via the RxyPPS output selection register or internally to a number of Core Independent Peripherals. The Timer0 output can be monitored through software via the OUT output bit.

Important: In 8-bit mode, when PR0 = 0 (either loaded with 0 or resets to 0), the TMR0 output remains high, and no interrupts are generated.

2.2. CPCON Charge Pump Threshold (CPT) Bit

In the CPCON register, the description of the Charge Pump Threshold (CPT) bit (CPCON[1]) is the opposite of its actual behavior. The correct description of the bit's operation is shown below (changes from the data sheet in **bold**).

Value	Description
1	V_{DD} is **below** the charge pump auto-enable threshold (V_{AUTO})
0	V_{DD} is **above** the charge pump auto-enable threshold (V_{AUTO})

2.3. SSPxCON3 SDA Hold Time Selection (SDAHT) Bit

The description of the SDA Hold Time Selection (SDAHT) bit in the SSPxCON3 register is opposite of its actual function. The correct description of the bit's function is shown below (changes from the data sheet in **bold**).

Value	Mode	Description
x	SPI	Not used in SPI mode
1	I^2C	**Minimum of 100 ns hold time on SDA after the falling edge of SCL (recommended)**
0	I^2C	**Minimum of 300 ns hold time on SDA after the falling edge of SCL**

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3. Appendix A: Revision History

Doc Rev.	Date	Comments
G	02/2026	Added data sheet clarification 2.3.
F	07/2024	Added silicon revision B4; corrected the REVID values; added silicon errata items 1.7.1, 1.8.1 and 1.9.1; added data sheet clarifications 2.1 and 2.2.
E	09/2022	Added silicon errata item 1.6.1; added silicon revision B3.
D	06/2022	Added silicon revision B2; updated DS revision letter to match latest DS revision.
C	05/2022	Added silicon errata item 1.5.1.
B	10/2021	Updated Table 2. Added silicon erratum items 1.1.1, 1.2.1, 1.3.1, and 1.4.1. Added new silicon Rev B1.
A	11/2020	Initial document release.

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