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PCI11101

PCIe Switch with Integrated USB 3.2 Gen 2 Host Controller & Programmable I/O

Highlights

- PCIe Gen 4 (8GT/s) switch fabric
- 2-lane PCIe Gen 4 (8GT/s) expansion port
- USB 3.2 Gen 2 (10Gbps) xHCI host
- I/O Multiplexer (SMBus/SPI/UART/GPIO)

Target Applications

- Math offload
- Vision intelligence / cameras / machine vision
- Servers with NG BMC & no PCH

Features

- Integrated PCI switching fabric
  - 512byte maximum payload size
- Integrated PCIe physical interfaces
  - 4-lane (4x8GT/s) upstream port
    - Allowing single, dual, or four lane links
  - 2-lane (2x8GT/s) downstream port
- Integrated USB 3.2 Gen 2 (10Gbps) physical interfaces
- Integrated xHCI USB 3.2 Gen 2 (10Gbps) USB host controller
  - 10Gbps Gen 2 PHY
  - USB HS/FS/LS PHY
- Two external power supplies: +3.3V, +1.1V
- Comprehensive power management features
  - PCIe 3.1 LPSS (Low Power Sub States): L2 (with aux. power supply)
- Power and I/O
  - Integrated power-on reset circuit with configurable under/over voltage protection
  - Latch-up performance exceeds 150mA per EIA/JESD78, Class II
  - JEDEC Class 3A ESD performance
- UARTs
  - RS232/RS485
  - Auto-direction control
  - Standard and advanced speed support
  - Basic or comprehensive signal support
- Additional features
  - Multifunction GPIOs
  - Programmable pin multiplexer
  - Ability to use low-cost 25MHz crystal or clock for reduced BOM
  - SPI peripheral interface
  - SMBus target interface
  - SMBus controller interface
  - PVT Sensor
  - JTAG TAP
- Packaging
  - Pb-free RoHS compliant 132-pin DRQFN package
- Environmental
  - Available in commercial and industrial grades

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1.0 INTRODUCTION

1.1 General Description

The Microchip PCI11101 is a single-chip PCIe switch with an integrated USB 3.2 Gen 2 host controller and programmable I/O. The integrated PCIe physical interfaces provide a 4-lane (4x8GT/s) upstream port and a 2-lane (2x8GT/s) downstream port. The device is targeted to address customer requests for higher bandwidth PCIe sub-systems within embedded applications. The maximum line rate is 8GT/s and it is certified against the GEN4 compliance program as defined in the PCIe Revision 4.x specifications. PCIe upstream can be delivered across a single or multiple lanes to accommodate best system architecture. The PCI11101 includes a compliant PCIe implementation from external facing physical interfaces through to switch fabric and endpoint controllers.

The PCI11101 includes a USB-IF and xHCI compliant USB 3.2 Gen 2 host controller with one USB 3.2 Gen 2 port. USB 3.2 Gen 2 10Gbps support is provided for USB Type-A, M.2 breakout, or embedded connections. Overcurrent Sense (OCS) and Port Control are provided for control of Vbus.

A programmable pin multiplexer is used to map I/O functions to package pins. This enables designers to work with either a default configuration or modify signals to best fit their application. Example signals include those associated with USB operation, through to GPIO or SMBus, which are accessed via a dedicated PCIe Endpoint Controller.

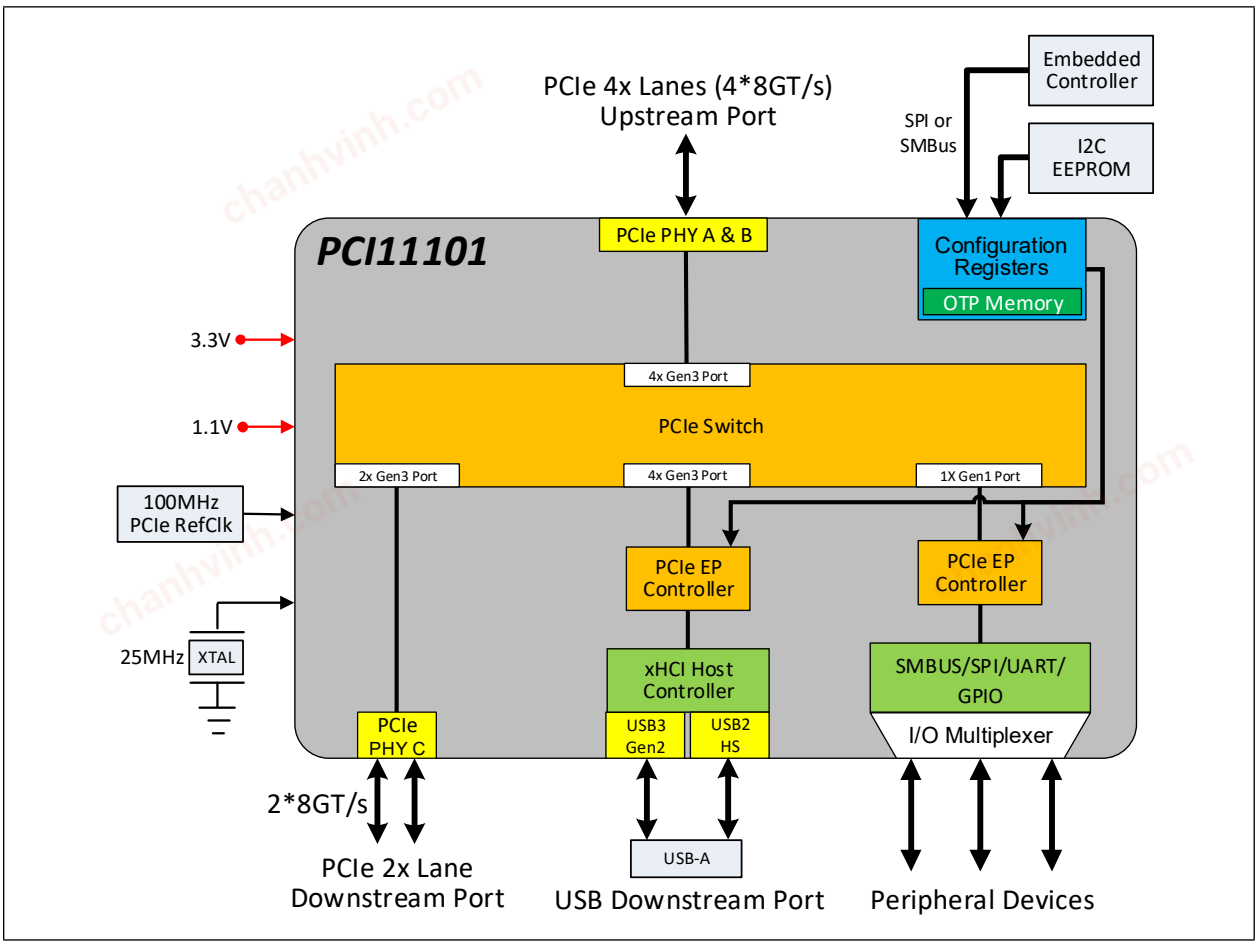
Though many clocks are required for PCI11101 operation, these are generated within an integrated clock farm. Only a single-ended 25MHz clock or crystal is required externally together with a PCIe reference clock.

PCI11101 software presentation is enabled using standard abstractions to major operating systems.

The PCI11101 is available in a 132-pin DRQFN package in commercial (0°C to +70°C) or industrial (-40°C to +85°C) temperature ranges.

An internal block diagram of the PCI11101 is shown in Figure 1-1.

FIGURE 1-1: INTERNAL BLOCK DIAGRAM



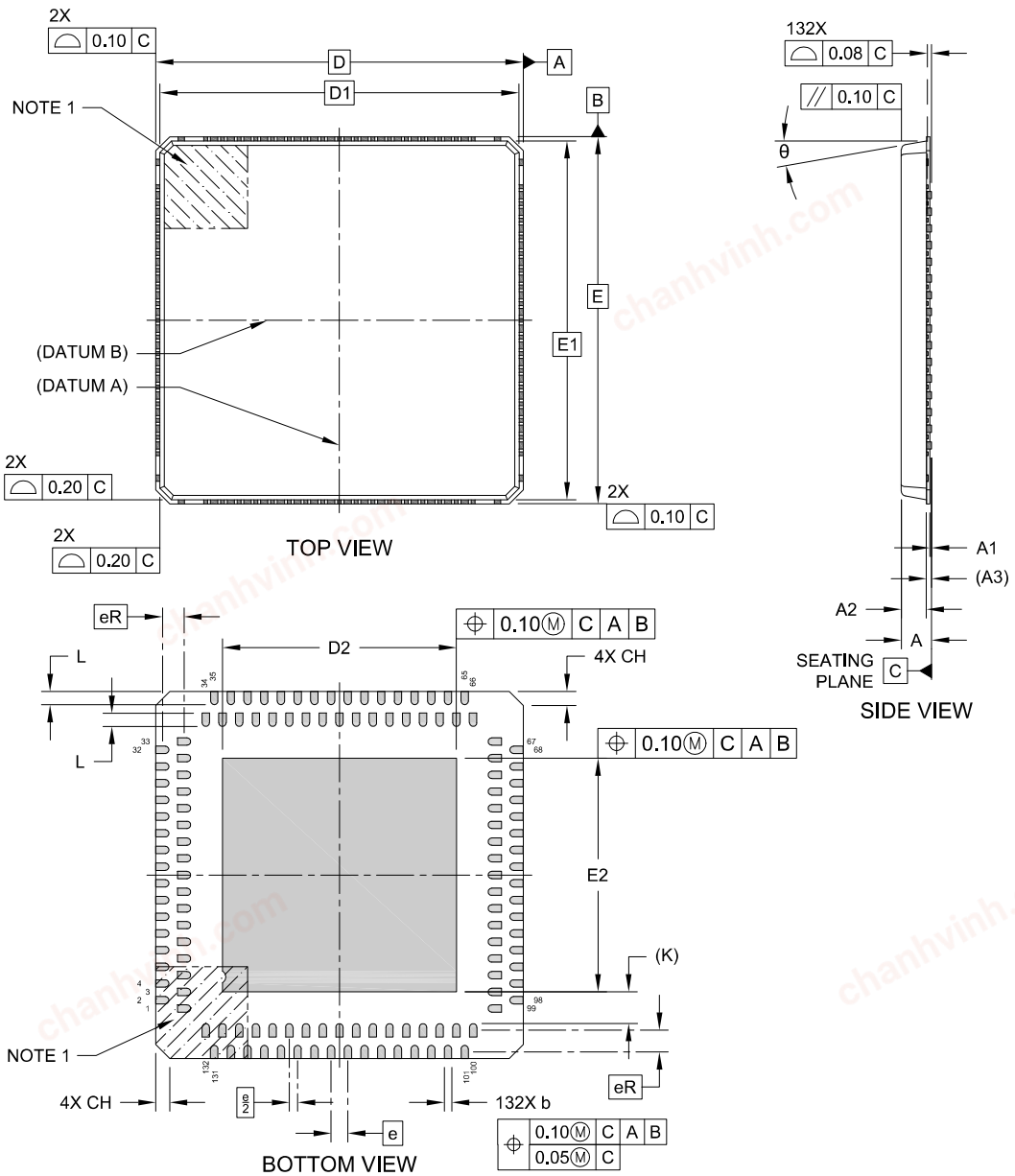
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2.0 PACKAGE INFORMATION

FIGURE 2-1: 132-DRQFN PACKAGE (DRAWING)

132-Lead Very Thin Plastic Quad Flat, No Lead Package (MXX) - 11x11x0.9 mm Body [VQFN]; Dual Row, Punch Singulated

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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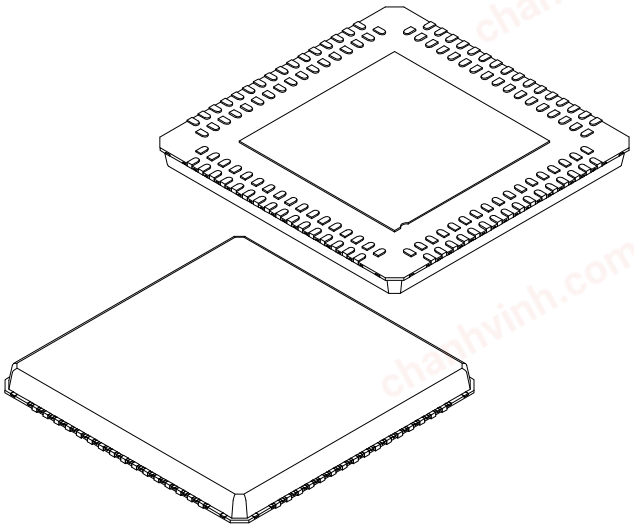
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FIGURE 2-2: 132-DRQFN PACKAGE (DIMENSIONS)

132-Lead Very Thin Plastic Quad Flat, No Lead Package (MXX) - 11x11x0.9 mm Body [VQFN]; Dual Row, Punch Singulated

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Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		132	
Pitch	e		0.50 BSC	
Overall Height	A	–	–	0.90
Standoff	A1	0.00	0.02	0.05
Standoff	A2	–	0.70	0.75
Terminal Thickness	A3		0.152 REF	
Overall Length	D		11.00 BSC	
Overall Length	D1		10.75 BSC	
Exposed Pad Length	D2	6.90	7.00	7.10
Overall Width	E		11.00 BSC	
Overall Length	E1		10.75 BSC	
Exposed Pad Width	E2	6.90	7.00	7.10
Spacing Between Rows	eR		0.65 BSC	
Terminal Width	b	0.18	0.22	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K		0.95 REF	
Package Corner Chamfer	CH	–	–	0.60
Mold Draft Angle	θ	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is punch singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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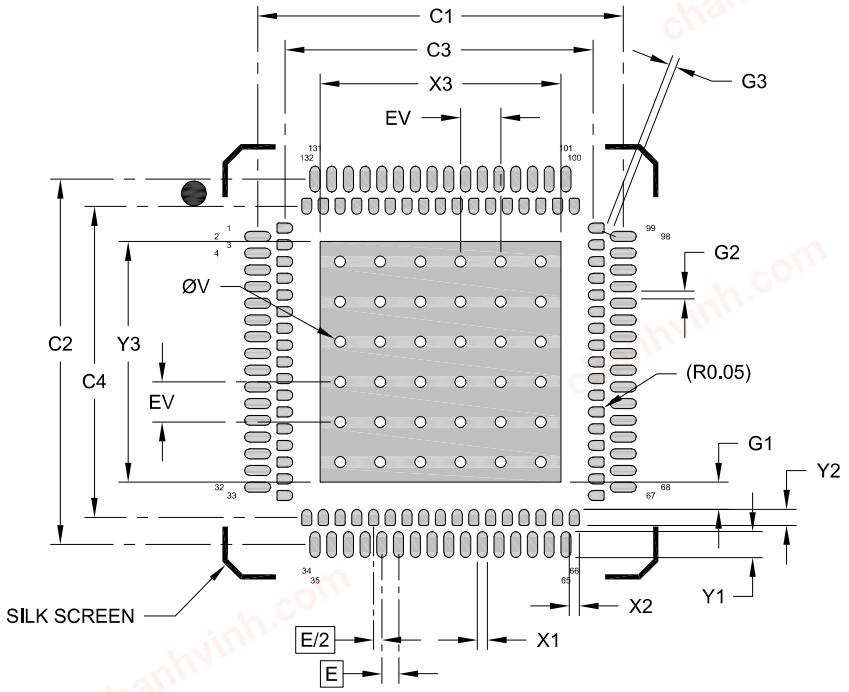
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FIGURE 2-3: 132-DRQFN PACKAGE (LAND PATTERN)

132-Lead Very Thin Plastic Quad Flat, No Lead Package (MXX) - 11x11x0.9 mm Body [VQFN]; Dual Row, Punch Singulated

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X3			7.20
Optional Center Pad Length	Y3			7.20
Contact Pad Spacing	C1		10.93	
Contact Pad Spacing	C2		10.93	
Contact Pad Spacing	C3		9.21	
Contact Pad Spacing	C4		9.21	
Outer Contact Pad Width (X64)	X1			0.30
Outer Contact Pad Length (X64)	Y1			0.78
Inner Contact Pad Width (X68)	X2			0.30
Inner Contact Pad Length (X68)	Y2			0.48
Inner Contact Pad to Center Pad	G1	0.80		
Contact Pad to Contact Pad	G2	0.20		
Outer Contact Pad to Inner Contact Pad	G3	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		0.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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APPENDIX A: PRODUCT BRIEF REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003791B (05-17-23)	Highlights	Updated cover bullets for clarity.
	Section 1.1, General Description	Added the following sentence to the first paragraph: “The maximum line rate is 8GT/s and it is certified against the GEN4 compliance program as defined in the PCIe Revision 4.x specifications.”
	Figure 1-1	Updated port names for clarity.
	Section 2.0, "Package Information"	Updated package drawing, dimensions and land pattern.
DS00003791A (01-08-21)	All	Initial Release.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-	X	/	XXX
Device	Tape and Reel Option		Temperature Range		Package

Device:	PCI11101= PCIe with USB Host, Ethernet MAC, Prog. I/O	
Tape and Reel Option:	Blank T	= Standard packaging (tray) = Tape and Reel (Note 1)
Temperature Range:	Blank I	= 0°C to +70°C (Commercial) = -40°C to +85°C (Industrial)
Package:	MXX =	132-pin DRQFN

Examples:

a) PCI11101/MXX
Tray, 0°C to +70°C, 132-pin DRQFN

b) PCI11101T/MXX
Tape & reel, 0°C to +70°C, 132-pin DRQFN

c) PCI11101-I/MXX
Tray, -40°C to +85°C, 132-pin DRQFN

d) PCI11101T-I/MXX
Tape & reel, -40°C to +85°C, 132-pin DRQFN

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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