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MIC94310

200 mA LDO with Ripple Blocker™ Technology

Features

- 1.8V to 3.6V Input Voltage Range
- Active Noise Rejection Over a Wide Frequency Band: >50 dB from 10 Hz to 10 MHz at 200 mA Load
- Rated to 200 mA Output Current
- Fixed Output Voltages
- Current-Limit and Thermal-Limit Protected
- 1.2 mm x 1.6 mm 4-Pin TDFN
- 5-Pin SOT-23
- Ultra-Small 0.88 mm x 0.88 mm WLCSP
- Logic-Controlled Enable Pin
- -40°C to +125°C Junction Temperature Range

Applications

- Smartphones/Smart Books
- Tablet PC/Notebooks and Webcams
- Digital Still and Video Cameras
- Global Positioning Systems
- Mobile Computing
- Automotive and Industrial Applications

General Description

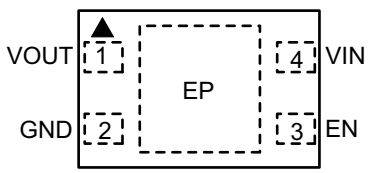
The MIC94310 Ripple Blocker™ is a monolithic integrated circuit that provides low-frequency ripple attenuation (switching noise rejection) to a regulated output voltage. This is important for applications where a DC/DC switching converter is required to lower or raise a battery voltage, but where switching noise cannot be tolerated by sensitive downstream circuits such as in RF applications. The MIC94310 maintains high power supply ripple rejection (PSRR) with input voltages operating near the output voltage level to improve overall system efficiency. A low-voltage logic enable pin facilitates ON/OFF control at typical GPIO voltage levels.

The MIC94310 operates from an input voltage of 1.8V to 3.6V.

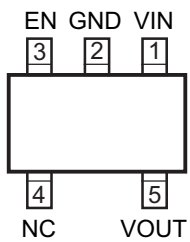
Packaged in a 4-pin 1.2 mm × 1.6 mm TDFN, a 5-pin SOT-23, or a 0.88 mm × 0.88 mm 4-Ball WLCSP, the MIC94310 has a junction operating temperature range of -40°C to +125°C.

Package Types

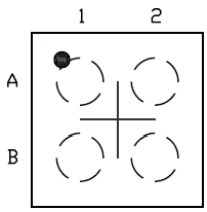
MIC94310
1.2 mm x 1.6 mm TDFN
(Top View)



MIC94310
SOT-23-5
(Top View)



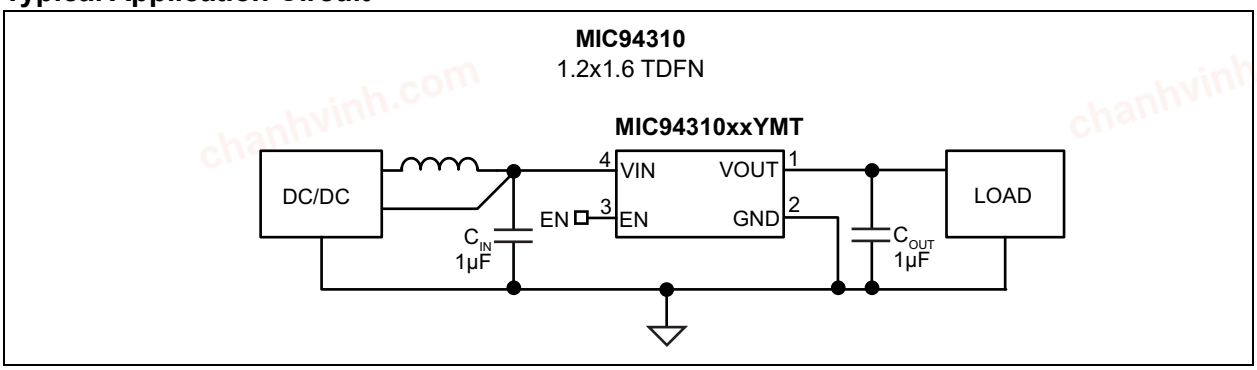
MIC94310
0.88 mm x 0.88 mm 4-Ball WLCSP
(Top View)



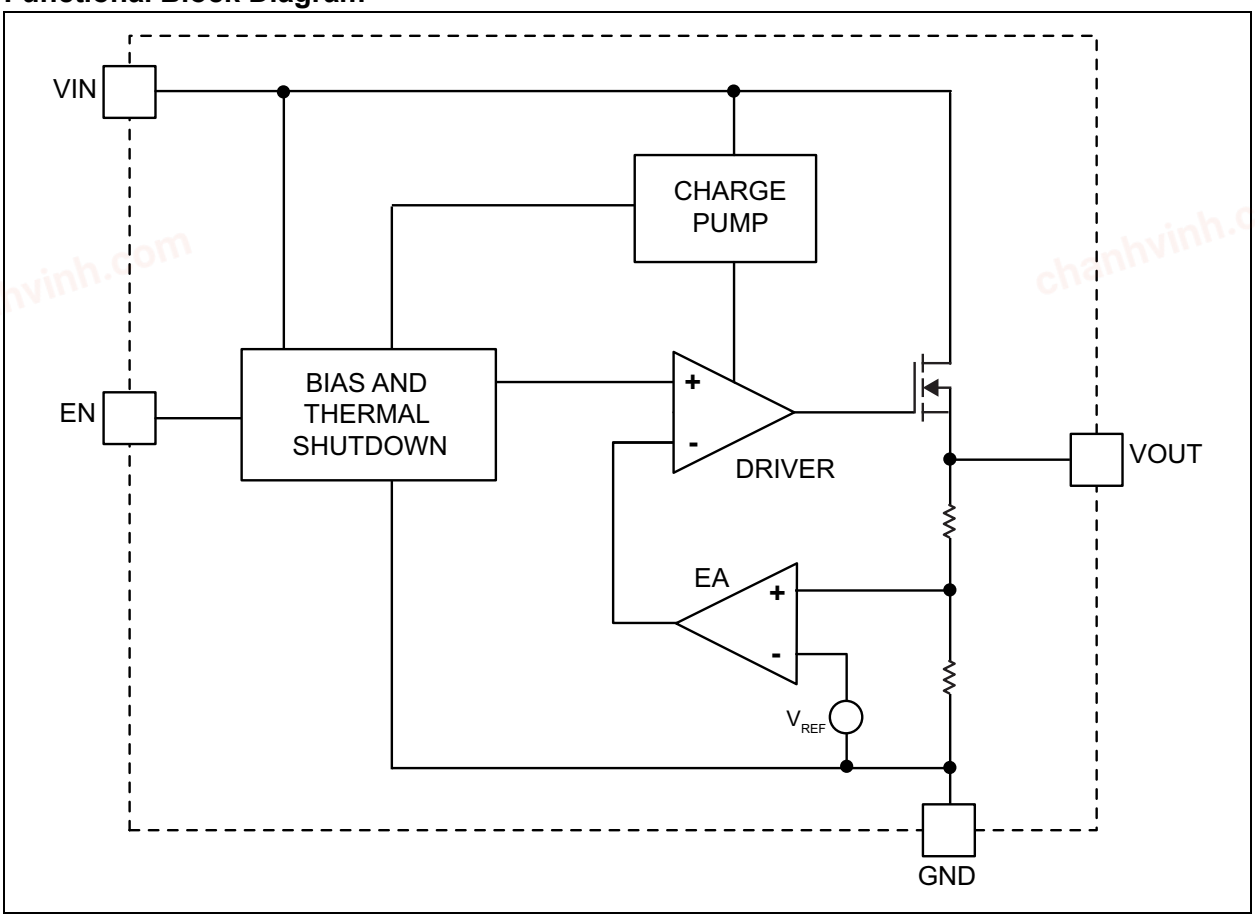
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Typical Application Circuit



Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Input Voltage, V_{IN} ..... –0.3V to +4.0V
Output Voltage, V_{OUT} ..... –0.3V to V_{IN}+0.3V or +4.0V
Enable Voltage, V_{EN} ..... –0.3V to V_{IN}+0.3V or +4.0V
ESD Rating (Note 1) ..... 3 kV

Operating Ratings ††

Supply Voltage, V_{IN} ..... +1.8V to +3.6V
Enable Voltage, V_{EN} ..... 0V to V_{IN}

† Notice: Exceeding the "Absolute Maximum Ratings †" may damage the device.

†† Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD-sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics: Unless otherwise indicated, $V_{IN} = V_{EN} = V_{OUT}$ + 500 mV ($V_{IN} = V_{EN}$ = 3.6V for $V_{OUT} \geq$ 3.1V); I_{OUT} = 1 mA; C_{OUT} = 1 µF (YMT), C_{OUT} = 10 µF (YM5); T_A = 25°C, **bold** values indicate –40°C ≤ T_J ≤ +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Voltage	V_{IN}	**1.8**	—	**3.6**	V	—
Output Voltage Accuracy	V_{OUT}	**–3**	±1	**+3**	%	Variation from nominal V_{OUT}
Dropout Voltage	V_{DO}	—	20	**50**	mV	V_{IN} to V_{OUT} dropout at 100 mA output current
		—	40	**100**	mV	V_{IN} to V_{OUT} dropout at 200 mA output current
Load Regulation	ΔV_{OUT}	—	4	—	mV	I_{OUT} = 1 mA to 100 mA
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	—	0.01	**0.5**	%	$V_{IN} = V_{OUT}$ + 500 mV to 3.6V
Ground Current	I_{GND}	—	170	250	µA	No load to full load
Shutdown Current	I_{SHDN}	—	0.2	5	µA	V_{EN} = 0V
V_{IN} Ripple Rejection	PSRR	—	85	—	dB	f = 100 Hz, I_{OUT} = 100 mA
		—	68	—	dB	f = 100 kHz, I_{OUT} = 100 mA
		—	57	—	dB	f = 1 MHz, I_{OUT} = 100 mA
		—	50	—	dB	f = 10 MHz, I_{OUT} = 100 mA
Current Limit	I_{LIM}	**250**	400	700	mA	V_{OUT} = 0V
Total Output Noise	e_{no}	—	83	—	μV_{RMS}	f = 10 Hz to 100 kHz
Turn-on Time	t_{ON}	—	70	—	µs	—
Enable						
Input Logic Low Level	V_{EN_LOW}	—	—	**0.4**	V	—
Input Logic High Level	V_{EN_HIGH}	**1.0**	—	—	V	—
Enable Input Current	I_{EN}	—	0.01	1	µA	—

Note 1: Specification for packaged product only.

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TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Operating Temperature	T_J	–40	—	+125	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 10 sec.
Storage Temperature Range	T_S	–65	—	+150	°C	—
Package Thermal Resistances						
Thermal Resistance, TDFN	θ_{JA}	—	173	—	°C/W	—
Thermal Resistance, SOT-23-5Ld	θ_{JA}	—	120	—	°C/W	—
Thermal Resistance WLCSP	θ_{JA}	—	250	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

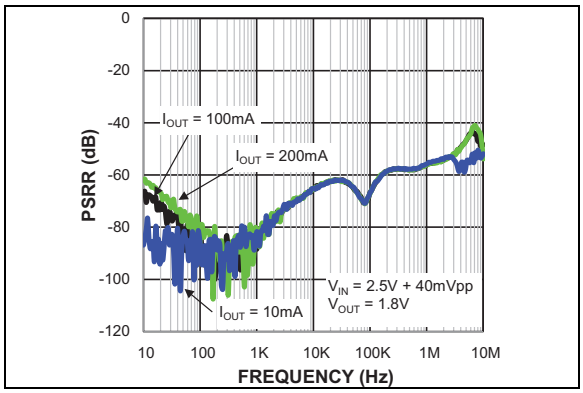


FIGURE 2-1: *PSRR C_{OUT} = 0.47 µF.*

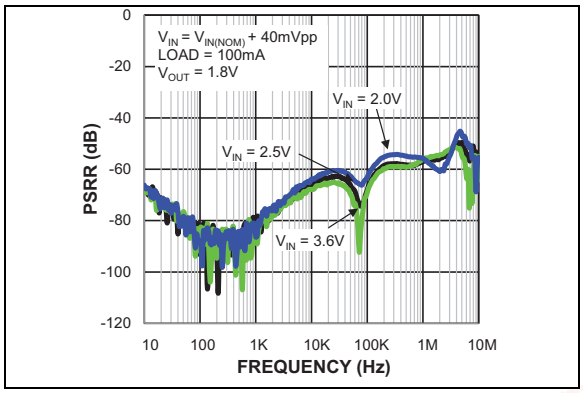


FIGURE 2-4: *PSRR C_{OUT} = 1 µF.*

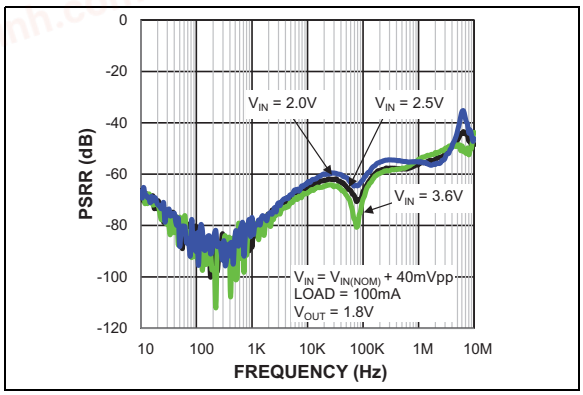


FIGURE 2-2: *PSRR C_{OUT} = 0.47 µF.*

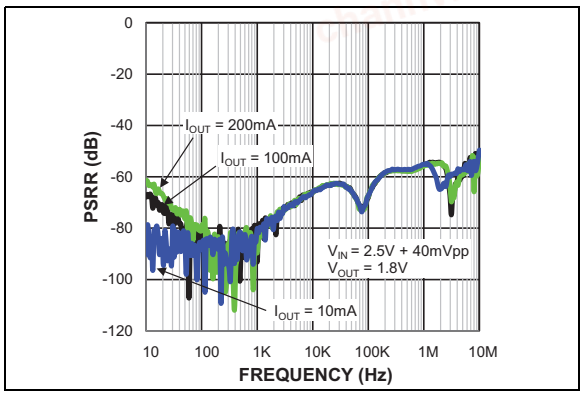


FIGURE 2-5: *PSRR C_{OUT} = 2.2 µF.*

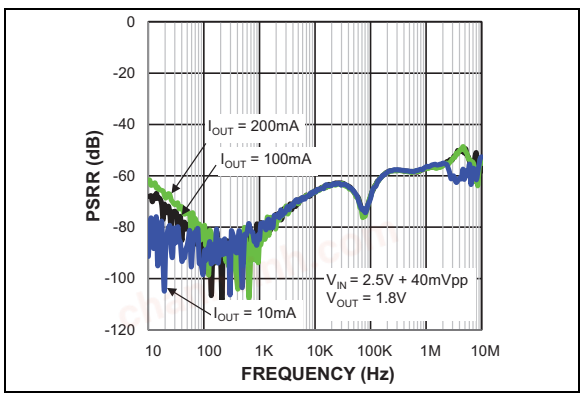


FIGURE 2-3: *PSRR C_{OUT} = 1 µF.*

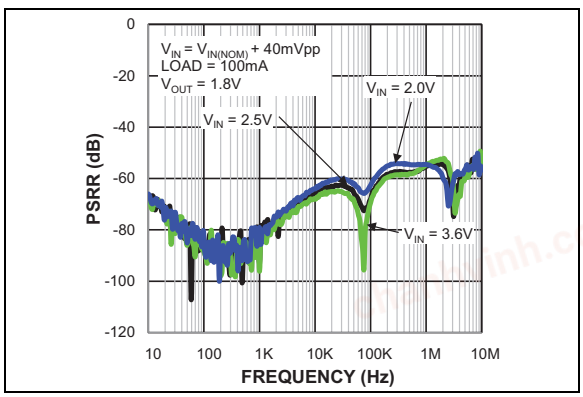


FIGURE 2-6: *PSRR C_{OUT} = 2.2 µF.*

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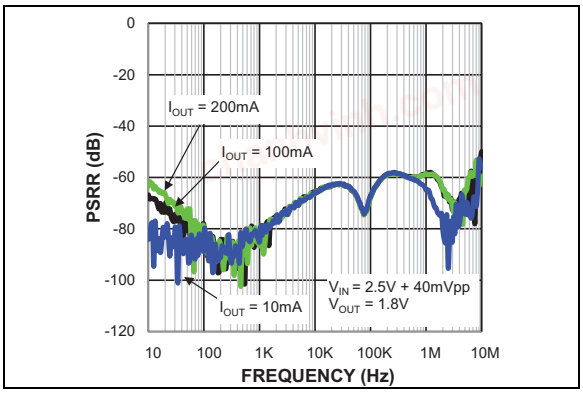


FIGURE 2-7: *PSRR C_{OUT} = 4.7 µF.*

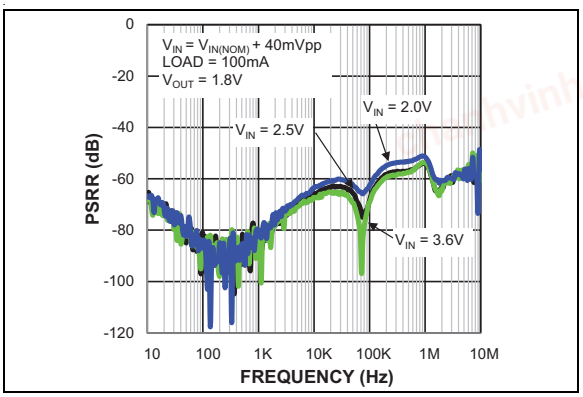


FIGURE 2-10: *PSRR C_{OUT} = 10 µF.*

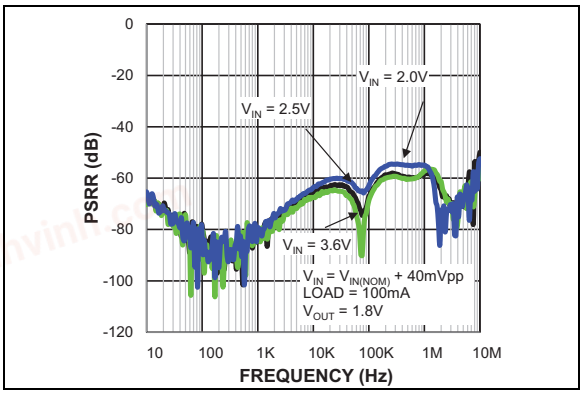


FIGURE 2-8: *PSRR C_{OUT} = 4.7 µF.*

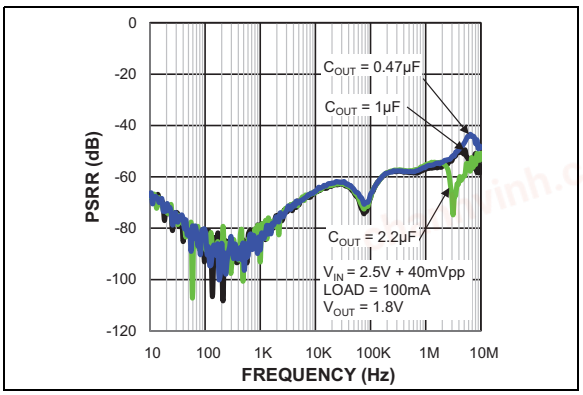


FIGURE 2-11: *PSRR (Varying C_{OUT}).*

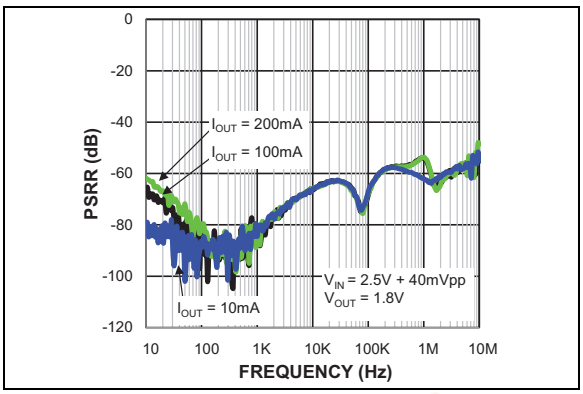


FIGURE 2-9: *PSRR C_{OUT} = 10 µF.*

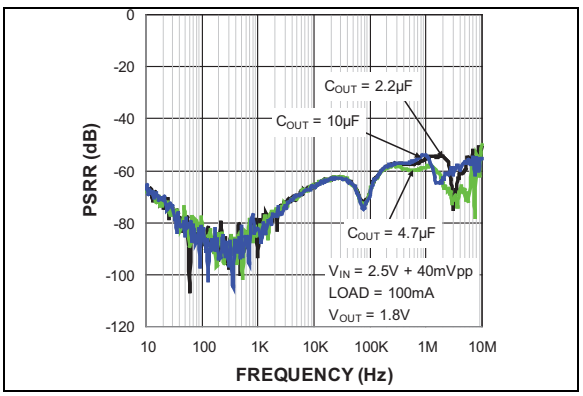


FIGURE 2-12: *PSRR (Varying C_{OUT}).*

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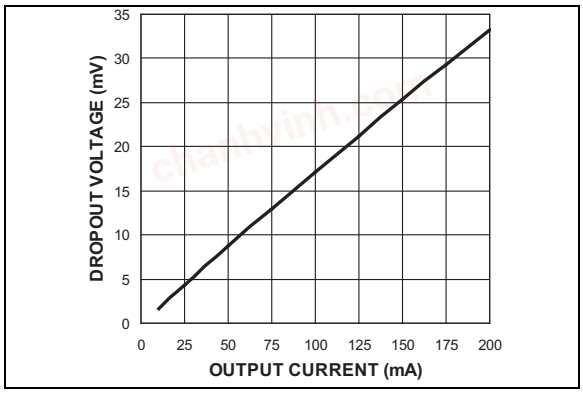


FIGURE 2-13: *Drop Voltage vs. Output Current.*

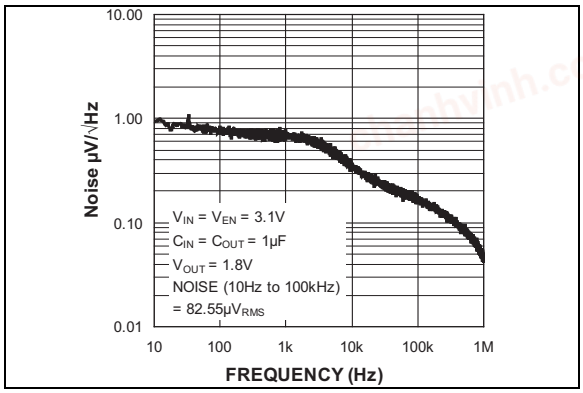


FIGURE 2-16: *Output Noise Spectral Density.*

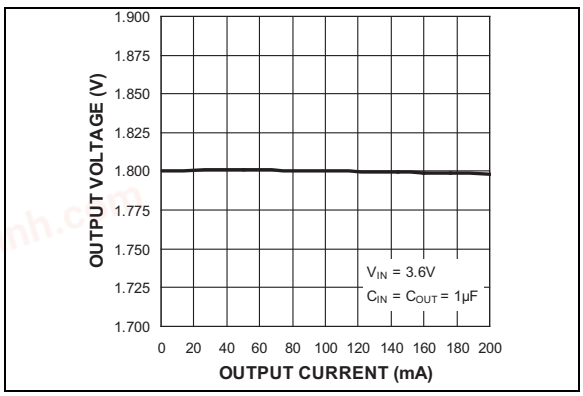


FIGURE 2-14: *Output Voltage vs. Output Current.*

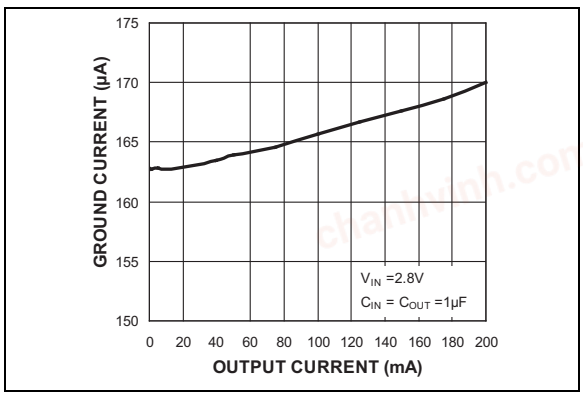


FIGURE 2-17: *Ground Current vs. Output Current.*

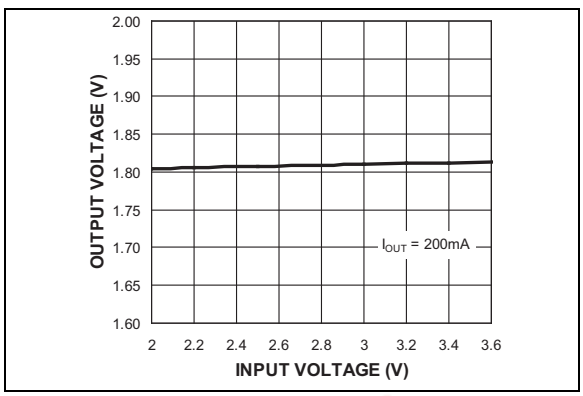


FIGURE 2-15: *Output Voltage vs. Input Voltage.*

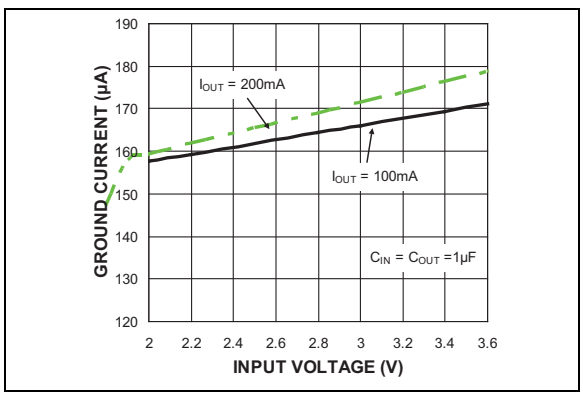


FIGURE 2-18: *Ground Current vs. Input Voltage.*

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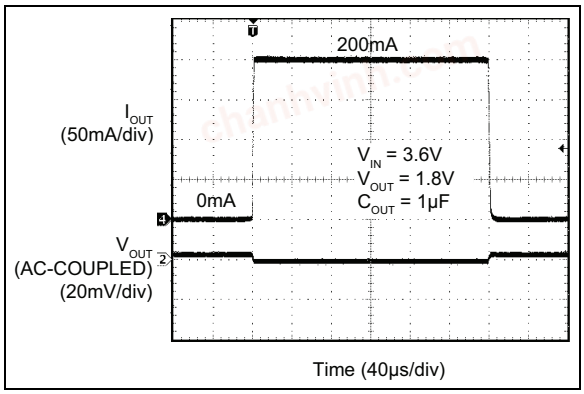


FIGURE 2-19: *Load Transient (0 mA to 200 mA).*

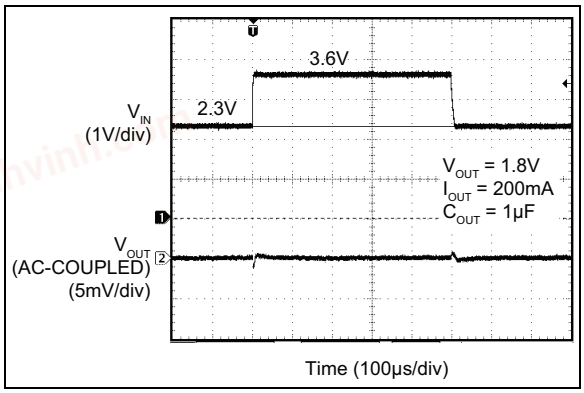


FIGURE 2-20: *Line Transient (2.6V to 3.6V).*

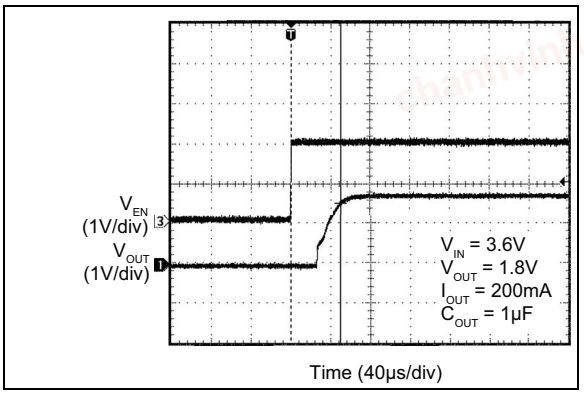


FIGURE 2-21: *Enable Turn-On.*

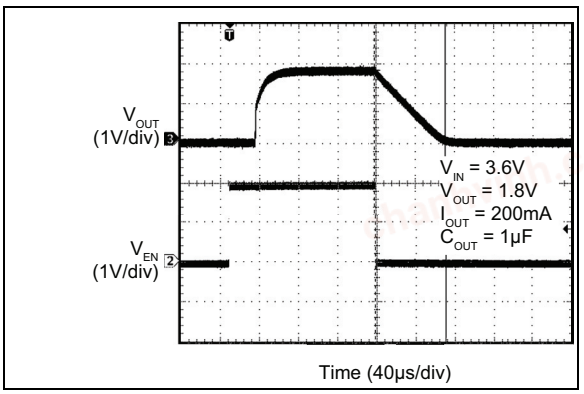


FIGURE 2-22: *Enable Turn-Off.*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MIC94310 TDFN	MIC94310 SOT-23	MIC94310 WLCSP	Symbol	Description
1	5	A2	V_{OUT}	Power Switch Output
2	2	B2	GND	Ground
3	3	B1	EN	Enable Input A logic HIGH signal on this pin enables the part. Logic LOW disables the part. Do not leave floating.
4	1	A1	V_{IN}	Power switch input and chip supply
—	4	—	NC	No Connect, not internally connected
EP	—	—	EPAD	Exposed Heatsink Pad Connect to ground for best thermal performance.

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4.0 APPLICATION INFORMATION

The MIC94310 is a very-high PSRR, fixed-output, 200 mA LDO utilizing Ripple Blocker technology. The MIC94310 is fully protected from damage due to fault conditions, offering linear current limiting and thermal shutdown.

4.1 Input Capacitor

The MIC94310 is a high-performance, high-bandwidth device. An input capacitor of 0.47 µF is required from the input to ground to provide stability. Low-ESR ceramic capacitors provide optimal performance at a minimum of space. Additional high-frequency capacitors, such as small-valued NPO dielectric-type capacitors, help filter out high-frequency noise and are good practice in any RF-based circuit. X5R or X7R dielectrics are recommended for the input capacitor. Y5V dielectrics lose most of their capacitance over temperature and are therefore, not recommended.

4.2 Output Capacitance

In order to maintain stability, the MIC94310 requires an output capacitor of 0.47 µF or greater for the Thin DFN package and 10 µF or greater for the SOT-23 package. For optimal ripple rejection performance, a 1 µF capacitor is recommended for the Thin DFN package. A 10 µF capacitor is recommended for the SOT-23 package. The design is optimized for use with low-ESR ceramic chip capacitors. High-ESR capacitors are not recommended because they may cause high-frequency oscillation. The output capacitor can be increased, but performance has been optimized for a 1 µF ceramic output capacitor and does not improve significantly with larger capacitance.

X7R/X5R dielectric type ceramic capacitors are recommended because of their temperature performance. X7R type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change their value by as much as 50% and 60%, respectively, over their operating temperature ranges. To use a ceramic chip capacitor with the Y5V dielectric, the value must be much higher than an X7R ceramic capacitor to ensure the same minimum capacitance over the equivalent operating temperature range.

4.3 No Load Stability

The MIC94310 will remain stable and in regulation with no load. This is especially important in CMOS RAM keep-alive applications.

4.4 Enable/Shutdown

Forcing the enable (EN) pin low disables the MIC94310 and sends it into a “zero” off mode current state. In this state, current consumed by the MIC94310 goes nearly to zero. Forcing EN high enables the output voltage. The EN pin uses CMOS technology and cannot be left floating as it could cause an indeterminate state on the output.

4.5 Thermal Considerations

The MIC94310 is designed to provide 200 mA of continuous current in a very small package. Maximum ambient operating temperature can be calculated based on the output current and the voltage drop across the part. For example if the input voltage is 2.5V, the output voltage is 1.8V, and the output current equals 200 mA. The actual power dissipation of the Ripple Blocker can be determined using Equation 4-1:

EQUATION 4-1:

$$P_D = (V_{IN} - V_{OUT1})I_{OUT} + V_{IN}I_{GND}$$

Because this device is CMOS and the ground current is typically <170 µA over the load range, the power dissipation contributed by the ground current is <1% and can be ignored for the calculation shown in Equation 4-2 and Equation 4-3.

EQUATION 4-2:

$$P_D = (2.5V - 1.8V) \times 200\ \text{mA}$$

EQUATION 4-3:

$$P_D = 0.14W$$

To determine the maximum ambient operating temperature of the package, use the junction-to-ambient thermal resistance of the device and the Equation 4-4:

EQUATION 4-4:

$$P_{D(MAX)} = \left(\frac{T_{J(MAX)} - T_A}{\theta_{JA}}\right)$$

$T_{J(MAX)}$ = 125ºC, the maximum junction temperature of the die, θ_{JA} thermal resistance = 173°C/W for the Thin DFN package.

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Substituting P_D for $P_{D(MAX)}$ and solving for the ambient operating temperature will give the maximum operating conditions for the regulator circuit.

For proper operation, the maximum power dissipation must not be exceeded.

For example, when operating the MIC94310-GYMT at an input voltage of 2.5V and 200 mA load with a minimum footprint layout, the maximum ambient operating temperature (T_A) can be determined as follows:

EQUATION 4-5:

$$0.14W = (125°C - T_A)/(173°C/\mathrm{W})$$

EQUATION 4-6:

$$T_A = 101°C$$

Therefore, the maximum ambient operating temperature allowed in a 1.2 mm × 1.6 mm Thin DFN package is 101°C.

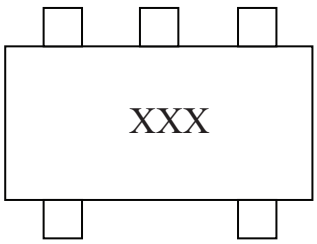
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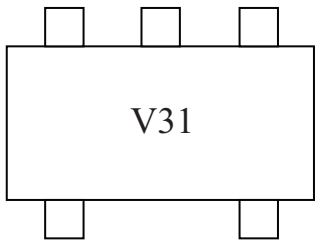
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

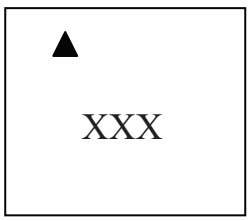
5-lead SOT-23*



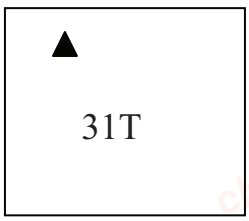
Example



4-lead TDFN*



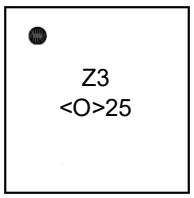
Example



4-ball WLCSP*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

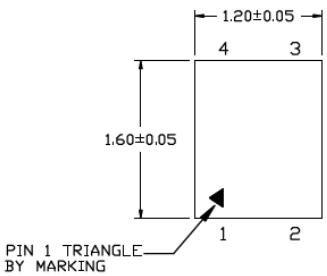
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4-Lead 1.2 mm × 1.6 mm Thin DFN Package Outline and Recommended Land Pattern

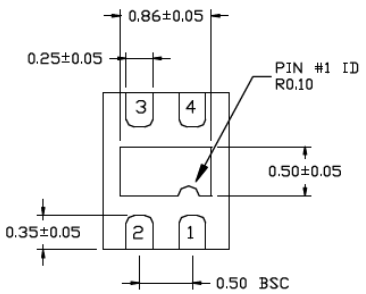
TITLE
4 LEAD TDFN 1.2x1.6mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	TDFN1216-4LD-PL-1	UNIT	MM



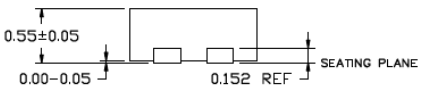
TOP VIEW

NOTE: 1, 2, 3



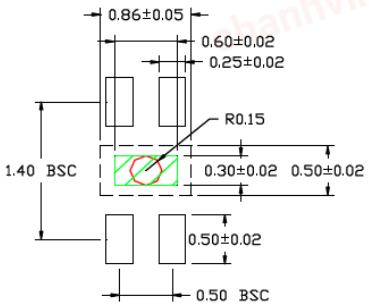
BOTTOM VIEW

NOTE: 1, 2, 3



SIDE VIEW

NOTE: 1, 2, 3



RECOMMENDED LAND PATTERN

NOTE: 4, 5

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. GREEN SHADED AREA INDICATES SOLDER STENCIL OPENING (OPTIONAL) FOR IMPROVED THERMAL PERFORMANCE. RECOMMENDED SIZE is 0.60mm x 0.30mm.
5. RED CIRCLE REPRESENTS THERMAL VIA & SHOULD BE CONNECTED TO GND FOR MAX PERFORMANCE. RECOMMENDED DIAMETER is 0.30mm - 0.35mm.

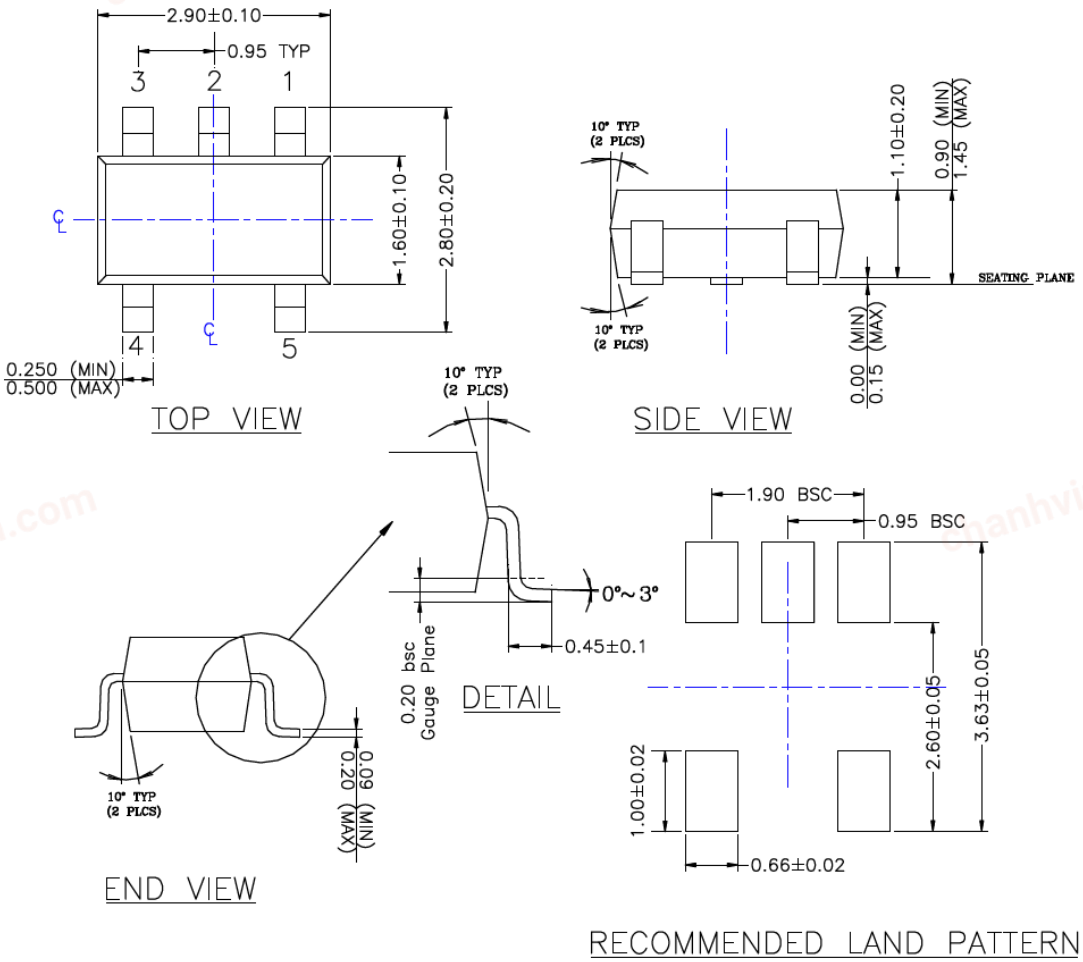
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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5-Pin SOT-23 Package Outline and Recommended Land Pattern

TITLE
5 LEAD SOT23 PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SOT23-5LD-PL-1	UNIT	MM



NOTE:
1. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & BURR.
2. PACKAGE OUTLINE INCLUSIVE OF SOLER PLATING.
3. DIMENSION AND TOLERANCE PER ANSI Y14.5M, 1982.
4. FOOT LENGTH MEASUREMENT BASED ON GAUGE PLANE METHOD.
5. DIE FACES UP FOR MOLD, AND FACES DOWN FOR TRIM/FORM.
6. ALL DIMENSIONS ARE IN MILLIMETERS.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

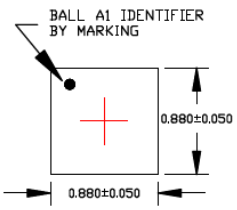
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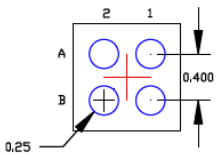
4-Ball WLCSP 0.88 mm x 0.88 mm Package Outline and Recommended Land Pattern

TITLE
4 BALL WLCSP 0.88x0.88mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

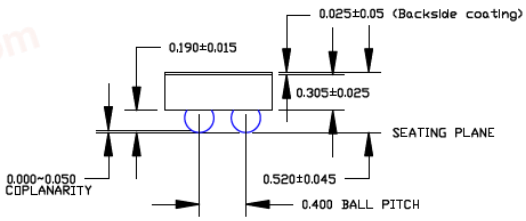
DRAWING #	WLCSP088088D-4BL-PL-9	UNIT	MM



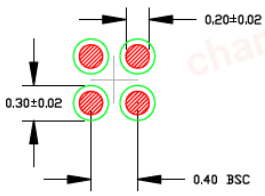
TOP VIEW
NOTE: 1,2



BOTTOM VIEW
NOTE: 1,2



SIDE VIEW
NOTE: 1,2



RECOMMENDED LAND PATTERN
NOTE: 3,4

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. NON-SOLDERMASK DEFINED PADS ARE RECOMMENDED FOR BOARD LAYOUT
4. SHADED RED CIRCLES REPRESENT CONTACT PAD AREA. GREEN CIRCLES REPRESENT SOLDER MASK OPENING

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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APPENDIX A: REVISION HISTORY

Revision B (September 2020)

- Added 0.88 mm × 0.88 mm 4-Ball WLCSP package.

Revision A (October 2018)

- Converted Micrel document MIC94310 to Microchip data sheet template DS20006105A.
- Minor grammatical text changes throughout.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	-X	X	XX	-XX
Device	Output Voltage	Temperature Range	Package	Media Type

Device:	MIC94310:	200 mA LDO with Ripple Blocker™ Technology	
Output Voltage:	4	=	1.2V
	F	=	1.5V
	G	=	1.8V
	D	=	1.85V
	J	=	2.5V
	L	=	2.7V
	M	=	2.8V
	N	=	2.85V
	P	=	3.0V
	S	=	3.3V
Temperature Range:	Y	=	–40°C to +85°C
	E	=	–40°C to +125°C
Packages:	MT	=	4-Lead 1.2 mm × 1.6 mm Thin DFN
	M5	=	5-Lead SOT-23
	CS	=	4-Ball 0.88 mm × 0.88 mm WLCSP
Media Type:	TR	=	3,000/Reel (SOT-23)
	TR	=	5,000/Reel (TDFN)
	TR	=	3,000/Reel (WLCSP)
	T5	=	500/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Examples:

a) MIC94310-4YMT-T5: 200 mA LDO with Ripple Blocker™ Technology, 1.2V Output Voltage, –40°C to +85°C Temperature Range, 5-Lead TDFN, 5,000/Reel

b) MIC94310-4YMT-TR: 200 mA LDO with Ripple Blocker™ Technology, 1.2V Output Voltage, –40°C to +85°C Temperature Range, 5-Lead TDFN, 5,000/Reel

c) MIC94310-4YM5-T5: 200 mA LDO with Ripple Blocker™ Technology, 1.2V Output Voltage, –40°C to +85°C Temperature Range, 5-Lead SOT-235,000/Reel

d) MIC94310-4YM5-TR: 200 mA LDO with Ripple Blocker™ Technology, 1.2V Output Voltage, –40°C to +85°C Temperature Range, 5-Lead SOT-23, 5,000/Reel

e) MIC94310-4YMT-T5: 200 mA LDO with Ripple Blocker™ Technology, 1.2V Output Voltage, –40°C to +85°C Temperature Range, 5-Lead TDFN, 5,000/Reel

f) MIC94310-4YMT-TR: 200 mA LDO with Ripple Blocker™ Technology, 1.2V Output Voltage, –40°C to +85°C Temperature Range, 5-Lead TDFN, 5,000/Reel

g) MIC94310-4YM5-T5: 200 mA LDO with Ripple Blocker™ Technology, 1.2V Output Voltage, –40°C to +85°C Temperature Range, 5-Lead SOT-23 5,000/Reel

h) MIC94310-4YM5-TR: 200 mA LDO with Ripple Blocker™ Technology, 1.2V Output Voltage, –40°C to +85°C Temperature Range, 5-Lead SOT-23, 5,000/Reel

i) MIC94310-4YCS-TR: 200 mA LDO with Ripple Blocker™ Technology, 1.2 Output Voltage –40°C to +125°C Extended Temperature Range, 4-Ball WLCSP 3,000/Reel

j) MIC94310-GYCS-TR: 200 mA LDO with Ripple Blocker™ Technology, 1.8 Output Voltage –40°C to +125°C Extended Temperature Range, 4-Ball WLCSP 3,000/Reel

k) MIC94310-JYCS-TR: 200 mA LDO with Ripple Blocker™ Technology, 2.5 Output Voltage –40°C to +125°C Extended Temperature Range, 4-Ball WLCSP 3,000/Reel

l) MIC94310-MYCS-TR: 200 mA LDO with Ripple Blocker™ Technology, 2.8 Output Voltage –40°C to +125°C Extended Temperature Range, 4-Ball WLCSP 3,000/Reel

m) MIC94310-PYCS-TR: 200 mA LDO with Ripple Blocker™ Technology, 0.0 Output Voltage –40°C to +125°C Extended Temperature Range, 4-Ball WLCSP 3,000/Reel

n) MIC94310-SYCS-TR: 200 mA LDO with Ripple Blocker™ Technology, 3.3 Output Voltage –40°C to +125°C Extended Temperature Range, 4-Ball WLCSP 3,000/Reel

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