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MIC5891

8-Bit Serial-Input Latched Source Driver

General Description

The MIC5891 latched driver is a high-voltage, high current integrated circuit comprised of eight CMOS data latches, CMOS control circuitry for the common STROBE and OUTPUT ENABLE, and bipolar Darlington transistor drivers for each latch.

Bipolar/MOS construction provides extremely low power latches with maximum interface flexibility.

The MIC5891 will typically operate at 5MHz with a 5V logic supply.

The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL circuits may be used with appropriate pull-up resistors to ensure a proper logic-high input.

A CMOS serial data output allows additional drivers to be cascaded when more than 8 bits are required.

The MIC5891 has open-emitter outputs with suppression diodes for protection against inductive load transients. The output transistors are capable of sourcing 500mA and will sustain at least 35V in the on-state.

Simultaneous operation of all drivers at maximum rated current requires a reduction in duty cycle due to package power limitations. Outputs may be paralleled for higher load current capability.

The MIC5891 is available in a 16-pin plastic DIP package (N) and 16-pin wide SOIC package (WM).

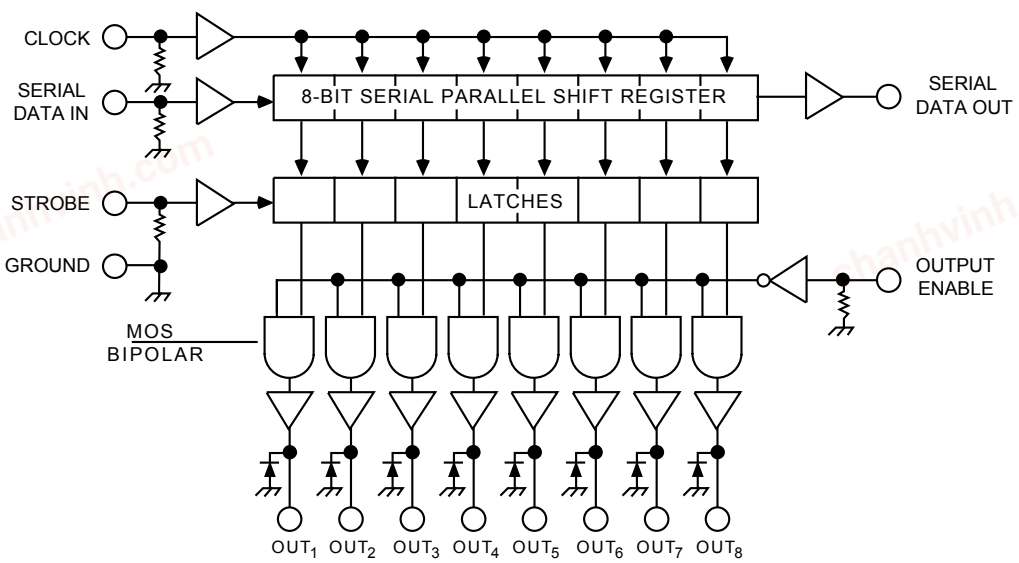
Features

- High-voltage, high-current outputs
- Output transient protection diodes
- CMOS-, PMOS-, NMOS-, and TTL-compatible inputs
- 5MHz typical data input rate
- Low-power CMOS latches

Applications

- Alphanumeric and bar graph displays
- LED and incandescent displays
- Relay and solenoid drivers
- Other high-power loads

Functional Diagram

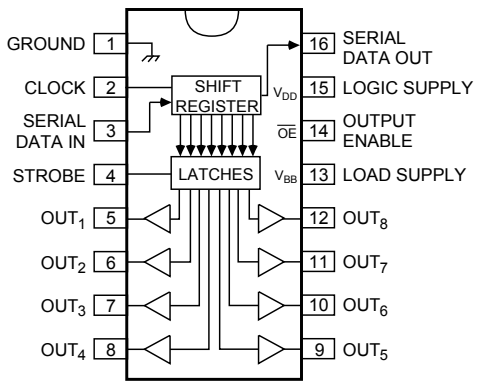


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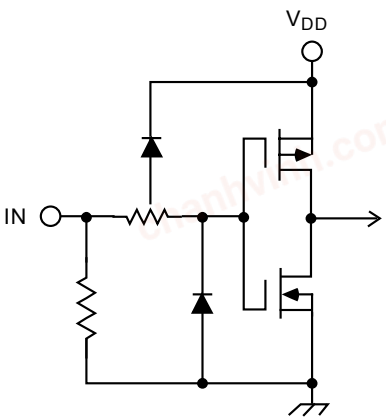
Ordering Information

Part Number		Temperature Range	Package
Standard	Pb-Free		
MIC5891BN	MIC5891YN	–40°C to +85°C	16-Pin Plastic DIP
MIC5891BWM	MIC5891YWM	–40°C to +85°C	16-Pin Wide SOIC

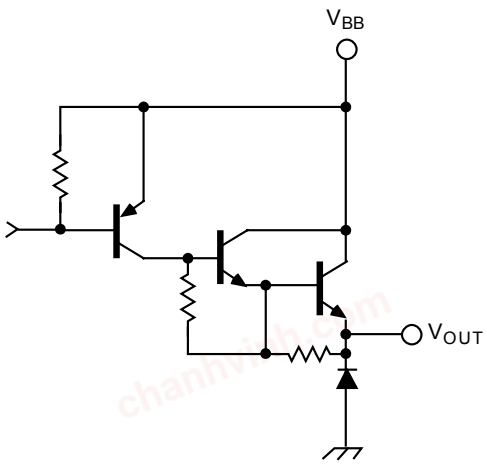
Pin Configuration



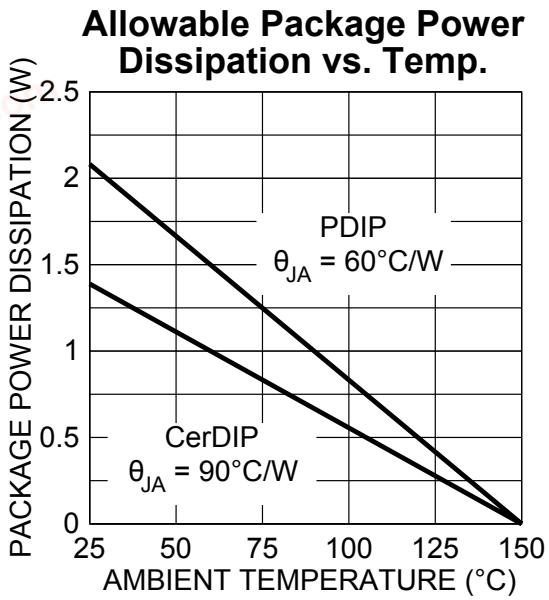
Typical Circuits



Typical Input Circuit



Typical Output Circuit



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Absolute Maximum Ratings (Notes 1, 2, 3)

Output Voltage (V_{OUT}) 50V
Logic Supply Voltage Range (V_{DD}) ..... 4.5V to 15V
Load Supply Voltage Range (V_{BB}) ..... 5.0V to 50V
Input Voltage Range (V_{IN}) ..... –0.3V to V_{DD}+0.3V
Continuous Collector Current (I_C) 500mA
Package Power Dissipation ..... *see graph*
Operating Temperature Range (T_A) ..... –55°C to +125°C
Storage Temperature Range (T_S) ..... –65°C to +150°C

Note 1: T_A = 25°C

Note 2: Derate at the rate of 20mW/°C above T_A = 25°C.

Note 3: Micrel CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Allowable Duty Cycles

Number of Outputs ON at I_{OUT} = –200 mA	Max. Allowable Duty Cycles at T_A of:		
	50°C	60°C	70°C
8	53%	47%	41%
7	60%	54%	48%
6	70%	64%	56%
5	83%	75%	67%
4	100%	94%	84%
3	100%	100%	100%
2	100%	100%	100%
1	100%	100%	100%

Electrical Characteristics

V_{BB} = 50V, V_{DD} = 5V to 12V; T_A = +25°C; unless noted.

Characteristic	Symbol	V_{BB}	Test Conditions	Limits		
				Min.	Max.	Units
Output Leakage Current	I_{CEX}	50V	T_A = +25°C		–50	µA
			T_A = +85°C		–100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	50V	I_{OUT} = –100mA, T_A = +85°C		1.8	V
			I_{OUT} = –225mA, T_A = +85°C		1.9	V
			I_{OUT} = –350mA, T_A = +85°C		2.0	V
Output Sustaining Voltage	$V_{CE(SUS)}$	50V	I_{OUT} = –350mA, L = 2mH	35		V
Input Voltage	$V_{IN(1)}$	50V	V_{DD} = 5.0V	3.5	V_{DD}+0.3	V
			V_{DD} = 12V	10.5	V_{DD}+0.3	V
	$V_{IN(0)}$	50V	V_{DD} = 5V to 12V	V_{SS}–0.3	0.8	V
Input Current	$I_{IN(1)}$	50V	V_{DD} = V_{IN} = 5.0V		50	µA
			V_{DD} = 12V		240	µA
Input Impedance	Z_{IN}	50V	V_{DD} = 5.0V	100		kΩ
			V_{DD} = 12V	50		kΩ
Maximum Clock Frequency	f_c	50V		3.3		MHz
Serial Data Output Resistance	R_{OUT}	50V	V_{DD} = 5.0V		20	kΩ
			V_{DD} = 12V		6.0	kΩ
Turn-On Delay	t_{PLH}	50V	Output Enable to Output, I_{OUT} = –350mA		2.0	µs
Turnoff Delay	t_{PHL}	50V	Output Enable to Output, I_{OUT} = –350mA		10	µs
Supply Current	I_{BB}	50V	all outputs on, all outputs open		10	mA
			all outputs off		200	µA
	I_{DD}	50V	V_{DD} = 5V, all outputs off, inputs = 0V		100	µA
			V_{DD} = 12V, all outputs off, inputs = 0V		200	µA
			V_{DD} = 5V, one output on, all inputs = 0V		1.0	mA
			V_{DD} = 12V, one output on, all inputs = 0V		3.0	mA
Diode Leakage Current	I_H	Max	T_A = +25°C		50	µA
			T_A = +85°C		100	µA
Diode Forward Voltage	V_F	Open	I_F = 350mA		2.0	V

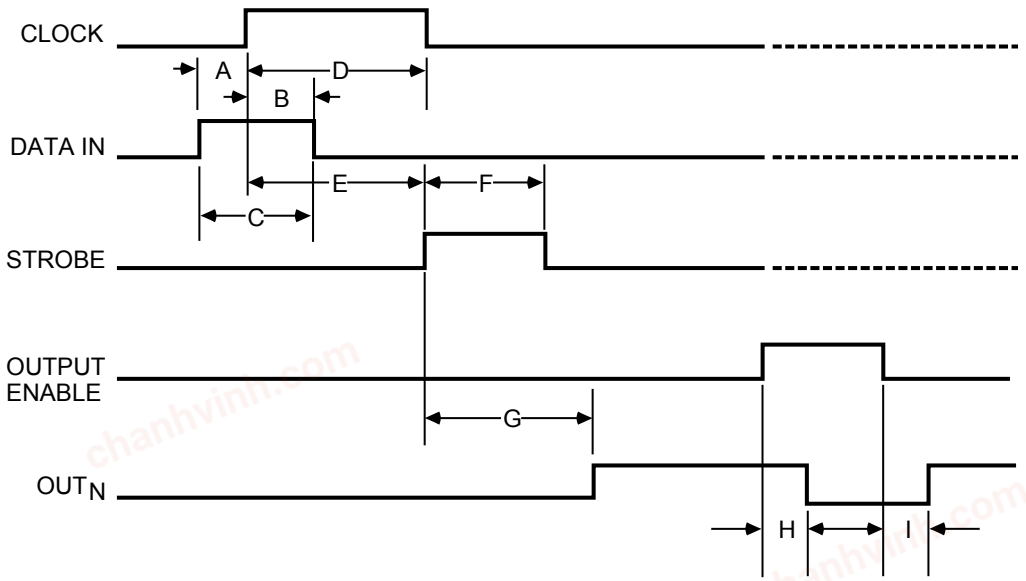
Note 4: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Note 5: Operation of these devices with standard TTL may require the use of appropriate pull-up resistors.

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Timing Conditions

(V_{DD} = 5.0V, Logic Levels are V_{DD} and Ground)

A. Minimum data active time before clock pulse (data set-up time) 75ns
B. Minimum data active time after clock pulse (data hold time) 75ns
C. Minimum data pulse width 150ns
D. Minimum clock pulse width 150ns
E. Minimum time between clock activation and strobe 300ns
F. Minimum strobe pulse width 100ns
G. Typical time between strobe activation and output transition 1.0µs
H. Turnoff delay ..... see Electrical Characteristics
I. Turn-on delay ..... see Electrical Characteristics



Timing Conditions

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Truth Table

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Output Enable	Output Content
		I_1 I_2 I_3 … I_{N-1} I_N			I_1 I_2 I_3 … I_{N-1} I_n		I_1 I_2 I_3 … I_{N-1} I_n
H	⎍	H R_1 R_2 … R_{N-2} R_{N-1}	R_{N-1}				
L	⎍	L R_1 R_2 … R_{N-2} R_{N-1}	R_{N-1}				
X	⎎	R_1 R_2 R_3 … R_{N-1} R_N	R_N				
		X X X … X X	X	L	R_1 R_2 R_3 … R_{N-1} R_N		
		P_1 P_2 P_3 … P_{N-1} P_N	P_N	H	P_1 P_2 P_3 … P_{N-1} P_N	L	P_1 P_2 P_3 … P_{N-1} P_N
					X X X … X X	H	L L L … L L

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

Applications Information

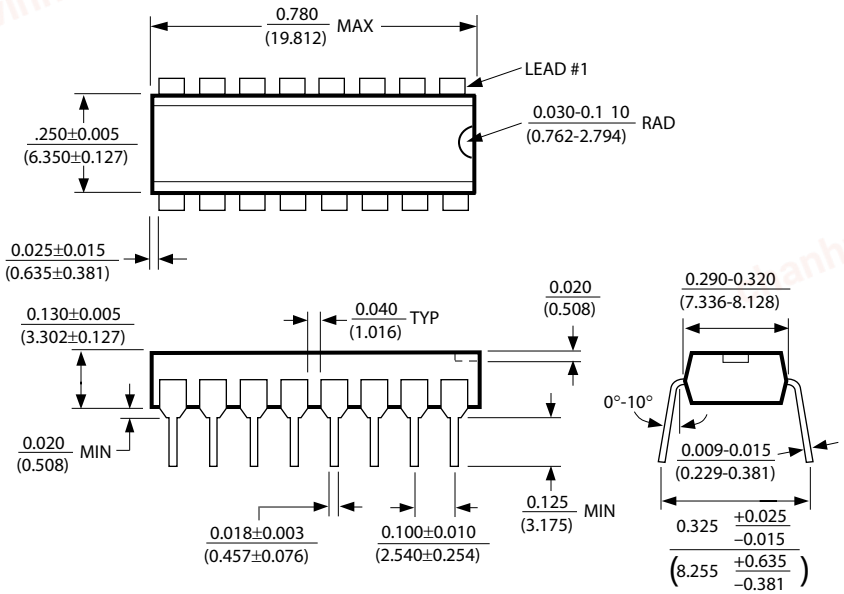
Serial data present at the input is transferred into the shift register on the rising edge of the CLOCK input pulse. Additional CLOCK pulses shift data information towards the SERIAL DATA OUTPUT. The serial data must appear at the input prior to the rising edge of the CLOCK input waveform.

The 8 bits present in the shift register are transferred to the respective latches when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Most applications where the latching feature is not used (STROBE tied high) require the OUTPUT ENABLE input to be high during serial data entry.

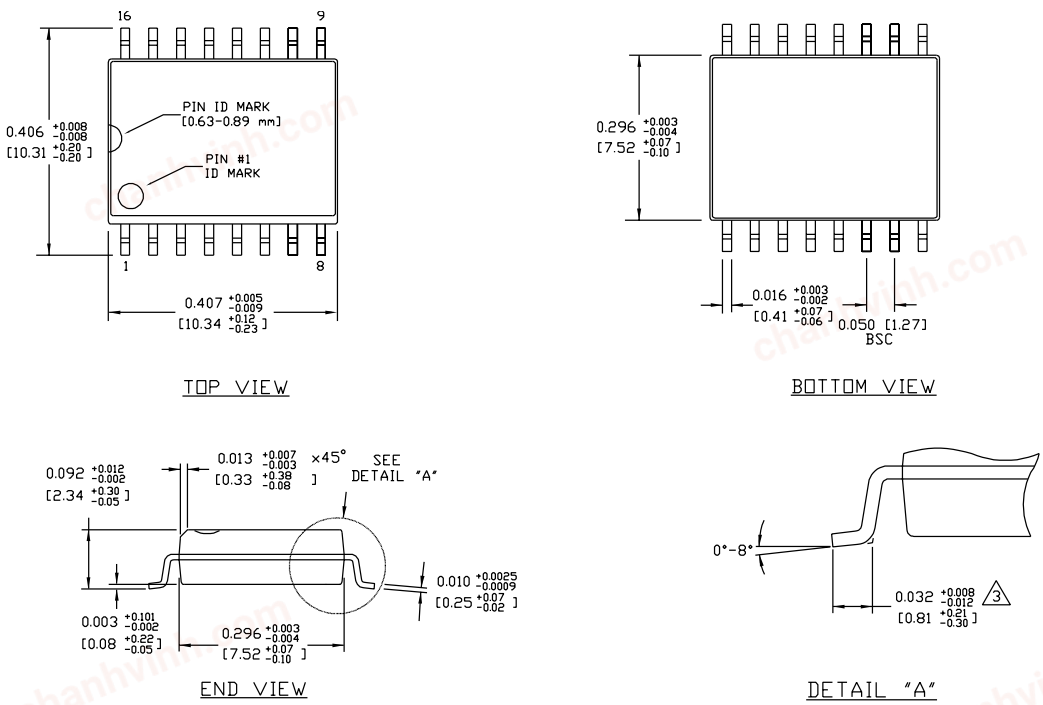
Outputs are active (controlled by the latch state) when the OUTPUT ENABLE is low. All Outputs are low (disabled) when the OUTPUT ENABLE is high. OUTPUT ENABLE does not affect the data in the shift register or latch.

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Package Information



16-Pin Plastic DIP (N)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.15] PER SIDE.

16-Pin Wide SOIC (WM)

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