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MIC4607A

85V, Three-Phase MOSFET Driver with Adaptive Dead-Time, Anti-Shoot-Through and Overcurrent Protection

Features

- Gate Drive Supply Voltage up to 16V
- Enhanced Overcurrent Protection with Add Blanking Time
- Drives High-Side and Low-Side N-Channel MOSFETs with Independent Inputs or with a Single PWM Signal
- TTL Input Thresholds
- On-Chip Bootstrap Diodes
- Fast 35 ns Propagation Times
- Shoot-Through Protection
- Drives 1000 pF Load with 20 ns Rise and Fall Times
- Low Power Consumption
- Supply Undervoltage Protection
- -40°C to +125°C Junction Temperature Range
- Qualified According to AEC-Q100 and AEC-Q006

Applications

- Three-Phase and BLDC Motor Drives
- Three-Phase Inverters
- Automotive BLDC Motor Applications

General Description

The MIC4607A is an 85V, three-phase MOSFET driver. The MIC4607A features a fast (35 ns) propagation delay time and a 20 ns driver rise/fall time for a 1 nF capacitive load. TTL inputs can be separate high- and low-side signals or a single PWM input with high and low drive generated internally. High- and low-side outputs are guaranteed to not overlap in either mode.

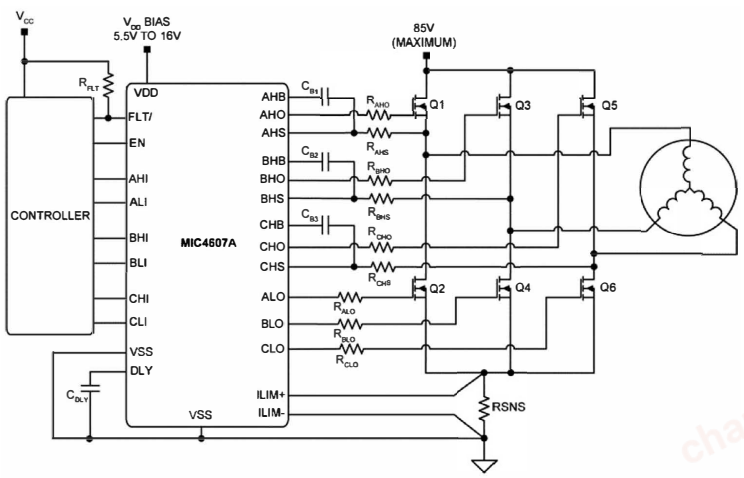
The MIC4607A includes overcurrent protection with blanking time insertion as well as a high-voltage internal diode that charges the high-side gate drive bootstrap capacitor.

The high-speed and low-power level shifter provides clean level transitions to the high-side output. The robust operation of the MIC4607A ensures that the outputs are not affected by supply glitches, HS ringing below ground, or HS slewing with high-speed voltage transitions. Undervoltage protection is provided on both the low-side and high-side drivers.

The MIC4607A is available in a 28-pin 4 mm x 5 mm VQFN package with wettable flanks in Moisture Sensitivity Level 1. The operating junction temperature range is between -40°C and +125°C.

Typical Application Circuit

MIC4607A
Three-Phase Motor Driver



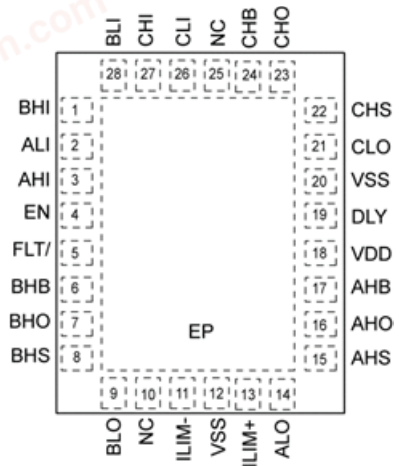
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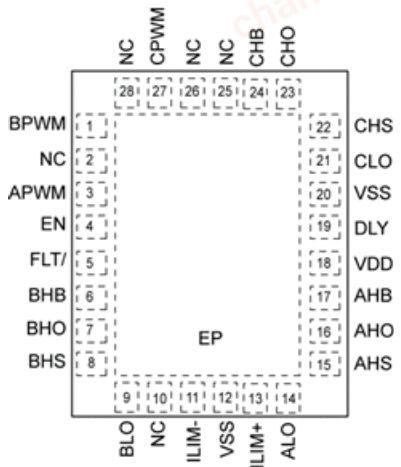
MIC4607A

Package Type

MIC4607A-1
28-pin VQFN



MIC4607A-2
28-pin VQFN

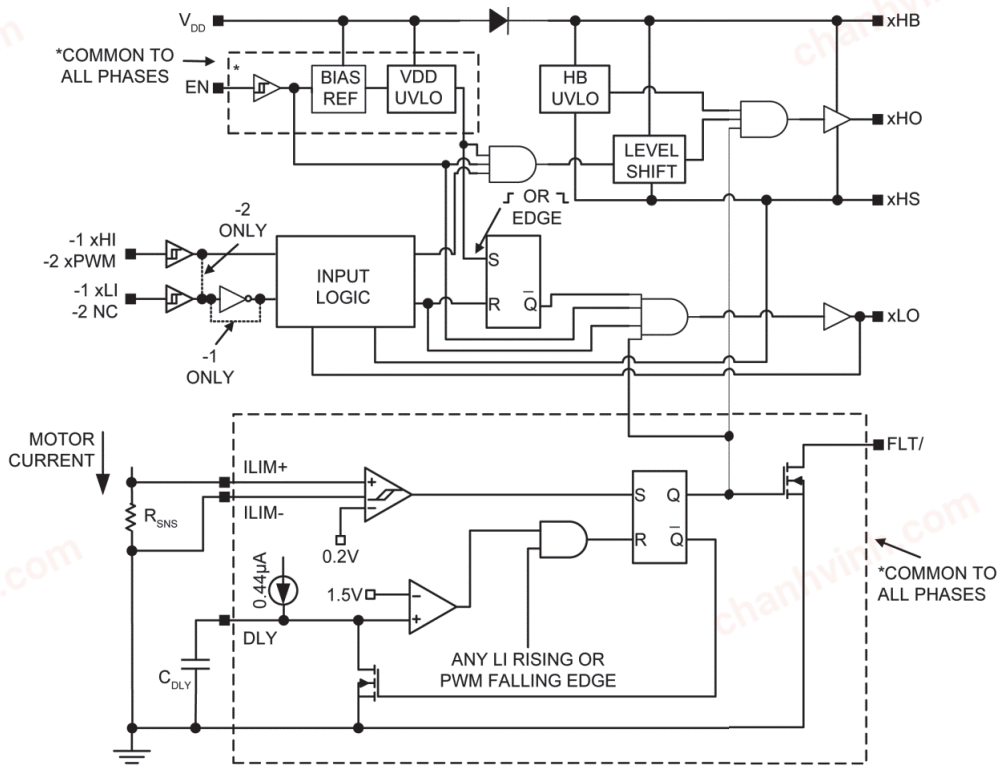


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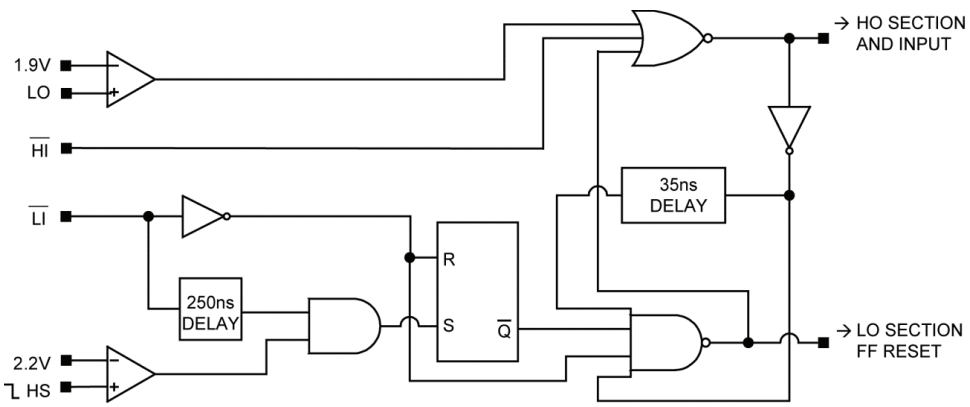
Functional Diagram

MIC4607A xPhase Top-Level Functional Diagram



NOTE:
x = A, B, OR C
-1 = MIC4607-1
-2 = MIC4607-2

Input Logic Block



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †, (Note 2)

Supply Voltage (V_{DD}, V_{xHB} – V_{xHS}) ..... -0.3V to 18V
Input Voltages (V_{xLI}, V_{xHI}, V_{xPWM}, V_{EN}) ..... -0.3V to V_{DD} + 0.3V
FLT/ Pin ..... -0.3V to V_{DD} + 0.3V
DLY Pin ..... -0.3V to 18V
Voltage on xLO (V_{xLO}) ..... -0.3V to V_{DD} + 0.3V
Voltage on xHO (V_{xHO}) ..... V_{HS} – 0.3V to V_{HB} + 0.3V
Voltage on xHS (Continuous) ..... -0.3V to 90V
Voltage on xHB 108V
ILIM+ ..... -0.3V to +5V
ILIM– ..... -0.3V to +2V
Average Current in V_{DD} to HB Diode ..... 100 mA
ESD Protection on All Pins (Note 1):
HBM ..... ±1 kV
CDM Corner Pins ..... ±750V
CDM All Other Pins ..... ±500V

Operational Characteristics ††, (Note 2)

Supply Voltage (V_{DD}), [decreasing V_{DD}] ..... 5.25V to 16V
Supply Voltage (V_{DD}), [increasing V_{DD}] ..... 5.5V to 16V
Voltage on xHS ..... -0.3V to 85V
Voltage on xHS (repetitive transient <100 ns) ..... -0.7V to 90V
ILIM+ to VSS (Continuous) ..... -0.25V to +1V
ILIM- to VSS (Continuous) ..... -0.25V to +1V
ILIM+ to ILIM- (Continuous) ..... -0.25V to +1V
HS Slew Rate ..... 50 V/ns
Voltage on xHB ..... V_{HS} + 5.5V to V_{HS} + 16V
and/or ..... V_{DD} –1V to V_{DD} +85V

† **Notice**: Exceeding the absolute maximum ratings may damage the device.
†† **Notice**: The device is not guaranteed to function outside its operating ratings

Note 1: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.
2: An “x” in front of a pin name refers to either A, B or C phase (e.g. xHI can be either AHI, BHI or CHI).

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DC CHARACTERISTICS (Note 1, 2)

Electrical Characteristics: Unless otherwise indicated, V_{DD} = V_{xHB} = 12V; V_{EN} = 5V; V_{SS} = V_{HS} = 0V; No load on xLO or xHO; T_A = 25°C; unless noted. **Bold** values indicate -40°C< T_J < +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Current						
V_{DD} Quiescent Current	I_{DD}	—	390	**750**	µA	xLI = xHI = 0V
V_{DD} Shutdown Current	I_{DDSH}	—	2.2	**10**	µA	xLI = xHI = 0V; EN = 0V with HS = floating
		—	58	**150**		xLI = xHI = 0V; EN = 0V; HS = 0V
V_{DD} Operating Current	I_{DDO}	—	0.6	**1.5**	mA	f = 20 kHz
Per Channel xHB Quiescent Current	I_{HB}	—	20	**75**	µA	xLI = xHI = 0V or xLI = 0V and xHI = 5V
Per Channel xHB Operating Current	I_{HBO}	—	30	**400**	µA	f = 20 kHz
xHB to V_{SS} Current, Quiescent	I_{HBS}	—	0.05	5	µA	V_{xHS} = V_{xHB} = 90V
xHB to V_{SS} Current, Operating	I_{HBSO}	—	30	—	µA	f = 20 kHz
Input (xLI, xHI, xPWM, EN) (Note 3)						
Low-Level Input Voltage	V_{IL}	—	—	**0.8**	V	—
High-Level Input Voltage	V_{IH}	**2.2**	—	—	V	—
Input Voltage Hysteresis	V_{HYS}	—	0.1	—	V	—
Input Pull-Down Resistance	R_I	**100**	300	**500**	kΩ	xLI and xHI Inputs (-1 Version)
		50	130	**250**		xPWM Input (-2 Version)
Undervoltage Protection						
V_{DD} Falling Threshold	V_{DDF}	**3.8**	4.4	**4.9**	V	—
V_{DD} Threshold Hysteresis	V_{DDH}	—	0.25	—	V	—
xHB Falling Threshold	V_{HBF}	**4.0**	4.4	**4.9**	V	—
xHB Threshold Hysteresis	V_{HBH}	—	0.25	—	V	—
Overcurrent Protection						
Rising Overcurrent Threshold	V_{ILIM+}	175	200	225	mV	(V_{ILIM+} – $V_{ILIM–}$)
ILIM Filter Time	t_{F_ILIM}	800	1000	1200	ns	V_{ILIM+} = 0.5V peak
ILIM to Gate Propagation Delay	t_{ILIM_PROP}	—	1100	—	ns	V_{ILIM+} = 0.5V peak
Fault Circuit						
FLT/ Output Low Voltage	V_{OLF}	—	0.2	0.5	V	V_{ILIM} = 1V; $I_{FLT/}$ = 1 mA
Rising DLY Threshold	V_{DLY+}	—	1.5	—	V	—
DLY Current Source	I_{DLY}	0.3	0.44	0.6	µA	V_{DLY} = 0V
Fault Clear Time	t_{FCL}	—	670	—	µs	C_{DLY} = 1 nF
Bootstrap Diode						
Low-Current Forward Voltage	V_{DL}	—	0.4	**0.70**	V	$I_{VDD-xHB}$ = 100 µA

Note 1: "x" in front of a pin name refers to either A, B or C phase. (e.g. xHI can be either AHI, BHI or CHI).

2: Specification for packaged product only.

3: $V_{IL(MAX)}$ = maximum positive voltage applied to the input which will be accepted by the device as a logic low.
$V_{IH(MIN)}$ = minimum positive voltage applied to the input which will be accepted by the device as a logic high.

4: Guaranteed by design. Not production tested.

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DC CHARACTERISTICS (Note 1, 2) (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, V_{DD} = V_{xHB} = 12V; V_{EN} = 5V; V_{SS} = V_{HS} = 0V; No load on xLO or xHO; T_A = 25°C; unless noted. **Bold** values indicate -40°C< T_J < +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
High-Current Forward Voltage	V_{DH}	—	0.8	**1**	V	$I_{VDD-xHB}$ = 50 mA
Dynamic Resistance	R_D	—	4	**7**	Ω	—
xLO Gate Driver						
Low-Level Output Voltage	V_{OLL}	—	0.3	**0.6**	V	I_{xLO} = 50 mA
High-Level Output Voltage	V_{OHL}	—	0.5	**1**	V	I_{xLO} = –50 mA, V_{OHL} = V_{DD} – V_{xLO}
Peak Sink Current	I_{OHL}	—	1	—	A	V_{xLO} = 0V
Peak Source Current	I_{OLL}	—	1	—	A	V_{xLO} = 12V
xHO Gate Driver						
Low-Level Output Voltage	V_{OLH}	—	0.3	0.6	V	I_{xHO} = 50 mA
High-Level Output Voltage	V_{OHH}	—	0.5	1	V	I_{xHO} = -50 mA, V_{OHH} = V_{xHB} – V_{xHO}
Peak Sink Current	I_{OHH}	—	1	—	A	V_{xHO} = 0V
Peak Source Current	I_{OLH}	—	1	—	A	V_{xHO} = 12V
Switching Specifications (LI/HI mode with inputs non-overlapping, assumes HS low before LI goes high and LO low before HI goes high).						
Lower Turn-Off Propagation Delay (LI Falling to LO Falling)	t_{LPHL}	—	35	**75**	ns	—
Upper Turn-Off Propagation Delay (HI Falling to HO Falling)	t_{HPHL}	—	35	**75**	ns	—
Lower Turn-On Propagation Delay (LI Rising to LO Rising)	t_{LPLH}	—	35	**75**	ns	—
Upper Turn-On Propagation Delay (HI Rising to HO Rising)	t_{HPLH}	—	35	**75**	ns	—
Output Rise/Fall Time	$t_{R/F}$	—	20	—	ns	C_L = 1000 pF
Output Rise/Fall Time (3V to 9V)	$t_{R/F}$	—	0.8	—	µs	C_L = 0.1 µF
Minimum Input Pulse Width that Changes the Output	t_{PW}	—	50	—	ns	Note 4
Switching Specifications PWM Mode (MIC4607A-2) or LI/HI mode (MIC4607A-1) with Overlapping LI/HI Inputs						
Delay from PWM Going High / LI Low, to LO Going Low	t_{LOOFF}	—	35	**75**	ns	—
LO Output Voltage Threshold for LO FET to be Considered Off	V_{LOOFF}	—	1.9	—	V	—
Delay from LO Off to HO Going High	t_{HOON}	—	35	**75**	ns	—
Delay from PWM or HI Going Low to HO Going Low	t_{HOOFF}	—	35	**75**	ns	—

Note 1: "x" in front of a pin name refers to either A, B or C phase. (e.g. xHI can be either AHI, BHI or CHI).

2: Specification for packaged product only.

3: $V_{IL(MAX)}$ = maximum positive voltage applied to the input which will be accepted by the device as a logic low.

$V_{IH(MIN)}$ = minimum positive voltage applied to the input which will be accepted by the device as a logic high.

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DC CHARACTERISTICS (Note 1, 2) (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, V_{DD} = V_{xHB} = 12V; V_{EN} = 5V; V_{SS} = V_{HS} = 0V; No load on xLO or xHO; T_A = 25°C; unless noted. **Bold** values indicate -40°C< T_J < +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Switch Node Voltage Threshold Signaling HO is Off	V_{SWTH}	1	2.2	**4**	V	—
Delay between HO FET Being Considered Off to LO Turning On	t_{LOON}	—	35	**75**	ns	—
Forced xLO On if V_{SWTH} is Not Detected	t_{SWTO}	**100**	250	**500**	ns	—

Note 1: "x" in front of a pin name refers to either A, B or C phase. (e.g. xHI can be either AHI, BHI or CHI).

2: Specification for packaged product only.

3: $V_{IL(MAX)}$ = maximum positive voltage applied to the input which will be accepted by the device as a logic low.
$V_{IH(MIN)}$ = minimum positive voltage applied to the input which will be accepted by the device as a logic high.

4: Guaranteed by design. Not production tested.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{IN} = V_{EN} = 12V, V_{BOOST} – V_{SW} = 3.3V, V_{OUT} = 3.3V

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_J	-40	—	+125	°C	—
Lead Temperature	—	—	260	—	°C	Soldering, 10s
Storage Temperature Range	T_S	-60	—	+150	°C	—
Maximum Junction Temperature	T_J	—	—	+125	°C	—
Package Thermal Resistances						
Thermal Resistance, 4 mm × 5 mm, VQFN-28	θ_{JA}	—	43	—	°C/W	—
Thermal Resistance, 4 mm × 5 mm, VQFN-28	θ_{JC}	—	5	—	°C/W	—

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

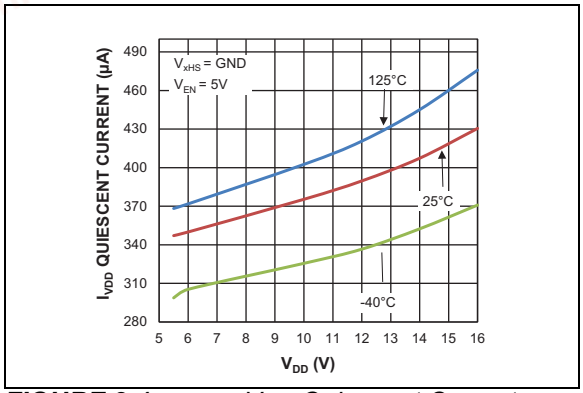


FIGURE 2-1: *V_{DD} Quiescent Current vs. V_{DD} Voltage.*

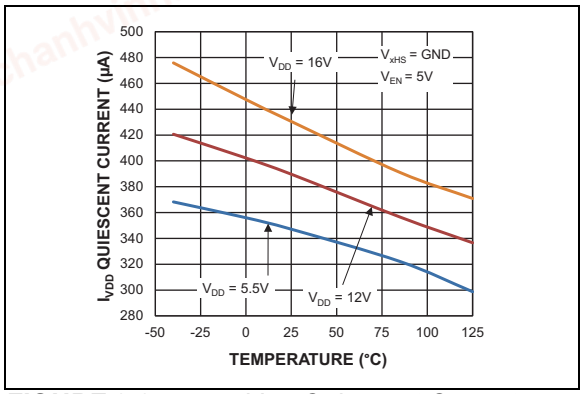


FIGURE 2-2: *V_{DD} Quiescent Current vs. Temperature.*

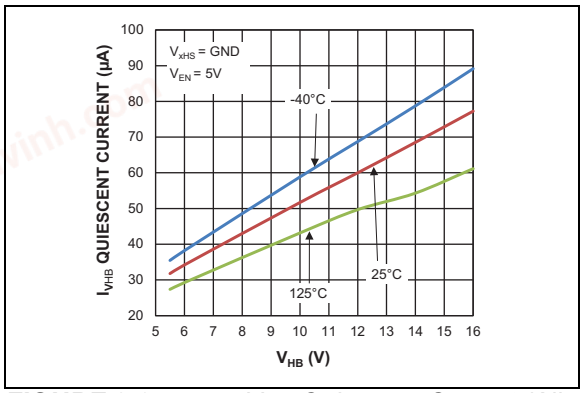


FIGURE 2-3: *V_{HB} Quiescent Current (All Channels) vs. V_{HB} Voltage.*

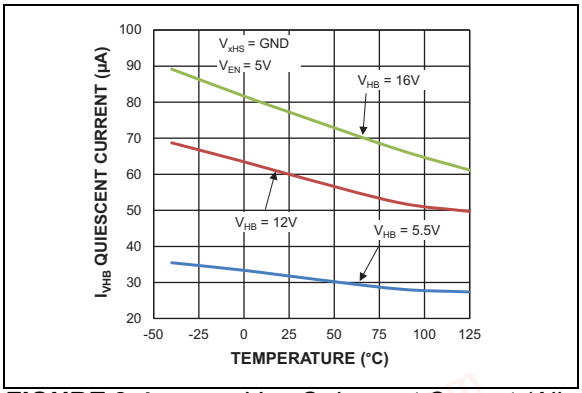


FIGURE 2-4: *V_{HB} Quiescent Current (All Channels) vs. Temperature.*

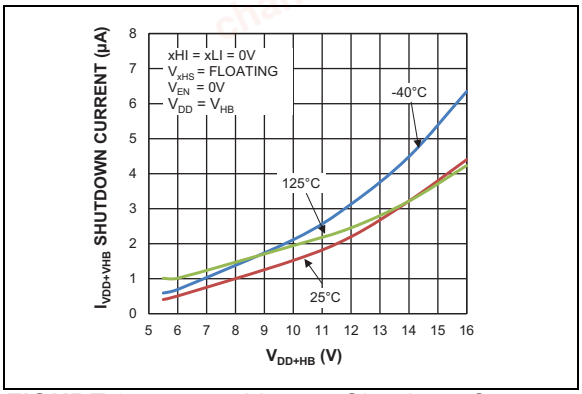


FIGURE 2-5: *V_{DD+HB} Shutdown Current (Floating Switch Node) vs. Voltage.*

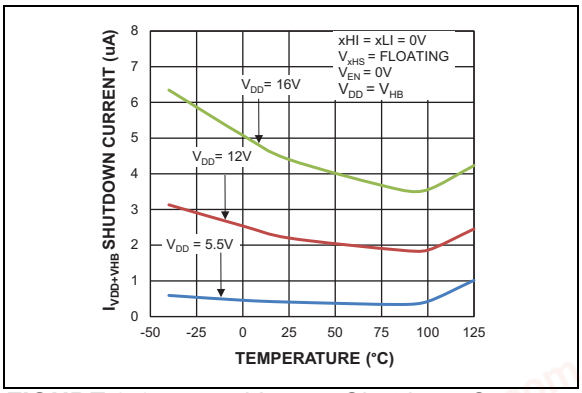


FIGURE 2-6: *V_{DD+HB} Shutdown Current (Floating Switch Node) vs. Temperature.*

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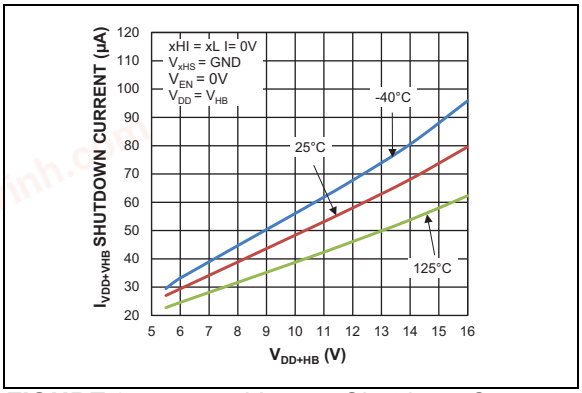


FIGURE 2-7: *V_{DD+HB} Shutdown Current (Grounded Switch Node) vs. Voltage.*

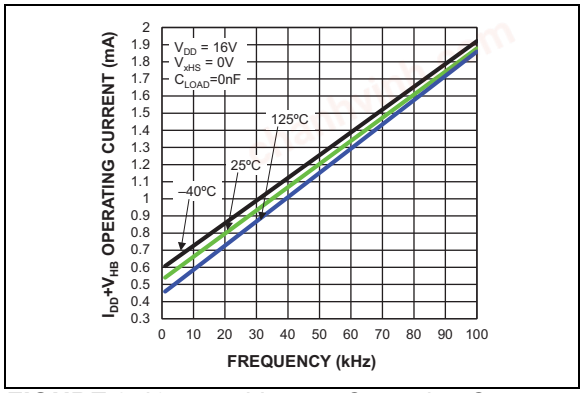


FIGURE 2-10: *V_{DD+HB} Operating Current vs. Switching Frequency.*

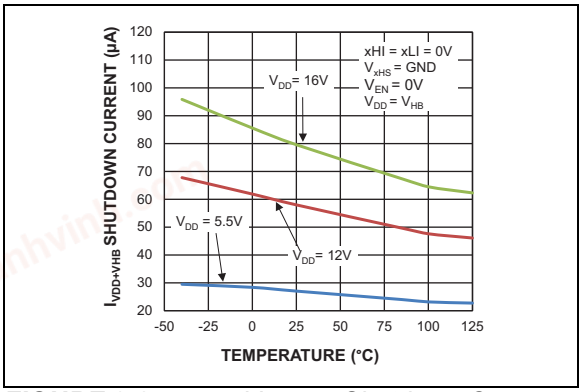


FIGURE 2-8: *V_{DD+HB} Shutdown Current (Grounded Switch Node) vs. Temperature.*

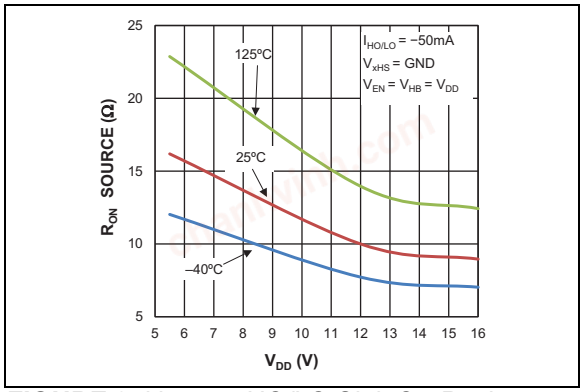


FIGURE 2-11: *HO/LO Sink On-Resistance vs. V_{DD}.*

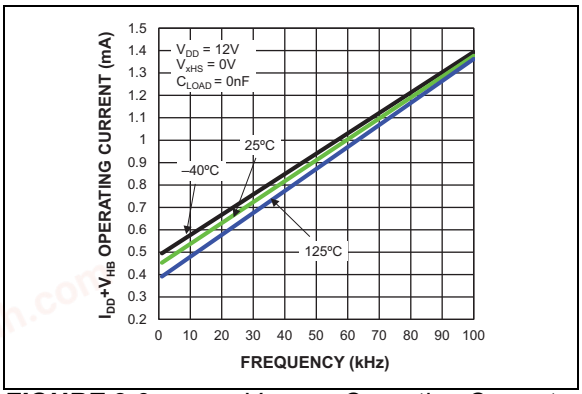


FIGURE 2-9: *V_{DD+HB} Operating Current vs. Switching Frequency.*

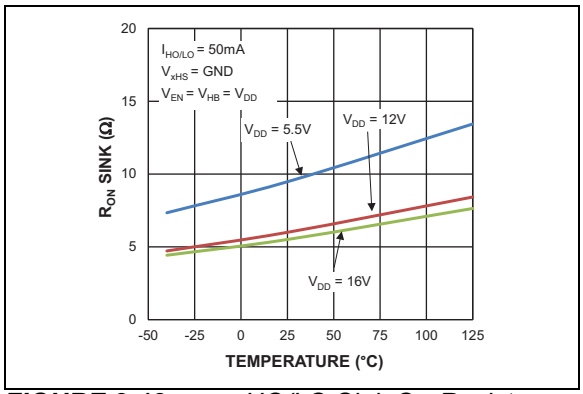


FIGURE 2-12: *HO/LO Sink On-Resistance vs. Temperature.*

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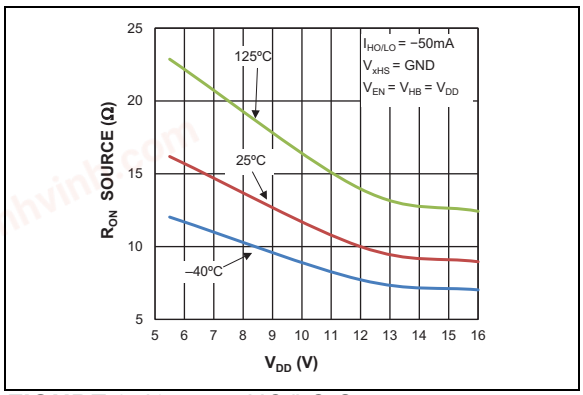


FIGURE 2-13: *HO/LO Source On-Resistance vs. V_{DD}.*

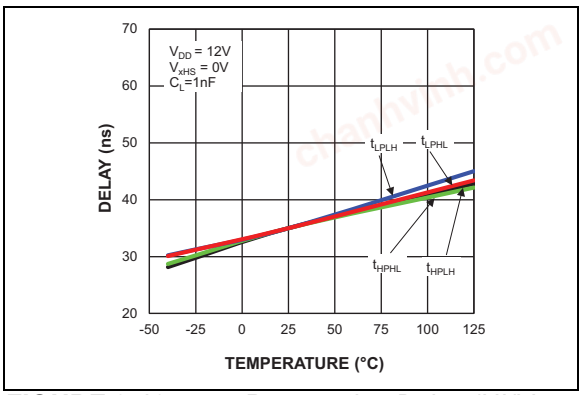


FIGURE 2-16: *Propagation Delay (HI/LI Input) vs. Temperature.*

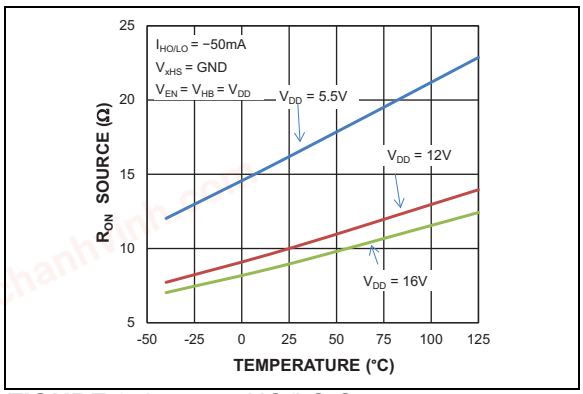


FIGURE 2-14: *HO/LO Source On-Resistance vs. Temperature.*

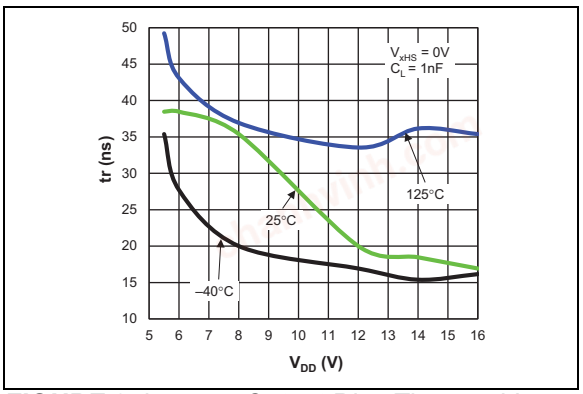


FIGURE 2-17: *Output Rise Time vs. V_{DD} Voltage.*

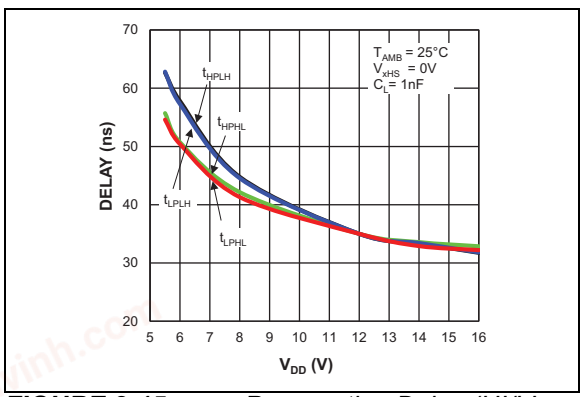


FIGURE 2-15: *Propagation Delay (HI/LI Input) vs. V_{DD} Voltage.*

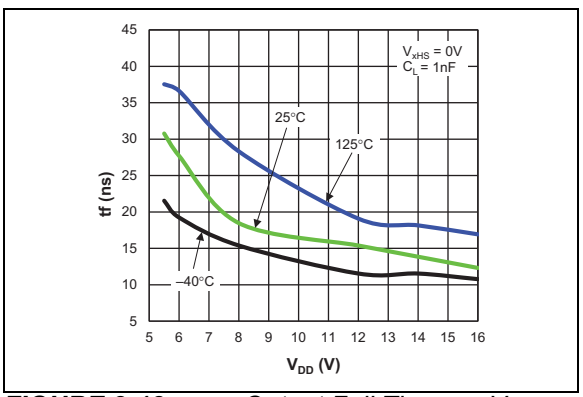


FIGURE 2-18: *Output Fall Time vs. V_{DD} Voltage.*

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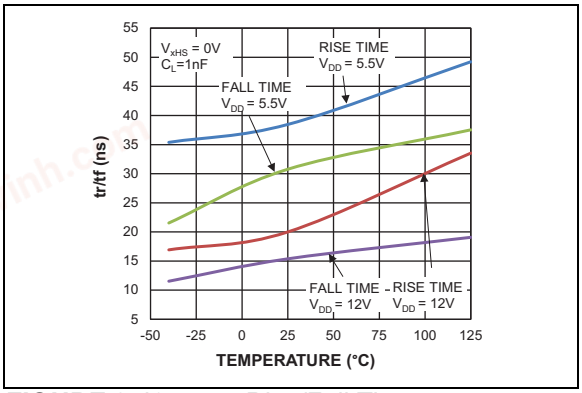


FIGURE 2-19: *Rise/Fall Time vs. Temperature.*

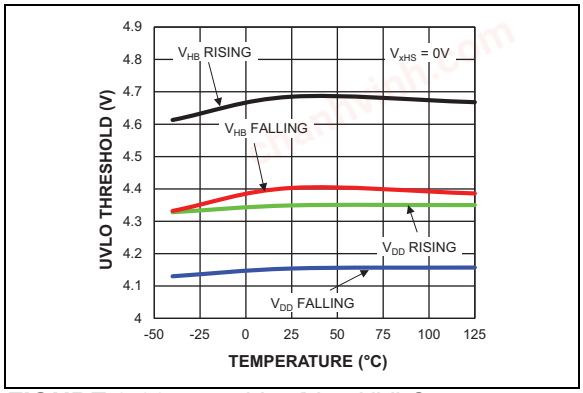


FIGURE 2-22: *V_{DD}/V_{HB} UVLO vs. Temperature.*

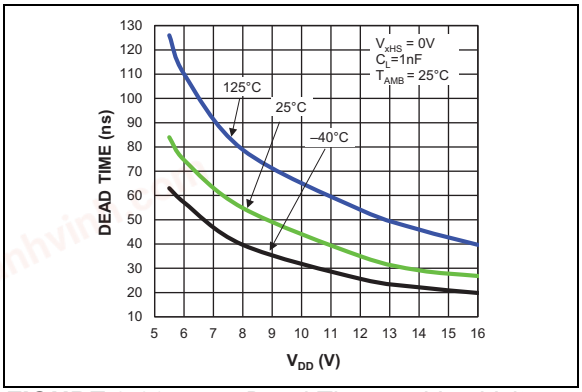


FIGURE 2-20: *Dead Time vs. V_{DD} Voltage.*

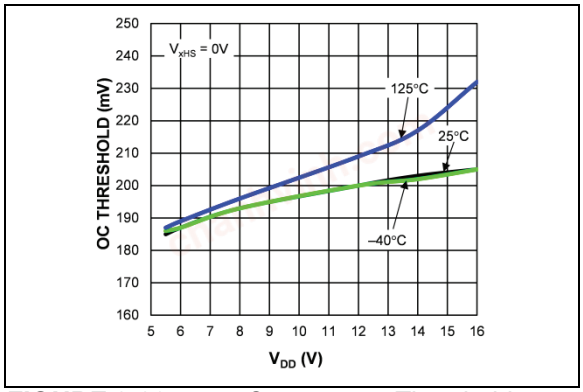


FIGURE 2-23: *Overcurrent Threshold vs. V_{DD} Voltage.*

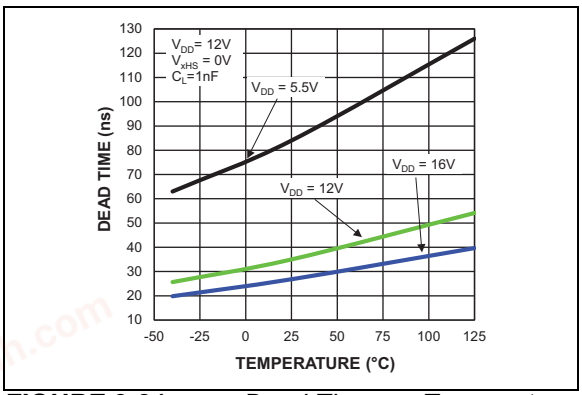


FIGURE 2-21: *Dead Time vs. Temperature.*

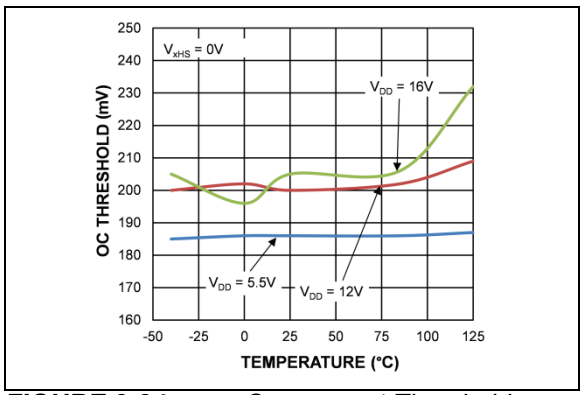


FIGURE 2-24: *Overcurrent Threshold vs. Temperature.*

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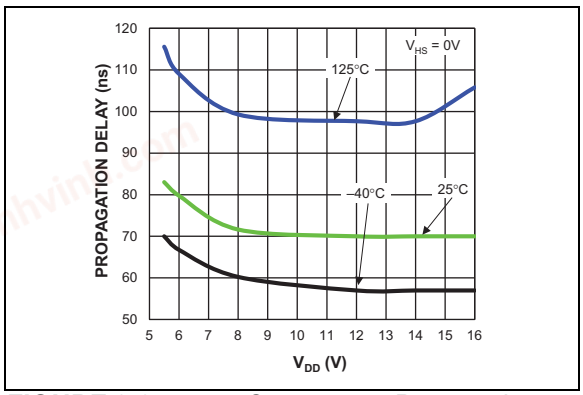


FIGURE 2-25: *Overcurrent Propagation Delay vs. V_{DD} Voltage.*

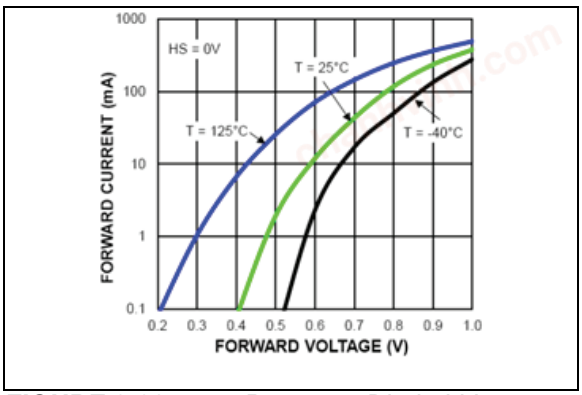


FIGURE 2-28: *Bootstrap Diode I-V Characteristics.*

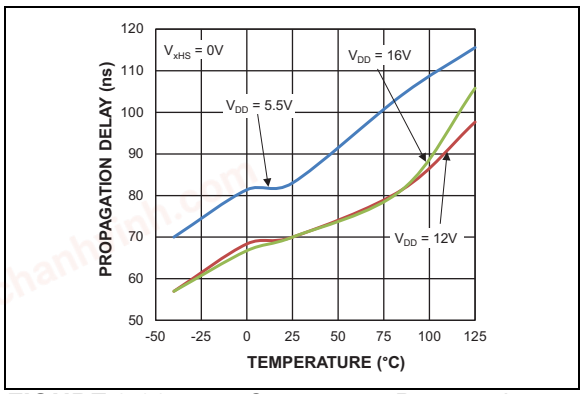


FIGURE 2-26: *Overcurrent Propagation Delay vs. Temperature.*

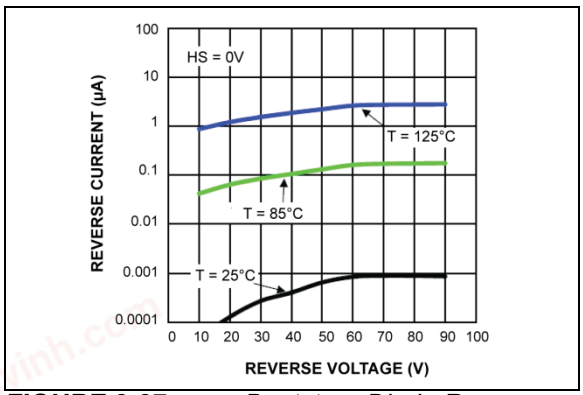


FIGURE 2-27: *Bootstrap Diode Reverse Current.*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins is listed in Table 3-1.

TABLE 3-1: VQFN PIN FUNCTION TABLE

Pin Number VQFN	Pin Name		Description
	MIC4607A-1	MIC4607A-2	
1	BHI	BPWM	High-side input (-1) or PWM input (-2) for Phase B.
2	ALI	NC	Low-side input (-1) or no connect (-2) for Phase A.
3	AHI	APWM	High-side input (-1) or PWM input (-2) for Phase A.
4	EN	EN	Active-high enable input. High input enables all outputs and initiates normal operation. Low input shuts down device into a low LQ mode.
5	FLT/	FLT/	Open-Drain. FLT/ pin goes low when outputs are latched off due to an overcurrent event. Must be pulled-up to an external voltage with a resistor.
6	BHB	BHB	Phase B High-Side Bootstrap Supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor across this pin and BHS. An on-board bootstrap diode is connected from V_{DD} to BHB.
7	BHO	BHO	Phase B High-Side Drive Output. Connect to the gate of the external high-side power MOSFET.
8	BHS	BHS	Phase B High-Side Driver Return. Connect to the bootstrap capacitor and to a resistor that connects to the source of the external MOSFET. See the Applications section for additional information on the resistor.
9	BLO	BLO	Phase B Low-Side Drive Output. Connect to the gate of the low-side power MOSFET gate.
10	NC	NC	No Connect.
11	ILIM-	ILIM-	Differential Current-Limit Input. Connect to the most negative end of the external current-sense resistor.
12	VSS	VSS	Power Ground for Phase A and Phase B.
13	ILIM+	ILIM+	Differential Current-Limit Input. Connect to most positive end of the external current-sense resistor.
14	ALO	ALO	Phase A Low-Side Drive Output. Connect to the gate of the low-side power MOSFET gate.
15	AHS	AHS	Phase A High-Side Driver Return. Connect to the bootstrap capacitor and to a resistor that connect to the source of the external MOSFET. See the Applications section for additional information on the resistor.
16	AHO	AHO	Phase A High Side Drive Output. Connect to the gate of the external high-side power MOSFET.
17	AHB	AHB	Phase A High-Side Bootstrap Supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor across this pin and AHS. An on-board bootstrap diode is connected from V_{DD} to AHB.
18	VDD	VDD	Input Supply for Gate Drivers and Internal Logic/Control Circuitry. Decouple this pin to V_{SS} with a minimum 2.2 µF ceramic capacitor.
19	DLY	DLY	Fault Delay. Connect an external capacitor from this pin to ground to increase the current-limit reset delay. Leave open for minimum delay. Do not externally drive this pin.
20	VSS	VSS	Phase C Power and Control Circuitry Ground.
21	CLO	CLO	Phase C Low-Side Drive Output. Connect to the gate of the low-side power MOSFET gate.
22	CHS	CHS	Phase C High-Side Driver Return. Connect to the bootstrap capacitor and to a resistor that connects to the source of the external MOSFET. See the Applications section for additional information on the resistor.

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TABLE 3-1: VQFN PIN FUNCTION TABLE (CONTINUED)

Pin Number VQFN	Pin Name		Description
	MIC4607A-1	MIC4607A-2	
23	CHO	CHO	Phase C High-Side Drive Output. Connects to the gate of the external high-side power MOSFET.
24	CHB	CHB	Phase C High-Side Bootstrap Supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor across this pin and CHS. An on-board bootstrap diode is connected from VDD to CHB.
25	NC	NC	No Connect.
26	CLI	NC	Low-Side Input (-1) or No Connect (-2) for Phase C.
27	CHI	CPWM	High-Side Input (-1) or PWM Input (-2) for Phase C.
28	BLI	NC	Low-Side Input (-1) or No Connect (-2) for Phase B.
EP	ePad	ePad	Exposed Heatsink Pad: Connect to GND for best thermal performance.

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4.0 TIMING DIAGRAMS

4.1 Non-Overlapping LI/HI Input Mode (MIC4607A-1)

In non-overlapping LI/HI input mode, enough delay is added between the xLI and xHI inputs to allow xHS to be low before xLI is pulled high and similarly xLO is low before xHI goes high.

xHO goes high with a high signal on xHI after a typical delay of 35 ns (t_{HPLH}). xHI going low drives xHO low also with typical delay of 35 ns (t_{HPHL}).

Likewise, xLI going high forces xLO high after typical delay of 35 ns (t_{LPLH}) and xLO follows low transition of xLI after typical delay of 35 ns (t_{LPHL}).

xHO and xLO output rise and fall times (t_R/t_F) are typically 20 ns driving 1000 pF capacitive loads.

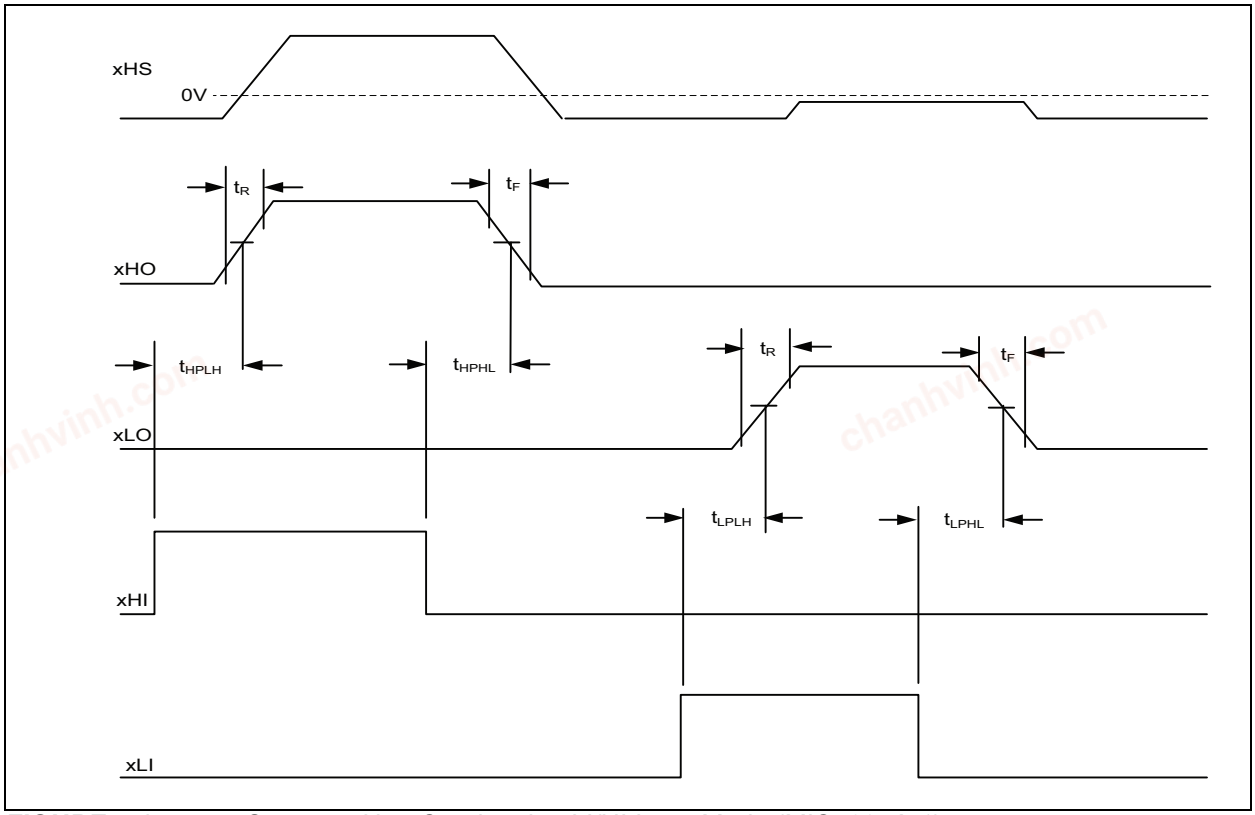


FIGURE 4-1: *Separate Non-Overlapping LI/HI Input Mode (MIC4607A-1).*

Note 1: All propagation delays are measured from the 50% voltage level and rise/fall times are measured 10% to 90%.

2: “x” in front of a pin name refers to either A, B or C phase (e.g. xHI can be either AHI, BHI or CHI).

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4.2 Overlapping LI/HI Input Mode (MIC4607A-1)

When xLI/xHI input high signals overlap, xLO/xHO output states are determined by the first output to be turned on. That is, if xLI goes high (ON), while xHO is high, xHO stays high until xHI goes low at which point, after a delay of t_{HOOFF} and when xHS < 2.2V, xLO goes high with a delay of t_{LOON}. Should xHS never trip the aforementioned internal comparator reference (2.2V), a falling xHI edge delayed by a typical 250 ns will set "HS latch" allowing xLO to go high.

If xHS falls very fast, xLO will be held low by a 35 ns delay gated by HI going low. Conversely, xHI going high (ON) when xLO is high has no effect on outputs until xLI is pulled low (off) and xLO falls to < 1.9V. Delay from xLI going low to xLO falling is t_{LOOFF} and delay from xLO < 1.9V to xHO being on is t_{HOON}.

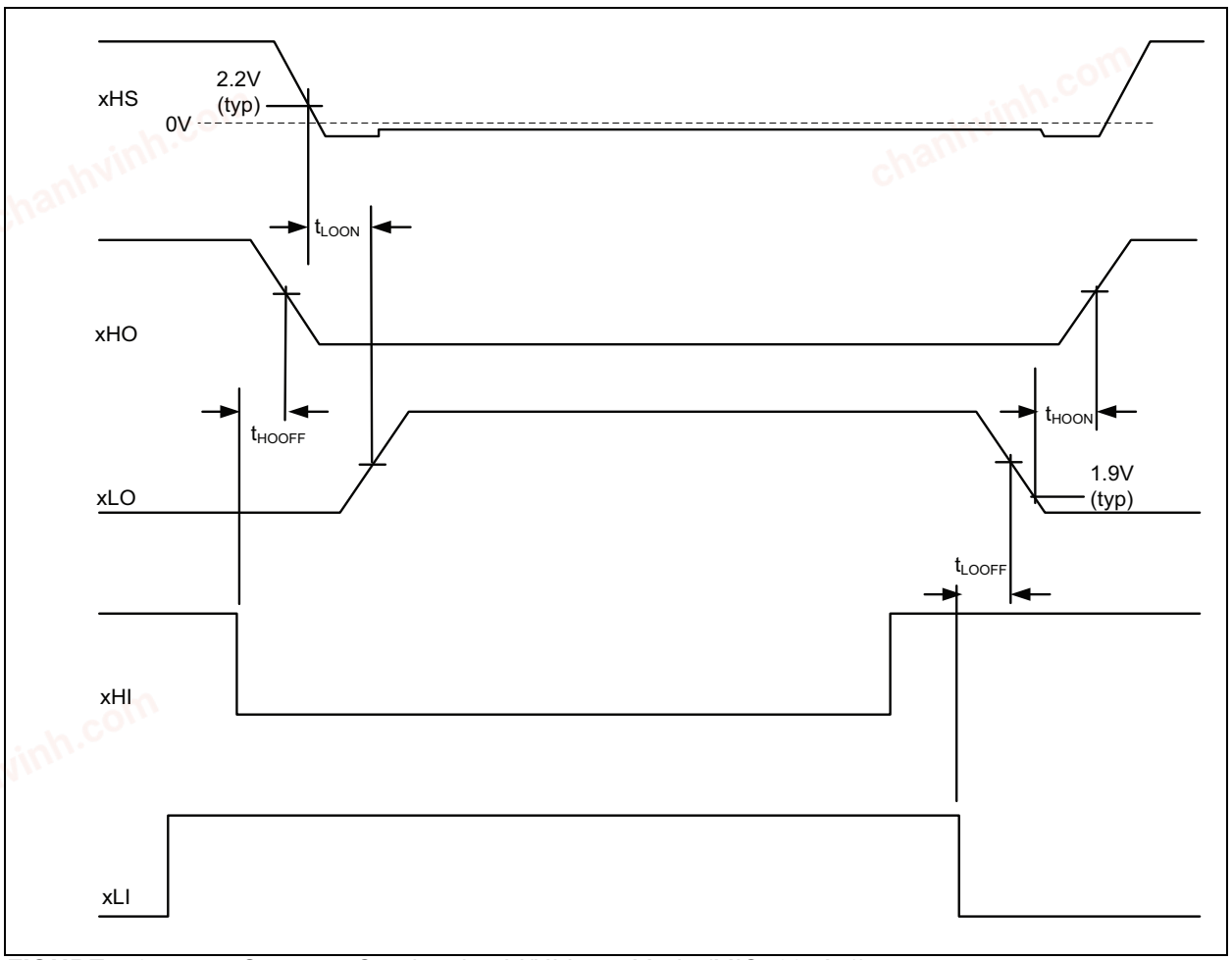


FIGURE 4-2: *Separate Overlapping LI/HI Input Mode (MIC4607A-1).*

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4.3 PWM Input Mode (MIC4607A-2)

A low going xPWM signal applied to the MIC4607A-2 causes xHO to go low, typically 35 ns (t_{HOOFF}) after the xPWM input goes low, at which point the switch node, xHS, falls (1-2).

When xHS reaches 2.2V (V_{SWTH}), the external high-side MOSFET is deemed off and xLO goes high, typically within 35 ns (t_{LOON}) (3-4). xHS falling below 2.2V sets a latch that can only be reset by xPWM going high. This design prevents ringing on xHS from causing an indeterminate xLO state. Should xHS never trip the aforementioned internal comparator reference (2.2V), a falling xPWM edge delayed by 250 ns will set “HS latch” allowing xLO to go high.

A 35 ns delay gated by xPWM going low can determine the time to xLO going high for fast falling HS designs. xPWM going high forces xLO low in typically 35ns (t_{LOOFF}) (5-6).

When xLO reaches 1.9V (V_{LOOFF}), the low-side MOSFET is deemed off and xHO is allowed to go high. The delay between these two points is typically 35 ns (t_{HOON}) (7-8).

xHO and xLO output rise and fall times (t_R/t_F) are typically 20 ns driving 1000 pF capacitive loads.

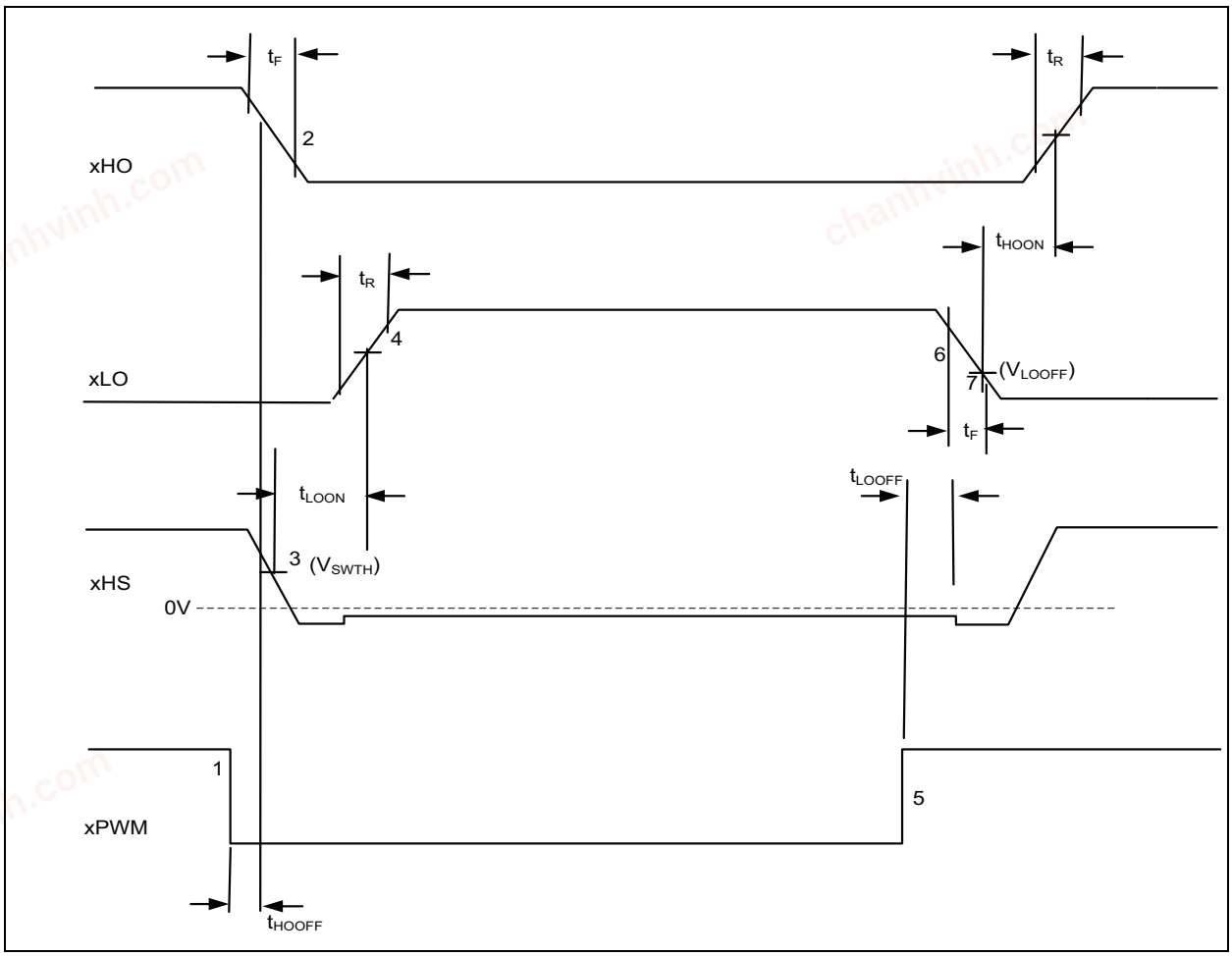


FIGURE 4-3: *PWM Mode (MIC4607A-2).*

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4.4 Overcurrent Timing Diagram

The motor current is sensed in an external resistor that is connected between the low-side MOSFET's source pins and ground. If the sense resistor voltage exceeds the rising overcurrent threshold (typically 0.2V), all LO and HO outputs are latched off and the FLT/ pin is pulled low. Once the outputs are latched off, an internal current source (typically 0.44 µA) begins to charge up the external C_{DLY} capacitor. The outputs remain latched off and all xLI/xHI (or xPWM) input signals are ignored until the voltage on the C_{DLY} capacitor rises above the V_{DLY+} threshold (typically 1.5V), which resets the latch on the first rising edge of any LI input of the MIC4607A-1 (or falling edge on any PWM input for the MIC4607A-2).

Once this occurs, the C_{DLY} capacitor is discharged, the FLT/ pin returns to a high impedance state and all outputs will respond to their respective input signals.

On startup, the current limit latch is reset during a rising V_{DD} or a rising EN pin voltage to assure normal operation.

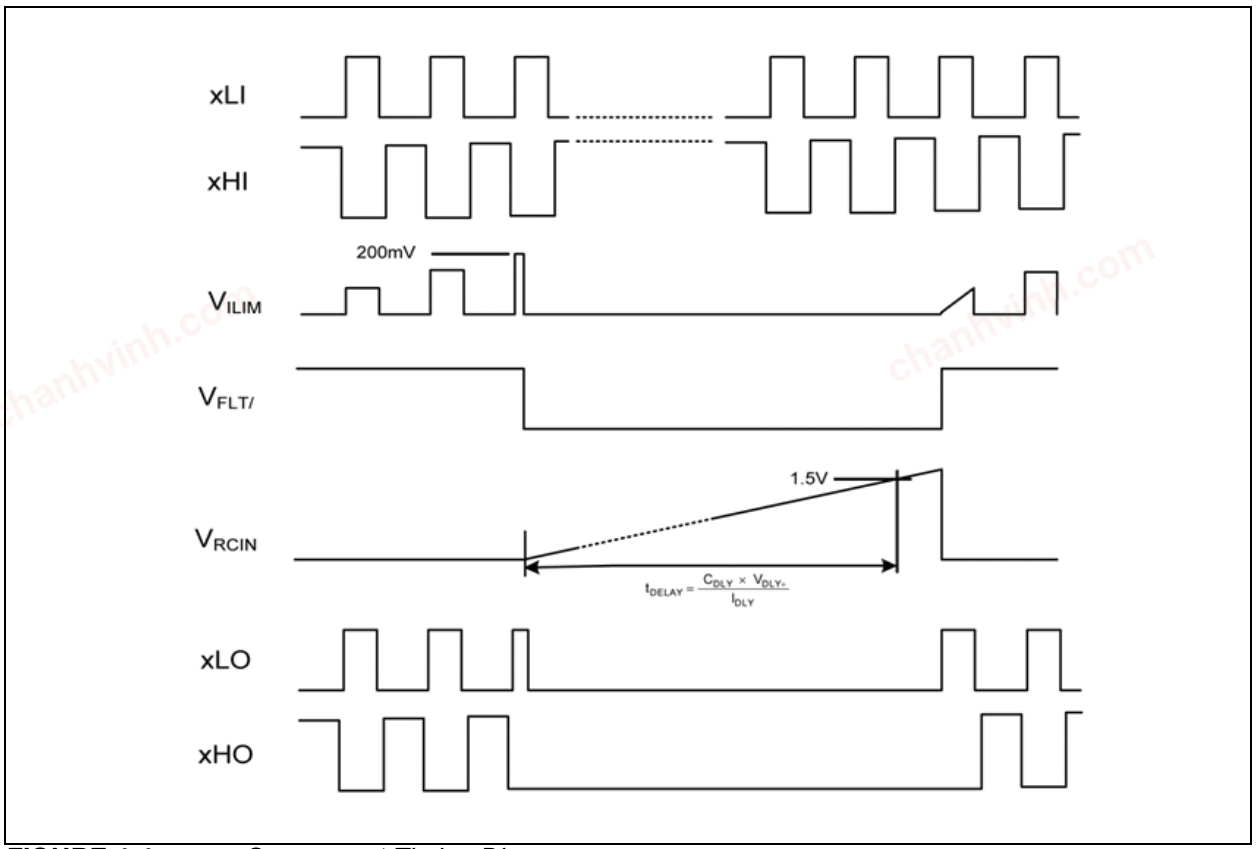


FIGURE 4-4: *Overcurrent Timing Diagram.*

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5.0 FUNCTIONAL DESCRIPTION

The MIC4607A is a non-inverting, 85V three-phase MOSFET driver designed to independently drive all six N-Channel MOSFETs in a three-phase bridge. The MIC4607A offers a wide 5.5V to 16V V_{DD} operating supply range with either six independent TTL inputs (MIC4607A-1) or three PWM inputs, one for each phase (MIC4607A-2). For more information, refer to the Functional Diagram section.

The drivers contain input buffers with hysteresis, four independent UVLO circuits (three high-side and one low-side), and six output drivers. The high-side output drivers utilize a high-speed level-shifting circuit that is referenced to its HS pin. Each phase has an internal diode that is used by the bootstrap circuits to provide the drive voltages for each of the three high-side outputs. A programmable overcurrent protection circuit turns off all outputs during an overcurrent fault.

5.1 Startup and UVLO

The UVLO circuits force the driver's outputs low until the supply voltage exceeds the UVLO threshold. The low-side UVLO circuit monitors the voltage between the V_{DD} and V_{SS} pins. The high-side UVLO circuits monitor the voltage between the xHB and xHS pins. Hysteresis in the UVLO circuits prevent system noise and finite circuit impedance from causing chatter during turn-on.

5.2 Enable Inputs

There is one external enable pin that controls all three phases. A logic high on the enable pin (EN) allows for startup of all phases and normal operation. Conversely, when a logic low is applied on the enable pin, all phases turn-off and the device enters a low current shutdown mode. All outputs (xHO and xLO) are pulled low when EN is low. Do not leave the EN pin floating.

5.3 Input Stage

All input pins (xLI and xHI) are referenced to the V_{SS} pin. The MIC4607A has a TTL-compatible input range and can be used with input signals with amplitude less than the supply voltage. The threshold level is independent of the V_{DD} supply voltage and there is no dependence between I_{VDD} and the input signal amplitude. This feature makes the MIC4607A an excellent level translator that will drive high level gate threshold MOSFETs from a low-voltage PWM IC.

5.4 Low-Side Driver

The low-side driver is designed to drive a ground (V_{SS} pin) referenced N-channel MOSFET. Low driver impedances allow the external MOSFET to be turned on and off quickly. The rail-to-rail drive capability of the output ensures a low $R_{DS(ON)}$ from the external power device (refer to Figure 5-1).

A high level applied to the xLI pin causes V_{DD} to be applied to the gate of the external MOSFET. A low level on the xLI pin grounds the gate of the external MOSFET.

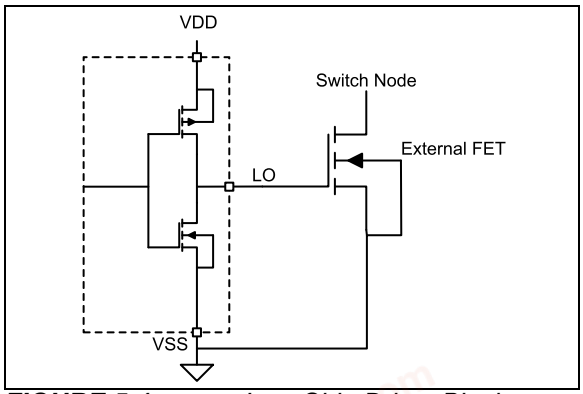


FIGURE 5-1: *Low-Side Driver Block Diagram.*

5.5 High-Side Driver and Bootstrap Circuit

Figure 5-2 illustrates a block diagram of the high-side driver and bootstrap circuit. This driver is designed to drive a floating N-channel MOSFET, whose source terminal is referenced to the HS pin.

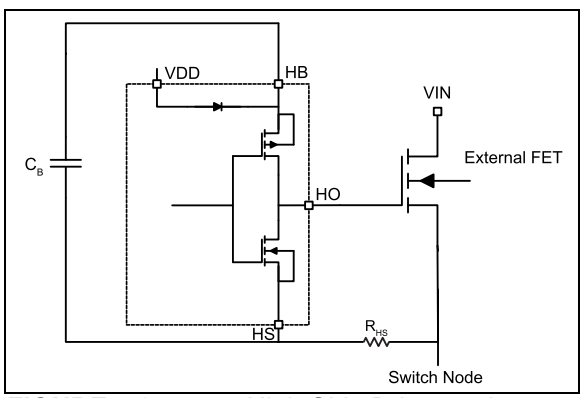


FIGURE 5-2: *High-Side Driver and Bootstrap-Circuit Block Diagram.*

A low-power, high-speed, level-shifting circuit isolates the low side (V_{SS} pin) referenced circuitry from the high-side (xHS pin) referenced driver. Power to the high-side driver and UVLO circuit is supplied by the bootstrap capacitor (C_B) while the voltage level of the xHS pin is shifted high.

The bootstrap circuit consists of an internal diode and external capacitor, C_B. In a typical application, such as the motor driver shown in Figure 5-3 (only Phase A illustrated), the AHS pin is at ground potential while the low-side MOSFET is on. The internal diode charges

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capacitor C_B to $V_{DD} – V_F$ during this time (where V_F is the forward voltage drop of the internal diode). After the low-side MOSFET is turned off and the AHO pin turns on, the voltage across capacitor C_B is applied to the gate of the high-side external MOSFET. As the high-side MOSFET turns on, voltage on the AHS pin rises with the source of the high-side MOSFET until it reaches V_{IN}. As the AHS and AHB pins rise, the internal diode is reverse biased, preventing capacitor C_B from discharging. During this time, the high-side MOSFET is kept ON by the voltage across capacitor C_B.

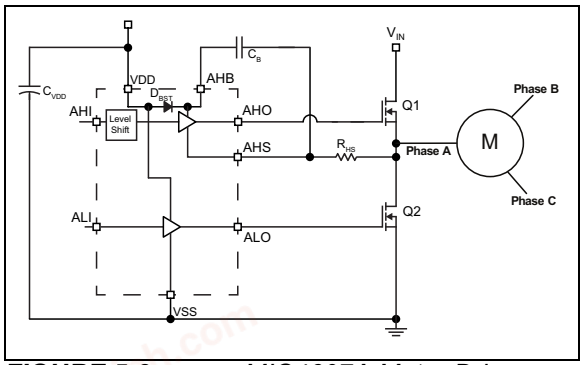


FIGURE 5-3: *MIC4607A Motor Driver Example.*

5.6 Programmable Gate Drive

The MIC4607A offers programmable gate drive, meaning the MOSFET gate drive (gate-to-source voltage) equals the V_{DD} voltage. This feature offers designers flexibility in selecting the proper MOSFETs for a given application. Different MOSFETs require different V_{GS} characteristics for optimum $R_{DS(ON)}$ performance. Typically, the higher the gate voltage (up to 16V), the lower the $R_{DS(ON)}$ achieved. For example, as shown in Figure 5-4, a NTMSF4899NF MOSFET can be driven to the ON state with a gate voltage of 5.5V but $R_{DS(ON)}$ is 5.2 mΩ. If driven to 10V, $R_{DS(ON)}$ is 4.1 mΩ — a decrease of 20%.

In low-current applications, the losses due to $R_{DS(ON)}$ are minimal, but in high-current motor drive applications such as power tools, the difference in $R_{DS(ON)}$ can lower the efficiency, reducing run time.

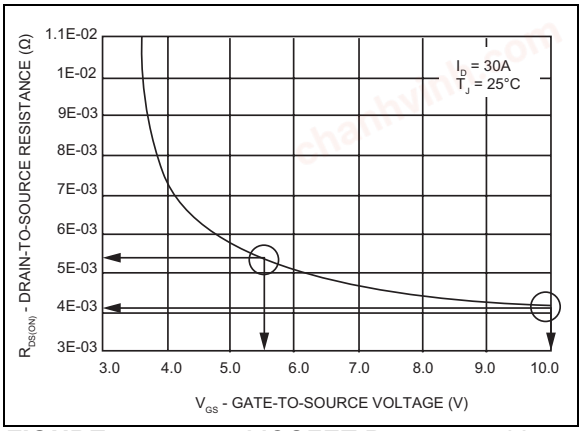


FIGURE 5-4: *MOSFET $R_{DS(ON)}$ vs. V_{GS}.*

5.7 Overcurrent Protection Circuitry

The MIC4607A provides overcurrent protection for the motor driver circuitry. It consists of:

- A comparator that senses the voltage across a current-sense resistor.
- A pulse filter that prevents false triggering of the OC circuit due to noise and other non short-circuit and overcurrent events.
- A latch and timer that keep all gate drivers off during a fault.
- An open-drain pin that pulls low during the fault.

If an overcurrent condition that is greater than the filter time is detected, the FLT/ pin is pulled low and the gate drive outputs are latched off for a time that is determined by the DLY pin circuitry. After the delay circuitry times out, a high-going edge on any of the LI pins (for the MIC4607A-1 version) or a low-going edge on any of the PWM pins (for the MIC4607A-2 version) is required to reset the latch, de-assert the FLT/ pin and allow the gate drive outputs to switch.

For additional information, refer to the Timing Diagrams section as well as the Functional Diagram section.

5.7.1 ILIM

The ILIM+ and ILIM- pins provide a Kelvin-sensed circuit that monitors the voltage across an external current sense resistor. This resistor is typically connected between the source pins of all three low-side MOSFETs and power ground. If the peak voltage across this resistor exceeds the V_{ILIM+} threshold, it will cause the comparator output to go high. If the width of the comparator output pulse exceeds the filter time, it sets the latch and turns off all six outputs.

Both the ILIM+ and ILIM– pins must be shorted to V_{SS} ground if the overcurrent features is not used.

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5.7.2 DLY

A capacitor connected to the DLY pin determines the amount of time the gate drive outputs are latched off before they can be restarted.

During normal operation, the DLY pin is held low by an internal MOSFET. After an overcurrent condition is detected, the MOSFET turns off and the external capacitor is charged up by an internal current source. The outputs remain latched off until the DLY pin voltage reaches the V_{DLY+} threshold (typically 1.5V).

The delay time can be approximately calculated using Equation 5-1.

EQUATION 5-1:

$$t_{DLY} = \frac{C_{DLY} \times V_{DLY-}}{I_{DLY}}$$

5.7.3 FLT/

This open-drain output is pulled low while the gate drive outputs are latched off after an over-current condition. It will de-assert once the DLY pin has reached the V_{DLY+} threshold and a rising edge occurs on any LI pin (for the MIC4607A-1) or a falling edge on any PWM pin (MIC4607A-2).

During normal operation, the internal pull-down MOSFET is of the pin is high impedance. A pull-up resistor must be connected to this pin.

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6.0 APPLICATION INFORMATION

6.1 Adaptive Dead-Time

For each phase, it is important that both MOSFETs of the same phase branch are not conducting at the same time or V_{IN} will be shorted to ground and current will "shoot through" the MOSFETs. Excessive shoot-through causes higher power dissipation in the MOSFETs, voltage spikes and ringing. The high switching current and voltage ringing generate conducted and radiated EMI.

Minimizing shoot-through can be done passively, actively or through a combination of both. Passive shoot-through protection can be achieved by implementing delays between the high and low gate drivers to prevent both MOSFETs from being on at the same time. These delays can be adjusted for different applications. Although simple, the disadvantage of this approach is that it requires long delays to account for process and temperature variations in the MOSFET and MOSFET driver.

Adaptive Dead-Time monitors voltages on the gate drive outputs and switch node to determine when to switch the MOSFETs on and off. This active approach adjusts the delays to account for some of the variations, but it too has its disadvantages. High currents and fast switching voltages in the gate drive and return paths can cause parasitic ringing to turn the MOSFETs back on even while the gate driver output is low. Another disadvantage is that the driver cannot monitor the gate voltage inside the MOSFET. Figure 6-1 shows an equivalent circuit of the high-side gate drive.

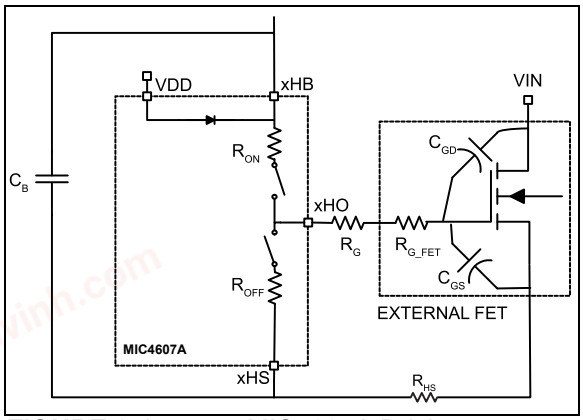


FIGURE 6-1: *MIC4607A Driving an External MOSFET.*

The internal gate resistance (R_{G_FET}) and any external damping resistor (R_G) and HS pin resistor (R_{HS}), isolate the MOSFET's gate from the driver output. There is a delay between when the driver output goes low and the MOSFET turns off. This turn-off delay is usually specified in the MOSFET data sheet. This delay increases when an external damping resistor is used.

The MIC4607A uses a combination of active sensing and passive delay to ensure that both MOSFETs are not on at the same time. Figure 6-2 illustrates how the adaptive dead-time circuitry works.

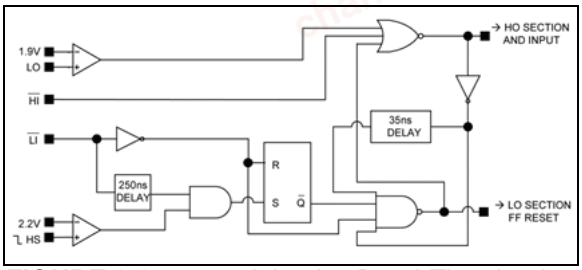


FIGURE 6-2: *Adaptive Dead-Time Logic Diagram.*

A transition of $\overline{HI}$ to low and $\overline{LI}$ to high is caused by a high level on the xPWM pin for the MIC4607A-2. This causes the xLO pin to go low. The MIC4607A monitors the xLO pin voltage and prevents the xHO pin from turning on until the voltage on the xLO pin reaches the V_{LOOFF} threshold. After a short delay, the MIC4607A drives the xHO pin high. Monitoring the xLO voltage eliminates any excessive delay due to the MOSFET driver's turn-off time and the short delay accounts for the MOSFET turn-off delay as well as letting the xLO pin voltage settle out. If an external resistor is used between the xLO output and the MOSFET gate, it must be made small enough to prevent excessive voltage drop across the resistor during turn-off. Figure 6-3 illustrates using a diode (D_{LS}) and resistor (R_{LS2}) in parallel with the gate resistor to prevent a large voltage drop between the xLO pin and MOSFET gate voltages during turn-off.

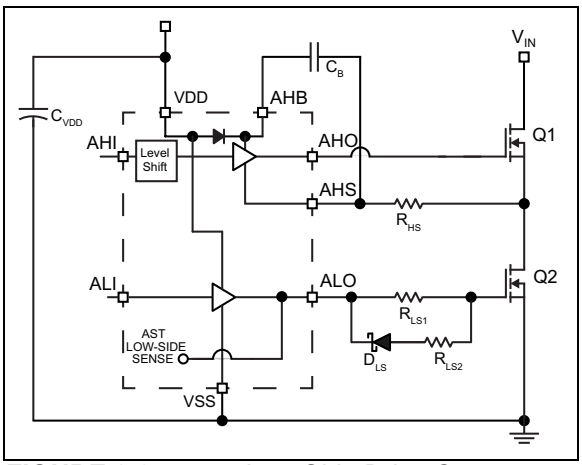


FIGURE 6-3: *Low-Side Drive Gate Resistor Configuration.*

A low on the xPWM pin causes $\overline{HI}$ to go high and $\overline{LO}$ to go low. This causes the xHO pin to go low after a short delay (t_{HOOFF}). Before the xLO pin can go high, the voltage on the switching node (xHS pin) must have dropped to 2.2V. Monitoring the switch voltage instead of the xHO pin voltage eliminates timing variations and

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excessive delays due to the high-side MOSFET turn-off. The xLO driver turns on after a short delay (t_{LOON}). Once the xLO driver is turned on, it is latched on until the xPWM signal goes high. This prevents any ringing or oscillations on the switch node or xHS pin from turning off the xLO driver. If the xPWM pin goes low and the voltage on the xHS pin does not cross the V_{SWTH} threshold, the xLO pin will be forced high after a short delay (t_{SWTO}), ensuring proper operation.

The internal logic circuits also ensure a "first on" priority at the inputs. If the xHO output is high, the xLI pin is inhibited. A high signal or noise glitch on the xLI pin has no effect on the xHO or xLO outputs until the xHI pin goes low. Similarly, xLO being high holds xHO low until xLI and xLO are low.

Fast propagation delay between the input and output drive waveform is desirable. It improves overcurrent protection by decreasing the response time between the control signal and the MOSFET gate drive. Minimizing propagation delay also minimizes phase shift errors in power supplies with wide bandwidth control loops.

Care must be taken to ensure that the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width can result in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high-side on-time to switching period) is determined by the time required for the C_B capacitor to charge during the off-time. Adequate time must be allowed for the C_B capacitor to charge up before the high-side driver is turned back on.

Although the adaptive dead-time circuit in the MIC4607A prevents the driver from turning both MOSFETs on at the same time, other factors outside of the anti-shoot-through circuit's control can cause shoot-through. Other factors include ringing on the gate drive node and capacitive coupling of the switching node voltage on the gate of the low-side MOSFET.

The scope photo in Figure 6-4 shows the dead time (<20 ns) between the high- and low-side MOSFET transitions as the low-side driver switches off while the high-side driver transitions from off to on.

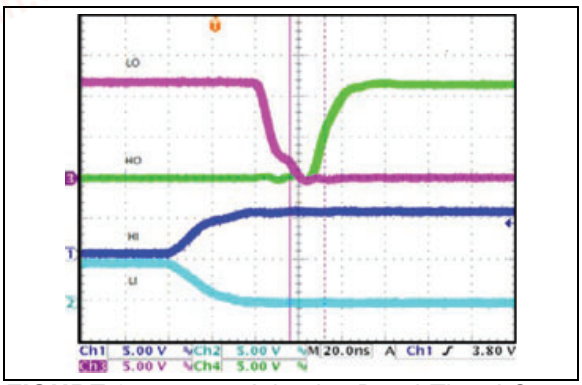


FIGURE 6-4: *Adaptive Dead-Time LO (LOW) to HO (HIGH).*

Table 6-1 contains truth tables for the MIC4607A-1 (independent TTL inputs) and Table 6-2 is for the MIC4607A-2 (PWM inputs) that details the "first on" priority as well as the failsafe delay (t_{SWTO}).

TABLE 6-1: MIC4607A-1 TRUTH TABLE

xLI	xHI	xLO	xHO	Comments
0	0	0	0	Both outputs off.
0	1	0	1	xHO will not go HIGH until xLO falls below 1.9V.
1	0	1	0	xLO will be delayed an extra 250 ns if xHS never falls below 2.2V.
1	1	X	X	First ON stays on until input of same goes LOW.

TABLE 6-2: MIC4607A-2 TRUTH TABLE

xPWM	xLO	xHO	Comments
0	1	0	xLO will be delayed an extra 250 ns if xHS never falls below 2.2V.
1	0	1	xHO will not go HIGH until xLO falls below 1.9V.

6.2 HS Pin Clamp

A resistor/diode clamp between the switching node and the HS pin is necessary to clamp large negative glitches or pulses on the HS pin.

Figure 6-5 shows the Phase A section high-side and low-side MOSFETs connected to one phase of the three phase motor. There is a brief period of time (dead time) between switching to prevent both MOSFETs from being on at the same time. When the high-side MOSFET is conducting during the on-time state, current flows into the motor. After the high-side MOSFET turns off, but before the low-side MOSFET turns on, current from the motor flows through the body diode in parallel with the low-side MOSFET. Depending upon the turn-on time of the body diode, the motor current, and circuit parasitics, the initial negative voltage on the switch node can be several volts or more. The forward voltage drop of the body diode can be several volts, depending on the body diode characteristics and motor current.

Even though the HS pin is rated for negative voltage, it is good practice to clamp the negative voltage on the HS pin with a resistor and a diode to prevent excessive negative voltage from damaging the driver. Depending upon the application and amount of negative voltage on the switch node, a 3Ω resistor is recommended. If the HS pin voltage exceeds 0.7V, a diode between the xHS pin and ground is recommended. The diode reverse

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voltage rating must be greater than the high-voltage input supply (V_{IN}). Larger values of resistance can be used if necessary.

Adding a series resistor in the switch node limits the peak high-side driver current during turn-off, which affects the switching speed of the high-side driver. The resistor in series with the HO pin may be reduced to help compensate for the extra HS pin resistance.

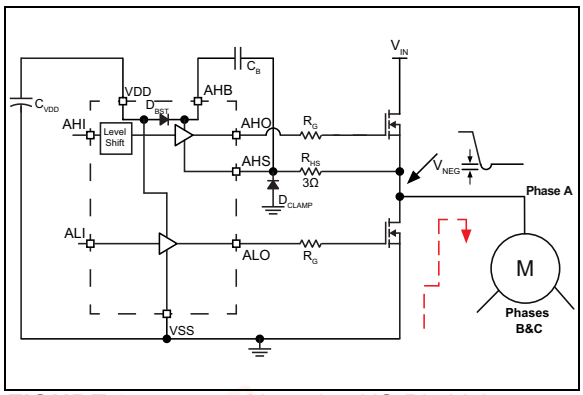


FIGURE 6-5: *Negative HS Pin Voltage.*

6.3 Power Dissipation Considerations

Power dissipation in the driver can be separated into three areas:

- Internal diode dissipation in the bootstrap circuit
- Internal driver dissipation
- Quiescent current dissipation used to supply the internal logic and control functions.

6.4 Bootstrap Circuit Power Dissipation

Power dissipation of the internal bootstrap diode primarily comes from the average charging current of the bootstrap capacitor (C_B) multiplied by the forward voltage drop of the diode. Secondary sources of diode power dissipation are the reverse leakage current and reverse recovery effects of the diode.

The average current drawn by repeated charging of the high-side MOSFET is calculated by Equation 6-1.

EQUATION 6-1:

$$I_{F(AVE)} = Q_{GATE} \times f_S$$

Where:

Q_{GATE} = Total gate charge at $V_{HB} - V_{HS}$.
f_S = Gate drive switching frequency.

The average power dissipated by the forward voltage drop of the diode equals:

EQUATION 6-2:

$$Pdiode_{FWD} = I_{F(AVE)} \times V_F$$

Where:

V_F = Diode forward voltage drop.

There are three phases in the MIC4607A. The power dissipation for each of the bootstrap diodes must be calculated and summed to obtain the total bootstrap diode power dissipation for the package.

The value of V_F should be taken at the peak current through the diode; however, this current is difficult to calculate because of differences in source impedances. The peak current can either be measured or the value of V_F at the average current can be used, which will yield a good approximation of diode power dissipation.

The reverse leakage current of the internal bootstrap diode is typically 3 µA at a reverse voltage of 85V at 125°C. Power dissipation due to reverse leakage is typically much less than 1 mW and can be ignored.

An optional external bootstrap diode may be used instead of the internal diode (Figure 6-6). An external diode may be useful if high gate charge MOSFETs are being driven and the power dissipation of the internal diode is contributing to excessive die temperatures. The voltage drop of the external diode must be less than the internal diode for this option to work. The reverse voltage across the diode will be equal to the input voltage minus the V_{DD} supply voltage. The above equations can be used to calculate power dissipation in the external diode; however, if the external diode has significant reverse leakage current, the power dissipated in that diode due to reverse leakage can be calculated with the formula in Equation 6-3:

EQUATION 6-3:

$$Pdiode_{REV} = I_R \times V_{REV} \times (1 - D)$$

Where:

I_R = Reverse current flow at V_{REV} and T_J.
V_{REV} = Diode reverse voltage.
D = Duty cycle ($t_{ON} \times f_S$).

The on-time is the time the high-side switch is conducting. In most topologies, the diode is reverse biased during the switching cycle off-time.

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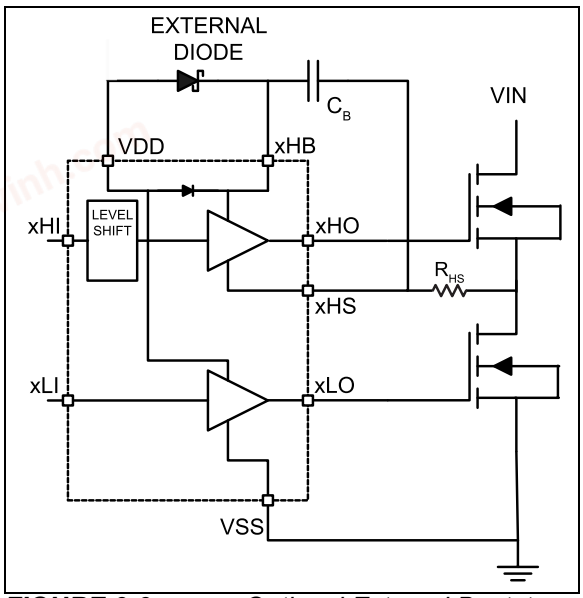


FIGURE 6-6: *Optional External Bootstrap Diode.*

6.5 Gate Driver Power Dissipation

Power dissipation in the output driver stage is mainly caused by charging and discharging the gate to source and gate to drain capacitance of the external MOSFET. Figure 6-7 shows a simplified equivalent circuit of the MIC4607A driving an external high-side MOSFET.

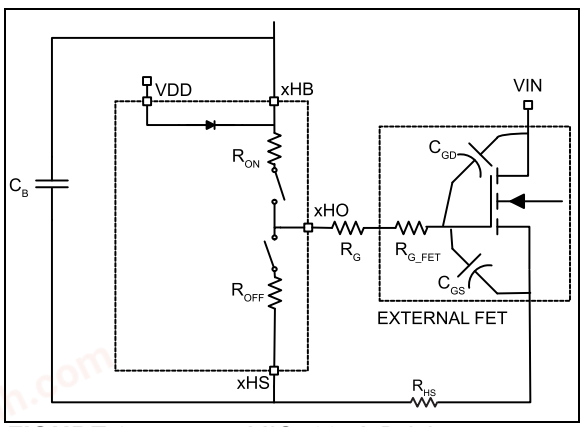


FIGURE 6-7: *MIC4607A Driving an External High-Side MOSFET.*

6.5.1 DISSIPATION DURING THE EXTERNAL MOSFET TURN-ON

Energy from capacitor C_B is used to charge up the input capacitance of the MOSFET (C_{GD} and C_{GS}). The energy delivered to the MOSFET is dissipated in the three resistive components, R_{ON}, R_G and R_{G_FET}. R_{ON} is the on resistance of the upper driver MOSFET in the MIC4607A. R_G is the series resistor (if any) between the driver and the MOSFET. R_{G_FET} is the gate resistance of the MOSFET and is typically listed in the power MOSFET's specifications. The ESR of capacitor C_B and the resistance of the connecting etch can be ignored since they are much less than R_{ON} and R_{G_FET}.

The effective capacitances of C_{GD} and C_{GS} are difficult to calculate because they vary non-linearly with I_D, V_{GS}, and V_{DS}. Fortunately, most power MOSFET specifications include a typical graph of total gate charge versus V_{GS}. Figure 6-8 shows a typical gate charge curve for an arbitrary power MOSFET. This chart shows that for a gate voltage of 10V, the MOSFET requires about 23.5 nC of charge. The energy dissipated by the resistive components of the gate drive circuit during turn-on is calculated as:

EQUATION 6-4:

$$E = \frac{1}{2} \times C_{ISS} \times V_{GS}^{2}$$

Where:

C_{ISS} = Total gate capacitance of the MOSFET.

but

EQUATION 6-5:

$$Q = C \times V$$

so,

EQUATION 6-6:

$$E = \frac{1}{2} \times Q_G \times V_{GS}$$

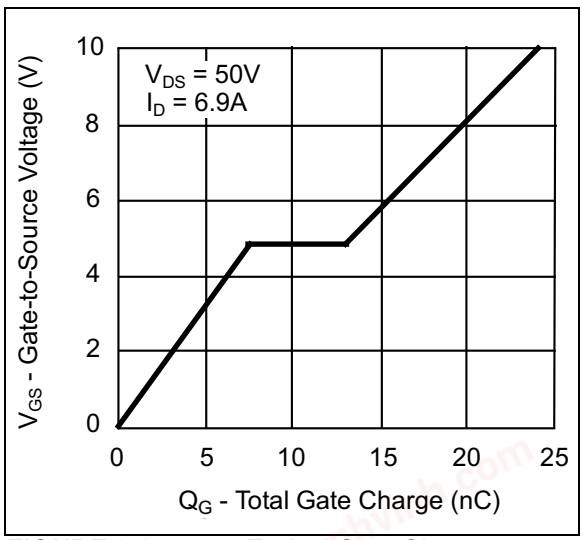


FIGURE 6-8: *Typical Gate Charge vs. V_{GS}.*

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The same energy is dissipated by R_{OFF}, R_G, and R_{G_FET} when the driver IC turns the MOSFET off. Assuming R_{ON} is approximately equal to R_{OFF}, the total energy and power dissipated by the resistive drive elements is:

EQUATION 6-7:

$$E_{DRIVER} = Q_G \times V_{GS}$$

Where:

E_{DRIVER} = Energy dissipated per switching cycle

and

EQUATION 6-8:

$$P_{DRIVER} = Q_G \times V_{GS} \times f_S$$

Where:

P_{DRIVER} =	Power dissipated per switching cycle
Q_G =	Total gate charge at V_{GS}
V_{GS} =	Gate-to-source voltage on MOSFET
f_S =	Switching freq. of the gate drive circuit

6.6 Supply Current Power Dissipation

Power is dissipated in the input and control sections of the MIC4607A, even if there is no external load. Current is still drawn from the V_{DD} and HB pins for the internal circuitry, the level shifting circuitry, and shoot-through current in the output drivers. The V_{DD} and V_{HB} currents are proportional to operating frequency and the V_{DD} and V_{HB} voltages. The Typical Performance Curves show how supply current varies with switching frequency and supply voltage.

The power dissipated by the MIC4607A due to supply current is:

EQUATION 6-9:

$$Pdiss_{SUPPLY} = V_{DD} \times I_{DD} + V_{HB} \times I_{HB}$$

Values for I_{DD} and I_{HB} are found in the EC table and the typical characteristics graphs.

6.7 Total Power Dissipation and Thermal Considerations

Total power dissipation in the MIC4607A is equal to the power dissipation caused by driving the external MOSFETs, the supply currents and the internal bootstrap diodes.

EQUATION 6-10:

$$Pdiss_{TOTAL} = Pdiss_{SUPPLY} + Pdiss_{DRIVE} + P_{DIODE}$$

The power dissipated in the driver equals the ratio of R_{ON} and R_{OFF} to the external resistive losses in R_G and R_{G_FET}. Letting $R_{ON} = R_{OFF}$, the power dissipated in the driver due to driving the external MOSFET is:

EQUATION 6-11:

$$Pdiss_{DRIVER} = P_{DRIVER} \times \frac{R_{ON}}{R_{ON} + R_G + R_{G_FET}}$$

There are six MOSFETs driven by the MIC4607A. The power dissipation for each of the drivers must be calculated and summed to obtain the total driver diode power dissipation for the package.

In some cases, the high-side FET of one phase may be pulsed at a frequency, f_S, while the low-side FET of the other phase is kept continuously on. Since the MOSFET gate is capacitive, there is no driver power if the FET is not switched. The operation of all driver outputs must be considered to accurately calculate power dissipation.

The die temperature can be calculated after the total power dissipation is known.

EQUATION 6-12:

$$T_J = T_A + Pdiss_{TOTAL} \times \theta_{JA}$$

Where:

T_A =	Maximum ambient temperature
T_J =	Junction temperature
$P_{dissTOTAL}$ =	Total power dissipation of MIC4607A
θ_{JA} =	Thermal resistance from junction to ambient air

6.8 Other Timing Considerations

Make sure the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width may result in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high-side on-time to switching period) is controlled by the minimum pulse width of the low side and by the time required for the C_B capacitor to charge during the off-time. Adequate time must be allowed for the C_B capacitor to charge up before the high-side driver is turned on.

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6.9 Decoupling and Bootstrap Capacitor Selection

Decoupling capacitors are required for both the low-side (V_{DD}) and high-side (xHB) supply pins. These capacitors supply the charge necessary to drive the external MOSFETs and also minimize the voltage ripple on these pins. The capacitor from xHB to xHS has two functions: it provides decoupling for the high-side circuitry and also provides current to the high-side circuit while the high-side external MOSFET is on. Ceramic capacitors are recommended because of their low impedance and small size. Z5U type ceramic capacitor dielectrics are not recommended because of the large change in capacitance over temperature and voltage. A minimum value of 0.1 µF is required for C_B (xHB to xHS capacitors) and 1 µF for the V_{DD} capacitor, regardless of the MOSFETs being driven. Larger MOSFETs may require larger capacitance values for proper operation. The voltage rating of the capacitors depends on the supply voltage, ambient temperature and the voltage derating used for reliability. 25V rated X5R or X7R ceramic capacitors are recommended for most applications. The minimum capacitance value should be increased if low voltage capacitors are used because even good quality dielectric capacitors, such as X5R, will lose 40% to 70% of their capacitance value at the rated voltage.

Placement of the decoupling capacitors is critical. The bypass capacitor for V_{DD} should be placed as close as possible between the V_{DD} and V_{SS} pins. The bypass capacitor (C_B) for the xHB supply pin must be located as close as possible between the xHB and xHS pins. The etch connections must be short, wide, and direct. The use of a ground plane to minimize connection impedance is recommended. Refer to the "Grounding, Component Placement and Circuit Layout" sub-section for more information.

The voltage on the bootstrap capacitor drops each time it delivers charge to turn on the MOSFET. The voltage drop depends on the gate charge required by the MOSFET. Most MOSFET specifications specify gate charge versus V_{GS} voltage. Based on this information and a recommended ΔV_{HB} of less than 0.1V, the minimum value of bootstrap capacitance is calculated as:

EQUATION 6-13:

$$C_B \geq \frac{Q_{GATE}}{\Delta V_{HB}}$$

Where:

Q_{GATE} = Total gate charge at V_{HB}.
ΔV_{HB} = Voltage drop at the HB pin.

If the high-side MOSFET is not switched but held in an on state, the voltage in the bootstrap capacitor will drop due to leakage current that flows from the HB pin to ground. This current is specified in the Electrical Characteristics table. In this case, the value of C_B is calculated as:

EQUATION 6-14:

$$C_B \geq \frac{I_{HBS} \times t_{ON}}{\Delta V_{HB}}$$

Where:

I_{HBS} = Maximum xHB pin leakage current.
t_{ON} = Maximum high-side FET on-time.

The larger value of C_B from Equation 6-13 or Equation 6-14 should be used.

6.10 Grounding, Component Placement and Circuit Layout

Nanosecond switching speeds and ampere peak currents in and around the MIC4607A driver require proper placement and trace routing of all components. Improper placement may cause degraded noise immunity, false switching, excessive ringing, or circuit latch-up.

Figure 6-9 shows the critical current paths of the high- and low-side driver when their outputs go high and turn on the external MOSFETs. It also helps demonstrate the need for a low impedance ground plane. Charge needed to turn-on the MOSFET gates comes from the decoupling capacitors C_{VDD} and C_B. Current in the low-side gate driver flows from C_{VDD} through the internal driver, into the MOSFET gate, and out the source. The return connection back to the decoupling capacitor is made through the ground plane. Any inductance or resistance in the ground return path causes a voltage spike or ringing to appear on the source of the MOSFET. This voltage works against the gate drive voltage and can either slow down or turn off the MOSFET during the period when it should be turned on.

Current in the high-side driver is sourced from capacitor C_B and flows into the xHB pin and out the xHO pin, into the gate of the high side MOSFET. The return path for the current is from the source of the MOSFET and back to capacitor C_B. The high-side circuit return path usually does not have a low-impedance ground plane so the etch connections in this critical path should be short and wide to minimize parasitic inductance. As with the low-side circuit, impedance between the MOSFET source and the decoupling capacitor causes negative voltage feedback that fights the turn-on of the MOSFET.

It is important to note that capacitor C_B must be placed close to the xHB and xHS pins. This capacitor not only provides all the energy for turn-on but it must also keep xHB pin noise and ripple low for proper operation of the high-side drive circuitry.

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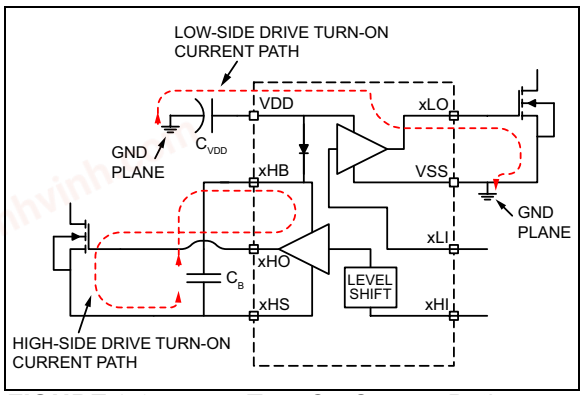


FIGURE 6-9: *Turn-On Current Paths.*

Figure 6-10 shows the critical current paths when the driver outputs go low and turn off the external MOSFETs. Short, low-impedance connections are important during turn-off for the same reasons given in the turn-on explanation. Current flowing through the internal diode replenishes charge in the bootstrap capacitor, C_B.

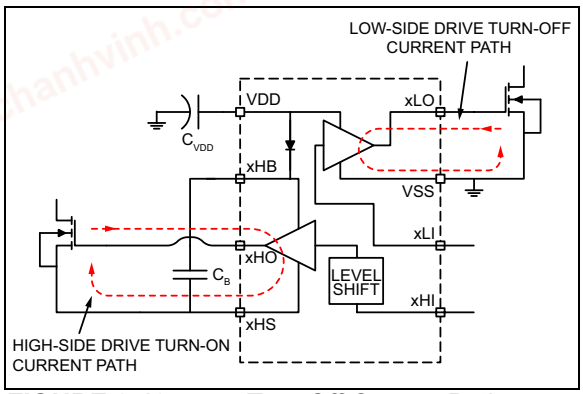


FIGURE 6-10: *Turn-Off Current Paths.*

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7.0 MOTOR APPLICATIONS

Figure 7-1 illustrates an automotive motor application. The 12V battery input voltage can see peaks as high as 60V during a load dump event. The 85V-rated MIC4607A drives six MOSFETs that provide power to the BLDC motor.

A current-sense resistor senses the peak motor current. The voltage across this resistor is monitored by the OC circuit in the MIC4607A, which provides overcurrent protection for the application. The 120V rating of the MIC5281 series of LDOs provide input surge voltage protection, while regulating the battery voltage down to 3.3V and 10V to 12V for the microcontroller and gate driver respectively. This circuit can also be used for power tool applications, where the battery voltage carries high-voltage peaks and surges.

Figure 7-2 is a block diagram for a 24V motor drive application. The regulated 24V bus allows the use of lower input voltage LDOs, such as the MIC5239-3.3 and MIC5234. This circuit configuration can be used in industrial applications.

Figure 7-3 illustrates an off-line motor application. Adding an off-line power supply to the front end allow the MIC4607A to be used in applications such as blenders and other white goods as well as ceiling fan applications. The circuit consists of an MIC38C44 based AC/DC power supply, that is used to generate 24 VDC to power a BLDC motor. The MIC4607A drives the six MOSFETs that provide power to the motor.

The MIC4607A can also be used in low and mid-voltage inverter applications. Figure 7-4 shows how power generated by a spinning (or breaking) motor can be used to generate DC power to a load or provide power for battery-charging applications.

The MIC4607A can sink as much as 1A, which is enough current to overcome the MOSFET's input capacitance and switch the MOSFET up to 50 kHz.

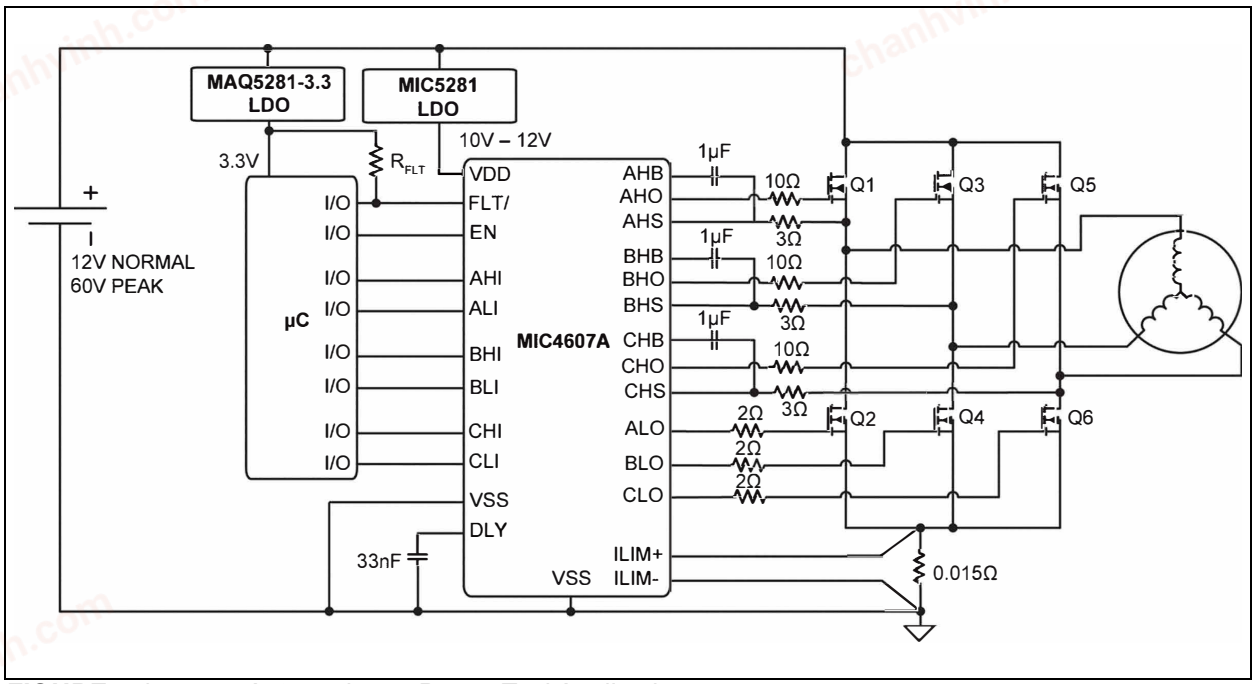


FIGURE 7-1: *Automotive or Power Tool Application.*

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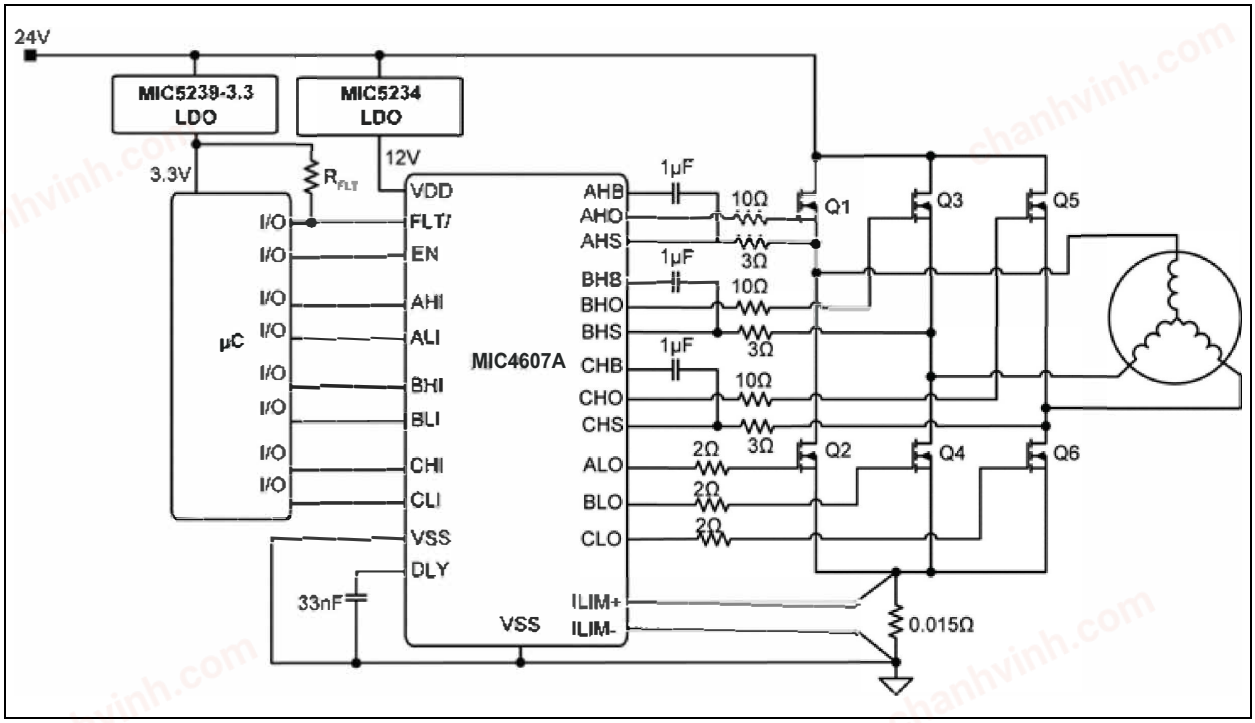


FIGURE 7-2: *Industrial Motor Driver.*

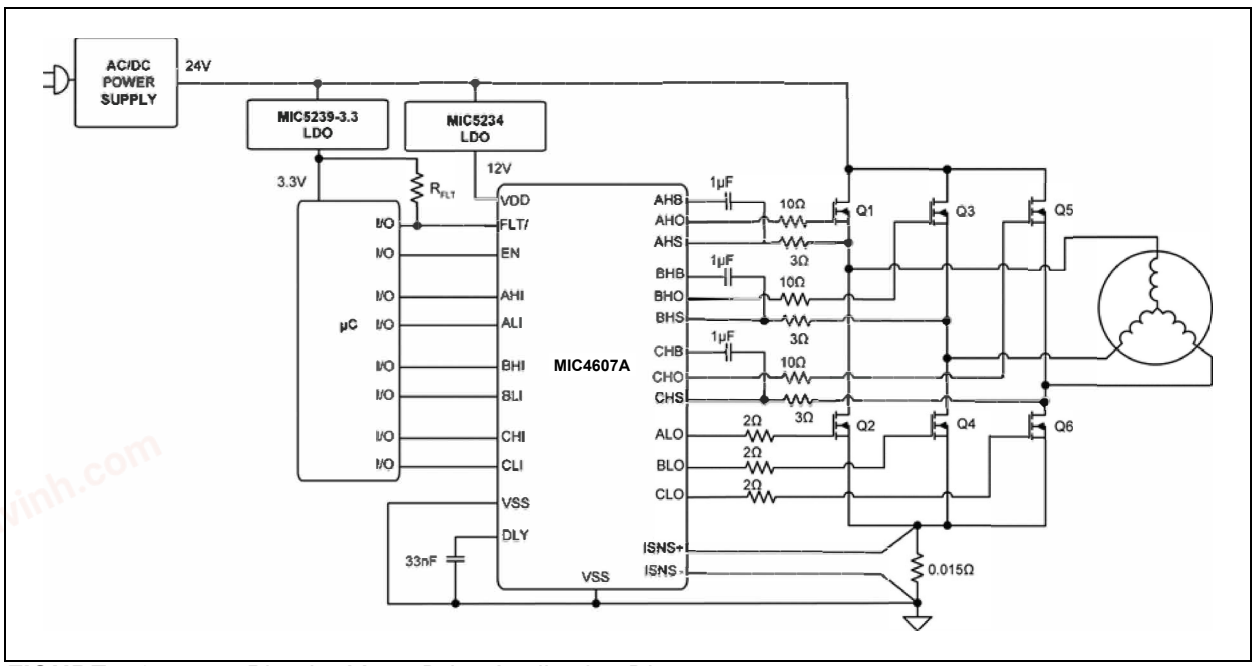


FIGURE 7-3: *Blender Motor Drive Application Diagram.*

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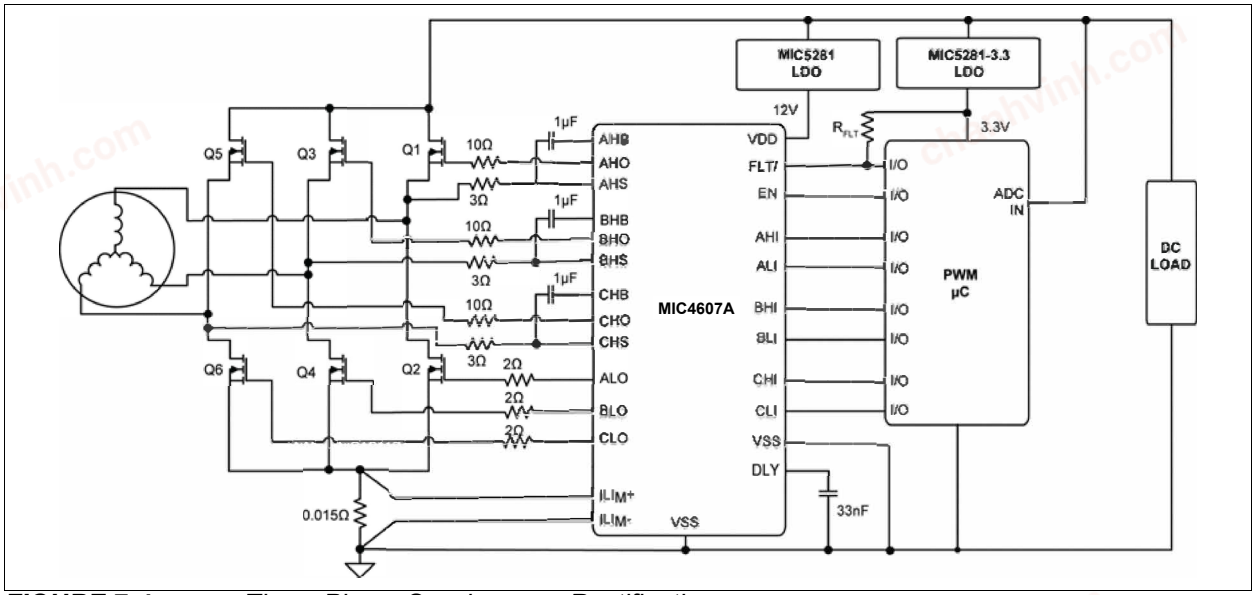


FIGURE 7-4: *Three-Phase Synchronous Rectification.*

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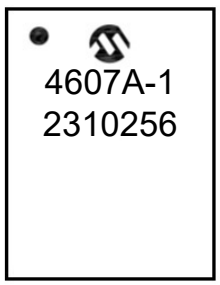
8.0 PACKAGING INFORMATION

8.1 Package Marking Information

28-Lead 4 x 5 mm VQFN*



Example



Note: -X indicates the Input option. 1 for Dual Inputs, 2 for Single PWM Input.

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

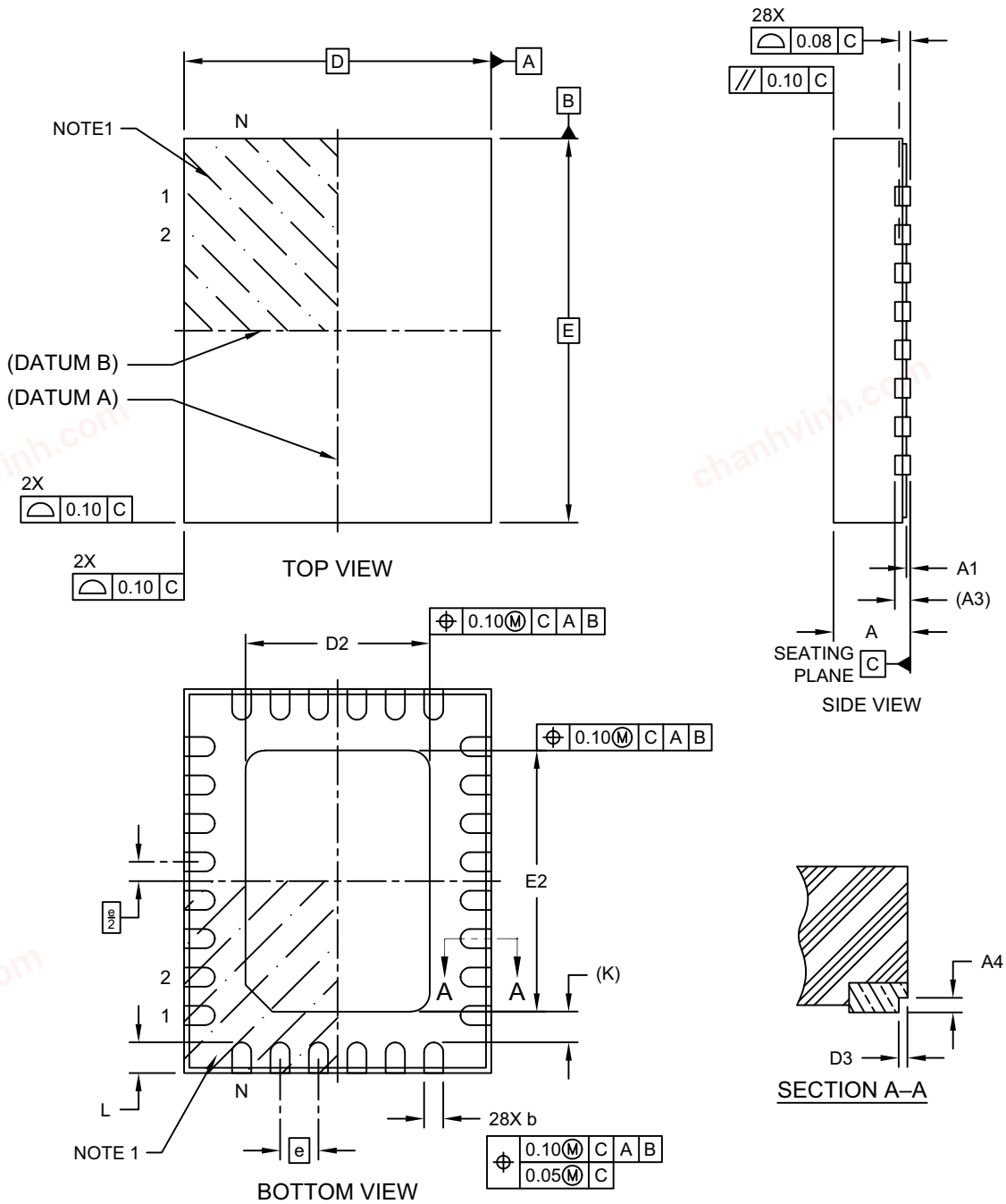
Underbar (_) and/or Overbar (¯) symbol may not be to scale.

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28-Lead Very Thin Plastic Quad Flat, No Lead Package (HPB) - 4x5x1.0 mm Body [VQFN] With 2.4x3.4 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

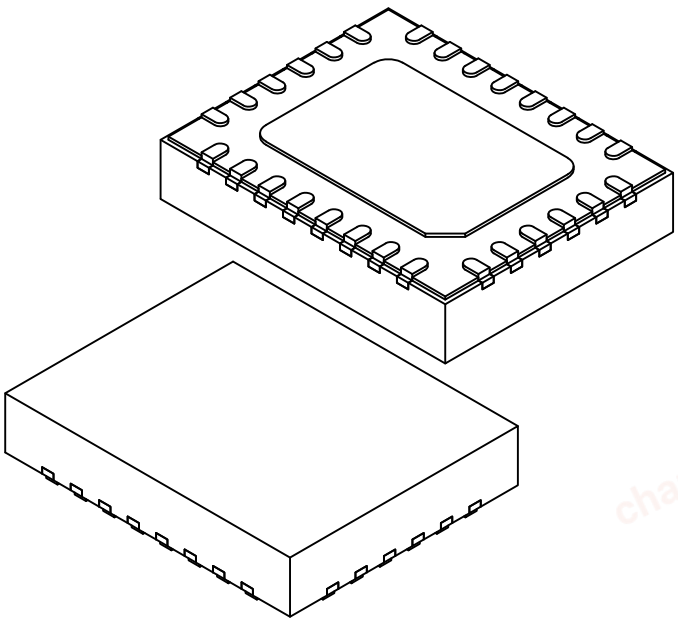


Microchip Technology Drawing C04-21564 Rev B Sheet 1 of 2

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28-Lead Very Thin Plastic Quad Flat, No Lead Package (HPB) - 4x5x1.0 mm Body [VQFN] With 2.4x3.4 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		28	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.30	2.40	2.50
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.30	3.40	3.50
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K		0.40 REF	
Wettable Flank Step Cut Length	D3	0.035	-	0.085
Wettable Flank Step Cut Height	A4	0.10	-	0.19

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

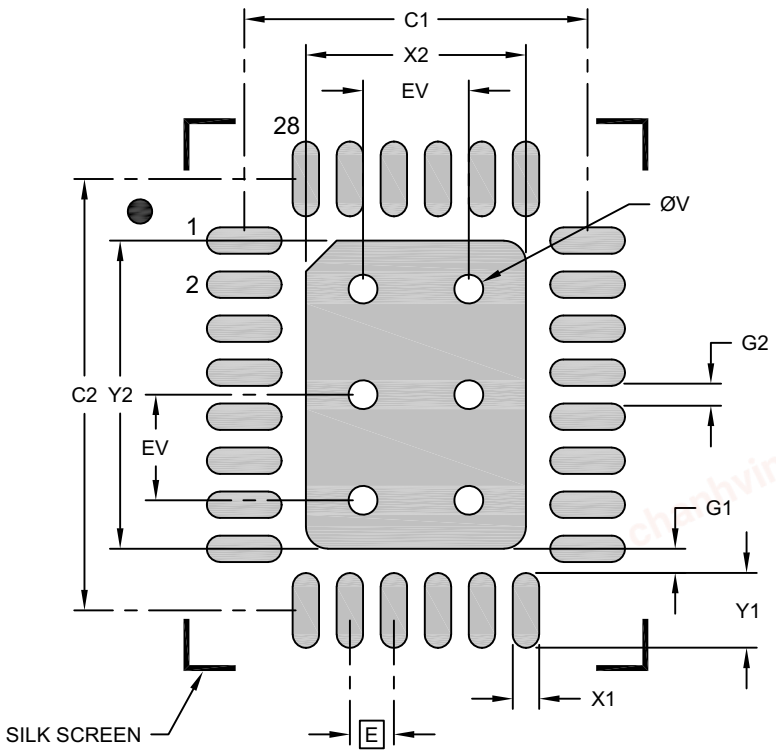
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RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			2.50
Center Pad Length	Y2			3.50
Contact Pad Spacing	C1		3.90	
Contact Pad Spacing	C2		4.90	
Contact Pad Width (X28)	X1			0.30
Contact Pad Length (X28)	Y1			0.85
Contact Pad to Center Pad (X28)	G1	0.28		
Contact Pad to Contact Pad (X24)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23564 Rev B

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APPENDIX A: REVISION HISTORY

Revision A (December 2024)

- Initial release of this document.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X	X	XX	-XX	XXX
Device	Input Option	Junction Temp. Range	Package	Media Type	Qualification

Device:	MIC4607A:	85V, Three-Phase MOSFET Driver with Adaptive Dead-Time, Anti-Shoot-Through and Overcurrent Protection
Input Option:	1 =	Dual Inputs
	2 =	Single PWM Input
Temperature Range:	Y =	-40°C to +125°C (RoHS Compliant)
Package:	ML =	28-lead VQFN
Media Type:	TR =	5000/Reel
Qualification:	<blank>=	Standard part
	VAO =	Automotive AEC-Q100 Qualified

Examples:

a) MIC4607A-1YML-TR: 85V, Three-Phase MOSFET Driver with Adaptive Dead-Time, Anti-Shoot-Through and Overcurrent Protection, Dual Inputs, -40°C to +125°C Temp. Range, 28-Pin VQFN, 5000/Reel.

b) MIC4607A-2YML-TR: 85V, Three-Phase MOSFET Driver with Adaptive Dead-Time, Anti-Shoot-Through and Overcurrent Protection, Single PWM Input, -40°C to +125°C Temp. Range, 28-Pin VQFN, 5000/Reel.

c) MIC4607A-2YML-TRVAO: 85V, Three-Phase MOSFET Driver with Adaptive Dead-Time, Anti-Shoot-Through and Overcurrent Protection, Single PWM Input, –40°C to +125°C Temp. Range, 28-Pin VQFN, 5000/Reel, Automotive Qualified

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip sales office for package availability for the Tape and Reel option.

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