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MIC4467/8/9

Quad 1.2A Peak Low-Side MOSFET Drivers

Features

- Reliable, Low-Power Bipolar/CMOS/DMOS Construction
- Latch-Up Protected to >500 mA Reverse Current
- Logic Input withstands Swing to –5V
- High 3A Peak Output Current
- Wide 4.5V to 18V Operating Range
- Symmetrical Rise and Fall Times
- Short <40 ns Typical Delay Time
- TTL Logic Input Independent of Supply Voltage
- Low Equivalent 6 pF Input Capacitance
- Low 5Ω Typical Output Impedance
- Output Voltage Swings within 25 mV of Ground or V_S.

Applications

- General-Purpose CMOS Logic Buffer
- Driving All 4 MOSFETs in an H-Bridge
- Direct Small Motor Driver
- Relay or Peripheral Drivers
- Dual Differential Output Power Drivers
- CCD Driver
- Pin Switching Network Driver

General Description

The MIC4467/8/9 family of four output CMOS buffer/drivers is an expansion from the earlier single- and dual-output drivers, to which they are functionally closely related. Because package pin count permitted it, each driver has been equipped with a dual input logic gate for added flexibility. Placing four high-power drivers in a single package also improves system reliability and reduces total system cost. In some applications, one of these drivers can replace not only two packages of single-input drivers, but some of the associated logic as well.

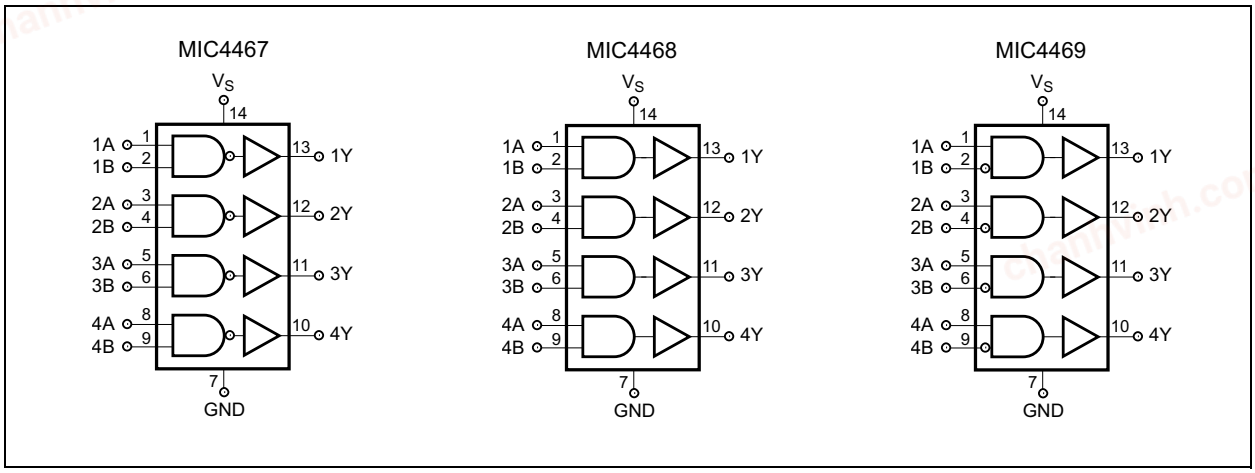
Although primarily intended for driving power MOSFETs, and similar highly capacitive loads, these drivers are equally well suited to driving any other load (capacitive, resistive, or inductive), which requires high efficiency, low-impedance driver capable of high peak currents, rail-to-rail voltage swings, and fast switching times. For example, heavily loaded clock lines, coaxial cables, and piezoelectric transducers can all be driven easily with MIC446x series drivers. The only limitation on loading is that total power dissipation in the IC must be kept within the power dissipation limits of the package.

The MIC446x series drivers are built using a BCD process. They will not latch under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking (either polarity) occurs on the ground line. They can accept up to half an amp of inductive kickback current (either polarity) into their outputs without damage or logic upset.

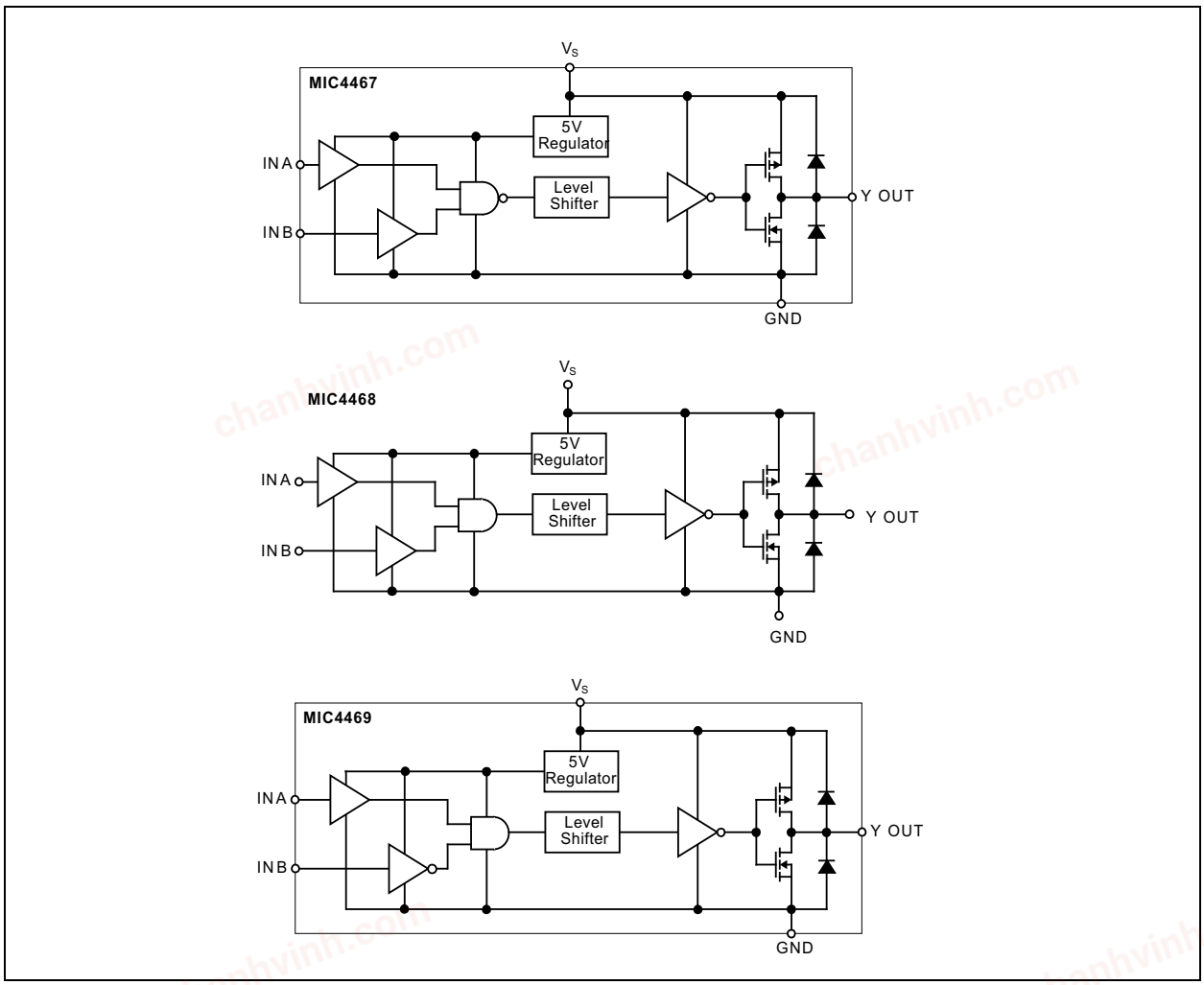
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Logic Diagrams



Block Diagrams



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage ..... +22V
Input Voltage ..... V_S + 0.3V to GND – 5V

Operating Ratings ‡

Power Dissipation
N Package (14-Pin Plastic DIP) 1.5W
WM package (16-Pin Wide SOIC) 1W

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability. Specifications are for packaged product only.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Measured at T_A = +25°C with 4.5V ≤ V_S ≤ 18V unless otherwise specified. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input						
Logic 1 Input Voltage	V_{IH}	2.4	1.3	—	V	—
Logic 0 Input Voltage	V_{IL}	—	1.2	0.8	V	—
Input Current	I_{IN}	–1	—	1	µA	0V ≤ V_{IN} ≤ V_S
Output						
High Output Voltage	V_{OH}	V_S - 0.15	—	—	V	I_{LOAD} = 10 mA
Low Output Voltage	V_{OL}	—	—	0.15	V	I_{LOAD} = 10 mA
Output Resistance	R_O	—	5	15	Ω	I_{OUT} = 10 mA, V_S = 18V
Peak Output Current	I_{PK}	—	1.2	—	A	—
Latch-Up Protection Withstand Reverse Current	I	>500	—	—	mA	—
Switching Time						
Rise Time	t_R	—	14	25	ns	Figure 1-1
Fall time	t_F	—	13	25	ns	Figure 1-1
Delay Time	t_{D1}	—	30	75	ns	Figure 1-1
	t_{D2}	—	45	75	ns	Figure 1-1
Power Supply						
Power Supply Current	I_S	—	0.2	4	mA	—

Note 1: Specification for packaged product only.

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ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Measured over operating temperature range with 4.5V ≤ V_S ≤ 18V unless otherwise specified. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input						
Logic 1 Input Voltage	V_{IH}	2.4	1.4	—	V	—
Logic 0 Input Voltage	V_{IL}	—	1.0	0.8	V	—
Input Current	I_{IN}	–1	—	1	µA	0V ≤ V_{IN} ≤ V_S
Output						
High Output Voltage	V_{OH}	V_S - 0.3	—	—	V	I_{LOAD} = 10 mA
Low Output Voltage	V_{OL}	—	—	0.3	V	I_{LOAD} = 10 mA
Output Resistance	R_O	—	7	30	Ω	I_{OUT} = 10 mA, V_S = 18V
Peak Output Current	I_{PK}	—	1.2	—	A	—
Latch-Up Protection Withstand Reverse Current	I	500	—	—	mA	—
Switching Time						
Rise Time	t_R	—	17	50	ns	Figure 1-1
Fall time	t_F	—	16	50	ns	Figure 1-1
Delay Time	t_{D1}	—	35	100	ns	Figure 1-1
	t_{D2}	—	55	100	ns	Figure 1-1
Power Supply						
Power Supply Current	I_S	—	0.4	8	mA	—

Note 1: Specification for packaged product only.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Ambient Temperature	T_A	–40	—	+85	°C	Temperature Range Device: Y
		0	—	+70	°C	Temperature Range Device: Z
Maximum Junction Temperature	T_J	—	—	+150	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	T_{LEAD}	—	—	+300	°C	Soldering, 10 sec.
Package Thermal Resistances						
Thermal Resistance 14-Lead PDIP	θ_{JA}	—	80	—	°C/W	—
Thermal Resistance 16-Lead Wide SOIC	θ_{JA}	—	120	—		—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}).

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Test Circuits

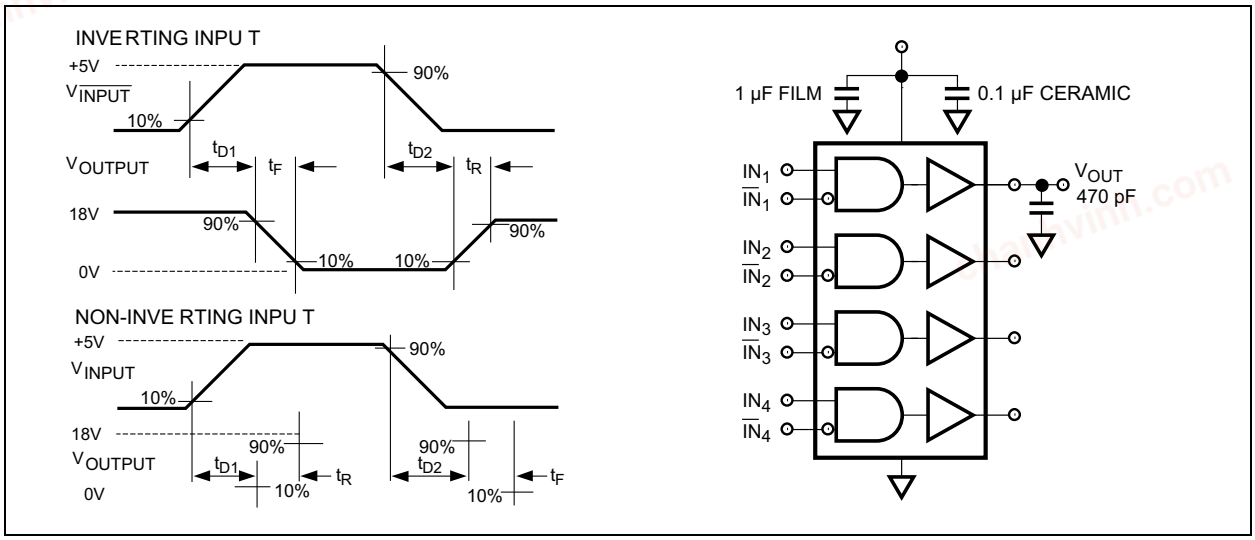


FIGURE 1-1: *Inverting and Non-Inverting Input.*

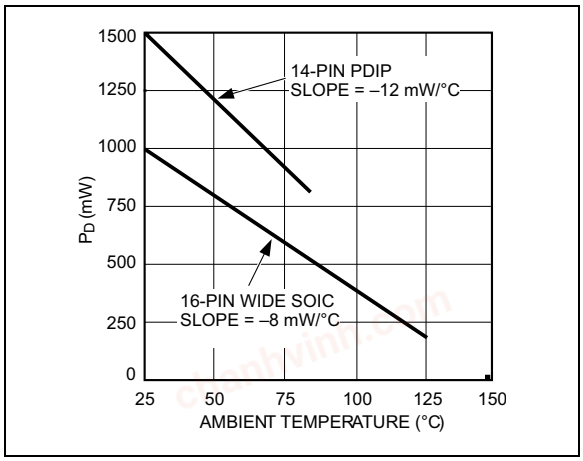


FIGURE 1-2: *Package Power Dissipation.*

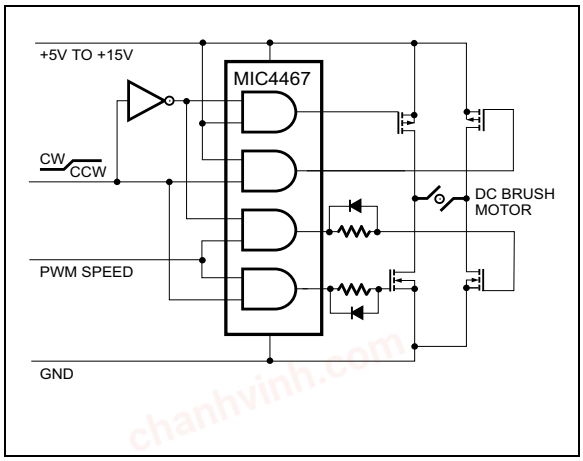


FIGURE 1-3: *Quad Driver Drives H Bridge to Control motor Speed and Direction.*

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

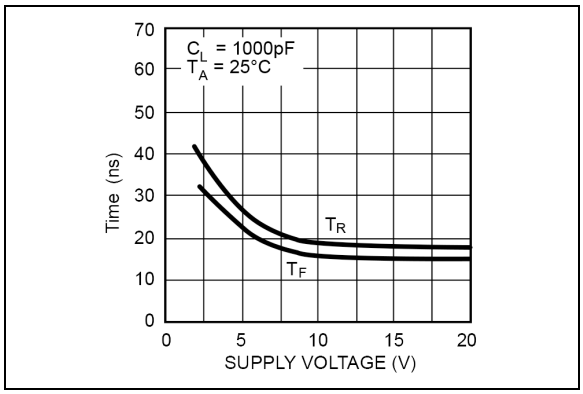


FIGURE 2-1: *Rise and Fall Time vs. Supply Voltage.*

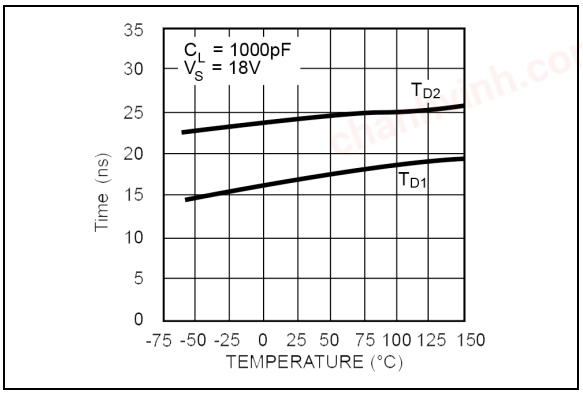


FIGURE 2-4: *Delay Time vs. Temperature.*

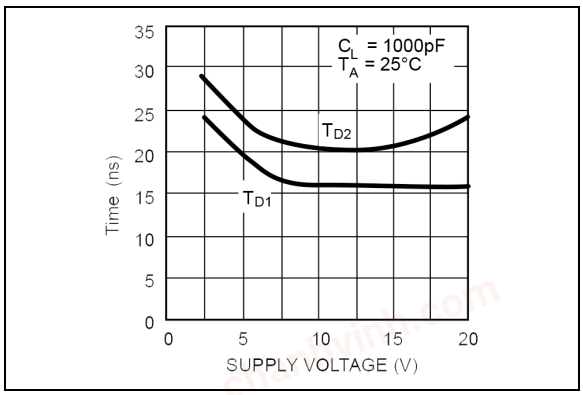


FIGURE 2-2: *Delay Time vs. Supply Voltage.*

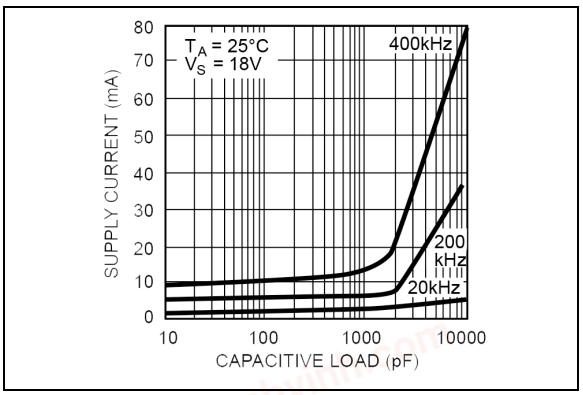


FIGURE 2-5: *Supply Current vs. Capacitive Load.*

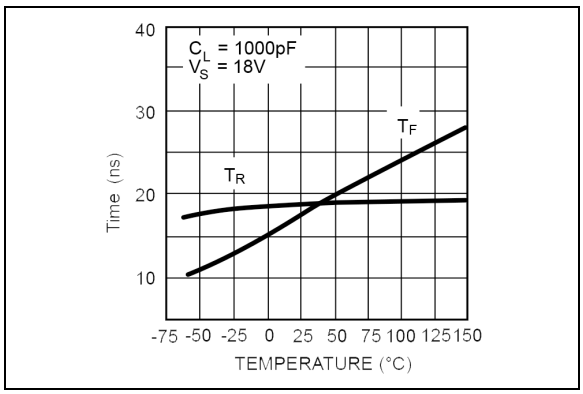


FIGURE 2-3: *Rise and Fall Time vs. Temperature.*

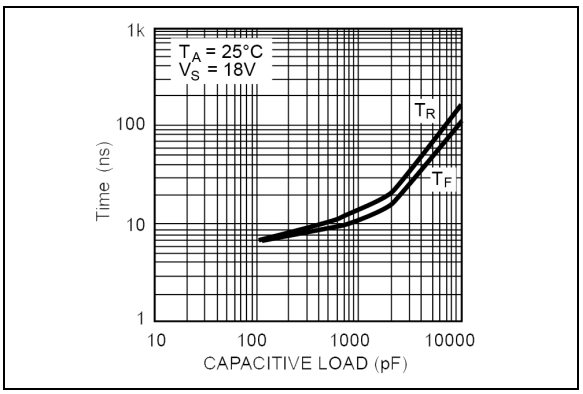


FIGURE 2-6: *Rise and Fall Time vs. Capacitive Load.*

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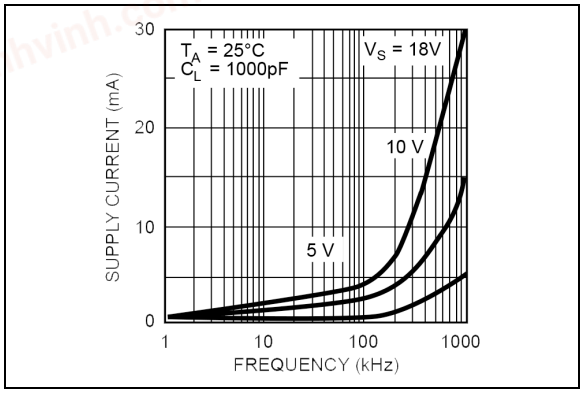


FIGURE 2-7: *Supply Current vs. Frequency.*

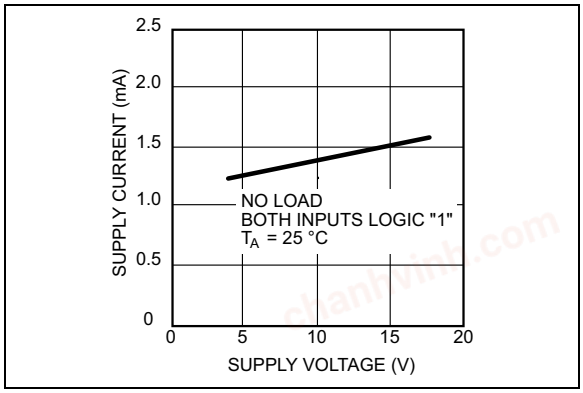


FIGURE 2-10: *Quiescent Power Supply Current vs. Supply Voltage.*

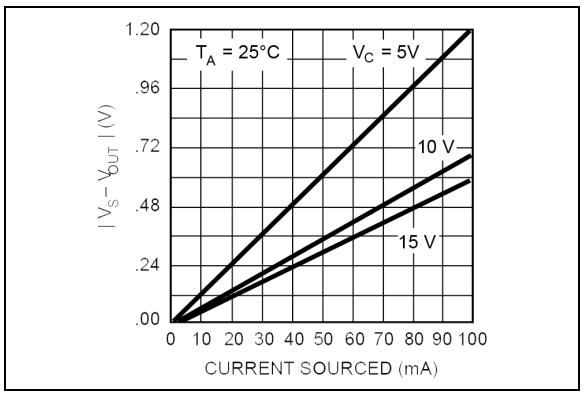


FIGURE 2-8: *High Output vs. Current.*

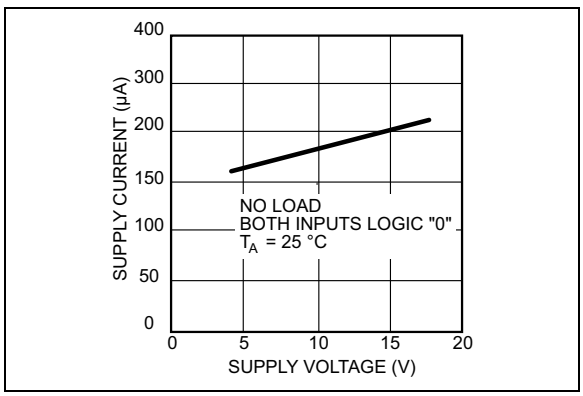


FIGURE 2-11: *Quiescent Power Supply Current vs. Supply Voltage.*

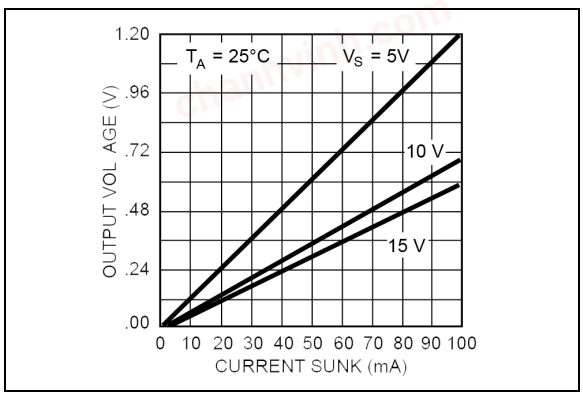
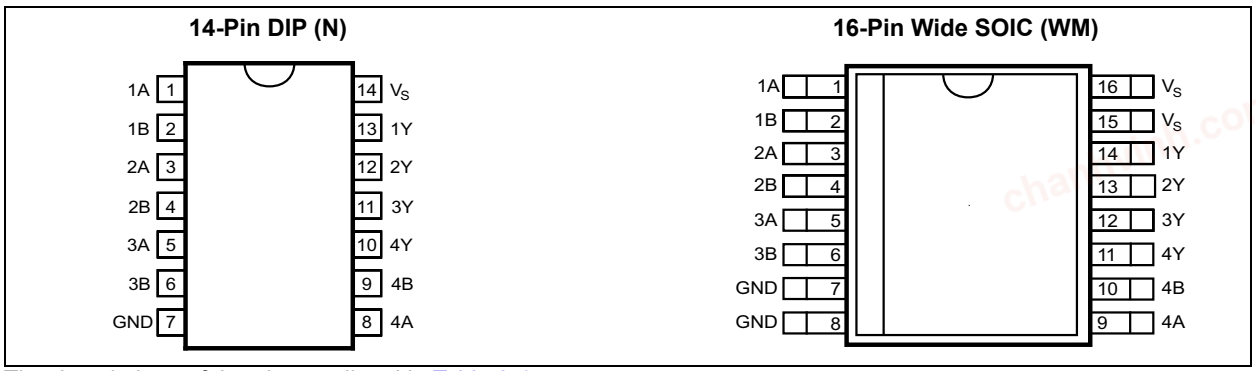


FIGURE 2-9: *Low Output vs. Current.*

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3.0 PIN DESCRIPTIONS

Package Types



The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number DIP	Pin Number Wide SOIC	Pin Name	Description
1	1	1A	Input A for Driver 1. TTL/CMOS Compatible Input
2	2	1B	Input B for Driver 1. TTL/CMOS Compatible Input
3	3	2A	Input A for Driver 2. TTL/CMOS Compatible Input
4	4	2B	Input B for Driver 2. TTL/CMOS Compatible Input
5	5	3A	Input A for Driver 3. TTL/CMOS Compatible Input
6	6	3B	Input B for Driver 3. TTL/CMOS Compatible Input
7	7	GND	Ground
8	—	4A	Input A for Driver 4. TTL/CMOS Compatible Input
—	8	GND	Ground
9	—	4B	Input B for Driver 4. TTL/CMOS Compatible Input
—	9	4A	Input A for Driver 4. TTL/CMOS Compatible Input
10	—	4Y	Output for Driver 4, CMOS Push-Pull Output
—	10	4B	Input B for Driver 4. TTL/CMOS Compatible Input
11	—	3Y	Output for Driver 3, CMOS Push-Pull Output
—	11	4Y	Output for Driver 4, CMOS Push-Pull Output
12	—	2Y	Output for Driver 2, CMOS Push-Pull Output
—	12	3Y	Output for Driver 3, CMOS Push-Pull Output
13	—	1Y	Output for Driver 1, CMOS Push-Pull Output
—	13	2Y	Output for Driver 2, CMOS Push-Pull Output
14	—	VS	Supply Input, 4.5V to 18V
—	14	1Y	Output for Driver 1, CMOS Push-Pull Output
—	15	VS	Supply Input, 4.5V to 18V
—	16	VS	Supply Input, 4.5V to 18V

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3.1 Truth Table

TABLE 3-2: TRUTH TABLE

Part No.	Inputs		Output
	A	B	Y
MIC4467 (Each Driver)	L	X	H
	X	L	H
	H	H	L
MIC4468 (Each Driver)	H	H	H
	L	X	L
	X	L	L
MIC4469 (Each Driver)	L	X	L
	X	H	L
	H	L	H

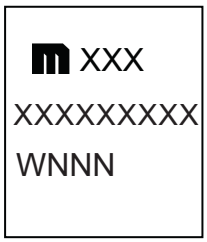
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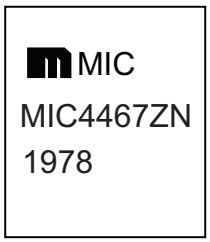
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

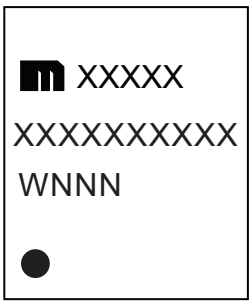
16-Lead PDIP*



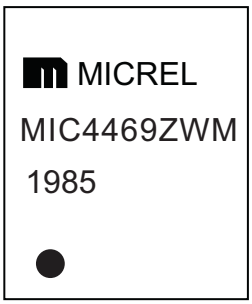
Example



16-Lead Wide SOIC*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:		In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo. Underbar (_) and/or Overbar (¯) symbol may not be to scale.

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N

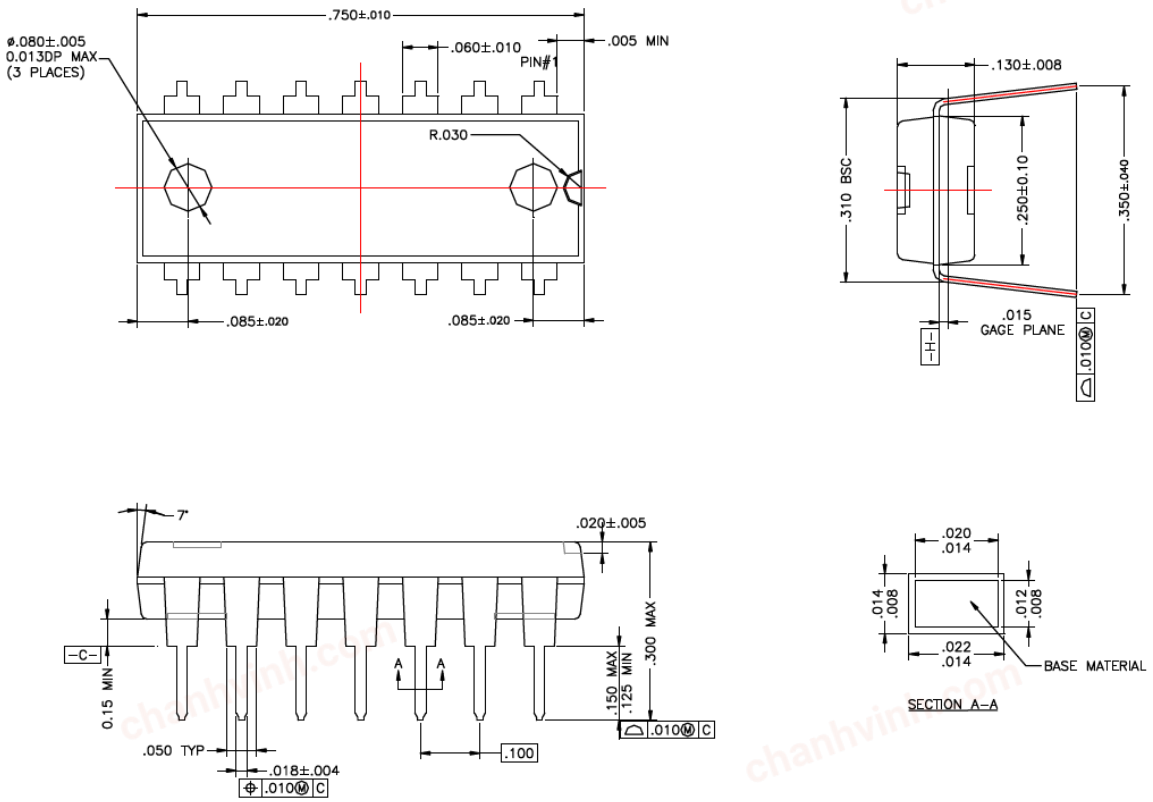
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14-Lead Plastic DIP Package Outline and Recommended Land Pattern

TITLE
14 LEAD PDIP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	PDIP-14LD-PL-1	UNIT	INCH
LEAD FRAME	Copper	LEAD FINISH	Matte Tin



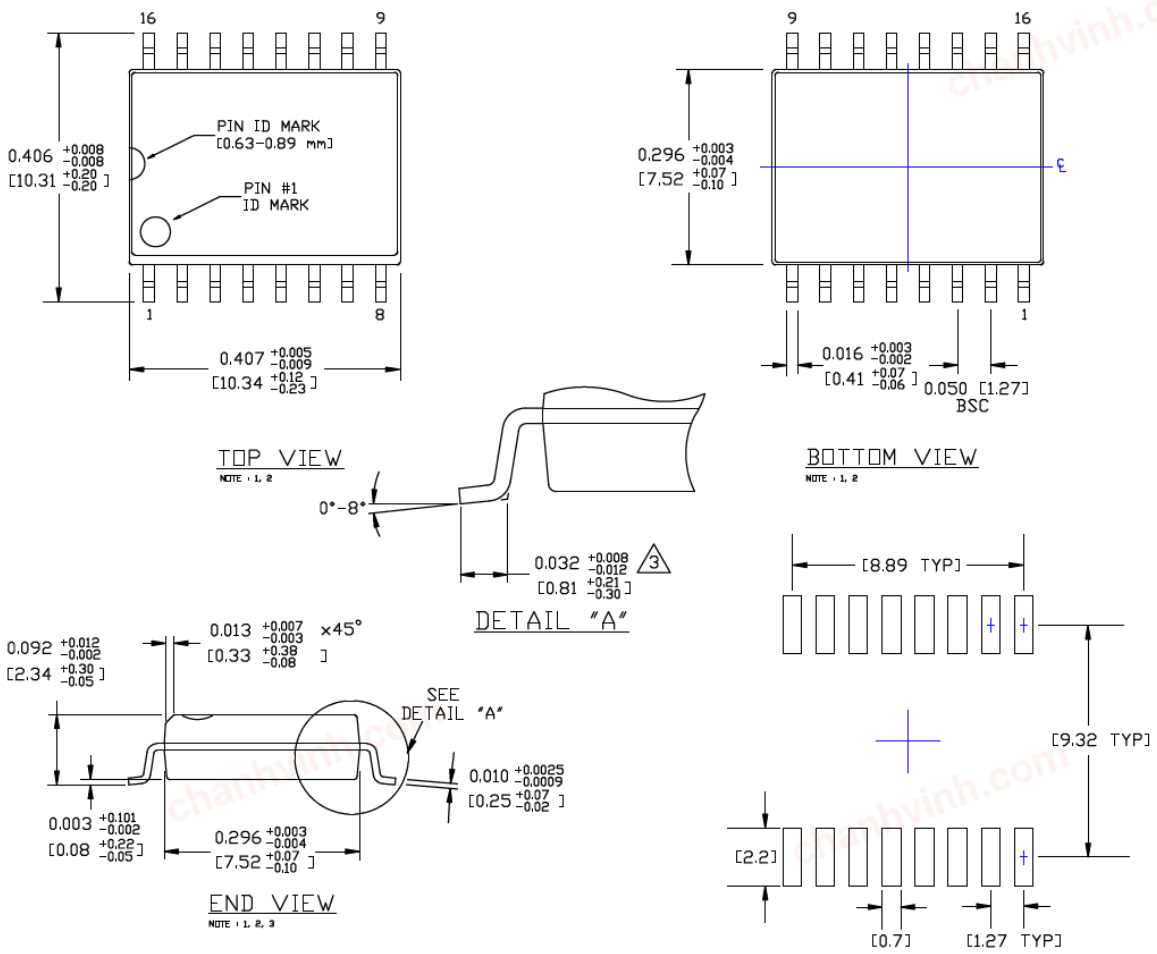
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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16-Lead Wide SOIC Package Outline and Recommended Land Pattern

TITLE
16 LEAD SOICW PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SOICW-16LD-PL-1	UNIT	INCH [MM]



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.15] PER SIDE.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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APPENDIX A: REVISION HISTORY

Revision A (May 2022)

- Converted Micrel document MIC4467/8/9 to Microchip data sheet DS20006614A.
- Minor text changes throughout.

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NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	XX	–XX
Device	Temperature Range	Package	Media Type

Device:	MIC4467:	Quad 1.2A-Peak Low-Side MOSFET Driver with Bi-Polar/CMOS/DMOS Process featuring NAND Input Logic
	MIC4468:	Quad 1.2A-Peak Low-Side MOSFET Driver with Bi-Polar/CMOS/DMOS Process featuring AND Input Logic
	MIC4469:	Quad 1.2A-Peak Low-Side MOSFET Driver with Bi-Polar/CMOS/DMOS Process featuring AND with 1 Inverting Input Logic
Temperature Range:	Y =	–40°C to +85°C, Industrial (RoHs Compliant)
	Z =	0°C to +70°C, Commercial (RoHs Compliant)
Package:	N =	14-Lead PDIP
	WM =	16-Lead SOIC (Wide Body)
Media Type:	<blank> =	25/Tube (N, PDIP)
	<blank> =	47/Tube (WM, SOIC)
	TR =	1,000/Reel (WM, SOIC)

Examples:

a) MIC4467:	**1.2A-Peak, Quad Low-Side MOSFET Driver, NAND Input Logic, –40°C to +85°C Industrial Temperature Range, RoHS Compliant**
MIC4467YWM	16-Lead SOIC Wide Package, 47/Tube
MIC4467YWM-TR	16-Lead SOIC Wide Package, 1,000/Reel
b) MIC4467:	**1.2A-Peak, Quad Low-Side MOSFET Driver, NAND Input Logic, 0°C to +70°C Commercial Temperature Range, RoHS Compliant**
MIC4467ZN	14-Lead PDIP Package, 25/Tube
MIC4467ZWM	16-Lead SOIC Wide Package, 47/Tube
MIC4467ZWM-TR	16-Lead SOIC Wide Package, 1000/Reel
c) MIC4468:	**1.2A-Peak, Quad Low-Side MOSFET Driver, AND Input Logic, –40°C to +85°C Industrial Temperature Range, RoHS Compliant**
MIC4468YN	14-Lead PDIP Package, 25/Tube
MIC4468YWM	16-Lead SOIC Wide Package, 47/Tube
MIC4468YWM-TR	16-Lead SOIC Wide Package, 1,000/Reel
d) MIC4468:	**1.2A-Peak, Quad Low-Side MOSFET Driver, AND Input Logic, 0°C to +70°C Commercial Temperature Range, RoHS Compliant**
MIC4468ZN	14-Lead PDIP Package, 25/Tube
MIC4468ZWM	16-Lead SOIC Wide Package, 47/Tube
MIC4468ZWM-TR	16-Lead SOIC Wide Package, 1,000/Reel
MIC4469:	**1.2A-Peak, Quad Low-Side MOSFET Driver, AND with 1 Inverting Input Logic, –40°C to +85°C Industrial Temperature Range, RoHS Compliant**
MIC4469YN	14-Lead PDIP Package, 25/Tube
MIC4469YWM	16-Lead SOIC Wide Package, 47/Tube
MIC4469YWM-TR	16-Lead SOIC Wide Package, 1,000/Reel
MIC4469:	**1.2A-Peak, Quad Low-Side MOSFET Driver, AND with 1 Inverting Input Logic, –40°C to +85°C Commercial Temperature Range, RoHS Compliant**
MIC4469ZN	14-Lead PDIP Package, 25/Tube
MIC4469ZWM	16-Lead SOIC Wide Package, 47/Tube
MIC4469WM-TR	16-Lead SOIC Wide Package, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
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