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MIC33M656

6A, Power Module Buck Converter with HyperLight Load® and I²C Interface

Features

- Input Voltage Range: 2.4V to 5.5V
- 6A Output Current
- Multiple Faults Indication through I²C
- I²C Programmable:
  - Output voltage: 0.6V-1.28V, 5 mV resolution; 0.6V-3.84V, 10/20 mV resolution
  - Slew rate: 0.2 ms/V-3.2 ms/V
  - On time (switching frequency)
  - High-side current limit: 3.5A-10A
  - Enable delay: 0.2 ms-3 ms
  - Output discharge when disabled (EN = GND)
- High Efficiency (up to 95%)
- Ultra-Fast Transient Response
- ±1.5% Output Voltage Accuracy Over Line/Load/Temperature Range
- Safe Start-up with Pre-Biased Output
- Typical 1.5 µA Shutdown Supply Current
- Low Dropout (100% Duty Cycle) Operation
- I²C Speed, Up to 3.4 MHz
- Latch-Off Thermal Shutdown Protection
- Latch-Off Current Limit Protection
- Meets CISPR32 Class B Emissions
- Power Good (PG) Open-Drain Output
- Package: 53-Lead, 6 mm x 10 mm B1QFN

Applications

- Solid-State Drives (SSD)
- FPGAs, DSP and Low-Voltage ASIC Power

General Description

The Microchip MIC33M656 is an I²C programmable, high-efficiency, low-voltage input, 6A current, synchronous step-down regulator power module with integrated inductor. The Constant-On-Time (COT) control architecture with HyperLight Load® mode provides very high efficiency at light loads, while still having ultra-fast transient response.

The I²C interface allows programming the output voltage, between 0.6V and 1.28V with 5 mV resolution, or between 0.6V and 3.84V with 10 mV and 20 mV resolution. Three different default voltage options (0.6V, 0.9V and 1.0V) are provided so that the application can be started with a safe voltage level and then moved to high-performance modes under I²C control.

An open-drain Power Good output facilitates output voltage monitoring and sequencing. If set in shutdown (EN = GND), the MIC33M656 typically draws 1.5 µA, while the output is discharged through a 10Ω pull-down (if the output discharge feature is enabled).

The MIC33M656 pinout is compatible with the MIC33M650, so that applications can be easily converted.

The 2.4V to 5.5V input voltage range, low shutdown and quiescent currents make the MIC33M656 ideal for single-cell Li-ion battery-powered applications. The 100% duty cycle capability provides low dropout operation, extending operating range in portable systems.

The MIC33M656 is available in a thermally efficient, 53-Lead, 6 mm x 10 mm x 3 mm B1QFN package, with an operating junction temperature range from -40°C to +125°C.

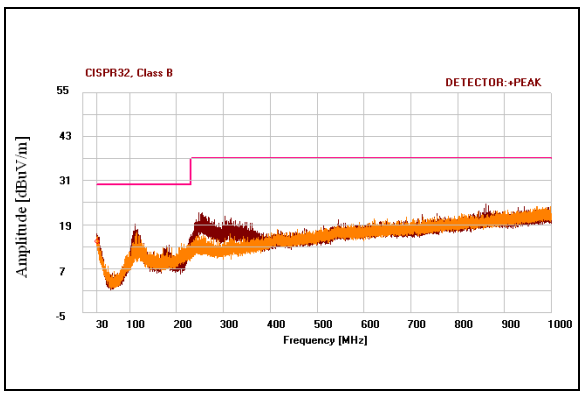


FIGURE 1: *Radiated Emissions, CISPR32, Class B (V_{IN} = 5V, V_{OUT} = 1V, I_{OUT} = 6A).*

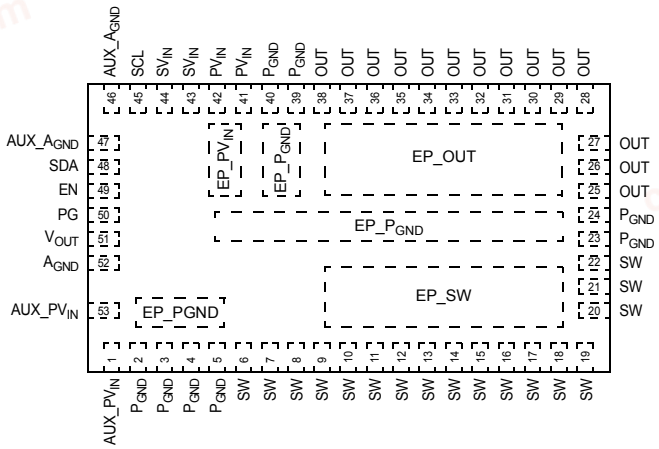
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MIC33M656

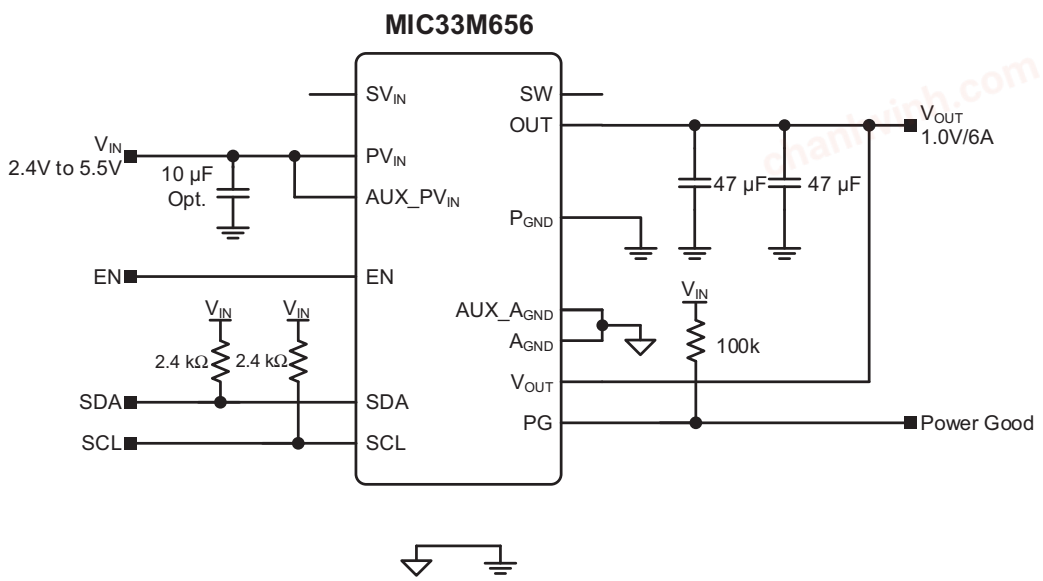
Package Types

MIC33M656
53-Pin B1QFN*
6 mm x 10 mm



* Includes Exposed Thermal Pads (EP); see Table 3-1.

Typical Application



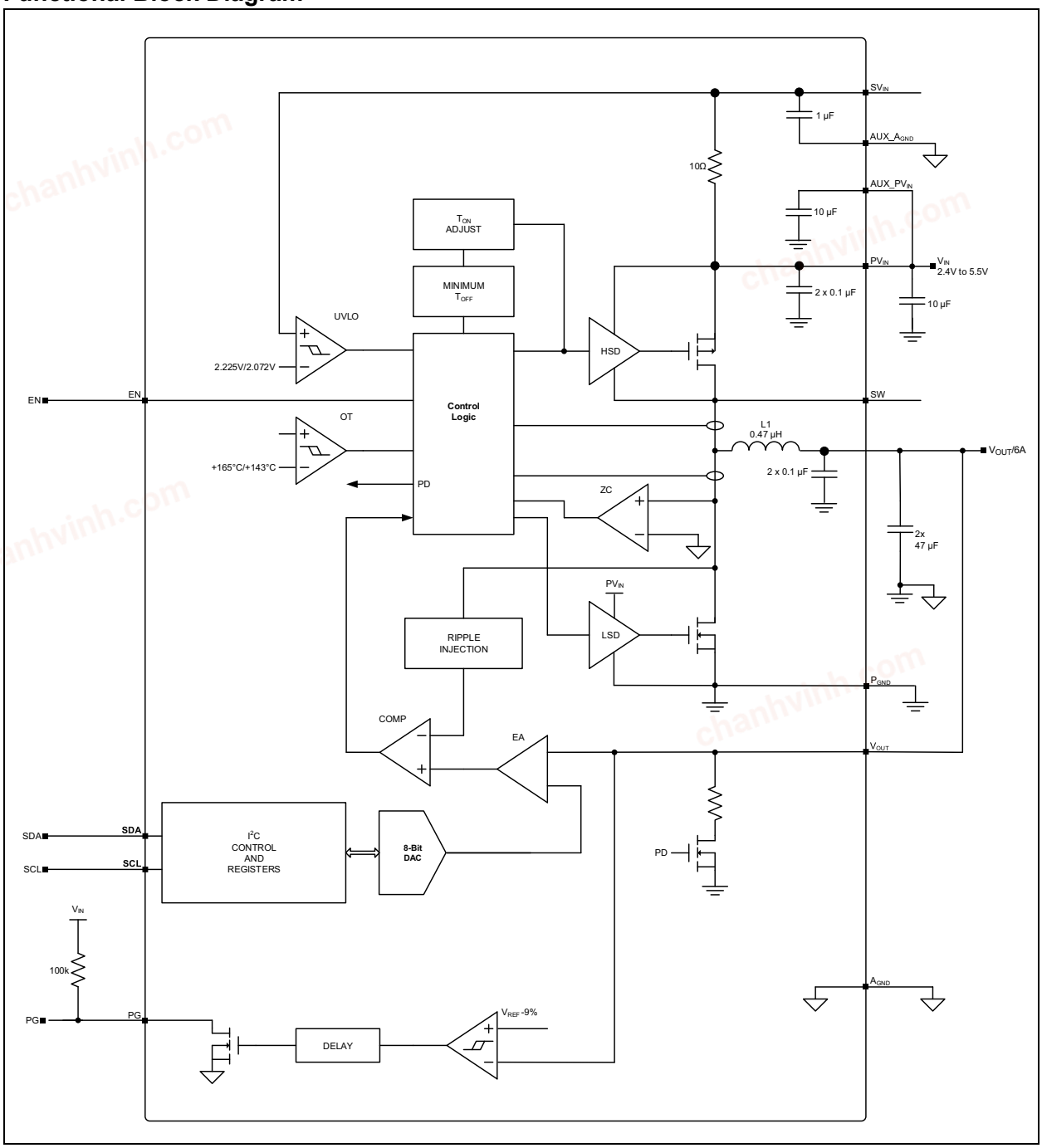
Ordering Information

Part Number	Default Status at Power-up						Output Voltage Range/Step
	Output Voltage	High-Side Current Limit (typical)	TON[1:0] (ns)	Soft Start Speed	Overtemp Latch-Off	Output Pull-Down When Disabled	
MIC33M656-HAYMP	1.0V	10A	[10] – 130 ns	800 µs/V	Latch-Off after 4 OT Cycles	Yes	0.600V-1.280V/5 mV
MIC33M656-FAYMP	0.9V	10A	[10] – 130 ns	800 µs/V	Latch-Off after 4 OT Cycles	Yes	0.600V-1.280V/5 mV
MIC33M656-SAYMP	1.0 V	10A	[10] – 130 ns	800 µs/V	Latch-Off after 4 OT Cycles	Yes	0.600V-1.280V/10 mV 1.280V-3.840V/20 mV

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Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

SV_{IN}, PV_{IN} to A_{GND} ..... -0.3V to +6V
V_{SW} to A_{GND} ..... -0.3V to +6V
V_{EN} to A_{GND} ..... -0.3V to PV_{IN}
V_{PG} to A_{GND} ..... -0.3V to PV_{IN}
V_{SDA}, V_{SCL} to A_{GND} ..... -0.3V to PV_{IN}
PV_{IN} to SV_{IN} ..... -0.3V to +0.3V
A_{GND} to P_{GND} ..... -0.3V to +0.3V
Junction Temperature ..... +150°C
Storage Temperature (T_S) ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +260°C
ESD Rating (**Note 1**)
HBM 2000V
CDM 1500V

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Devices are ESD-sensitive. Handling precautions recommended. Human body model, 1.5 kΩ in series with 100 pF.

Operating Ratings(1)

Supply Voltage (PV_{IN}) ..... 2.4V to 5.5V
Enable Voltage (V_{EN}) ..... 0V to PV_{IN}
Power Good (PG) Pull-up Voltage (V_{PU_PG}) ..... 0V to 5.5V
AUX_PV_{IN} to PV_{IN} .....0V (shorted in operation)
AUX_A_{GND} to A_{GND} .....0V (shorted in operation)
Maximum Output Current..... 6A
Junction Temperature (T_J) ..... -40°C to +125°C

Note 1: The device is not ensured to function outside the operating range.

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ELECTRICAL CHARACTERISTICS[1,2]

Electrical Specifications: Unless otherwise specified, PV_{IN} = 5V; V_{OUT} = 1.0V; C_{OUT} = 2 x 47 µF; T_A = +25°C. **Boldface** values indicate -40°C ≤ T_J ≤ +125°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
V_{IN} Supply						
Input Range	PV_{IN}	**2.4**	—	**5.5**	V	
Undervoltage Lockout Threshold	UVLO	**2.15**	2.225	**2.35**	V	SV_{IN} rising
Undervoltage Lockout Hysteresis	UVLO_H	—	153	—	V	SV_{IN} falling
Operating Supply Current	I_{IN0}	—	60	**100**	µA	V_{FB} = 1.2V, non-switching
Shutdown Current	I_{SHDN}	—	1.5	10	µA	V_{EN} = 0V, PV_{IN} = SV_{IN} = 5.5V, V_{SW} = V_{SDA}= V_{SCL} = 0V, -40°C ≤ T_J ≤ +105°C
				20	µA	V_{EN} = 0V, PV_{IN} = SV_{IN} = 5.5V, V_{SW} = V_{SDA}= V_{SCL} = 0V, -40°C ≤ T_J ≤ +125°C
Output Voltage						
Output Accuracy	V_{OUT_ACC}	**-1.5**	—	**1.5**	%	V_{OUT} from 0.6V to 1.28V (includes line and load regulation)
Output Voltage Step (options HAYMP, FAYMP)	V_{OUT_STEP}	—	5	—	mV	V_{OUT} from 0.6V to 1.28V
Output Voltage Step (option SAYMP)	V_{OUT_STEP}	—	10	—	mV	V_{OUT} from 0.6V to 1.28V
		—	20	—		V_{OUT} from 1.28V to 3.84V
Line Regulation		—	0.06	—	%	V_{OUT} = 1.0V, V_{IN} = 2.5 to 5.5V, I_{OUT} = 300 mA
Load Regulation		—	0.2	—	%	V_{OUT} = 1.0V, I_{OUT} = 0A to 6A
Enable Control						
EN Logic Level High	V_{EN_H}	**1.2**	—	—	V	V_{EN} Rising, regulator enabled
EN Logic Level Low	V_{EN_L}	—	—	**0.4**	V	V_{EN} falling, regulator shutdown
EN Low Input Current	I_{EN_L}	—	0.01	500	nA	V_{EN} = 0V
EN High Input Current	I_{EN_H}	—	0.01	500	nA	V_{EN} = 5.5V
Enable Delay (Two Bits)						
Enable Lockout Delay		0.15	0.25	0.4	ms	EN_DELAY[1:0] = 00, default
		0.85	1	1.20	ms	EN_DELAY[1:0] = 01
		1.70	2	2.35	ms	EN_DELAY[1:0] = 10
		2.55	3	3.5	ms	EN_DELAY[1:0] = 11

Note 1: Specification for packaged product only.

2: Characterized in open loop.

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ELECTRICAL CHARACTERISTICS[1,2] (CONTINUED)

Electrical Specifications: Unless otherwise specified, PV_{IN} = 5V; V_{OUT} = 1.0V; C_{OUT} = 2 x 47 µF; T_A = +25°C. **Boldface** values indicate -40°C ≤ T_J ≤ +125°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Internal DAC Slew Rate (Four Bits)						
Slew Rate Time (time to 1V)	T_{RISE}	100	200	300	µs/V	SLEW_RATE[3:0] = 0000
		250	400	550	µs/V	SLEW_RATE[3:0] = 0001
		400	600	800	µs/V	SLEW_RATE[3:0] = 0010
		600	800	1000	µs/V	SLEW_RATE[3:0] = 0011, default
		750	1000	1250	µs/V	SLEW_RATE[3:0] = 0100
		950	1200	1450	µs/V	SLEW_RATE[3:0] = 0101
		1100	1400	1700	µs/V	SLEW_RATE[3:0] = 0110
		1300	1600	1900	µs/V	SLEW_RATE[3:0] = 0111
		1450	1800	2150	µs/V	SLEW_RATE[3:0] = 1000
		1650	2000	2350	µs/V	SLEW_RATE[3:0] = 1001
		1800	2200	2600	µs/V	SLEW_RATE[3:0] = 1010
		2000	2400	2800	µs/V	SLEW_RATE[3:0] = 1011
		2180	2600	3020	µs/V	SLEW_RATE[3:0] = 1100
		2350	2800	3250	µs/V	SLEW_RATE[3:0] = 1101
		2520	3000	3480	µs/V	SLEW_RATE[3:0] = 1110
		2690	3200	3710	µs/V	SLEW_RATE[3:0] = 1111
TON Control/Switching Frequency (Two Bits)						
Switching On Time	T_{ON}	—	260	—	ns	V_{OUT} = 1V, TON[1:0] = 00
		—	180	—		V_{OUT} = 1V, TON[1:0] = 01
		—	130	—		V_{OUT} = 1V, TON[1:0] = 10
		—	105	—		V_{OUT} = 1V, TON[1:0] = 11
Switching Frequency	FREQ	—	1.6	—	MHz	V_{OUT} = 1V, TON[1:0] = 10, I_{OUT} = 3A
		—	2.2	—	MHz	V_{OUT} = 3.3V, TON[1:0] = 10, I_{OUT} = 3A
Maximum Duty Cycle	DCMAX	—	100	—	%	

Note 1: Specification for packaged product only.

2: Characterized in open loop.

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ELECTRICAL CHARACTERISTICS[1,2] (CONTINUED)

Electrical Specifications: Unless otherwise specified, PV_{IN} = 5V; V_{OUT} = 1.0V; C_{OUT} = 2 x 47 µF; T_A = +25°C. **Boldface** values indicate -40°C ≤ T_J ≤ +125°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Short-Circuit Protection						
High-Side MOSFET Forward Current Limit	I_{LIM_HS}	2.1	3.5	4.9	A	ILIM[1:0] = 00
		4.0	5.0	6.5		ILIM[1:0] = 01
		6.4	8.5	10.6		ILIM[1:0] = 10
		8.0	10.0	12.0		ILIM[1:0] = 11, default
Low-Side MOSFET Forward Current Limit	I_{LIM_LS}	—	3.0	—	A	ILIM[1:0] = 00
		—	4.2	—		ILIM[1:0] = 01
		—	6.8	—		ILIM[1:0] = 10
		—	8.0	—		ILIM[1:0] = 11, default
Low-Side MOSFET Negative Current Limit	I_{LIM_NEG}	-2	-3	-4	A	
N-Channel Zero-Crossing Threshold	I_{ZC_TH}	—	0.9	—	A	
Current Limit Pulses before Hiccup	HICCUP	—	8	—	Cycles	
Hiccup Period before Restart	—	—	1	—	ms	
Internal MOSFETs						
High-Side On-Resistance	$R_{DS-ON-HS}$	—	30	60	mΩ	I_{SW} = 1A
Low-Side On-Resistance	$R_{DS-ON-LS}$	—	16	40	mΩ	I_{SW} = -1A
Output Discharge Resistance	$R_{DS-ON-DSC}$	—	10	50	Ω	V_{EN} = 0V, V_{SW} = 5.5V, from V_{OUT} to P_{GND}
SW Leakage Current	I_{LEAK_SW}	—	1	**10**	µA	PV_{IN} = 5.5V, V_{SW} = 5.5V, V_{EN} = 0V
Power Good (PG)						
PG Threshold	PG_TH	87	91	95	$\%V_{OUT}$	V_{OUT} rising (good)
PG Hysteresis	PG_HYS	—	4	—	$\%V_{OUT}$	V_{OUT} falling
PG Blanking Time	PG_BLANK	—	65	—	µs	
PG Output Leakage Current	PG_LEAK	—	30	—	nA	
PG Sink Low Voltage	PG_SINKV	—	—	200	mV	V_{OUT} = 0V, I_{PG} = 10 mA
I^2C Interface (SCL, SDA)						
Low-Level Input Voltage	V_{IL}	0	—	0.4	V	SV_{IN} = 5.5V
High-Level Input Voltage	V_{IH}	1.2	—	5.5	V	SV_{IN} = 5.5V
High-Level Input Current	I_{I2C_H}	-1	0.01	1	µA	
Low-Level Input Current	I_{I2C_L}	-1	0.01	1	µA	
Logic 0 Output Voltage	V_{OL}	—	—	0.4	V	I_{SDA} = 3 mA, I_{SCL} = 3 mA
SCL,SDA Pin Capacitance	I2C_CAP	—	0.7	—	pF	
SDA Pull-Down Resistance	SDA_PD	—	80	—	Ω	

Note 1: Specification for packaged product only.

2: Characterized in open loop.

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ELECTRICAL CHARACTERISTICS[1,2] (CONTINUED)

Electrical Specifications: Unless otherwise specified, PV_{IN} = 5V; V_{OUT} = 1.0V; C_{OUT} = 2 x 47 µF; T_A = +25°C. **Boldface** values indicate -40°C ≤ T_J ≤ +125°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
I^2C Interface Timing						
Maximum SCL Clock Frequency	SCL_CLOCK	—	100	—	kHz	Standard mode
		—	400	—	kHz	Fast mode
		—	3.4	—	MHz	High-Speed mode
Thermal Shutdown						
Thermal Shutdown	T_{SHDN}	—	165	—	°C	T_J rising
Thermal Shutdown Hysteresis	T_{SHDN_HYST}	—	22	—	°C	T_J falling
Thermal Warning Threshold	T_{ThWrn}	—	118	—	°C	T_J rising
Thermal Latch-Off Soft Start Cycles	TH_LATCH	—	4	—	—	

Note 1: Specification for packaged product only.

2: Characterized in open loop.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise specified, PV_{IN} = 5V; V_{OUT} = 1.0V; C_{OUT} = 2 x 47 µF; T_A = +25°C. **Boldface** values indicate -40°C ≤ T_J ≤ +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature	T_J	40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Package Thermal Resistances						
Thermal Resistance, 53-Lead 6 mm x 10 mm x 3 mm B1QFN	θ_{JA}	—	45	—	°C/W	

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2.0 TYPICAL CHARACTERISTIC CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{IN} = PV_{IN} = AUX_PV_{IN} = 5V; V_{OUT} = 1V; C_{OUT} = 2 x 47 µF; T_A = +25°C.

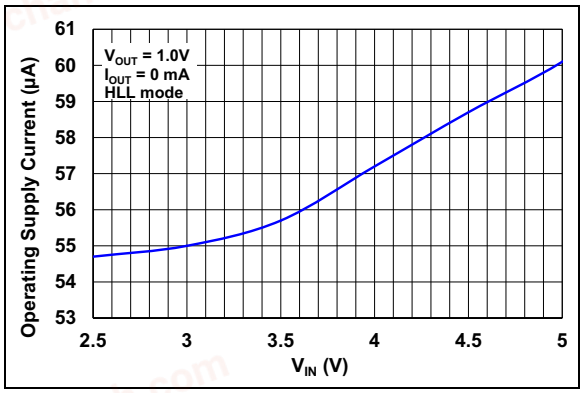


FIGURE 2-1: *Operating Supply Current vs. Input Voltage, Switching.*

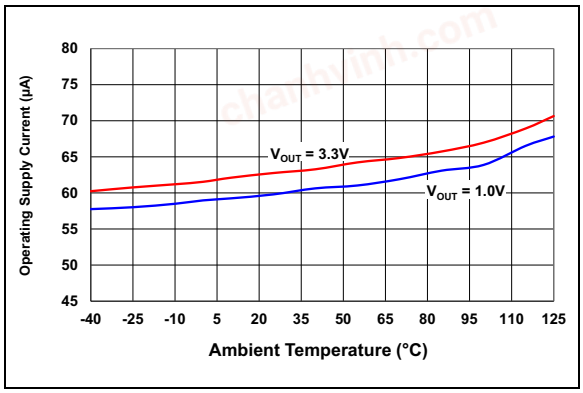


FIGURE 2-4: *Operating Supply Current vs. Temperature, Switching.*

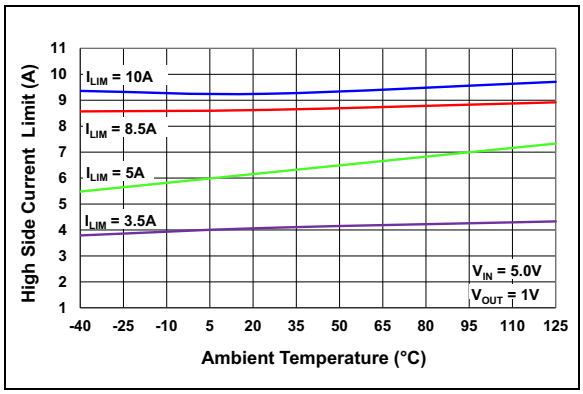


FIGURE 2-2: *High-Side Current Limits vs. Temperature (V_{OUT} = 1.0V), Closed Loop.*

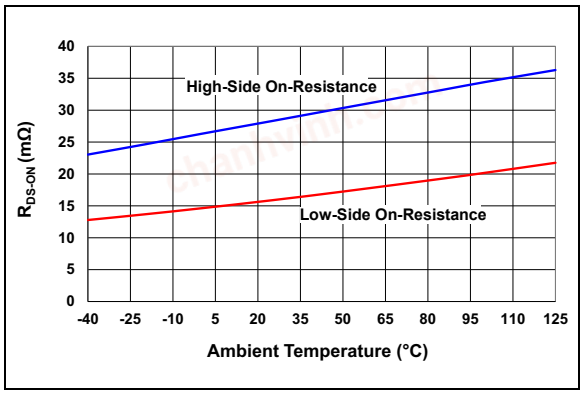


FIGURE 2-5: *$R_{DS(on)}$ vs. Temperature.*

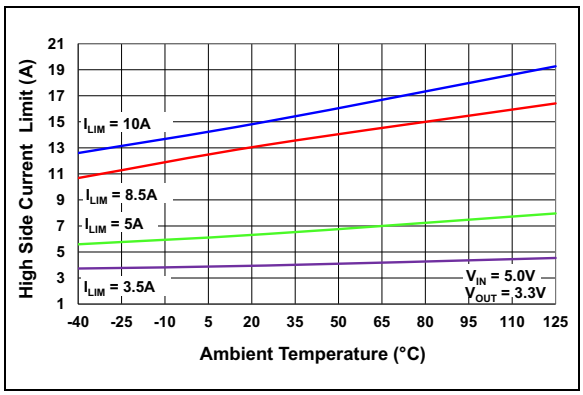


FIGURE 2-3: *High-Side Current Limits vs. Temperature (V_{OUT} = 3.3V), Closed Loop.*

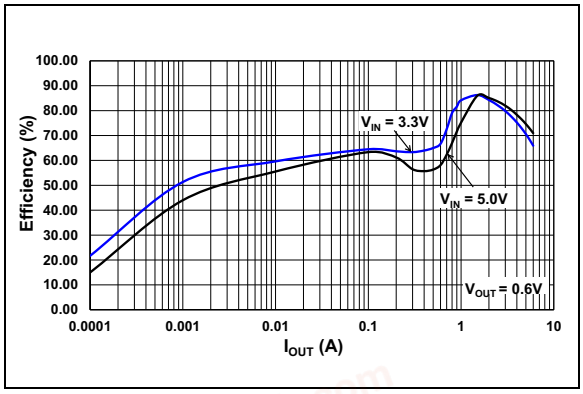


FIGURE 2-6: *Efficiency vs. Load Current (V_{OUT} = 0.6V).*

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Note: Unless otherwise indicated, V_{IN} = PV_{IN} = AUX_PV_{IN} = 5V; V_{OUT} = 1V; C_{OUT} = 2 x 47 µF; T_A = +25°C.

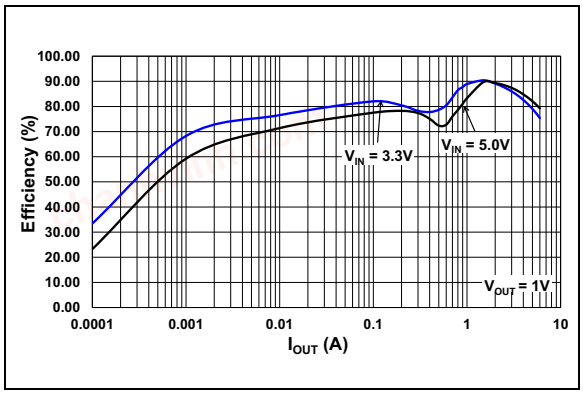


FIGURE 2-7: *Efficiency vs. Load Current (V_{OUT} = 1.0V).*

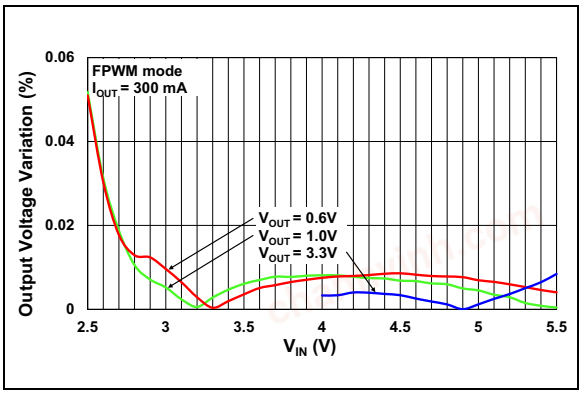


FIGURE 2-10: *Line Regulation: Output Voltage Variation vs. Input Voltage.*

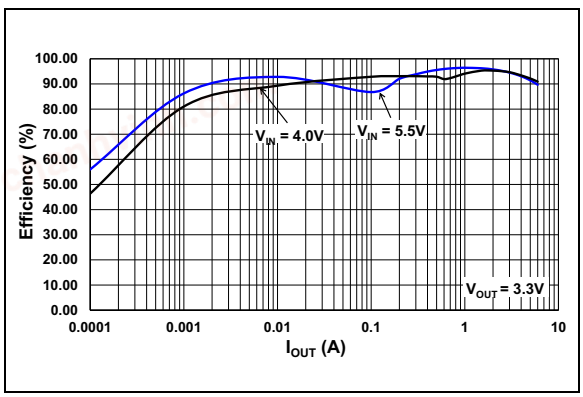


FIGURE 2-8: *Efficiency vs. Load Current (V_{OUT} = 3.3V).*

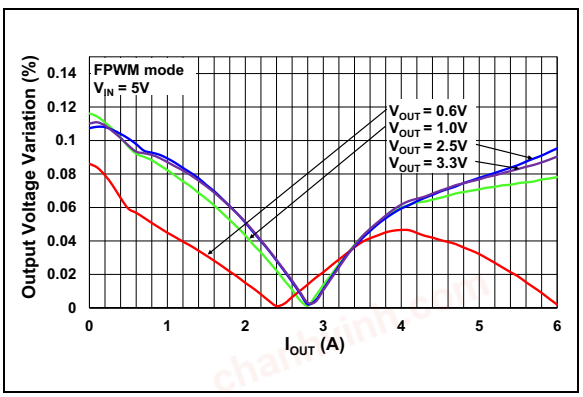


FIGURE 2-11: *Load Regulation: V_{OUT} Voltage Variation vs. I_{OUT}.*

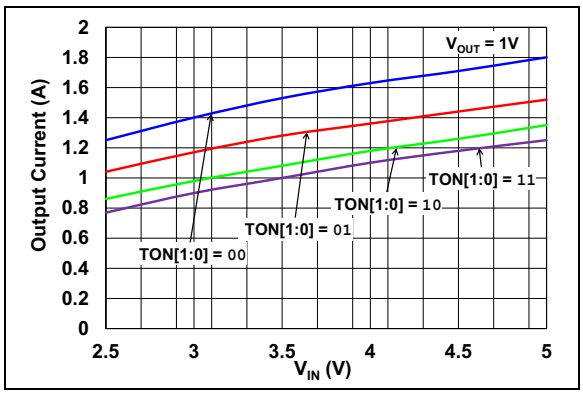


FIGURE 2-9: *DCM/FPWM I_{OUT} Threshold vs. V_{IN}.*

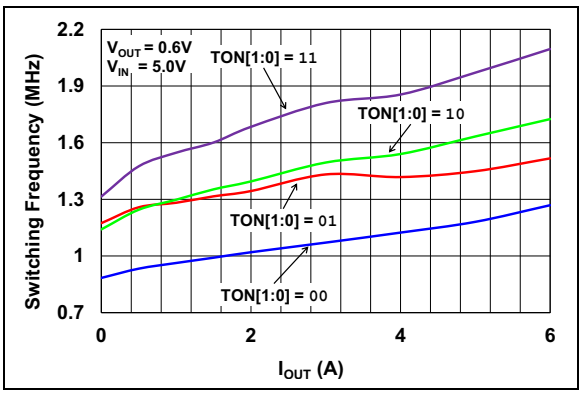


FIGURE 2-12: *Switching Frequency vs. I_{OUT} (V_{OUT} = 0.6V).*

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Note: Unless otherwise indicated, V_{IN} = PV_{IN} = AUX_PV_{IN} = 5V; V_{OUT} = 1V; C_{OUT} = 2 x 47 µF; T_A = +25°C.

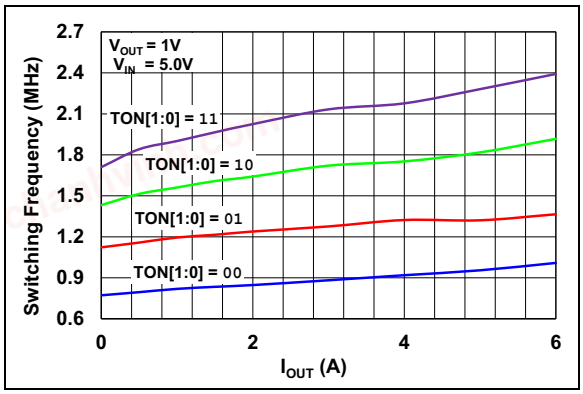


FIGURE 2-13: *Switching Frequency vs. I_{OUT} (V_{OUT} = 1.0V).*

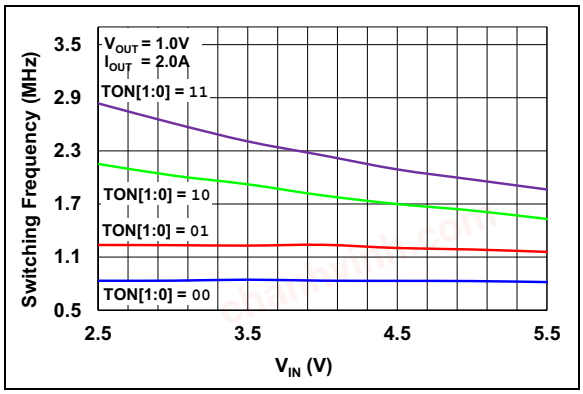


FIGURE 2-16: *Switching Frequency vs. V_{IN} (V_{OUT} = 1.0V).*

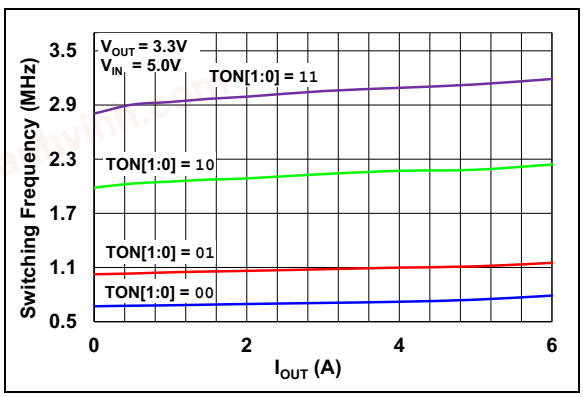


FIGURE 2-14: *Switching Frequency vs. I_{OUT} (V_{OUT} = 3.3V).*

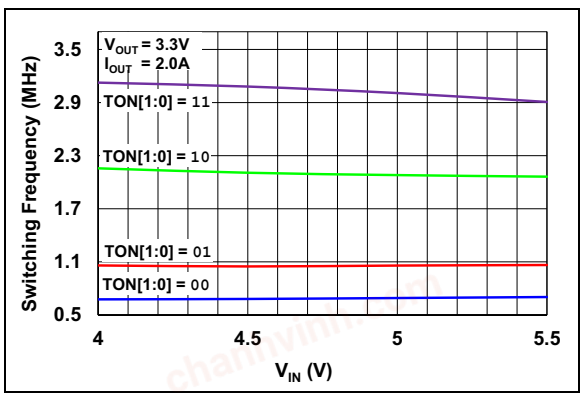


FIGURE 2-17: *Switching Frequency vs. V_{IN} (V_{OUT} = 3.3V).*

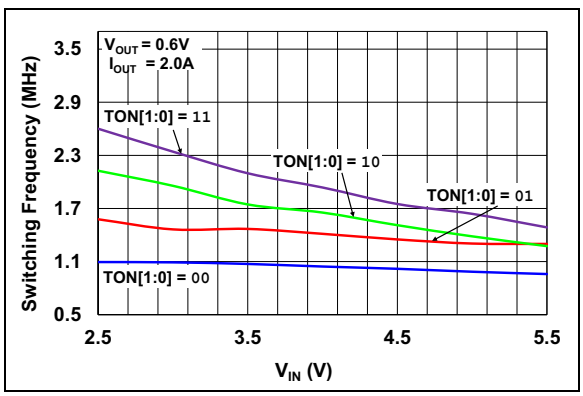


FIGURE 2-15: *Switching Frequency vs. V_{IN} (V_{OUT} = 0.6V).*

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Note: Unless otherwise indicated, V_{IN} = PV_{IN} = AUX_PV_{IN} = 5V; C_{OUT} = 2 x 47 µF; TON[1:0] = 11; ILIM[1:0] = 11; V_{OUT} = 1V; T_A = +25°C.

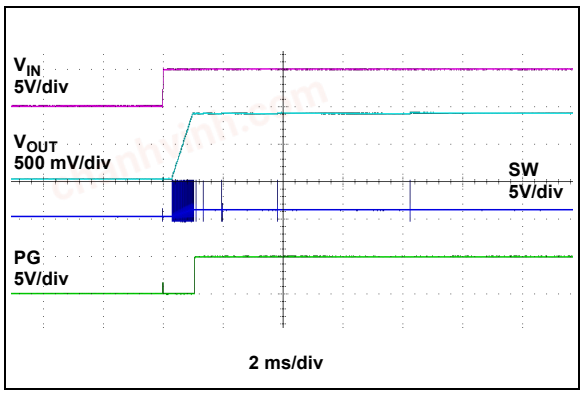


FIGURE 2-18: *V_{IN} Turn-On (EN = PV_{IN}).*

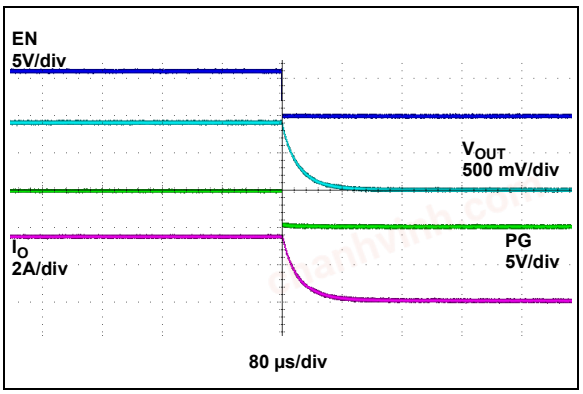


FIGURE 2-21: *EN Turn-Off, R_{LOAD} = 0.3Ω.*

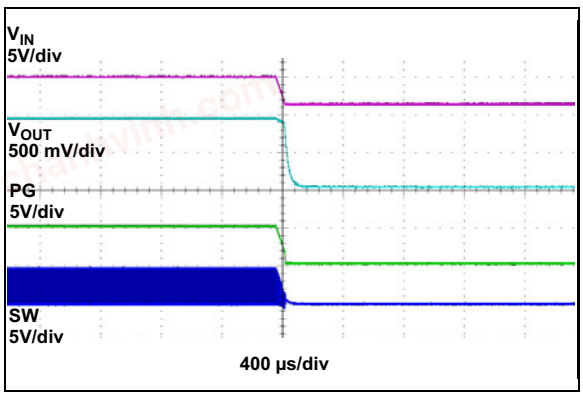


FIGURE 2-19: *V_{IN} Turn-Off (EN = PV_{IN}), R_{LOAD} = 0.3Ω.*

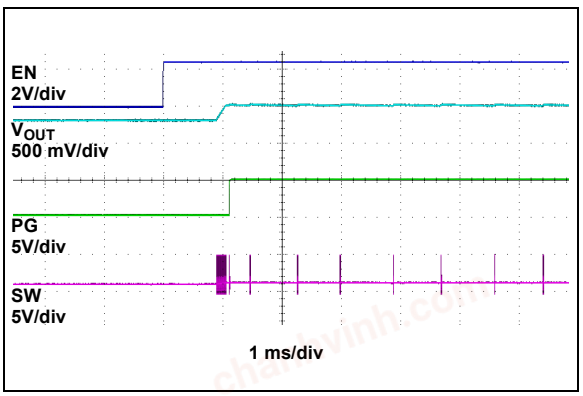


FIGURE 2-22: *EN Turn-On into Pre-Biased Output ($V_{pre\text{-}bias}$ = 0.8V).*

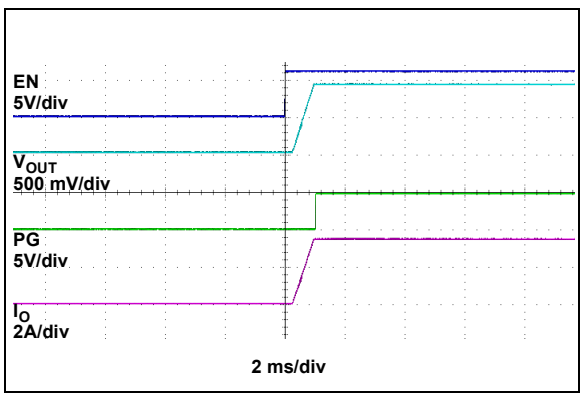


FIGURE 2-20: *EN Turn-On, R_{LOAD} = 0.3Ω.*

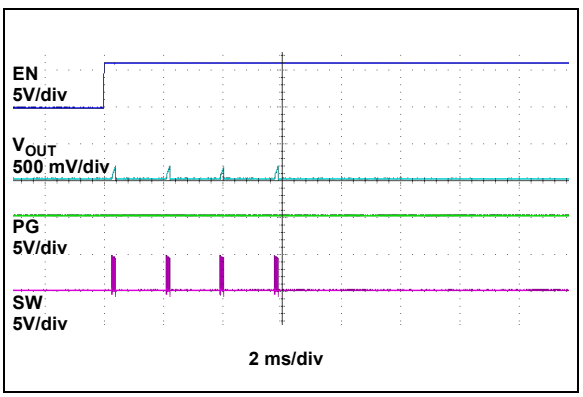


FIGURE 2-23: *Power-up into Short Circuit.*

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Note: Unless otherwise indicated, V_{IN} = PV_{IN} = AUX_PV_{IN} = 5V; C_{OUT} = 2 x 47 µF; TON[1:0] = 11; ILIM[1:0] = 11; V_{OUT} = 1V; T_A = +25°C.

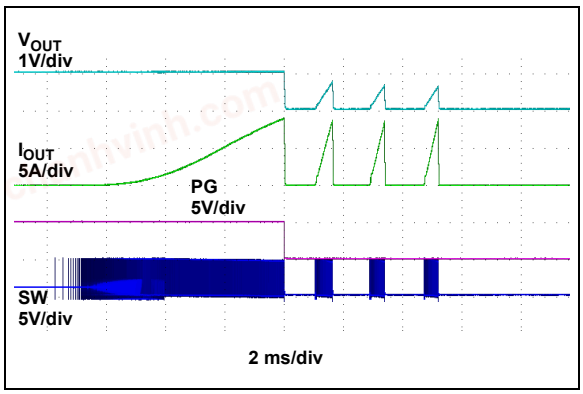


FIGURE 2-24: *Output Current Limit Threshold.*

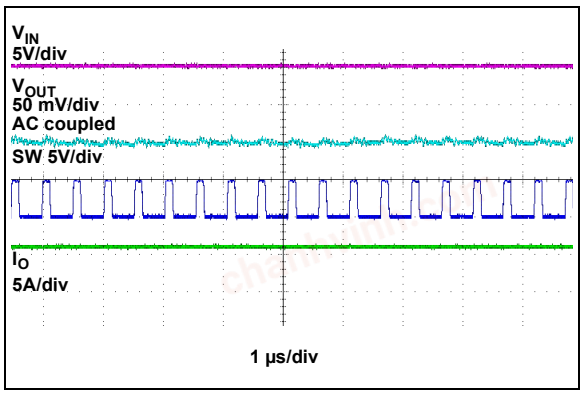


FIGURE 2-27: *Switching Waveforms – I_{OUT} = 6A.*

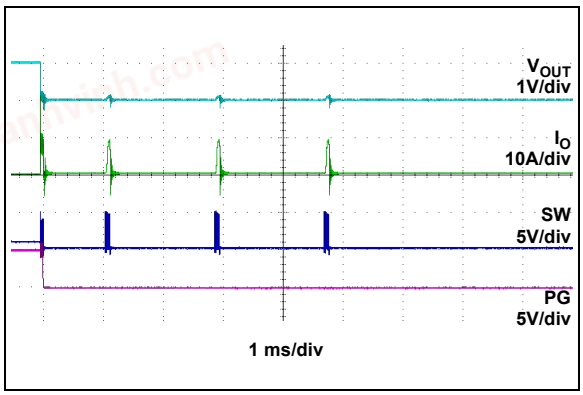


FIGURE 2-25: *Hiccup Mode Short-Circuit Current Limit Response.*

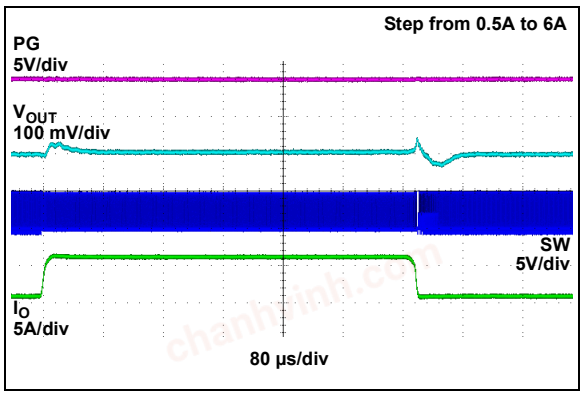


FIGURE 2-28: *Load Transient Response.*

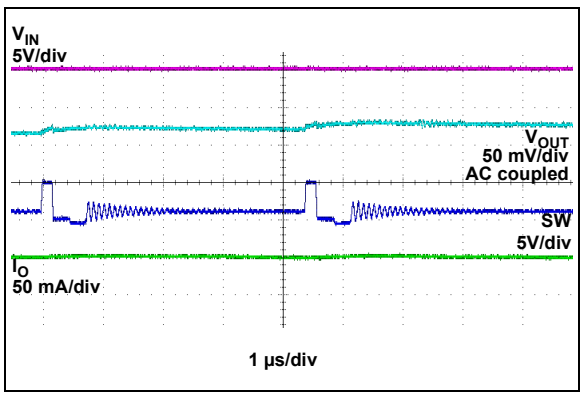


FIGURE 2-26: *Switching Waveforms – I_{OUT} = 50 mA, HLL.*

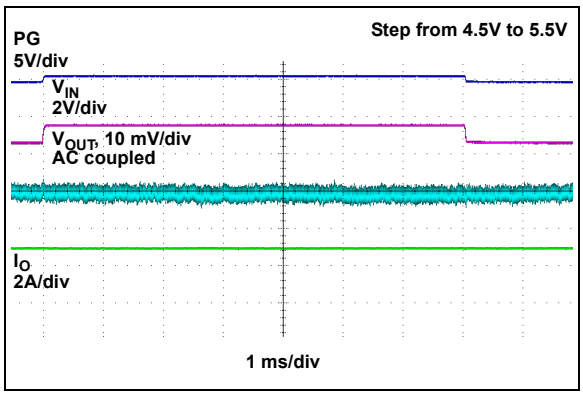


FIGURE 2-29: *Line Transient Response.*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Symbol	Description
2, 3, 4, 5, 23, 24, 39, 40	P_{GND}	Power Ground is the ground path for the MIC33M650 power module.
1, 53	AUX_PV_{IN}	Auxiliary Power Input Voltage Pins: Connect externally to P_{VIN}.
6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22	SW	Switch Node Pins. SW connects to the internal MOSFETs and inductor. Do not connect any external load to this point.
41, 42	PV_{IN}	Power Supply Voltage Pins.
25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38	OUT	Output Side Connection Pins.
43, 44	SV_{IN}	Analog Voltage Input Pins: The power to the internal reference and control sections of the MIC33M650. Internally connected to PV_{IN} through a 10Ω resistor.
46, 47	AUX_A_{GND}	Auxiliary Analog Ground Pins: Connect externally to A_{GND}.
45	SCL	I^2C Clock (Input) Pin: I^2C serial bus clock input.
48	SDA	I^2C Data (Input/Output) Pin: I^2C serial bus data bidirectional pin.
49	EN	Enable (Input) Pin: Logic high enables the operation of the regulator. The EN pin should not be left floating.
50	PG	Power Good (Output) Pin: This is an open-drain output that indicates when the output voltage is higher than the 91% limit.
51	V_{OUT}	Output Voltage Sense (Input) Pin: This pin is used to remotely sense the output voltage. Connect V_{OUT} as close to the output capacitor as possible to sense the output voltage.
52	A_{GND}	Analog Ground Pin: Internal signal ground for all low-power circuits.
54	EP_OUT	Exposed Thermal Pad: Internally connected to OUT.
55	EP_SW	Exposed Thermal Pad: Internally connected to SW node.
56	EP_P_{GND}	Exposed Thermal Pad: Internally connected to P_{GND}.
57	EP_PV_{IN}	Exposed Thermal Pad: Internally connected to PV_{IN}.

3.1 Power Ground Pin (P_{GND})

P_{GND} is the ground path for the MIC33M656 buck converter power stage. The P_{GND} pin connects to the sources of the low-side N-channel MOSFET, the negative terminals of the input capacitors and the negative terminals of the output capacitors. The loop for the Power Ground should be as small as possible and separate from the Analog Ground (A_{GND}) loop.

3.2 Switch Node Pin (SW)

Switching node output pin which connects to the internal MOSFETs and inductor. This is a high-frequency connection; therefore, traces should be kept as short and as wide as practical.

3.3 Input Voltage Pin (PV_{IN})

Input supply to the source of the internal high-side P-channel MOSFET. The PV_{IN} operating voltage range is from 2.4V to 5.5V. An input capacitor between PV_{IN} and the Power Ground (P_{GND}) pin is required and placed as close as possible to the IC.

3.4 Analog Voltage Input Pin (SV_{IN})

The power to the internal reference and control sections of the MIC33M656. Internally connected to PV_{IN} through a 10Ω resistor.

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3.5 I²C Clock Input Pin (SCL)

The SCL pin is the serial interface's serial clock pin. This pin is connected to the host controller SCL pin.

The MIC33M656 is a slave device, so its SCL pin is only an input.

3.6 I²C Data Input/Output Pin (SDA)

The SDA pin is the serial interface's serial data pin. This pin is connected to the host controller SDA pin. The SDA pin has an open-drain N-channel driver.

3.7 Enable Pin (EN)

Logic high enables operation of the regulator. Logic low will shut down the device. In the OFF state, the supply current of the device is greatly reduced (typically 1.5 µA). The EN pin should not be left open.

3.8 Power Good Pin (PG)

This is an open-drain output that indicates when the rising output voltage is higher than the 91% threshold. There is a 4% hysteresis; therefore, PG will return low when the output voltage falls below 87% of the target regulation voltage.

3.9 Output Voltage Sense Pin (V_{OUT})

This pin is used to remotely sense the output voltage. Connect to V_{OUT} as close to the output capacitor as possible to sense the output voltage. This pin also provides the path to discharge the output through an internal 10Ω resistor when the device is disabled.

3.10 Analog Ground Pin (A_{GND})

Internal signal ground for all low-power circuits. Connect to ground plane. For best load regulation, the connection path from A_{GND} to the output capacitor ground terminal should be free from parasitic voltage drops.

3.11 Auxiliary Analog Ground Pins (AUX_A_{GND})

Connect these pins to A_{GND} to make use of the internal decoupling capacitor for SV_{IN} pin filtering.

3.12 Auxiliary Input Voltage Pins (AUX_PV_{IN})

Connect these pins to PV_{IN} to make use of the internal 10 µF capacitor for PV_{IN} filtering/decoupling.

3.13 P_{GND} Exposed Pad (EP_P_{GND})

Electrically connected to the P_{GND} pins. Connect with thermal vias to the ground plane to ensure adequate heat sinking. See **Section 8.0 "Packaging Information"**.

3.14 OUT Exposed Pad (EP_OUT)

Electrically connected to the OUT pins. Must be externally connected to the output power connection.

3.15 SW Exposed Pad (EP_SW)

Electrically connected to the SW node.

3.16 PV_{IN} Exposed Pad (EP_PV_{IN})

Electrically connected to the PV_{IN} pins. Must be connected to the input power connection.

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4.0 FUNCTIONAL DESCRIPTION

4.1 Device Overview

The MIC33M656 is a high-efficiency 6A peak current, synchronous buck regulator with HyperLight Load mode. The module integrates the inductor alongside high-frequency, ripple dampening capacitors on the input and output of the converter and decoupling capacitor for the signal input. The Constant-On-Time (COT) control architecture with automatic HyperLight Load mode provides very high efficiency at light loads and ultra-fast transient response.

The MIC33M656 output voltage is programmed through the I^2C interface, in the range of 0.6V to 1.28V, with 5 mV resolution (options YMP, HAYMP and FAYMP), or between 0.6V and 3.84V (option SAYMP). The latter option has a 10 mV resolution, from 0.6V up to 1.28V and a 20 mV resolution, from 1.28V to 3.84V.

The 2.4V to 5.5V input voltage operating range makes the device ideal for single-cell Li-ion battery-powered applications. Automatic HyperLight Load mode provides very high efficiency at light loads.

This device focuses on high output voltage accuracy. Total output error is less than 1.5% over line, load and temperature.

The MIC33M656 buck regulator uses an adaptive Constant-On-Time control method. The adaptive on-time control scheme is employed to obtain a nearly constant switching frequency in Continuous Conduction mode. Overcurrent protection is implemented by sensing the current on both the low-side and high-side internal power MOSFETs. The device includes an internal soft start function, which reduces the power supply input surge current at start-up by controlling the output voltage rise time.

4.2 HyperLight Load Mode (HLL)

HLL is a power-saving switching mode. In HLL, the switching frequency is not constant over the operation current range. At light loads, the fixed on-time operation, coupled with low-side MOSFET diode emulation, causes the switching frequency to decrease. This reduces switching and drive losses, and increases efficiency. The HLL switching mode can be disabled for reduced output ripple and low noise by setting the FPWM bit in the CTRL2 register.

4.3 Enable (EN Pin)

When the EN pin is pulled low, the IC is in a shutdown state with all internal circuits disabled and with the Power Good (PG) output low. During shutdown, the part typically consumes 1.5 µA. When the EN pin is pulled high, the start-up sequence is initiated. There is a programmable enable delay that is used to delay the start of the output ramp. The enable delay timer can be programmed to one of four time intervals of 0.25 ms, 1 ms, 2 ms or 3 ms in the CTRL1 register. Note that if the 0 ms delay setting is chosen, there is an internal delay of 250 µs before the part will start to switch in order to bias up internal circuitry.

4.4 I^2C Programming

The MIC33M656 behaves as an I^2C slave, accessible at 0x5B (7-bit addressing).

The I^2C interface remains active and the MIC33M656 can be programmed whether the Enable pin is high or low, as long as the input voltage is above the UVLO threshold. This feature is useful in applications where a housekeeping MCU preconfigures the MIC33M656 before enabling power delivery. The registers do not get reset when the enable pin is low. The output voltage can be programmed to a new value with I^2C, regardless of the EN pin status. If the EN pin is high, the output voltage will move to the newly programmed value on-the-fly, with the programmed slew rate.

4.5 Power Good (PG)

The Power Good output is generally used for power sequencing where the Power Good output is tied to the enable output of another regulator. This technique avoids all the regulators powering up at the same time, causing large inrush current.

The Power Good output is an open-drain output. During start-up, when the output voltage is rising, the Power Good output goes high by means of an external pull-up resistor when the output voltage reaches 91% of its set value. The Power Good threshold has 4% hysteresis, so the Power Good output stays high until the output voltage falls below 87% of the set value. A built-in 65 µs blanking time is incorporated to prevent nuisance tripping.

The pull-up resistor from the PG pin can be connected to V_{IN}, V_{OUT} or an external source that is less than or equal to V_{IN}. The PG pin can be connected to another regulator's enable pin for sequencing of the outputs. The PG output is deasserted as soon as the Enable pin is pulled low, or an input undervoltage condition or any other Fault is detected.

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4.6 Output Soft Discharge Option

To ensure a known output condition when the device is turned off, then back on again, the output is actively discharged to ground by means of an internal 10Ω resistor. The active discharge resistor can be enabled or disabled through I^2C in the CTRL2 register.

4.7 Output Voltage Setting

The MIC33M656 output voltage has an 8-bit control DAC that can be programmed from 0.6V to 1.28V, in 5 mV increments, for part options HAYMP and FAYMP. Option SAYMP can be programmed from 0.6V, up to 1.28V, with 10 mV resolution and from 1.28V up to 3.84V, with 20 mV resolution. This can be programmed in the Output Voltage Control (VOUT) register.

The output voltage sensing pin, V_{OUT}, should be connected exactly to the desired Point-of-Load (POL) regulation, avoiding parasitic resistive drops.

4.8 Converter Stability/Output Capacitor

The MIC33M656 utilizes an internal compensation network and it is designed to provide stable operation with output capacitors from 47 µF to 1000 µF. This greatly simplifies the design where supplementary output capacitance can be added without affecting stability.

4.9 Soft Start

Excess bulk capacitance on the output can cause excessive input inrush current. The MIC33M656 internal soft start feature forces the output voltage to rise gradually, keeping the inrush current at reasonable levels. This is particularly important in battery-powered applications. The ramp rate can be set in the CTRL2 register by means of the SLEW_RATE[3:0] bits (see Register 7-2).

When the enable pin goes high, the output voltage starts to rise. Once the soft start period has finished, the Power Good comparator is enabled and if the output voltage is above 91% of the nominal regulation voltage, then the Power Good output goes high.

The output voltage soft start time is determined by the soft start equation below. The Soft Start Time, t_{SS}, can be calculated using Equation 4-1.

EQUATION 4-1:

$$t_{SS} = V_{OUT} \times t_{RAMP}$$
$$t_{SS} = 1.0V \times 800\mu s/V$$
$$t_{SS} = 800\mu s = 0.8ms$$

Where:

V_{OUT} = 1.0V
t_{RAMP} = 800 µs/V

4.10 100% Duty Cycle Operation

The MIC33M656 can deliver 100% duty cycle. To achieve 100% duty cycle, the high-side switch is latched on when the duty cycle reaches around 92% and stays latched until the output voltage falls 4% below its regulated value. This feature is especially useful in battery-operated applications. It is recommended that this feature is enabled together with the highest TON setting, corresponding to the lowest switching frequency (TON[1:0] = 00 in the CTRL1 register). The high-side latch circuitry can be disabled by setting the DIS_100PCT bit in the CTRL2 register to '1'.

4.11 Switching Frequency

The switching frequency of the MIC33M656 is indirectly set by programming the TON value. The equation below provides an estimation for the resulting switching frequency:

EQUATION 4-2:

$$f_{SW} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{T_{ON}}$$

Equation 4-2 is valid only in Continuous Conduction mode and for a loss-less converter. In practice, losses will cause an increase of the switching frequency with respect to the ideal case. As the load current increases, losses will increase too and so will the switching frequency.

The on-time calculation is adaptive, in that the T_{ON} value is modulated based on the input voltage, and on the target output voltage, to stabilize the switching frequency against their variations. Losses are not accounted for.

The table below highlights the resulting On Time (T_{ON}) for typical output voltages:

TABLE 4-1: ON-TIME CALCULATIONS

		T_{ON}			
V_{IN} (V)	V_{OUT} (V)	[00]	[01]	[10]	[11]
5	0.6	140	110	100	80
	1	260	180	130	105
	1.8	520	340	200	150
	2.5	740	490	260	190
	3.3	930	610	310	220
3.3	1	380	270	170	130

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4.12 Undervoltage Protection (UVLO)

Undervoltage protection ensures that the IC has enough voltage to bias the internal circuitry properly and provide sufficient gate drive for the power MOSFETs. When the input voltage starts to rise, both power MOSFETs are off and the Power Good output is pulled low. The IC starts at approximately 2.225V typical and has a nominal 153 mV of hysteresis to prevent chattering between the UVLO high and low states.

4.13 Overtemperature Fault

The MIC33M656 monitors the die junction temperature to keep the IC operating properly. If the IC junction temperature exceeds +118°C, the warning flag, "OT_WARN", is set, but does not affect the operation mode. It automatically resets if the junction temperature drops below the temperature threshold. If the IC junction temperature exceeds +165°C, both power MOSFETs are immediately turned off. The IC is allowed to start when the die temperature falls below +143°C.

During the Fault condition, several changes will occur in the STATUS Register. The OT bit will go high, indicating the junction temperature reached +165°C, while the OT_WARN automatically resets. If the controller is enabled to restart after the first thermal shutdown event (OT_LATCH bit in CTRL2 register is set), the SSD bit will go low and the HICCUP bit will go high. Finally, the PG bit in the FAULT register (address 0x03) will go low and the PG pin will be pulled low until the output voltage has restarted and is once again in regulation. The I^2C interface remains active and all the values stored in registers are maintained. When the die temperature decreases below the lower thermal shutdown threshold, and the MIC33M656 resumes switching with the output voltage going back in regulation, the global Power Good output is pulled high, but the Overtemperature Fault bit, OT, is still set to '1'. To clear the Fault, either recycle input power or write a logic '0' to the Overtemperature bit, OT, in the FAULT register.

During recovery from a thermal shutdown event, if the regulator hits another thermal shutdown event before Power Good can be achieved, the controller will again reset. If this happens four times in a row, the part will be in a Latch-Off state and the MOSFETs are permanently latched off. The LATCH_OFF bit in the STATUS Register will be set to '1', which will latch off the MIC33M656. The device can be restarted by toggling the enable input, by recycling the input power or by software Enable Control (EN_CON). This latch-off feature eliminates the thermal stress on the MIC33M656 during a Fault event. The OT_LATCH bit in the CTRL2 register can be set to '0', which will cause this latch-off to happen after the first overtemperature event, instead of waiting for four consecutive overtemperatures. This is a more conservative approach to protect the part and is available to the user.

4.14 Safe Start-up into a Pre-Biased Output

The MIC33M656 is designed for safe start-up into a pre-biased output in forced PWM. This feature prevents high negative inductor current flow in a pre-bias condition, which can damage the IC. This is achieved by not allowing forced PWM until the control loop commands eight switching cycles. After eight cycles, the low-side negative current limit is switched from 0A to -3A. The cycle counter is reset to zero if the Enable pin is pulled low, or an input undervoltage condition or any other Fault is detected.

4.15 Current Limiting

The MIC33M656 regulator uses both high-side and low-side current sense for current limiting. When the high-side current sense threshold is reached, the high-side MOSFET is turned off and the low-side MOSFET is turned on. The low-side MOSFET stays on until the current falls to 80% of the high-side current threshold value, then the high-side current can be turned on again. If the overload condition lasts for more than seven cycles, the MIC33M656 enters hiccup current limiting and both MOSFETs are turned off. There is a 1 ms cool-off period before the MOSFETs are allowed to be turned on. If the regulator has another hiccup event before it reaches the Power Good threshold on restart, it will again turn off both MOSFETs and wait for 1 ms. If this happens more than three times in a row, then the part will enter the Latch-Off state, which will permanently turn off both MOSFETs until the part is reset by toggling the EN pin, recycling power or via an I^2C command.

During a hiccup event, the HICCUP bit in the STATUS Register will go high and the SSD bit will go low until the output has recovered. The Power Good FAULT register bit, PG, will also go low and the PG pin will be pulled low.

In latch-off, the LATCH_OFF status bit is set to '1'.

The high-side current limit can be programmed by setting the ILIM[1:0] bits in the CTRL1 register. For maximum efficiency and current limit precision, the highest current limit must be programmed together with a higher TON setting (corresponding to a lower frequency).

4.16 Thermal Considerations

Although the MIC33M656 is capable of delivering up to 6A under load, the package thermal resistance and the device internal power dissipation may dictate some limitations to the continuous output current.

As a reference, for V_{IN} = 5V, V_{OUT} = 1V, I_{OUT} = 5A, the DT100108 Evaluation Board application shows a stable +40°C chip self-heating.

For V_{IN} = 5V, V_{OUT} = 3.3V, the same self-heating is produced at about 4A.

If operated above the rated junction temperature, electrical parameters may drift beyond characterized specifications. The MIC33M656 is protected under all circumstances by thermal shutdown.

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5.0 APPLICATION INFORMATION

5.1 Power-up State

When power is first applied to the MIC33M656 and the Enable pin is high, all I^2C registers are loaded with their default values and the device starts delivering power to the output based on those default values. After the soft start ramp has finished, these registers can be reconfigured. These new settings are saved, even if the Enable pin is pulled low. When the Enable pin is pulled high again, the MIC33M656 is configured to the new register settings, not the original default settings. To set the I^2C registers to their original settings, the input power has to be recycled.

When power is first applied to the MIC33M656 and the Enable pin is low, all I^2C registers can be configured. When the Enable pin is pulled high, the regulator will power up with the new I^2C register settings. Again, these register settings will not be lost when the Enable pin is pulled low. If power is recycled, the register settings are lost and they will have to be reprogrammed.

5.2 Output Voltage Sensing

To achieve accurate output voltage regulation, the V_{OUT} pin (internal feedback divider top terminal) should be Kelvin connected as close as possible to the point of regulation top terminal. Since both the internal reference and the internal feedback divider's bottom terminal refer to A_{GND}, it is important to minimize voltage drops between A_{GND} and the point of regulation return terminal (typically, the ground terminal of the output capacitor which is closest to the load).

5.3 Digital Voltage Control (DVC)

When the buck converter is programmed to a lower voltage, the regulator is placed into forced PWM mode and the Power Good monitor is blanked during the transition time.

5.4 Output Capacitor Selection

The MIC33M656 utilizes an internal compensation network and is designed to provide stable operation, with output capacitors from 47 µF to 1000 µF. This greatly simplifies the design, where supplementary output capacitance can be added without affecting stability.

The type of output capacitor is usually determined by its Equivalent Series Resistance (ESR). Voltage and RMS current capability are two other important factors to consider when selecting the output capacitor. Recommended capacitor types are ceramic, OS-CON and POSCAP. The output capacitor ESR is usually the main cause of the output ripple. The output capacitor ESR also affects the control loop from a stability point of view. The maximum value of ESR is calculated using Equation 5-1.

EQUATION 5-1:

$$ESR_{COUT} \leq \frac{\Delta V_{OUT(PP)}}{\Delta I_{L(PP)}}$$

Where:

$\Delta V_{OUT(PP)}$ = Peak-to-Peak Output Voltage Ripple

$\Delta I_{L(PP)}$ = Peak-to-Peak Inductor Current Ripple

The peak-to-peak inductor current ripple can be calculated by using the formula in Equation 5-3.

EQUATION 5-2:

$$\Delta I_{L(PP)} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times L}$$

Where:

L = 0.47 µH

The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated in Equation 5-3.

EQUATION 5-3:

$$\Delta V_{OUT(PP)} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{C_{OUT} \times f_{SW} \times 8}\right)^2 + \left(\Delta I_{L(PP)} \times ESR_{COUT}\right)^2}$$

Where:

C_{OUT} = Output Capacitance Value

f_{SW} = Switching Frequency

The output capacitor RMS current is calculated in Equation 5-4.

EQUATION 5-4:

$$I_{COUT(RMS)} = \frac{\Delta I_{L(PP)}}{\sqrt{12}}$$

The power dissipated in the output capacitor is:

EQUATION 5-5:

$$P_{DISS(COUT)} = I_{COUT(RMS)}^2 \times ESR_{COUT}$$

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5.5 Input Capacitor Selection

The MIC33M656 integrates high-frequency input bypass capacitors connected between PV_{IN} and P_{GND}, and an additional 10 µF, low-ESR ceramic capacitor for input ripple smoothing, connected between P_{GND} and AUX_PV_{IN}. Therefore, the connection between PV_{IN} and AUX_PV_{IN} should have very low stray resistance and inductance (i.e., many vias) to take advantage of the internal 10 µF capacitor. While the internal 10 µF capacitor can support the RMS ripple current, additional external input ceramic capacitors can be added optionally to further attenuate the input voltage ripple amplitude. The need for additional external input capacitance also depends on the impedance of the input supply distribution network.

5.6 I²C Bus Pull-ups Selection

The optimal pull-up resistors must be strong enough such that the RC constant of the bus is not too large (causing the line not to rise to a logical high before being pulled low), but weak enough for the IC to drive the line low (see Table 5-1).

TABLE 5-1: I²C BUS CONSTRAINTS

	Standard Mode	Fast Mode	High-Speed Mode	
Bit Rate (kbits/s)	0 to 100	0 to 400	0 to 1700	0 to 3400
Max Cap Load (pF)	400	400	400	100
Rise Time (ns)	1000	300	160	80
Spike Filtered (ns)	N/A	50	10	

EQUATION 5-6:

$$Rp(min) = \frac{V_{CC} - V_{OL}(max)}{I_{OL}}$$

Where:

V_{CC} = Pull-up Reference Voltage (i.e., V_{IN})
$V_{OL}(max)$ = 0.4V
I_{OL} = 3 mA

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6.0 I²C INTERFACE DESCRIPTION

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are: a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy. MIC33M656 is a slave only device (i.e., it cannot generate a SCL signal and does not have SCL clock stretching capability). Every data transfer, to and from the MIC33M656, must be initiated by a master device which drives the SCL line.

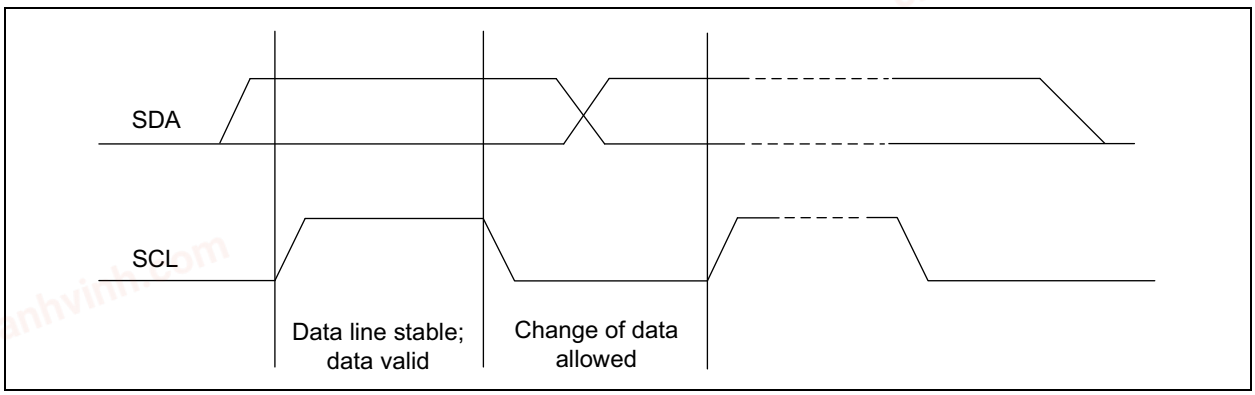


FIGURE 6-1: *Bit Transfer Diagram.*

6.1 Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse as changes in the data line, at this time, will be interpreted as control signals.

6.2 Start and Stop Conditions

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line, while the clock is high, is defined as the Start (S) or Repeated Start (Sr) condition. A low-to-high transition of the data line while the clock is high is defined as the Stop condition (P). Start and Stop conditions are always generated by the master. The bus is considered to be busy after the Start condition. The bus is considered to be free again a certain time after the Stop condition. The bus stays busy if a Repeated Start (Sr) is generated instead of a Stop condition.

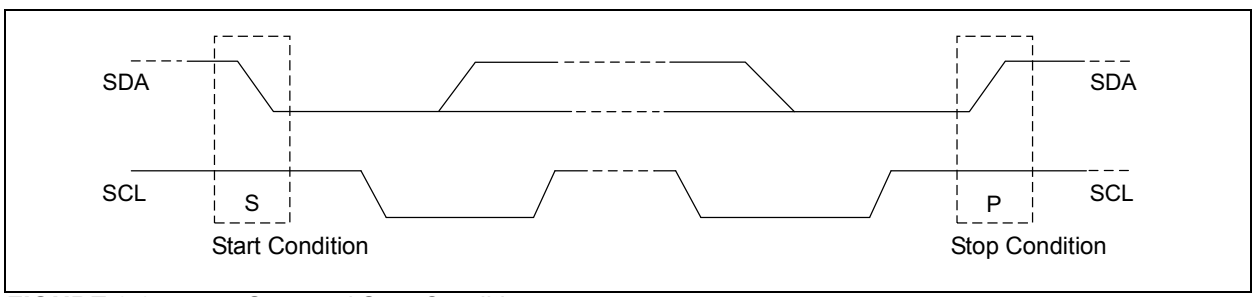


FIGURE 6-2: *Start and Stop Conditions.*

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6.3 Device Address

The MIC33M656 device uses a fixed 7-bit address, which is set in hardware. This address is ‘0x5B’.

6.4 Acknowledge

The number of data bytes transferred between the Start and the Stop conditions, from transmitter to receiver, is not limited. Each byte of eight bits is followed by one Acknowledge bit. The Acknowledge bit is a high level put on the bus by the transmitter, whereas the master generates an extra Acknowledge related clock pulse. The device that Acknowledges has to pull down the SDA line during the Acknowledge clock pulse, so that the SDA line is stable low during the high period of the Acknowledge related clock pulse; setup and hold times must be taken into account.

A slave receiver, which is addressed, must generate an Acknowledge after the reception of each byte.

Also, a master receiver must generate an Acknowledge after the reception of each byte that has been clocked out of the slave transmitter, except on the last received byte. A master receiver must signal an end of data to the transmitter by not generating an Acknowledge on the last byte that has been clocked out of the slave transmitter. In this event, the transmitter must leave the data line high to enable the master to generate a Stop condition.

6.5 Bus Transactions

6.5.1 SINGLE WRITE

The first seven bits of the first byte make up the slave address. The eighth bit is the LSb (Least Significant bit). It determines the direction of the message (R/W). A ‘0’ in the least significant position of the first byte means that the master will write information to a selected slave. A ‘1’ in this position means that the master will read information from the slave. When an address is sent, each device in a system compares the first seven bits after the Start condition with its address. If they match, the device considers itself addressed by the master as a slave-receiver or slave-transmitter, depending on the R/W bit.

A command byte is a data byte which selects a register on the device. The Least Significant six bits of the command byte determine the address of the register that needs to be written.

The data to port are the 8-bit data that need to be written to the selected register. This is followed by the Acknowledge from the slave and then the Stop condition.

The Write command is as follows and it is illustrated in the timing diagram shown in Figure 6-3:

1. Send Start sequence.
2. Send 7-bit slave address.
3. Send the R/W bit – ‘0’ to indicate a write operation.
4. Wait for Acknowledge from the slave.
5. Send the command byte containing the address that needs to be written.
6. Wait for Acknowledge from the slave.
7. Receive the 8-bit data from the master and write them to the slave register, indicated in Step 5, starting from the MSB.
8. Acknowledge from the slave.
9. Send Stop sequence.

Note: Writing to a non-existing register location will have no effect.

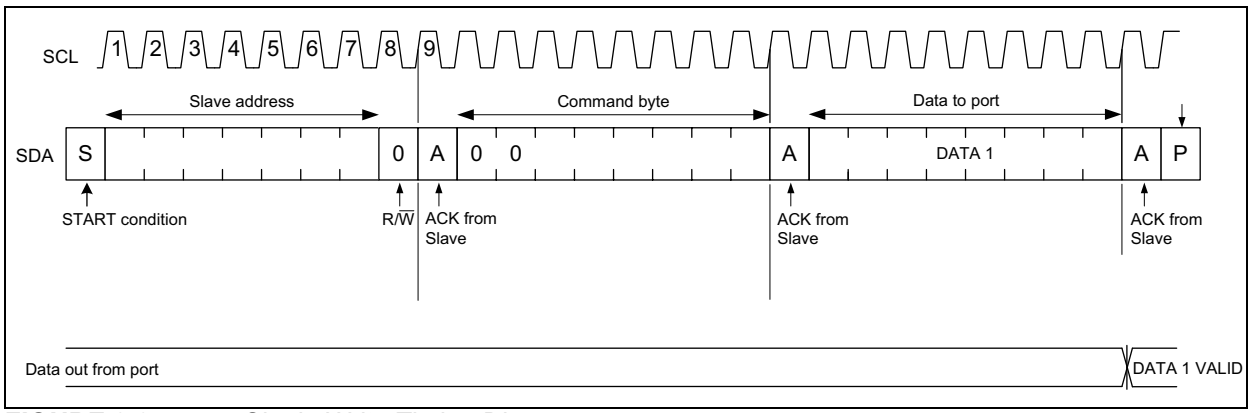


FIGURE 6-3: *Single Write Timing Diagram.*

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6.5.2 SINGLE READ

This reads a single byte from a device, from a designated register. The register is specified through the command byte.

The Read command is as follows and it is illustrated in the timing diagram of Figure 6-4 below.

1. Send Start sequence.
2. Send 7-bit slave address.
3. Send the R/W bit – '0' to indicate a write operation.
4. Wait for Acknowledge from the slave.
5. Send the register address that needs to be read.
6. Wait for Acknowledge from the slave.
7. Send Start sequence again (Repeated Start condition).
8. Send the 7-bit slave address.
9. Send R/W bit – '1' to indicate a read operation.
10. Wait for Acknowledge from the slave.
11. Receive the 8-bit data from the slave starting from MSB.
12. Acknowledge from the master. On the received byte, the master receiver issues a NACK in place of an ACK to signal the end of the data transfer.
13. Send Stop sequence.

Note: Attempts to read from a non-existing register location will return all zeros.

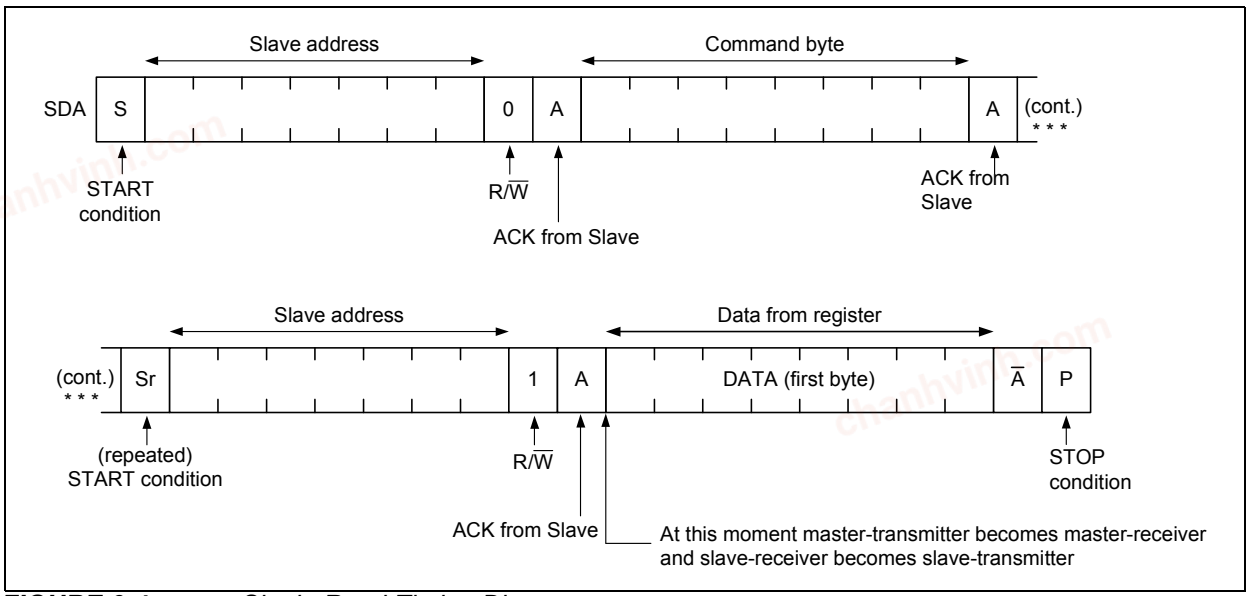


FIGURE 6-4: *Single Read Timing Diagram.*

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NOTES:

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7.0 REGISTER MAP AND I²C PROGRAMMABILITY

The MIC33M656 internal registers are summarized in the MIC33M656 Register Map.

TABLE 7-1: MIC33M656 REGISTER MAP

Address	Register Name							
0x00	Control Register (CTRL1)							
	TON[1:0]		ILIM[1:0]		EN_DELAY[1:0]		EN_INT	EN_CON
0x01	Output Control Register (CTRL2)							
	DIS_100PCT	FPWM	OT_LATCH	PULL_DN	SLEW_RATE[3:0]			
0x02	Output Voltage Register (VOUT)							
	VO[7:0]							
0x03	Status and Fault Register (FAULT)							
	OT_WARN	EN_STAT	BOOT_ERR	SSD	HICCUP	OT	LATCH_OFF	PG

REGISTER 7-1: CTRL1: CONTROL REGISTER (ADDRESS 0x00)

R/W-V	R/W-V	R/W-V	R/W-V	R/W-0	R/W-0	R/W-0	R/W-0
TON[1:0]		ILIM[1:0]		EN_DELAY[1:0]		EN_INT	EN_CON
bit 7							bit 0

Legend:	V = Factory programmed POR value		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **TON[1:0]:** On Time
00 = Low frequency
01 = Medium frequency
10 = High frequency
11 = Very high frequency

bit 5-4 **ILIM[1:0]:** High-Side Peak Current Limit
00 = 3.5A
01 = 5A
10 = 8.5A
11 = 10A

bit 3-2 **EN_DELAY[1:0]:** Enable Delay
00 = 250 µs
01 = 1 ms
10 = 2 ms
11 = 3 ms

bit 1 **EN_INT:** Enable Bit Register Control
0 = Register controlled
1 = Enable pin controlled

bit 0 **EN_CON:** Enable Control
0 = Off
1 = On

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REGISTER 7-2: CTRL2: OUTPUT CONTROL REGISTER (ADDRESS 0x01)

R/W-0	R/W-0	R/W-V	R/W-V	R/W-V	R/W-V	R/W-V	R/W-V
DIS_100PCT	FPWM	OT_LATCH	PULLDN	SLEW_RATE[3:0]			
bit 7							bit 0

Legend:	V = Factory programmed POR value		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **DIS_100PCT:** Disable 100% Duty Cycle
0 = 100% DC
1 = Disable 100% DC

bit 6 **FPWM:** Force PWM
0 = HLL
1 = FPWM

bit 5 **OT_LATCH:** Overtemperature Latch
0 = Latch off immediately
1 = Latch off after four OT cycles

bit 4 **PULLDN:** Enable/Disable Regulator Pull-Down when Power-Down
0 = No pull-down
1 = Pull-down

bit 3-0 **SLEW_RATE[3:0]:** Step Slew Rate Time in µs/V
0000 = 200
0001 = 400
0010 = 600
0011 = 800
0100 = 1000
0101 = 1200
0110 = 1400
0111 = 1600
1000 = 1800
1001 = 2000
1010 = 2200
1011 = 2400
1100 = 2600
1101 = 2800
1110 = 3000
1111 = 3200

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REGISTER 7-3: VOUT: OUTPUT VOLTAGE CONTROL REGISTER (ADDRESS 0x02)

R/W-V	R/W-V	R/W-V	R/W-V	R/W-V	R/W-V	R/W-V	R/W-V
VO[7:0]							
bit 7							bit 0

Legend:	V = Factory programmed POR value		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **VO[7:0]:** Output Voltage Control (HAYMP, FAYMP options)
For codes 0x00 to 0x76: 0.6V.

	0x80 = 0.645	0xA0 = 0.805V	0xC0 = 0.965	0xE0 = 1.125V
	0x81 = 0.65V	0xA1 = 0.81V	0xC1 = 0.97V	0xE1 = 1.13V
	0x82 = 0.655V	0xA2 = 0.815V	0xC2 = 0.975V	0xE2 = 1.135V
	0x83 = 0.66V	0xA3 = 0.82V	0xC3 = 0.98V	0xE3 = 1.14V
	0x84 = 0.665V	0xA4 = 0.825V	0xC4 = 0.985V	0xE4 = 1.145V
	0x85 = 0.67V	0xA5 = 0.83V	0xC5 = 0.99V	0xE5 = 1.15V
	0x86 = 0.675V	0xA6 = 0.835V	0xC6 = 0.995V	0xE6 = 1.155V
	0x87 = 0.68V	0xA7 = 0.84V	0xC7 = 1V	0xE7 = 1.16V
	0x88 = 0.685V	0xA8 = 0.845V	0xC8 = 1.005V	0xE8 = 1.165V
	0x89 = 0.69V	0xA9 = 0.85V	0xC9 = 1.01V	0xE9 = 1.17V
	0x8A = 0.695V	0xAA = 0.855V	0xCA = 1.015V	0xEA = 1.175V
	0x8B = 0.7V	0xAB = 0.86V	0xCB = 1.02V	0xEB = 1.18V
	0x8C = 0.705V	0xAC = 0.865V	0xCC = 1.025V	0xEC = 1.185V
	0x8D = 0.71V	0xAD = 0.87V	0xCD = 1.03V	0xED = 1.19V
	0x8E = 0.715V	0xAE = 0.875V	0xCE = 1.035V	0xEE = 1.195V
	0x8F = 0.72V	0xAF = 0.88V	0xCF = 1.04V	0xEF = 1.2V
	0x90 = 0.725V	0xB0 = 0.885V	0xD0 = 1.045V	0xF0 = 1.205V
	0x91 = 0.73V	0xB1 = 0.89V	0xD1 = 1.05V	0xF1 = 1.21V
	0x92 = 0.735V	0xB2 = 0.895V	0xD2 = 1.055V	0xF2 = 1.215V
	0x93 = 0.74V	0xB3 = 0.9V	0xD3 = 1.06V	0xF3 = 1.22V
	0x94 = 0.745V	0xB4 = 0.905V	0xD4 = 1.065V	0xF4 = 1.225V
	0x95 = 0.75V	0xB5 = 0.91V	0xD5 = 1.07V	0xF5 = 1.23V
	0x96 = 0.755V	0xB6 = 0.915V	0xD6 = 1.075V	0xF6 = 1.235V
0x77 = 0.6V	0x97 = 0.76V	0xB7 = 0.92V	0xD7 = 1.08V	0xF7 = 1.24V
0x78 = 0.605V	0x98 = 0.765V	0xB8 = 0.925V	0xD8 = 1.085V	0xF8 = 1.245V
0x79 = 0.61V	0x99 = 0.77V	0xB9 = 0.93V	0xD9 = 1.09V	0xF9 = 1.25V
0x7A = 0.615V	0x9A = 0.775V	0xBA = 0.935V	0xDA = 1.095V	0xFA = 1.255V
0x7B = 0.62V	0x9B = 0.78V	0xBB = 0.94V	0xDB = 1.1V	0xFB = 1.26V
0x7C = 0.625V	0x9C = 0.785V	0xBC = 0.945V	0xDC = 1.105V	0xFC = 1.265V
0x7D = 0.63V	0x9D = 0.79V	0xBD = 0.95V	0xDD = 1.11V	0xFD = 1.27V
0x7E = 0.635V	0x9E = 0.795V	0xBE = 0.955V	0xDE = 1.115V	0xFE = 1.275V
0x7F = 0.64V	0x9F = 0.8V	0xBF = 0.96V	0xDF = 1.12V	0xFF = 1.28V

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REGISTER 7-3: VOUT: OUTPUT VOLTAGE CONTROL REGISTER (ADDRESS 0x02) (CONTINUED)

bit 7-0 **VO[7:0]:** Output Voltage Control (SAYMP option)
For codes 0x00 to 0x3B: 0.6V.

	0x40 = 0.65V	0x60 = 0.97V	0x80 = 1.3V	0xA0 = 1.94V	0xC0 = 2.58V	0xE0 = 3.22V
	0x41 = 0.66V	0x61 = 0.98V	0x81 = 1.32V	0xA1 = 1.96V	0xC1 = 2.6V	0xE1 = 3.24V
	0x42 = 0.67V	0x62 = 0.99V	0x82 = 1.34V	0xA2 = 1.98V	0xC2 = 2.62V	0xE2 = 3.26V
	0x43 = 0.68V	0x63 = 1V	0x83 = 1.36V	0xA3 = 2V	0xC3 = 2.64V	0xE3 = 3.28V
	0x44 = 0.69V	0x64 = 1.01V	0x84 = 1.38V	0xA4 = 2.02V	0xC4 = 2.66V	0xE4 = 3.3V
	0x45 = 0.7V	0x65 = 1.02V	0x85 = 1.4V	0xA5 = 2.04V	0xC5 = 2.68V	0xE5 = 3.32V
	0x46 = 0.71V	0x66 = 1.03V	0x86 = 1.42V	0xA6 = 2.06V	0xC6 = 2.7V	0xE6 = 3.34V
	0x47 = 0.72V	0x67 = 1.04V	0x87 = 1.44V	0xA7 = 2.08V	0xC7 = 2.72V	0xE7 = 3.36V
	0x48 = 0.73V	0x68 = 1.05V	0x88 = 1.46V	0xA8 = 2.1V	0xC8 = 2.74V	0xE8 = 3.38V
	0x49 = 0.74V	0x69 = 1.06V	0x89 = 1.48V	0xA9 = 2.12V	0xC9 = 2.76V	0xE9 = 3.4V
	0x4A = 0.75V	0x6A = 1.07V	0x8A = 1.5V	0xAA = 2.14V	0xCA = 2.78V	0xEA = 3.42V
	0x4B = 0.76V	0x6B = 1.08V	0x8B = 1.52V	0xAB = 2.16V	0xCB = 2.8V	0xEB = 3.44V
	0x4C = 0.77V	0x6C = 1.09V	0x8C = 1.54V	0xAC = 2.18V	0xCC = 2.82V	0xEC = 3.46V
	0x4D = 0.78V	0x6D = 1.1V	0x8D = 1.56V	0xAD = 2.2V	0xCD = 2.84V	0xED = 3.48V
	0x4E = 0.79V	0x6E = 1.11V	0x8E = 1.58V	0xAE = 2.22V	0xCE = 2.86V	0xEE = 3.5V
	0x4F = 0.8V	0x6F = 1.12V	0x8F = 1.6V	0xAF = 2.24V	0xCF = 2.88V	0xEF = 3.52V
	0x50 = 0.81V	0x70 = 1.13V	0x90 = 1.62V	0xB0 = 2.26V	0xD0 = 2.9V	0xF0 = 3.54V
	0x51 = 0.82V	0x71 = 1.14V	0x91 = 1.64V	0xB1 = 2.28V	0xD1 = 2.92V	0xF1 = 3.56V
	0x52 = 0.83V	0x72 = 1.15V	0x92 = 1.66V	0xB2 = 2.3V	0xD2 = 2.94V	0xF2 = 3.58V
	0x53 = 0.84V	0x73 = 1.16V	0x93 = 1.68V	0xB3 = 2.32V	0xD3 = 2.96V	0xF3 = 3.6V
	0x54 = 0.85V	0x74 = 1.17V	0x94 = 1.7V	0xB4 = 2.34V	0xD4 = 2.98V	0xF4 = 3.62V
	0x55 = 0.86V	0x75 = 1.18V	0x95 = 1.72V	0xB5 = 2.36V	0xD5 = 3V	0xF5 = 3.64V
	0x56 = 0.87V	0x76 = 1.19V	0x96 = 1.74V	0xB6 = 2.38V	0xD6 = 3.02V	0xF6 = 3.66V
	0x57 = 0.88V	0x77 = 1.2V	0x97 = 1.76V	0xB7 = 2.4V	0xD7 = 3.04V	0xF7 = 3.68V
	0x58 = 0.89V	0x78 = 1.21V	0x98 = 1.78V	0xB8 = 2.42V	0xD8 = 3.06V	0xF8 = 3.7V
	0x59 = 0.9V	0x79 = 1.22V	0x99 = 1.8V	0xB9 = 2.44V	0xD9 = 3.08V	0xF9 = 3.72V
	0x5A = 0.91V	0x7A = 1.23V	0x9A = 1.82V	0xBA = 2.46V	0xDA = 3.1V	0xFA = 3.74V
0x3B = 0.6V	0x5B = 0.92V	0x7B = 1.24V	0x9B = 1.84V	0xBB = 2.48V	0xDB = 3.12V	0xFB = 3.76V
0x3C = 0.61V	0x5C = 0.93V	0x7C = 1.25V	0x9C = 1.86V	0xBC = 2.5V	0xDC = 3.14V	0xFC = 3.78V
0x3D = 0.62V	0x5D = 0.94V	0x7D = 1.26V	0x9D = 1.88V	0xBD = 2.52V	0xDD = 3.16V	0xFD = 3.8V
0x3E = 0.63V	0x5E = 0.95V	0x7E = 1.27V	0x9E = 1.9V	0xBE = 2.54V	0xDE = 3.18V	0xFE = 3.82V
0x3F = 0.64V	0x5F = 0.96V	0x7F = 1.28V	0x9F = 1.92V	0xBF = 2.56V	0xDF = 3.2V	0xFF = 3.84V

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REGISTER 7-4: FAULT: STATUS AND FAULT REGISTER (ADDRESS 0x03)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
OT_WARN	EN_STAT	BOOT_ERR	SSD	HICCUP	OT	LATCH_OFF	PG
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **OT_WARN:** Overtemperature Warning
0 = No Fault
1 = Fault

bit 6 **EN_STAT:** Buck On/Off Control
0 = Off
1 = On

bit 5 **BOOT_ERR:** Boot-up Error
0 = No Fault
1 = Fault

bit 4 **SSD:** Soft Start Done
0 = Ramp not done
1 = Ramp done

bit 3 **HICCUP:** Current Limit Hiccup
0 = Not in Hiccup mode
1 = In Hiccup mode

bit 2 **OT:** Overtemperature
0 = No Fault
1 = Fault

bit 1 **LATCH_OFF:** Overcurrent or Overtemperature Fault Latch-Off
0 = No Fault
1 = Fault (device is latched off)

bit 0 **PG:** Power Good
0 = Power not good
1 = Power good

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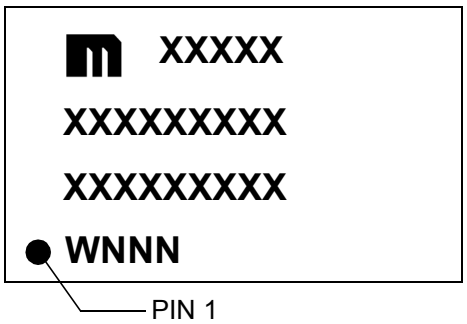
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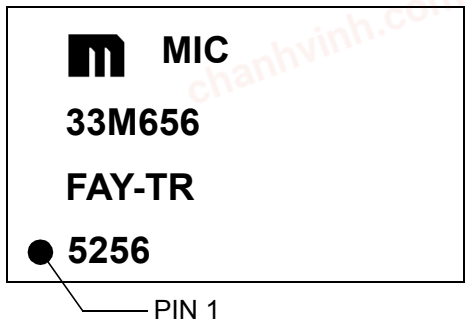
8.0 PACKAGING INFORMATION

8.1 Package Marking Information

53-Lead B1QFN



Example



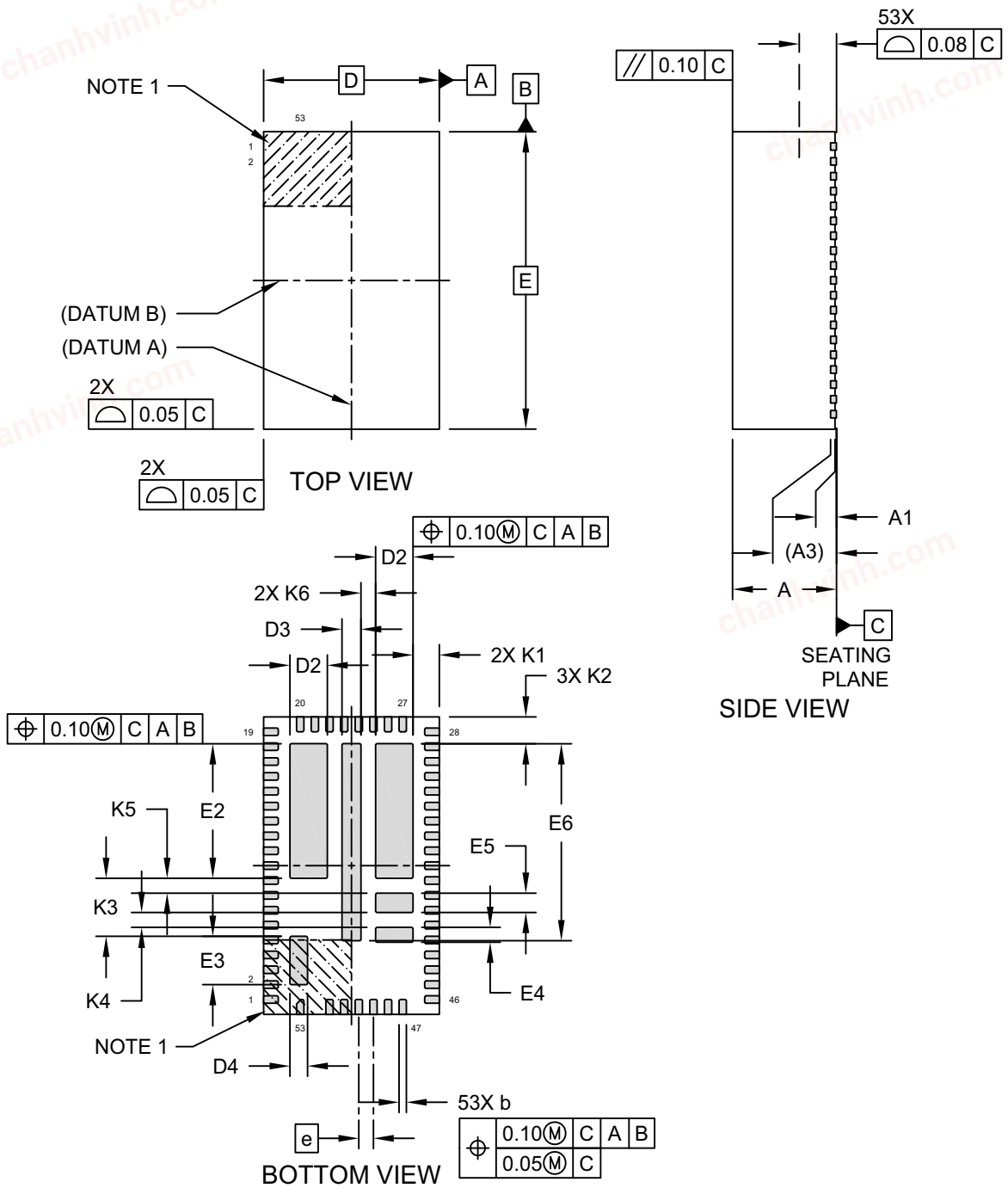
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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53-Lead Very Thick Plastic Quad Flat, No Lead Package (QDA) - 6x10x3.05 mm Body [B1QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



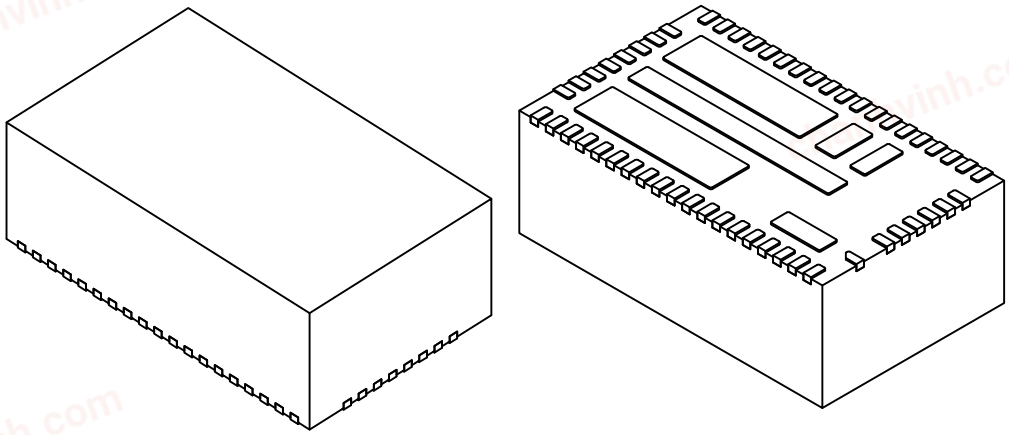
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53-Lead Very Thick Plastic Quad Flat, No Lead Package (QDA) - 6x10x3.05 mm Body [B1QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		53	
Pitch	e		0.50 BSC	
Overall Height	A	2.95	3.00	3.05
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	1.225	1.275	1.325
Exposed Pad Length	D3	0.60	0.65	0.70
Exposed Pad Length	D4	0.55	0.60	0.65
Overall Width	E		10.00 BSC	
Exposed Pad Width	E2	4.475	4.525	4.575
Exposed Pad Width	E3	1.575	1.625	1.675
Exposed Pad Width	E4	0.45	0.50	0.55
Exposed Pad Width	E5	0.60	0.65	0.70
Exposed Pad Width	E6	6.573	6.623	6.673
Package Edge to Exposed Pad	K1	0.85	0.90	0.95
Package Edge to Exposed Pad	K2	0.85	0.90	0.95
Exposed Pad to Exposed Pad	K3	1.90	1.95	2.00
Exposed Pad to Exposed Pad	K4	0.45	0.50	0.55
Exposed Pad to Exposed Pad	K5	0.45	0.50	0.55
Exposed Pad to Exposed Pad	K6	0.45	0.50	0.55
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.45	0.50	0.55

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

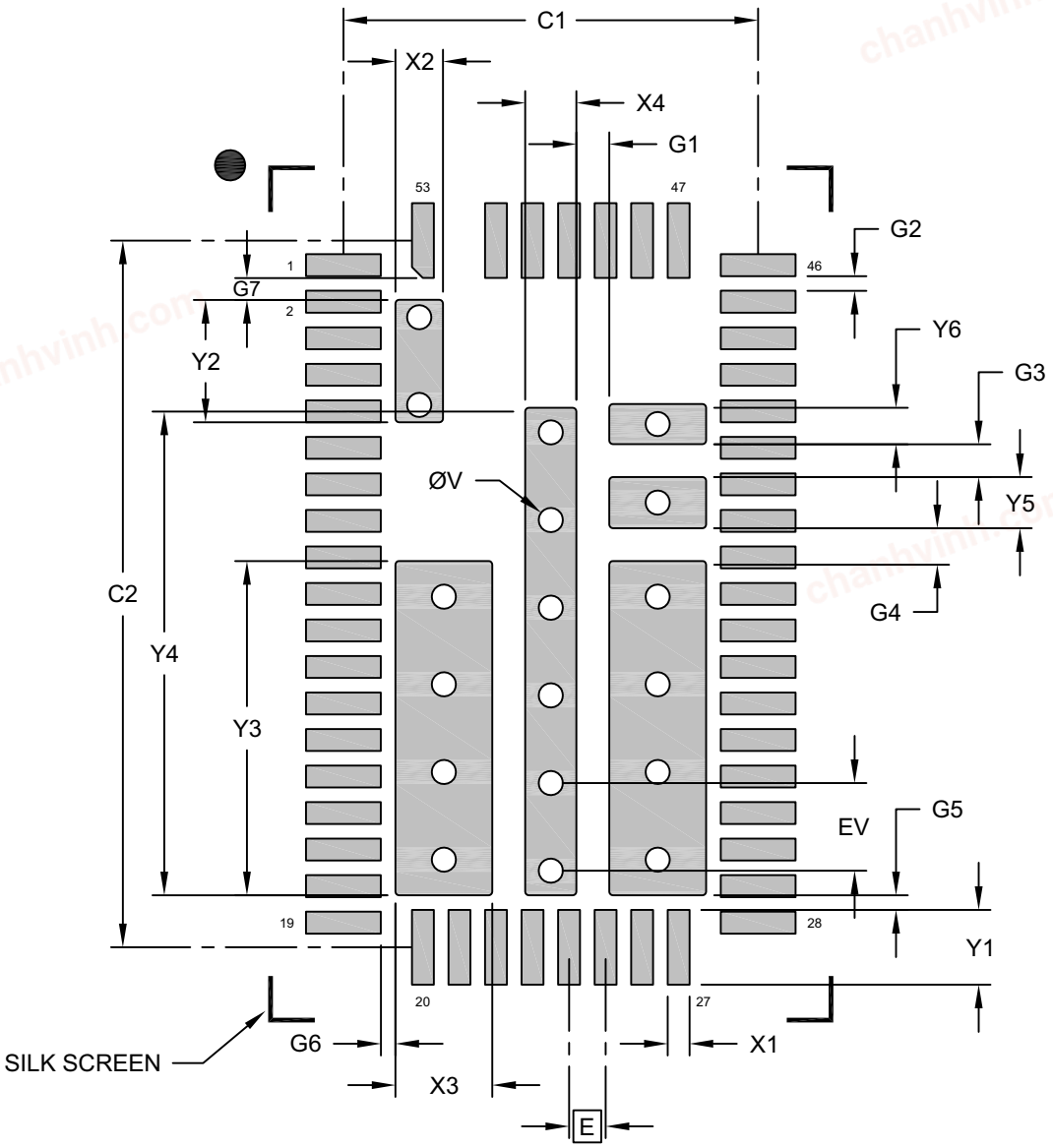
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53-Lead Very Thick Plastic Quad Flat, No Lead Package (QDA) - 6x10x3.05 mm Body [B1QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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53-Lead Very Thick Plastic Quad Flat, No Lead Package (QDA) - 6x10x3.05 mm Body [B1QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		5.68	
Contact Pad Spacing	C2		9.68	
Contact Pad Width (X53)	X1			0.30
Contact Pad Length (X53)	Y1			1.02
Center Pad Width	X2			0.65
Center Pad Length	Y2			1.68
Center Pad Width (X4)	X3			1.33
Center Pad Length (X2)	Y3			4.58
Center Pad Width	X4			0.70
Center Pad Length	Y4			6.62
Center Pad Length	Y5			0.70
Center Pad Length	Y6			0.55
Contact Pad to Center Pad (X2)	G1	0.45		
Contact Pad to Contact Pad (X48)	G2	0.20		
Contact Pad to Center Pad	G3	0.45		
Contact Pad to Center Pad	G4	0.45		
Contact Pad to Center Pad	G5	0.20		
Contact Pad to Center Pad	G6	0.20		
Contact Pad to Center Pad	G7	0.30		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch (X12)	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process
3. Thermal vias are centered within each exposed pad.

Microchip Technology Drawing C04-3272 Rev B Sheet 2 of 2

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APPENDIX A: REVISION HISTORY

Revision A (September 2019)

- Initial release of this Data Sheet.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX	XX
Device	Temperature Range	Package	Tape and Reel Option

Device:	MIC33M656: 6A, Power Module Buck Converter with HyperLight Load® and I²C Interface
Output Voltage Option:	FA = 0.9V HA = 1.0V SA = 1.0V, with 10 mV or 20 mV resolution
Junction Temperature Range:	Y = -40°C to +125°C
Package:	MP = 53 Lead 6 mm x 10 mm x 3 mm Very Thick Plastic Quad Flat, No Lead (B1QFN)
Tape and Reel Option:	TR = Tape and Reel(1)

Examples:

a) MIC33M656-FAYMP-TR: 0.9V Output, -40°C to +125°C Temperature Range, 53-Lead B1QFN Package, Tape and Reel

b) MIC33M656-HAYMP-TR: 1.0V Output, -40°C to +125°C Temperature Range, 53-Lead B1QFN Package, Tape and Reel

c) MIC33M656-SAYMP-TR: 1.0V Output, -40°C to +125°C Temperature Range, 53-Lead B1QFN Package, Tape and Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with Microchip for package availability with the Tape and Reel option.

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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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