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MCP7940M

Low-Cost I²C™ Real-Time Clock/Calendar with SRAM

Timekeeping Features:

- Real-Time Clock/Calendar (RTCC):
  - Hours, Minutes, Seconds, Day of Week, Day, Month, Year
  - Leap year compensated to 2399
  - 12/24 hour modes
- Oscillator for 32.768 kHz Crystals:
  - Optimized for 6-9 pF crystals
- On-Chip Digital Trimming/Calibration:
  - ±1 PPM resolution
  - ±129 PPM range
- Dual Programmable Alarms
- Versatile Output Pin:
  - Clock output with selectable frequency
  - Alarm output
  - General purpose output

Low-Power Features:

- Wide Voltage Range:
  - Operating voltage range of 1.8V to 5.5V
- Low Typical Timekeeping Current:
  - Operating from VCC: 1.2 µA at 3.3V

User Memory:

- 64-byte SRAM

Operating Ranges:

- 2-Wire Serial Interface, I²C™ Compatible
  - I²C clock rate up to 400 kHz
- Temperature Range:
  - Industrial (I): -40°C to +85°C

Packages:

- 8-Lead SOIC, MSOP, TSSOP, PDIP and 2x3 TDFN

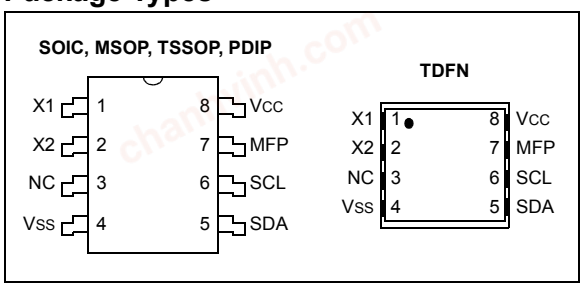
General Description:

The MCP7940M Real-Time Clock/Calendar (RTCC) tracks time using internal counters for hours, minutes, seconds, days, months, years, and day of week. Alarms can be configured on all counters up to and including months. For usage and configuration, the MCP7940M supports I²C communications up to 400 kHz.

The open-drain, multi-functional output can be configured to assert on an alarm match, to output a selectable frequency square wave, or as a general purpose output.

The MCP7940M is designed to operate using a 32.768 kHz tuning fork crystal with external crystal load capacitors. On-chip digital trimming can be used to adjust for frequency variance caused by crystal tolerance and temperature.

Package Types



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FIGURE 1-1: TYPICAL APPLICATION SCHEMATIC

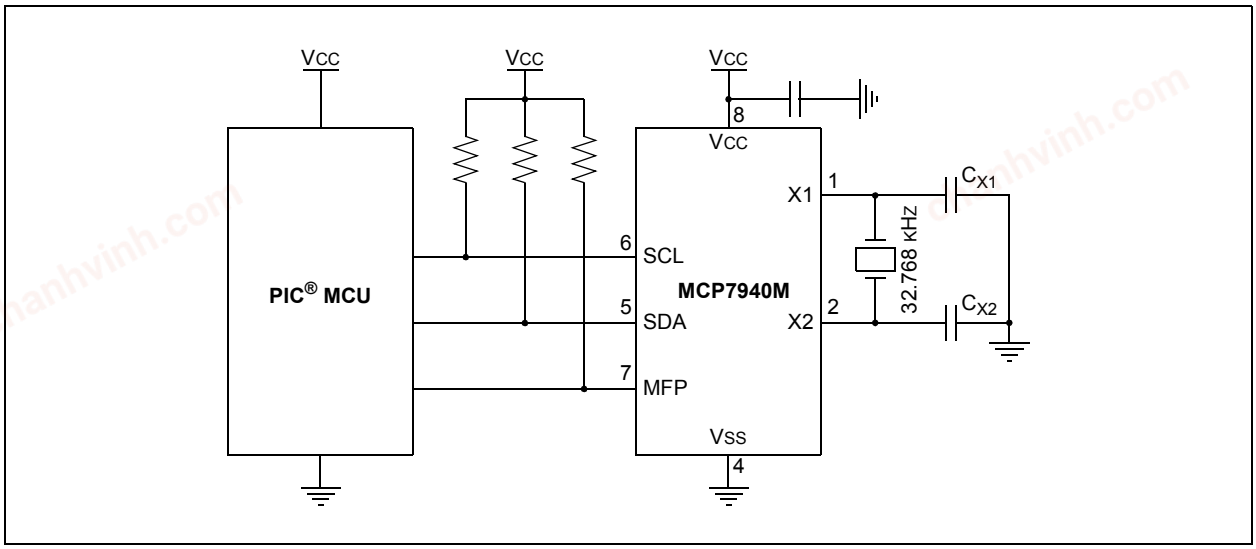
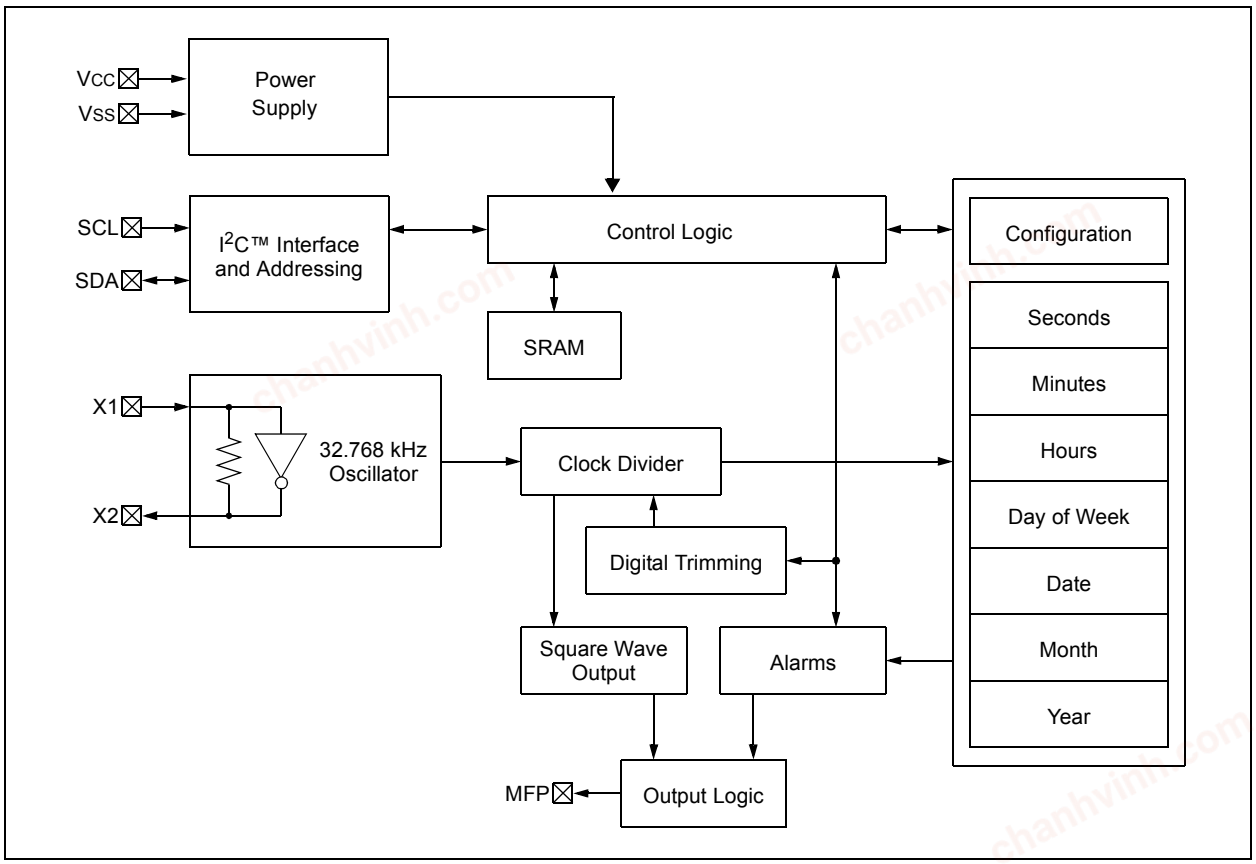


FIGURE 1-2: BLOCK DIAGRAM



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

VCC.....6.5V

All inputs and outputs (except SDA and SCL) w.r.t. VSS.....-0.6V to VCC +1.0V

SDA and SCL w.r.t. VSS.....-0.6V to 6.5V

Storage temperature.....-65°C to +150°C

Ambient temperature with power applied.....-40°C to +125°C

ESD protection on all pins.....≥ 4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = +1.8V to 5.5V TA = -40°C to +85°C				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
D1	VIH	High-level input voltage	0.7 VCC	—	—	V	—
D2	VIL	Low-level input voltage	—	—	0.3 VCC 0.2 VCC	V V	VCC ≥ 2.5V VCC < 2.5V
D3	VHYS	Hysteresis of Schmitt Trigger inputs (SDA, SCL pins)	0.05 VCC	—	—	V	(Note 1)
D4	VOL	Low-level output voltage (MFP, SDA pins)	—	—	0.40	V	IOL = 3.0 mA @ VCC = 4.5V IOL = 2.1 mA @ VCC = 2.5V
D5	ILI	Input leakage current	—	—	±1	µA	VIN = VSS or VCC
D6	ILO	Output leakage current	—	—	±1	µA	VOUT = VSS or VCC
D7	CIN, COUT	Pin capacitance (SDA, SCL, MFP pins)	—	—	10	pF	VCC = 5.0V (Note 1) TA = 25°C, f = 1 MHz
D8	COSC	Oscillator pin capacitance (X1, X2 pins)	—	3	—	pF	(Note 1)
D9	ICCREAD	SRAM/RTCC register operating current	—	—	300	µA	VCC = 5.5V, SCL = 400 kHz
	ICCWRITE		—	—	400	µA	VCC = 5.5V, SCL = 400 kHz
D10	ICCDAT	VCC data-retention current (oscillator off)	—	—	1	µA	SCL, SDA, VCC = 5.5V
D11	ICCT	Timekeeping current	—	1.2	—	µA	VCC = 3.3V (Note 1)

Note 1: This parameter is not tested but ensured by characterization.

2: Typical measurements taken at room temperature.

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TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = +1.8V to 5.5V TA = -40°C to +85°C				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
1	FCLK	Clock frequency	— —	— —	100 400	kHz	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V
2	THIGH	Clock high time	4000 600	— —	— —	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V
3	TLOW	Clock low time	4700 1300	— —	— —	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V
4	TR	SDA and SCL rise time (**Note 1**)	— —	— —	1000 300	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V
5	TF	SDA and SCL fall time (**Note 1**)	— —	— —	1000 300	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V
6	THD:STA	Start condition hold time	4000 600	— —	— —	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V
7	TSU:STA	Start condition setup time	4700 600	— —	— —	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V
8	THD:DAT	Data input hold time	0	—	—	ns	(**Note 2**)
9	TSU:DAT	Data input setup time	250 100	— —	— —	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V
10	TSU:STO	Stop condition setup time	4000 600	— —	— —	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V
11	TAA	Output valid from clock	— —	— —	3500 900	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V
12	TBUF	Bus free time: Time the bus must be free before a new transmission can start	4700 1300	— —	— —	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V
13	TSP	Input filter spike suppression (SDA and SCL pins)	—	—	50	ns	(**Note 1**)
14	FOSC	Oscillator frequency	—	32.768	—	kHz	—
15	TOSF	Oscillator timeout period	1	—	—	ms	(**Note 1**)

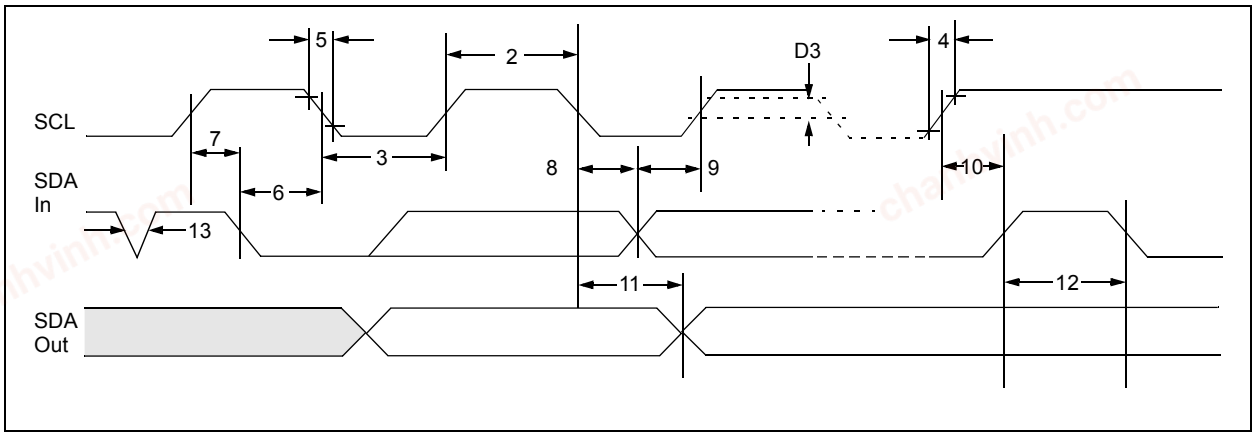
Note 1: Not 100% tested.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

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FIGURE 1-3: I²C BUS TIMING DATA



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2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	8-pin SOIC	8-pin MSOP	8-pin TSSOP	8-pin TDFN	8-pin PDIP	Function
X1	1	1	1	1	1	Quartz Crystal Input, External Oscillator Input
X2	2	2	2	2	2	Quartz Crystal Output
NC	3	3	3	3	3	Not Connected
Vss	4	4	4	4	4	Ground
SDA	5	5	5	5	5	Bidirectional Serial Data (I^2C™)
SCL	6	6	6	6	6	Serial Clock (I^2C)
MFP	7	7	7	7	7	Multifunction Pin
VCC	8	8	8	8	8	Primary Power Supply

Note: Exposed pad on TFDN can be connected to VSS or left floating.

2.1 Serial Data (SDA)

This is a bidirectional pin used to transfer addresses and data into and out of the device. It is an open-drain terminal. Therefore, the SDA bus requires a pull-up resistor to VCC (typically 10 kΩ for 100 kHz, 2 kΩ for 400 kHz). For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

2.2 Serial Clock (SCL)

This input is used to synchronize the data transfer to and from the device.

2.3 Oscillator Input/Output (X1, X2)

These pins are used as the connections for an external 32.768 kHz quartz crystal and load capacitors. X1 is the crystal oscillator input and X2 is the output. The MCP7940M is designed to allow for the use of external load capacitors in order to provide additional flexibility when choosing external crystals. The MCP7940M is optimized for crystals with a specified load capacitance of 6-9 pF.

X1 also serves as the external clock input when the MCP7940M is configured to use an external oscillator.

2.4 Multifunction Pin (MFP)

This is an output pin used for the alarm and square wave output functions. It can also serve as a general purpose output pin by controlling the OUT bit in the CONTROL register.

The MFP is an open-drain output and requires a pull-up resistor to VCC (typically 10 kΩ). This pin may be left floating if not used.

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3.0 I²C BUS CHARACTERISTICS

3.1 I²C Interface

The MCP7940M supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the Start and Stop conditions, while the MCP7940M works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.1.1 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1.1.1 Bus Not Busy (A)

Both data and clock lines remain high.

3.1.1.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

3.1.1.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must end with a Stop condition.

3.1.1.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

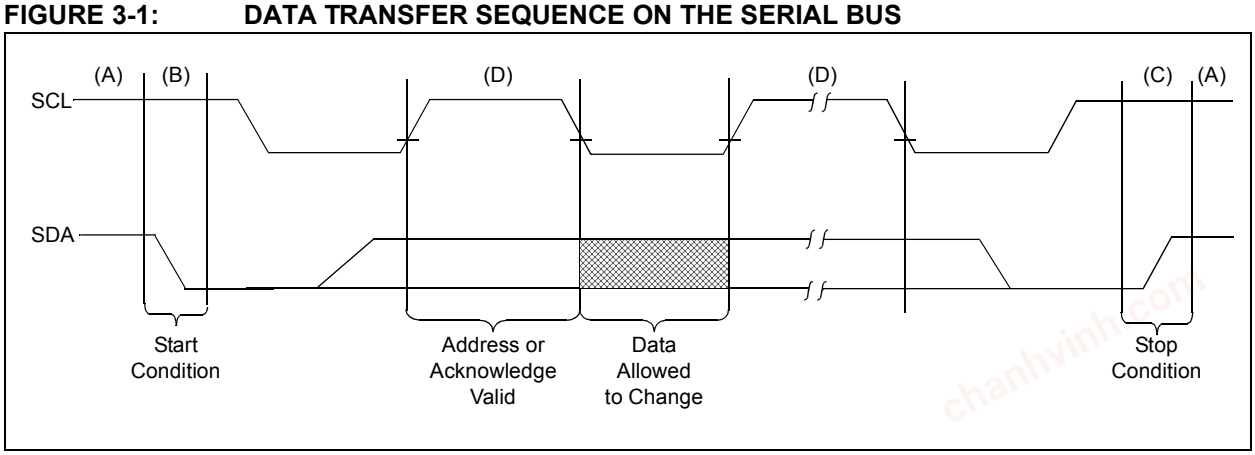
Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device.

3.1.1.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

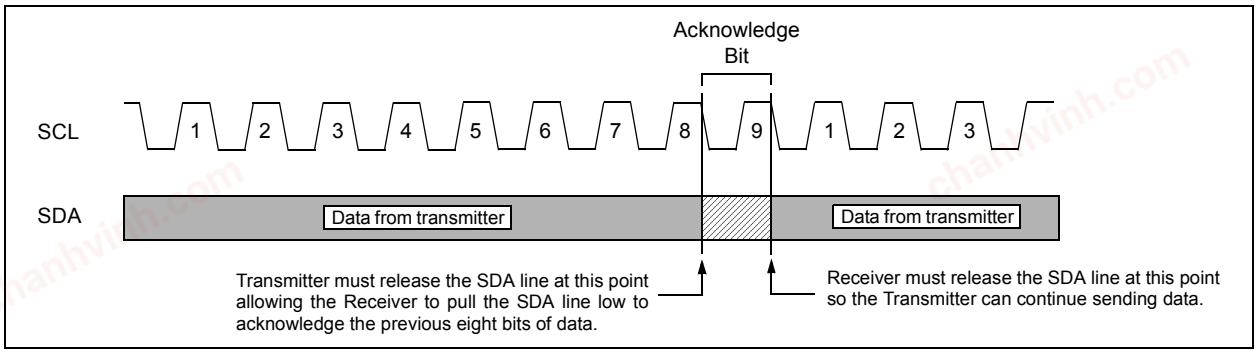
A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable-low during the high period of the Acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (MCP7940M) will leave the data line high to enable the master to generate the Stop condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



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FIGURE 3-2: ACKNOWLEDGE TIMING



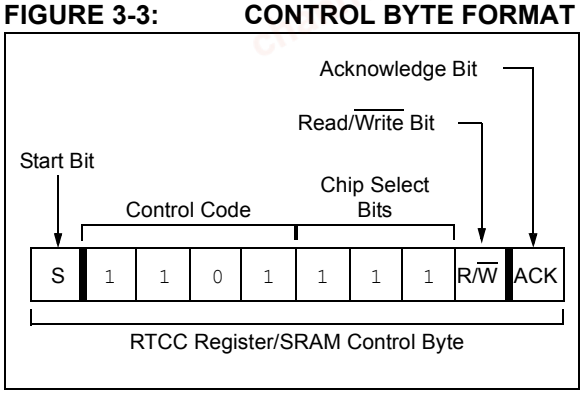
3.1.2 DEVICE ADDRESSING

The control byte is the first byte received following the Start condition from the master device (Figure 3-3). The control byte begins with a 4-bit control code. For the MCP7940M, this is set '1101' for register read and write operations. The next three bits are non-configurable Chip Select bits that must always be set to '1'.

The last bit of the control byte defines the operation to be performed. When set to a '1' a read operation is selected, and when set to a '0' a write operation is selected.

The combination of the 4-bit control code and the three Chip Select bits is called the slave address. Upon receiving a valid slave address, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the MCP7940M will select a read or a write operation.

FIGURE 3-3: CONTROL BYTE FORMAT



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4.0 FUNCTIONAL DESCRIPTION

The MCP7940M is a highly-integrated Real-Time Clock/Calendar (RTCC). Using an on-board, low-power oscillator, the current time is maintained in seconds, minutes, hours, day of week, date, month, and year. The MCP7940M also features 64 bytes of general purpose SRAM. Two alarm modules allow interrupts to be generated at specific times with flexible comparison options. Digital trimming can be used to compensate for inaccuracies inherent with crystals.

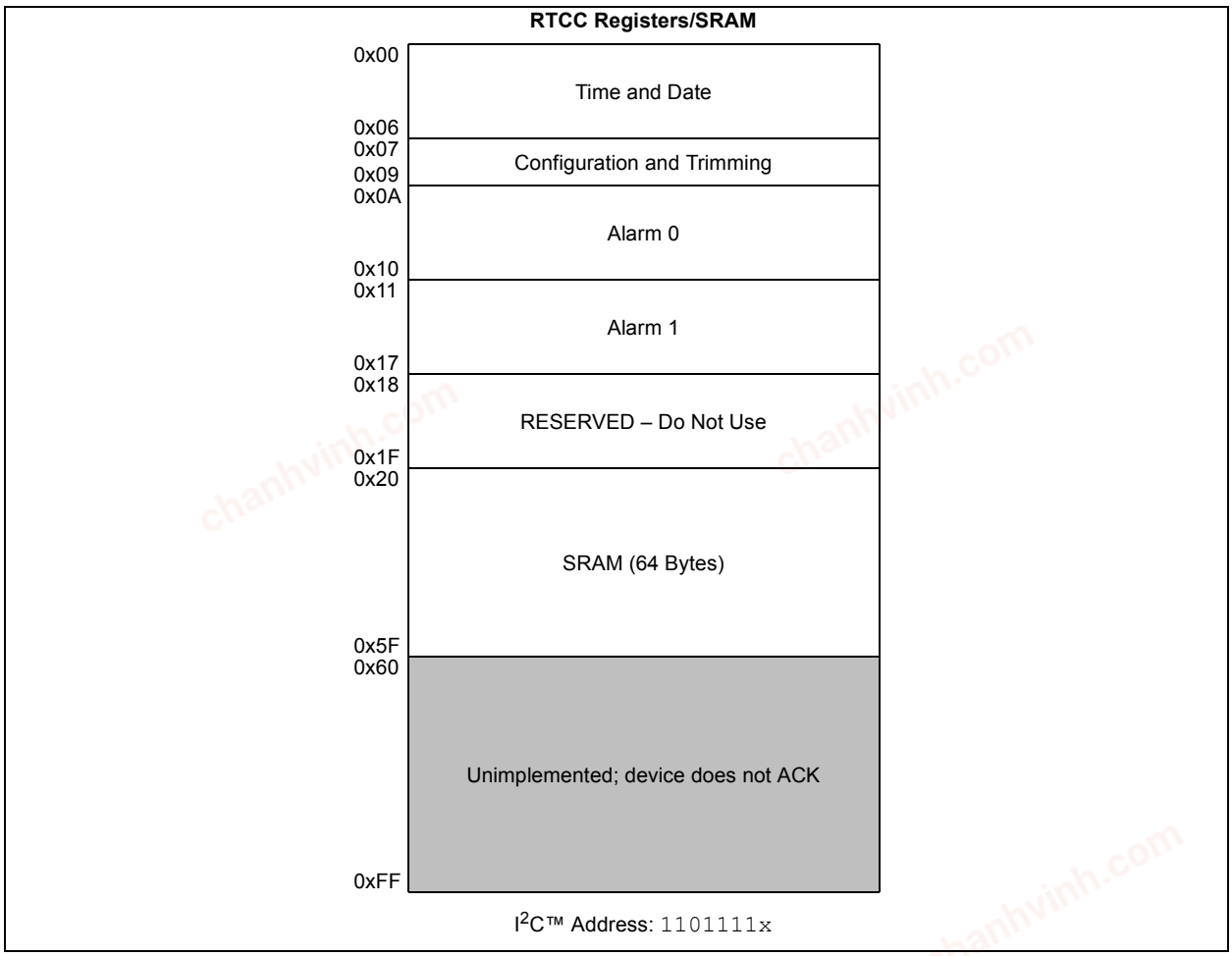
The RTCC configuration and Status registers are used to access all of the modules featured on the MCP7940M.

4.1 Memory Organization

The MCP7940M features two different blocks of memory: the RTCC registers and general purpose SRAM (Figure 4-1). They share the same address space, accessed through the '1101111X' control byte. Unused locations are not accessible. The MCP7940M will not acknowledge if the address is out of range, as shown in the shaded region of the memory map in Figure 4-1.

The RTCC registers are contained in addresses 0x00-0x1F. Table 4-1 shows the detailed RTCC register map. There are 64 bytes of user-accessible SRAM, located in the address range 0x20-0x5F. The SRAM is a separate block from the RTCC registers.

FIGURE 4-1: MEMORY MAP



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TABLE 4-1: DETAILED RTCC REGISTER MAP

Addr.	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Section 4.3 “Timekeeping”									
00h	RTCSEC	ST	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
01h	RTCMIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
02h	RTCHOUR	—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
03h	RTCWKDAY	—	—	OSCRUN	—	—	WKDAY2	WKDAY1	WKDAY0
04h	RTCDATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
05h	RTCMTH	—	—	LPYR	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
06h	RTCYEAR	YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
07h	CONTROL	OUT	SQWEN	ALM1EN	ALM0EN	EXTOSC	CRSTRIM	SQWFS1	SQWFS0
08h	OSCTRIM	SIGN	TRIMVAL6	TRIMVAL5	TRIMVAL4	TRIMVAL3	TRIMVAL2	TRIMVAL1	TRIMVAL0
09h	Reserved	Reserved – Do not use							
Section 4.4 “Alarms”									
0Ah	ALM0SEC	—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
0Bh	ALM0MIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
0Ch	ALM0HOUR	—	12/$\overline{24}$(2)	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
0Dh	ALM0WKDAY	ALMPOL	ALM0MSK2	ALM0MSK1	ALM0MSK0	ALM0IF	WKDAY2	WKDAY1	WKDAY0
0Eh	ALM0DATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
0Fh	ALM0MTH	—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
10h	Reserved	Reserved – Do not use							
Section 4.4 “Alarms”									
11h	ALM1SEC	—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
12h	ALM1MIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
13h	ALM1HOUR	—	12/$\overline{24}$(2)	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
14h	ALM1WKDAY	ALMPOL(3)	ALM1MSK2	ALM1MSK1	ALM1MSK0	ALM1IF	WKDAY2	WKDAY1	WKDAY0
15h	ALM1DATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
16h	ALM1MTH	—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
17h-1Fh	Reserved	Reserved – Do not use							

Note 1: Grey areas are unimplemented.

2: The 12/$\overline{24}$ bits in the ALMxHOUR registers are read-only and reflect the value of the 12/$\overline{24}$ bit in the RTCHOUR register.

3: The ALMPOL bit in the ALM1WKDAY register is read-only and reflects the value of the ALMPOL bit in the ALM0WKDAY register.

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4.2 Oscillator Configuration

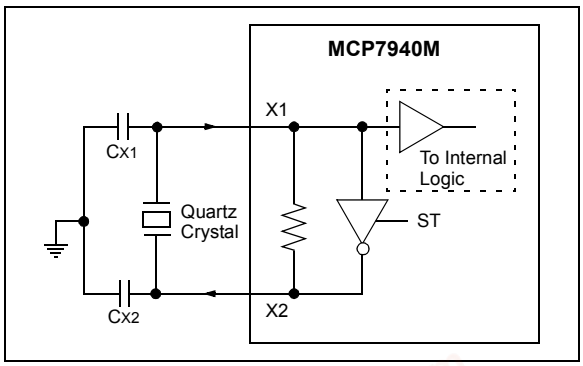
The MCP7940M can be operated in two different oscillator configurations: using an external crystal or using an external clock input.

4.2.1 EXTERNAL CRYSTAL

The crystal oscillator circuit on the MCP7940M is designed to operate with a standard 32.768 kHz tuning fork crystal and matching external load capacitors. By using external load capacitors, the MCP7940M allows for a wide selection of crystals. Suitable crystals have a load capacitance (C_L) of 6-9 pF. Crystals with a load capacitance of 12.5 pF are not recommended.

Figure 4-2 shows the pin connections when using an external crystal.

FIGURE 4-2: CRYSTAL OPERATION



Note 1:	The ST bit must be set to enable the crystal oscillator circuit.
2:	Always verify oscillator performance over the voltage and temperature range that is expected for the application.

4.2.1.1 Choosing Load Capacitors

C_L is the effective load capacitance as seen by the crystal, and includes the physical load capacitors, pin capacitance, and stray board capacitance. Equation 4-1 can be used to calculate C_L.

C_{X1} and C_{X2} are the external load capacitors. They must be chosen to match the selected crystal's specified load capacitance.

Note:	If the load capacitance is not correctly matched to the chosen crystal's specified value, the crystal may give a frequency outside of the crystal manufacturer's specifications.

EQUATION 4-1: LOAD CAPACITANCE CALCULATION

$$C_L = \frac{C_{X1} \times C_{X2}}{C_{X1} + C_{X2}} + C_{STRAY}$$

Where:

C_L = Effective load capacitance
C_{X1} = Capacitor value on X1 + C_{OSC}
C_{X2} = Capacitor value on X2 + C_{OSC}
C_{STRAY} = PCB stray capacitance

4.2.1.2 Layout Considerations

The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to V_{SS}. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

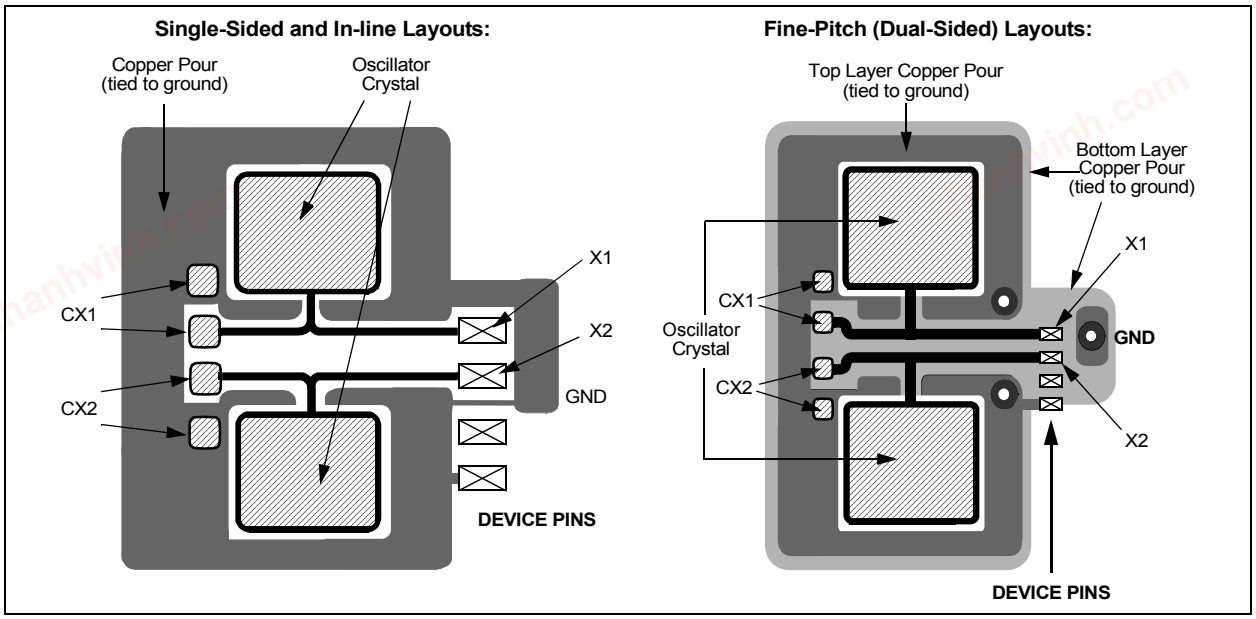
Layout suggestions are shown in Figure 4-3. In-line packages may be handled with a single-sided layout that completely encompasses the oscillator pins. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the corporate web site (www.microchip.com):

- *AN1365, "Recommended Usage of Microchip Serial RTCC Devices"*
- *AN1519, "Recommended Crystals for Microchip Stand-Alone Real-Time Clock Calendar Devices"*

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FIGURE 4-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT

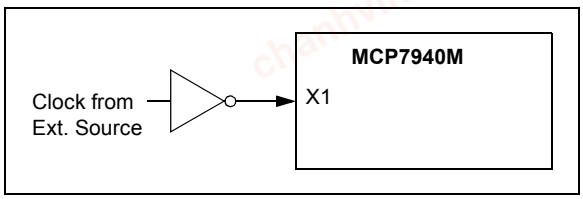


4.2.2 EXTERNAL CLOCK INPUT

A 32.768 kHz external clock source can be connected to the X1 pin (Figure 4-4). When using this configuration, the X2 pin should be left floating.

Note:	The EXTOSC bit must be set to enable an external clock source.

FIGURE 4-4: EXTERNAL CLOCK INPUT OPERATION



4.2.3 OSCILLATOR FAILURE STATUS

The MCP7940M features an oscillator failure flag, OSCRUN, that indicates whether or not the oscillator is running. The OSCRUN bit is automatically set after 32 oscillator cycles are detected. If no oscillator cycles are detected for more than TOSF, then the OSCRUN bit is automatically cleared (Figure 4-5). This can occur if the oscillator is stopped by clearing the ST bit or due to oscillator failure.

FIGURE 4-5: OSCILLATOR FAILURE STATUS TIMING DIAGRAM

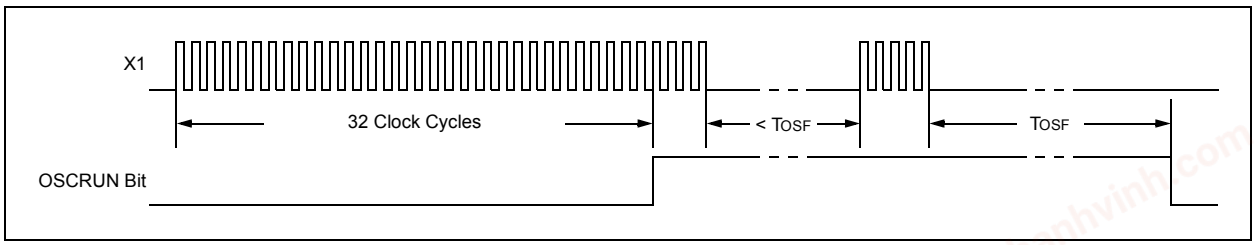


TABLE 4-2: SUMMARY OF REGISTERS ASSOCIATED WITH OSCILLATOR CONFIGURATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
RTCSEC	ST	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0	14
RTCWKDAY	—	—	OSCRUN	—	—	WKDAY2	WKDAY1	WKDAY0	16
CONTROL	OUT	SQWEN	ALM1EN	ALM0EN	EXTOSC	CRSTRIM	SQWFS1	SQWFS0	24

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by oscillator configuration.

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4.3 Timekeeping

The MCP7940M maintains the current time and date using an external 32.768 kHz crystal or clock source. Separate registers are used for tracking seconds, minutes, hours, day of week, date, month, and year. The MCP7940M automatically adjusts for months with less than 31 days and compensates for leap years from 2001 to 2399. The year is stored as a two-digit value.

Both 12-hour and 24-hour time formats are supported and are selected using the 12/$\overline{24}$ bit.

The day of week value counts from 1 to 7, increments at midnight, and the representation is user-defined (i.e., the MCP7940M does not require 1 to equal Sunday, etc.).

All time and date values are stored in the registers as binary-coded decimal (BCD) values.

When reading from the timekeeping registers, the registers are buffered to prevent errors due to rollover of counters. The following events cause the buffers to be updated:

- When a read is initiated from the RTCC registers (addresses 0x00 to 0x1F)
- During an RTCC register read operation, when the register address rolls over from 0x1F to 0x00

The timekeeping registers should be read in a single operation to utilize the on-board buffers and avoid rollover issues.

Note 1: Loading invalid values into the time and date registers will result in undefined operation.

2: To avoid rollover issues when loading new time and date values, the oscillator/clock input should be disabled by clearing the ST bit for External Crystal mode and the EXTOSC bit for External Clock Input mode. After waiting for the OSCRUN bit to clear, the new values can be loaded and the ST or EXTOSC bit can then be re-enabled.

4.3.1 DIGIT CARRY RULES

The following list explains which timer values cause a digit carry when there is a rollover:

- Time of day: from 11:59:59 PM to 12:00:00 AM (12-hour mode) or 23:59:59 to 00:00:00 (24-hour mode), with a carry to the Date and Weekday fields
- Date: carries to the Month field according to Table 5-3
- Weekday: from 7 to 1 with no carry
- Month: from 12/31 to 01/01 with a carry to the Year field
- Year: from 99 to 00 with no carry

TABLE 4-3: DAY TO MONTH ROLLOVER SCHEDULE

Month	Name	Maximum Date
01	January	31
02	February	28 or 29(1)
03	March	31
04	April	30
05	May	31
06	June	30
07	July	31
08	August	31
09	September	30
10	October	31
11	November	30
12	December	31

Note 1: 29 during leap years, otherwise 28.

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REGISTER 4-1: RTCSEC: TIMEKEEPING SECONDS VALUE REGISTER (ADDRESS 0x00)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ST	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7 **ST:** Start Oscillator bit
1 = Oscillator enabled
0 = Oscillator disabled

bit 6-4 **SECTEN<2:0>:** Binary-Coded Decimal Value of Second's Tens Digit
Contains a value from 0 to 5

bit 3-0 **SECONE<3:0>:** Binary-Coded Decimal Value of Second's Ones Digit
Contains a value from 0 to 9

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REGISTER 4-2: RTCMIN: TIMEKEEPING MINUTES VALUE REGISTER (ADDRESS 0x01)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **MINTEN<2:0>:** Binary-Coded Decimal Value of Minute's Tens Digit
Contains a value from 0 to 5

bit 3-0 **MINONE<3:0>:** Binary-Coded Decimal Value of Minute's Ones Digit
Contains a value from 0 to 9

REGISTER 4-3: RTCHOUR: TIMEKEEPING HOURS VALUE REGISTER (ADDRESS 0x02)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

If 12/$\overline{24}$ = 1 (12-hour format):

bit 7 **Unimplemented:** Read as '0'

bit 6 **12/$\overline{24}$:** 12 or 24 Hour Time Format bit
1 = 12-hour format
0 = 24-hour format

bit 5 **$\overline{AM}$/PM:** AM/PM Indicator bit
1 = PM
0 = AM

bit 4 **HRTEN0:** Binary-Coded Decimal Value of Hour's Tens Digit
Contains a value from 0 to 1

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour's Ones Digit
Contains a value from 0 to 9

If 12/$\overline{24}$ = 0 (24-hour format):

bit 7 **Unimplemented:** Read as '0'

bit 6 **12/$\overline{24}$:** 12 or 24 Hour Time Format bit
1 = 12-hour format
0 = 24-hour format

bit 5-4 **HRTEN<1:0>:** Binary-Coded Decimal Value of Hour's Tens Digit
Contains a value from 0 to 2.

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour's Ones Digit
Contains a value from 0 to 9

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REGISTER 4-4: RTCWKDAY: TIMEKEEPING WEEKDAY VALUE REGISTER (ADDRESS 0x03)

U-0	U-0	R-0	U-0	U-0	R/W-0	R/W-0	R/W-1
—	—	OSCRUN	—	—	WKDAY2	WKDAY1	WKDAY0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **OSCRUN:** Oscillator Status bit
1 = Oscillator is enabled and running
0 = Oscillator has stopped or has been disabled

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **WKDAY<2:0>:** Binary-Coded Decimal Value of Day of Week
Contains a value from 1 to 7. The representation is user-defined.

REGISTER 4-5: RTCDATE: TIMEKEEPING DATE VALUE REGISTER (ADDRESS 0x04)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DATETEN<1:0>:** Binary-Coded Decimal Value of Date's Tens Digit
Contains a value from 0 to 3

bit 3-0 **DATEONE<3:0>:** Binary-Coded Decimal Value of Date's Ones Digit
Contains a value from 0 to 9

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REGISTER 4-6: RTCMTH: TIMEKEEPING MONTH VALUE REGISTER (ADDRESS 0x05)

U-0	U-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	LPYR	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **LPYR:** Leap Year bit
1 = Year is a leap year
0 = Year is not a leap year

bit 4 **MTHTEN0:** Binary-Coded Decimal Value of Month's Tens Digit
Contains a value of 0 or 1

bit 3-0 **MTHONE<3:0>:** Binary-Coded Decimal Value of Month's Ones Digit
Contains a value from 0 to 9

REGISTER 4-7: RTCYEAR: TIMEKEEPING YEAR VALUE REGISTER (ADDRESS 0x06)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-4 **YRTEN<3:0>:** Binary-Coded Decimal Value of Year's Tens Digit
Contains a value from 0 to 9

bit 3-0 **YRONE<3:0>:** Binary-Coded Decimal Value of Year's Ones Digit
Contains a value from 0 to 9

TABLE 4-4: SUMMARY OF REGISTERS ASSOCIATED WITH TIMEKEEPING

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
RTCSEC	ST	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0	14
RTCMIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0	15
RTCHOUR	—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0	15
RTCWKDAY	—	—	OSCRUN	—	—	WKDAY2	WKDAY1	WKDAY0	16
RTCDATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0	16
RTCMTH	—	—	LPYR	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0	17
RTCYEAR	YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0	17

Legend: — = unimplemented location, read as '0'. Shaded cells are not used in timekeeping.

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4.4 Alarms

The MCP7940M features two independent alarms. Each alarm can be used to either generate an interrupt at a specific time in the future, or to generate a periodic interrupt every minute, hour, day, day of week, or month.

There is a separate interrupt flag, ALMxIF, for each alarm. The interrupt flags are set by hardware when the chosen alarm mask condition matches (Table 4-5). The interrupt flags must be cleared in software.

If either alarm module is enabled by setting the corresponding ALMxEN bit in the CONTROL register, and if the square wave clock output is disabled (SQWEN = 0), then the MFP will operate in Alarm Interrupt Output mode. Refer to **Section 4.5 "Output Configurations"** for details.

Both Alarm0 and Alarm1 offer identical operation. All time and date values are stored in the registers as binary-coded decimal (BCD) values.

Note: Throughout this section, references to the register and bit names for the alarm modules are referred to generically by the use of 'x' in place of the specific module number. Thus, "ALMxSEC" might refer to the seconds register for Alarm0 or Alarm1.

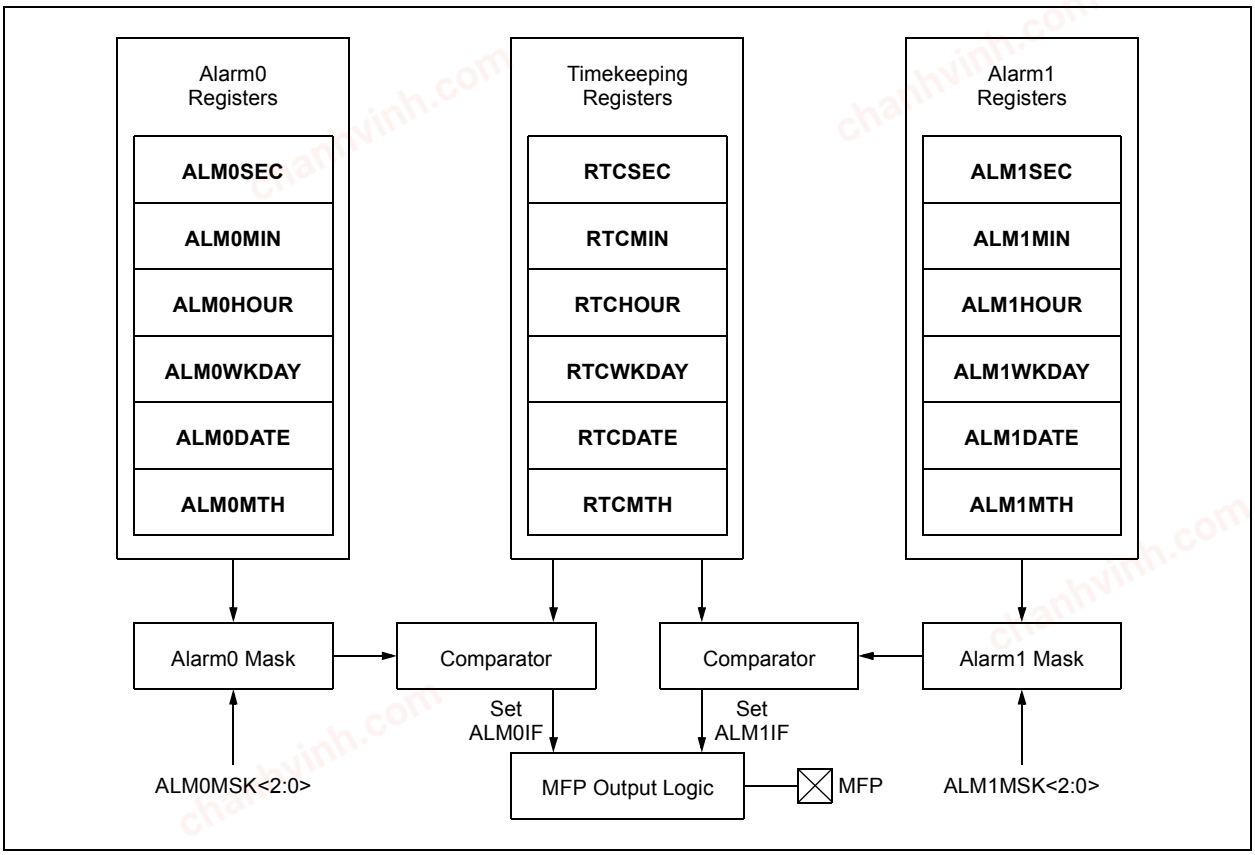
TABLE 4-5: ALARM MASKS

ALMxMSK<2:0>	Alarm Asserts on Match of
000	Seconds
001	Minutes
010	Hours
011	Day of Week
100	Date
101	Reserved
110	Reserved
111	Seconds, Minutes, Hours, Day of Week, Date, and Month

Note 1: The alarm interrupt flags must be cleared by the user. If a flag is cleared while the corresponding alarm condition still matches, the flag will be set again, generating another interrupt.

2: Loading invalid values into the alarm registers will result in undefined operation.

FIGURE 4-6: ALARM BLOCK DIAGRAM



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4.4.1 CONFIGURING THE ALARM

In order to configure the alarm modules, the following steps need to be performed:

1. Load the timekeeping registers and enable the oscillator
2. Configure the ALMxMSK<2:0> bits to select the desired alarm mask
3. Set or clear the ALMPOL bit according to the desired output polarity
4. Ensure the ALMxIF flag is cleared
5. Based on the selected alarm mask, load the alarm match value into the appropriate register(s)
6. Enable the alarm module by setting the ALMxEN bit

REGISTER 4-8: ALMxSEC: ALARM0/1 SECONDS VALUE REGISTER (ADDRESSES 0x0A/0x11)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **SECTEN<2:0>:** Binary-Coded Decimal Value of Second’s Tens Digit
Contains a value from 0 to 5

bit 3-0 **SECONE<3:0>:** Binary-Coded Decimal Value of Second’s Ones Digit
Contains a value from 0 to 9

REGISTER 4-9: ALMxMIN: ALARM0/1 MINUTES VALUE REGISTER (ADDRESSES 0x0B/0x12)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is clear	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **MINTEN<2:0>:** Binary-Coded Decimal Value of Minute’s Tens Digit
Contains a value from 0 to 5

bit 3-0 **MINONE<3:0>:** Binary-Coded Decimal Value of Minute’s Ones Digit
Contains a value from 0 to 9

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REGISTER 4-10: ALMxHOUR: ALARM0/1 HOURS VALUE REGISTER (ADDRESSES 0x0C/0x13)

U-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

If 12/$\overline{24}$ = 1 (12-hour format):

bit 7 **Unimplemented:** Read as '0'

bit 6 **12/$\overline{24}$:** 12 or 24 Hour Time Format bit(1)
1 = 12-hour format
0 = 24-hour format

bit 5 **$\overline{AM}$/PM:** AM/PM Indicator bit
1 = PM
0 = AM

bit 4 **HRTEN0:** Binary-Coded Decimal Value of Hour's Tens Digit
Contains a value from 0 to 1

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour's Ones Digit
Contains a value from 0 to 9

If 12/$\overline{24}$ = 0 (24-hour format):

bit 7 **Unimplemented:** Read as '0'

bit 6 **12/$\overline{24}$:** 12 or 24 Hour Time Format bit(1)
1 = 12-hour format
0 = 24-hour format

bit 5-4 **HRTEN<1:0>:** Binary-Coded Decimal Value of Hour's Tens Digit
Contains a value from 0 to 2.

bit 3-0 **HRONE<3:0>:** Binary-Coded Decimal Value of Hour's Ones Digit
Contains a value from 0 to 9

Note 1: This bit is read-only and reflects the value of the 12/$\overline{24}$ bit in the RTCHOUR register.

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REGISTER 4-11: ALMxWKDAY: ALARM0/1 WEEKDAY VALUE REGISTER (ADDRESSES 0x0D/ 0x14)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
ALMPOL	ALMxMSK2	ALMxMSK1	ALMxMSK0	ALMxIF	WKDAY2	WKDAY1	WKDAY0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7 **ALMPOL:** Alarm Interrupt Output Polarity bit
1 = Asserted output state of MFP is a logic high level
0 = Asserted output state of MFP is a logic low level

bit 6-4 **ALMxMSK<2:0>:** Alarm Mask bits
000 = Seconds match
001 = Minutes match
010 = Hours match (logic takes into account 12-/24-hour operation)
011 = Day of week match
100 = Date match
101 = Reserved; do not use
110 = Reserved; do not use
111 = Seconds, Minutes, Hour, Day of Week, Date and Month

bit 3 **ALMxIF:** Alarm Interrupt Flag bit(1,2)
1 = Alarm match occurred (must be cleared in software)
0 = Alarm match did not occur

bit 2-0 **WKDAY<2:0>:** Binary-Coded Decimal Value of Day bits
Contains a value from 1 to 7. The representation is user-defined.

Note 1: If a match condition still exists when this bit is cleared, it will be set again automatically.
2: The ALMxIF bit cannot be written to a 1 in software. Writing to the ALMxWKDAY register will always clear the ALMxIF bit.

REGISTER 4-12: ALMxDATE: ALARM0/1 DATE VALUE REGISTER (ADDRESSES 0x0E/0x15)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DATETEN<1:0>:** Binary-Coded Decimal Value of Date's Tens Digit
Contains a value from 0 to 3

bit 3-0 **DATEONE<3:0>:** Binary-Coded Decimal Value of Date's Ones Digit
Contains a value from 0 to 9

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REGISTER 4-13: ALMxMTH: ALARM0/1 MONTH VALUE REGISTER (ADDRESSES 0x0F/0x16)

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **MTHTEN0:** Binary-Coded Decimal Value of Month's Tens Digit
Contains a value of 0 or 1

bit 3-0 **MTHONE<3:0>:** Binary-Coded Decimal Value of Month's Ones Digit
Contains a value from 0 to 9

TABLE 4-6: SUMMARY OF REGISTERS ASSOCIATED WITH ALARMS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ALM0SEC	—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0	19
ALM0MIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0	19
ALM0HOUR	—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0	20
ALM0WKDAY	ALMPOL	ALM0MSK2	ALM0MSK1	ALM0MSK0	ALM0IF	WKDAY2	WKDAY1	WKDAY0	21
ALM0DATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0	21
ALM0MTH	—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0	22
ALM1SEC	—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0	19
ALM1MIN	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0	19
ALM1HOUR	—	12/$\overline{24}$	$\overline{AM}$/PM HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0	20
ALM1WKDAY	ALMPOL	ALM1MSK2	ALM1MSK1	ALM1MSK0	ALM1IF	WKDAY2	WKDAY1	WKDAY0	21
ALM1DATE	—	—	DATETEN1	DATETEN0	DATEONE3	DATEONE2	DATEONE1	DATEONE0	21
ALM1MTH	—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0	22
CONTROL	OUT	SQWEN	ALM1EN	ALM0EN	EXTOSC	CRSTRIM	SQWFS1	SQWFS0	24

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by alarms.

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4.5 Output Configurations

The MCP7940M features Square Wave Clock Output, Alarm Interrupt Output, and General Purpose Output modes. All of the output functions are multiplexed onto MFP according to Table 4-7.

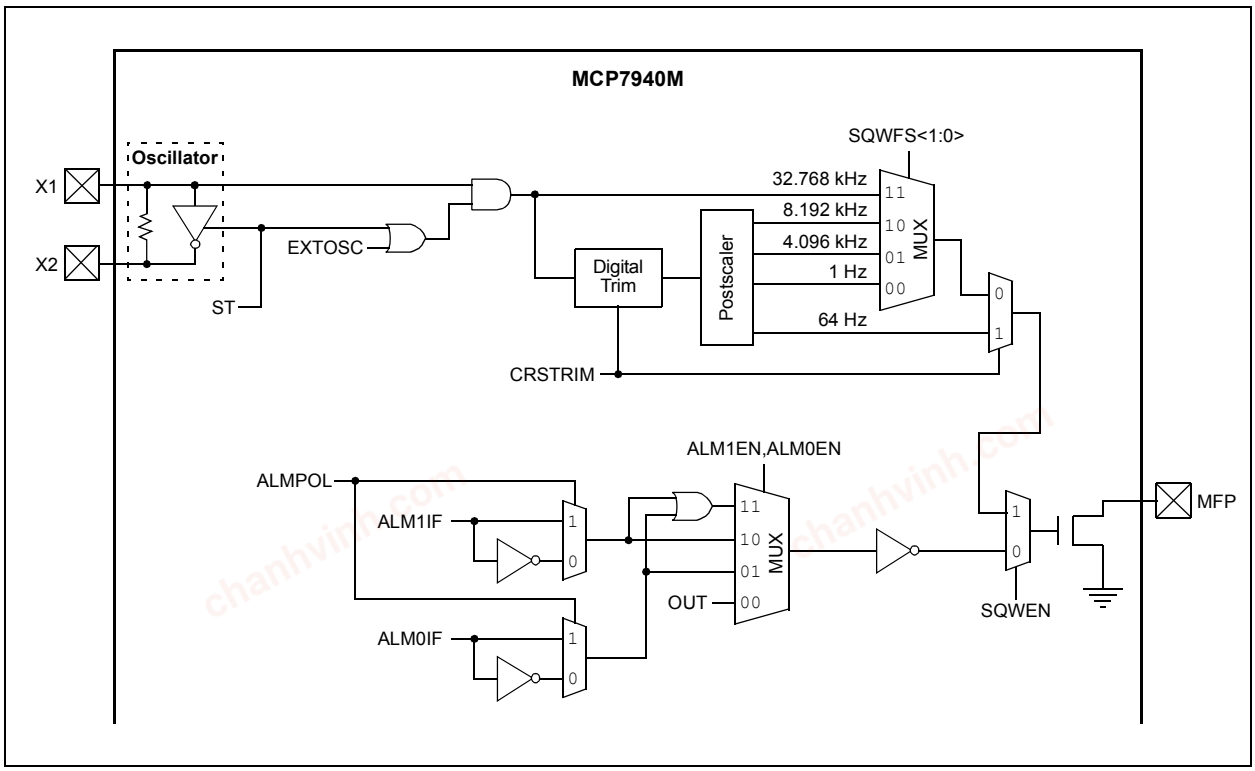
If none of the output functions are being used, the MFP can safely be left floating.

Note: The MFP is an open-drain output and requires a pull-up resistor to VCC (typically 10 kΩ).

TABLE 4-7: MFP OUTPUT MODES

SQWEN	ALM0EN	ALM1EN	Mode
0	0	0	General Purpose Output
0	1	0	Alarm Interrupt Output
0	0	1	
0	1	1	
1	x	x	Square Wave Clock Output

FIGURE 4-7: MFP OUTPUT BLOCK DIAGRAM



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REGISTER 4-14: CONTROL: RTCC CONTROL REGISTER (ADDRESS 0x07)

R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OUT	SQWEN	ALM1EN	ALM0EN	EXTOSC	CRSTRIM	SQWFS1	SQWFS0
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7 **OUT:** Logic Level for General Purpose Output bit

Square Wave Clock Output Mode (SQWEN = 1):
Unused.

Alarm Interrupt Output mode (ALM0EN = 1 or ALM1EN = 1):
Unused.

General Purpose Output mode (SQWEN = 0, ALM0EN = 0, and ALM1EN = 0):
1 = MFP signal level is logic high
0 = MFP signal level is logic low

bit 6 **SQWEN:** Square Wave Output Enable bit
1 = Enable Square Wave Clock Output mode
0 = Disable Square Wave Clock Output mode

bit 5 **ALM1EN:** Alarm 1 Module Enable bit
1 = Alarm 1 enabled
0 = Alarm 1 disabled

bit 4 **ALM0EN:** Alarm 0 Module Enable bit
1 = Alarm 0 enabled
0 = Alarm 0 disabled

bit 3 **EXTOSC:** External Oscillator Input bit
1 = Enable X1 pin to be driven by external 32.768 kHz source
0 = Disable external 32.768 kHz input

bit 2 **CRSTRIM:** Coarse Trim Mode Enable bit
Coarse Trim mode results in the MCP7940M applying digital trimming every 64 Hz clock cycle.
1 = Enable Coarse Trim mode. If SQWEN = 1, MFP will output trimmed 64 Hz(1) nominal clock signal.
0 = Disable Coarse Trim mode
See **Section 4.6 "Digital Trimming"** for details

bit 1-0 **SQWFS<1:0>:** Square Wave Clock Output Frequency Select bits

If SQWEN = 1 and CRSTRIM = 0:
Selects frequency of clock output on MFP
00 = 1 Hz(1)
01 = 4.096 kHz(1)
10 = 8.192 kHz(1)
11 = 32.768 kHz

If SQWEN = 0 or CRSTRIM = 1:
Unused.

Note 1: The 8.192 kHz, 4.096 kHz, 64 Hz, and 1 Hz square wave clock output frequencies are affected by digital trimming.

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4.5.1 SQUARE WAVE OUTPUT MODE

The MCP7940M can be configured to generate a square wave clock signal on MFP. The input clock frequency, FOSC, is divided according to the SQWFS<1:0> bits as shown in Table 4-8.

Note:	All of the clock output rates are affected by digital trimming except for the 1:1 postscaler value (SQWFS<1:0> = 00).

TABLE 4-8: CLOCK OUTPUT RATES

SQWFS<1:0>	Postscaler	Nominal Frequency
00	1:1	32.768 kHz
01	1:4	8.192 kHz
10	1:8	4.096 kHz
11	1:32,768	1 Hz

Note 1: Nominal frequency assumes FOSC is 32.768 kHz.

4.5.2 ALARM INTERRUPT OUTPUT MODE

The MFP will provide an interrupt output when enabled alarms match and the square wave clock output is disabled. This prevents the user from having to poll the alarm interrupt flag to check for a match.

The ALMxIF flags control when the MFP is asserted, as described in the following sections.

4.5.2.1 Single Alarm Operation

When only one alarm module is enabled, the MFP output is based on the corresponding ALMxIF flag and the ALMPOL flag. If ALMPOL = 1, the MFP output reflects the value of the ALMxIF flag. If ALMPOL = 0, the MFP output reflects the inverse of the ALMxIF flag (Table 4-9).

TABLE 4-9: SINGLE ALARM OUTPUT TRUTH TABLE

ALMPOL	ALMxIF(1)	MFP
0	0	1
0	1	0
1	0	0
1	1	1

Note 1: ALMxIF refers to the interrupt flag corresponding to the alarm module that is enabled.

4.5.2.2 Dual Alarm Operation

When both alarm modules are enabled, the MFP output is determined by a combination of the ALM0IF, ALM1IF, and ALMPOL flags.

If ALMPOL = 1, the ALM0IF and ALM1IF flags are OR'd together and the result is output on MFP. If ALMPOL = 0, the ALM0IF and ALM1IF flags are AND'd together, and the result is inverted and output on MFP (Table 4-10). This provides the user with flexible options for combining alarms.

Note:	If ALMPOL = 0 and both alarms are enabled, the MFP will only assert when both ALM0IF and ALM1IF are set.

TABLE 4-10: DUAL ALARM OUTPUT TRUTH TABLE

ALMPOL	ALM0IF	ALM1IF	MFP
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

4.5.3 GENERAL PURPOSE OUTPUT MODE

If the square wave clock output and both alarm modules are disabled, the MFP acts as a general purpose output. The output logic level is controlled by the OUT bit.

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TABLE 4-11: SUMMARY OF REGISTERS ASSOCIATED WITH OUTPUT CONFIGURATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ALM0WKDAY	ALMPOL	ALM0MSK2	ALM0MSK1	ALM0MSK0	ALM0IF	WKDAY2	WKDAY1	WKDAY0	21
ALM1WKDAY	ALMPOL	ALM1MSK2	ALM1MSK1	ALM1MSK0	ALM1IF	WKDAY2	WKDAY1	WKDAY0	21
CONTROL	OUT	SQWEN	ALM1EN	ALM0EN	EXTOSC	CRSTRIM	SQWFS1	SQWFS0	24

Legend: — = unimplemented location, read as '0'. Shaded cells are not used in output configuration.

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4.6 Digital Trimming

The MCP7940M features digital trimming to correct for inaccuracies of the external crystal or clock source, up to roughly ±129 PPM when CRSTRIM = 0. In addition to compensating for intrinsic inaccuracies in the clock, this feature can also be used to correct for error due to temperature variation. This can enable the user to achieve high levels of accuracy across a wide temperature operating range.

Digital trimming consists of the MCP7940M periodically adding or subtracting clock cycles, resulting in small adjustments in the internal timing. The adjustment occurs once per minute when CRSTRIM = 0. The SIGN bit specifies whether to add cycles or to subtract them. The TRIMVAL<6:0> bits are used to specify by how many clock cycles to adjust. Each step in the TRIMVAL<6:0> value equates to adding or subtracting two clock pulses to or from the 32.768 kHz clock signal. This results in a correction of roughly 1.017 PPM per step when CRSTRIM = 0. Setting TRIMVAL<6:0> to 0x00 disables digital trimming.

REGISTER 4-15: OSCTRIM: OSCILLATOR DIGITAL TRIM REGISTER (ADDRESS 0x08)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SIGN	TRIMVAL6	TRIMVAL5	TRIMVAL4	TRIMVAL3	TRIMVAL2	TRIMVAL1	TRIMVAL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is clear	x = Bit is unknown

bit 7 **SIGN:** Trim Sign bit
1 = Add clocks to correct for slow time
0 = Subtract clocks to correct for fast time

bit 6-0 **TRIMVAL<6:0>:** Oscillator Trim Value bits

When CRSTRIM = 0:
1111111 = Add or subtract 254 clock cycles every minute
1111110 = Add or subtract 252 clock cycles every minute
•
•
•
0000010 = Add or subtract 4 clock cycles every minute
0000001 = Add or subtract 2 clock cycles every minute
0000000 = Disable digital trimming

When CRSTRIM = 1:
1111111 = Add or subtract 254 clock cycles 128 times per second
1111110 = Add or subtract 252 clock cycles 128 times per second
•
•
•
0000010 = Add or subtract 4 clock cycles 128 times per second
0000001 = Add or subtract 2 clock cycles 128 times per second
0000000 = Disable digital trimming

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4.6.1 CALIBRATION

In order to perform calibration, the number of error clock pulses per minute must be found and the corresponding trim value must be loaded into TRIMVAL<6:0>.

There are two methods for determining the trim value. The first method involves measuring an output frequency directly and calculating the deviation from ideal. The second method involves observing the number of seconds gained or lost over a period of time.

Once the OSCTRIM register has been loaded, digital trimming will automatically occur every minute.

4.6.1.1 Calibration by Measuring Frequency

To calibrate the MCP7940M by measuring the output frequency, perform the following steps:

1. Enable the crystal oscillator or external clock input by setting the ST bit or EXTOSC bit, respectively.
2. Ensure TRIMVAL<6:0> is reset to 0x00.
3. Select an output frequency by setting SQWFS<1:0>.
4. Set SQWEN to enable the square wave output.
5. Measure the resulting output frequency using a calibrated measurement tool, such as a frequency counter.
6. Calculate the number of error clocks per minute (see Equation 4-2).

EQUATION 4-2: CALCULATING TRIM VALUE FROM MEASURED FREQUENCY

$$\text{TRIMVAL<6:0>} = \frac{(F_{IDEAL} - F_{MEAS}) \cdot \frac{32768}{F_{IDEAL}} \cdot 60}{2}$$

Where:

F_{IDEAL} = Ideal frequency based on SQWFS<1:0>
F_{MEAS} = Measured frequency

- If the number of error clocks per minute is negative, then the oscillator is *faster* than ideal and the SIGN bit must be cleared.
- If the number of error clocks per minute is positive, then the oscillator is *slower* than ideal and the SIGN bit must be set.

7. Load the correct value into TRIMVAL<6:0>.

Note: Using a lower output frequency and/or averaging the measured frequency over a number of clock pulses will reduce the effects of jitter and improve accuracy.

4.6.1.2 Calibration by Observing Time Deviation

To calibrate the MCP7940M by observing the deviation over time, perform the following steps:

1. Ensure TRIMVAL<6:0> is reset to 0x00.
2. Load the timekeeping registers to synchronize the MCP7940M with a known-accurate reference time.
3. Enable the crystal oscillator or external clock input by setting the ST bit or EXTOSC bit, respectively.
4. Observe how many seconds are gained or lost over a period of time (larger time periods offer more accuracy).
5. Calculate the PPM deviation (see Equation 4-3).

EQUATION 4-3: CALCULATING ERROR PPM

$$PPM = \frac{SecDeviation}{ExpectedSec} \cdot 1000000$$

Where:

$ExpectedSec$ = Number of seconds in chosen period
$SecDeviation$ = Number of seconds gained or lost

- If the MCP7940M has gained time relative to the reference clock, then the oscillator is *faster* than ideal and the SIGN bit must be cleared.
- If the MCP7940M has lost time relative to the reference clock, then the oscillator is *slower* than ideal and the SIGN bit must be set.

6. Calculate the trim value (see Equation 4-4).

EQUATION 4-4: CALCULATING TRIM VALUE FROM ERROR PPM

$$\text{TRIMVAL<6:0>} = \frac{PPM \cdot 32768 \cdot 60}{1000000 \cdot 2}$$

7. Load the correct value into TRIMVAL<6:0>.

Note 1: Choosing a longer time period for observing deviation will improve accuracy.

2: Large temperature variations during the observation period can skew results.

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4.6.2 COARSE TRIM MODE

When CRSTRIM = 1, Coarse Trim mode is enabled. While in this mode, the MCP7940M will apply trimming at a rate of 128 Hz. If SQWEN is set, the MFP will output a trimmed 64 Hz nominal clock signal.

Because trimming is applied at a rate of 128 Hz rather than once every minute, each step of the TRIMVAL<6:0> value has a significantly larger effect on the resulting time deviation and output clock frequency.

By monitoring the MFP output frequency while in this mode, the user can easily observe the TRIMVAL<6:0> value affecting the clock timing.

Note:	With Coarse Trim mode enabled, the TRIMVAL<6:0> value has a drastic effect on timing. Leaving the mode enabled during normal operation will likely result in inaccurate time.

TABLE 4-12: SUMMARY OF REGISTERS ASSOCIATED WITH DIGITAL TRIMMING

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CONTROL	OUT	SQWEN	ALM1EN	ALM0EN	EXTOSC	CRSTRIM	SQWFS1	SQWFS0	24
OSCTRIM	SIGN	TRIMVAL6	TRIMVAL5	TRIMVAL4	TRIMVAL3	TRIMVAL2	TRIMVAL1	TRIMVAL0	27

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by digital trimming.

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5.0 ON-BOARD MEMORY

The MCP7940M has 64 bytes of SRAM for general purpose usage.

Although the SRAM is a separate block from the RTCC registers, they are accessed using the same control byte, '1101111X'.

5.1 SRAM/RTCC Registers

The RTCC registers are located at addresses 0x00 to 0x1F, and the SRAM is located at addresses 0x20 to 0x5F. The SRAM can be accessed while the RTCC registers are being internally updated. The SRAM is not initialized by a Power-On Reset (POR).

5.1.1 SRAM/RTCC REGISTER BYTE WRITE

Following the Start condition from the master, the control code and the R/$\overline{W}$ bit (which is a logic low) are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that the address byte will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the address and will be written into the Address Pointer of the MCP7940M. After receiving another Acknowledge bit from the MCP7940M, the master device transmits the data byte to be written into the addressed memory location. The MCP7940M stores the data byte into memory and acknowledges again, and the master generates a Stop condition (Figure 5-1).

If an attempt is made to write to an address past 0x5F, the MCP7940M will not acknowledge the address or data bytes, and no data will be written. After a byte Write command, the internal Address Pointer will point to the address location following the one that was just written.

5.1.2 SRAM/RTCC REGISTER SEQUENTIAL WRITE

The write control byte, address, and the first data byte are transmitted to the MCP7940M in the same way as in a byte write. But instead of generating a Stop condition, the master transmits additional data bytes. Upon receipt of each byte, the MCP7940M responds with an Acknowledge, during which the data is latched into memory and the Address Pointer is internally incremented by one. As with the byte write operation, the master ends the command by generating a Stop condition (Figure 5-2).

There is no limit to the number of bytes that can be written in a single command. However, because the RTCC registers and SRAM are separate blocks, writing past the end of each block will cause the Address Pointer to roll over to the beginning of the same block. Specifically, the Address Pointer will roll over from 0x1F to 0x00, and from 0x5F to 0x20.

FIGURE 5-1: SRAM/RTCC BYTE WRITE

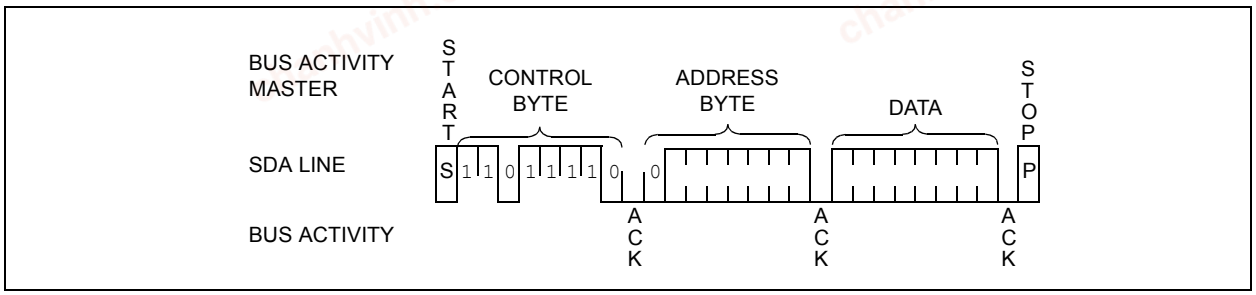
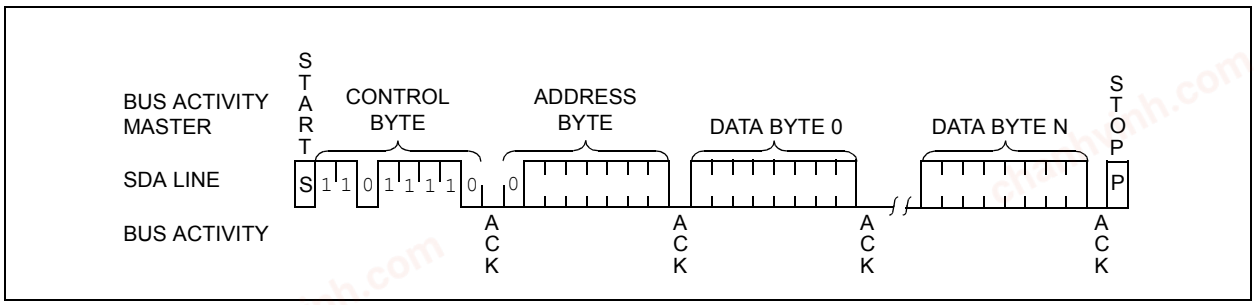


FIGURE 5-2: SRAM/RTCC SEQUENTIAL WRITE



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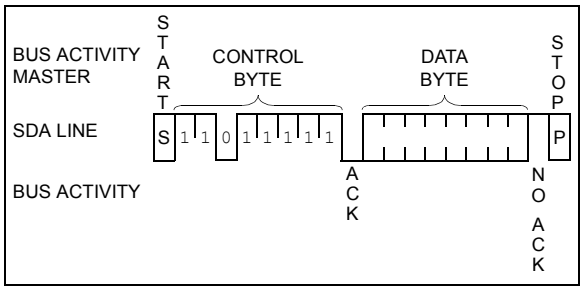
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5.1.3 SRAM/RTCC REGISTER CURRENT ADDRESS READ

The MCP7940M contains an address counter that maintains the address of the last byte accessed, internally incremented by one. Therefore, if the previous read access was to address n (n is any legal address), the next current address read operation would access data from address n + 1.

Upon receipt of the control byte with R/$\overline{W}$ bit set to '1', the MCP7940M issues an Acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a Stop condition and the MCP7940M discontinues transmission (Figure 5-3).

FIGURE 5-3: SRAM/RTCC CURRENT ADDRESS READ



5.1.4 SRAM/RTCC REGISTER RANDOM READ

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the address must be set. This is done by sending the address to the MCP7940M as part of a write operation (R/$\overline{W}$ bit set to '0'). After the address is sent, the master generates a Start condition following the Acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. Then, the master issues the control byte again but with the R/$\overline{W}$ bit set to a '1'. The MCP7940M will then issue an Acknowledge and transmit the 8-bit data word. The master will not acknowledge the transfer but it does generate a Stop condition which causes the MCP7940M to discontinue transmission (Figure 5-4). After a random Read command, the internal address counter will point to the address location following the one that was just read.

5.1.5 SRAM/RTCC REGISTER SEQUENTIAL READ

Sequential reads are initiated in the same way as a random read except that after the MCP7940M transmits the first data byte, the master issues an Acknowledge as opposed to the Stop condition used in a random read. This Acknowledge directs the MCP7940M to transmit the next sequentially addressed 8-bit word (Figure 5-5). Following the final byte transmitted to the master, the master will NOT generate an Acknowledge but will generate a Stop condition. To provide sequential reads, the MCP7940M contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory block to be serially read during one operation.

Because the RTCC registers and SRAM are separate blocks, reading past the end of each block will cause the Address Pointer to roll over to the beginning of the same block. Specifically, the Address Pointer will roll over from 0x1F to 0x00, and from 0x5F to 0x20.

FIGURE 5-4: SRAM/RTCC RANDOM READ

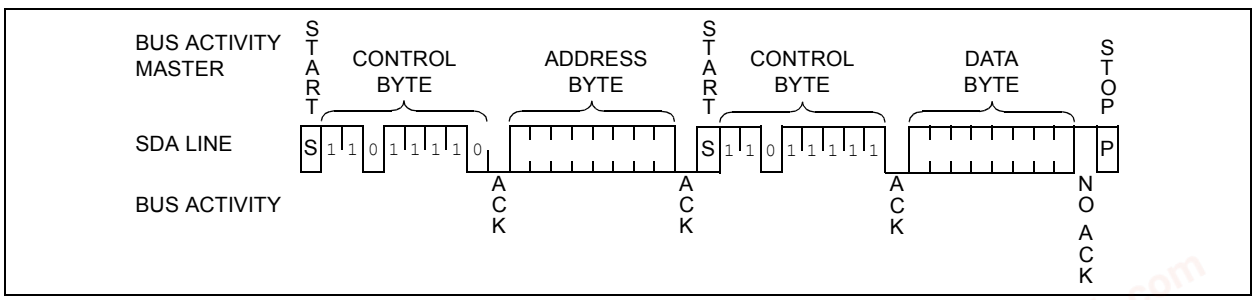
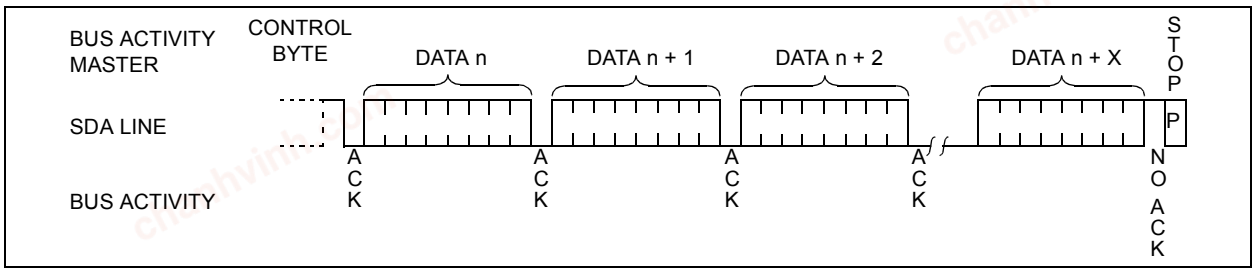


FIGURE 5-5: SRAM/RTCC SEQUENTIAL READ

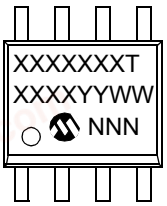


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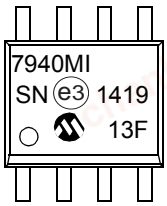
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

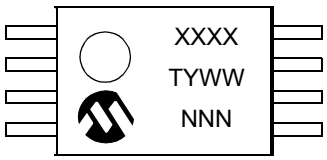
8-Lead SOIC (3.90 mm)



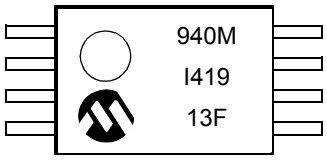
Example:



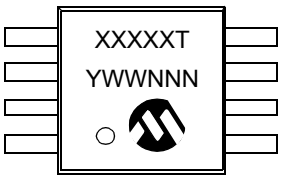
8-Lead TSSOP



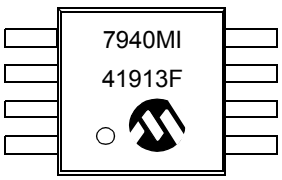
Example:



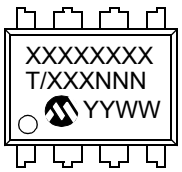
8-Lead MSOP



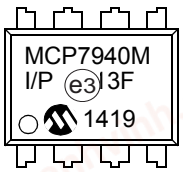
Example:



8-Lead PDIP (300 mil)



Example:



8-Lead 2x3 TDFN



Example:



Part Number	1st Line Marking Codes				
	SOIC	TSSOP	MSOP	TDFN	PDIP
MCP7940M	7940MT	940M	7940MT	AU1	MCP7940M

T = Temperature grade

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	JEDEC® designator for Matte Tin (Sn)
	*	This package is RoHs compliant. The JEDEC designator ((e3)) can be found on the outer packaging for this package.

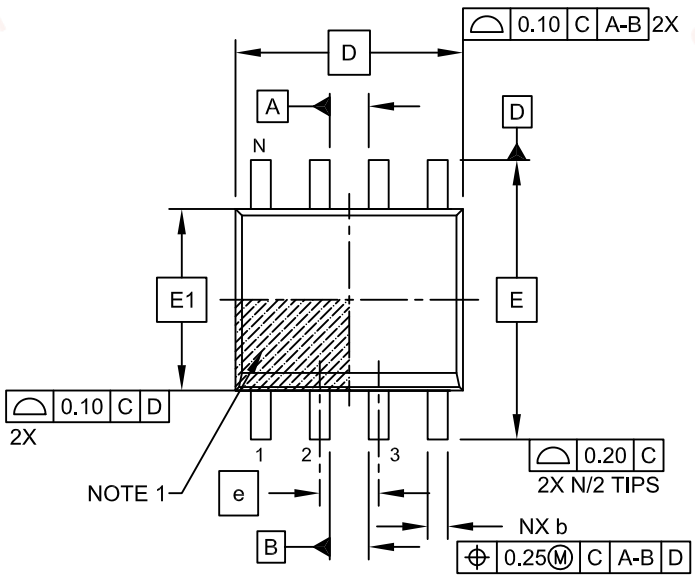
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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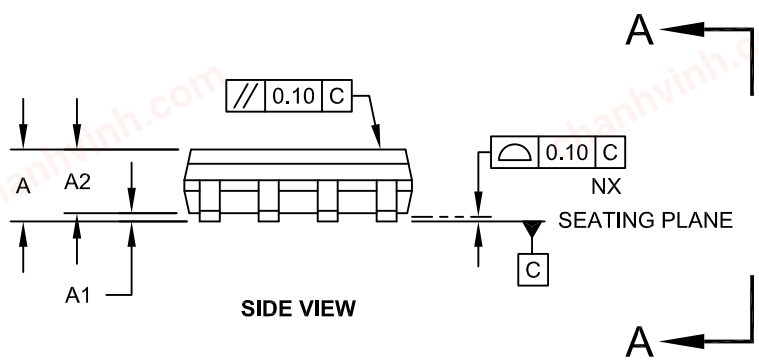
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8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

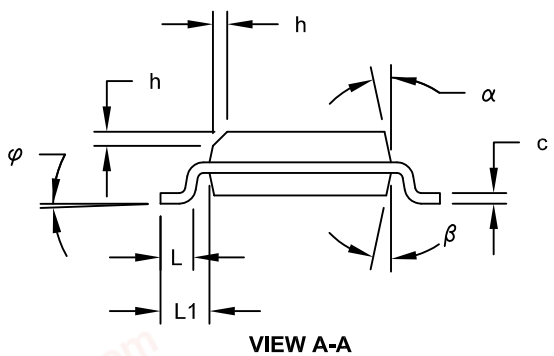
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



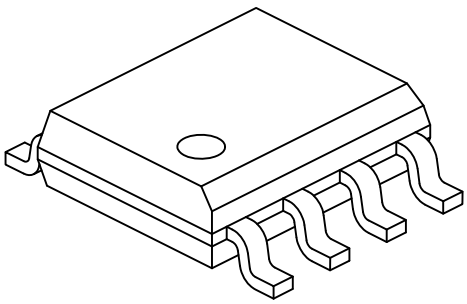
VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

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8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

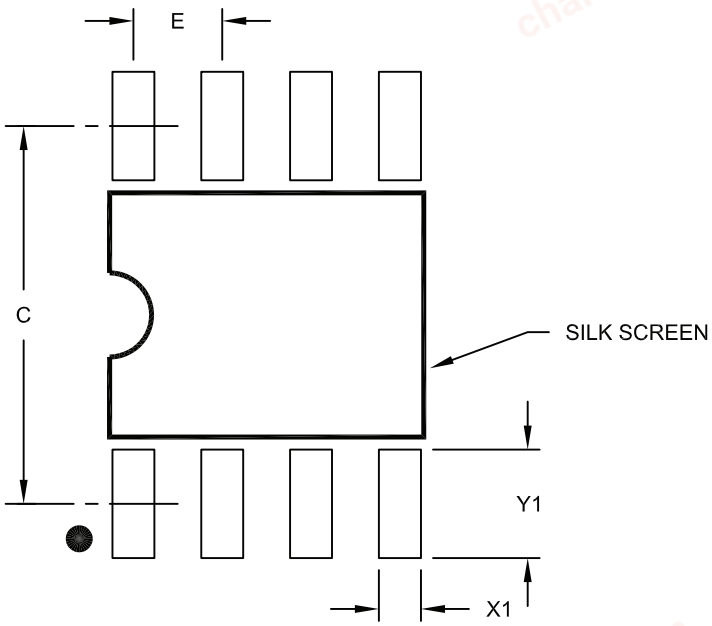
Microchip Technology Drawing No. C04-057C Sheet 2 of 2

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8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

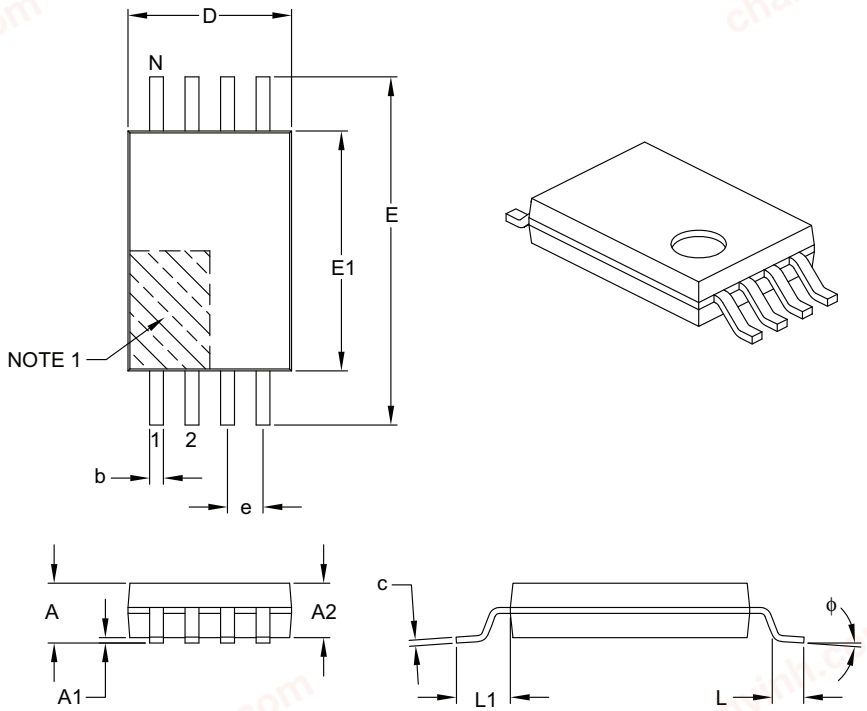
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

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8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

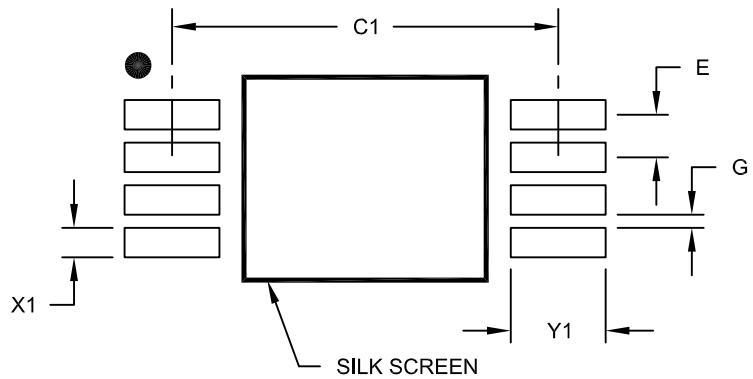
Microchip Technology Drawing C04-086B

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8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

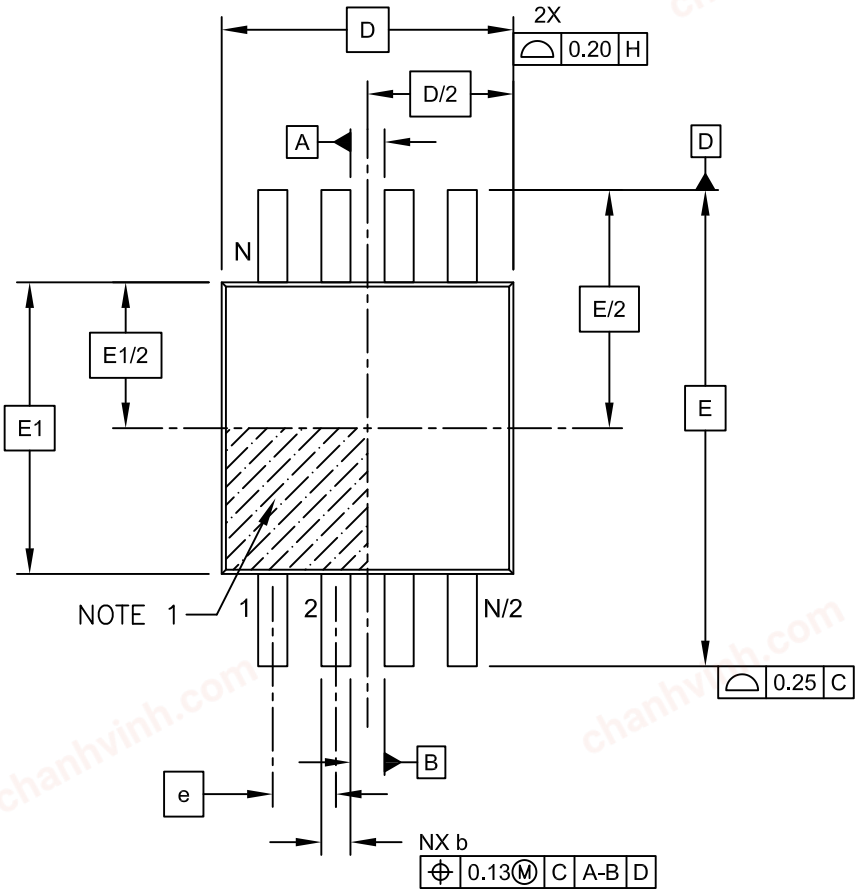
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8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



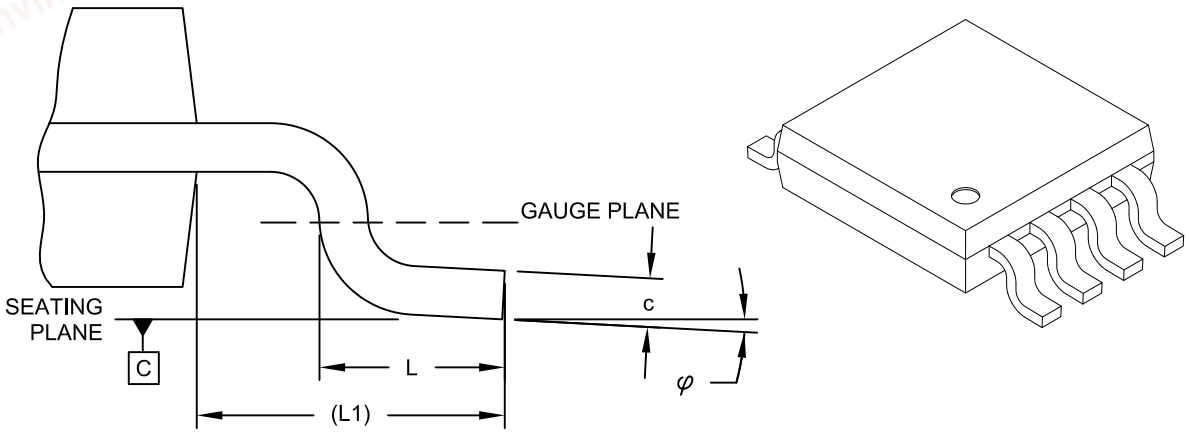
Microchip Technology Drawing C04-111C Sheet 1 of 2

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8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

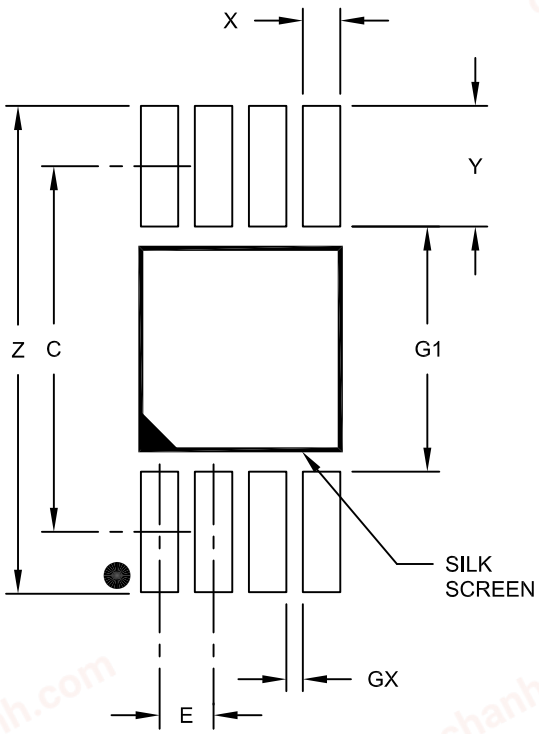
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8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

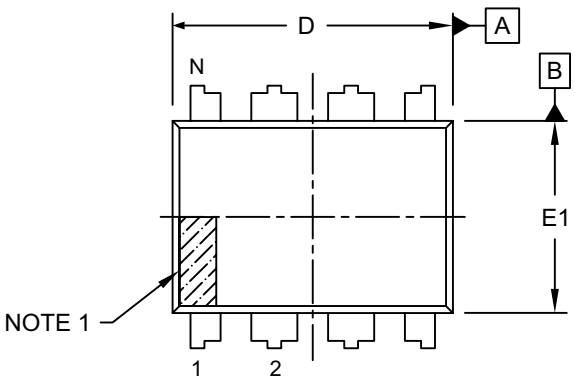
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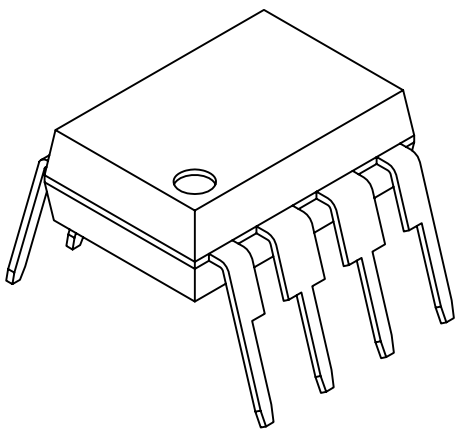
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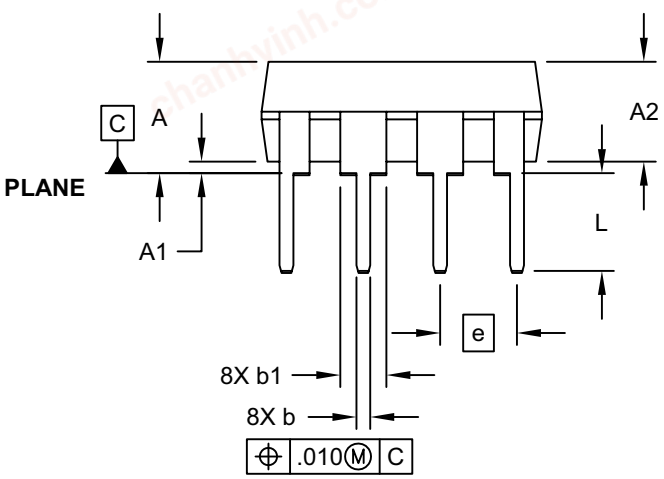
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

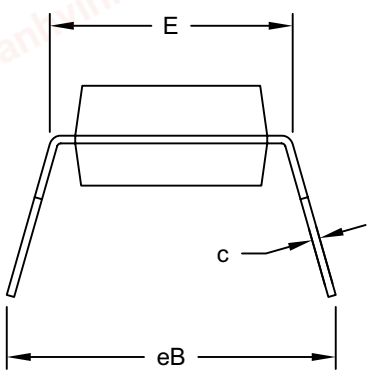


TOP VIEW





SIDE VIEW



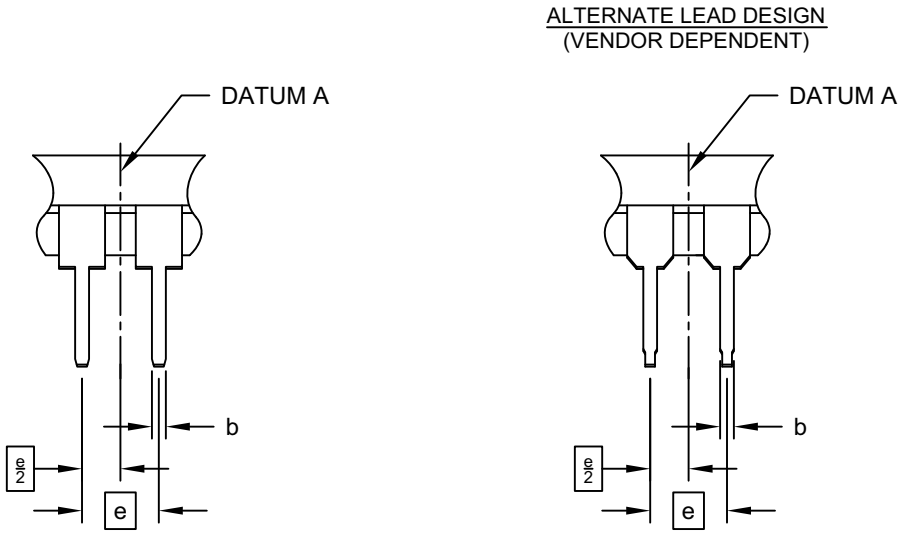
END VIEW

Microchip Technology Drawing No. C04-018D Sheet 1 of 2

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8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

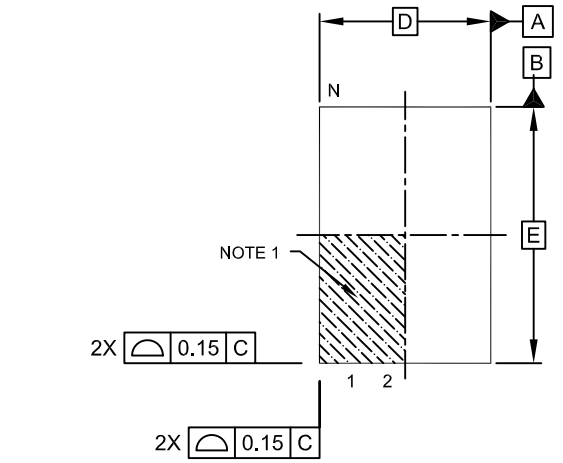
Microchip Technology Drawing No. C04-018D Sheet 2 of 2

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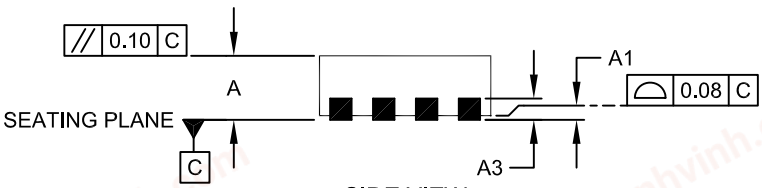
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8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

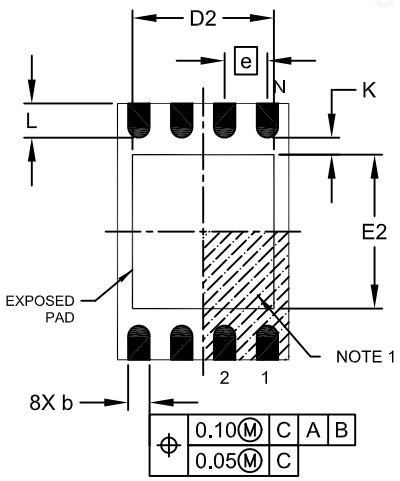
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



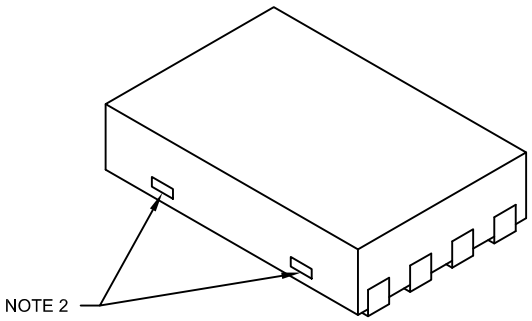
BOTTOM VIEW

Microchip Technology Drawing No. C04-129C

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8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

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Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.20	-	1.60
Exposed Pad Width	E2	1.20	-	1.60
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

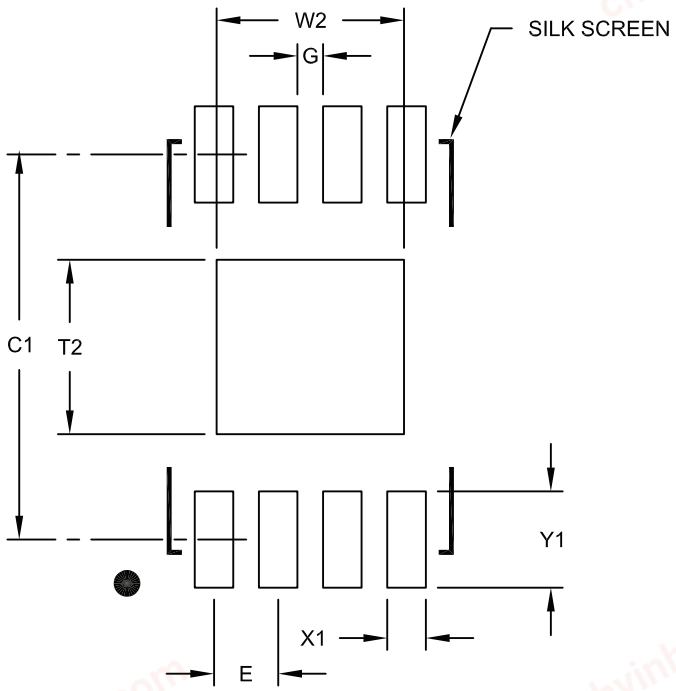
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8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			1.46
Optional Center Pad Length	T2			1.36
Contact Pad Spacing	C1		3.00	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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APPENDIX A: REVISION HISTORY

Revision A (02/2012)

Original release of this document.

Revision B (06/2014)

Updated overall content for improved clarity. Added detailed descriptions of registers. Updated block diagram and application schematic.

Defined names for all bits and registers, and renamed the bits shown in Table 6-1 for clarification.

Renamed the DC characteristics shown in Table 6-2 for clarification.

Updated 8-Lead PDIP Package.

TABLE 6-1: BIT NAME CHANGES

Old Bit Name	New Bit Name
OSCON	OSCRUN
LP	LPYR
SQWE	SQWEN
ALM0	ALM0EN
ALM1	ALM1EN
RS0	SQWFS0
RS1	SQWFS1
RS2	CRSTRIM
CALIBRATION	TRIMVAL<6:0>
ALM0POL	ALMPOL
ALM1POL	ALMPOL
ALM0C<2:0>	ALM0MSK<2:0>
ALM1C<2:0>	ALM1MSK<2:0>

TABLE 6-2: DC CHARACTERISTIC NAME CHANGES

Old Name	Old Symbol	New Name	New Symbol
Operating current SRAM	ICC Read	SRAM/RTCC register operating current	ICCREAD
	ICC Write		ICCWRITE
Operating current	IVCC	Timekeeping current	ICCT
Standby current	ICCS	VCC data retention current (oscillator off)	ICCDAT

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office. Not every possible ordering combination is listed below.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	MCP7940M =	1.8V - 5.5V I²C™ Serial RTCC
	MCP7940MT=	1.8V - 5.5V I²C Serial RTCC (Tape and Reel)
Temperature Range:	I =	-40°C to +85°C
Package:	SN =	8-Lead Plastic Small Outline (3.90 mm body)
	ST =	8-Lead Plastic Thin Shrink Small Outline (4.4 mm)
	MS =	8-Lead Plastic Micro Small Outline
	MNY(1) =	8-Lead Plastic Dual Flat, No Lead
	P =	8-Lead Plastic PDIP (300mil body)

Note 1: "Y" indicates a Nickel Palladium Gold (NiPdAu) finish.

Examples:

a) MCP7940M-I/SN: Industrial Temperature, SOIC package.

b) MCP7940MT-I/SN: Industrial Temperature, SOIC package, Tape and Reel.

c) MCP7940MT-I/MNY: Industrial Temperature, TDFN package, Tape and Reel

d) MCP7940M-I/P: Industrial Temperature, PDIP package.

e) MCP7940M-I/MS: Industrial Temperature MSOP package.

f) MCP7940M-I/ST: Industrial Temperature, TSSOP package.

g) MCP7940MT-I/ST: Industrial Temperature, TSSOP package, Tape and Reel.

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