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# MCP41U83

## 10-Bit Single-Channel Digital Potentiometers with Selectable SPI/I²C Serial Interface

### Features

- Single-Channel Digital Potentiometers
- 10-Bit Resolution:
  1,023 Resistors (1,024 Steps) Zero to Full Scale
- Resistance Options:
  - MCP41U83-502: 5 kΩ
  - MCP41U83-103: 10 kΩ
  - MCP41U83-203: 20 kΩ
  - MCP41U83-503: 50 kΩ
  - MCP41U83-104: 100 kΩ
- Flexible Power Supply Options:
  - Single Voltage Rail: 2.7V to 5.5V
    ($V_{DD}$ – $V_{SS}$ where DGND = $V_{SS}$ = 0V)
  - Dual Voltage Rail: ±2.25V to ±2.75V
    ($V_{DD}$ – $V_{SS}$ where DGND = 0V)
- Multiple-Time Programmable (MTP) Nonvolatile (NV) Memory with 1,000 Write Cycles
- User-Selectable Serial Interface Using a Dedicated Hardware Pin:
  - SPI: 20 MHz Read/Write Operation
  - I²C: 100 kHz, 400 kHz, 1.7 MHz and 3.4 MHz Communication Speeds
- Resistor Network Terminal Disconnect
- Can Be Configured as Potentiometer or Rheostat
- Cyclic Redundancy Check (CRC) for Robust Communication; Software CRC Enable/Disable
- SPI Daisy-Chain Support for up to 128 devices
- Dedicated Commands for Software Reset
- Device Status Indication Using Internal Register
- Configuration Lock Bits Can Be Modified Using Software Commands
- Dedicated Register Bits to Select How to Update Wipers: Independently or Synchronously
- Dedicated Bit to Latch Wiper Values and Trigger Output Update
- 3 General Purpose MTP Memory Locations for Storing Custom Data
- Counter Registers to Track Number of MTP Writes to Wiper and GP Data Registers
- Extended Temperature Range: -40°C to +125°C
- AEC-Q100 Qualified (Automotive Applications)
- Package Types:
  - 14-Lead TSSOP (4.4 mm Body)
  - 16-Lead VQFN (4x4 mm Body)

### General Description

MCP41U83 devices are 10-bit single-channel digital potentiometers, having both volatile and nonvolatile MTP memory with 1,000 write cycles.

The features provided by MCP41U83 facilitate device integration into automotive and industrial applications.

MCP41U83 can have either a single-ended or a dual power supply without requiring any initial configuration. Configuring the operating mode in a dedicated register allows MCP41U83 to be used either as a potentiometer or as a rheostat (variable resistor). The internal resistor ladder has 1,023 resistors with 1,024 wiper connection points, from zero to full scale.

All three terminals (A, B and W) can be independently disconnected from the resistor ladder to reduce power consumption or to configure the part as a potentiometer or as a rheostat.

For the serial communication interface, select between Serial Peripheral Interface (SPI) and Inter-Integrated Circuit (I²C) using a single device pin – SPI2C.

Use the A0 and A1 hardware pins to configure the I²C address. These pins control the last two bits of the standard 7-bit I²C address.

Use SPI to connect several MCP41U83 devices in Daisy-Chain mode.

Both SPI and I²C have internal CRC modules to support hardware data integrity checks.

A special register shows the status of MCP41U83 in real-time. A series of dedicated commands can reset the device to a known state or force reinitialization. This ensures full user control of the initialization sequence and that proper steps can be taken based on the real status of the system.

MCP41U83 devices are AEC-Q100 Grade-1 qualified for automotive applications.

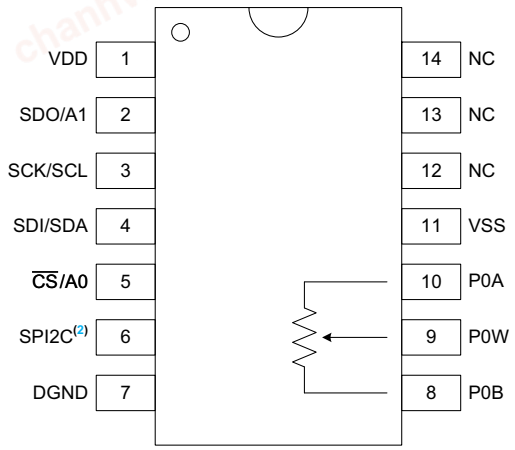
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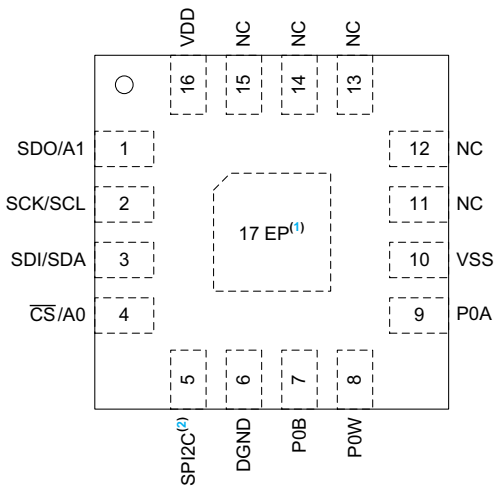
# MCP41U83

## Package Types (Top View)

**MCP41U83**
14-Lead TSSOP (4.4 mm)




**MCP41U83**
16-Lead VQFN (4x4 mm)




**NOTES**:
1. Includes Exposed Thermal Pad (EP).
2. Serial interface type is configurable using the SPI2C pin.

## MCP41U83 Device Characteristics

| Device | End-to-End Resistance (typical) $R_{AB}$ (1) (kΩ) | Package Type | Number of Channels | Number of Taps | Memory | POR Wiper Setting | $V_{DD}$ Operating Range (2) (V) |
|---|---|---|---|---|---|---|---|
| MCP41U83-502 | 5 | 14-Lead TSSOP, 16-Lead VQFN | 1 | 1,024 | RAM/MTP | 200h | 2.7 to 5.5 |
| MCP41U83-103 | 10 | | | | | | |
| MCP41U83-203 | 20 | | | | | | |
| MCP41U83-503 | 50 | | | | | | |
| MCP41U83-104 | 100 | | | | | | |

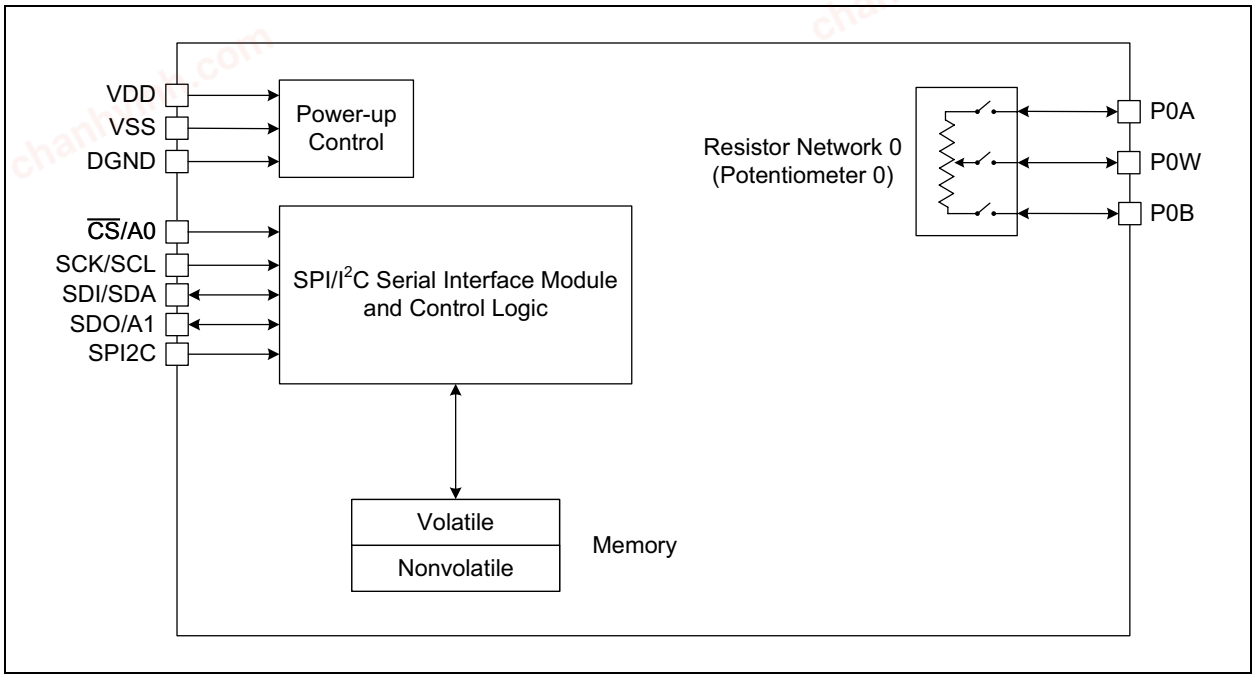
**Note 1:** Floating either terminal A or terminal B allows MCP41U83 to be used as a rheostat (variable resistor).
**2:** MCP41U83 also supports ±2.25V to ±2.75V when the DGND pin is set midpoint between $V_{DD}$ and $V_{SS}$.


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## Functional Block Diagram




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# 1.0 ELECTRICAL SPECIFICATIONS

## 1.1 Absolute Maximum Ratings†

Voltage on VDD pin with respect to VSS pin . . . . . -0.6V to +6.5V
Voltage on VSS pin with respect to DGND pin . . . . . DGND + 0.6V to DGND – 6.5V
Voltage on VDD pin with respect to DGND pin . . . . . DGND – 0.6V to DGND + 6.5V
Voltage on SCL, SDA, A0 and A1 pins with respect to DGND pin . . . . . DGND – 0.6V to DGND + 6.5V
Voltage on SCK, SDI and NC pins with respect to DGND pin . . . . . DGND – 0.6V to DGND + 6.5V
Voltage on all other pins (P0A, P0W and P0B) with respect to VSS pin . . . . . -0.6V to $V_{DD}$ + 0.6V
Maximum current into supply pins . . . . . ±20 mA
Maximum $I_W$ current into P0A, P0W and P0B pins (continuous) . . . . . ±3 mA

Package Power Dissipation ($P_{DIS}$) (*):

14-Lead TSSOP . . . . . 946 mW
16-Lead VQFN . . . . . 3040 mW

Electrostatic Discharge (ESD) Protection on all pins:

Human Body Model (HBM) . . . . . ≥ ±2 kV
Charge Device Model (CDM) . . . . . ≥ ±2 kV

Latch-up (per JEDEC JESD78A) at +125°C . . . . . ± 100 mA

Storage Temperature ($T_{STG}$) . . . . . -65°C to +150°C
Ambient Temperature under Bias ($T_A$) . . . . . -40°C to +125°C
Maximum Junction Temperature ($T_J$) . . . . . +150°C
Soldering Temperature of Leads (10 seconds) . . . . . +300°C

* Power Dissipation ($P_{DIS}$) is calculated using Equation 1-1, for $T_A$ = +50°C and $T_J$ = +150°C.

**EQUATION 1-1:**

$$P_{DIS} = V_{DD} \times (I_{DD} - \sum I_{OH}) + \sum [I_{OH} \times (V_{DD} - V_{OH})] + \sum (V_{OL} \times I_{OL})$$

Where:

$P_{DIS}$ = Power Dissipation (mW)
$V_{DD}$ = Supply Voltage (V)
$I_{DD}$ = Supply Current (mA)
$V_{OH}$ = Output High Voltage (V)
$I_{OH}$ = Output High Current (mA)
$V_{OL}$ = Output Low Voltage (V)
$I_{OL}$ = Output Low Current (mA)

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these, or any other conditions above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.


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## 1.2 Electrical Characteristics

### TABLE 1-1: DC SPECIFICATIONS

**Standard Operating Conditions:** Unless otherwise indicated, $T_A$ = -40°C to +125°C (extended temperature), $V_{DD}$ = 2.7V to 5.5V, DGND = 0V, $V_{SS}$ = 0V. All parameters apply across the specified operating ranges unless noted. Typical characteristics represent values for $V_{DD}$ = 5.5V, DGND = 0V, $V_{SS}$ = 0V and $T_A$ = +25°C.

| Parameter | Symbol | Min. | Typical | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| Single Supply Range | $V_{DD}$ | 2.7 | — | 5.5 | V | DGND = 0V, $V_{SS}$ = 0V |
| Dual Supply Range | $V_{DD}$ | 2.25 | — | 2.75 | V | DGND = 0V |
| | $V_{SS}$ | -2.25 | — | -2.75 | V | DGND = 0V |
| VDD (Rising) to Ensure Device POR | $V_{POR}$ | | | | | RAM Retention Voltage ($V_{RAM}$) < $V_{POR}$ |
| | | — | — | 2.6 | V | Single Supply. $V_{DD}$ > DGND = $V_{SS}$ |
| | | — | — | 2.25(1) | V | Dual Supply. $V_{DD}$ > DGND > $V_{SS}$ |
| Supply Current | $I_{DD}$ | — | 1 | 2 | µA | Serial communication inactive |
| | $I_{DD,NV_Write}$ | — | 15 | — | mA | During nonvolatile (NV) write only. Digital inputs = VDD or DGND (Note 1) |
| **Potentiometer** | | | | | | |
| Resolution (Note 1) | N | — | — | 10 | bits | 1,024 Taps. Potentiometer or Rheostat operating mode. |
| End-to-End Resistance | $R_{AB}$ | 4.5 | 5 | 5.5 | kΩ | MCP41U83-502 devices |
| | | 9 | 10 | 11 | kΩ | MCP41U83-103 devices |
| | | 18 | 20 | 22 | kΩ | MCP41U83-203 devices |
| | | 45 | 50 | 55 | kΩ | MCP41U83-503 devices |
| | | 90 | 100 | 110 | kΩ | MCP41U83-104 devices |
| Integral Nonlinearity Error | P-INL | -1 | — | 1 | LSb | P0A = $V_{DD}$, P0B = $V_{SS}$, Unloaded |
| Differential Nonlinearity Error | P-DNL | -1 | — | 1 | LSb | P0A = $V_{DD}$, P0B = $V_{SS}$, Unloaded |
| Full Scale Error | FSE | -10 | -5 | 0 | LSb | $R_{AB}$ = 5 kΩ; P0A = $V_{DD}$, P0B = $V_{SS}$, Unloaded, Code = full-scale |
| | | -5 | -2.5 | 0 | LSb | $R_{AB}$ = 10 kΩ |
| | | -2.5 | -1 | 0 | LSb | $R_{AB}$ = 20 kΩ |
| | | -1.25 | -0.4 | 0 | LSb | $R_{AB}$ = 50 kΩ |
| | | -1 | -0.35 | 0 | LSb | $R_{AB}$ = 100 kΩ |
| Zero Scale Error | ZSE | 0 | 4 | 10 | LSb | $R_{AB}$ = 5 kΩ; P0A = $V_{DD}$, P0B = $V_{SS}$, Unloaded, Code = zero-scale |
| | | 0 | 2 | 4 | LSb | $R_{AB}$ = 10 kΩ |
| | | 0 | 1 | 2 | LSb | $R_{AB}$ = 20 kΩ |
| | | 0 | 0.5 | 1.25 | LSb | $R_{AB}$ = 50 kΩ |
| | | 0 | 0.4 | 1 | LSb | $R_{AB}$ = 100 kΩ |
| Nominal Resistance Temperature Coefficient (Note 2) | P-$R_{TC}$ | — | 43 | — | ppm/°C | $R_{AB}$ = 5 kΩ; P0A = $V_{DD}$, P0B = $V_{SS}$, Unloaded, Code = midscale |
| | | — | 25 | — | ppm/°C | $R_{AB}$ = 10 kΩ |
| | | — | 12 | — | ppm/°C | $R_{AB}$ = 20 kΩ |
| | | — | 10 | — | ppm/°C | $R_{AB}$ = 50 kΩ |
| | | — | 9 | — | ppm/°C | $R_{AB}$ = 100 kΩ |

**Note 1:** Not production tested. Parameter ensured by design.
**2:** Not production tested. Parameter ensured by characterization.

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**TABLE 1-1: DC SPECIFICATIONS (CONTINUED)**

**Standard Operating Conditions:** Unless otherwise indicated, $T_A$ = -40°C to +125°C (extended temperature), $V_{DD}$ = 2.7V to 5.5V, DGND = 0V, $V_{SS}$ = 0V. All parameters apply across the specified operating ranges unless noted. Typical characteristics represent values for $V_{DD}$ = 5.5V, DGND = 0V, $V_{SS}$ = 0V and $T_A$ = +25°C.

| Parameter | Symbol | Min. | Typical | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Potentiometer (continued)** | | | | | | |
| Ratiometric Temperature Coefficient (Note 2) | $V_{TC}$ | — | 2.2 | — | ppm/°C | $R_{AB}$ = 5 kΩ; P0A = $V_{DD}$, P0B = $V_{SS}$, Unloaded, Code = midscale |
| | | — | 2.5 | — | ppm/°C | $R_{AB}$ = 10 kΩ |
| | | — | 2.6 | — | ppm/°C | $R_{AB}$ = 20 kΩ |
| | | — | 0.7 | — | ppm/°C | $R_{AB}$ = 50 kΩ |
| | | — | 1.1 | — | ppm/°C | $R_{AB}$ = 100 kΩ |
| Power Supply Sensitivity (Note 1) | PSS | — | 0.0005 | 0.0046 | %/% | P0A = 2.7V, P0B = $V_{SS}$, $V_{DD}$ = 2.7V to 5.5V, Unloaded, Code = midscale |
| **Rheostat** | | | | | | |
| Wiper-to-End Resistance | $R_{WB}$ | 4.5 | 5 | 5.5 | kΩ | MCP41U83-502 devices only |
| | | 9 | 10 | 11 | kΩ | MCP41U83-103 devices only |
| | | 18 | 20 | 22 | kΩ | MCP41U83-203 devices only |
| | | 45 | 50 | 55 | kΩ | MCP41U83-503 devices only |
| | | 90 | 100 | 110 | kΩ | MCP41U83-104 devices only |
| Wiper Resistance | $R_W$ | — | 19 | 40 | Ω | $R_{AB}$ = 5 kΩ; P0B = $V_{SS}$, $I_W = (V_{DD} - 1)/R_{WB_TYP}$, Code = zero-scale |
| | | — | 19 | 40 | Ω | $R_{AB}$ = 10 kΩ |
| | | — | 19 | 40 | Ω | $R_{AB}$ = 20 kΩ |
| | | — | 32 | 60 | Ω | $R_{AB}$ = 50 kΩ |
| | | — | 32 | 60 | Ω | $R_{AB}$ = 100 kΩ |
| Integral Nonlinearity Error (Note 2) | R-INL | -2 | — | 2 | LSb | P0B = $V_{SS}$, $I_W = (V_{DD} - 1)/R_{WB_TYP}$ |
| Differential Nonlinearity Error (Note 2) | R-DNL | -1 | — | 1 | LSb | P0B = $V_{SS}$, $I_W = (V_{DD} - 1)/R_{WB_TYP}$ |
| Nominal Resistance Temperature Coefficient (Note 2) | R-$R_{TC}$ | — | 42 | — | ppm/°C | $R_{AB}$ = 5 kΩ; P0B = $V_{SS}$, Code = full-scale |
| | | — | 23 | — | ppm/°C | $R_{AB}$ = 10 kΩ |
| | | — | 9 | — | ppm/°C | $R_{AB}$ = 20 kΩ |
| | | — | 7 | — | ppm/°C | $R_{AB}$ = 50 kΩ |
| | | — | 5 | — | ppm/°C | $R_{AB}$ = 100 kΩ |
| Power Supply Rejection Ratio (Note 1) | PSRR | — | -51 | — | dB | $R_{AB}$ = 5 kΩ; $I_W$ = 2.7V/$R_{WB}$, P0B = $V_{SS}$, $V_{DD}$ = 2.7V to 5.5V, Code = midscale |
| | | — | -57 | — | dB | $R_{AB}$ = 10 kΩ |
| | | — | -64 | — | dB | $R_{AB}$ = 20 kΩ |
| | | — | -66 | — | dB | $R_{AB}$ = 50 kΩ |
| | | — | -74 | — | dB | $R_{AB}$ = 100 kΩ |

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**TABLE 1-1: DC SPECIFICATIONS (CONTINUED)**

**Standard Operating Conditions:** Unless otherwise indicated, $T_A$ = -40°C to +125°C (extended temperature), $V_{DD}$ = 2.7V to 5.5V, DGND = 0V, $V_{SS}$ = 0V. All parameters apply across the specified operating ranges unless noted. Typical characteristics represent values for $V_{DD}$ = 5.5V, DGND = 0V, $V_{SS}$ = 0V and $T_A$ = +25°C.

| Parameter | Symbol | Min. | Typical | Max. | Units | Conditions | |
|---|---|---|---|---|---|---|---|
| **Dynamic Characteristics** | | | | | | | |
| -3dB Bandwidth (Note 1) | BW | — | 1166 | — | MHz | $R_{AB}$ = 5 kΩ | P0A - P0B = ±1 $V_{P-P}$, P0B - $V_{SS}$ = 2.75V, $C_L$ = 10 pF, Code = midscale |
| | | — | 586 | — | MHz | $R_{AB}$ = 10 kΩ | |
| | | — | 294 | — | MHz | $R_{AB}$ = 20 kΩ | |
| | | — | 166 | — | MHz | $R_{AB}$ = 50 kΩ | |
| | | — | 83 | — | MHz | $R_{AB}$ = 100 kΩ | |
| Total Harmonic Distortion (Note 1) | THD | — | 0.0063 | — | % | $R_{AB}$ = 5 kΩ | P0A = 1 $V_{RMS}$ at $f$ = 1 kHz, P0B = $V_{SS}$, Code = midscale |
| | | — | 0.0037 | — | % | $R_{AB}$ = 10 kΩ | |
| | | — | 0.0041 | — | % | $R_{AB}$ = 20 kΩ | |
| | | — | 0.0047 | — | % | $R_{AB}$ = 50 kΩ | |
| | | — | 0.0088 | — | % | $R_{AB}$ = 100 kΩ | |
| Resistor Noise Density (Note 1) | $E_{NWB}$ | — | 4.6 | — | nV/√Hz | $R_{AB}$ = 5 kΩ | P0A = $V_{DD}$, P0B = $V_{SS}$, $f$ = 1 kHz, Unloaded, Code = midscale |
| | | — | 6.4 | — | nV/√Hz | $R_{AB}$ = 10 kΩ | |
| | | — | 9.1 | — | nV/√Hz | $R_{AB}$ = 20 kΩ | |
| | | — | 14.3 | — | nV/√Hz | $R_{AB}$ = 50 kΩ | |
| | | — | 20.2 | — | nV/√Hz | $R_{AB}$ = 100 kΩ | |
| **Wiper Terminals (P0A, P0W, P0B)** | | | | | | | |
| Leakage Current | $I_L$ | -1 | — | 1 | µA | P0A = $V_{SS}$, P0W = $V_{SS}$ (Potentiometer configuration only) | |
| | | -1 | — | 1 | µA | P0B = $V_{SS}$ (Rheostat configuration only) | |
| P0A Pin Capacitances (Note 2) | $C_A$ | — | 90 | — | pF | $R_{AB}$ = 5 kΩ | Code = midscale |
| | | — | 90 | — | pF | $R_{AB}$ = 10 kΩ | |
| | | — | 90 | — | pF | $R_{AB}$ = 20 kΩ | |
| | | — | 56 | — | pF | $R_{AB}$ = 50 kΩ | |
| | | — | 56 | — | pF | $R_{AB}$ = 100 kΩ | |
| P0W Pin Capacitances (Note 2) | $C_W$ | — | 150 | — | pF | $R_{AB}$ = 5 kΩ | |
| | | — | 150 | — | pF | $R_{AB}$ = 10 kΩ | |
| | | — | 150 | — | pF | $R_{AB}$ = 20 kΩ | |
| | | — | 78 | — | pF | $R_{AB}$ = 50 kΩ | |
| | | — | 78 | — | pF | $R_{AB}$ = 100 kΩ | |
| P0B Pin Capacitances (Note 2) | $C_B$ | — | 90 | — | pF | $R_{AB}$ = 5 kΩ | |
| | | — | 90 | — | pF | $R_{AB}$ = 10 kΩ | |
| | | — | 90 | — | pF | $R_{AB}$ = 20 kΩ | |
| | | — | 56 | — | pF | $R_{AB}$ = 50 kΩ | |
| | | — | 56 | — | pF | $R_{AB}$ = 100 kΩ | |

**Note 1:** Not production tested. Parameter ensured by design.
**2:** Not production tested. Parameter ensured by characterization.

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### TABLE 1-1: DC SPECIFICATIONS (CONTINUED)

**Standard Operating Conditions:** Unless otherwise indicated, $T_A$ = -40°C to +125°C (extended temperature), $V_{DD}$ = 2.7V to 5.5V, DGND = 0V, $V_{SS}$ = 0V. All parameters apply across the specified operating ranges unless noted. Typical characteristics represent values for $V_{DD}$ = 5.5V, DGND = 0V, $V_{SS}$ = 0V and $T_A$ = +25°C.

| Parameter | Symbol | Min. | Typical | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Digital Inputs/Outputs (SCL, SCA, A0, A1)** | | | | | | |
| High Input Threshold | $V_{IH}$ | 0.7 x $V_{DD}$ | — | — | V | |
| Low Input Threshold | $V_{IL}$ | — | — | 0.3 x $V_{DD}$ | V | |
| Output Low Voltage (SDA) | $V_{OL}$ | — | — | 0.4 | V | $V_{DD}$ > 2V, $I_{OL}$ = 3 mA |
| Input Leakage Current | $I_{IL}$ | -1 | — | 1 | µA | $V_{IN}$ = $V_{DD}$, $V_{IN}$ = DGND |
| Pin Capacitance (**Note 2**) | $C_{IN}$ | — | 15 | — | pF | |
| **Digital Inputs (SPI2C, SCK, SDI, $\overline{CS}$)** | | | | | | |
| High Input Threshold | $V_{IH}$ | 0.45 x $V_{DD}$ | — | — | V | |
| Low Input Threshold | $V_{IL}$ | — | — | 0.15 x $V_{DD}$ | V | |
| Input Leakage Current | $I_{IL}$ | -1 | — | 1 | µA | $V_{IN}$ = $V_{DD}$, $V_{IN}$ = DGND |
| Pin Capacitance (**Note 2**) | $C_{IN}$, $C_{OUT}$ | — | 15 | — | pF | |
| **Digital Outputs (SDO)** | | | | | | |
| Output Low Voltage | $V_{OL}$ | DGND | — | 0.3 x $V_{DD}$ | V | $I_{OL}$ = 200 µA |
| Output High Voltage | $V_{OH}$ | 0.7 x $V_{DD}$ | — | $V_{DD}$ | V | $I_{OH}$ = -200 µA |
| Pin Capacitance (**Note 2**) | $C_{OUT}$ | — | 40 | — | pF | |
| **Nonvolatile Memory Reliability** | | | | | | |
| Endurance (**Note 2**) | $TP_{END}$ | — | — | 1,000 | Cycles | All NV registers |
| Data Retention (**Note 2**) | $TP_{DR}$ | — | — | 10 | Years | $T_A$ = +125°C |

**Note 1:** Not production tested. Parameter ensured by design.
**2:** Not production tested. Parameter ensured by characterization.

### TABLE 1-2: TEMPERATURE SPECIFICATIONS

**Standard Operating Conditions:** Unless otherwise indicated, $T_A$ = -40°C to +125°C (extended temperature), $V_{DD}$ = 2.7V to 5.5V, DGND = 0V, $V_{SS}$ = 0V. All parameters apply across the specified operating ranges unless noted. Typical characteristics represent values for $V_{DD}$ = 5.5V, DGND = 0V, $V_{SS}$ = 0V and $T_A$ = +25°C.

| Parameter | Symbol | Min. | Typical | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Temperature Ranges** | | | | | | |
| Specified Temperature Range | $T_A$ | -40 | — | +125 | °C | |
| Operating Temperature Range | $T_{OP}$ | -40 | — | +125 | °C | |
| Storage Temperature Range | $T_{STG}$ | -65 | — | +150 | °C | |
| **Thermal Package Resistances** | | | | | | |
| Thermal Resistance, 14-Lead TSSOP | $\theta_{JA}$ | — | 105.7 | — | °C/W | |
| Thermal Resistance, 16-Lead VQFN | $\theta_{JA}$ | — | 32.9 | — | °C/W | |


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## 1.3 General Timing Characteristics

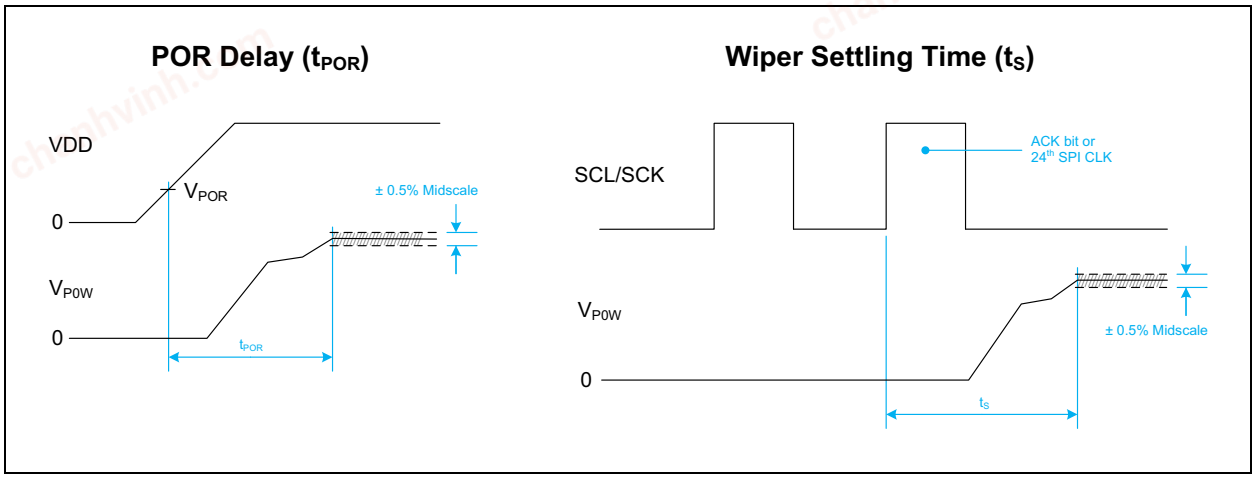



**FIGURE 1-1:** *General Timing Characteristics.*

**TABLE 1-3: GENERAL TIMING CHARACTERISTICS**

**Standard Operating Conditions:** Unless otherwise indicated, $T_A$ = -40°C to +125°C (extended temperature), $V_{DD}$ = 2.7V to 5.5V, DGND = 0V, $V_{SS}$ = 0V. All parameters apply across the specified operating ranges unless noted. Typical characteristics represent values for $V_{DD}$ = 5.5V, DGND = 0V, $V_{SS}$ = 0V and $T_A$ = +25°C.

| Parameter | Symbol | Min. | Typical | Max. | Units | Conditions | |
|---|---|---|---|---|---|---|---|
| POR Delay (**Note 1**, **2**) | $t_{POR}$ | — | — | 400 | µs | P0A = $V_{DD}$, P0B = $V_{SS}$, Unloaded | |
| Write NV Address (**Note 1**) | $t_{WriteNV}$ | — | 10 | 100 | ms | | |
| Wiper Settling Time (**Note 1**) | $t_S$ | — | 1.3 | — | µs | $R_{AB}$ = 5 kΩ | P0A = $V_{DD}$, P0B = $V_{SS}$, $C_{LOAD}$ = 10 pF, From code = 0 to midscale (**Note 3**) |
| | | — | 2.3 | — | µs | $R_{AB}$ = 10 kΩ | |
| | | — | 4.3 | — | µs | $R_{AB}$ = 20 kΩ | |
| | | — | 9.7 | — | µs | $R_{AB}$ = 50 kΩ | |
| | | — | 21 | — | µs | $R_{AB}$ = 100 kΩ | |

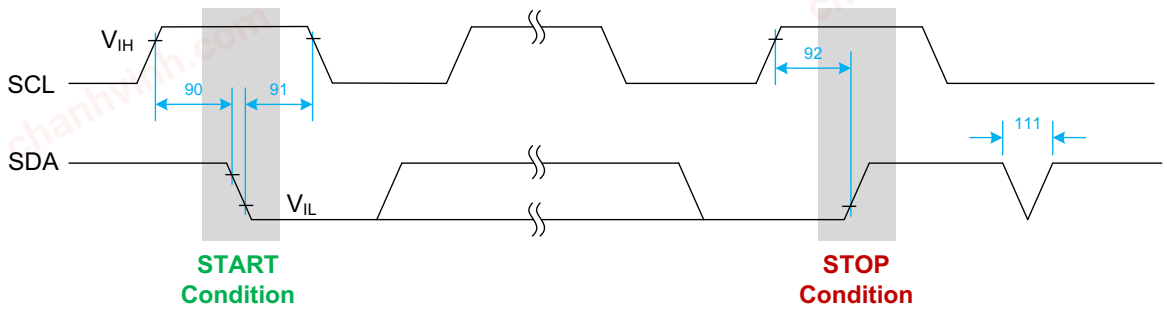
**Note 1:** Not production tested. Parameter ensured by characterization.
**2:** Measured from $V_{POR}$ threshold to ±0.5% of midscale value.
**3:** Measure from the last byte's 8th rising edge of the clock cycle to ±0.5% of midscale value.

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## 1.4 I²C Timing Characteristics




**NOTE:** All values are referred to $V_{IH}$ and $V_{IL}$ levels.

**FIGURE 1-2:** *I²C Bus Start/Stop Bits Timing Waveforms.*

**TABLE 1-4: I²C BUS START/STOP BITS TIMING CHARACTERISTICS**

**Standard Operating Conditions:** Unless otherwise indicated, $T_A$ = -40°C to +125°C (extended temperature). The operating voltage range is described in the **DC Specifications** table.

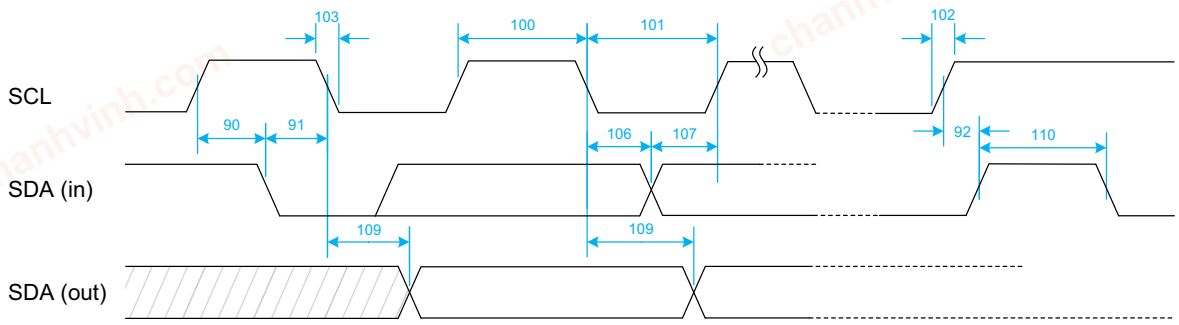
| Parameter | Symbol | Characteristic | Mode | Min. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|
| — | $f_{SCL}$ | I²C Frequency | Standard mode | — | 100 | kHz | $C_B$ = 400 pF, $V_{DD}$ = 2.7V to 5.5 V (**Note 1**) |
| | | | Fast mode | — | 400 | kHz | $C_B$ = 400 pF, $V_{DD}$ = 2.7V to 5.5 V |
| | | | High Speed 1.7 | — | 1.7 | MHz | $C_B$ = 400 pF, $V_{DD}$ = 4.5V to 5.5 V (**Note 1**) |
| | | | High Speed 3.4 | — | 3.4 | MHz | $C_B$ = 100 pF, $V_{DD}$ = 4.5V to 5.5 V (**Note 1**) |
| 90 | $t_{SU:STA}$ | Setup Time for repeated START condition | Standard mode | 4,700 | — | ns | **Note 1** |
| | | | Fast mode | 600 | — | ns | |
| | | | High Speed 1.7 | 160 | — | ns | **Note 1** |
| | | | High Speed 3.4 | 160 | — | ns | **Note 1** |
| 91 | $t_{HD:STA}$ | Hold Time for repeated START condition | Standard mode | 4,000 | — | ns | After this period, the first clock pulse is generated. **Note 1** |
| | | | Fast mode | 600 | — | ns | After this period, the first clock pulse is generated. |
| | | | High Speed 1.7 | 160 | — | ns | **Note 1** |
| | | | High Speed 3.4 | 160 | — | ns | **Note 1** |
| 92 | $t_{SU:STO}$ | Setup Time for STOP condition | Standard mode | 4,000 | — | ns | **Note 1** |
| | | | Fast mode | 600 | — | ns | |
| | | | High Speed 1.7 | 160 | — | ns | **Note 1** |
| | | | High Speed 3.4 | 160 | — | ns | **Note 1** |
| 111 | $t_{SP}$ | Pulse width of spikes that the input filter must suppress | Standard mode | — | 50 | ns | **Note 1** |
| | | | Fast mode | — | 50 | ns | |
| | | | High Speed 1.7 | — | 10 | ns | **Note 1** |
| | | | High Speed 3.4 | — | 10 | ns | **Note 1** |

**Note 1:** Not production tested. Parameter ensured by characterization.


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**NOTE:** All values are referred to $V_{IH}$ and $V_{IL}$ levels.

**FIGURE 1-3:** *$I^2C$ Bus Data Timing Waveforms.*

**TABLE 1-5: $I^2C$ BUS DATA TIMING CHARACTERISTICS**

| **Standard Operating Conditions:** Unless otherwise indicated, $T_A$ = -40°C to +125°C (extended temperature). The operating voltage range is described in the **DC Specifications** table. | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Characteristic** | **Mode** | **Min.** | **Max.** | **Units** | **Conditions** |
| 90 | $t_{SU:STA}$ | For details, see **Table 1-4, "I2C Bus Start/Stop Bits Timing Characteristics"**. | | | | | |
| 91 | $t_{HD:STA}$ | | | | | | |
| 92 | $t_{SU:STO}$ | | | | | | |
| 100 | $t_{HIGH}$ | SCL Clock High Period | Standard mode | 4,000 | — | ns | **Note 1** |
| | | | Fast mode | 600 | — | ns | |
| | | | High Speed 1.7 | 120 | — | ns | **Note 1** |
| | | | High Speed 3.4 | 60 | — | ns | **Note 1** |
| 101 | $t_{LOW}$ | SCL Clock Low Period | Standard mode | 4,700 | — | ns | **Note 1** |
| | | | Fast mode | 1,300 | — | ns | |
| | | | High Speed 1.7 | 320 | — | ns | **Note 1** |
| | | | High Speed 3.4 | 160 | — | ns | **Note 1** |

**Note 1:** Not production tested. Parameter ensured by characterization.

**2:** Not production tested. Parameter ensured by design.

**3:** MCP41U83 must internally provide a hold time ≥ 300 ns for the SDA signal to bridge the undefined region of the falling edge of the SCL signal. The SDA signal is with respect to the minimum value of the High Input Threshold ($V_{IH}$) of the SCL signal.

**4:** The maximum fall time ($t_F$) for the SDA and SCL bus lines is specified at 300 ns. The maximum $t_F$ for SDA output stage is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified $t_F$.

**5:** $t_{HD:DAT}$ is measured from the SCL falling edge. It applies to data in transmission and acknowledgment.

**6:** A Fast mode (500 kHz) $I^2C$ bus device can be used in a Standard mode (100 kHz) $I^2C$ bus system if the data input setup time is 250 ns ($t_{SU:DAT}$ = 250 ns). This automatically occurs when the $I^2C$ bus device does not stretch the low period of the SCL signal. If the bus device stretches the low period of the SCL signal, it must output the next data bit on the SDA line. According to the Standard mode $I^2C$ bus specification, the sum of the maximum rise time ($t_{R_MAX}$) and $t_{SU:DAT}$ must be 1,250 ns before the SCL line is released: $t_{R_MAX}$ + $t_{SU:DAT}$ = 1,000 ns + 250 ns = 1,250 ns.

**7:** The maximum data hold time ($t_{HD:DAT}$) can be 3.45 µs for Standard mode and 0.9 µs for Fast mode. However, $t_{HD:DAT}$ must be less than the maximum $t_{AA}$ (output valid from clock) by a transition time. The maximum $t_{HD:DAT}$ must be met only when MCP41U83 does not stretch the low period of the SCL signal ($t_{LOW}$). If the clock stretches the SCL signal, the data must be valid by the setup time ($t_{SU:DAT}$) before MCP41U83 releases the clock.

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**TABLE 1-5: I²C BUS DATA TIMING CHARACTERISTICS (CONTINUED)**

**Standard Operating Conditions:** Unless otherwise indicated, $T_A$ = -40°C to +125°C (extended temperature). The operating voltage range is described in the **DC Specifications** table.

| Parameter | Symbol | Characteristic | Mode | Min. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 102A | $t_{RSCL}$ | SCL Rise Time | Standard mode | — | 1,000 | ns | Note 2 |
| | | | Fast mode | 20 | 300 | ns | Note 2 |
| | | | High Speed 1.7 | 20 | 80 | ns | Note 2 |
| | | | High Speed 1.7 | 20 | 160 | ns | After a repeated start or ACK bit (Note 2) |
| | | | High Speed 3.4 | 10 | 40 | ns | Note 2 |
| | | | High Speed 3.4 | 10 | 80 | ns | After a repeated start or ACK bit (Note 2) |
| 102B | $t_{RSDA}$ | SDA Rise Time | Standard mode | — | 1,000 | ns | Note 2 |
| | | | Fast mode | 20 | 300 | ns | Note 2 |
| | | | High Speed 1.7 | 20 | 160 | ns | Note 2 |
| | | | High Speed 3.4 | 10 | 80 | ns | Note 2 |
| 103A | $t_{FSCL}$ | SCL Fall Time | Standard mode | — | 300 | ns | Notes 2, 3, 4 |
| | | | Fast mode | 20 x $V_{DD}$/5.5 | 300 | ns | Notes 2, 3, 4 |
| | | | High Speed 1.7 | 20 | 80 | ns | Note 2 |
| | | | High Speed 3.4 | 10 | 40 | ns | Note 2 |
| 103B | $t_{FSDA}$ | SDA Fall Time | Standard mode | — | 300 | ns | Notes 2, 3, 4 |
| | | | Fast mode | 20 x $V_{DD}$/5.5 | 300 | ns | Notes 2, 3, 4 |
| | | | High Speed 1.7 | 20 | 160 | ns | Note 2 |
| | | | High Speed 3.4 | 10 | 80 | ns | Note 2 |
| 106 | $t_{HD:DAT}$ | Data Hold Time | Standard mode | 0 (3) | — (7) | ns | Notes 1, 5 |
| | | | Fast mode | 0 (3) | — (7) | ns | Note 5 |
| | | | High Speed 1.7 | 0 (3) | 150 | ns | Note 1 |
| | | | High Speed 3.4 | 0 (3) | 70 | ns | Note 1 |
| 107 | $t_{SU:DAT}$ | Data Input Setup Time | Standard mode | 250 | — | ns | Note 1 |
| | | | Fast mode | 250 | — | ns | Note 6 |
| | | | High Speed 1.7 | 10 | — | ns | Note 1 |
| | | | High Speed 3.4 | 10 | — | ns | Note 1 |

**Note 1:** Not production tested. Parameter ensured by characterization.

**2:** Not production tested. Parameter ensured by design.

**3:** MCP41U83 must internally provide a hold time ≥ 300 ns for the SDA signal to bridge the undefined region of the falling edge of the SCL signal. The SDA signal is with respect to the minimum value of the High Input Threshold ($V_{IH}$) of the SCL signal.

**4:** The maximum fall time ($t_F$) for the SDA and SCL bus lines is specified at 300 ns. The maximum $t_F$ for SDA output stage is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified $t_F$.

**5:** $t_{HD:DAT}$ is measured from the SCL falling edge. It applies to data in transmission and acknowledgment.

**6:** A Fast mode (500 kHz) I²C bus device can be used in a Standard mode (100 kHz) I²C bus system if the data input setup time is 250 ns ($t_{SU:DAT}$ = 250 ns). This automatically occurs when the I²C bus device does not stretch the low period of the SCL signal. If the bus device stretches the low period of the SCL signal, it must output the next data bit on the SDA line. According to the Standard mode I²C bus specification, the sum of the maximum rise time ($t_{R_MAX}$) and $t_{SU:DAT}$ must be 1,250 ns before the SCL line is released: $t_{R_MAX}$ + $t_{SU:DAT}$ = 1,000 ns + 250 ns = 1,250 ns.

**7:** The maximum data hold time ($t_{HD:DAT}$) can be 3.45 µs for Standard mode and 0.9 µs for Fast mode. However, $t_{HD:DAT}$ must be less than the maximum $t_{AA}$ (output valid from clock) by a transition time. The maximum $t_{HD:DAT}$ must be met only when MCP41U83 does not stretch the low period of the SCL signal ($t_{LOW}$). If the clock stretches the SCL signal, the data must be valid by the setup time ($t_{SU:DAT}$) before MCP41U83 releases the clock.


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**TABLE 1-5: $I^2C$ BUS DATA TIMING CHARACTERISTICS (CONTINUED)**

| **Standard Operating Conditions:** Unless otherwise indicated, $T_A$ = -40°C to +125°C (extended temperature). The operating voltage range is described in the **DC Specifications** table. | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Characteristic** | **Mode** | **Min.** | **Max.** | **Units** | **Conditions** |
| 109 | $t_{AA}$ | Output Valid from Clock | Standard mode | — | 3,450 | ns | **Note 1** |
| | | | Fast mode | — | 900 | ns | |
| | | | High Speed 1.7 | — | N/A | ns | |
| | | | High Speed 3.4 | — | N/A | ns | |
| 110 | $t_{BUF}$ | Bus Free Time between STOP and START conditions | Standard mode | 4,700 | — | ns | **Note 1** |
| | | | Fast mode | 1,300 | — | ns | |
| | | | High Speed 1.7 | N/A | — | ns | |
| | | | High Speed 3.4 | N/A | — | ns | |

**Note 1:** Not production tested. Parameter ensured by characterization.

**2:** Not production tested. Parameter ensured by design.

**3:** MCP41U83 must internally provide a hold time ≥ 300 ns for the SDA signal to bridge the undefined region of the falling edge of the SCL signal. The SDA signal is with respect to the minimum value of the High Input Threshold ($V_{IH}$) of the SCL signal.

**4:** The maximum fall time ($t_F$) for the SDA and SCL bus lines is specified at 300 ns. The maximum $t_F$ for SDA output stage is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified $t_F$.

**5:** $t_{HD:DAT}$ is measured from the SCL falling edge. It applies to data in transmission and acknowledgment.

**6:** A Fast mode (500 kHz) $I^2C$ bus device can be used in a Standard mode (100 kHz) $I^2C$ bus system if the data input setup time is 250 ns ($t_{SU:DAT}$ = 250 ns). This automatically occurs when the $I^2C$ bus device does not stretch the low period of the SCL signal. If the bus device stretches the low period of the SCL signal, it must output the next data bit on the SDA line. According to the Standard mode $I^2C$ bus specification, the sum of the maximum rise time ($t_{R_MAX}$) and $t_{SU:DAT}$ must be 1,250 ns before the SCL line is released: $t_{R_MAX} + t_{SU:DAT}$ = 1,000 ns + 250 ns = 1,250 ns.

**7:** The maximum data hold time ($t_{HD:DAT}$) can be 3.45 µs for Standard mode and 0.9 µs for Fast mode. However, $t_{HD:DAT}$ must be less than the maximum $t_{AA}$ (output valid from clock) by a transition time. The maximum $t_{HD:DAT}$ must be met only when MCP41U83 does not stretch the low period of the SCL signal ($t_{LOW}$). If the clock stretches the SCL signal, the data must be valid by the setup time ($t_{SU:DAT}$) before MCP41U83 releases the clock.

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## 1.5 SPI Timings

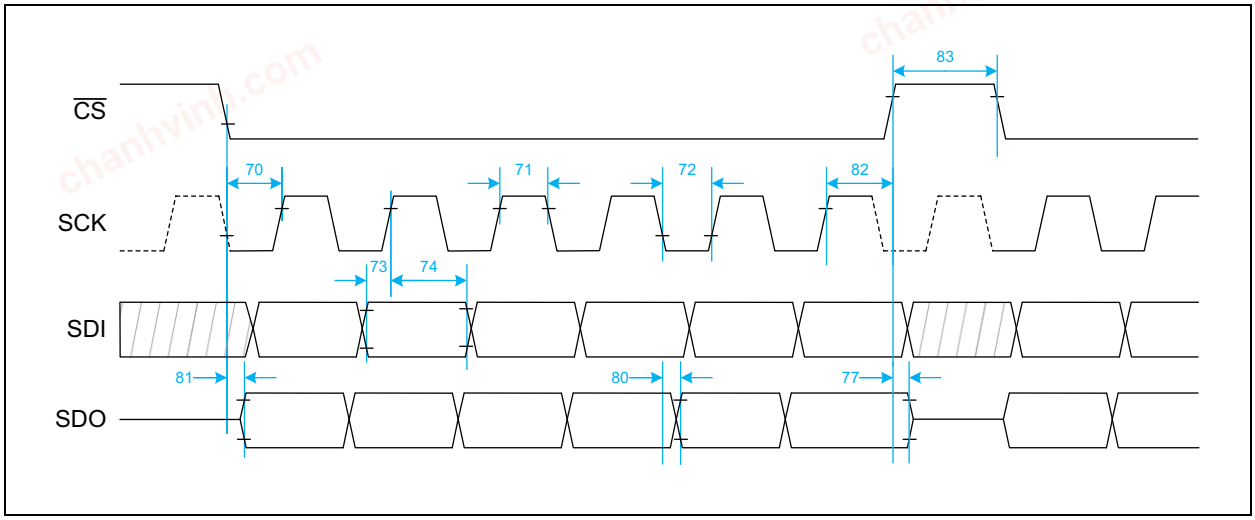



**FIGURE 1-4:** *SPI Timing Waveforms.*

**TABLE 1-6: SPI TIMING CHARACTERISTICS**

| **Standard Operating Conditions:** Unless otherwise indicated, $T_A$ = -40°C to +125°C (extended temperature). The operating voltage range is described in the **DC Specifications** table. | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Characteristic** | **Min.** | **Max.** | **Units** | **Conditions** |
| — | $f_{SCK}$ | SCK Input Frequency | — | 20 | MHz | Read/Write command, $C_L$ = 20 pF (**Note 1**) |
| 70 | $t_{CSA2SCH}$ | NCS Active ($V_{IL}$) to SCK Rising Edge | 25 | — | ns | **Note 1** |
| 71 | $t_{SCH}$ | SCK Input High Time | 20 | — | ns | **Note 1** |
| 72 | $t_{SCL}$ | SCK Input Low Time | 20 | — | ns | **Note 1** |
| 73 | $t_{DIV2SCH}$ | SDI Input Valid to SCK Rising Edge (Setup Time) | 15 | — | ns | **Note 1** |
| 74 | $t_{SCH2DIL}$ | SCK Rising Edge to SDI Input Invalid (Hold Time) | 10 | — | ns | **Note 1** |
| 77 | $t_{CSH2DOZ}$ | NSC Inactive ($V_{IH}$) to SDO Output High Impedance | — | 20 | ns | **Note 2** |
| 80 | $t_{SCL2DOV}$ | SCK Falling Edge to SDO Data Output Valid | — | 20 | ns | **Note 1** |
| 81 | $t_{SSL2DOV}$ | NCS Active ($V_{IL}$) to SDO Data Output Valid | — | 20 | ns | **Note 2** |
| 82 | $t_{SCH2SCL}$ | SCK Rising Edge to NCS Inactive ($V_{IH}$) (Hold Time) | 25 | — | ns | **Note 1** |
| 83 | $t_{CSA2CSL}$ | NCS Input High Time | 50 | — | ns | **Note 1** |

**Note 1:** Not production tested. Parameter ensured by characterization.

**2:** Not production tested. Parameter ensured by design.

**3:** All input signals are specified with $t_R$ = 1 ns/V and $t_F$ = 1 ns/V (10% to 90% of $V_{DD}$) and all timed values referred to $V_{IH}$ (min.) and $V_{IL}$ (max.) levels.


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## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (for example, outside specified power supply range) and therefore outside the warranted range.

### 2.1 Electrical Data

**Note:** Unless otherwise indicated, $T_A$ = +25°C and $V_{DD}$ = 5.5V.

† Potentiometer mode. P0A = $V_{DD}$, P0B = $V_{SS}$, $V_{SS}$ = DGND = GND.

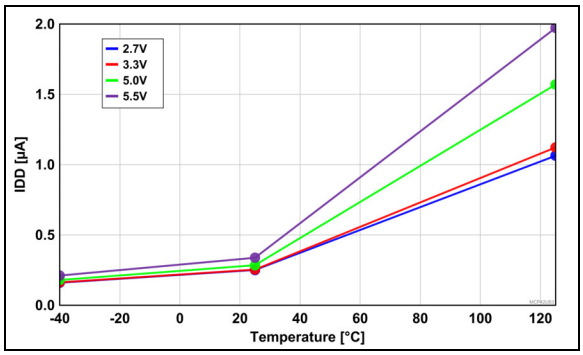



**FIGURE 2-1:** *Supply Static Current ($I_{DD}$) vs. Temperature, across $V_{DD}$. VSS = DGND = GND.*

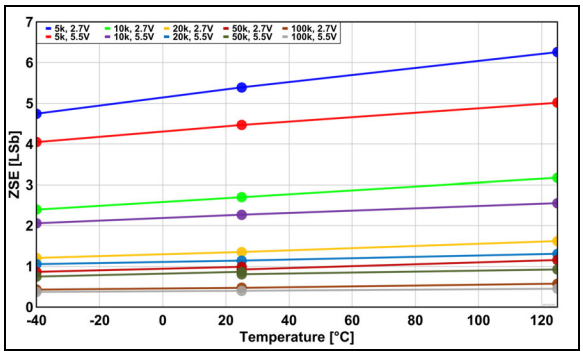



**FIGURE 2-4:** *Zero Scale Error (ZSE) vs. Temperature, across $V_{DD}$ and $R_{AB}$.* †

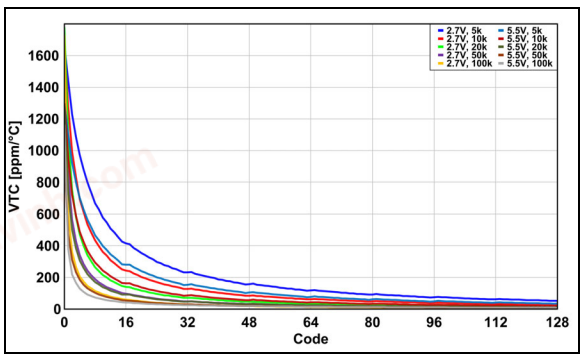



**FIGURE 2-2:** *Ratiometric Temperature Coefficient ($V_{TC}$) vs. Wiper Position (Code 0 to 128), across $V_{DD}$ and $R_{AB}$.*

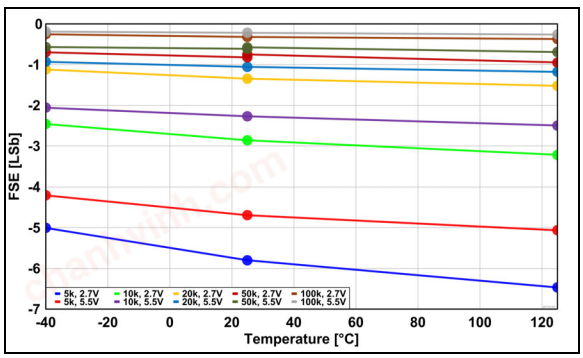



**FIGURE 2-5:** *Full Scale Error (FSE) vs. Temperature, across $V_{DD}$ and $R_{AB}$.* †

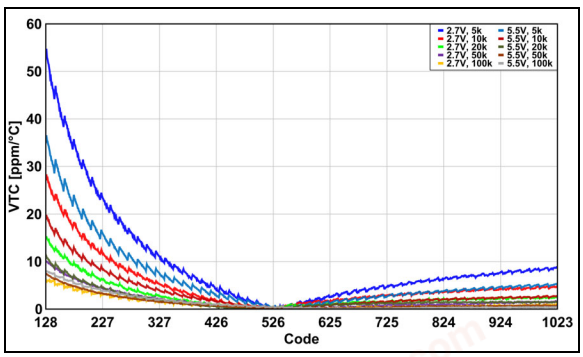



**FIGURE 2-3:** *Ratiometric Temperature Coefficient ($V_{TC}$) vs. Wiper Position (Code 128 to 1,023), across $V_{DD}$ and $R_{AB}$.*

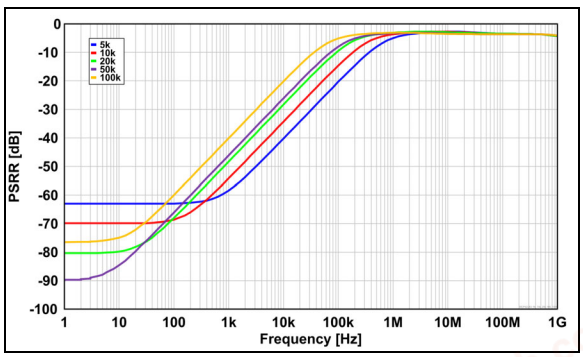



**FIGURE 2-6:** *Power Supply Rejection Ration (PSRR) vs. Frequency, across $R_{AB}$.*

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## 2.2 Linearity Data

### 2.2.1 RESISTANCE OPTION – $R_{AB}$ = 5 kΩ

**Note:** Unless otherwise indicated, $T_A$ = +25°C and $V_{DD}$ = 5.5V.

#### 2.2.1.1 Potentiometer Mode

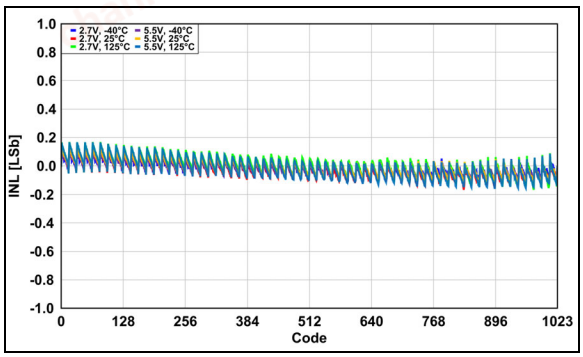



**FIGURE 2-7:** *Potentiometer Integral Nonlinearity (P-INL) Error vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*

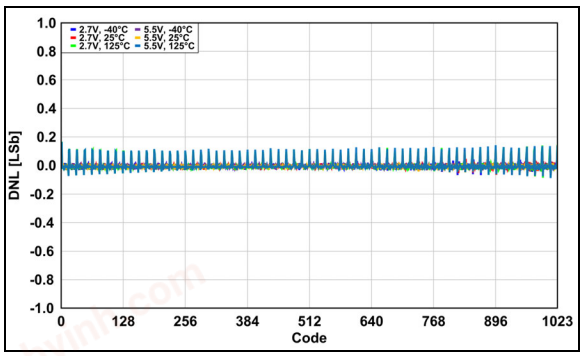



**FIGURE 2-8:** *Potentiometer Differential Nonlinearity (P-DNL) Error vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*

#### 2.2.1.2 Rheostat Mode

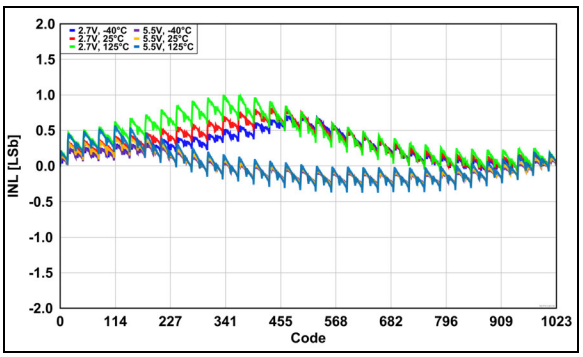



**FIGURE 2-9:** *Rheostat Integral Nonlinearity (R-INL) Error vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*

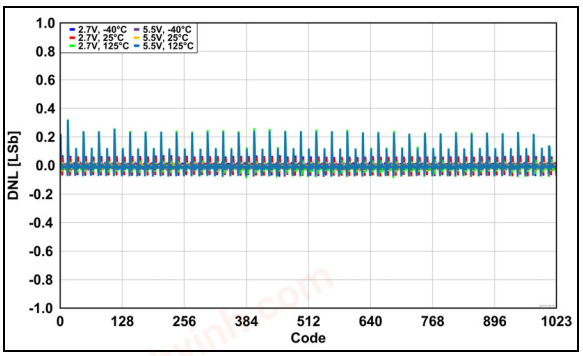



**FIGURE 2-10:** *Rheostat Differential Nonlinearity (R-DNL) Error vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*

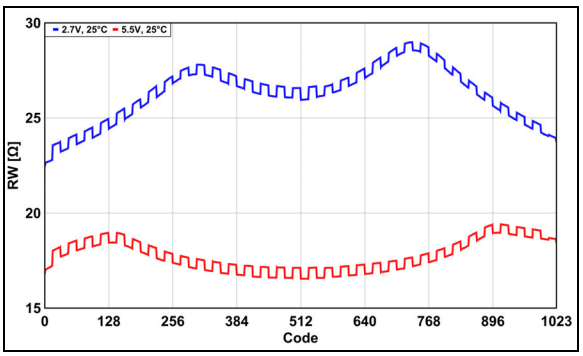



**FIGURE 2-11:** *Wiper Resistance ($R_W$) in Rheostat Mode vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*


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### 2.2.2 RESISTANCE OPTION – $R_{AB}$ = 10 kΩ

**Note:** Unless otherwise indicated, $T_A$ = +25°C and $V_{DD}$ = 5.5V.

#### 2.2.2.1 Potentiometer Mode

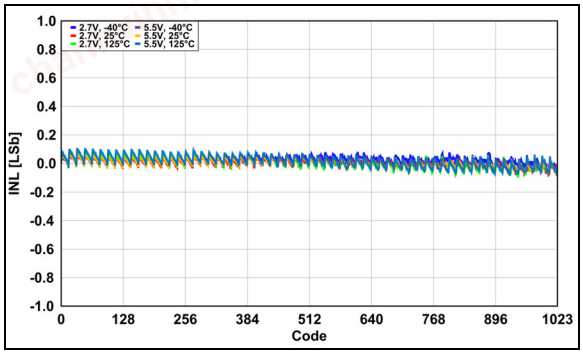



**FIGURE 2-12:** *Potentiometer Integral Nonlinearity (P-INL) Error vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*

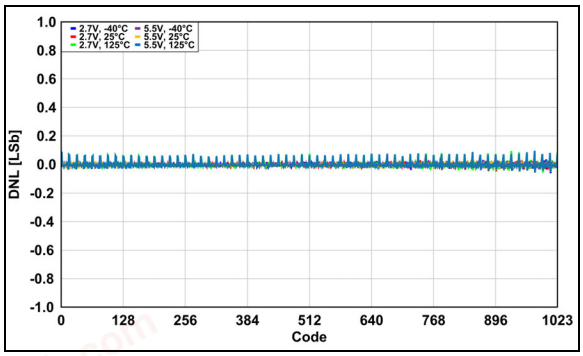



**FIGURE 2-13:** *Potentiometer Differential Nonlinearity (P-DNL) Error vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*

#### 2.2.2.2 Rheostat Mode

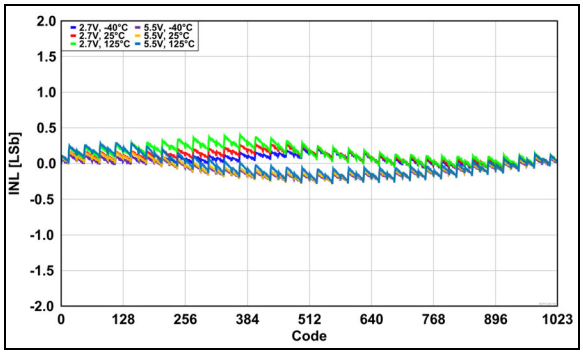



**FIGURE 2-14:** *Rheostat Integral Nonlinearity (R-INL) Error vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*

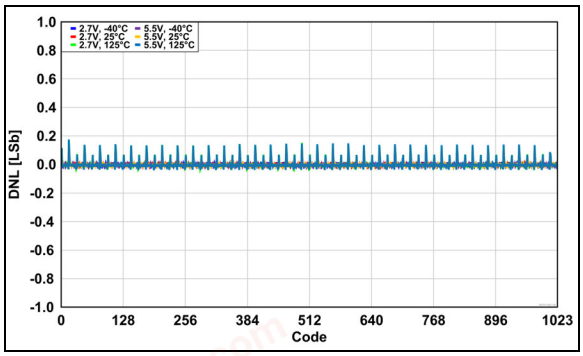



**FIGURE 2-15:** *Rheostat Differential Nonlinearity (R-DNL) Error vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*

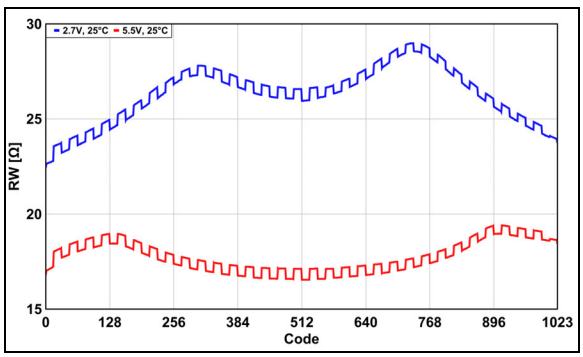



**FIGURE 2-16:** *Wiper Resistance ($R_W$) in Rheostat Mode vs Wiper Position (Code), across $V_{DD}$ and Temperature.*

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### 2.2.3 RESISTANCE OPTION – $R_{AB}$ = 20 kΩ

**Note:** Unless otherwise indicated, $T_A$ = +25°C and $V_{DD}$ = 5.5V.

#### 2.2.3.1 Potentiometer Mode

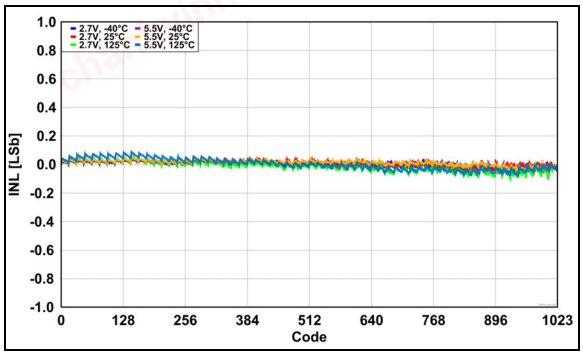



**FIGURE 2-17:** *Potentiometer Integral Nonlinearity (P-INL) Error vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*

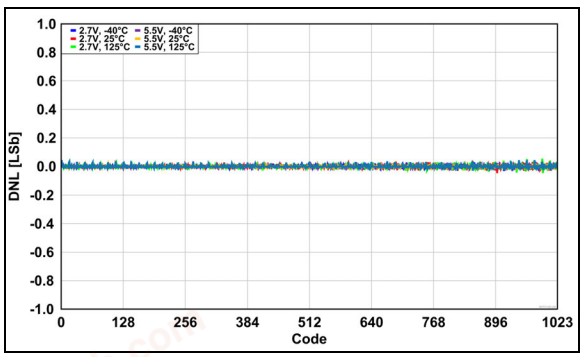



**FIGURE 2-18:** *Potentiometer Differential Nonlinearity (P-DNL) Error vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*

#### 2.2.3.2 Rheostat Mode

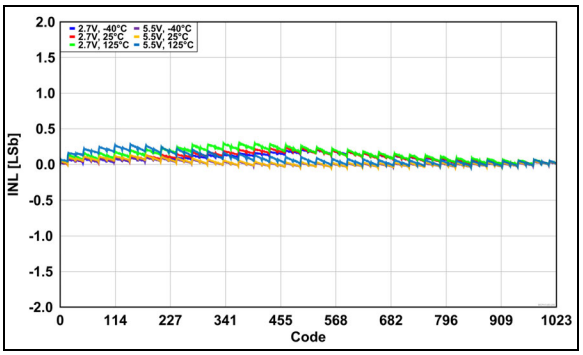



**FIGURE 2-19:** *Rheostat Integral Nonlinearity (R-INL) Error vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*

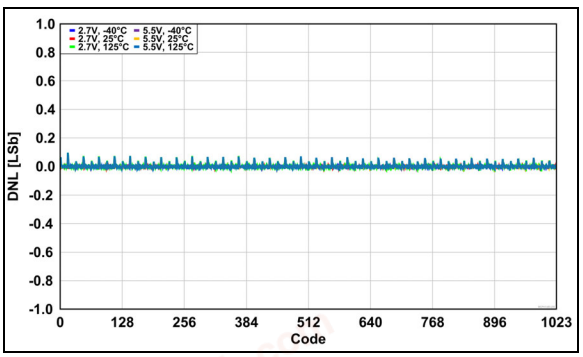



**FIGURE 2-20:** *Rheostat Differential Nonlinearity (R-DNL) Error vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*

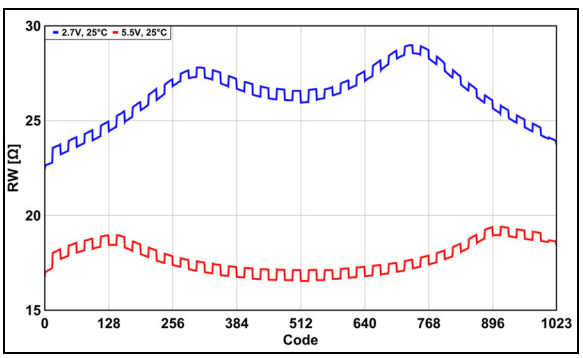



**FIGURE 2-21:** *Wiper Resistance ($R_W$) in Rheostat Mode vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*


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### 2.2.4 RESISTANCE OPTION – $R_{AB}$ = 50 kΩ

**Note:** Unless otherwise indicated, $T_A$ = +25°C and $V_{DD}$ = 5.5V.

#### 2.2.4.1 Potentiometer Mode

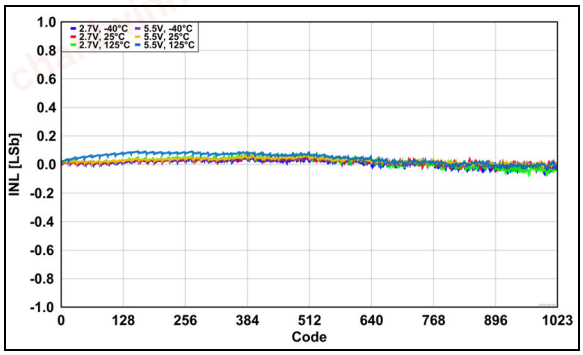



**FIGURE 2-22:** *Potentiometer Integral Nonlinearity (P-INL) Error vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*

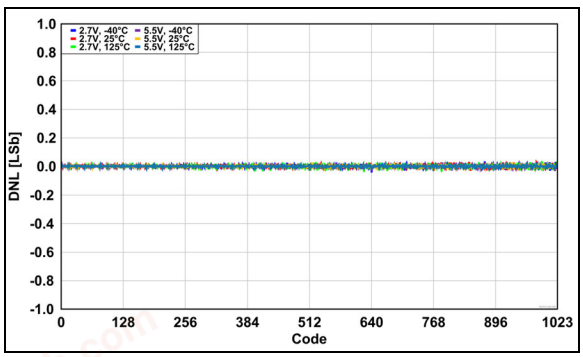



**FIGURE 2-23:** *Potentiometer Differential Nonlinearity (P-DNL) Error vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*

#### 2.2.4.2 Rheostat Mode

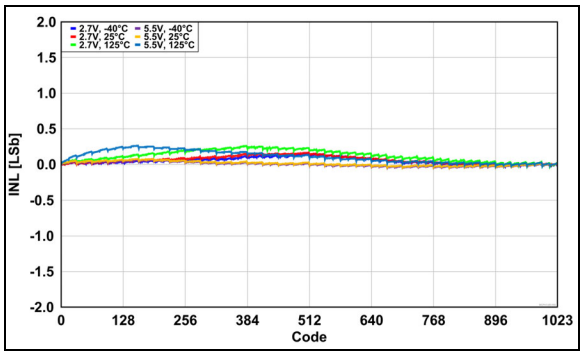



**FIGURE 2-24:** *Rheostat Integral Nonlinearity (R-INL) Error vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*

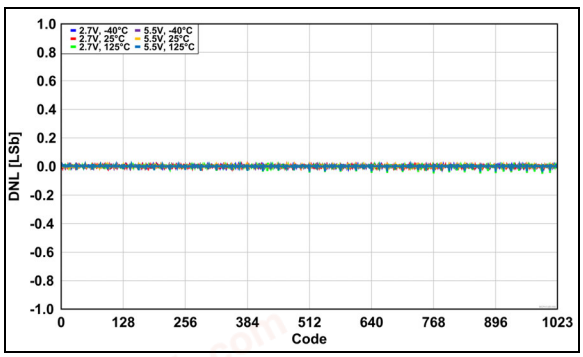



**FIGURE 2-25:** *Rheostat Differential Nonlinearity (R-DNL) Error vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*

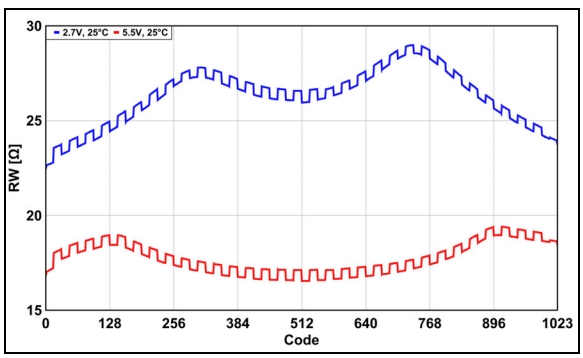



**FIGURE 2-26:** *Wiper Resistance ($R_W$) in Rheostat Mode vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*

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### 2.2.5 RESISTANCE OPTION – $R_{AB}$ = 100 kΩ

**Note:** Unless otherwise indicated, $T_A$ = +25°C and $V_{DD}$ = 5.5V.

#### 2.2.5.1 Potentiometer Mode

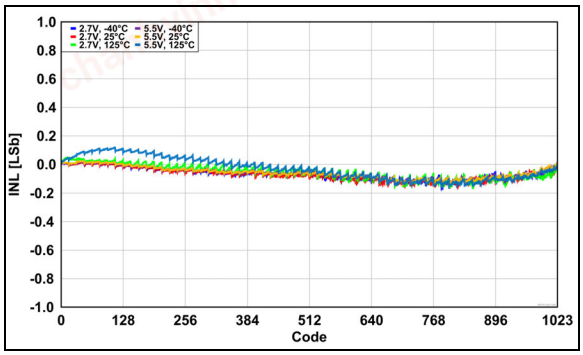



**FIGURE 2-27:** *Potentiometer Integral Nonlinearity (P-INL) Error vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*

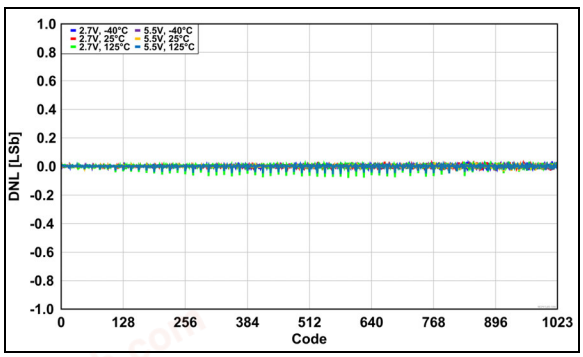



**FIGURE 2-28:** *Potentiometer Differential Nonlinearity (P-DNL) Error vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*

#### 2.2.5.2 Rheostat Mode

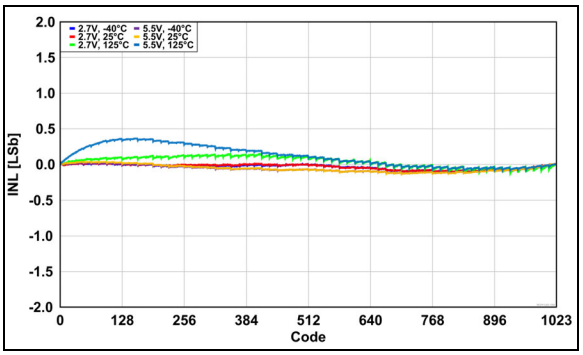



**FIGURE 2-29:** *Rheostat Integral Nonlinearity (R-INL) Error vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*

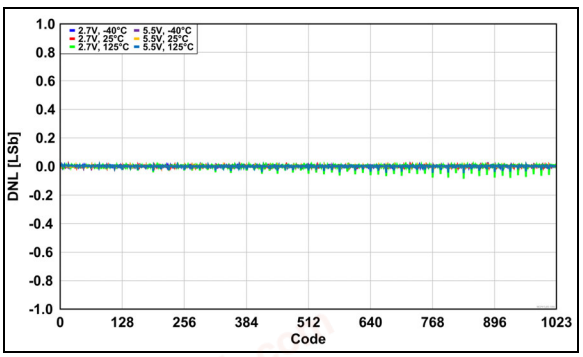



**FIGURE 2-30:** *Rheostat Differential Nonlinearity (R-DNL) Error vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*

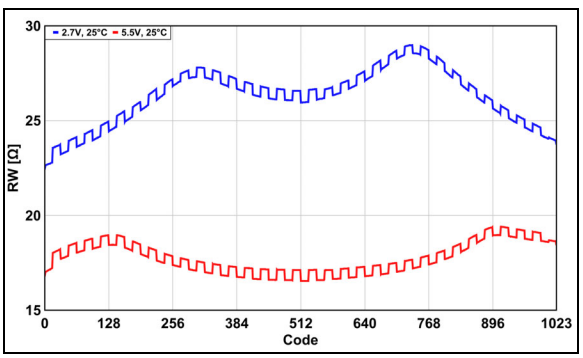



**FIGURE 2-31:** *Wiper Resistance ($R_W$) in Rheostat Mode vs. Wiper Position (Code), across $V_{DD}$ and Temperature.*


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## 3.0 PIN DESCRIPTION

MCP41U83 pin descriptions are listed in Table 3-1.

Overviews for the pin functions are provided in **Section 3.1** through **Section 3.14**.

**TABLE 3-1: MCP41U83 (SINGLE DIGITAL POTENTIOMETER) PIN FUNCTION TABLE**

| Pin Number | | Symbol | I/O Type | | Buffer Type | | Description | |
|---|---|---|---|---|---|---|---|---|
| 14-Lead TSSOP | 16-Lead VQFN | | SPI | $I^2C$ | SPI | $I^2C$ | SPI Mode | $I^2C$ Mode |
| 1 | 16 | VDD | P | P | — | — | Positive Power Supply | |
| 2 | 1 | SDO/A1 | O | I | — | ST | SPI Serial Data Output | $I^2C$ Target Address Bit 1 Pin |
| 3 | 2 | SCK/SCL | I | I | ST | ST | SPI Serial Clock Input | $I^2C$ Serial Clock Input |
| 4 | 3 | SDI/SDA | I | I/O | ST | ST | SPI Serial Data Input | $I^2C$ Serial Data |
| 5 | 4 | $\overline{CS}$/A0 | I | I | ST | ST | SPI Chip Select | $I^2C$ Target Address Bit 0 Pin |
| 6 | 5 | SPI2C | I | I | ST | ST | SPI/$I^2C$ Interface Select Pin | |
| 7 | 6 | DGND | P | P | — | — | Digital Interface Ground | |
| 8 | 7 | P0B | A | A | — | — | Potentiometer 0 B Terminal | |
| 9 | 8 | P0W | A | A | — | — | Potentiometer 0 Wiper Terminal | |
| 10 | 9 | P0A | A | A | — | — | Potentiometer 0 A Terminal | |
| 11 | 10 | VSS | P | P | — | — | Negative Power Supply | |
| 12 | 11 | NC | — | — | — | — | Not Connected | |
| 13 | 12 | NC | — | — | — | — | Not Connected | |
| 14 | 13 | NC | — | — | — | — | Not Connected | |
| — | 14 | NC | — | — | — | — | Not Connected | |
| — | 15 | NC | — | — | — | — | Not Connected | |
| — | 17 | EP | — | — | — | — | Exposed Pad (**Note**) | |

**Legend:** A = Analog, I = Input, ST = Schmitt Trigger, O = Output, I/O = Input/Output, P = Power.

**Note:** The 16-Lead VQFN package has a contact on the bottom of the package. This contact is conductively connected to the die substrate ($V_{SS}$) and must be left unconnected or connected to the DGND pin of MCP41U83.

### 3.1 Positive Power Supply Input (VDD)

The VDD pin is the positive power supply input of MCP41U83. The analog input power supply is relative to $V_{SS}$.

### 3.2 Digital Logic Ground (DGND)

The DGND pin is the digital logic ground reference of MCP41U83. Digital thresholds are determined by the $V_{DD}$ to DGND voltage range.

### 3.3 Negative Power Supply Input (VSS)

The VSS pin is the negative analog supply reference of MCP41U83.

### 3.4 SPI or $I^2C$ Select Pin (SPI2C)

Based on the input status of the SPI2C pin, the serial interface of MCP41U83 is configured as either SPI or $I^2C$. This pin is level-sensitive – switching between the serial interfaces is possible during normal operation.

The function of the pins described in Table 3-2 changes based on the SPI2C pin status:

**TABLE 3-2: SPI2C PIN FUNCTION CHANGES**

| SPI2C Pin | Connected to DGND | Connected to VDD |
|---|---|---|
| **SDO/A1** | SDO | A1 |
| **SCK/SCL** | SCK | SCL |
| **SDI/SDA** | SDI | SDA |
| **$\overline{CS}$/A0** | $\overline{CS}$ | A0 |

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### 3.5 I²C Serial Clock Pin (SCL)

**Note:** Available only when MCP41U83 is configured for I²C operation.

The SCL pin is the I²C Serial Clock pin. This pin must connect to the I²C Controller SCL pin.

### 3.6 I²C Serial Data Pin (SDA)

**Note:** Available only when MCP41U83 is configured for I²C operation.

The SDA pin is the I²C Serial Data pin. This pin must connect to the I²C Controller SDA pin.

### 3.7 I²C Device Address Pins (A0, A1)

**Note:** Available only when MCP41U83 is configured for I²C operation.

The state of the A0 and A1 pins determines the values of bit 0 and bit 1 of the MCP41U83 I²C Target Address. With A0 and A1, up to four devices having the same Target Address can be connected on a single I²C bus. After POR, the A0 and A1 pins are floating. Connect these pins to VDD or DGND to get the desired address before starting communication with MCP41U83.

### 3.8 SPI Chip Select Pin ($\overline{CS}$)

**Note:** Available only when MCP41U83 is configured for SPI operation.

The $\overline{CS}$ pin enables or disables the SPI serial interface allowing multiple MCP41U83 devices to connect to the SPI Controller. The SPI Controller must enable the serial interface before MCP41U83 can receive SPI commands.

### 3.9 SPI Serial Data Input Pin (SDI)

**Note:** Available only when MCP41U83 is configured for SPI operation.

The SDI pin is the SPI Serial Data Input pin. This pin transfers data from the SPI Controller to MCP41U83.

### 3.10 SPI Serial Data Output Pin (SDO)

**Note:** Available only when MCP41U83 is configured for SPI operation.

The SDO pin is the SPI Serial Data Output pin. This pin transfers data from MCP41U83 to the SPI Controller.

### 3.11 SPI Serial Clock Pin (SCK)

**Note:** Available only when MCP41U83 is configured for SPI operation.

The SCK pin is the SPI Serial Clock pin. This pin must connect to the SPI Controller SCK line.

### 3.12 Potentiometer Terminal A Pin (P0A)

The P0A pin connects to Terminal A of the internal potentiometers.

The potentiometer's Terminal A is the fixed connection to the full scale wiper value of the digital potentiometer. This corresponds to a wiper value of `3FFh`.

The P0A pin does not have a polarity relative to the pins of Terminal W or B. The P0A pin can support both positive and negative currents. Voltage on Terminal A must be between $V_{SS}$ and $V_{DD}$.

### 3.13 Potentiometer Terminal W (Wiper) Pin (P0W)

The P0W pin connects to Terminal W (wiper) of the internal potentiometers.

Terminal W is the adjustable terminal of the digital potentiometer.

The P0W pin does not have a polarity relative to the pins of Terminal A or B. The P0W pin can support both positive and negative currents. Voltage on Terminal W must be between $V_{SS}$ and $V_{DD}$.

### 3.14 Potentiometer Terminal B Pin (P0B)

The P0B pin connects to Terminal B of the internal potentiometers.

The potentiometer's Terminal B is the fixed connection to the zero scale wiper value of the digital potentiometer. This corresponds to a wiper value of `000h`.

The P0B pin does not have a polarity relative to the pins of Terminal A or W. The P0B pin can support both positive and negative currents. Voltage on Terminal B must be between $V_{SS}$ and $V_{DD}$.


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# 4.0 MCP41U83 DEVICE OPERATION

## 4.1 General Description

MCP41U83 devices are 10-bit digital potentiometers designed for automotive and industrial automation use. A 1,000 cycles Multiple-Time Programmable (MTP) nonvolatile (NV) memory enables MCP41U83 to retain the set values beyond a power cycle. The communication is done using a user-selectable serial interface, with two options: SPI and $I^2C$.

To help with system integration, the power supply can be configured with both single or dual (split) voltage. This enables the use of negative analog voltages in signal processing applications. Also, the terminals of the resistor ladder, including the wiper, are able to be individually disconnected from the internal structures to configure MCP41U83 as rheostats or to reduce current consumption.

Serial commands and digital features provide many advantages and fail-safe operation in demanding environments. MCP41U83 can be reset and is fully software configurable. To increase the communication reliability, it has a dedicated Cyclic Redundancy Check (CRC) module, that can be enabled or disabled. SPI operating mode allows up to 128 devices to connect in daisy-chain configuration, simplifying complex designs.

MCP41U83 devices support an extended temperature range of -40°C to +125°C and are AEC-Q100 Grade-1 qualified for automotive applications.

## 4.2 Power Supply Configurations

MCP41U83 operates using one of two power supply configurations: single voltage and dual (split) voltage.

### 4.2.1 SINGLE VOLTAGE CONFIGURATION

In single voltage configuration, the VSS and DGND pins are connected together at a single point to form the ground reference, as shown in Figure 4-1. $V_{DD}$ is common for both analog and digital modules.

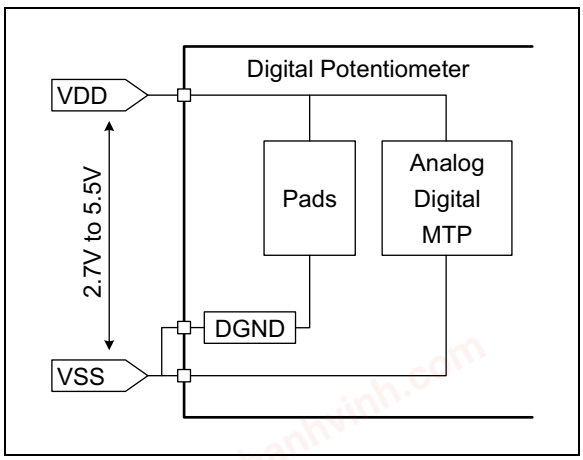



**FIGURE 4-1:** *Single Voltage Configuration.*

### 4.2.2 DUAL VOLTAGE CONFIGURATION

In dual voltage configuration, the VSS and DGND pins are not connected together and voltage levels are kept separate, as shown in Figure 4-2. $V_{DD}$ is common for both analog and digital modules.

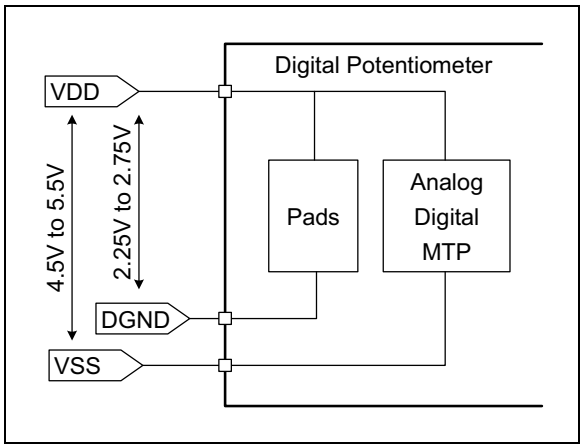



**FIGURE 4-2:** *Dual Voltage Configuration.*

## 4.3 Power-on Reset/Brown-out Reset Modules

Specific sequences must be followed on power-up and power-down to ensure safe operating conditions.

### 4.3.1 POWER-UP CONSIDERATIONS

Microchip recommends the next power-up sequence:

1. Apply power to the VDD, VSS and DGND pins.
2. Apply power to the digital pins used in serial communication: SDO/A1, SCK/SCL, SDI/SDA, $\overline{CS}$/A0 and SPI2C.
3. Apply power to the analog P0A, P0B and P0W pins.

**Note:** Applying power to other pins when the power modules are not supplied with proper voltage levels using the VDD, VSS and DGND pins is not advised. This leads to unpredictable behavior and/or damage to the internal circuitry of the MCP41U83 device.

When power is properly applied to the VDD pin, the POR module becomes active and sets the wipers to midscale. Then, for nonvolatile MCP41U83 devices, the POR module restores the most recent programmed MTP value stored in the nonvolatile wiper registers.

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The wiper value during power-up depends on the memory type and the time at which $V_{DD}$ level reaches $V_{POR}$ and $V_{RAM}$ levels. Figure 4-3 shows a diagram for power-up, followed by power-down.

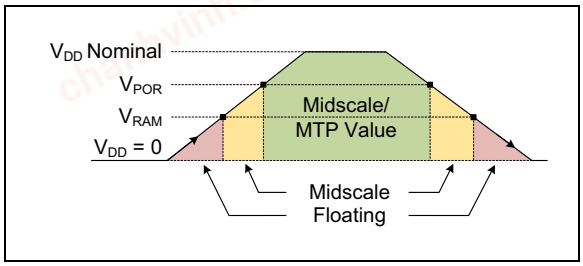



**FIGURE 4-3:** *Power-up and Power-down.*

In the red zone of Figure 4-3, when $V_{DD}$ is below $V_{RAM}$, the wiper is floating. In the orange zones the wiper is at midscale. When $V_{DD}$ crosses the $V_{POR}$ threshold, MCP41U83 loads the wiper register with the value stored in the corresponding nonvolatile register and updates the wiper register's position relative to the resistor ladder endpoints.

### 4.3.2 POWER-DOWN CONSIDERATIONS

Microchip recommends the next power-down sequence:

1. Power down the analog P0A, P0B and P0W pins.
2. Power down the VDD, VSS and DGND pins.

| **Note:** | Powering down the power supply pins before the analog pins is not advised. This damages the MCP41U83 device. |
|---|---|

## 4.4 Cyclic Redundancy Check (CRC) Module

Digital communication with MCP41U83 can be secured through the insertion of a CRC byte at the end of each transmitted or received frame. CRC checksums allow excellent coverage for communication errors that can happen in the system in noisy environments.

The CRC feature is enabled or disabled using the CRCEN (CRC Enable) bit in the CRC register. If an error is detected, MCP41U83 sets the CRCERR (CRC Error) bit in the STATUS register.

**Note:** CMDERR (Command Error) and CRCERR (CRC Error) bits are independent of each other.

To compute an 8-bit CRC byte for MCP41U83, use the CRC-8 polynomial: $CRC_8(x) = x^8 + x^2 + x^1 + x^0$.

The Controller must generate and transmit the CRC byte when using a command that modifies the memory, while MCP41U83 responds with the CRC byte when receiving a command to read data.

The Controller is responsible for handling the CRC verification:

- For Writes: the Controller must read the STATUS register and verify there was no error.
- For Reads: the CRC byte must be computed and compared with the received value.

## 4.5 Device Memory

MCP41U83 includes two types of user memory:

- Volatile memory (RAM)
- Nonvolatile memory (MTP)

Table 4-3 shows the memory-mapped register space. The available commands that modify the registers are detailed in **Section 6.7, "I2C Device Commands"** and **Section 7.4, "SPI Device Commands"**.

### 4.5.1 VOLATILE REGISTER MEMORY (RAM)

Several of the volatile memory address locations are reserved for specific operations. These locations are detailed in Table 4-3.

Every Wiper address location is 10 bits in size to fit the 1,024 steps of the wiper setting. Several registers do not implement all 10 bits. The bits in these registers are described in **Section 5.0, "Register Description"**.

### 4.5.2 NONVOLATILE REGISTER MEMORY (MTP)

MCP41U83 uses Multiple-Time Programmable (MTP) nonvolatile memory. Every MTP memory location can be programmed 1,000 times. MTP memory locations are 10 bits in size.

Up to four nonvolatile (NV) registers are available for Read or Write operations:

- NV Wiper0
- GP Data0, GP Data1 and GP Data2.

Use NV Wiper 0 to modify the POR or reset the values of the volatile Wiper0 register. Use GP Data0, GP Data1 and GP Data2 to store custom data.

As all NV registers are mapped to the MTP memory, only a limited number of 1,000 programming cycles is available for each of these four NV registers.


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**Note:** Read the associated counter registers prior to writing to any of the user NV registers, as shown in Table 4-1.

**TABLE 4-1: NV REGISTERS AND THEIR ASSOCIATED COUNT REGISTERS**

| Address | NV Register | Address | Associated Count Register |
|---|---|---|---|
| 03h | NV Wiper0 | 15h | NV W0 Count |
| 05h | GP Data0 | 19h | DATA0 Count |
| 06h | GP Data1 | 1Bh | DATA1 Count |
| 07h | GP Data2 | 1Dh | DATA2 Count |

For every write operation executed on the user NV registers, MCP41U83 increments the associated count register by 1.

Once the count registers reach 1,000, no more writes are allowed to the corresponding NV register.

When the MTP memory becomes full, MCP41U83 sets the CMDERR bit or sends a negative acknowledgment (NACK). MCP41U83 also ignores (does not execute) any further write commands that it receives.

**Note:** Writing to a NV register can be significantly slower than writing to a RAM location. For details, see **Section 1.3, "General Timing Characteristics"**, parameter $t_{WriteNV}$.

### 4.5.3 MEMORY UPDATE ON RESET

After a POR or software reset, part of the RAM memory is updated with the default POR values, while other locations can get modified with the values stored in the MTP memory. Table 4-2 indicates which RAM locations are updated from their corresponding NV locations.

**TABLE 4-2: POR/SOFTWARE RESET UPDATE OF RAM LOCATIONS FROM MTP MEMORY**

| RAM Memory | | MTP Memory | | Comments |
|---|---|---|---|---|
| Address | Register | Address | Register | |
| 01h | Volatile Wiper0 | 03h | NV Wiper0 | **Note** |

**Note:** Modifying a NV Wiper register location does not trigger an update of the associated volatile register location, unless there is a POR or a software reset occurs.

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**TABLE 4-3: MEMORY MAP AND COMMANDS**

| Address | Function | Allowed Commands | Disallowed Commands[1] | Memory Type | Factory Initial/ POR Value |
|---|---|---|---|---|---|
| 00h | Reserved for SPI Daisy Chain | — | — | — | — |
| 01h | Volatile Wiper0[2] | All | — | RAM | 200h |
| 02h | Reserved | — | — | — | — |
| 03h | NV Wiper0[2] | Read/Write | Increment/Decrement | MTP[3] | 200h |
| 04h | Reserved | — | — | — | — |
| 05h | GP Data0 | Read/Write | Increment/Decrement | MTP[3] | 000h |
| 06h | GP Data1 | Read/Write | Increment/Decrement | MTP[3] | 000h |
| 07h | GP Data2 | Read/Write | Increment/Decrement | MTP[3] | 000h |
| 08h | STATUS Register | Read | Write/Increment/Decrement | RAM | 002h |
| 09h | LOCK Register | Read/Write | Increment/Decrement | RAM | 000h |
| 0Ah | Terminal Control Register | Read/Write | Increment/Decrement | RAM | 000h |
| 0Bh | SYNC Register | Read/Write | Increment/Decrement | RAM | 000h |
| 0Ch | CRC Register | Read/Write | Increment/Decrement | RAM | 000h |
| 0Dh | RESET Register | Write | Read/Increment/Decrement | RAM | 000h |
| 0Eh - 14h | Reserved | — | — | — | — |
| 15h | NV W0 Count | Read | Write/Increment/Decrement | MTP[3] | |
| 16h - 18h | Reserved | — | — | — | — |
| 19h | Data0 Count | Read | Write/Increment/Decrement | MTP[3] | |
| 1Ah | Reserved | — | — | — | — |
| 1Bh | Data1 Count | Read | Write/Increment/Decrement | MTP[3] | |
| 1Ch | Reserved | — | — | — | — |
| 1Dh | Data2 Count | Read | Write/Increment/Decrement | MTP[3] | |
| 1Eh | Reserved | — | — | — | — |
| 1Fh | Reserved for SPI Daisy Chain | — | — | — | — |

**Legend:** = Reserved, = Volatile Memory – RAM, = Nonvolatile (NV) Memory – MTP.

**Note 1:** In SPI mode, MCP41U83 sets the CMDERR bit in the STATUS register for any invalid command and address combination that it receives. In $I^2C$ mode, MCP41U83 sends a NACK if the command and/or address is incorrect.

**2:** Volatile Wiper0 loads the value from NV Wiper 0 after a POR or a software reset. After initialization, the wiper position is modified only by writing to the volatile wiper register, while its NV register counterparts is only used to set the initial value.

**3:** RAM location mapped to MTP memory. Writing to this location, if allowed, triggers an update of the MTP memory with specific constraints, including a longer write time. For more details, see **Section 4.5.2, "Nonvolatile Register Memory (MTP)"**.

**4:** Following a write to NV registers, the NV counter register and target registers reflect the newly programmed values. To check if the MTP write was successful, read the NV counter register and target registers.


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## 4.6 Resistor Network

MCP41U83 has two 10-bit resolution resistor networks. Each resistor network allows zero scale to full scale connections. Figure 4-4 shows a block diagram for the resistor network of a single channel.

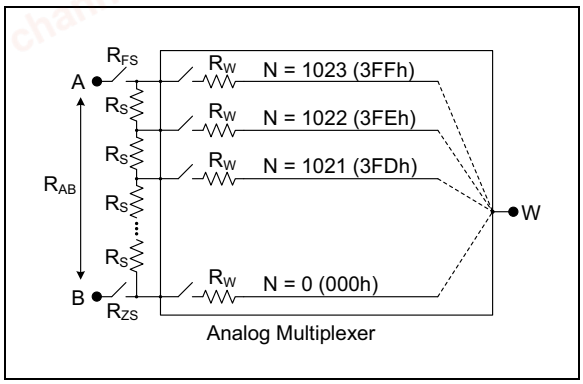



**FIGURE 4-4:** *Block Diagram of Resistor Network.*

Each resistor network is divided into several blocks and includes the following components:

- Resistor ladder
- Wiper
- Shutdown switches (terminal connections).

The wiper resistance, $R_W$, depends on the following factors: wiper code, MCP41U83 $V_{DD}$, terminal voltages (on A, B, and W) and temperature.

Also, for the previously mentioned factors, every tap selection resistance has a small variation. For devices with a smaller end-to-end resistance ($R_{AB}$), this variation has greater effects on some specifications, such as the integral nonlinearity (INL), compared to devices with a larger $R_{AB}$.

## 4.7 Resistor Ladder Module

A resistor ladder is a series of resistors ($R_S$) of equal value with a connection point (tap) between each two resistors. The total number of resistors in the ladder determines $R_{AB}$ as shown in Figure 4-4. The end points of the resistor ladder are connected to analog switches, that are connected to the Terminal A and Terminal B pins of MCP41U83. $R_{AB}$ and $R_S$ have small variations over voltage and temperature.

For 10-bit resolution MCP41U83 devices, there are 1,023 resistors connected in a string between terminal A and terminal B. The wiper can be set to tap onto any of these 1,023 resistors, thus providing 1,024 possible settings, including direct connections to terminals A and B.

The step resistance, $R_S$, for 10-bit resolution devices is calculated using Equation 4-1.

**EQUATION 4-1:**

$$R_S = \frac{R_{AB}}{1,023}$$

Where:

$R_S$ = Step Resistance (Ω)
$R_{AB}$ = End-to-End Resistance (kΩ)

### 4.7.1 RESISTOR NETWORK TERMINAL DISCONNECT

The TCON0 register independently controls the A, B and W terminals of resistor network 0 using the following bits:

- R0A bit controls terminal A
- R0B bit controls terminal B
- R0W bit controls terminal W.

A shutdown switch is closed when its associated bit (R0A, R0B or R0W) is set to '0'. The switch is opened when its associated bit is set to '1'.

For more details about the available options, see **TCON0 Register**.

### 4.7.2 POTENTIOMETER/RHEOSTAT CONFIGURATION

To configure MCP41U83 to function as a Potentiometer or a Rheostat, clear or set either the R0A bit or the R0B bit of the TCON0 register, as shown in Figure 4-5.

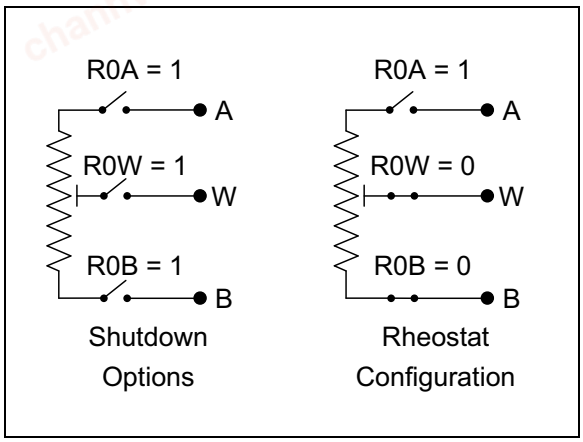



**FIGURE 4-5:** *Resistor Network Terminal Configuration Options.*

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By default, the R0A, R0B and R0W bits are set to ‘0’. Thus, MCP41U83 functions as a Potentiometer.

To configure MCP41U83 as a Rheostat, follow one of the next two procedures:

1. Disconnect the P0A pin:
   - Set bits R0W and R0B to ‘0’
   - Set bit R0A to ‘1’
   - (Optionally) Disconnect the P0A pin from the resistor network. Pin P0A still carries voltage and can affect MCP41U83 functionality.
2. Disconnect the P0B pin:
   - Set bits R0A and R0W to ‘0’
   - Set bit R0B to ‘1’
   - (Optionally) Disconnect the P0B pin from the resistor network. Pin P0B still carries voltage and can affect MCP41U83 functionality.


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## 5.0 REGISTER DESCRIPTION

The following section provides information on MCP41U83 registers and their implemented bits.

**Note:** The values provided in Register 5-1 through Register 5-15 are right-justified.

### 5.1 Volatile Wiper 0

The Volatile Wiper0 register reflects Wiper0 resistor ladder position.

Write, Increment or Decrement commands to this register update the Wiper0 position.

Read this register to determine the value of the Wiper0 resistor ladder position.

**REGISTER 5-1: VOLATILE WIPER 0 REGISTER (ADDRESS 01H)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-1 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | D9 | D8 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-10 Unimplemented at this time. Always reads as ‘0’.

bit 9-0 **D9 – D0:** Wiper0 position bits
Examples:
`3FFh` = Full scale position.
`200h` = Midscale position.
`000h` = Zero scale position.

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## 5.2 Nonvolatile Wiper 0

The NV Wiper0 register stores the user-defined reset value for the Volatile Wiper0 register.

This register supports Read and Write commands.

Increment or Decrement commands to this register set the CMDERR bit of the STATUS register in SPI mode or are not acknowledged (NACK) in $I^2C$ mode.

**REGISTER 5-2: NONVOLATILE WIPER 0 REGISTER (ADDRESS 03H)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-1 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | D9 | D8 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-10 Unimplemented at this time. Always reads as ‘0’.

bit 9-0 **D9 – D0:** NV Wiper0 data bits


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## 5.3 GP Data0

This register supports read and write commands and allows it to store custom data. Data written to the GP Data0 register can be retrieved after a power loss.

Increment or Decrement commands to this register set the CMDERR bit of the STATUS register in SPI mode or are not acknowledged (NACK) in $I^2C$ mode.

**REGISTER 5-3: GP DATA0 REGISTER (ADDRESS 05H)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | D9 | D8 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-10 Unimplemented at this time. Always reads as ‘0’.

bit 9-0 **D9 – D0:** NV general data storage bits

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## 5.4 GP Data1

This register supports read and write commands and allows it to store custom data. Data written to the GP Data1 register can be retrieved after a power loss.

Increment or Decrement commands to this register set the CMDERR bit of the STATUS register in SPI mode or are not acknowledged (NACK) in $I^2C$ mode.

**REGISTER 5-4: GP DATA1 REGISTER (ADDRESS 06H)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | D9 | D8 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-10 Unimplemented at this time. Always reads as '0'.

bit 9-0 **D9 – D0:** NV general data storage bits


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## 5.5 GP Data2

This register supports read and write commands and allows it to store custom data. Data written to the GP Data2 register can be retrieved after a power loss.

Increment or Decrement commands to this register set the CMDERR bit of the STATUS register in SPI mode or are not acknowledged (NACK) in $I^2C$ mode.

**REGISTER 5-5: GP DATA0 REGISTER (ADDRESS 07H)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | D9 | D8 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-10 Unimplemented at this time. Always reads as ‘0’.

bit 9-0 **D9 – D0:** NV general data storage bits

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## 5.6 STATUS Register

Read the 7-bit STATUS register to determine the status of MCP41U83.

**Note:** The CMDERR bit is available only in SPI communication mode.

**REGISTER 5-6: STATUS REGISTER (ADDRESS 08H)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-1 | R-0 |
|---|---|---|---|---|---|---|---|
| — | ECED | SPIWDT(1) | CMDERR(1),(2) | CRCERR(2) | SRST(2) | POR(2) | MTPMA |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

**Note 1:** Available only in SPI communication mode.

**2:** This bit is cleared every time the STATUS register is read.

bit 15-7 Unimplemented at this time. Always reads as '0'.

bit 6 **ECED:** Error Correction Conducted (ECC) status bit.
This bit indicates whether or not an internal error correction was conducted by the NV memory. Its value does not influence device functionality. Ignore the bit as it can change value during device operation.
1 = Error correction conducted.
0 = No error correction conducted.

bit 5 **SPIWDT:** SPI Watchdog Timer (WDT) status bit.
Available when MCP41U83 operates in SPI communication mode.
This bit is set when the SPI was reset by multiple clock pulses. For details, see Figure 7-11.
1 = SPIWDT triggered.
0 = SPIWDT not triggered.

bit 4 **CMDERR:** Command Error status bit.
Available when MCP41U83 operates in SPI communication mode.
This bit indicates whether or not a command error occurred since the most recent read of the STATUS register.
1 = A command error occurred since the most recent STATUS register read.
0 = No command error occurred since the most recent STATUS register read.

bit 3 **CRCERR:** Cyclic Redundancy Check (CRC) Error status bit.
This bit indicates whether or not a CRC error occurred since the most recent read of the STATUS register.
The indication is valid only when the CRCEN bit is set in the CRC Register and MCP41U83 is not in Daisy-Chain mode while operating in SPI communication mode.
1 = CRC error occurred.
0 = No CRC error occurred.

bit 2 **SRST:** Software Reset status bit.
This bit indicates whether or not a software reset triggered by a Write command to the RESET register was detected.
1 = A software reset triggered by a Write command to the RESET register was detected.
0 = No software reset detected since the most recent read of the RESET register.


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**REGISTER 5-6: STATUS REGISTER (ADDRESS 08H) (CONTINUED)**

bit 1 **POR:** Power-on Reset (POR) event status bit.
This bit indicates whether or not a POR event occurred.
1 = POR occurred.
0 = No POR occurred.

bit 0 **MTPMA:** Multiple-Time Programming (MTP) memory write status bit.
This bit indicates whether or not a MTP write or start-up procedure is currently active.
1 = MTP write or start-up procedure in progress. Subsequent writes must wait for the current operation to complete.
0 = No MTP write or start-up currently active.

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## 5.7 LOCK Register

The LOCK register allows or disallows to modify the values of Volatile or NV registers.

This register supports Write and Read commands. All other commands set the CMDERR bit of the STATUS register in SPI mode or are not acknowledged (NACK) in $I^2C$ mode.

If the LOCKNV or LOCKV bit is set, Write commands to a memory location from the locked category does not change the target value.

Commands that try to change a locked register result in setting the CMDERR bit in the STATUS register when in SPI mode or the commands are not acknowledged (NACK) in $I^2C$ mode.

**REGISTER 5-7: LOCK REGISTER (ADDRESS 09H)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | LOCKNV | LOCKV |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-2 Unimplemented at this time. Always reads as '0'.

bit 1 **LOCKNV:** Nonvolatile memory (MTP memory) access lock bit.
Disable Write operations for NV registers (NV Wiper0, GP Data0, GP Data1 and GP Data2).
1 = NV registers cannot be modified.
0 = NV registers can be modified.

bit 0 **LOCKV:** Volatile memory (RAM memory) access lock bit.
Disable Write operations for volatile registers (Wiper0 and TCON0).
1 = Volatile registers cannot be modified.
0 = Volatile registers can be modified.


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## 5.8 TCON0 Register

The Terminal Control (TCON0) register has six bits (three bits for each Wiper).

Write to this register to connect or disconnect the resistor ladder terminals from the pins of MCP41U83.

Read this register to retrieve the terminal-to-pin connection status.

Increment or Decrement commands to this register set the CMDERR bit of the STATUS register in SPI mode or are not acknowledged (NACK) in $I^2C$ mode.

On POR or software resets, MCP41U83 sets all the bits in this register to '0' and connects all the terminals to the resistor ladder. To disconnect the resistor ladder from the terminal pin, the Controller must update the TCON0 register with the desired value.

**REGISTER 5-8: TCON0 REGISTER (ADDRESS 0AH)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | R0A | R0W | R0B |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-3 Unimplemented at this time. Always reads as '0'.

bit 2 **R0A:** Resistor Network 0 Terminal A (P0A pin) disconnect control bit.
This bit controls whether or not the P0A pin connects to Resistor Network 0.
1 = P0A pin does not connect to Resistor Network 0.
0 = P0A pin connects to Resistor Network 0.

bit 1 **R0W:** Resistor Network 0 Wiper Terminal (P0W pin) disconnect control bit.
This bit controls whether or not the P0W pin connects to Resistor Network 0.
1 = P0W pin does not connect to Resistor Network 0.
0 = P0W pin connects to Resistor Network 0.

bit 0 **R0B:** Resistor Network 0 Terminal B (P0B pin) disconnect control bit.
This bit controls whether or not the P0B pin connects to Resistor Network 0.
1 = P0B pin does not connect to Resistor Network 0.
0 = P0B pin connects to Resistor Network 0.

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## 5.9 SYNC Register

The Synchronization (SYNC) register enables or disables the synchronization of Volatile Wiper register operations with an external event or between channels.

Read this register to retrieve the current configuration for the synchronization.

Increment or Decrement commands to this register set the CMDERR bit of the STATUS register in SPI mode or are not acknowledged (NACK) in $I^2C$ mode.

**Note:** All the bits of the SYNC register are valid only for the Volatile Wipers.

**REGISTER 5-9: SYNC REGISTER (ADDRESS 0BH)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | WLAT(1) | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

**Note 1:** Reading the wiper registers returns a different value based on the value of the WLAT bit.
- WLAT = 0 → Reads the value latched to the resistor ladder (actual position).
- WLAT = 1 → Reads the value written to the wiper register.

bit 15-3 Unimplemented at this time. Always reads as '0'.

bit 2 **WLAT:** Write Latch control bit.
This bit controls whether or not new values written to the volatile wiper registers are also written to the corresponding resistor network.
1 = New values written to the volatile wiper registers are not written to the corresponding resistor network. This continues to occur until the WLAT bit is cleared.
0 = New values written to the volatile wiper register are also written to the corresponding resistor network.

bit 1-0 Unimplemented at this time. Always reads as '0'.


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## 5.10 CRC Register

The Cyclic Redundancy Check (CRC) register enables or disables the CRC feature.

Read this register to retrieve the current status of the CRC feature.

Increment or Decrement commands to this register set the CMDERR bit of the STATUS register in SPI mode or are not acknowledged (NACK) in $I^2C$ mode.

**Note:** CRC is available in both the SPI and $I^2C$ modes.

**REGISTER 5-10: CRC REGISTER (ADDRESS 0CH)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | CRCEN(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

**Note 1:** CRC is disabled by hardware once MCP41U83 enters Daisy-Chain mode. The CRCEN bit does not have any effect in Daisy-Chain mode.

bit 15-1 Unimplemented at this time. Always reads as ‘0’.

bit 0 **CRCEN:** Cyclic Redundancy Check (CRC) enable bit.
This bit enables or disables the CRC feature.
1 = CRC enabled.
0 = CRC disabled.

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## 5.11 RESET Register

The RESET register triggers a MCP41U83 software reset when written with a special value. When this occurs, the SRST bit in the STATUS register is set by hardware.

The RESET Register is write-only. Read, Increment or Decrement commands to this register set the CMDERR bit of the STATUS register in SPI mode or are not acknowledged (NACK) in $I^2C$ mode.

On POR or software resets, the Controller differentiates the reset type by reading the SRST bit of the STATUS register. If the reset was triggered by a software reset command, the SRST bit is set.

**REGISTER 5-11: RESET REGISTER (ADDRESS 0DH)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
|---|---|---|---|---|---|---|---|
| SWRSTVAL[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

**Note 1:** In SPI Daisy-Chain mode, a reset instruction does not exit the Daisy-Chain mode.

bit 15-8 Unimplemented at this time. Always reads as ‘0’.

bit 7-0 **SWRSTVAL:** Software Reset value bits.
Writing `0A5h` to this register location triggers a MCP41U83 software reset and sets the SRST bit of the STATUS register, indicating a software reset has occurred.
This is a write-only register that only accepts the predefined `0A5h` reset value. Writing a different value than the predefined value has no effect. Thus, the CMDERR bit of the STATUS register is not set.


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## 5.12 NV W0 Count Register

The NV W0 Count register is read-only. Read this register to retrieve the number, in binary, of write cycles executed on the NV Wiper0 register.

Write, Increment or Decrement commands to this register set the CMDERR bit of the STATUS register in SPI mode or are not acknowledged (NACK) in $I^2C$ mode.

**REGISTER 5-12: NV W0 COUNT REGISTER (ADDRESS 15H)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | C9 | C8 |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-10 Unimplemented at this time. Always reads as ‘0’.

bit 9-0 **C9 – C0:** The number, in binary, of write cycles executed on the NV Wiper0 register.

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## 5.13 Data0 Count Register

The Data0 Count register is read-only. Read this register to retrieve the number, in binary, of write cycles executed on the GP Data0 register.

Write, Increment or Decrement commands to this register set the CMDERR bit of the STATUS register in SPI mode or are not acknowledged (NACK) in $I^2C$ mode.

**REGISTER 5-13: DATA0 COUNT REGISTER (ADDRESS 19H)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | C9 | C8 |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-10 Unimplemented at this time. Always reads as ‘0’.

bit 9-0 **C9 – C0:** The number, in binary, of write cycles executed on the GP Data0 register.


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## 5.14 Data1 Count Register

The Data1 Count register is read-only. Read this register to retrieve the number, in binary, of write cycles executed on the GP Data1 register.

Write, Increment or Decrement commands to this register set the CMDERR bit of the STATUS register in SPI mode or are not acknowledged (NACK) in $I^2C$ mode.

**REGISTER 5-14: DATA1 COUNT REGISTER (ADDRESS 1BH)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | C9 | C8 |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-10 Unimplemented at this time. Always reads as ‘0’.

bit 9-0 **C9 – C0:** The number, in binary, of write cycles executed on the GP Data1 register.

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## 5.15 Data2 Count Register

The Data2 Count register is read-only. Read this register to retrieve the number, in binary, of write cycles executed on the GP Data2 register.

Write, Increment or Decrement commands to this register set the CMDERR bit of the STATUS register in SPI mode or are not acknowledged (NACK) in $I^2C$ mode.

**Note:** The Data2 Count Register is available only for NV MCP41U83 devices.

**REGISTER 5-15: DATA2 COUNT REGISTER (ADDRESS 1DH)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | C9 | C8 |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-10 Unimplemented at this time. Always reads as ‘0’.

bit 9-0 **C9 – C0:** The number, in binary, of write cycles executed on the GP Data2 register.


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# 6.0 I²C SERIAL INTERFACE

## 6.1 I²C General Considerations

MCP41U83 supports the I²C serial protocol. Its I²C module operates in target mode and does not generate the serial clock signal. For more details, refer to the official I²C specifications.

Figure 6-1 shows the typical I²C interface connections.

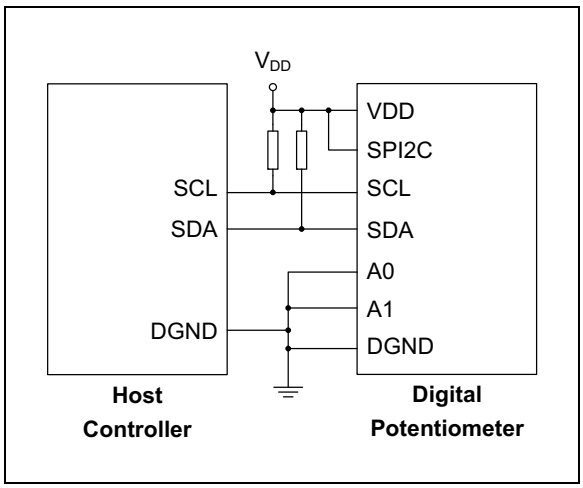



**FIGURE 6-1:** *Typical I²C Interface Connections.*

## 6.2 I²C Bus Signals Description

To enable I²C interface mode, connect the SPI2C pin to the MCP41U83's $V_{DD}$.

The I²C interface uses the following four pins:

- SDA – Serial Data
- SCL – Serial Clock
- A0 – Address 0 bit
- A1 – Address 1 bit.

### 6.2.1 SERIAL DATA (SDA)

The Serial Data (SDA) signal is the data signal received or transmitted by MCP41U83.

### 6.2.2 SERIAL CLOCK (SCL)

The Serial Clock (SCL) signal is the clock signal of MCP41U83. Memory read access occurs fast enough that MCP41U83 does not stretch the clock signal.

### 6.2.3 ADDRESS BITS (A1:A0)

The 7-bit I²C target address is generated by combining the internal predefined address bits (`01011b`) with the logic levels of the A1 and A0 hardware pins. The logic states of the A1 and A0 pins must be static:

- The pins must connect to either $V_{DD}$ or DGND.
- The pins' respective levels must be stable at POR and not change during operation.

## 6.3 I²C Operation

The I²C module of MCP41U83 is compatible with the official I²C specifications developed by Philips Semiconductors (now NXP Semiconductors). Following are some of the module's features:

- 7-bit target addressing
- Supports three clock rate modes:
  - Standard mode: clock rates up to 100 kHz
  - Fast (FS) mode: clock rates up to 400 kHz
  - High-speed (HS) mode: clock rates up to 3.4 MHz
- Supports Multi-Controller applications
- Supports General Call addressing.

MCP41U83 does not support the 10-bit addressing mode and clock stretching features of the I²C protocol.

## 6.4 I²C Target Addressing

The Controller starts communication by sending a Start bit and then a Control byte that consists of the 7 bits of the target address followed by the R/W bit. The R/W bit indicates the transmission direction of the SDA line for the bytes that follow after the Control byte. This is valid only until one of the following conditions occurs:

- START (`S`)
- Repeated START (`Sr`)
- STOP (`P`).

During the Acknowledge cycle following the Control byte, the target device that matches the address in the Control byte sends the `ACK` (`A`) bit. All other devices connected to the I²C bus must reply with `NACK` ($\overline{A}$).

Figure 6-2 shows the start sequence and the control byte format containing the seven address bits and the Read/Write bit.

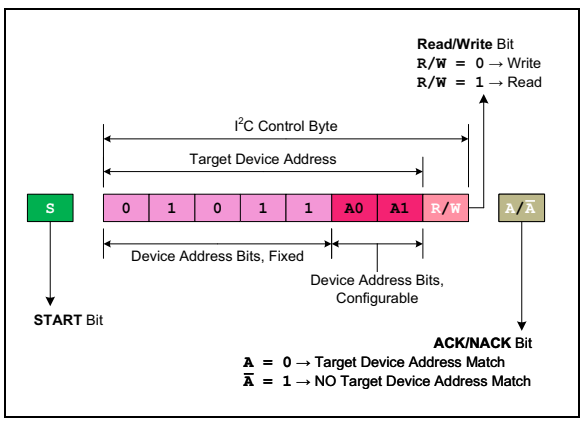



**FIGURE 6-2:** *Target Device Address Bits of the I²C Control Byte.*

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## 6.5 Slope Control

MCP41U83 implements slope control on SDA output. As the device transitions from High-Speed (HS) to Fast (FS) mode, the slope control parameter changes from the HS specification to the FS specification.

When operating in FS or HS mode, MCP41U83 uses spike suppression and Schmitt trigger circuits at the SDA and SCL input pins.

## 6.6 High-Speed (HS) Mode

The I²C specification requires devices to be *activated* to operate in HS (3.4 Mb/s) mode. To activate a device, the Controller sends a special byte after the Start bit called the High-Speed Controller Code (HSCC).

As per the I²C specification, MCP41U83 devices do not acknowledge this byte. However, upon receiving this byte, MCP41U83 switches to HS mode and can now communicate at up to 3.4 Mb/s on the SDA and SCL lines. MCP41U83 switches out of HS mode on the next STOP condition.

The High-Speed Controller Code is sent as follows:

1. Controller sends a START (S) condition.
2. High-Speed Select Byte = HSCC (`00001XXXb`). The `XXX` bits are unique to the HS mode Controller.
3. No ACK bit from the target.
4. Controller sends a Repeated START (Sr) condition.

After switching to HS mode, the next transferred byte is the I²C control byte that specifies with what the device to communicate and any number of data bytes plus acknowledgments. The Controller can then either issue an Repeated Start bit to address a different HS device or a Stop bit to return the current device to Fast or Standard mode. After the Stop bit, any other Controller device part of a Multi-Controller system can arbitrate the I²C bus.

Figure 6-3 illustrates the HS mode communication sequence.

For more information on the HS mode or other I²C modes, please refer to the NXP I²C specifications.

**Note:** If CRCEN = 1, then the HS Select byte (`00001XXXb`) is not used for calculating the CRC checksum. The Controller does not send a checksum byte after the HS Select byte (`0001XXXb`).

### 6.6.1 PULSE GOBBLER

The Pulse Gobbler on the SCL pin is automatically adjusted to suppress spikes < 10 ns during HS mode.

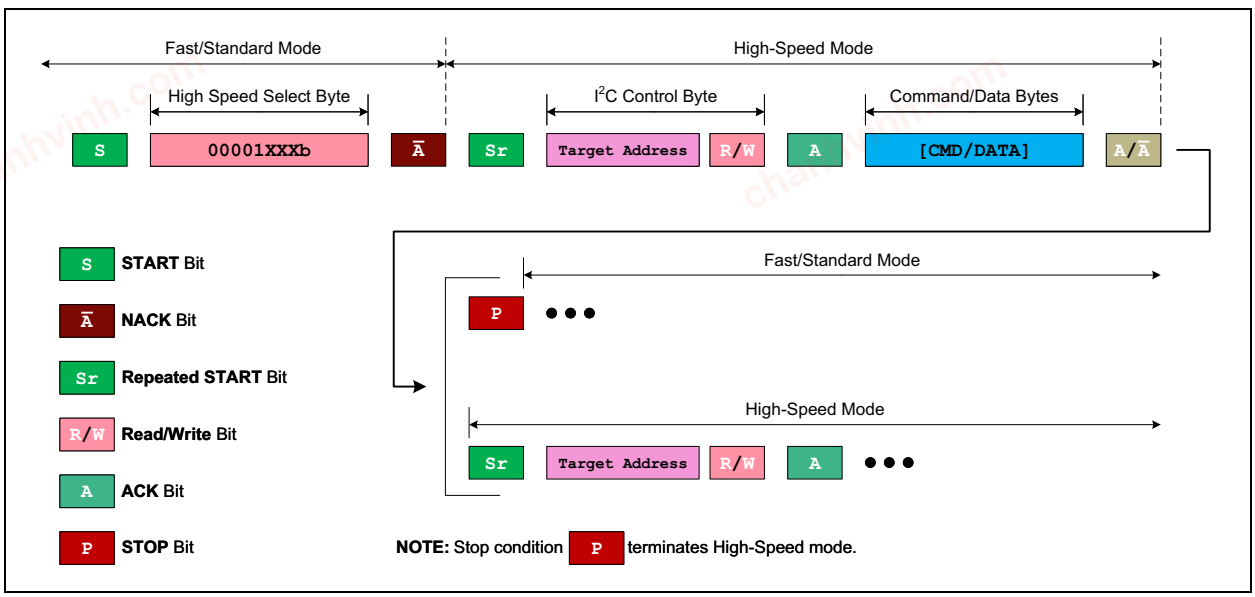



**FIGURE 6-3:** *I²C High-Speed (HS) Mode Communication Sequence.*


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### 6.6.2 GENERAL CALL

The General Call feature allows for multiple $I^2C$ digital potentiometers to operate synchronously on the same $I^2C$ bus.

The General Call is started when the Controller device sends a Start (S) bit followed by a General Call Address byte (00h). Devices that implement General Call addressing do ACK this byte, while the other devices connected to the same $I^2C$ bus do NACK and ignore the following bytes until a Repeated START (Sr) or STOP (P) condition occurs. After the General Call Address byte, the Controller transmits one or more General Call Command bytes.

Some of the General Call commands are reserved as specified by the $I^2C$ standard, while others are device specific. MCP41U83 devices support the General Call commands specified in Table 6-1. Unsupported values for the Command byte are NACK'ed.

The General Call command sequence illustrated in Figure 6-4 is a Microchip extension to the General Call format.

**Note:** MCP41U83 only supports one Command byte for every issued General Call address.

**TABLE 6-1: GENERAL CALL COMMANDS**

| Operation (General Call Address = 00h) | 7-bit Command [C6:C0] | Command Byte | First Data Byte | Second Data Byte |
|---|---|---|---|---|
| Write Volatile Wiper0 | 0000100 | 08h | [D9:D8] | [D7:D0] |
| Write NV Wiper0 | 0001100 | 18h | [D9:D8] | [D7:D0] |
| Write GP Data0 | 0010100 | 28h | [D9:D8] | [D7:D0] |
| Write GP Data1 | 0011000 | 30h | [D9:D8] | [D7:D0] |
| Write GP Data2 | 0011100 | 38h | [D9:D8] | [D7:D0] |
| Write LOCK | 0100100 | 48h | [D9:D8] | [D7:D0] |
| Write TCON0 | 0101000 | 50h | [D9:D8] | [D7:D0] |
| Write SYNC | 0101100 | 58h | [D9:D8] | [D7:D0] |
| Write CRC | 0110000 | 60h | [D9:D8] | [D7:D0] |
| Write RESET | 0110100 | 68h | [D9:D8] | [D7:D0] |
| Increment Wiper0 | 0000101 | 0Ah | N/A | N/A |
| Decrement Wiper0 | 0000110 | 0Ch | N/A | N/A |

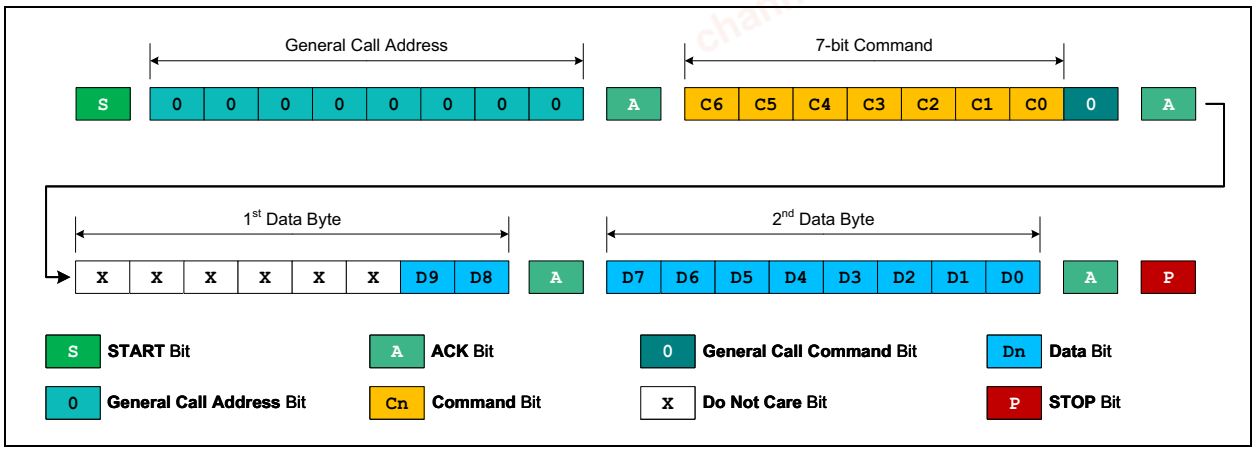



**FIGURE 6-4:** *General Call Command Sequence.*

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## 6.7 I²C Device Commands

Read or modify the memory of MCP41U83 using the following four basic I²C commands:

1. I²C Write Data
2. I²C Read Data
3. I²C Increment Wiper
4. I²C Decrement Wiper.

**Note:** Depending on memory location, MCP41U83 supports all or only some of the commands in Table 6-2.

**TABLE 6-2: COMMAND BYTE OVERVIEW**

| [C2:C0] Bits | Command | Comments |
|---|---|---|
| 00Xb | Write Data | |
| 11Xb | Read Data | |
| 010b | Increment Wiper | Wiper value + 1 |
| 100b | Decrement Wiper | Wiper value – 1 |

### 6.7.1 COMMAND BYTE

Commands and their target addresses are encoded as a single byte. The Command byte contains two data fields, as illustrated in Figure 6-5:

- Register Address, contained in the Command byte's [R4:R0] bits.
- Operation, encoded in the Command byte's [C2:C0] bits.

Additionally, Read and Write memory commands require two extra data bytes to complete.

When CRC is enabled, all command formats change to accommodate the additional checksum byte.

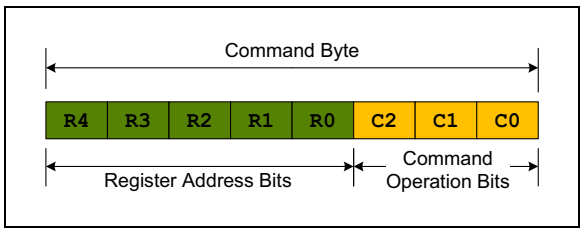



**FIGURE 6-5:** *I²C Command Byte Format.*

### 6.7.2 DATA BYTE

Only Read and Write commands have Data Byte(s).

### 6.7.3 ERROR CONDITION

If the register address bits and command operation bits are an invalid combination, then MCP41U83 does NACK across the I²C bus.

Once an error condition occurs, any following bytes are ignored by MCP41U83 until the Controller ends or restarts the current communication, by sending a STOP, START or Repeated START condition.

### 6.7.4 IGNORING AN I²C TRANSMISSION AND "FALLING OFF" THE BUS

MCP41U83 expects to receive only complete, valid I²C commands. If any command is not correctly received (command not recognized as valid because of a bus corruption), MCP41U83 releases the bus. All signals are then ignored until the next valid Start bit and Control byte are received.

### 6.7.5 ABORTING A TRANSMISSION

If the Controller device ends the transmission before the command is complete, MCP41U83 aborts the command execution.

### 6.7.6 I²C WRITE COMMANDS

Write commands to MCP41U83 modify the content of its memory (Volatile or NV). The command format includes the START condition, the I²C Control byte, multiple Command and Data bytes and the STOP (or RESTART) condition.

There are two types of Write commands: Single and Continuous.

#### 6.7.6.1 Single Write to Memory

Single Write commands need four bytes: one Control byte, one Command byte and two Data bytes.

The Control byte contains the device address and the R/W bit. The Command byte encodes the memory address and the command code. Data bytes contain the desired 10-bit wiper position code, right-aligned. Padding bits are ignored.

Writing data to MCP41U83 must occur after the second byte transfer completes, on the rising edge of the Acknowledge cycle. If a STOP or RESTART condition is generated during a data transfer, before the final ACK bit, the data is not written. After the ACK bit, the Controller can initiate the next sequence with a START or RESTART condition or it terminates communication by sending a STOP condition.


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Figure 6-6 illustrates the Single Write command sequence.

For Single Write commands, data transfer from the I²C stream to the any addressed location occurs at the last ACK bit, on the rising edge of the SCL signal.

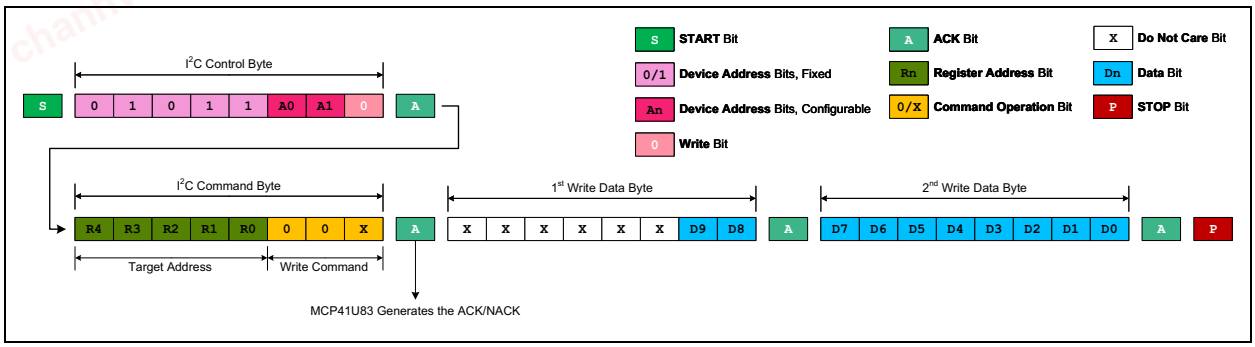



**FIGURE 6-6:** *I²C Single Write Command Sequence.*

### 6.7.6.2 Continuous Write to Volatile Memory

Continuous Write allows writing to volatile memory without repeatedly transmitting the I²C Control Byte for every addressed memory location.

**Note 1:** Continuous Writes are possible only when addressing volatile memory locations.

**2:** Mixing volatile and NV memory addresses in a Continuous Write command is not allowed.

**3:** When CRC is enabled, MCP41U83 does not support Continuous Write commands.

Figure 6-7 shows an example sequence for three memory locations. The Continuous Write commands do not need to be to the same volatile memory address. The sequence ends with the Controller device sending a STOP or RESTART condition.

For Continuous Writes, data transfer from the I²C stream occurs at the last ACK bit, on the rising edge of the SCL signal, for every individual memory location in the command sequence (after the single command byte and the two data bytes).

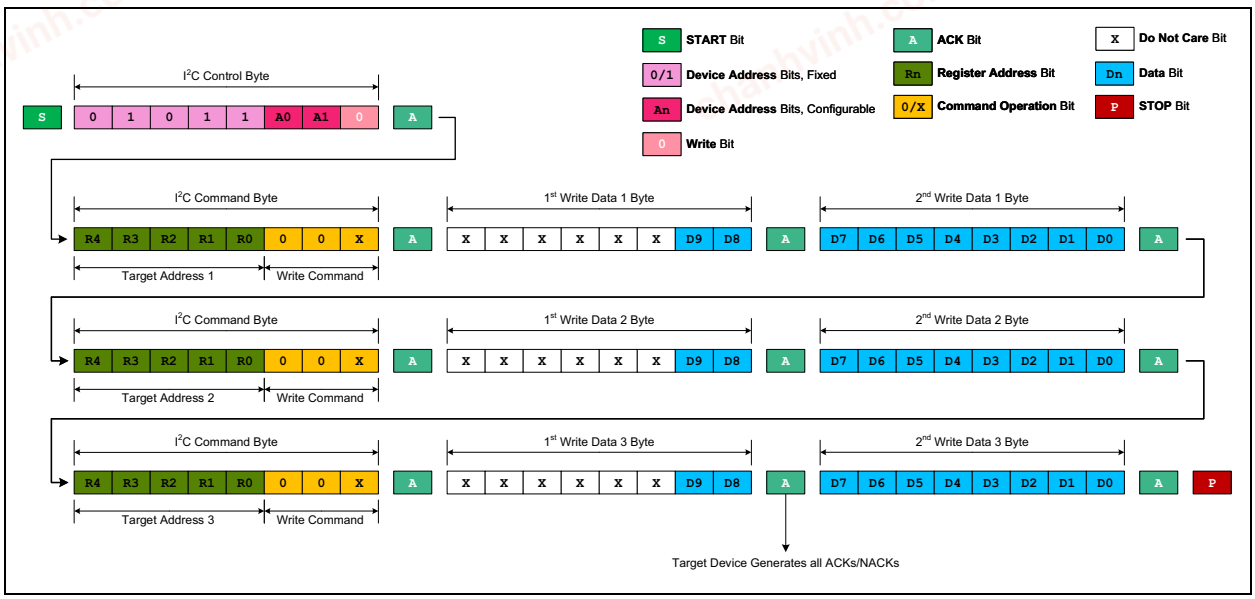



**FIGURE 6-7:** *I²C Continuous Write Command Sequence Example.*

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### 6.7.7 I²C READ COMMANDS

Read commands to MCP41U83 retrieve the content of its memory (Volatile or NV). Read commands have three formats: Random Single, Last Address Single and Last Address Continuous.

**Note 1:** MCP41U83 retains the last received "device memory address". MCP41U83 does not "corrupt" the internal "device memory address" after Repeated START or STOP conditions.

**2:** MCP41U83 is responsible for the A/$\overline{A}$ signal after the Control byte and the Address/Command byte.

**3:** The Controller is responsible for the A/$\overline{A}$ signal of the read data bytes. When the Controller does NACK, MCP41U83 releases the bus so the Controller can generate a STOP or Repeated START condition.

#### 6.7.7.1 Single Read of a Random Address

The Single Read of a random address allows reading any individual register location, volatile or NV.

Figure 6-8 illustrates the Read Random Address command sequence.

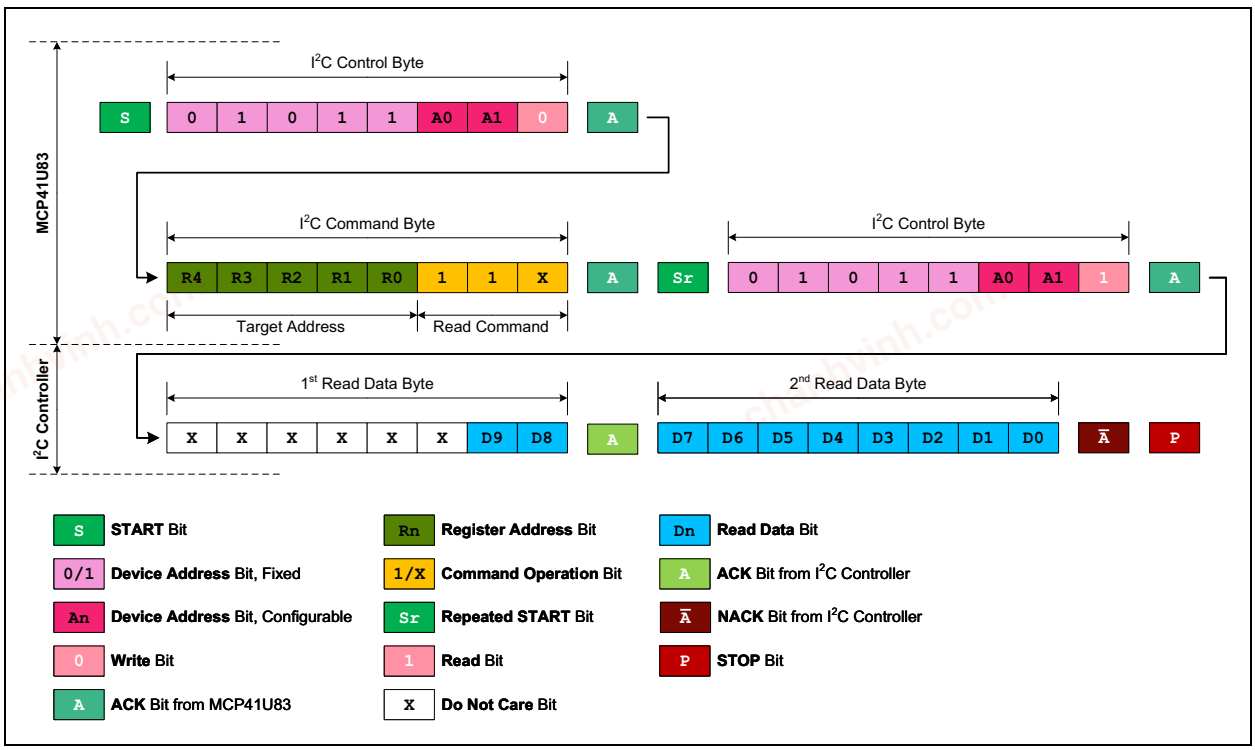



**FIGURE 6-8:** *I²C Read Random Address Command Sequence.*


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### 6.7.7.2 Single Read of the Last Memory Address

For Single Read commands, the Controller sends a STOP or RESTART condition after the data byte is received from the target. The next I²C Read command (following the Control byte) does not require sending the Address/Command byte to read same memory location (poll for a register).

**Note:** The address pointer is internally stored for any valid Write, Read, Increment or Decrement command. Thus, Read Last Memory Address is valid when it follows any of the previously mentioned commands.

Figure 6-9 illustrates the Read Last Memory Address command sequence.

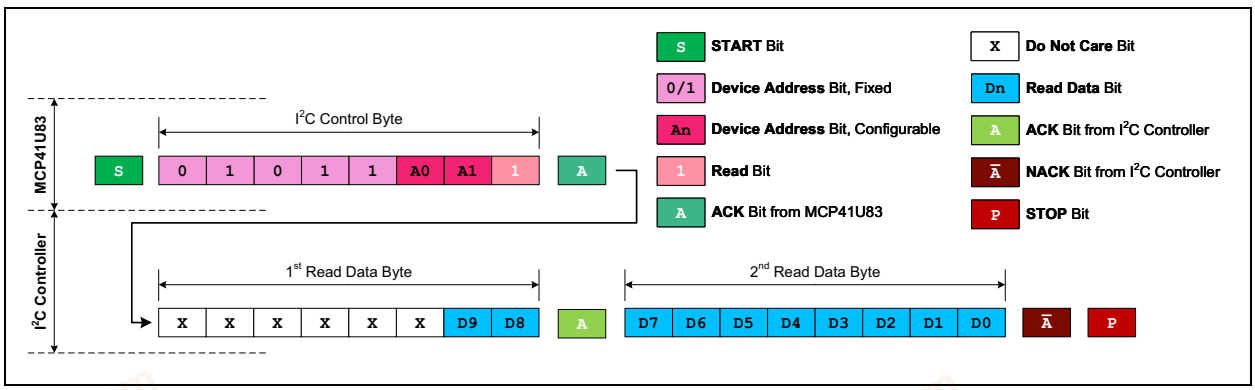



**FIGURE 6-9:** *I²C Read Last Memory Address Command Sequence.*

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### 6.7.7.3 Continuous Read of the Last Memory Address

Continuous Read of the Last Memory Address commands repeatedly read multiple times (without resending the Control Byte) the last accessed memory on MCP41U83. Continuous Read commands are useful to read status bits like MTPMA, which changes status only after an MTP Write is complete. The MTP Write operation executes over a variable period of time, depending on external conditions.

| **Note:** | MCP41U83 does not support Continuous Read commands while CRC is enabled. |
|---|---|

Continuous Read commands are similar to Single Read. The internal address pointer is stored. Thus, there no STOP or RESTART condition is needed after every data read. The Controller continues to read the same address multiple times, until it ends communication by sending a NACK and then a STOP or RESTART condition.

Figure 6-10 shows the sequence of three Continuous Reads of the Last Memory Address.

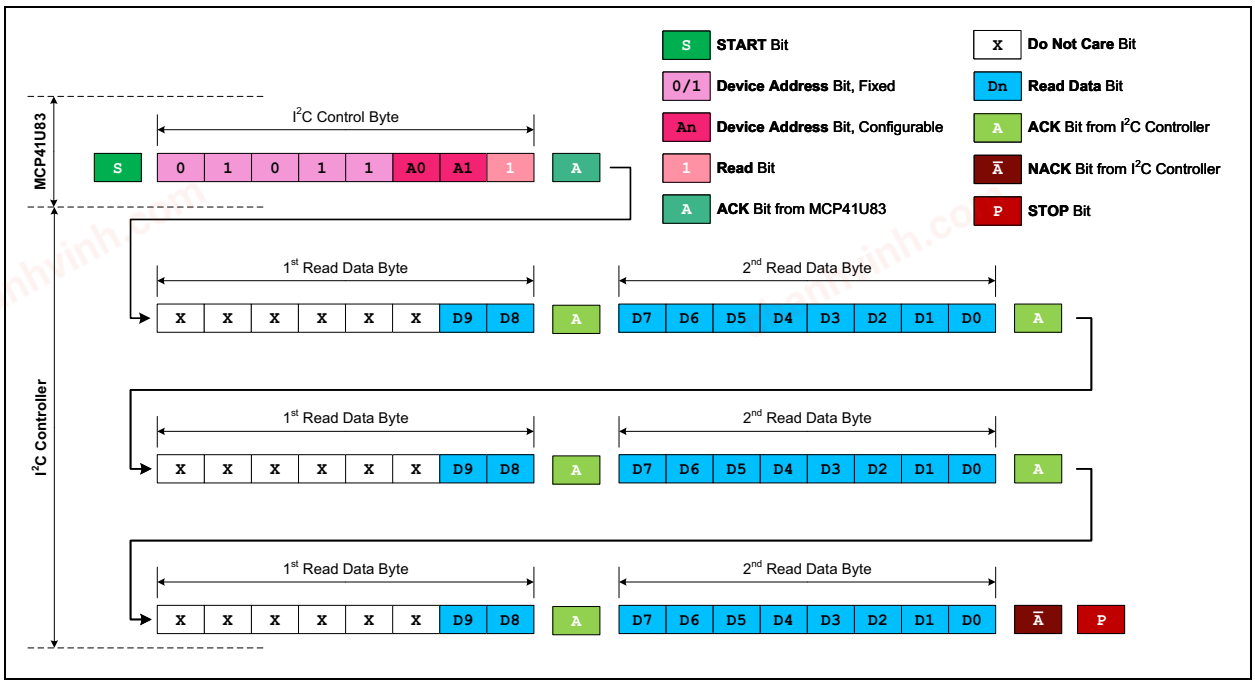



**FIGURE 6-10:** *I²C Continuous Read of Last Memory Address Command Sequence.*


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### 6.7.8 INCREMENT/DECREMENT WIPER POSITION COMMANDS

Increment/Decrement commands allow to quickly and easily modify the volatile potentiometer's wiper position by one unit, up or down, with minimal overhead.

Updating the volatile wipers occurs on the rising edge of the ACK clock.

**Note 1:** A Stop bit is not required to terminate the Increment/Decrement command sequence.

**2:** The sequence can change to any other command sequence: Increment/Decrement or Write.

**3:** The Read command needs a Repeated START condition to execute.

#### 6.7.8.1 Incrementing the Wiper Position

Increment commands increase the wiper position value of MCP41U83 by one unit.

The wiper position increments up to a maximum of `3FFh` and no more. Further Increment commands are ignored and the wiper position value remains at `3FFh`. Once the value reaches `3FFh`, MCP41U83 does NACK subsequent Increment commands.

Figure 6-11 illustrates the sequence of four Increment Wiper Position commands.

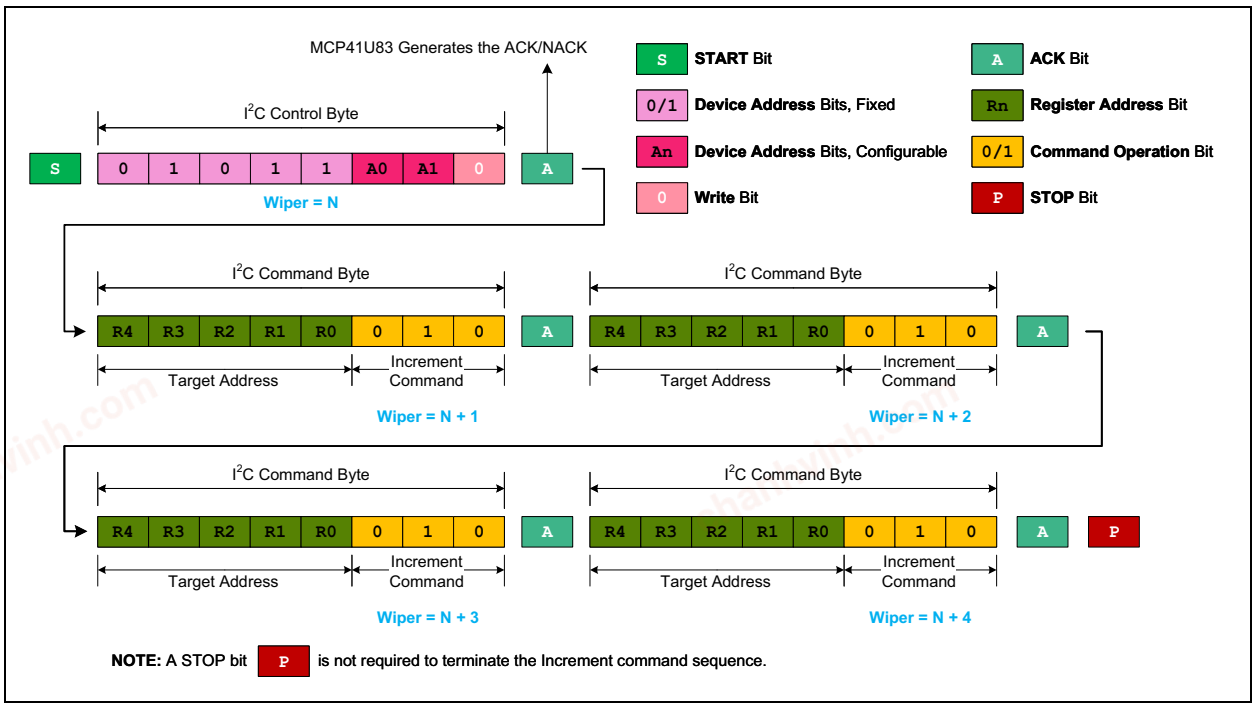



**FIGURE 6-11:** *$I^2C$ Increment Wiper Position Command Sequence.*

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### 6.7.8.2 Decrementing the Wiper Position

Decrement commands decrease the wiper position value of MCP41U83 by one unit.

The wiper position decrements down to a minimum of `000h` and no more. Further Decrement commands are ignored and the wiper position value remains at `000h`. Once the value reaches `000h`, MCP41U83 does NACK subsequent Decrement commands.

Figure 6-12 illustrates the sequence of four Decrement Wiper Position commands.

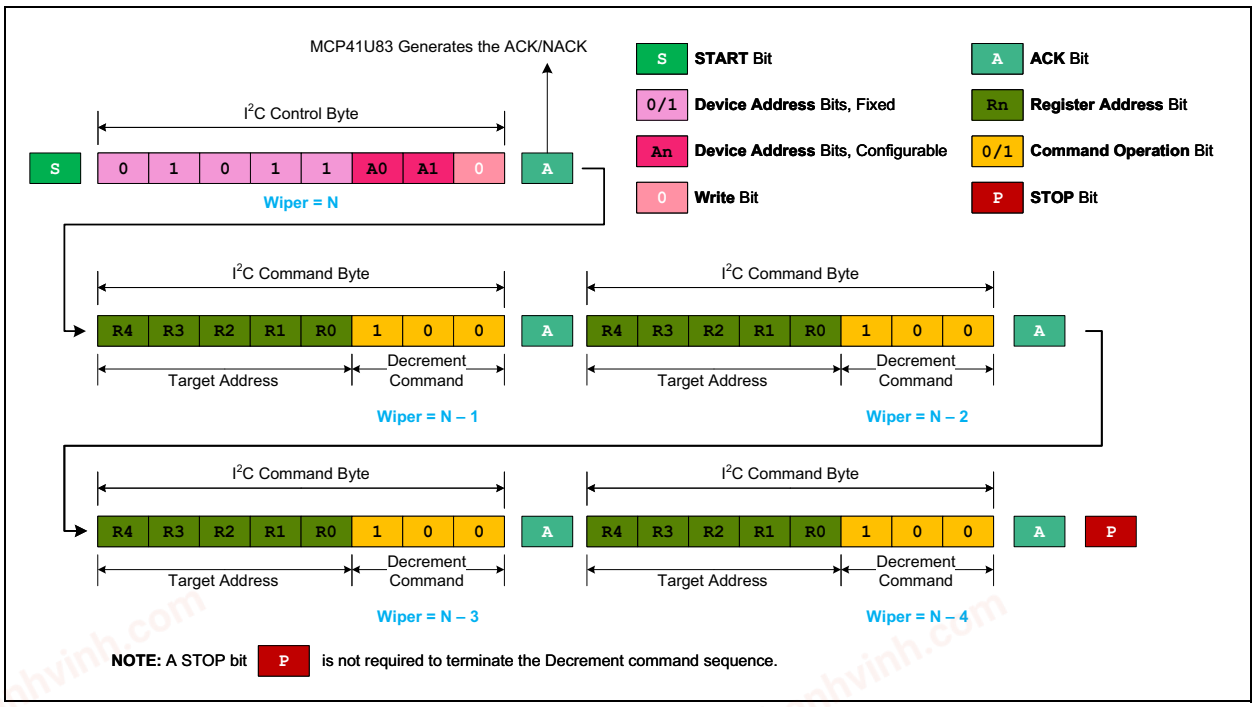



**FIGURE 6-12:** *$I^2C$ Decrement Wiper Position Command Sequence.*


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## 6.8 I²C and Cyclic Redundancy Check (CRC)

A general description of the CRC module is presented in **Section 4.4, "Cyclic Redundancy Check (CRC) Module"**. The following section describes the CRC module's I²C specific functionality.

CRC is supported for all I²C commands, including General Call commands.

**Note 1:** When the CRCEN bit in the CRC register is set (CRCEN = 1), data only updates during the ACK bit, after the CRC byte.

**2:** If the CRCERR bit in the STATUS register is set (CRCERR = 1), then Wiper registers are not updated and MCP41U83 does NACK after the CRC byte.

**3:** Continuous Write, Increment, Decrement commands are not allowed when CRC is enabled.

**4:** CRC calculation does not include ACK, START and Repeated START conditions.

**5:** If CRC is enabled, then the Controller must always end the communication sequence with a STOP condition.

### 6.8.1 I²C WRITE, INCREMENT AND DECREMENT COMMANDS WITH CRC ENABLED

Figure 6-13 shows the I²C Write command sequence with CRC enabled. The Controller sends the CRC checksum after the data to write and it includes the Control byte, Address/Command byte and Data bytes. After the Controller sends the CRC byte, if an error occurs, the CRCERR bit in the STATUS register is set. Also, in this scenario, the last ACK, before the Stop bit, becomes a NACK.

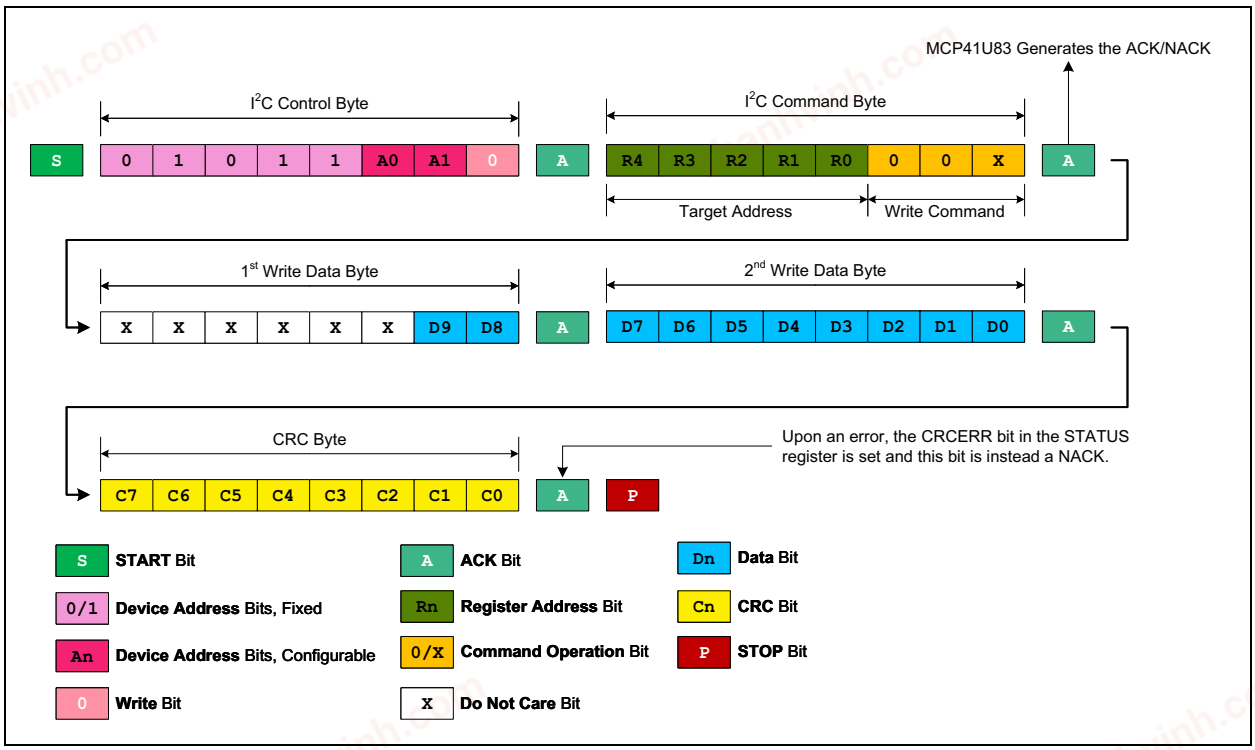



**FIGURE 6-13:** *I²C Write Command Sequence with CRC Enabled.*

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Figure 6-14 and Figure 6-15 show the Increment and Decrement command sequences with CRC enabled. The Controller sends the CRC checksum after the wiper position to increment or decrement and it includes the Control byte and Address/Command byte. After the Controller sends the CRC byte, if an error occurs, the CRCERR bit in the STATUS register is set. Also, in this scenario, the last ACK, before the Stop bit, becomes a NACK.

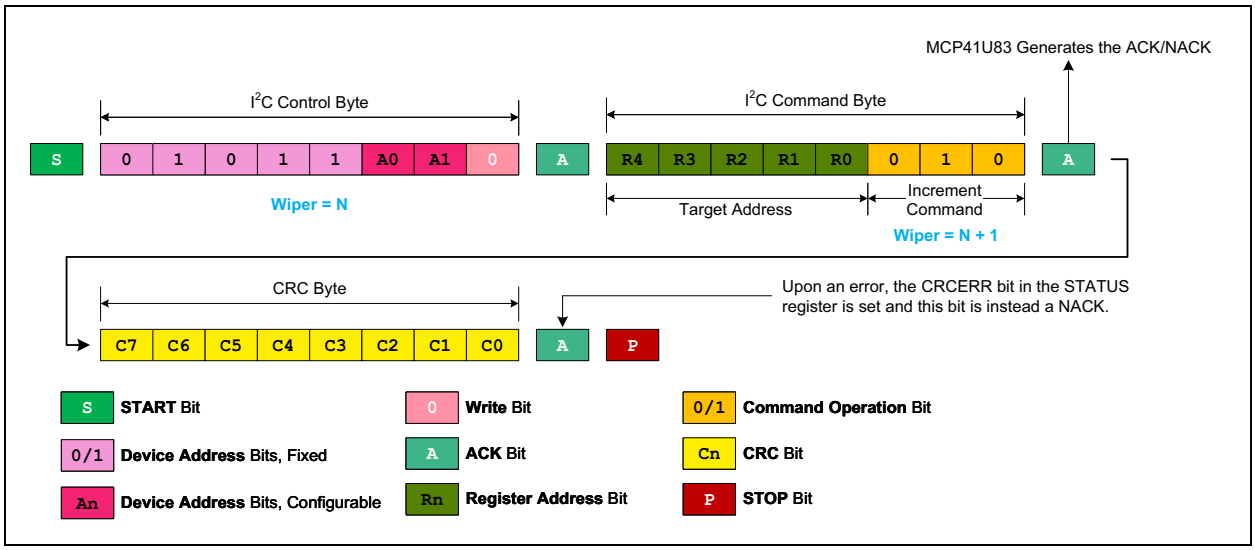



**FIGURE 6-14:** *I²C Increment Command Sequence with CRC Enabled.*

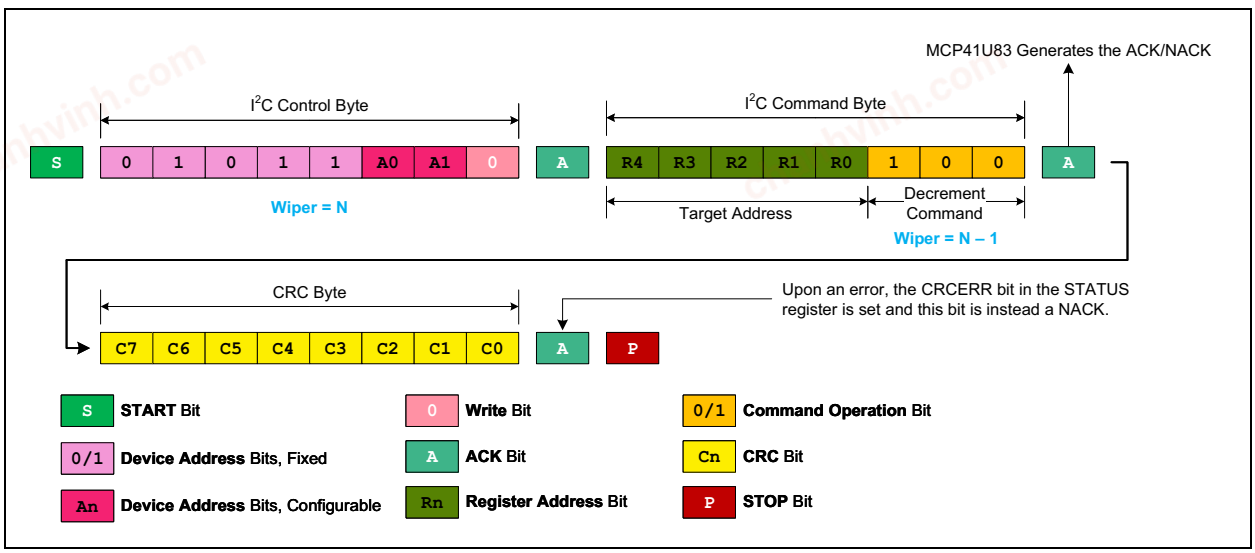



**FIGURE 6-15:** *I²C Decrement Command Sequence with CRC Enabled.*


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### 6.8.2 I²C READ WITH CRC ENABLED

For I²C Read commands, there are two CRC bytes involved. The Controllers sends the first byte and it includes the CRC byte of the Control byte and Address/ Command byte. MCP41U83 sends another CRC byte after the two read data bytes. Its value does not include the Control byte sent by the Controller.

Figure 6-16 illustrates the Read Random Address command sequence with CRC enabled.

For Read Last Memory Address commands, there is only a single CRC byte. MCP41U83 sends the CRC byte and calculates the CRC checksum based only on the two read data bytes.

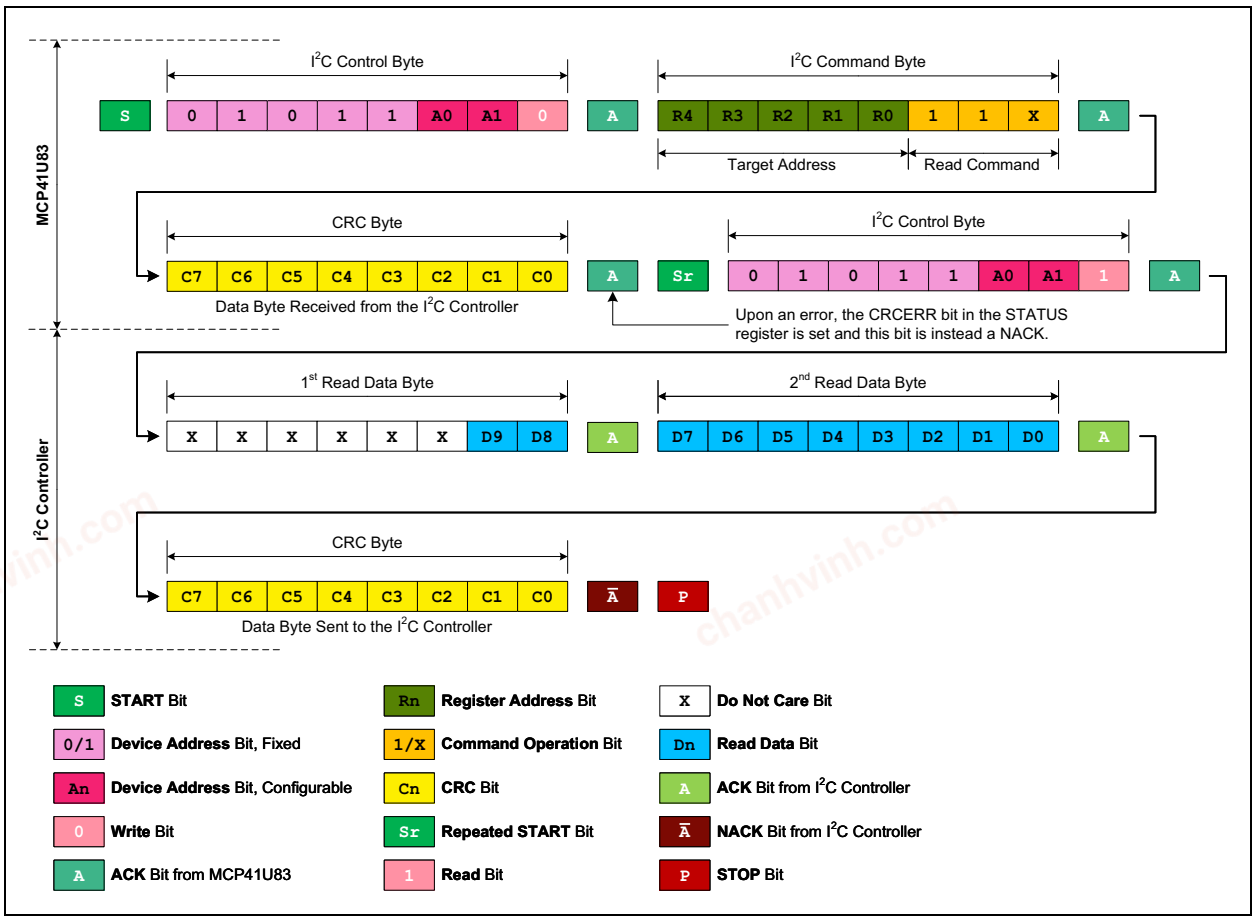



**FIGURE 6-16:** *I²C Read Random Address Command Sequence with CRC Enabled.*

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Figure 6-17 illustrates the Read Last Memory Address command sequence with CRC enabled.

**Note:** After receiving the CRC byte, once the Controller sends a NACK bit, Microchip recommends sending a Stop bit. To read the same location again, repeat the same procedure once more.

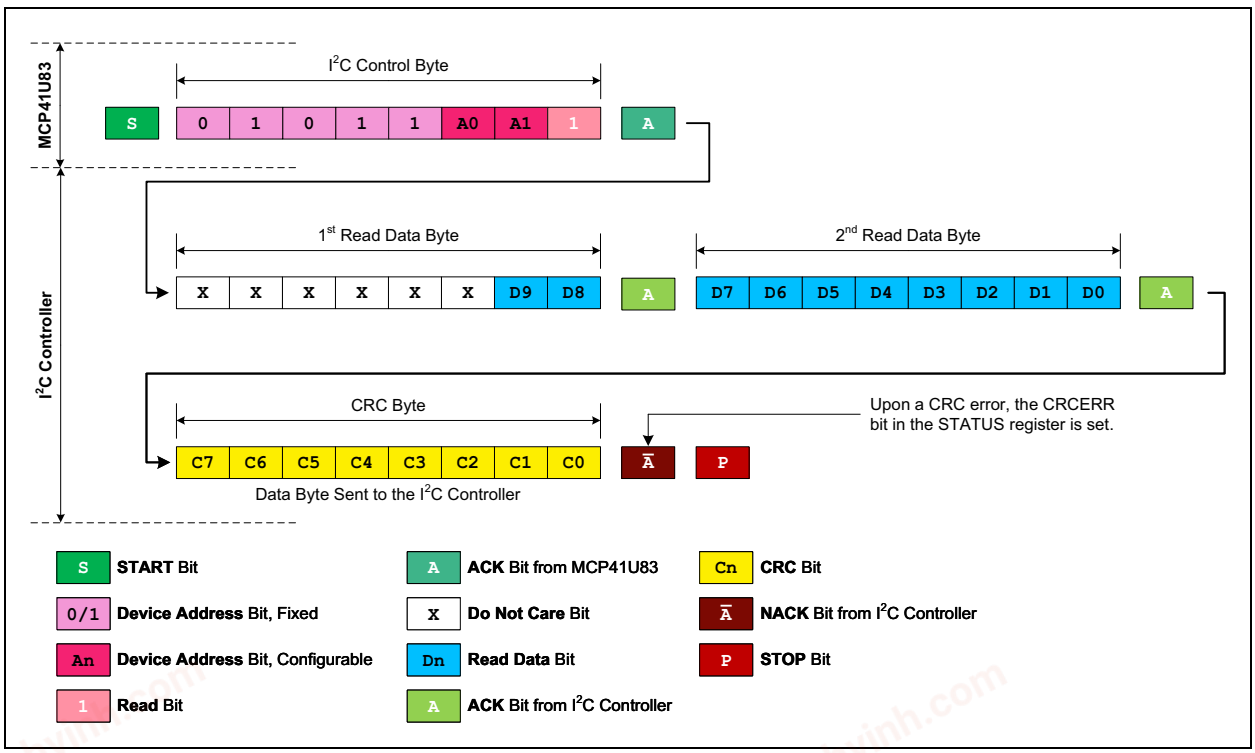



**FIGURE 6-17:** *I²C Read Last Accessed Memory Command Sequence with CRC Enabled.*


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# 7.0 SERIAL PERIPHERAL INTERFACE (SPI)

## 7.1 General Considerations

MCP41U83 supports the SPI serial protocol. Its SPI module operates in peripheral mode and does not generate the serial clock signal. For more details, refer to the official SPI specifications.

Figure 7-1 shows the typical SPI connections.

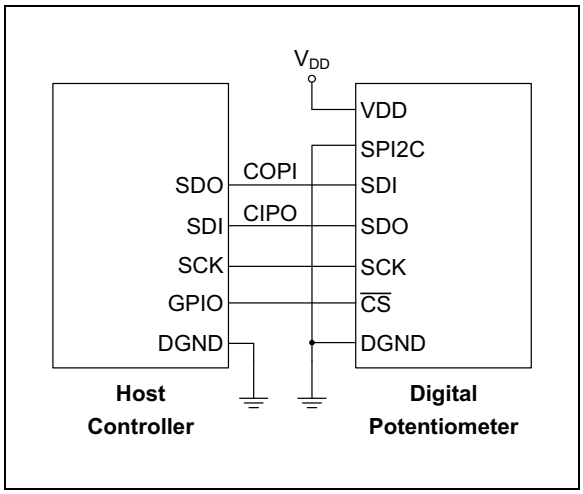



**FIGURE 7-1:** *Typical SPI Connections.*

The SPI module of MCP41U83 supports two standard SPI modes: (0,0) and (1,1). The idle state of the SCK pin ($V_{IH}$ or $V_{IL}$) determines the SPI mode.

## 7.2 SPI Bus Signals Description

To enable SPI mode, connect the SPI2C pin to GND.

The SPI uses the following four pins:

- $\overline{CS}$ – Chip Select
- SDI – Serial Data Input
- SDO – Serial Data Output
- SCK – Serial Clock.

The SPI interface on MCP41U83 works with either 8-bit or 24-bit boundaries depending on the selected command. The $\overline{CS}$ pin frames the SPI commands.

### 7.2.1 $\overline{CS}$ SIGNAL AND $\overline{CS}$ PIN

An SPI Host communicates with several SPI Clients by sharing the connection to the SCK, SDO and SDI lines. The $\overline{CS}$ signal is used to select the specific device and frame a command sequence. To start a command or sequence of commands, the $\overline{CS}$ signal must transition from the inactive state ($V_{IH}$) to the active state ($V_{IL}$).

When the $\overline{CS}$ pin returns to the inactive state ($V_{IH}$), the SPI module resets (including the address pointer). While the $\overline{CS}$ pin is in the inactive state ($V_{IH}$), the serial clock and the data lines are ignored. This allows the SPI Host to interface with other SPI devices using the same SDI, SDO and SCK signals.

The $\overline{CS}$ pin can be grounded (connected to $V_{IL}$) if the Host's SPI interface communicates only with a single device. However, this denies the Host from disabling the device using the $\overline{CS}$ pin.

**Note:** Daisy-Chain mode cannot be used when the $\overline{CS}$ pin is permanently active.

### 7.2.2 SERIAL DATA INPUT (SDI)

The SDI pin is the serial data input of MCP41U83's SPI interface.The SDI pin transfers data from the SPI Host to MCP41U83.

### 7.2.3 SERIAL DATA OUTPUT (SDO)

The SDO pin is the serial data output of MCP41U83's SPI interface. The SDO pin transfers data from MCP41U83 to the SPI Host.

### 7.2.4 SERIAL CLOCK (SCK)

The SCK pin is the serial clock pin of MCP41U83's SPI interface and can also reset the serial interface communication module (for example, if the $\overline{CS}$ pin is permanently connected to $V_{IL}$).

To perform the reset, MCP41U83 must receive 4,096 clock pulses (equivalent to 512 bytes) while keeping the $\overline{CS}$ and SDI pins at $V_{IL}$ (low state), as in Figure 7-2.

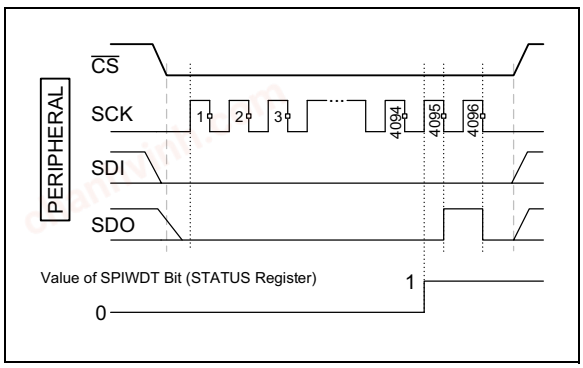



**FIGURE 7-2:** *SPI Reset Sequence.*

Once the SPI interface is reset, the SDO pin transitions to $V_{IH}$ (high state) and the SPIWDT bit in the STATUS register is set. The SDO pin remains high until either the 4,096$^{th}$ falling edge of the clock pulse, in SPI mode (0,0), or until the next $V_{IH}$ to $V_{IL}$ transition of the $\overline{CS}$ signal, in SPI mode (1,1).

**Note 1:** After an SPI reset, the CMDERR bit in the STATUS register is also set. Before sending other commands, read the STATUS register to reset the error bit.

**2:** In Daisy-Chain mode, toggle the $\overline{CS}$ pin once ($V_{IH} \rightarrow V_{IL} \rightarrow V_{IH}$) before the SPI reset to ensure that MCP41U83 devices are not in the data output phase of any Read command.

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## 7.3 Interface Operation Modes

SPI interfaces work in four modes, depending on the signal sampling on both Controller and Peripheral side.

MCP41U83 works in one of the following two modes:

- **Mode (0,0):**
  - The SCK idle state is low ($V_{IL}$)
  - The SDI pin is sampled on the SCK rising edge
  - The SDO pin is driven on the SCK falling edge
- **Mode (1,1):**
  - The SCK idle state is high ($V_{IH}$)
  - The SDI pin is sampled on the SCK rising edge
  - The SDO pin is driven on the SCK falling edge

Figure 7-3 through Figure 7-5 show the different SPI command waveforms for modes (0,0) and (1,1). Figure 7-3 and Figure 7-4 illustrate the Read and Write commands, while Figure 7-5 shows the Increment and Decrement commands.

**Note:** Invalid device command/ registry address combinations can generate errors. When an error occurs, the CMDERR bit in the STATUS register is set. The CMDERR bit is set on the last rising edge of the SCK clock.

Data transfer from the SPI stream to the Wiper occurs on the last rising edge of the SCK clock.

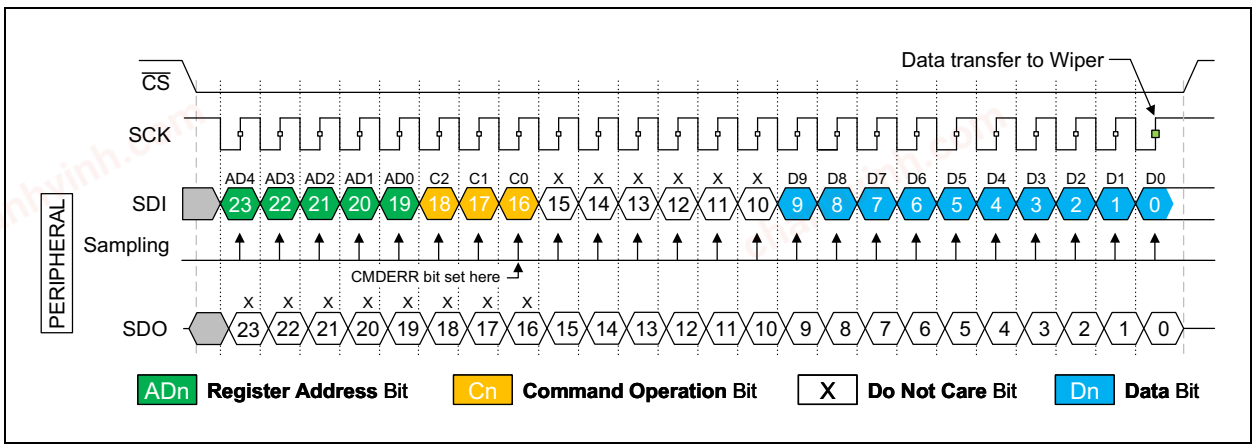



**FIGURE 7-3:** *24-Bit Commands (Write, Read) – SPI Mode (1,1) Waveform.*


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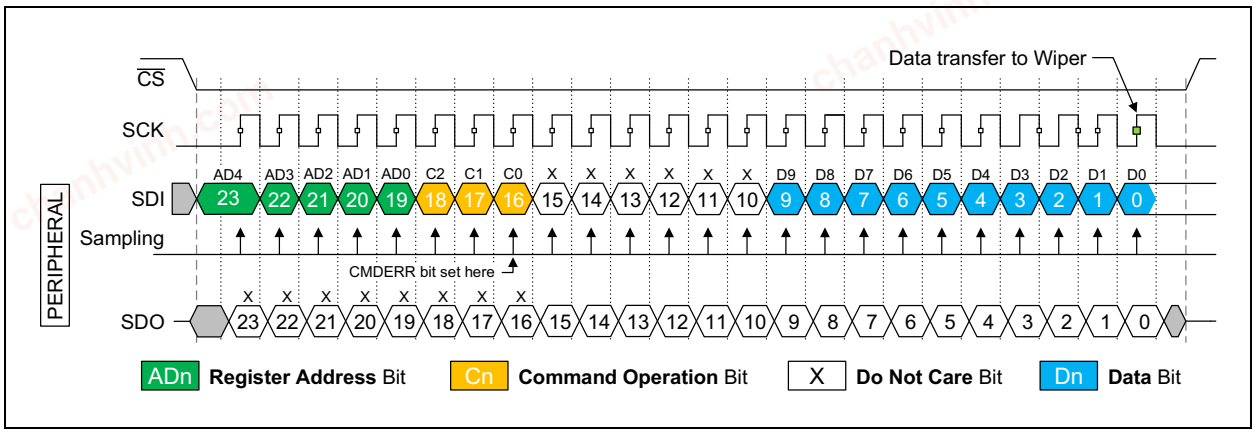



**FIGURE 7-4:** *24-Bit Commands (Write, Read) – SPI Mode (0,0) Waveform.*

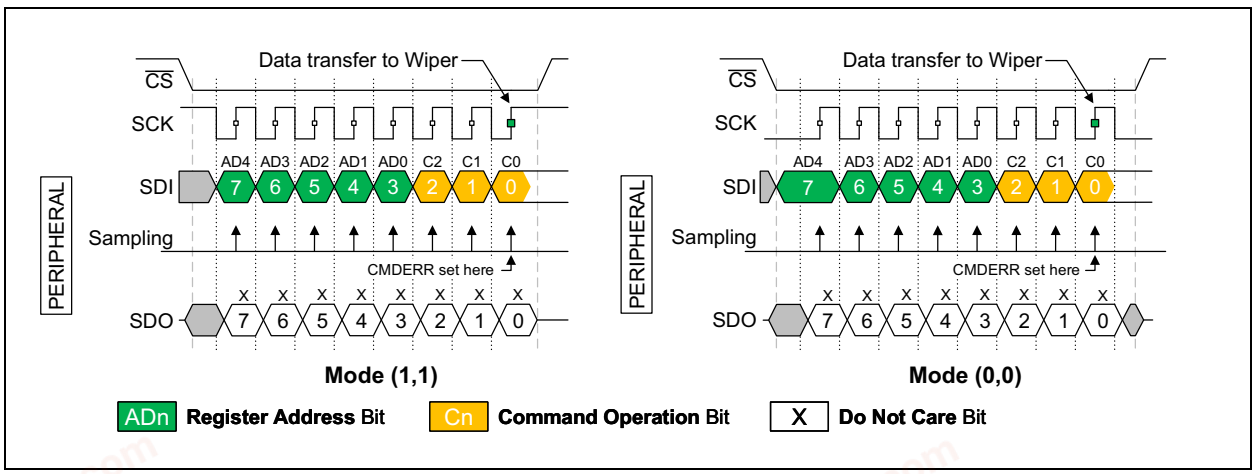



**FIGURE 7-5:** *8-Bit Commands (Increment/Decrement Wiper) Waveforms.*

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## 7.4 SPI Device Commands

Read or modify the memory of MCP41U83 using the following four basic SPI commands:

1. SPI Write Data (24-bit)
2. SPI Read Data (24-bit)
3. SPI Increment Wiper (8-bit)
4. SPI Decrement Wiper (8-bit).

8-bit commands contain a Command byte, while 24-bit commands contain a Command byte and two Data bytes.

Data transfer from the SPI stream to any register occurs on the last rising edge of the SCK signal.

### 7.4.1 GENERAL CONSIDERATIONS

#### 7.4.1.1 Command Byte

The Command Byte has two fields: the Register Address [R4:R0] and the Command Bits [C2:C0], as shown in Figure 7-6.

The SDO pin is driven low as soon as the $\overline{CS}$ signal goes active, while the Command byte is loaded on the SCK signal edge.

Table 7-1 shows the Command byte options.

**TABLE 7-1: COMMAND BYTE OVERVIEW**

| [C2:C0] Bits | Command | Number of Bits | Comments |
|---|---|---|---|
| 00Xb | Write Data | 24 | |
| 11Xb | Read Data | 24 | |
| 010b | Increment Wiper | 8 | Wiper value + 1 |
| 100b | Decrement Wiper | 8 | Wiper value – 1 |

#### 7.4.1.2 Data Byte

Only Read and Write Commands use the Data bytes. The Data bytes are send in two parts: the first byte has the D9 and D8 data bits, while the second byte has data bits D7 through D0, as shown in Figure 7-6.

#### 7.4.1.3 Error Condition

The Command Error (CMDERR) condition indicates that an invalid device command/register address combination was used in the SPI command.

If the CMDERR bit in the STATUS register is set, the $\overline{CS}$ pin must be pulled down to the inactive state to reset the SPI interface. A POR also clears and resets the SPI interface. If the CMDERR bit is set, only Read commands are executed until the bit is cleared.

**Note:** A soft reset clears the CMDERR bit, but it does not reset the SPI interface.

#### 7.4.1.4 Aborting SPI Transmissions

SPI transmissions are executed only when they have the correct number of SCK pulses. Commands are not executed until the complete number of clocks is received.

**Note:** When SPI is idle, force the $\overline{CS}$ pin to the inactive state ($V_{IH}$).

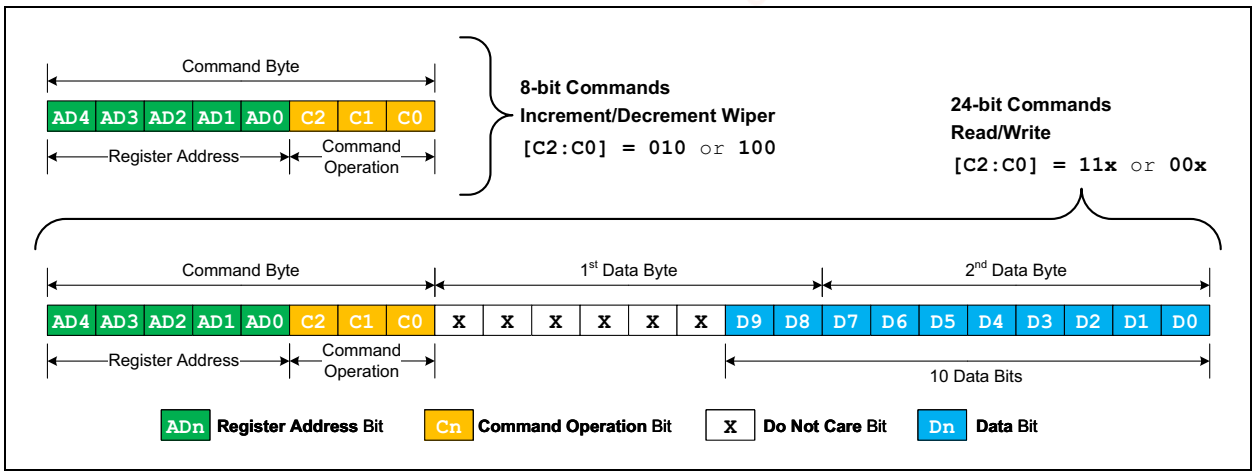



**FIGURE 7-6:** *General SPI 8-Bit and 24-Bit Command Formats.*


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### 7.4.2 SPI WRITE COMMAND

A Write command to MCP41U83 modifies the content of its memory (Volatile or NV). This is a 24-bit command and its format is shown in Figure 7-7.

SPI communication starts with the $\overline{CS}$ pin going active ($V_{IL}$). The 24-bit command sequence (Command byte and Data bytes) is then clocked in on the SCK and SDI pins.

Once all 24 bits are received, the specified register address is updated on the last rising edge of the SCK signal, unless a command error occurred.

Memory is not updated if a Write command sequence does not consist of exactly 24 clock pulses.

**Note:** When writing to NV memory locations, verify the success of the operation by reading back the values and comparing them to the intended ones. This is also valid when using the CRC feature (for more details, see **Section 7.6, "SPI and Cyclic Redundancy Check (CRC)"**).

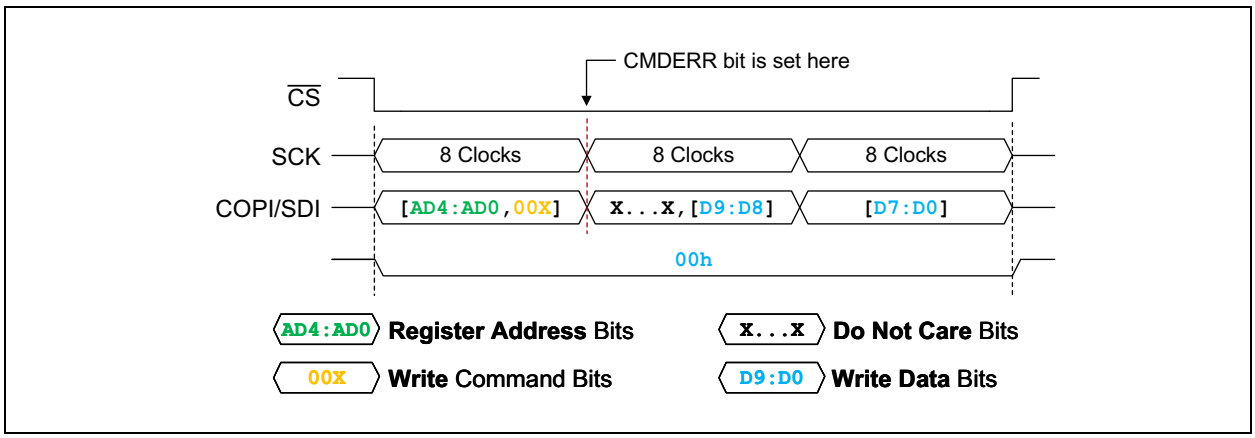



**FIGURE 7-7:** *SPI Write Command – SDI and SDO States.*

### 7.4.3 SPI READ COMMAND

A Read command to MCP41U83 retrieves the content of its memory (Volatile or NV). This is a 24-bit command and its format is shown in Figure 7-8.

Once the $\overline{CS}$ signal becomes active, the SDO line is driven to $V_{IL}$ (low).

On the SDI line, the Controller sends the initial 8 bits of the Read command that contain the memory address to access and the corresponding Command Code.

For the remaining 16 bits, any data received on the SDI pin is ignored while the SCK clock facilitates the transmission of the requested 10-bit register data through the SDO pin.

The SDO signal remains low until the 10-bit value [D9:D0] stored at the specified address [A4:A0] starts to be transmitted.

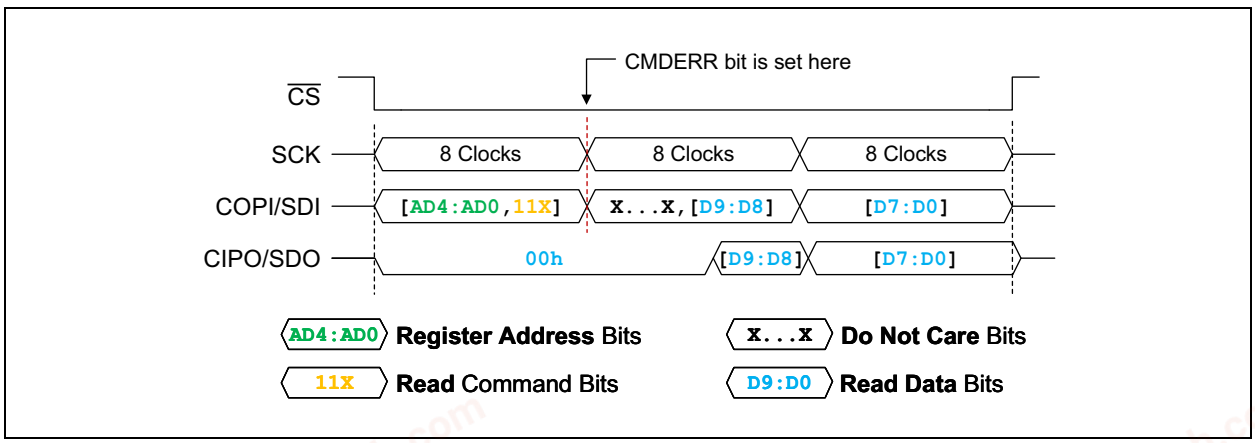



**FIGURE 7-8:** *SPI Read Command – SDI and SDO States.*

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### 7.4.4 SPI INCREMENT/DECREMENT WIPER POSITION COMMANDS

Increment/Decrement commands allow to quickly and easily modify the volatile potentiometer's wiper position by one unit, up or down, with minimal overhead.

The commands are designed to be faster than Random Address Writes, having a length of only 8 bits.

The update of the volatile wipers occurs after the last rising edge of the 8$^{th}$ SCK signal.

Executing either command on a register address that does not support them generates an error indicated by setting the CMDERR bit in the STATUS register.

#### 7.4.4.1 SPI Increment Wiper

Increment commands increase the wiper position value of MCP41U83 by one unit. This is a 8-bit command and its format is shown in Figure 7-8.

The wiper position increments up to a maximum of `3FFh` and no more. Further Increment commands are ignored, the CMDERR bit is set and the wiper position value remains at `3FFh`.

#### 7.4.4.2 SPI Decrement Wiper

Decrement commands decrease the wiper position value of MCP41U83 by one unit. This is a 8-bit command and its format is shown in Figure 7-8.

The wiper position decrements down to a minimum of `000h` and no more. Further Decrement commands are ignored, the CMDERR bit is set and the wiper position value remains at `000h`.

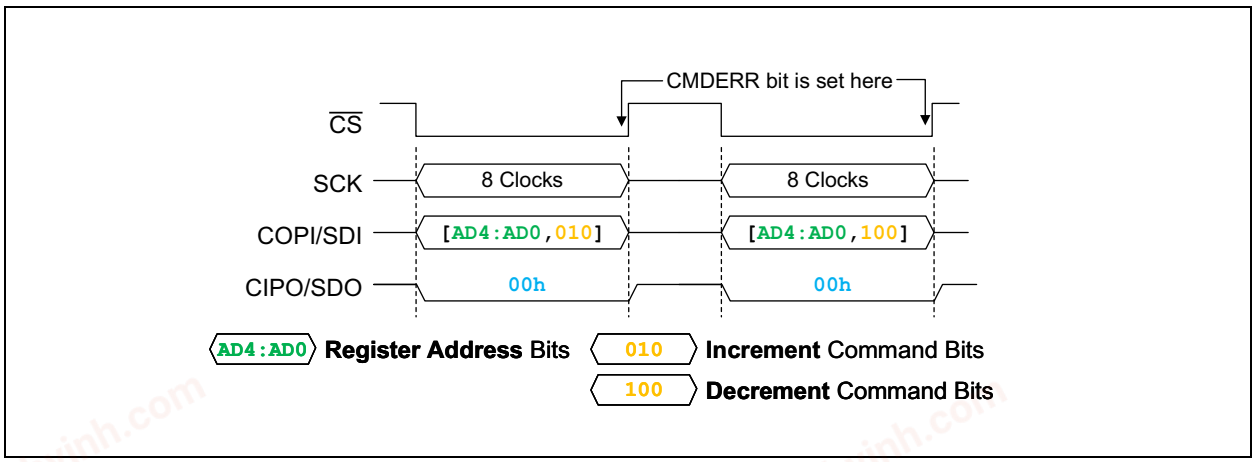



**FIGURE 7-9:** *SPI Increment/Decrement Wiper Commands – SDI and SDO States.*


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## 7.5 SPI Daisy-Chain Mode

### 7.5.1 GENERAL CONSIDERATIONS

When in SPI mode, multiple MCP41U83 devices can be connected in a Daisy-Chain bus configuration. This capability enables multiple devices to share the same SPI bus and thus, minimize the number of required $\overline{CS}$ lines to only a single line.

The Daisy-Chain bus configuration requires a different physical connection of SPI lines than the typical one. As shown in Figure 7-10, the COPI (Controller Output Peripheral Input) line is only connected to the SDI line of the first device, while the CIPO (Controller Input Peripheral Output) line is connected to the SDO line of the last device in the chain.

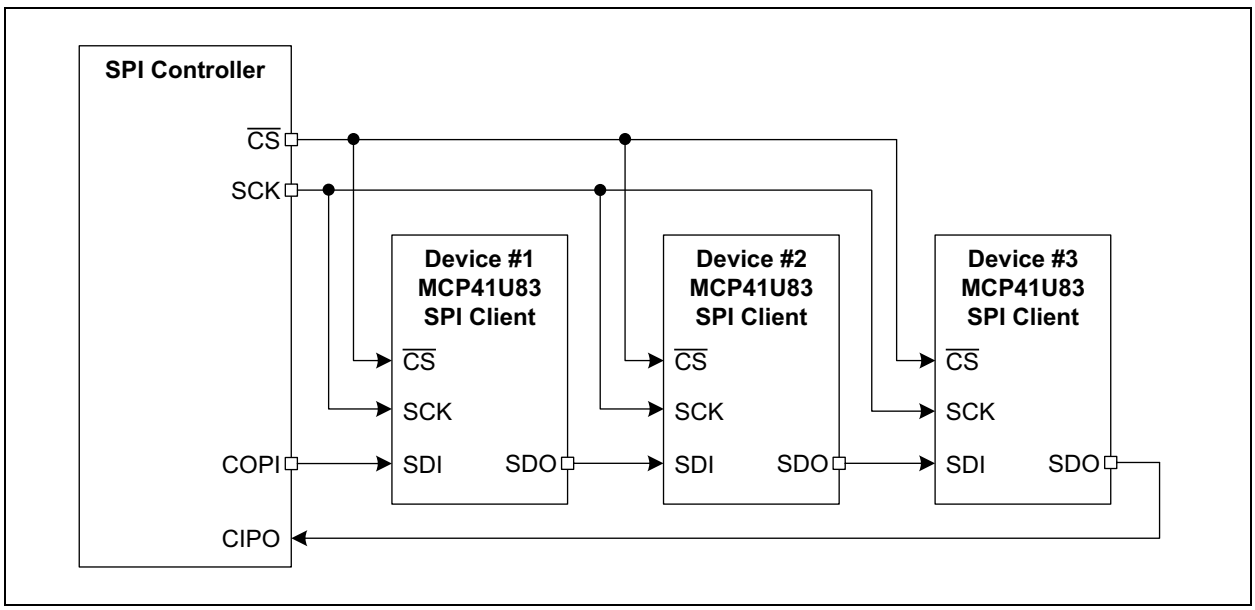



**FIGURE 7-10:** *SPI Daisy-Chain Bus Configuration – Connection Example for Three MCP41U83 Devices.*

Once a MCP41U83 device is configured to operate in Daisy-Chain mode, it uses the SDO line to transmit the data received on the SDI line, on every SCK cycle. This enables the next device in the daisy chain to receive data transmitted by the Controller and the Controller is able to receive data from all devices in the chain.

Once MCP41U83 is put in Daisy-Chain mode, the data transfer behavior differs from that of the standalone SPI mode:

1. There are two special Command bytes that are valid only in Daisy-Chain mode:
   - The first Command byte is `FFh`. It enables Daisy-Chain mode for every MCP41U83 device in the chain.
   - The second Command byte is `00h`. It is a no-operation (NOP) instruction and it ensures that the device executing the command keeps its internal state.
2. Input data decoding and command execution occur only when the $\overline{CS}$ pin goes high, except for Daisy-Chain Enable and NOP commands. These two operations are always executed on the rising edge of their 8$^{th}$ clock cycle. They are decoded without requiring the $\overline{CS}$ pin to go high.
3. The CMDERR bit in the STATUS register is set when an invalid command is detected, but its state changes only after the $\overline{CS}$ pin goes high. If the command error occurred only on certain devices in the chain, reissue Write commands only to devices with the CMDERR bit set, using the addressable Daisy-Chain Write feature.
4. Read, Write, Increment and Decrement cannot be mixed in the same command sequence. As such, the STATUS register can be checked only after other commands are executed.
5. A single command sequence must contain only 8-bit commands or 24-bit commands, not a mix of both types. In Daisy-Chain mode, a command sequence involves commands sent after the $\overline{CS}$ pin becomes active (high-to-low transition) and until the pin becomes inactive again (low-to-high transition).
6. Daisy-chain does not support CRC.

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### 7.5.2 DAISY-CHAIN ENTRY

When MCP41U83 devices are physically connected in Daisy-Chain mode, the Controller configures them to switch to the corresponding operation mode. It sends one FFh Command byte, followed by a number of 00h Command bytes on the COPI line, until it receives the first FFh byte on the CIPO line. The minimum number of 00h Command bytes sent by the Controller is equal to the number of devices connected in the daisy chain. This guarantees that all devices in the chain are now operating in Daisy-Chain mode.

For example, if there are three MCP41U83 devices to connect, the minimum sequence of Command bytes transmitted is: 00h 00h 00h FFh, where FFh is the first byte sent. Figure 7-11 shows the SPI signals when three devices are connected in a daisy chain.

**Note:** The maximum number of devices allowed in a daisy chain is 128.

After power-up, the first command received by devices connected in a daisy chain is the Daisy-Chain Enter command. If the devices do not receive this command, they are prevented from entering Daisy-Chain mode, unless an SPI interface reset procedure is used.

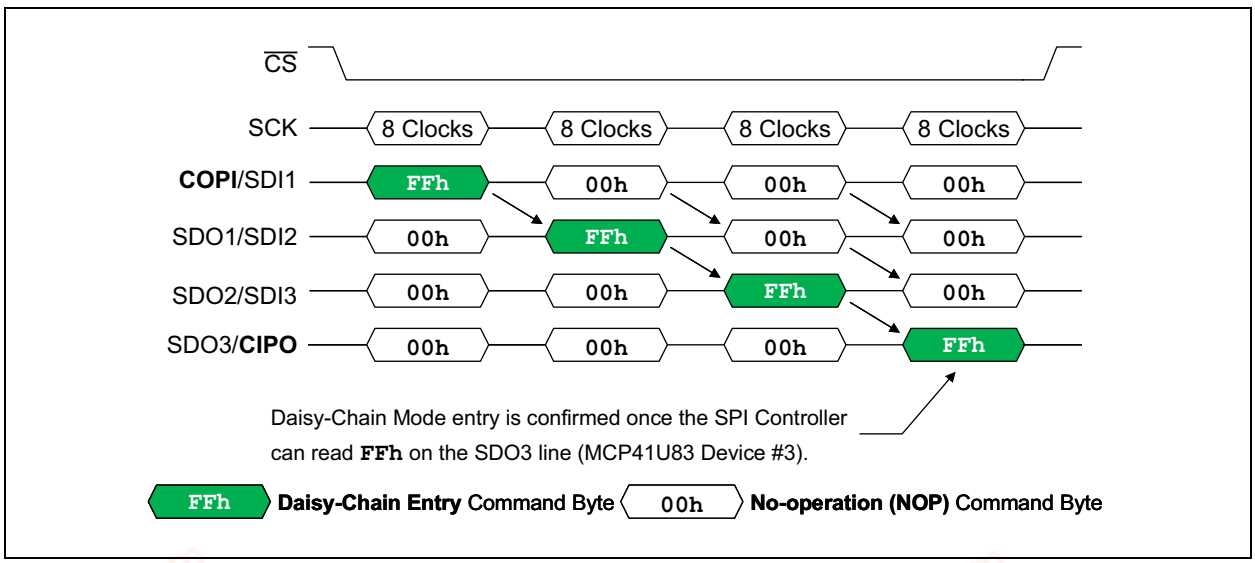



**FIGURE 7-11:** *SPI Daisy-Chain Entry Sequence – Example for Three MCP41U83 Devices.*

### 7.5.3 DAISY-CHAIN EXIT

Once set up in Daisy-Chain mode, a device breaking the chain is an abnormal event due to the physical connections involved. As such, there are no specific commands implemented for this purpose. However, when integrating MCP41U83 devices in an application, consider the following two scenarios in which a device exits Daisy-Chain mode:

- POR events make MCP41U83 exit Daisy-Chain mode. Thus, reinitialize every single device in a chain after each power-up.
- Resetting the SPI interface using the SCK pin reconfigures the devices in standalone mode. For details on SCK reset, see **Section 7.2.4, "Serial Clock (SCK)"**.

### 7.5.4 SOFTWARE RESET

Daisy-Chain mode support software resets. However, Microchip recommends to avoid using software resets due to the following potential implications.

**Note:** Software resets do not cause MCP41U83 devices to exit Daisy-Chain mode.

When triggering a software reset using the dedicated register, all the devices in the daisy chain must be reset simultaneously to ensure that the execution of all reset commands is within the same communication frame.

During initialization, MCP41U83 devices are unable to communicate and ignore commands received during this time. If not all the devices reset simultaneously, unexpected behavior appears and the daisy chain's integrity breaks.


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### 7.5.5 DAISY-CHAIN WRITE

When MCP41U83 is in Daisy-Chain mode, data enters the SDI pin and exits through the SDO pin. If all the devices in a daisy chain require updating, ensure to plan accordingly. In software, issue the correct Write command sequence that addresses every device in the chain. For example, if three devices are in Daisy-Chain mode, the command for device 3 must be first, followed by the command for device 2 and finally the command for device 1.

#### 7.5.5.1 8-Bit Increment/Decrement Commands

In the example in Figure 7-12, the software is writing a byte to every device in the daisy chain. Devices 1 and 2 receive a Decrement 8-bit command, while Device 3 receives an Increment 8-bit command.

**Note:** 8-bit commands can only be Increment or Decrement commands.

Once all 24 bits of data are clocked in, the $\overline{CS}$ pin must transition to $V_{IH}$ for the respective commands to execute on the corresponding devices in the chain.

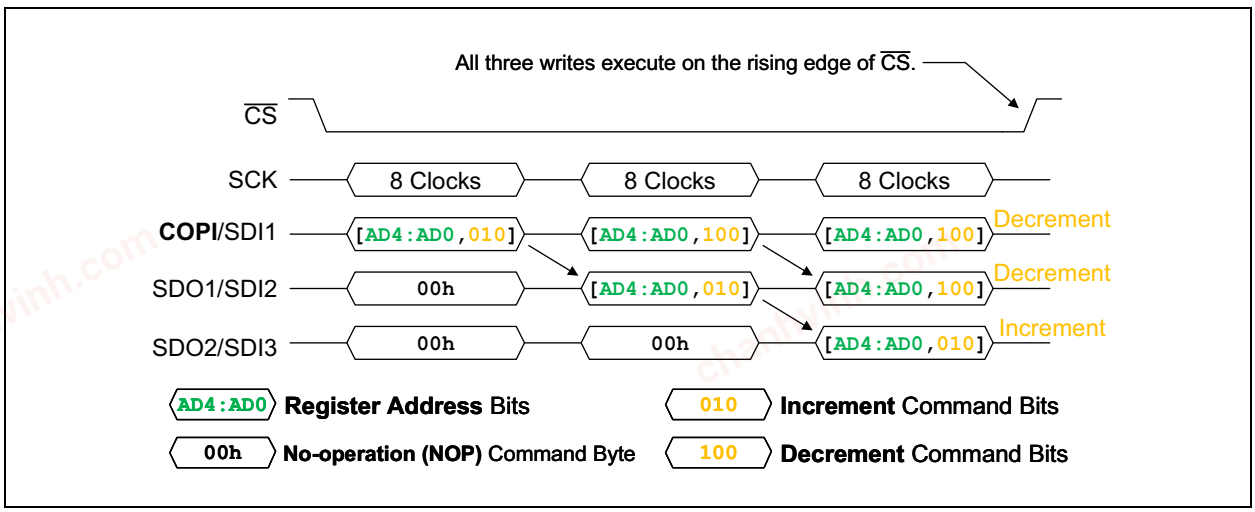



**FIGURE 7-12:** *SPI Daisy-Chain 8-Bit Increment/Decrement Commands Example.*

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### 7.5.5.2 24-Bit Write Commands

In the example in Figure 7-13, the software is writing to three devices in a daisy chain and using a 24-bit Write command.

The first byte for every device contains the register address and the command code. The next two bytes contain the 10-bit data to write. The data to write is `11h` for Device 1, `22h` for Device 2 and `33h` for Device 3.

The Controller first pulls the $\overline{CS}$ pin low, then sends the data in the following order:

1. `[A4:A0,00X]h`, `03h`, `33h` (Device 3)
2. `[A4:A0,00X]h`, `02h`, `22h` (Device 2)
3. `[A4:A0,00X]h`, `01h`, `11h` (Device 1).

Once all the 72 bits of data are clocked in, the $\overline{CS}$ pin must be set high to execute the commands and write the respective values to the wiper registers of the corresponding devices.

**Note:** Bits whose values are ignored by the device are marked with 'X'. They can be either `0` or `1`.

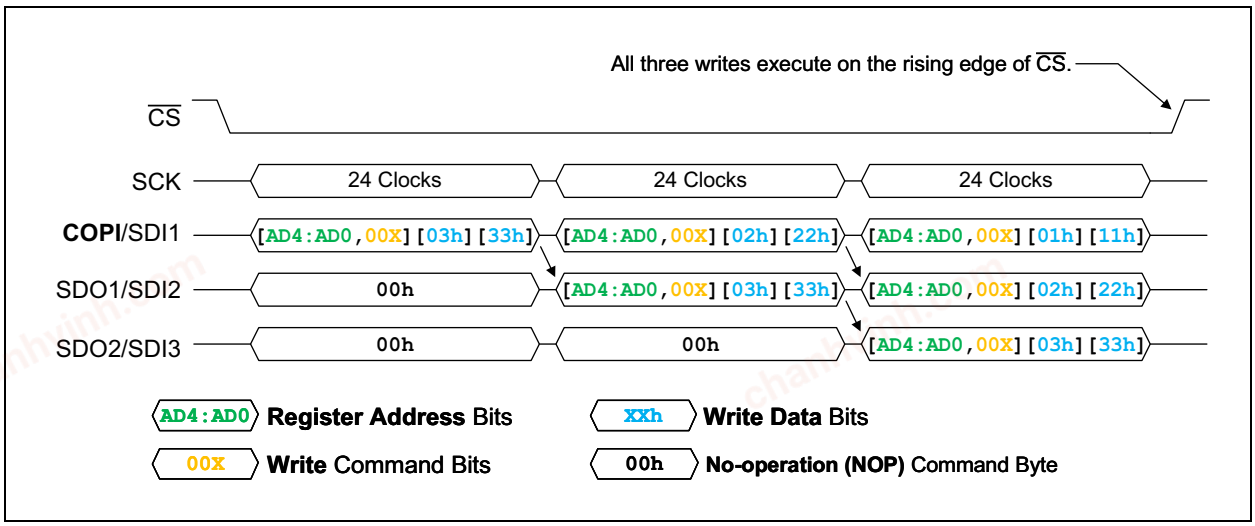



**FIGURE 7-13:** *SPI Daisy-Chain 24-Bit Write Commands Example.*


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### 7.5.6 ADDRESSABLE DAISY-CHAIN WRITES

Addressable Daisy-Chain Write commands help avoid a major drawback of chaining together multiple devices: modifying a register value on a single device also overwrites the rest of the registers with dummy or existing values. This is done to move the data along the daisy chain.

MCP41U83 solves this issue by employing a special Command byte with value `00h`. This is a no-operation (NOP) instruction and it ensures that devices executing the command keep their internal state.

Once in Daisy Chain mode, the Controller can send the NOP byte to a specific MCP41U83 device, ensuring it remains transparent or inactive to the input data. If a device receives a NOP byte, it decodes the command and then performs one of the following actions based on the state of the $\overline{CS}$ pin:

- If the $\overline{CS}$ pin remains low after receiving the NOP byte, MCP41U83 continues to pass the NOP byte through the SDO pin.
- If the $\overline{CS}$ pin goes high immediately after receiving the NOP byte, MCP41U83 becomes inactive and takes no further actions.

Besides Write commands, Increment and Decrement Wiper commands also benefit from this feature. The difference is the number of bytes transmitted by the Controller.

#### 7.5.6.1 8-Bit Addressable Increment/ Decrement Commands

The example in Figure 7-14 shows how to send an Increment command to Device 3 out of three daisy chained devices. The first step is to pull the $\overline{CS}$ pin low. Since Device 3 is last in the daisy chain, its command must be sent first. Next, Devices 1 and 2 receive NOP Command bytes to remain inactive when the $\overline{CS}$ pin goes high.

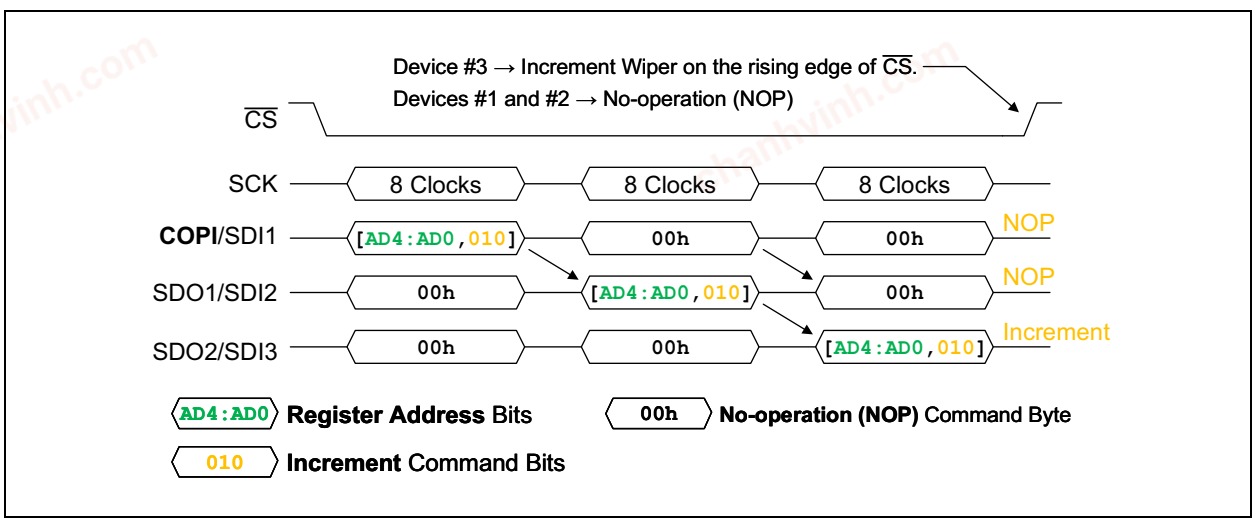



**FIGURE 7-14:** *SPI Daisy-Chain Addressable 8-Bit Increment/Decrement Commands Example.*

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### 7.5.6.2 24-Bit Addressable Write Commands

In the example in Figure 7-15, an updated wiper value must reach Device 2 out of three daisy chained devices. The Controller first pulls the $\overline{CS}$ pin low, then sends the data in the following order:

1. `00h`, `00h`, `00h` (Device 3)
2. `[A4:A0,00X]h`, `02h`, `22h` (Device 2)
3. `00h`, `00h`, `00h` (Device 1).

When the $\overline{CS}$ pin goes high, only Device 2 updates one of its wiper values. The NOP byte is decoded 'on the fly', therefore three `00h` bytes must be sent to every device to ensure data alignment is correct.

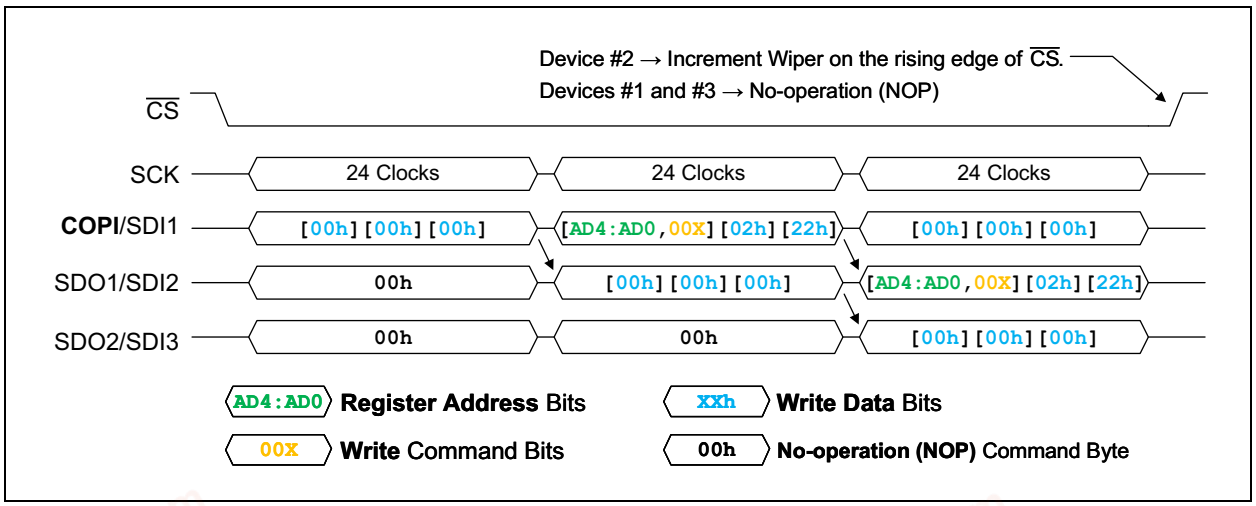



**FIGURE 7-15:** *SPI Daisy-Chain Addressable 24-Bit Write Commands Example.*


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### 7.5.7 DAISY-CHAIN READ COMMANDS

Read commands are different between Daisy-Chain and standalone mode due to the need to extract the read data from all devices in the daisy chain, while also sending commands. As such, the Read command procedure has two distinct stages:

1. In the first stage, the Controller sends either a Read or NOP command, resulting in one byte per device.

   **Note:** If another command is present in this frame, it results in unpredictable behavior.

   The frame of the first stage begins with the $\overline{CS}$ pin transitioning from $V_{IH}$ to $V_{IL}$ and ends with it transitioning from $V_{IL}$ to $V_{IH}$. No other data must be sent until the next frame, in which the data to read is transmitted on the bus. The $\overline{CS}$ pin must stay high until the Controller initiates the data read frame.

2. The second stage consists of a frame in which only the serial clock is required, while the COPI data sent by the Controller is ignored.

   For every 16 clock cycles, corresponding to two bytes, each MCP41U83 device in the daisy chain transmits on its SDO line the data read from the register address sent in the first stage frame.

   This stage ends whenever the $\overline{CS}$ pin becomes high again, regardless if all devices in the daisy chain managed to output their data or not. This event resets the SPI interface to its default state, basically stopping the read operation.

   **Note:** If a MCP41U83 device receives a NOP byte in the first stage, it outputs a single NOP byte. Ensure proper consideration to properly identify this value in the byte sequence read by the Controller.

The example in Figure 7-16 illustrates the command sequence when reading data from three daisy chained devices.

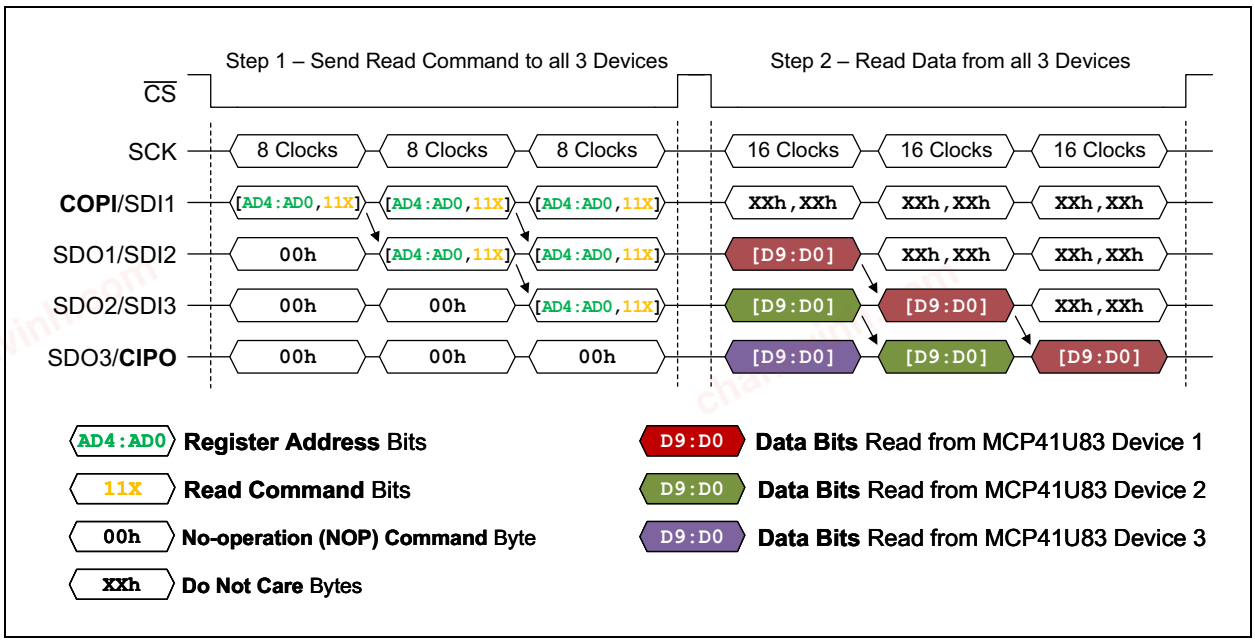



**FIGURE 7-16:** *SPI Daisy-Chain Read Command Example.*

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## 7.6 SPI and Cyclic Redundancy Check (CRC)

A general description of the CRC module is presented in **Section 4.4, "Cyclic Redundancy Check (CRC) Module"**. The following section describes the CRC module's SPI specific functionality.

### 7.6.1 WRITE, INCREMENT AND DECREMENT COMMANDS WITH CRC ENABLED

For Write, Increment or Decrement commands, the Controller sends the CRC byte after the usual data is transmitted. The CRC byte is the last byte during a communication frame. Figure 7-17 illustrates the command sequence for a Write command with CRC enabled, while Figure 7-18 illustrates the command sequence for an Increment or Decrement command.

Once MCP41U83 receives the transmitted data from the Controller, the CRC hardware module constantly checks incoming data. Once the $\overline{CS}$ pin goes high, if the CRC byte sent by the Controller mismatched the internally computed CRC byte, MCP41U83 sets the CRCERR bit in the STATUS register.

If CRCERR or CMDERR bits are set, the command is aborted. As such, ensure to read the STATUS register after every Write, Increment or Decrement command.

The actual execution timing of Write, Increment or Decrement commands is different with CRC enabled. It is executed only on the 8th rising edge of the CRC byte transmission, as long as there is no command or CRC error. If CRC is disabled, Write, Increment or Decrement commands are executed on the 8th rising edge of the command byte transmission.

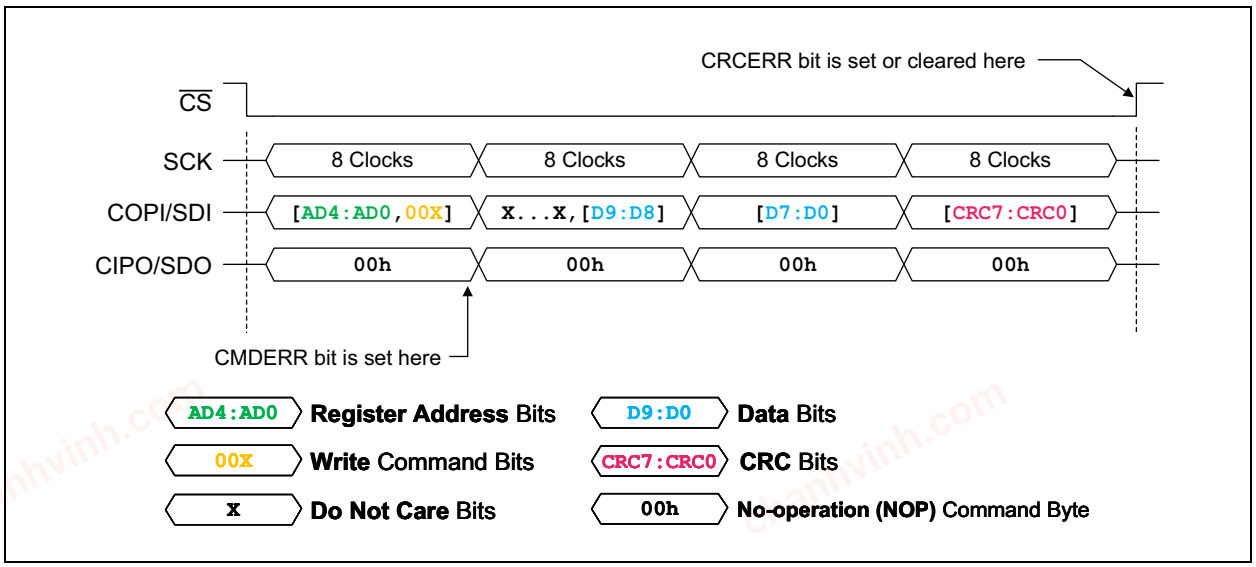



**FIGURE 7-17:** *SPI Write Command Sequence with CRC Enabled.*

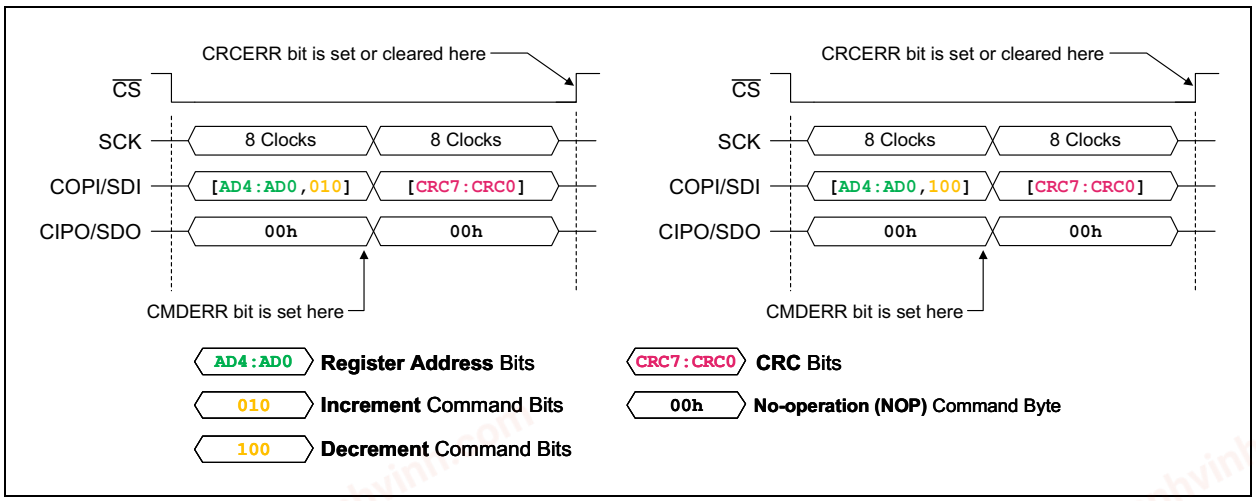



**FIGURE 7-18:** *SPI Increment/Decrement Command Sequence with CRC Enabled.*


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### 7.6.2 READ COMMAND WITH CRC ENABLED

Read commands with CRC enabled increase the total number of bytes in a frame by 1, as shown in Figure 7-19.

The first byte is the Command byte and contains the register address and command code. The next byte sent by the Controller is the CRC checksum, computed for the Command byte.

Once the CRC checksum is received, MCP41U83 sets the CRCERR bit in the STATUS register based on the received CRC byte by comparing it with the internally computed CRC value.

Next, the Controller sends two dummy bytes to read back data from the device. MCP41U83 sends the register value in the second and third bytes. The fourth and last byte is the CRC checksum computed for the data bytes.

With CRC enabled, if there is a CRC or command error while executing the Read command, MCP41U83 sets the CRCERR or CMDERR bits in the STATUS register. To ensure that there were no CRC or command errors, read the STATUS register.

Reading the STATUS register with CRC enabled does not generate CRC errors, since this operation is for reading and clearing the existing CRC error status.

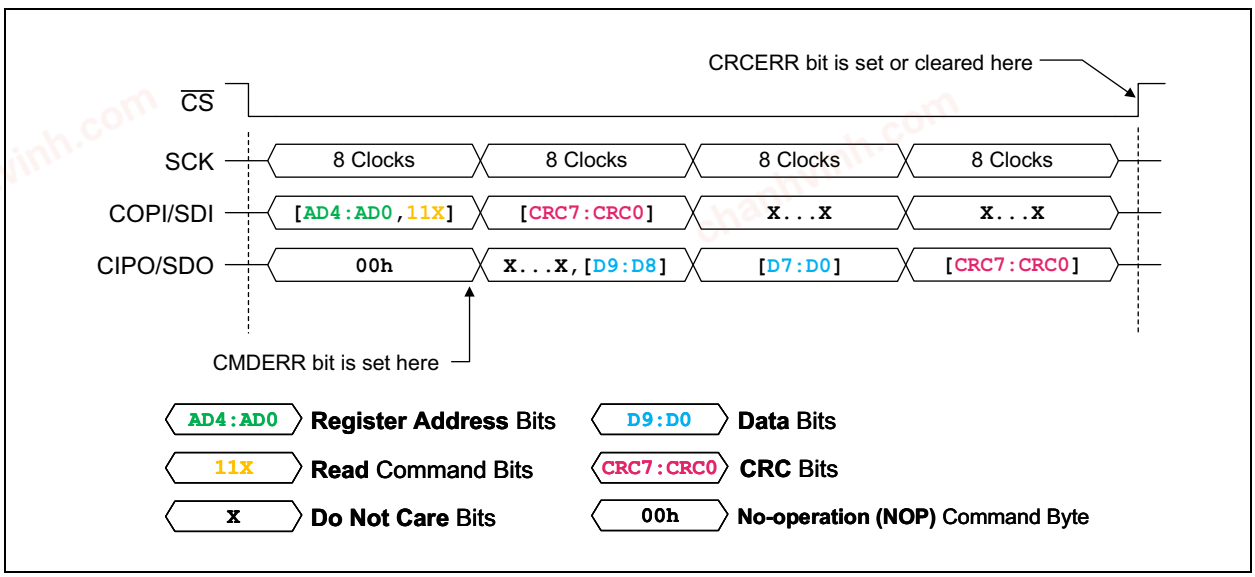



**FIGURE 7-19:** *SPI Read Command Sequence with CRC Enabled.*

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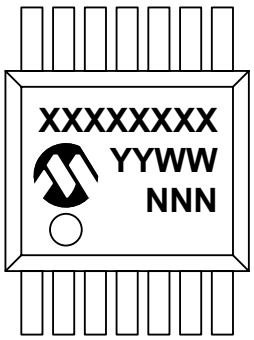
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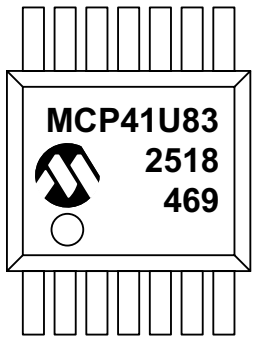
## 8.0 PACKAGE INFORMATION

### 8.1 Package Marking Information

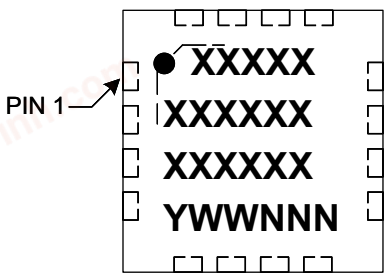
**14-Lead TSSOP, 4.4 mm Body**



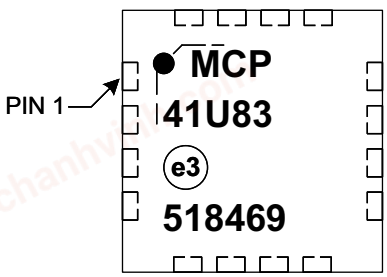

**Example:**




**16-Lead VQFN, 4x4 mm Body**




**Example:**




| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.


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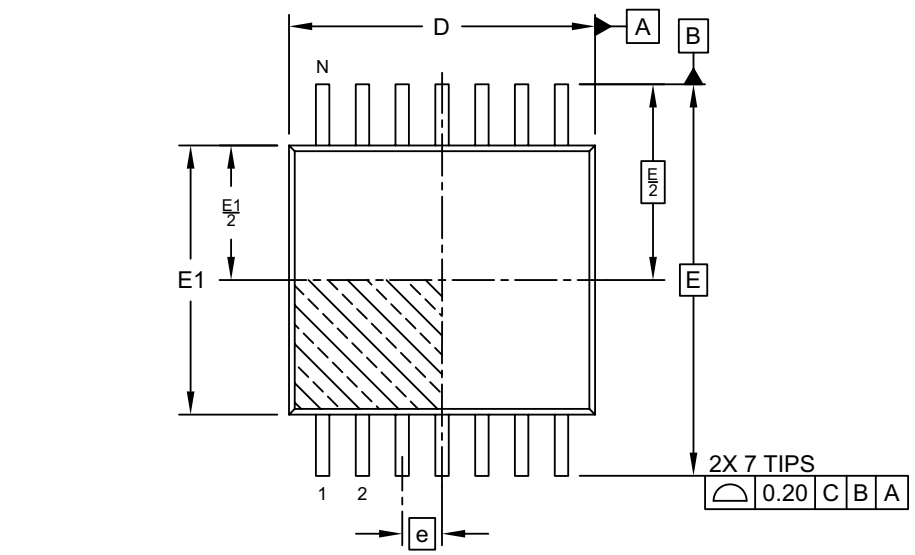
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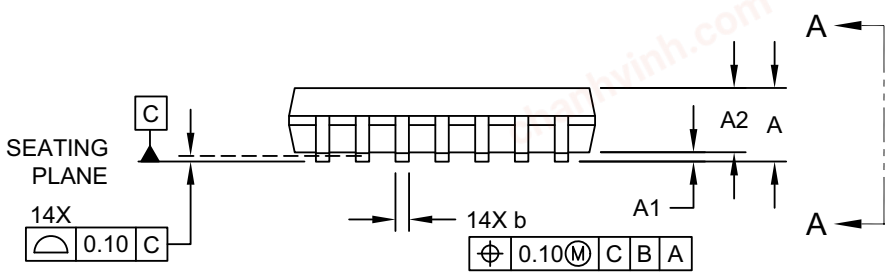
## 8.2 Package Drawings

### 14-Lead Plastic Thin Shrink Small Outline Package [ST] - 4.4 mm Body [TSSOP]

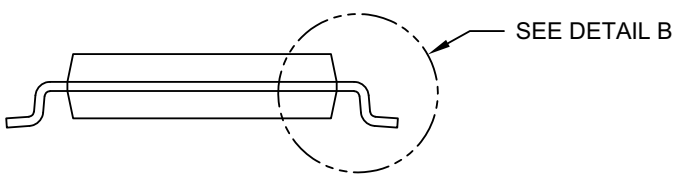
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW




SIDE VIEW




VIEW A–A

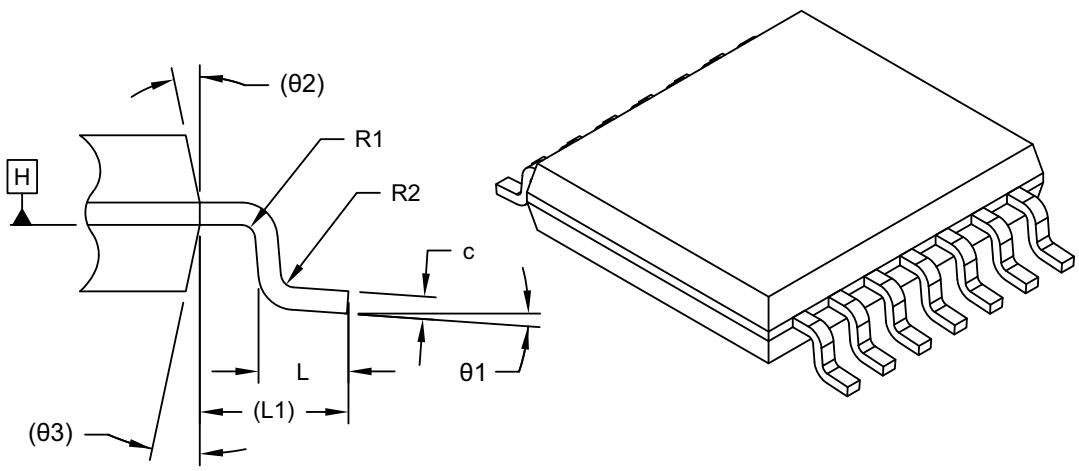
Microchip Technology Drawing C04-087-ST Rev F Sheet 1 of 2

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## 14-Lead Plastic Thin Shrink Small Outline Package [ST] - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




DETAIL B

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 14 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | – | – | 1.20 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Molded Package Thickness | A2 | 0.80 | 1.00 | 1.05 |
| Overall Length | D | 4.90 | 5.00 | 5.10 |
| Overall Width | E | | 6.40 BSC | |
| Molded Package Width | E1 | 4.30 | 4.40 | 4.50 |
| Terminal Width | b | 0.19 | – | 0.30 |
| Terminal Thickness | c | 0.09 | – | 0.20 |
| Terminal Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Lead Bend Radius | R1 | 0.09 | – | – |
| Lead Bend Radius | R2 | 0.09 | – | – |
| Foot Angle | θ1 | 0° | – | 8° |
| Mold Draft Angle | θ2 | – | 12° REF | – |
| Mold Draft Angle | θ3 | – | 12° REF | – |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087-ST Rev F Sheet 2 of 2

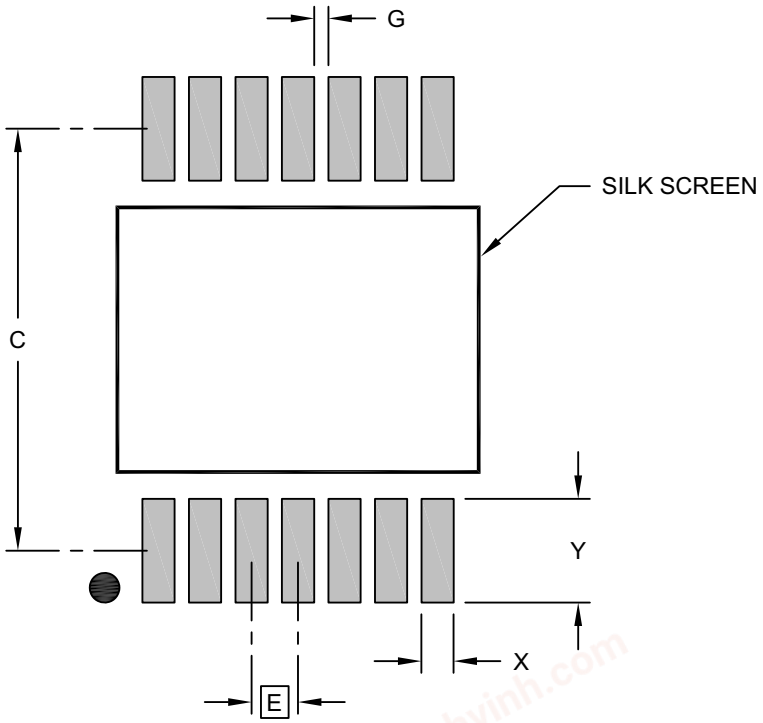

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## 14-Lead Plastic Thin Shrink Small Outline Package [ST] – 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Contact Pad Spacing | C | | 5.90 | |
| Contact Pad Width (X14) | X | | | 0.45 |
| Contact Pad Length (X14) | Y | | | 1.45 |
| Contact Pad to Contact Pad (X12) | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2087-ST Rev F

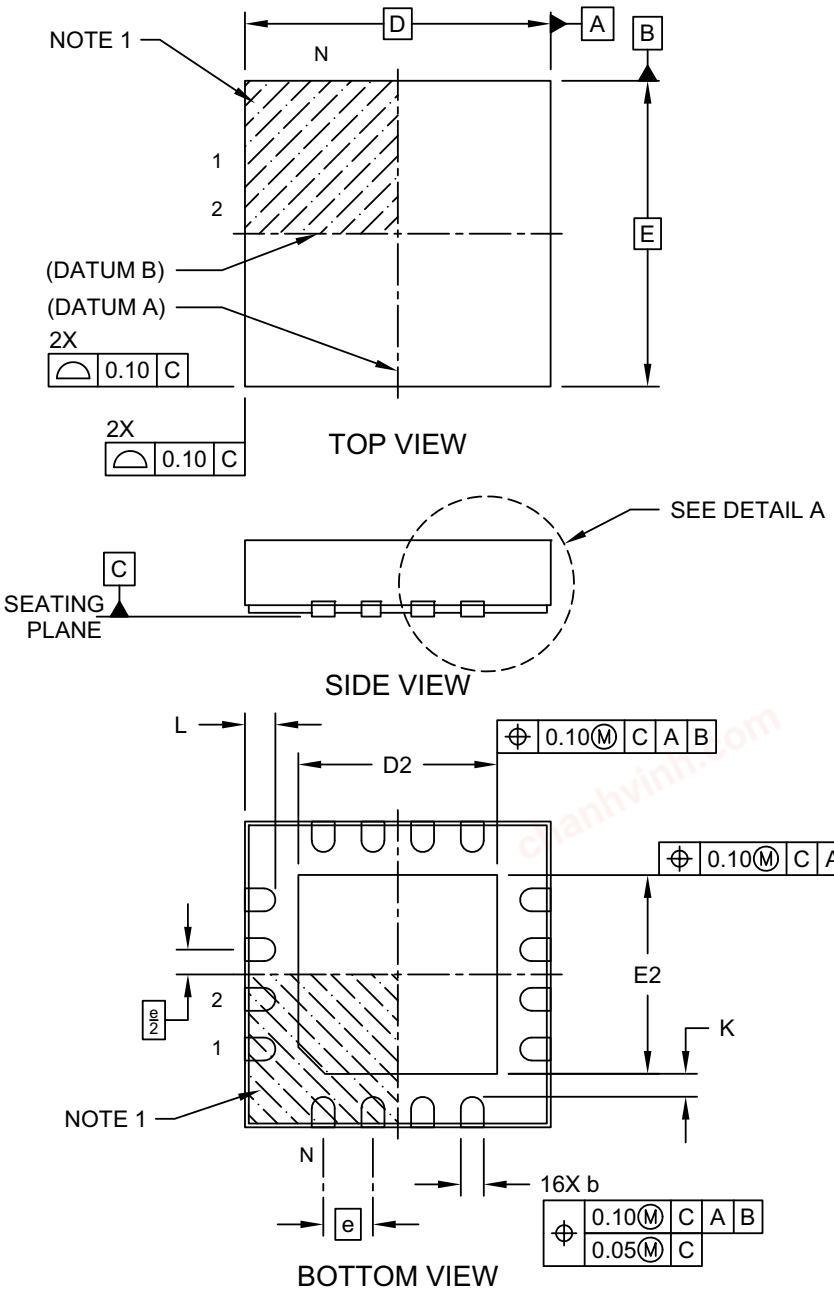
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**16-Lead Plastic Quad Flat, No Lead Package (7N) - 4x4x1.0 mm Body [VQFN]**
**Wettable Flanks (Stepped), 0.40 mm Terminal Length**

| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




Microchip Technology Drawing C04-403-7N Rev. D Sheet 1 of 2

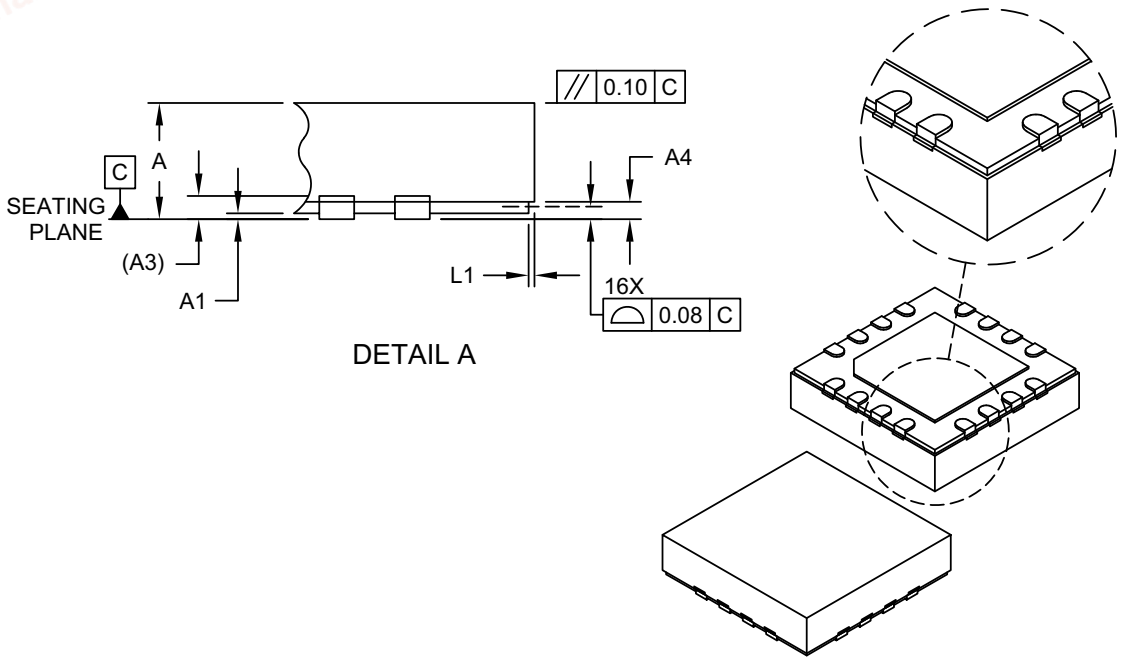

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## 16-Lead Plastic Quad Flat, No Lead Package (7N) - 4x4x1.0 mm Body [VQFN] Wettable Flanks (Stepped), 0.40 mm Terminal Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 16 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.20 REF | |
| Step Height | A4 | 0.10 | – | 0.19 |
| Overall Width | E | | 4.00 BSC | |
| Exposed Pad Width | E2 | 2.50 | 2.60 | 2.70 |
| Overall Length | D | | 4.00 BSC | |
| Exposed Pad Length | D2 | 2.50 | 2.60 | 2.70 |
| Terminal Width | b | 0.25 | 0.30 | 0.35 |
| Terminal Length | L | 0.30 | 0.40 | 0.50 |
| Step Length | L1 | 0.035 | 0.060 | 0.085 |
| Terminal-to-Exposed Pad | K | 0.30 | - | - |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-403-7N Rev. D Sheet 2 of 2

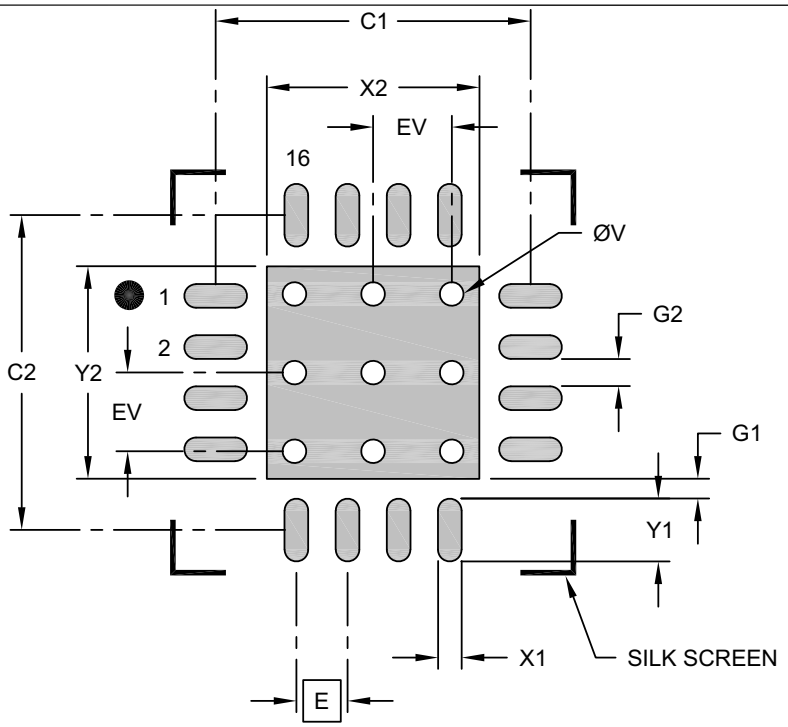
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### 16-Lead Plastic Quad Flat, No Lead Package (7N) - 4x4x1.0 mm Body [VQFN] Wettable Flanks (Stepped), 0.40 mm Terminal Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.65 BSC | |
| Optional Center Pad Width | X2 | | | 2.70 |
| Optional Center Pad Length | Y2 | | | 2.70 |
| Contact Pad Spacing | C1 | | 4.00 | |
| Contact Pad Spacing | C2 | | 4.00 | |
| Contact Pad Width (X16) | X1 | | | 0.30 |
| Contact Pad Length (X16) | Y1 | | | 0.80 |
| Contact Pad to Center Pad (X16) | G1 | 0.20 | | |
| Contact Pad to Contact Pad (X12) | G2 | 0.35 | | |
| Thermal Via Diameter | V | | 0.30 | |
| Thermal Via Pitch | EV | | 1.00 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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# APPENDIX A: REVISION HISTORY

## Revision B (October 2025)

Following are the changes made in this revision:

- Added AEC-Q100 Grade-1 qualification.
- Added **Section "Product Identification System (Automotive)"**.
- Updated Figure 7-10 and Figure 7-15.
- Updated **Section 8.1, "Package Marking Information"**.

## Revision A (March 2025)

- Initial release of this document.

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# APPENDIX B: TERMINOLOGY

Digital potentiometers behave differently when they are used in potentiometer (resistive divider) configuration versus rheostat (variable resistor) configuration.

**Note:** Throughout this appendix, the following notation is used:

- *codeN* refers to a wiper register value.

## B.1 Generic Parameters

This section presents the parameters common for both potentiometer and rheostat modes.

### B.1.1 RESOLUTION (N)

The Resolution (N) is the number of wiper output states that divide the full scale range. For a 10-bit digital potentiometer, the resolution is equal to $2^{10}$ and means that the digital potentiometer wiper code can be set to any number from 0 to $2^{10} – 1$.

### B.1.2 LEAST SIGNIFICANT BIT (LSB)

This is the voltage difference between two successive wiper codes. A given output voltage range is divided by the resolution of MCP41U83. The range is either full scale to zero scale (measured) or from the voltage of the A pin to the voltage on the B pin (ideal).

The LSb is calculated using Equation B-1.

**EQUATION B-1:**

$$V_{LSb}|_{measured} = \frac{V_{P0W}|_{FS} - V_{P0W}|_{ZS}}{2^N - 1}$$

$$V_{LSb}|_{ideal} = \frac{V_{P0A} - V_{P0B}}{2^N - 1}$$

Where:

| | | |
|---|---|---|
| $V_{LSb}\|_{measured}$ | = | Measured LSb Voltage Range (V) |
| $V_{P0W}\|_{FS}$ | = | Voltage Measured on the Wiper Pin at Full Scale Wiper Code (V) |
| $V_{P0W}\|_{ZS}$ | = | Voltage Measured on the Wiper Pin at Zero Scale Wiper Code (V) |
| $N$ | = | MCP41U83 Resolution (10 bits) |
| $V_{LSB}\|_{ideal}$ | = | Ideal LSb Voltage Range (V) |
| $V_{P0A}$ | = | Voltage Measured on the A pin (V) |

## B.2 Potentiometer Mode Parameters

This section presents the parameters distinct to only potentiometer mode.

### B.2.1 END-TO-END RESISTANCE ($R_{AB}$)

The End-to-End Resistance ($R_{AB}$) is the resistance between the P0A and P0B pins. $R_{AB}$ is composed of the wiper resistance ($R_W$) and the resistance of each analog switch of every individual P0A and P0B pin.

$R_{AB}$ is calculated using Equation B-2.

**EQUATION B-2:**

$$R_{AB} = \frac{V_{P0A} - V_{P0B}}{I_{AB}}$$

Where:

| | | |
|---|---|---|
| $R_{AB}$ | = | End-to-End Resistance (kΩ) |
| $V_{P0A}$ | = | P0A Voltage (V) |
| $V_{P0B}$ | = | P0B Voltage (V) |
| $I_{AB}$ | = | Resistor Ladder Current (mA) |

### B.2.2 POTENTIOMETER INTEGRAL NONLINEARITY (P-INL)

The Potentiometer Integral Nonlinearity (P-INL) error is the maximum deviation of an actual transfer function from an ideal transfer function (straight line) passing through the defined endpoints of the transfer function.

P-INL is calculated using the zero scale and full scale wiper code endpoints, as shown in Equation B-3. P-INL is expressed in LSb.

**EQUATION B-3:**

$$P-INL = \frac{V_{P0W}|_{codeN} - V_{P0W}|_{ZS}}{V_{LSb}|_{measured}} - codeN$$

Where:

| | | |
|---|---|---|
| $P\text{-}INL$ | = | Potentiometer Integral Nonlinearity (LSb) |
| $V_{P0W}\|_{codeN}$ | = | Voltage Measured on the Wiper Pin for a Given Wiper Code (V) |
| $V_{P0W}\|_{ZS}$ | = | Voltage Measured on the Wiper Pin at Zero Scale Wiper Code (V) |
| $V_{LSb}\|_{measured}$ | = | Measured LSb Voltage Range (V) |
| $codeN$ | = | Wiper Register Value |

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### B.2.3 POTENTIOMETER DIFFERENTIAL NONLINEARITY (P-DNL)

The Potentiometer Differential Nonlinearity (P-DNL) error is the measure of the step size between codes in the actual transfer function.

The ideal step size between codes is 1 LSb. A P-DNL error of zero implies that every code is exactly 1 LSb in size. If the P-DNL error is less than 1 LSb, MCP41U83 guarantees monotonic output and no missing codes. The P-DNL error is the measure of variations in code sizes from the ideal code size using the zero scale and full scale wiper code endpoints.

P-DNL is expressed in LSb and is calculated as shown in Equation B-4.

**EQUATION B-4:**

$$P-DNL = \frac{V_{P0W}|_{codeN+1} - V_{P0W}|_{codeN}}{V_{LSb}|_{measured}} - 1$$

Where:

| | | |
|---|---|---|
| $P\text{-}DNL$ | = | Potentiometer Differential Nonlinearity (LSb) |
| $V_{P0W}\|_{codeN+1}$ | = | Voltage Measured on the Wiper Pin for a Given Wiper Code + 1 (V) |
| $V_{P0W}\|_{codeN}$ | = | Voltage Measured on the Wiper Pin for a Given Wiper Code (V) |
| $V_{LSb}\|_{measured}$ | = | Measured LSb Voltage Range (V) |
| $codeN$ | = | Wiper Register Value |

### B.2.4 FULL SCALE ERROR (FSE)

The Full Scale Error (FSE) is the voltage error on the P0W pin relative to the expected (theoretical) voltage on the P0A pin, calculated for the maximum (full scale) wiper code ($2^N - 1$). FSE depends on the resistive load on the P0W pin and its connection, either to VSS or VDD. FSE increases for loads to VSS that are greater than specified.

FSE is determined by the theoretical voltage step size, resulting in an error measured in LSb, as shown in Equation B-5.

**EQUATION B-5:**

$$FSE = \frac{V_{P0W}|_{FS} - V_{P0A}|_{measured}}{V_{LSb}|_{ideal}}$$

Where:

| | | |
|---|---|---|
| $FSE$ | = | Full Scale Error (LSb) |
| $V_{P0W}\|_{FS}$ | = | Voltage Measured on the Wiper Pin at Full Scale Wiper Code (V) |
| $V_{P0A}\|_{measured}$ | = | Measured P0A Voltage (V) |
| $V_{LSb}\|_{ideal}$ | = | Ideal LSb Voltage Range (V) |

### B.2.5 ZERO SCALE ERROR (ZSE)

The Zero Scale Error (ZSE) is the difference between the measured voltage on the P0W pin with the minimum (zero scale) wiper code (0) and the measured voltage on the P0B pin. ZSE depends on the resistive load on the P0W pin and its connection, either to VSS or VDD. FSE increases for loads to VDD that are greater than specified.

FSE is determined by the theoretical voltage step size, resulting in an error measured in LSb, as shown in Equation B-6.

**EQUATION B-6:**

$$ZSE = \frac{V_{P0W}|_{ZS} - V_{P0B}|_{measured}}{V_{LSb}|_{ideal}}$$

Where:

| | | |
|---|---|---|
| $ZSE$ | = | Zero Scale Error (LSb) |
| $V_{P0W}\|_{ZS}$ | = | Voltage Measured on the Wiper Pin at Zero Scale Wiper Code (V) |
| $V_{P0B}\|_{measured}$ | = | Measured P0B Voltage (V) |
| $V_{LSb}\|_{ideal}$ | = | Ideal LSb Voltage Range (V) |

### B.2.6 POTENTIOMETER NOMINAL RESISTANCE TEMPERATURE COEFFICIENT (P-$R_{TC}$)

The Potentiometer Nominal Resistance Temperature Coefficient (P-$R_{TC}$) quantifies the error in the End-to-End resistance ($R_{AB}$) caused by temperature drift. This is typically the critical error when using MCP41U83 in resistive divider configuration.

P-$R_{TC}$ is calculated using Equation B-7.

**EQUATION B-7:**

$$P-R_{TC} = \frac{\frac{R_{AB}|_{max} - R_{AB}|_{min}}{R_{AB}|_{average}}}{T_{OP}|_{max} - T_{OP}|_{min}} \times 10^6$$

Where:

| | | |
|---|---|---|
| $P\text{-}R_{TC}$ | = | Potentiometer Nominal Resistance Temperature Coefficient (ppm/°C) |
| $R_{AB}\|_{max}$ | = | Maximum End-to-End Resistance Value (kΩ) |
| $R_{AB}\|_{min}$ | = | Minimum End-to-End Resistance Value (kΩ) |
| $R_{AB}\|_{average}$ | = | Typical End-to-End Resistance Value (kΩ) |
| $T_{min}$ | = | Minimum Operating Temperature (°C) |
| $T_{max}$ | = | Maximum Operating Temperature (°C) |

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### B.2.7 RATIOMETRIC TEMPERATURE COEFFICIENT ($V_{TC}$)

The Ratiometric Temperature Coefficient ($V_{TC}$) quantifies the error in the $R_{AW}/R_{WB}$ ratio caused by temperature drift. This is typically the critical error when using MCP41U83 in voltage divider configuration.

$V_{TC}$ is calculated using Equation B-8.

**EQUATION B-8:**

$$V_{TC} = \frac{\frac{V_{P0W}|_{max} - V_{P0W}|_{min}}{V_{P0W}|_{average}}}{T_{OP}|_{max} - T_{OP}|_{min}} \times 10^6$$

Where:

| | | |
|---|---|---|
| $V_{TC}$ | = | Ratiometric Temperature Coefficient (ppm/°C) |
| $V_{P0W}\|_{max}$ | = | Maximum P0W Voltage (V) |
| $V_{P0W}\|_{min}$ | = | Minimum P0W Voltage (V) |
| $V_{P0W}\|_{average}$ | = | Typical P0W Voltage (V) |
| $T_{min}$ | = | Minimum Operating Temperature (°C) |
| $T_{max}$ | = | Maximum Operating Temperature (°C) |

### B.2.8 POTENTIOMETER CHANNEL-TO-CHANNEL MATCHING (P-$RM_{AB}$)

The Potentiometer Channel-to-Channel Matching (P-$RM_{AB}$) quantifies the End-to-End resistance ($R_{AB}$) error between channels 0 and 1.

P-$RM_{AB}$ is calculated using Equation B-9.

**EQUATION B-9:**

$$P-RM_{AB} = \frac{R_{AB0} - R_{AB1}}{\frac{1}{2} \cdot (R_{AB0} + R_{AB1})} \times 100$$

Where:

| | | |
|---|---|---|
| $P\text{-}RM_{AB}$ | = | Potentiometer Channel-to-Channel Matching (%) |
| $R_{AB0}$ | = | Channel 0 End-to-End Resistance (kΩ) |
| $R_{AB1}$ | = | Channel 1 End-to-End Resistance (kΩ) |

### B.2.9 POWER SUPPLY SENSITIVITY (PSS)

The Power Supply Sensitivity (PSS) indicates how the voltage output of MCP41U83 ($V_{P0W}$) is affected by changes in the supply voltage. PSS is the ratio of the change in $V_{P0W}$ to changes in $V_{DD}$ for the midscale output of the digital potentiometer. $V_{P0W}$ is measured while $V_{DD}$ varies from 5.5V to 2.7V as a step. PSS in expressed as the percentage change in $V_{P0W}$ with respect to the percentage change in $V_{DD}$.

PSS is calculated using Equation B-10.

**EQUATION B-10:**

$$PSS = \frac{\frac{V_{P0W}|_{5.5V} - V_{P0W}|_{2.7V}}{V_{P0W}|_{5.5V}}}{\frac{5.5V - 2.7V}{5.5V}}$$

Where:

| | | |
|---|---|---|
| $PSS$ | = | Power Supply Sensitivity (%/%) |
| $V_{P0W}\|_{5.5V}$ | = | P0W Voltage at $V_{DD}$ = 5.5V (V) |
| $V_{P0W}\|_{2.7V}$ | = | P0W Voltage at $V_{DD}$ = 2.7V (V) |

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## B.3 Rheostat Mode Parameters

This section presents the parameters distinct to only rheostat mode.

### B.3.1 WIPER-TO-END RESISTANCE ($R_{WB}$)

The Wiper-to-End Resistance ($R_{WB}$) is the resistance between the P0W and P0B pins. This resistance is composed of the wiper resistance ($R_W$) and the analog switch of every P0B pin at full scale.

$R_{WB}$ is calculated using Equation B-11.

**EQUATION B-11:**

$$R_{WB} = \frac{V_{P0W}|_{FS} - V_{P0B}}{I_{WB}}$$

Where:

| | | |
|---|---|---|
| $R_{WB}$ | = | Wiper-to-End Resistance (kΩ) |
| $V_{P0W}\|_{FS}$ | = | Voltage Measured on the Wiper Pin at Full Scale Wiper Code (V) |
| $V_{P0B}$ | = | P0B Voltage (V) |
| $I_{WB}$ | = | Wiper-to-End Current (mA) |

### B.3.2 WIPER RESISTANCE ($R_W$)

The Wiper Resistance ($R_W$) is the series resistance of the analog switch that connects the selected resistor ladder node to the wiper terminal common signal. The value written in the Volatile Wiper register selects what analog switch to close, connecting terminal W to the selected node of the resistor ladder.

$R_W$ depends on the following parameters:

- Voltages on the analog switch source, gate and drain nodes.
- MCP41U83's wiper code, temperature and current through the switches on terminals W and B.
- As the voltage of MCP41U83 decreases, $R_W$ increases.

$R_W$ is determined by forcing a current through terminals W and B ($I_W$) and measuring the zero scale voltage on terminal W. $R_{WB}$ is calculated using Equation B-12.

**EQUATION B-12:**

$$R_W = \frac{1}{2} \times \frac{V_{P0W}|_{ZS} - V_{P0B}}{I_W}$$

Where:

| | | |
|---|---|---|
| $R_W$ | = | Wiper Resistance (kΩ) |
| $V_{P0W}\|_{ZS}$ | = | Voltage Measured on the Wiper Pin at Zero Scale Wiper Code (V) |
| $V_{P0B}$ | = | P0B Voltage (V) |
| $I_W$ | = | Wiper Current (mA) |

### B.3.3 RHEOSTAT INTEGRAL NONLINEARITY (R-INL)

The Rheostat Integral Nonlinearity (R-INL) error is the maximum deviation of an actual transfer function from an ideal transfer function (straight line) passing through the defined endpoints of the transfer function.

R-INL is calculated using the zero scale and full scale wiper code endpoints, as shown in Equation B-13. R-INL is expressed in LSb.

**EQUATION B-13:**

$$R - INL = \frac{V_{P0W}|_{codeN} - V_{P0W}|_{ZS}}{V_{LSb}|_{measured}} - codeN$$

Where:

| | | |
|---|---|---|
| $R\text{-}INL$ | = | Rheostat Integral Nonlinearity (LSb) |
| $V_{P0W}\|_{codeN}$ | = | Voltage Measured on the Wiper Pin for a Given Wiper Code (V) |
| $V_{P0W}\|_{ZS}$ | = | Voltage Measured on the Wiper Pin at Zero Scale Wiper Code (V) |
| $V_{LSb}\|_{measured}$ | = | Measured LSb Voltage Range (V) |
| $codeN$ | = | Wiper Register Value |

### B.3.4 RHEOSTAT DIFFERENTIAL NONLINEARITY (R-DNL)

The Rheostat Differential Nonlinearity (R-DNL) error is the measure of the step size between codes in the actual transfer function.

The ideal step size between codes is 1 LSb. A R-DNL error of zero implies that every code is exactly 1 LSb in size. If the R-DNL error is less than 1 LSb, MCP41U83 guarantees monotonic output and no missing codes. The R-DNL error is the measure of variations in code sizes from the ideal code size using the zero scale and full scale wiper code endpoints.

R-DNL is expressed in LSb and is calculated as shown in Equation B-14.

**EQUATION B-14:**

$$R - DNL = \frac{V_{P0W}|_{codeN+1} - V_{P0W}|_{codeN}}{V_{LSb}|_{measured}} - 1$$

Where:

| | | |
|---|---|---|
| $R\text{-}DNL$ | = | Rheostat Differential Nonlinearity (LSb) |
| $V_{P0W}\|_{codeN+1}$ | = | Voltage Measured on the Wiper Pin for a Given Wiper Code + 1 (V) |
| $V_{P0W}\|_{codeN}$ | = | Voltage Measured on the Wiper Pin for a Given Wiper Code (V) |
| $V_{LSb}\|_{measured}$ | = | Measured LSb Voltage Range (V) |
| $codeN$ | = | Wiper Register Value |

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### B.3.5 RHEOSTAT NOMINAL RESISTANCE TEMPERATURE COEFFICIENT (R-$R_{TC}$)

The Rheostat Nominal Resistance Temperature Coefficient (R-$R_{TC}$) quantifies the error in the Wiper-to-End resistance ($R_{WB}$) caused by temperature drift. This is typically the critical error when using MCP41U83 in adjustable resistor configuration.

R-$R_{TC}$ is calculated using Equation B-15.

**EQUATION B-15:**

$$R - R_{TC} = \frac{\frac{R_{WB}|_{max} - R_{WB}|_{min}}{R_{WB}|_{average}}}{T_{OP}|_{max} - T_{OP}|_{min}} \times 10^6$$

Where:

- $R\text{-}R_{TC}$ = Rheostat Nominal Resistance Temperature Coefficient (ppm/°C)
- $R_{WB}|_{max}$ = Maximum Wiper-to-End Resistance Value (kΩ)
- $R_{WB}|_{min}$ = Minimum Wiper-to-End Resistance Value (kΩ)
- $R_{WB}|_{average}$ = Typical Wiper-to-End Resistance Value (kΩ)
- $T_{min}$ = Minimum Operating Temperature (°C)
- $T_{max}$ = Maximum Operating Temperature (°C)

### B.3.6 RHEOSTAT CHANNEL-TO-CHANNEL MATCHING (P-$RM_{AB}$)

The Rheostat Channel-to-Channel Matching (R-$RM_{WB}$) quantifies the Wiper-to-End resistance ($R_{WB}$) error between channels 0 and 1.

R-$RM_{WB}$ is calculated using Equation B-16.

**EQUATION B-16:**

$$R - RM_{WB} = \frac{R_{WB0} - R_{WB1}}{\frac{1}{2} \cdot (R_{WB0} + R_{WB1})} \times 100$$

Where:

- $R\text{-}RM_{WB}$ = Potentiometer Channel-to-Channel Matching (%)
- $R_{WB0}$ = Channel 0 Wiper-to-End Resistance (kΩ)
- $R_{WB1}$ = Channel 1 Wiper-to-End Resistance (kΩ)

### B.3.7 POWER SUPPLY REJECTION RATIO (PSRR)

The Power Supply Rejection Ratio (PSRR) indicates how the voltage output of MCP41U83 ($V_{P0W}$) is affected by changes in the supply voltage. PSRR is the ratio of the change in $V_{P0W}$ to changes in $V_{DD}$ for the midscale output of the digital rheostat. $V_{P0W}$ is measured while $V_{DD}$ varies from 5.5V to 2.7V with a fixed current value.

PSS is calculated using Equation B-17 and expressed in dB.

**EQUATION B-17:**

$$PSRR = 20 \cdot \log\left(\frac{|V_{P0W}|_{5.5V} - V_{P0W}|_{2.7V}|}{5.5V - 2.7V}\right)$$

Where:

- $PSRR$ = Power Supply Rejection Ratio (dB)
- $V_{P0W}|_{5.5V}$ = P0W Voltage at $V_{DD}$ = 5.5V (V)
- $V_{P0W}|_{2.7V}$ = P0W Voltage at $V_{DD}$ = 2.7V (V)

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## B.4 Testing Circuits

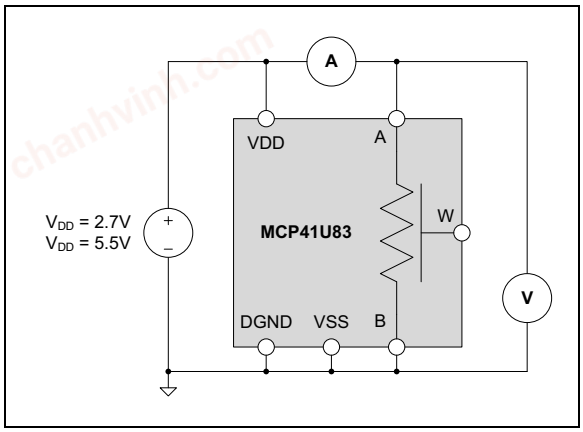



**FIGURE B-1:** *Test Circuit for $R_{AB}$ and P-$R_{TC}$.*

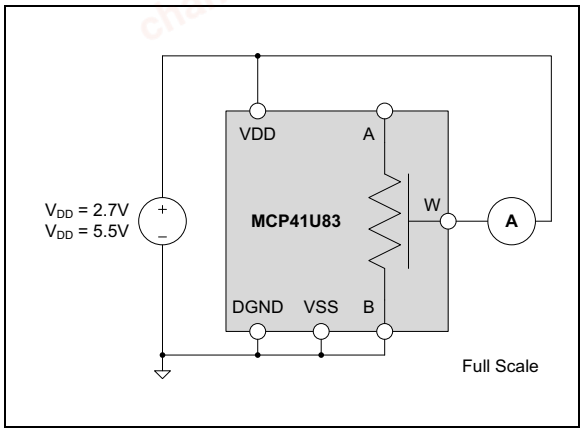



**FIGURE B-4:** *Test Circuit for $R_{WB}$ and R-$R_{TC}$.*

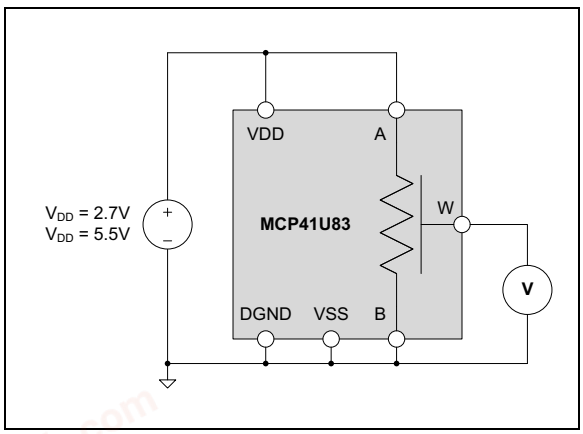



**FIGURE B-2:** *Test Circuit for Linearity Errors in Potentiometer Configuration (P-INL, P-DNL, FSE, ZSE and $V_{TC}$).*

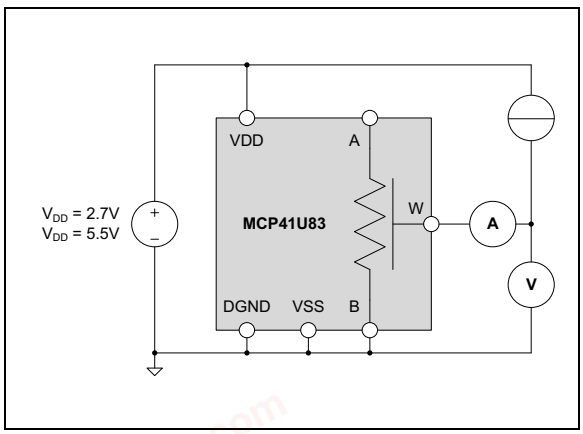



**FIGURE B-5:** *Test Circuit for Linearity Errors in Rheostat Configuration (R-INL, R-DNL and $R_W$).*

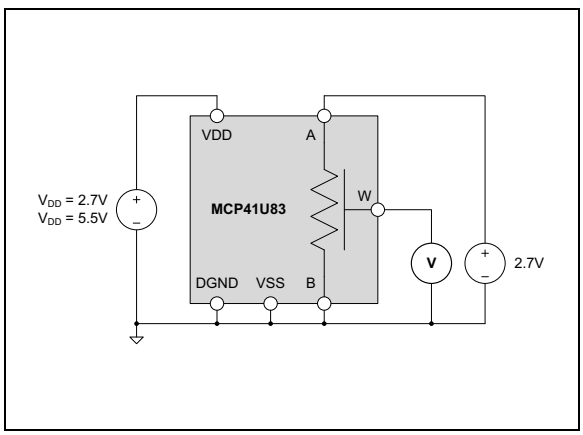



**FIGURE B-3:** *Test Circuit for PSS.*

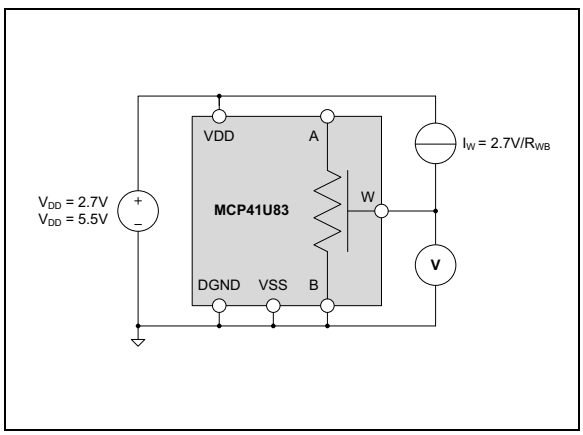



**FIGURE B-6:** *Test Circuit for PSRR.*

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## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, for example, on pricing or delivery, refer to the factory or a Microchip sales office.

| PART NO. | T[1] | -XXX | E | /XX | [XXX][2] |
|---|---|---|---|---|---|
| Device | Tape and Reel Option | End-to-End Resistance | Temperature Range | Package | Class |

| | | | |
|---|---|---|---|
| **Device:** | MCP41U83 | = | 10-Bit Single-Channel Digital Potentiometer |
| **Tape and Reel Option:** | T | = | Tape and Reel[1] |
| **End-to-End Resistance:** | -502 | = | $R_{AB}$ = 5 kΩ |
| | -103 | = | $R_{AB}$ = 10 kΩ |
| | -203 | = | $R_{AB}$ = 20 kΩ |
| | -503 | = | $R_{AB}$ = 50 kΩ |
| | -104 | = | $R_{AB}$ = 100 kΩ |
| **Temperature Range:** | E | = | -40°C to +125°C (Extended) |
| **Package:** | /ST | = | 14-Lead Thin Shrink Small Outline Package, 4.4 mm Body TSSOP |
| | /7N | = | 16-Lead Plastic Quad Flat, No Lead Package, 4x4 mm Body VQFN |
| **Class:** | Blank | = | Non-automotive |
| | VAO | = | Automotive |

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**2:** Automotive parts are AEC-Q100 Grade-1 qualified.

**Examples:**

a) MCP41U83T-502E/ST = 10-Bit Digital Potentiometer, Tape and Reel, $R_{AB}$ = 5 kΩ, Extended Temperature, 14-Lead TSSOP

b) MCP41U83T-103E/ST = 10-Bit Digital Potentiometer, Tape and Reel, $R_{AB}$ = 10 kΩ, Extended Temperature, 14-Lead TSSOP

c) MCP41U83T-203E/ST = 10-Bit Digital Potentiometer, Tape and Reel, $R_{AB}$ = 20 kΩ, Extended Temperature, 14-Lead TSSOP

d) MCP41U83T-503E/ST = 10-Bit Digital Potentiometer, Tape and Reel, $R_{AB}$ = 50 kΩ, Extended Temperature, 14-Lead TSSOP

e) MCP41U83T-104E/ST = 10-Bit Digital Potentiometer, Tape and Reel, $R_{AB}$ = 100 kΩ, Extended Temperature, 14-Lead TSSOP

f) MCP41U83T-502E/7N = 10-Bit Digital Potentiometer, Tape and Reel, $R_{AB}$ = 5 kΩ, Extended Temperature, 16-Lead VQFN

g) MCP41U83T-103E/7N = 10-Bit Digital Potentiometer, Tape and Reel, $R_{AB}$ = 10 kΩ, Extended Temperature, 16-Lead VQFN

h) MCP41U83T-203E/7N = 10-Bit Digital Potentiometer, Tape and Reel, $R_{AB}$ = 20 kΩ, Extended Temperature, 16-Lead VQFN

i) MCP41U83T-503E/7N = 10-Bit Digital Potentiometer, Tape and Reel, $R_{AB}$ = 50 kΩ, Extended Temperature, 16-Lead VQFN

j) MCP41U83T-104E/7N = 10-Bit Digital Potentiometer, Tape and Reel, $R_{AB}$ = 100 kΩ, Extended Temperature, 16-Lead VQFN

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# MCP41U83

## PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, for example, on pricing or delivery, refer to the factory or a Microchip sales office.

| PART NO. | T[1] | -XXX | E | /XX | [XXX][2] |
|---|---|---|---|---|---|
| Device | Tape and Reel Option | End-to-End Resistance | Temperature Range | Package | Class |

| | | | |
|---|---|---|---|
| **Device:** | MCP41U83 | = | 10-Bit Single-Channel Digital Potentiometer |
| **Tape and Reel Option:** | T | = | Tape and Reel[1] |
| **End-to-End Resistance:** | -502 | = | $R_{AB}$ = 5 kΩ |
| | -103 | = | $R_{AB}$ = 10 kΩ |
| | -203 | = | $R_{AB}$ = 20 kΩ |
| | -503 | = | $R_{AB}$ = 50 kΩ |
| | -104 | = | $R_{AB}$ = 100 kΩ |
| **Temperature Range:** | E | = | -40°C to +125°C (Extended) |
| **Package:** | /ST | = | 14-Lead Thin Shrink Small Outline Package, 4.4 mm Body TSSOP |
| | /7N | = | 16-Lead Plastic Quad Flat, No Lead Package, 4x4 mm Body VQFN |
| **Class:** | Blank | = | Non-automotive |
| | VAO | = | Automotive |

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**2:** Automotive parts are AEC-Q100 Grade-1 qualified.

**Examples:**

a) MCP41U83T-502E/STVAO = 10-Bit Digital Potentiometer, Tape and Reel, $R_{AB}$ = 5 kΩ, Extended Temperature, 14-Lead TSSOP, Automotive

b) MCP41U83T-103E/STVAO = 10-Bit Digital Potentiometer, Tape and Reel, $R_{AB}$ = 10 kΩ, Extended Temperature, 14-Lead TSSOP, Automotive

c) MCP41U83T-203E/STVAO = 10-Bit Digital Potentiometer, Tape and Reel, $R_{AB}$ = 20 kΩ, Extended Temperature, 14-Lead TSSOP, Automotive

d) MCP41U83T-503E/STVAO = 10-Bit Digital Potentiometer, Tape and Reel, $R_{AB}$ = 50 kΩ, Extended Temperature, 14-Lead TSSOP, Automotive

e) MCP41U83T-104E/STVAO = 10-Bit Digital Potentiometer, Tape and Reel, $R_{AB}$ = 100 kΩ, Extended Temperature, 14-Lead TSSOP, Automotive

f) MCP41U83T-502E/7NVAO = 10-Bit Digital Potentiometer, Tape and Reel, $R_{AB}$ = 5 kΩ, Extended Temperature, 16-Lead VQFN, Automotive

g) MCP41U83T-103E/7NVAO = 10-Bit Digital Potentiometer, Tape and Reel, $R_{AB}$ = 10 kΩ, Extended Temperature, 16-Lead VQFN, Automotive

h) MCP41U83T-203E/7NVAO = 10-Bit Digital Potentiometer, Tape and Reel, $R_{AB}$ = 20 kΩ, Extended Temperature, 16-Lead VQFN, Automotive

i) MCP41U83T-503E/7NVAO = 10-Bit Digital Potentiometer, Tape and Reel, $R_{AB}$ = 50 kΩ, Extended Temperature, 16-Lead VQFN, Automotive

j) MCP41U83T-104E/7NVAO = 10-Bit Digital Potentiometer, Tape and Reel, $R_{AB}$ = 100 kΩ, Extended Temperature, 16-Lead VQFN, Automotive


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