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MCP41HVX1

7/8-Bit Single, +36V (±18V) Digital POT with SPI Serial Interface and Volatile Memory

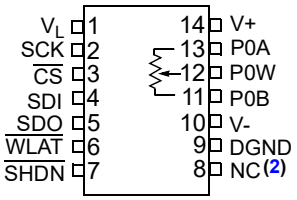
Features

- High-Voltage Analog Support:
  - +36V Terminal Voltage Range (DGND = V-)
  - ±18V Terminal Voltage Range (DGND = V- + 18V)
- Wide Operating Voltage:
  - Analog: 10V to 36V (specified performance)
  - Digital: 2.7V to 5.5V
    1.8V to 5.5V (DGND ≥ V- + 0.9V)
- Single Resistor Network
- Potentiometer Configuration Options
- Resistor Network Resolution
  - 7-bit: 127 resistors (128 Taps)
  - 8-bit: 255 resistors (256 Taps)
- R_{AB} Resistance Options:
  - 5 kΩ – 10 kΩ
  - 50 kΩ – 100 kΩ
- High Terminal/Wiper Current (I_W) Support:
  - 25 mA (for 5 kΩ)
  - 12.5 mA (for 10 kΩ)
  - 6.5 mA (for 50 kΩ and 100 kΩ)
- Zero-Scale to Full-Scale Wiper Operation
- Low Wiper Resistance: 75 Ω (Typical)
- Low Temperature Coefficient:
  - Absolute (Rheostat): 50 ppm typical (0°C to +70°C)
  - Ratiometric (Potentiometer): 15 ppm typical
- SPI Serial Interface (10 MHz, Modes 0,0 and 1,1)
- Resistor Network Terminal Disconnect Via:
  - Shutdown pin ($\overline{SHDN}$)
  - Terminal Control (TCON) register
- Write Latch ($\overline{WLAT}$) Pin to Control Update of Volatile Wiper Register (such as Zero Crossing)
- Power-on Reset/Brown-out Reset for Both:
  - Digital supply (V_L/DGND); 1.5V typical
  - Analog supply (V+/V-); 3.5V typical
- Serial Interface Inactive Current (3 µA Typical)
- 500 kHz Typical Bandwidth (-3 dB) Operation (5.0 kΩ Device)
- Extended Temperature Range (-40°C to +125°C)
- Package Types: TSSOP-14 and VQFN-20 (5x5)

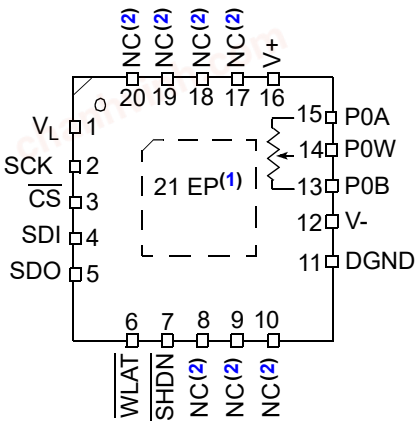
Package Types

MCP41HVX1 Single Potentiometer

TSSOP (ST)



5 x 5 VQFN (MQ)



Note 1: Exposed Pad (EP)
2: NC = Not Internally Connected

Description

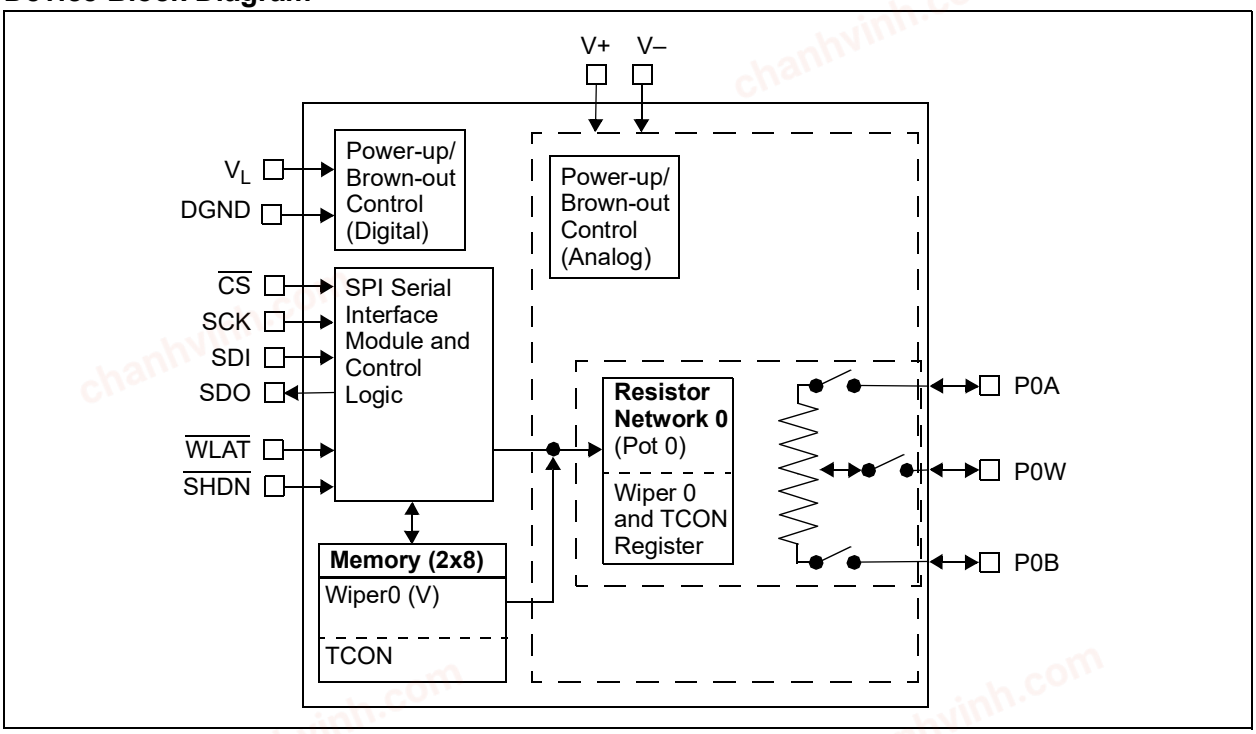
The MCP41HVX1 family of devices have dual power rails (analog and digital). The analog power rail allows high voltage on the resistor network terminal pins. The analog voltage range is determined by the V+ and V- voltages. The maximum analog voltage is +36V, while the operating analog output minimum specifications are specified from either 10V or 20V. As the analog supply voltage becomes smaller, the analog switch resistances increase, which affects certain performance specifications. The system can be implemented as dual rail (±18V) relative to the digital logic ground (DGND).

The device also has a Write Latch ($\overline{WLAT}$) function, which will inhibit the volatile wiper register from being updated (latched) with the received data until the $\overline{WLAT}$ pin is low. This allows the application to specify a condition where the volatile wiper register is updated (such as zero crossing).

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Device Block Diagram



Device Features

Device	# of POTs	Wiper Configuration	Control Interface	POR Wiper Setting	Resistance (Typical)		Number of:		Specified Operating Range	
					R_{AB} Options (kΩ)	Wiper - R_W (Ω)	R_S	Taps	V_L (2)	V+ (3)
MCP41HV31	1	Potentiometer (1)	SPI	3Fh	5.0, 10.0, 50.0, 100.0	75	127	128	1.8V to 5.5V	10V (4) to 36V
MCP41HV51	1	Potentiometer (1)	SPI	7Fh	5.0, 10.0, 50.0, 100.0	75	255	256	1.8V to 5.5V	10V (4) to 36V
MCP45HV31 (5)	1	Potentiometer (1)	I²C™	3Fh	5.0, 10.0, 50.0, 100.0	75	127	128	1.8V to 5.5V	10V (4) to 36V
MCP45HV51 (5)	1	Potentiometer (1)	I²C	7Fh	5.0, 10.0, 50.0, 100.0	75	255	256	1.8V to 5.5V	10V (4) to 36V

Note 1: Floating either terminal (A or B) allows the device to be used as a Rheostat (variable resistor).

2: This is relative to the DGND signal. There is a separate requirement for the V+/V- voltages: $V_L \geq$ V- + 2.7V.

3: Relative to V-, the V_L and DGND signals must be between (inclusive) V- and V+.

4: Analog operation will continue while the V+ voltage is above the device's analog Power-on Reset (POR)/Brown-out Reset (BOR) voltage. Operational characteristics may exceed specified limits while the V+ voltage is below the specified minimum voltage.

5: For additional information on these devices, refer to DS20005304.

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Voltage on V- with respect to DGND ..... DGND + 0.6V to -40.0V
Voltage on V+ with respect to DGND ..... DGND - 0.3V to 40.0V
Voltage on V+ with respect to V- ..... DGND - 0.3V to 40.0V
Voltage on V_L with respect to V+ ..... -0.6V to -40.0V
Voltage on V_L with respect to V- ..... -0.6V to +40.0V
Voltage on V_L with respect to DGND ..... -0.6V to +7.0V
Voltage on $\overline{CS}$, SCK, SDI, $\overline{WLAT}$, and $\overline{SHDN}$ with respect to DGND ..... -0.6V to V_L + 0.6V
Voltage on all other pins (PxA, PxW, and PxB) with respect to V- .....-0.3V to V+ + 0.3V
Input clamp current, I_{IK} (V_I < 0, V_I > V_L, V_I > V_{PP} on HV pins) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_L) ..... ±20 mA
Maximum current out of DGND pin ..... 100 mA
Maximum current into V_L pin ..... 100 mA
Maximum current out of V- pin ..... 100 mA
Maximum current into V+ pin ..... 100 mA
Maximum current into PxA, PxW, & PxB pins (Continuous)
- R_{AB} = 5 kΩ ..... ±25 mA
- R_{AB} = 10 kΩ ..... ±12.5 mA
- R_{AB} = 50 kΩ ..... ±6.5 mA
- R_{AB} = 100 kΩ ..... ±6.5 mA

Maximum current into PxA, PxW, & PxB pins (Pulsed)
- F_{PULSE} > 10 kHz ..... (Max $I_{Continuous}$)/(Duty Cycle)
- F_{PULSE} ≤ 10 kHz ..... (Max $I_{Continuous}$)/√ (Duty Cycle)

Maximum output current sunk by any Output pin ..... 25 mA
Maximum output current sourced by any Output pin ..... 25 mA
Package Power Dissipation (T_A = + 50°C, T_J = +150°C)
- TSSOP-14 ..... 1000 mW
- VQFN-20 (5x5) ..... 2800 mW

Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins
- Human Body Model (HBM) ..... ≥ ±4 kV
- Machine Model (MM) ..... ≥ ±400V
- Charged Device Model (CDM) for TSSOP-14 ..... ≥ ±1 kV

Maximum Junction Temperature (T_J) ..... 150°C
Storage temperature ..... -65°C to +150°C
Ambient temperature with power applied ..... -40°C to +125°C

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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AC/DC CHARACTERISTICS

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.				
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Digital Positive Supply Voltage (V_L)	V_L	2.7	—	5.5	V	With respect to DGND(4)
		1.8	—	5.5	V	DGND = V- + 0.9V (referenced to V-)(1,4)
		—	—	0	V	With respect to V+
Analog Positive Supply Voltage (V+)	V+	V_L(16)	—	36.0	V	With respect to V-(4)
Digital Ground Voltage (DGND)	V_{DGND}	V-	—	V+ - V_L	V	With respect to V-(4,5)
Analog Negative Supply Voltage (V-)	V-	-36.0 + V_L	—	0	V	With respect to DGND and V_L = 1.8V
Resistor Network Supply Voltage	V_{RN}	—	—	36V	V	Delta voltage between V+ and V-(4)
V_L Start Voltage to ensure Wiper Reset	V_{DPOR}	—	—	1.8	V	With respect to DGND, V+ > 6.0V RAM retention voltage (V_{RAM}) < V_{DBOR}
V+ Voltage to ensure Wiper Reset	V_{APOR}	—	—	6.0	V	With respect to V-, V_L = 0V RAM retention voltage (V_{RAM}) < V_{BOR}
Digital to Analog Level Shifter Operational Voltage	V_{LS}	—	—	2.3	V	V_L to V- voltage. DGND = V-
Power Rail Voltages during Power-Up(1)	V_{LPOR}	—	—	5.5	V	Digital Powers (V_L/DGND) up 1st: V+ and V- floating or as V+/V- powers up (V+ must be ≥ to DGND)(18)
	$V+_{POR}$	—	—	36	V	Analog Powers (V+/V-) up 1st: V_L and DGND floating or as V_L/DGND powers up (DGND must be between V- and V+)(18)
V_L Rise Rate to ensure Power-on Reset	V_{LRR}	Note 6			V/ms	With respect to DGND

Note 1 This specification is by design.

Note 4 V+ voltage is dependent on V- voltage. The maximum delta voltage between V+ and V- is 36V. The digital logic DGND potential can be anywhere between V+ and V-. The V_L potential must be ≥ DGND and ≤ V+.

Note 5 The minimum value determined by maximum V- to V+ potential equals 36V, and the minimum value for operation equals 1.8V. So, 36V - 1.8V = 34.2V.

Note 6 POR/BOR is not rate dependent.

Note 16 For specified analog performance, V+ must be 20V or greater (unless otherwise noted).

Note 18 During the power-up sequence, to ensure expected Analog POR operation, the two power systems (Analog and Digital) should have a common reference to ensure that the driven DGND voltage is not at a higher potential than the driven V+ voltage.

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Delay after device exits the reset state (V_L > V_{BOR})	T_{BORD}	—	10	20	µs		
Supply Current[7]	I_{DDD}	—	45	300	µA	Serial Interface Active, Write all 0's to Volatile Wiper 0 (address 0h) V_L = 5.5V, $\overline{CS}$ = V_{IL}, F_{SCK} = 5 MHz, V- = DGND	
		—	—	7	µA	Serial Interface Inactive, V_L = 5.5V, SCK = V_{IH}, $\overline{CS}$ = V_{IH}, Wiper = 0, V- = DGND	
	I_{DDA}	—	—	5	µA	Current V+ to V-, PxA = PxB = PxW, DGND = V- +(V+/2)	
Resistance (± 20%)[8]	R_{AB}	4.0	5	6.0	kΩ	-502 devices, V+/V- = 10V to 36V	
		8.0	10	12.0	kΩ	-103 devices, V+/V- = 10V to 36V	
		40.0	50	60.0	kΩ	-503 devices, V+/V- = 10V to 36V	
		80.0	100	120.0	kΩ	-104 devices, V+/V- = 10V to 36V	
R_{AB} Current	I_{AB}	—	—	9.00	mA	-502 devices	36V / $R_{AB(MIN)}$, V- = -18V, V+ = +18V[9]
		—	—	4.50	mA	-103 devices	
		—	—	0.90	mA	-503 devices	
		—	—	0.45	mA	-104 devices	
Resolution	N	256			Taps	8-bit	No Missing Codes
		128			Taps	7-bit	No Missing Codes
Step Resistance (see **Appendix B.4**)	R_S	—	R_{AB}/(255)	—	Ω	8-bit	**Note 1**
		—	R_{AB}/(127)	—	Ω	7-bit	**Note 1**

Note 1 This specification is by design.

Note 7 Supply current (IDDD and IDDA) is independent of current through the resistor network.

Note 8 Resistance (RAB) is defined as the resistance between Terminal A to Terminal B.

Note 9 Guaranteed by the R_{AB} specification and Ohms Law.

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Wiper Resistance (see **Appendix B.5**)	R_W	—	75	170	Ω	I_W = 1 mA	V+ = +18V, V- = -18V, code = 00h, PxA = floating, PxB = V-.
		—	145	200	Ω	I_W = 1 mA	V+ = +5.0V, V- = -5.0V, code = 00h, PxA = floating, PxB = V-(2)
Nominal Resistance Temperature Coefficient (see **Appendix B.23**)	$\Delta R_{AB}/\Delta T$	—	50	—	ppm/°C	T_A = -40°C to +85°C	
		—	100	—	ppm/°C	T_A = -40°C to +125°C	
Ratiometeric Tempco (see **Appendix B.22**)	$\Delta V_{WB}/\Delta T$	—	15	—	ppm/°C	Code = Mid-scale (80h or 40h)	
Resistor Terminal Input Voltage Range (Terminals A, B and W)	V_A, V_W, V_B	V-	—	V+	V	**Note 1**, **Note 11**	
Current through Terminals (A, B, and Wiper)(1)	I_T, I_W	—	—	25	mA	-502 devices	$I_{BW(W \neq ZS)}$ and $I_{AW(W \neq FS)}$
		—	—	12.5	mA	-103 devices	$I_{BW(W \neq ZS)}$ and $I_{AW(W \neq FS)}$
		—	—	6.5	mA	-503 devices	$I_{BW(W \neq ZS)}$ and $I_{AW(W \neq FS)}$
		—	—	6.5	mA	-104 devices	$I_{BW(W \neq ZS)}$ and $I_{AW(W \neq FS)}$
		—	—	36	mA	$I_{BW(W = ZS)}$, or $I_{AW(W = FS)}$	
Leakage current into A, W or B	I_{TL}	—	5	—	nA	A = W = B = V-	

Note 1 This specification is by design.

Note 2 This parameter is not tested, but specified by characterization.

Note 11 Resistor terminals A, W and B's polarity with respect to each other is not restricted.

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**		
Full-Scale Error (Potentiometer) (8-bit code = FFh, 7-bit code = 7Fh)[10,17] (V_A = V+, V_B = V-) (see Appendix B.10)	V_{WFSE}	-10.5	—	—	LSb	5 kΩ	8-bit	V_{AB} = 20V to 36V
		-8.5	—	—	LSb			V_{AB} = 20V to 36V -40°C ≤ T_A ≤ +85°C[2]
		-13.5	—	—	LSb			V_{AB} = 10V to 36V
		-5.5	—	—	LSb		7-bit	V_{AB} = 20V to 36V
		-4.5	—	—	LSb			V_{AB} = 20V to 36V -40°C ≤ T_A ≤ +85°C[2]
		-7.0	—	—	LSb			V_{AB} = 10V to 36V
		-4.5	—	—	LSb	10 kΩ	8-bit	V_{AB} = 20V to 36V
		-6.0	—	—	LSb			V_{AB} = 10V to 36V
		-2.65	—	—	LSb		7-bit	V_{AB} = 20V to 36V
		-2.25	—	—	LSb			V_{AB} = 20V to 36V -40°C ≤ T_A ≤ +85°C[2]
		-3.5	—	—	LSb			V_{AB} = 10V to 36V
		-1.0	—	—	LSb	50 kΩ	8-bit	V_{AB} = 20V to 36V
		-0.9	—	—	LSb			V_{AB} = 20V to 36V -40°C ≤ T_A ≤ +85°C[2]
		-1.4	—	—	LSb			V_{AB} = 10V to 36V
		-1.25	—	—	LSb			V_{AB} = 10V to 36V -40°C ≤ T_A ≤ +85°C[2]
		-0.95	—	—	LSb		7-bit	V_{AB} = 20V to 36V
		-1.2	—	—	LSb			V_{AB} = 10V to 36V
		-1.1	—	—	LSb			V_{AB} = 10V to 36V -40°C ≤ T_A ≤ +85°C[2]
		-0.7	—	—	LSb	100 kΩ	8-bit	V_{AB} = 20V to 36V
		-0.95	—	—	LSb			V_{AB} = 10V to 36V
		-0.7	—	—	LSb			V_{AB} = 10V to 36V -40°C ≤ T_A ≤ +85°C[2]
		-0.85	—	—	LSb		7-bit	V_{AB} = 20V to 36V
		-0.9	—	—	LSb			V_{AB} = 10V to 36V

Note 2 This parameter is not tested, but specified by characterization.

Note 10 Measured at V_W with V_A = V+ and V_B = V-.

Note 17 Analog switch leakage affects this specification. Higher temperatures increase the switch leakage.

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**		
Zero-Scale Error (Potentiometer) (8-bit code = 00h, 7-bit code = 00h)(10,17) (V_A = V+, V_B = V-) (see Appendix B.11)	V_{WZSE}	—	—	+8.5	LSb	5 kΩ	8-bit	V_{AB} = 20V to 36V
		—	—	+13.5	LSb			V_{AB} = 10V to 36V
		—	—	+4.5	LSb		7-bit	V_{AB} = 20V to 36V
		—	—	+7.0	LSb			V_{AB} = 10V to 36V
		—	—	+4.0	LSb	10 kΩ	8-bit	V_{AB} = 20V to 36V
		—	—	+6.5	LSb			V_{AB} = 10V to 36V
		—	—	+6.0	LSb			V_{AB} = 10V to 36V -40°C ≤ T_A ≤ +85°C(2)
		—	—	+2.0	LSb		7-bit	V_{AB} = 20V to 36V
		—	—	+3.25	LSb			V_{AB} = 10V to 36V
		—	—	+3.0	LSb			V_{AB} = 10V to 36V -40°C ≤ T_A ≤ +85°C(2)
		—	—	+0.9	LSb	50 kΩ	8-bit	V_{AB} = 20V to 36V
		—	—	+0.8	LSb			V_{AB} = 20V to 36V -40°C ≤ T_A ≤ +85°C(2)
		—	—	+1.3	LSb			V_{AB} = 10V to 36V
		—	—	+1.2	LSb			V_{AB} = 10V to 36V -40°C ≤ T_A ≤ +85°C(2)
		—	—	+0.5	LSb		7-bit	V_{AB} = 20V to 36V
		—	—	+0.7	LSb			V_{AB} = 10V to 36V
		—	—	+0.5	LSb	100 kΩ	8-bit	V_{AB} = 20V to 36V
		—	—	+0.95	LSb			V_{AB} = 10V to 36V
		—	—	+0.7	LSb			V_{AB} = 10V to 36V -40°C ≤ T_A ≤ +85°C(2)
		—	—	+0.25	LSb		7-bit	V_{AB} = 20V to 36V
		—	—	+0.4	LSb			V_{AB} = 10V to 36V

Note 2 This parameter is not tested, but specified by characterization.

Note 10 Measured at V_W with V_A = V+ and V_B = V-.

Note 17 Analog switch leakage affects this specification. Higher temperatures increase the switch leakage.

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**		
Potentiometer Integral Nonlinearity(10, 17) (see **Appendix B.12**)	P-INL	-1	±0.5	+1	LSb	5 kΩ	8-bit	V_{AB} = 10V to 36V
		-0.5	±0.25	+0.5	LSb		7-bit	V_{AB} = 10V to 36V
		-1	±0.5	+1	LSb	10 kΩ	8-bit	V_{AB} = 10V to 36V
		-0.5	±0.25	+0.5	LSb		7-bit	V_{AB} = 10V to 36V
		-1.1	±0.5	+1.1	LSb	50 kΩ	8-bit	V_{AB} = 10V to 36V
		-1	±0.5	+1	LSb			V_{AB} = 20V to 36V(2)
		-1	±0.5	+1	LSb			V_{AB} = 10V to 36V, -40°C ≤ T_A ≤ +85°C(2)
		-0.6	±0.25	+0.6	LSb		7-bit	V_{AB} = 10V to 36V
		-1.85	±0.5	+1.85	LSb	100 kΩ	8-bit	V_{AB} = 10V to 36V
		-1.2	±0.5	+1.2	LSb			V_{AB} = 20V to 36V(2)
		-1	±0.5	+1	LSb			V_{AB} = 10V to 36V, -40°C ≤ T_A ≤ +85°C(2)
		-1	±0.5	+1	LSb		7-bit	V_{AB} = 10V to 36V
Potentiometer Differential Nonlinearity(10, 17) (see **Appendix B.13**)	P-DNL	-0.5	±0.25	+0.5	LSb	5 kΩ	8-bit	V_{AB} = 10V to 36V
		-0.25	±0.125	+0.25	LSb		7-bit	V_{AB} = 10V to 36V
		-0.375	±0.125	+0.375	LSb	10 kΩ	8-bit	V_{AB} = 10V to 36V
		-0.125	±0.1	+0.125	LSb		7-bit	V_{AB} = 10V to 36V
		-0.25	±0.125	+0.25	LSb	50 kΩ	8-bit	V_{AB} = 10V to 36V
		-0.125	±0.1	+0.125	LSb		7-bit	V_{AB} = 10V to 36V
		-0.25	±0.125	+0.25	LSb	100 kΩ	8-bit	V_{AB} = 10V to 36V
		-0.125	-0.15	+0.125	LSb		7-bit	V_{AB} = 10V to 36V

Note 2 This parameter is not tested, but specified by characterization.

Note 10 Measured at V_W with V_A = V+ and V_B = V-.

Note 17 Analog switch leakage affects this specification. Higher temperatures increase the switch leakage.

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**		
Bandwidth -3 dB (load = 30 pF) (see **Appendix B.24**)	BW	—	480	—	kHz	5 kΩ	8-bit	Code = 7Fh
		—	480	—	kHz		7-bit	Code = 3Fh
		—	240	—	kHz	10 kΩ	8-bit	Code = 7Fh
		—	240	—	kHz		7-bit	Code = 3Fh
		—	48	—	kHz	50 kΩ	8-bit	Code = 7Fh
		—	48	—	kHz		7-bit	Code = 3Fh
		—	24	—	kHz	100 kΩ	8-bit	Code = 7Fh
		—	24	—	kHz		7-bit	Code = 3Fh
V_W Settling Time (V_A = 10V, V_B = 0V, ±1LSb error band, C_L = 50 pF) (see **Appendix B.17**)	t_S	—	1	—	µs	5 kΩ	Code = 00h → FFh (7Fh); FFh (7Fh) → 00h	
		—	1	—	µs	10 kΩ	Code = 00h → FFh (7Fh); FFh (7Fh) → 00h	
		—	2.5	—	µs	50 kΩ	Code = 00h → FFh (7Fh); FFh (7Fh) → 00h	
		—	5	—	µs	100 kΩ	Code = 00h → FFh (7Fh); FFh (7Fh) → 00h	

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**		
Rheostat Integral Nonlinearity[12,13,14,17] (see Appendix B.5)	R-INL	-1.75	—	+1.75	LSb	5 kΩ	8-bit	I_W = 6.0 mA, (V+ - V-) = 36V[2]
		-2.5	—	+2.5	LSb			I_W = 3.3 mA, (V+ - V-) = 20V[2]
		-4.0	—	+4.0	LSb			I_W = 1.7 mA, (V+ - V-) = 10V
		-1.0	—	+1.0	LSb		7-bit	I_W = 6.0 mA, (V+ - V-) = 36V[2]
		-1.5	—	+1.5	LSb			I_W = 3.3 mA, (V+ - V-) = 20V[2]
		-2.0	—	+2.0	LSb			I_W = 1.7 mA, (V+ - V-) = 10V
		-1.0	—	+1.0	LSb	10 kΩ	8-bit	I_W = 3.0 mA, (V+ - V-) = 36V[2]
		-1.75	—	+1.75	LSb			I_W = 1.7 mA, (V+ - V-) = 20V[2]
		-2.0	—	+2.0	LSb			I_W = 830 µA, (V+ - V-) = 10V
		-0.6	—	+0.6	LSb		7-bit	I_W = 3.0 mA, (V+ - V-) = 36V[2]
		-0.8	—	+0.8	LSb			I_W = 1.7 mA, (V+ - V-) = 20V[2]
		-1.0	—	+1.0	LSb			I_W = 830 µA, (V+ - V-) = 10V
		-1.0	—	+1.0	LSb	50 kΩ	8-bit	I_W = 600 µA, (V+ - V-) = 36V[2]
		-1.0	—	+1.0	LSb			I_W = 330 µA, (V+ - V-) = 20V[2]
		-1.2	—	+1.2	LSb			I_W = 170 µA, (V+ - V-) = 10V
		-0.5	—	+0.5	LSb		7-bit	I_W = 600 µA, (V+ - V-) = 36V[2]
		-0.5	—	+0.5	LSb			I_W = 330 µA, (V+ - V-) = 20V[2]
		-0.6	—	+0.6	LSb			I_W = 170 µA, (V+ - V-) = 10V
		-1.0	—	+1.0	LSb	100 kΩ	8-bit	I_W = 300 µA, (V+ - V-) = 36V[2]
		-1.0	—	+1.0	LSb			I_W = 170 µA, (V+ - V-) = 20V[2]
		-1.2	—	+1.2	LSb			I_W = 83 µA, (V+ - V-) = 10V
		-0.5	—	+0.5	LSb		7-bit	I_W = 300 µA, (V+ - V-) = 36V[2]
		-0.5	—	+0.5	LSb			I_W = 170 µA, (V+ - V-) = 20V[2]
		-0.6	—	+0.6	LSb			I_W = 83 µA, (V+ - V-) = 10V

Note 2 This parameter is not tested, but specified by characterization.

Note 12 Nonlinearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

Note 13 Externally connected to a Rheostat configuration (RBW), and then tested.

Note 14 Wiper current (I_W) condition determined by $R_{AB(max)}$ and Voltage Condition, the delta voltage between V+ and V- (voltages are 36V, 20V, and 10V).

Note 17 Analog switch leakage affects this specification. Higher temperatures increase the switch leakage.

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**		
Rheostat Differential Nonlinearity (12,13,14,17) (see Appendix B.5)	R-DNL	-0.5	—	+0.5	LSb	5 kΩ	8-bit	I_W = 6.0 mA, (V+ - V-) = 36V(2)
		-0.5	—	+0.5	LSb			I_W = 3.3 mA, (V+ - V-) = 20V(2)
		-0.8	—	+0.8	LSb			I_W = 1.7 mA, (V+ - V-) = 10V
		-0.6	—	+0.6	LSb			I_W = 1.7 mA, (V+ - V-) = 10V -40°C ≤ T_A ≤ +85°C(2)
		-0.25	—	+0.25	LSb		7-bit	I_W = 6.0 mA, (V+ - V-) = 36V(2)
		-0.25	—	+0.25	LSb			I_W = 3.3 mA, (V+ - V-) = 20V(2)
		-0.3	—	+0.3	LSb			I_W = 1.7 mA, (V+ - V-) = 10V
		-0.5	—	+0.5	LSb	10 kΩ	8-bit	I_W = 3.0 mA, (V+ - V-) = 36V(2)
		-0.5	—	+0.5	LSb			I_W = 1.7 mA, (V+ - V-) = 20V(2)
		-0.5	—	+0.5	LSb			I_W = 830 µA, (V+ - V-) = 10V
		-0.25	—	+0.25	LSb		7-bit	I_W = 3.0 mA, (V+ - V-) = 36V(2)
		-0.25	—	+0.25	LSb			I_W = 1.7 mA, (V+ - V-) = 20V(2)
		-0.25	—	+0.25	LSb			I_W = 830 µA, (V+ - V-) = 10V
		-0.5	—	+0.5	LSb	50 kΩ	8-bit	I_W = 600 µA, (V+ - V-) = 36V(2)
		-0.5	—	+0.5	LSb			I_W = 330 µA, (V+ - V-) = 20V(2)
		-0.5	—	+0.5	LSb			I_W = 170 µA, (V+ - V-) = 10V
		-0.25	—	+0.25	LSb		7-bit	I_W = 600 µA, (V+ - V-) = 36V(2)
		-0.25	—	+0.25	LSb			I_W = 330 µA, (V+ - V-) = 20V(2)
		-0.25	—	+0.25	LSb			I_W = 170 µA, (V+ - V-) = 10V
		-0.5	—	+0.5	LSb	100 kΩ	8-bit	I_W = 300 µA, (V+ - V-) = 36V(2)
		-0.5	—	+0.5	LSb			I_W = 170 µA, (V+ - V-) = 20V(2)
		-0.5	—	+0.5	LSb			I_W = 83 µA, (V+ - V-) = 10V
		-0.25	—	+0.25	LSb		7-bit	I_W = 300 µA, (V+ - V-) = 36V(2)
		-0.25	—	+0.25	LSb			I_W = 170 µA, (V+ - V-) = 20V(2)
		-0.25	—	+0.25	LSb			I_W = 83 µA, (V+ - V-) = 10V

Note 2 This parameter is not tested, but specified by characterization.

Note 12 Nonlinearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

Note 13 Externally connected to a Rheostat configuration (RBW), and then tested.

Note 14 Wiper current (I_W) condition determined by $R_{AB(max)}$ and Voltage Condition, the delta voltage between V+ and V- (voltages are 36V, 20V, and 10V).

Note 17 Analog switch leakage affects this specification. Higher temperatures increase the switch leakage.

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.				
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Capacitance (P_A)	C_A	—	75	—	pF	Measured to V-, f =1 MHz, Wiper code = Mid-Scale
Capacitance (P_w)	C_W	—	120	—	pF	Measured to V-, f =1 MHz, Wiper code = Mid-Scale
Capacitance (P_B)	C_B	—	75	—	pF	Measured to V-, f =1 MHz, Wiper code = Mid-Scale
Common-Mode Leakage	I_{CM}	—	5	—	nA	$V_A = V_B = V_W$
Digital Interface Pin Capacitance	C_{IN}, C_{OUT}	—	10	—	pF	f_C = 400 kHz
Digital Inputs/Outputs ($\overline{CS}$, SDI, SDO, SCK, $\overline{SHDN}$, $\overline{WLAT}$)						
Schmitt Trigger High-Input Threshold	V_{IH}	0.45 V_L	—	V_L + 0.3V	V	2.7V ≤ V_L ≤ 5.5V
		0.5 V_L	—	V_L + 0.3V	V	1.8V ≤ V_L ≤ 2.7V
Schmitt Trigger Low-Input Threshold	V_{IL}	DGND - 0.5V	—	0.2 V_L	V	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	0.1 V_L	—	V	
Output Low Voltage (SDO)	V_{OL}	DGND	—	0.2 V_L	V	V_L = 5.5V, I_{OL} = 5 mA
		DGND	—	0.2 V_L	V	V_L = 1.8V, I_{OL} = 800 µA
Output High Voltage (SDO)	V_{OH}	0.8 V_L	—	V_L	V	V_L = 5.5V, I_{OH} = -2.5 mA
		0.8 V_L	—	V_L	V	V_L = 1.8V, I_{OL} = -800 µA
Input Leakage Current	I_{IL}	-1		1	uA	$V_{IN} = V_L$ and V_{IN} = DGND

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max**	**Units**	**Conditions**	
RAM (Wiper, TCON) Value							
Wiper Value Range	N	0h	—	FFh	hex	8-bit	
		0h	—	7Fh	hex	7-bit	
Wiper POR/BOR Value	$N_{POR/BOR}$	7Fh			hex	8-bit	
		3Fh			hex	7-bit	
TCON Value Range	N	0h	—	FFh	hex		
TCON POR/BOR Value	N_{TCON}	FF			hex	All Terminals connected	
Power Requirements							
Power Supply Sensitivity (see **Appendix B.20**)	PSS	—	0.0015	0.0035	%/%	8-bit	V_L = 2.7V to 5.5V, V+ = 18V, V- = -18V, Code = 7Fh
		—	0.0015	0.0035	%/%	7-bit	V_L = 2.7V to 5.5V, V+ = 18V, V- = -18V, Code = 3Fh
Power Dissipation	P_{DISS}	—	260	—	mW	5 kΩ	V_L = 5.5V, V+ = 18V, V- = -18V(15)
		—	130	—	mW	10 kΩ	
		—	26	—	mW	50 kΩ	
		—	13	—	mW	100 kΩ	

Note 15 $P_{DISS} = I * V$, or $((I_{DDD} * 5.5V) + (I_{DDA} * 36V) + (I_{AB} * 36V))$.

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AC/DC Notes:

1. This specification is by design.
2. This parameter is not tested, but specified by characterization.
3. See Absolute Maximum Ratings.
4. V+ voltage is dependent on V- voltage. The maximum delta voltage between V+ and V- is 36V. The digital logic DGND potential can be anywhere between V+ and V-. The V_L potential must be ≥ DGND and ≤ V+.
5. The minimum value determined by maximum V- to V+ potential equals 36V, and the minimum value for operation equals 1.8V. So, 36V - 1.8V = 34.2V.
6. POR/BOR is not rate dependent.
7. Supply current (I_{DDD} and I_{DDA}) is independent of current through the resistor network.
8. Resistance (R_{AB}) is defined as the resistance between Terminal A to Terminal B.
9. Guaranteed by the R_{AB} specification and Ohms Law.
10. Measured at V_W with V_A = V+ and V_B = V-.
11. Resistor terminals A, W and B's polarity with respect to each other is not restricted.
12. Nonlinearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.
13. Externally connected to a Rheostat configuration (R_{BW}), and then tested.
14. Wiper current (I_W) condition determined by $R_{AB(max)}$ and Voltage Condition, the delta voltage between V+ and V- (voltages are 36V, 20V, and 10V).
15. $P_{DISS} = I * V$, or $((I_{DDD} * 5.5V) + (I_{DDA} * 36V) + (I_{AB} * 36V))$.
16. For specified analog performance, V+ must be 20V or greater (unless otherwise noted).
17. Analog switch leakage affects this specification. Higher temperatures increase the switch leakage.
18. During the power-up sequence, to ensure expected Analog POR operation, the two power systems (Analog and Digital) should have a common reference to ensure that the driven DGND voltage is not at a higher potential than the driven V+ voltage.

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1.1 SPI Mode Timing Waveforms and Requirements

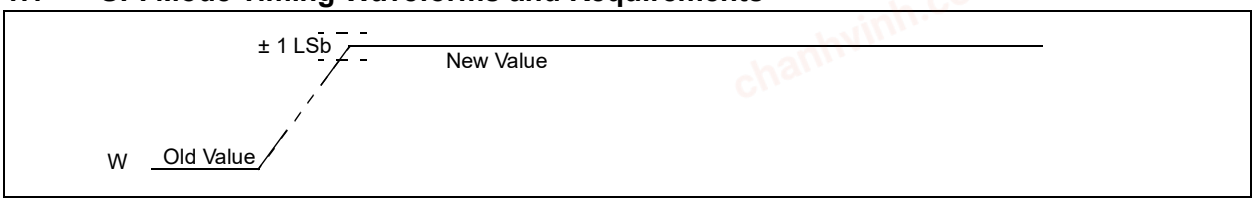


FIGURE 1-1: *Settling Time Waveforms.*

TABLE 1-1: WIPER SETTLING TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V+ = 10V to 36V (referenced to V-); V+ = +5V to +18V & V- = -5.0V to -18V (referenced to DGND ≥ ±5V to ±18V), V_L = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_L = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
V_W Settling Time (V_A = 10V, V_B = 0V, ±1LSb error band, C_L = 50 pF) (see **Appendix B.17**)	t_S	—	1	—	µs	5 kΩ	Code = 00h ≥ FFh (7Fh); FFh (7Fh) ≥ 00h
		—	1	—	µs	10 kΩ	Code = 00h ≥ FFh (7Fh); FFh (7Fh) ≥ 00h
		—	2.5	—	µs	50 kΩ	Code = 00h ≥ FFh (7Fh); FFh (7Fh) ≥ 00h
		—	5	—	µs	100 kΩ	Code = 00h ≥ FFh (7Fh); FFh (7Fh) ≥ 00h

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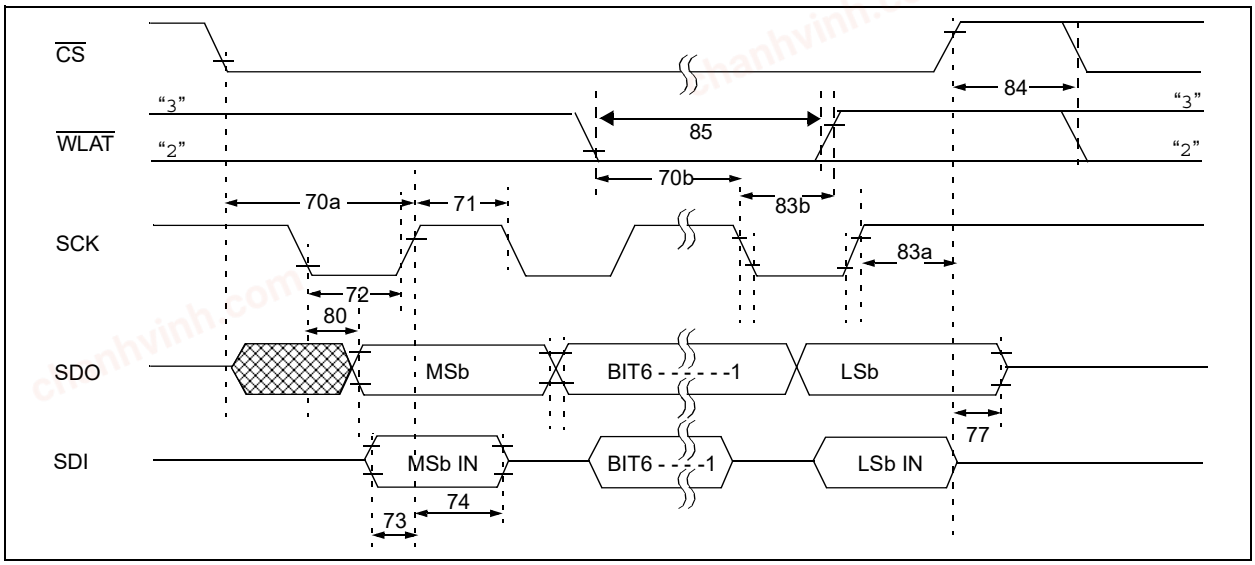


FIGURE 1-2: *SPI Timing Waveform (Mode = 11).*

TABLE 1-2: SPI REQUIREMENTS (MODE = 11)

#	Characteristic	Symbol	Min.	Max.	Units	Conditions
	SCK Input Frequency	F_{SCK}	—	10	MHz	V_L = 2.7V to 5.5V
			—	1	MHz	V_L = 1.8V to 2.7V
70a	$\overline{CS}$ Active (V_{IL}) to SCK↑ input	TcsA2scH	25	—	ns	
70b	$\overline{WLAT}$ Active (V_{IL}) to eighth (or sixteenth) SCK↓ of the Serial Command to ensure previous data is latched (set-up time)	TwlA2scH	20	—	ns	
71	SCK input high time	TscH	35	—	ns	V_L = 2.7V to 5.5V
			120	—	ns	V_L = 1.8V to 2.7V
72	SCK input low time	TscL	35	—	ns	V_L = 2.7V to 5.5V
			120	—	ns	V_L = 1.8V to 2.7V
73	Set-up time of SDI input to SCK↑ edge	TDIV2scH	10	—	ns	
74	Hold time of SDI input from SCK↑ edge	TscH2DIL	20	—	ns	
77	$\overline{CS}$ Inactive (V_{IH}) to SDO output high-impedance	TcsH2DOZ	—	50	ns	**Note 1**
80	SDO data output valid after SCK↓ edge	TscL2DOV	—	55	ns	V_L = 2.7V to 5.5V
				90	ns	V_L = 1.8V to 2.7V
83a	$\overline{CS}$ Inactive (V_{IH}) after SCK↑ edge	TscH2csI	100	—	ns	
83b	$\overline{WLAT}$ Inactive (V_{IH}) after eighth (or sixteenth) SCK↓ edge (hold time)	TscH2wlatI	50	—	ns	
84	Hold time of $\overline{CS}$ (or $\overline{WLAT}$) Inactive (V_{IH}) to $\overline{CS}$ (or $\overline{WLAT}$) Active (V_{IL})	TcsA2csI	20	—	ns	
85	$\overline{WLAT}$ input low time	T_{WLAT}L	25	—	ns	

Note 1: This specification is by design.

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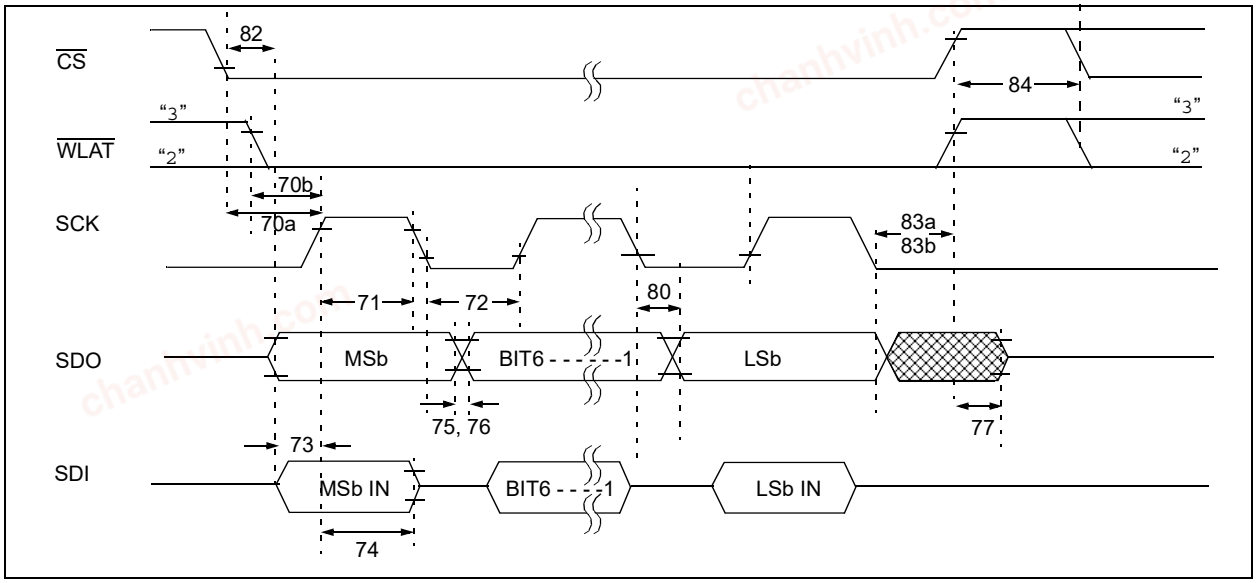


FIGURE 1-3: *SPI Timing Waveform (Mode = 00).*

TABLE 1-3: SPI REQUIREMENTS (MODE = 00)

#	Characteristic	Symbol	Min.	Max.	Units	Conditions
	SCK Input Frequency	F_{SCK}	—	10	MHz	V_L = 2.7V to 5.5V
			—	1	MHz	V_L = 1.8V to 2.7V
70a	$\overline{CS}$ Active (V_{IL}) to SCK↑ input	TcsA2scH	25	—	ns	
70b	$\overline{WLAT}$ Active (V_{IL}) to eighth (or sixteenth) SCK↓ of the Serial Command to ensure previous data is latched (setup time)	TwlA2scH	20	—	ns	
71	SCK input high time	TscH	35	—	ns	V_L = 2.7V to 5.5V
			120	—	ns	V_L = 1.8V to 2.7V
72	SCK input low time	TscL	35	—	ns	V_L = 2.7V to 5.5V
			120	—	ns	V_L = 1.8V to 2.7V
73	Set-up time of SDI input to SCK↑ edge	TDIV2scH	10	—	ns	
74	Hold time of SDI input from SCK↑ edge	TscH2DIL	20	—	ns	
77	$\overline{CS}$ Inactive (V_{IH}) to SDO output high-impedance	TcsH2DOZ	—	50	ns	**Note 1**
80	SDO data output valid after SCK↓ edge	TscL2DOV	—	55	ns	V_L = 2.7V to 5.5V
				90	ns	V_L = 1.8V to 2.7V
82	SDO data output valid after $\overline{CS}$ Active (V_{IL})	TscL2DOV	—	70	ns	
83a	$\overline{CS}$ Inactive (V_{IH}) after SCK↓ edge	TscL2csI	100	—	ns	
83b	$\overline{WLAT}$ Inactive (V_{IH}) after SCK↓ edge	TscL2wlatI	50	—	ns	
84	Hold time of $\overline{CS}$ (or $\overline{WLAT}$) Inactive (V_{IH}) to $\overline{CS}$ (or $\overline{WLAT}$) Active (V_{IL})	TcsA2csI	20	—	ns	
85	$\overline{WLAT}$ input low time	T_{WLAT}L	25	—	ns	

Note 1: This specification is by design.

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TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 14L-TSSOP (ST)	θ_{JA}	—	100	—	°C/W	
Thermal Resistance, 20L-VQFN (MQ)	θ_{JA}	—	38.3	—	°C/W	

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2.0 TYPICAL PERFORMANCE CURVES

Note: The device Performance Curves are available in a separate document. This is done to keep the file size of this PDF document less than the 10 MB file attachment limit of many servers.
The MCP41HVX1 Performance Curves document is literature number DS20005209, and can be found on the Microchip website. Look at the MCP41HVX1 Product Page under Documentation and Software, in the Data Sheets category.

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.
Additional descriptions of the device pins follows.

TABLE 3-1: PINOUT DESCRIPTION FOR THE MCP41HVX1

Pin		Symbol	Type	Buffer Type	Function
TSSOP 14L	VQFN 20L				
1	1	V_L	P	—	Positive Digital Power Supply Input
2	2	SCK	I	ST	SPI Serial Clock pin
3	3	$\overline{CS}$	I	ST	Chip Select
4	4	SDI	I	ST	SPI Serial Data In pin
5	5	SDO	O	—	SPI Serial Data Out
6	6	$\overline{WLAT}$	I	ST	Wiper Latch Enable 0 = Received SPI Shift Register Buffer (SPIBUF) value is transferred to Wiper register 1 = Received SPI data value is held in SPI Shift Register Buffer (SPIBUF)
7	7	$\overline{SHDN}$	I	ST	Shutdown
8	8, 9, 10, 17, 18, 19, 20	NC	—	—	Pin not internally connected to die. To reduce noise coupling, connect pin either to DGND or V_L.
9	11	DGND	P	—	Ground
10	12	V-	P	—	Analog Negative Potential Supply
11	13	P0B	I/O	A	Potentiometer 0 Terminal B
12	14	P0W	I/O	A	Potentiometer 0 Wiper Terminal
13	15	P0A	I/O	A	Potentiometer 0 Terminal A
14	16	V+	P	—	Analog Positive Potential Supply
—	21	EP	P	—	Exposed Pad, connect to V- signal or Not Connected (floating)(1)

Legend: A = Analog, ST = Schmitt Trigger, I = Input, O = Output, I/O = Input/Output, P = Power

Note 1: The VQFN package has a contact on the bottom of the package. This contact is conductively connected to the die substrate, and therefore should be unconnected or connected to the same ground as the device's V- pin.

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3.1 Positive Power Supply Input (V_L)

The V_L pin is the device's positive power supply input. The input power supply is relative to DGND and can range from 1.8V to 5.5V. A decoupling capacitor on V_L (to DGND) is recommended to achieve maximum performance.

While the device's $V_L < V_{min}$ (2.7V), the electrical performance of the device may not meet the data sheet specifications.

3.2 Serial Clock (SCK)

The SCK pin is the serial interface's Serial Clock pin. This pin is connected to the host controllers' SCK pin. The MCP41HVX1 is an SPI slave device, so its SCK pin is an input-only pin.

3.3 Chip Select ($\overline{CS}$)

The $\overline{CS}$ pin is the serial interface's chip select input. Forcing the $\overline{CS}$ pin to V_{IL} enables the serial commands.

3.4 Serial Data In (SDI)

The SDI pin is the serial interface's Serial Data In pin. This pin is connected to the host controller's SDO pin.

3.5 Serial Data Out (SDO)

The SDO pin is the serial interface's Serial Data Out pin. This pin is connected to the host controller's SDI pin. This pin allows the host controller to read the digital potentiometer registers (Wiper and TCON), or monitor the state of the command error bit.

3.6 Wiper Latch ($\overline{WLAT}$)

The $\overline{WLAT}$ pin is used to delay the transfer of the received wiper value (in the shift register) to the wiper register. This allows this transfer to be synchronized to an external event (such as zero crossing). See **Section 4.3.2 "Wiper Latch"**.

3.7 Shutdown ($\overline{SHDN}$)

The $\overline{SHDN}$ pin is used to force the resistor network terminals into the hardware shutdown state. See **Section 4.3.1 "Shutdown"**.

3.8 Digital Ground (DGND)

The DGND pin is the device's digital ground reference.

3.9 Not Connected (NC)

This pin is not internally connected to the die. To reduce noise coupling, these pins should be connected to either V_L or DGND.

3.10 Analog Negative Voltage (V-)

Analog circuitry negative supply voltage. Must **not** have a higher potential then the DGND pin.

3.11 Potentiometer Terminal B

The Terminal B pin is connected to the internal potentiometer's terminal B.

The potentiometer's terminal B is the fixed connection to the zero-scale wiper value of the digital potentiometer. This corresponds to a wiper value of 0x00 for both 7-bit and 8-bit devices.

The Terminal B pin does not have a polarity relative to the Terminal W or A pins. The Terminal B pin can support both positive and negative current. The voltage on Terminal B must be between V+ and V-.

3.12 Potentiometer Wiper (W) Terminal

The Terminal W pin is connected to the internal potentiometer's Terminal W (the Wiper). The wiper terminal is the adjustable terminal of the digital potentiometer. The Terminal W pin does not have a polarity relative to terminal's A or B pins. The Terminal W pin can support both positive and negative current. The voltage on Terminal W must be between V+ and V-.

If the V+ voltage powers-up before the V_L voltage, the wiper is forced to mid-scale once the Analog POR voltage is crossed.

If the V+ voltage powers-up after the V_L voltage is greater than the Digital POR voltage, the wiper is forced to the value in the wiper register once the Analog POR voltage is crossed.

3.13 Potentiometer Terminal A

The Terminal A pin is connected to the internal potentiometer's Terminal A.

The potentiometer's Terminal A is the fixed connection to the full-scale wiper value of the digital potentiometer. This corresponds to a wiper value of 0xFF for 8-bit devices or 0x7F for 7-bit devices.

The Terminal A pin does not have a polarity relative to the Terminal W or B pins. The Terminal A pin can support both positive and negative current. The voltage on Terminal A must be between V+ and V-.

3.14 Analog Positive Voltage (V+)

The analog circuitry's positive supply voltage. The V+ pin must have a higher potential then the V- pin.

3.15 Exposed Pad (EP)

This pad is only on the bottom of the VQFN packages. This pad is conductively connected to the device substrate. The EP pin must be connected to the V- signal or left floating. This pad could be connected to a Printed Circuit Board (PCB) heat sink to assist as a heat sink for the device.

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4.0 FUNCTIONAL OVERVIEW

This data sheet covers a family of two volatile digital potentiometer devices that will be referred to as MCP41HVX1.

As the **Device Block Diagram** shows, there are six main functional blocks. These are:

- **Operating Voltage Range**
- **POR/BOR Operation**
- **Memory Map**
- **Control Module**
- **Resistor Network**
- **Serial Interface (SPI)**

The POR/BOR operation and the Memory Map are discussed in this section, and the Resistor Network and SPI operation are described in their own sections. The Device Commands are discussed in **Section 7.0 "Device Commands"**.

4.1 Operating Voltage Range

The MCP41HVX1 devices have four voltage signals. These are:

- V+ - Analog power
- V_L - Digital power
- DGND - Digital ground
- V- - Analog ground

Figure 4-1 shows the two possible power-up sequences: analog power rails power-up first, or digital power rails power-up first. The device has been designed so that either power rail may power-up first. The device has a POR circuit for both digital power circuitry and analog power circuitry.

If the V+ voltage powers-up before the V_L voltage, the wiper is forced to mid-scale once the analog POR voltage is crossed.

If the V+ voltage powers-up after the V_L voltage is greater than the digital POR voltage, the wiper is forced to the value in the wiper register once the analog POR voltage is crossed.

Figure 4-2 shows the three cases of the digital power signals (V_L/DGND) with respect to the analog power signals (V+/V-). The device implements level shifts between the digital and analog power systems, which allows the digital interface voltage to be anywhere in the V+/V- voltage window.

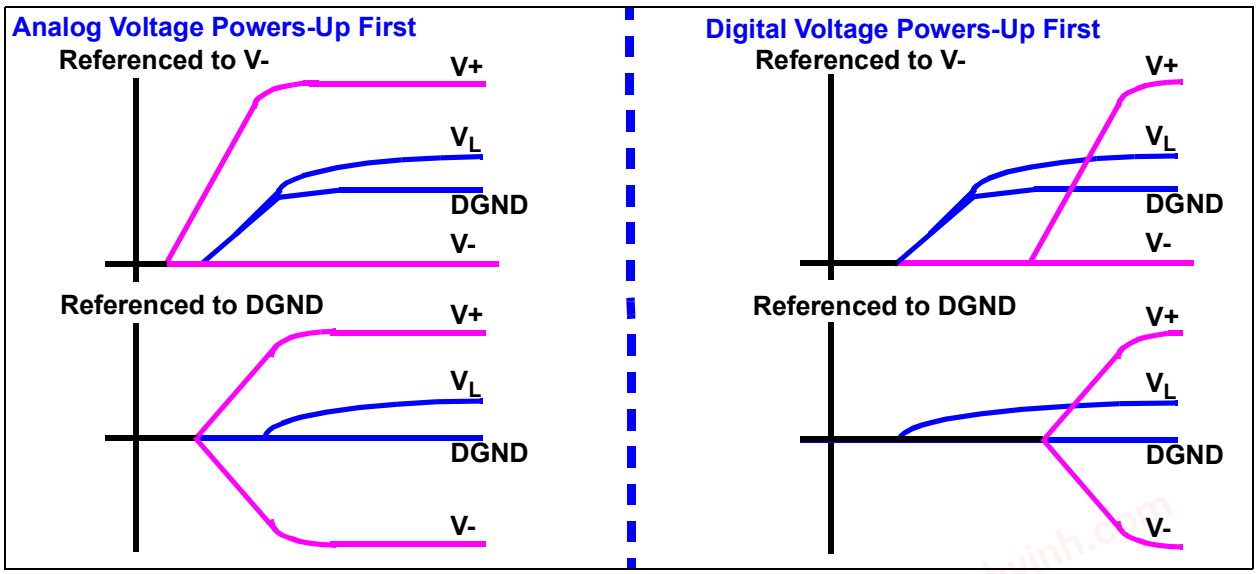


FIGURE 4-1: *Power-On Sequences.*

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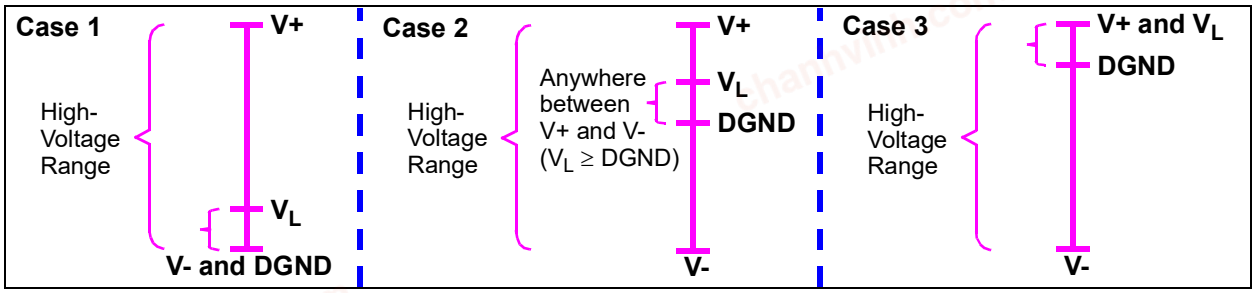


FIGURE 4-2: *Voltage Ranges.*

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4.2 POR/BOR Operation

The resistor network's devices are powered by the analog power signals (V+/V-), but the digital logic (including the wiper registers) is powered by the digital power signals (V_L/DGND). So, both the digital circuitry and analog circuitry have independent POR/BOR circuits.

The wiper position will be forced to the default state when the V+ voltage (relative to V-) is above the analog POR/BOR trip point. The wiper register will be in the default state when the V_L voltage (relative to DGND) is above the digital POR/BOR trip point.

The digital-signal-to-analog-signal voltage level shifters require a minimum voltage between the V_L and V- signals. This voltage requirement is below the operating supply voltage specifications. The wiper output may fluctuate while the V_L voltage is less than the level shifter operating voltage, since the analog values may not reflect the digital value. Output issues may be reduced by powering-up the digital supply voltages to their operating voltage before powering the analog supply voltage.

4.2.1 POWER-ON RESET

Each power system has its own independent Power-on Reset circuitry. This is done so that regardless of the power-up sequencing of the analog and digital power rails, the wiper output will be forced to a default value after minimum conditions are met for either power supply.

Table 4-1 shows the interaction between the analog and digital PORs for the V+ and V_L voltages on the wiper pin state.

TABLE 4-1: WIPER PIN STATE BASED ON POR CONDITIONS

V_L Voltage	V+ Voltage		Comments
	V+ < V_{APOR}	V+ ≥ V_{APOR}	
$V_L < V_{DPOR}$	Unknown	Mid-Scale	
$V_L \geq V_{DPOR}$	Unknown	Wiper Register Value(1)	Wiper Register can be updated

Note 1: The default POR state of the wiper register value is the mid-scale value.

4.2.1.1 Digital Circuitry

A Digital Power-on Reset (DPOR) occurs when the device's V_L signal has power applied (referenced from DGND) and the voltage rises above the trip point. A Brown-out Reset (BOR) occurs when a device has power applied to it, and the voltage drops below the trip point.

The device's RAM retention voltage (V_{RAM}) is lower than the POR/BOR voltage trip point (V_{POR}/V_{BOR}). The maximum V_{POR}/V_{BOR} voltage is less then 1.8V.

When the device powers-up, the device V_L will cross the V_{POR}/V_{BOR} voltage. Once the V_L voltage crosses the V_{POR}/V_{BOR} voltage, the following happens:

- The volatile wiper registers are loaded with the POR/BOR value
- The TCON registers are loaded with the default values
- The device is capable of digital operation

Table 4-2 shows the default POR/BOR wiper register setting selection.

When V_{POR}/V_{BOR} < V_{DD} < 2.7V, the electrical performance may not meet the data sheet specifications. In this region, the device is capable of incrementing, decrementing, reading and writing to its volatile memory if the proper serial command is executed.

TABLE 4-2: DEFAULT POR/BOR WIPER REGISTER SETTING (DIGITAL)

Typical R_{AB} Value	Package Code	Default POR Wiper Register Setting	Device Resolution	Wiper Code
5.0 kΩ	-502	Mid-Scale	8-bit	7Fh
			7-bit	3Fh
10.0 kΩ	-103	Mid-Scale	8-bit	7Fh
			7-bit	3Fh
50.0 kΩ	-503	Mid-Scale	8-bit	7Fh
			7-bit	3Fh
100.0 kΩ	-104	Mid-Scale	8-bit	7Fh
			7-bit	3Fh

Note 1: Register setting independent of analog power voltage.

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4.2.1.2 Analog Circuitry

An Analog Power-on Reset (APOR) occurs when the device's V+ pin voltage has power applied (referenced from V-) and the V+ pin voltage rises above the trip point.

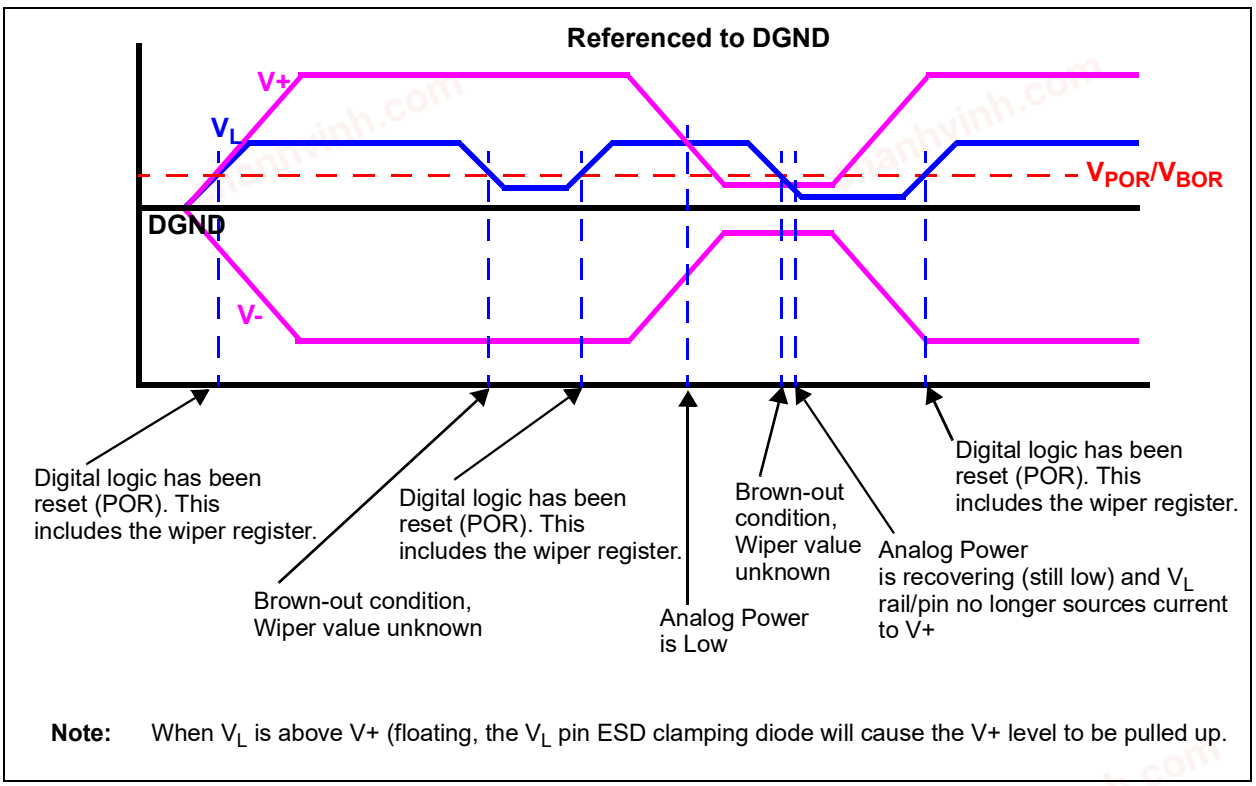
Once the V_L pin voltage exceeds the digital POR trip point voltage, the wiper register will control the wiper setting.

Table 4-3 shows the default POR/BOR Wiper Setting for when the V_L pin is not powered (< digital POR trip point).

TABLE 4-3: DEFAULT POR/BOR WIPER SETTING (ANALOG)

Typical R_{AB} Value	Package Code	Default POR Wiper Setting	Device Resolution
5.0 kΩ	-502	Mid-Scale	8-bit
			7-bit
10.0 kΩ	-103	Mid-Scale	8-bit
			7-bit
50.0 kΩ	-503	Mid-Scale	8-bit
			7-bit
100.0 kΩ	-104	Mid-Scale	8-bit
			7-bit

Note 1: Wiper setting is dependent on the wiper register value if the V_L voltage is greater than the digital POR voltage.



Note: When V_L is above V+ (floating, the V_L pin ESD clamping diode will cause the V+ level to be pulled up.

FIGURE 4-3: *DGND, V_L, V+, and V- Signal Waveform Examples.*

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4.2.2 BROWN-OUT RESET

Each power system has its own independent Brown-out Reset circuitry. This is done so that regardless of the power-down sequencing of the analog and digital power rails, the wiper output will be forced to a default value after the low-voltage conditions are met for either power supply.

Table 4-4 shows the interaction between the analog and digital BORs for the V+ and V_L voltages on the wiper pin state.

TABLE 4-4: WIPER PIN STATE BASED ON BOR CONDITIONS

V_L Voltage	V+ Voltage		Comments
	V+ < V_{ABOR}	V+ ≥ V_{ABOR}	
$V_L < V_{DBOR}$	Unknown	Mid-Scale	
$V_L \geq V_{DBOR}$	Unknown	Wiper register value (1)	Wiper register can be updated

Note 1: The default POR state of the wiper register value is the mid-scale value.

4.2.2.1 Digital Circuitry

When the device's digital power supply powers-down, the device's V_L pin voltage will cross the digital V_{DPOR}/V_{DBOR} voltage.

Once the V_L voltage decreases below the V_{DPOR}/V_{DBOR} voltage, the following happens:

- Serial Interface is disabled

If the V_L voltage decreases below the V_{RAM} voltage, the following happens:

- Volatile wiper registers may become corrupted
- TCON registers may become corrupted

Section 4.2.1 "Power-on Reset" describes what occurs as the voltage recovers above the V_{DPOR}/V_{DBOR} voltage.

Serial commands not completed due to a brown-out condition may cause the memory location to become corrupted.

The brown-out circuit establishes a minimum V_{DBOR} threshold for operation (V_{DBOR} < 1.8V). The digital BOR voltage (V_{DBOR}) is higher than the RAM retention voltage (V_{RAM}) so that as the device voltage crosses the digital BOR threshold, the value that is loaded into the volatile wiper register is not corrupted due to RAM retention issues.

When $V_L < V_{DBOR}$, all communications are ignored and the potentiometer terminals are forced to the analog BOR state.

Whenever V_L transitions from $V_L < V_{DBOR}$ to $V_L > V_{DBOR}$ (a POR event), the wiper's POR/BOR value is latched into the wiper register and the volatile TCON register is forced to the POR/BOR state.

When $1.8V \leq V_L$, the device is capable of digital operation.

Table 4-5 shows the digital potentiometer's level of functionality across the entire V_L range, while Figure 4-4 illustrates the Power-up and Brown-out functionality.

4.2.2.2 Analog Circuitry

An Analog Brown-out Reset (ABOR) occurs when the device's V+ pin has power applied (referenced from V-) and the V+ pin voltage drops below the trip point. In this case, the resistor network terminal pins can become an unknown state.

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TABLE 4-5: DEVICE FUNCTIONALITY AT EACH VL REGION

V_L Level	V+ / V- Level	Serial Interface	Potentiometer Terminals(2)	Wiper		Comment
				Register Setting	Output(2)	
$V_L < V_{DBOR} < 1.8V$	Valid Range	Ignored	"unknown"	Unknown	Invalid	
	Invalid Range	Ignored	"unknown"	Unknown	Invalid	
$V_{DBOR} \leq V_L < 1.8V$	Valid Range	"Unknown"	connected	Volatile wiper Register initialized	Valid	The volatile registers are forced to the POR/BOR state when V_L transitions above the V_{DPOR} trip point
	Invalid Range	"Unknown"	connected		Invalid	
$1.8V \leq V_L \leq 5.5V$	Valid Range	Accepted	connected	Volatile wiper Register determines Wiper Setting	Valid	
	Invalid Range	Accepted	connected		Invalid	

Note 1: For system voltages below the minimum operating voltage, it is recommended to use a voltage supervisor to hold the system in reset. This ensures that MCP41HVX1 commands are not attempted out of the operating range of the device.

2: Assumes that $V+ > V_{APOR}$.

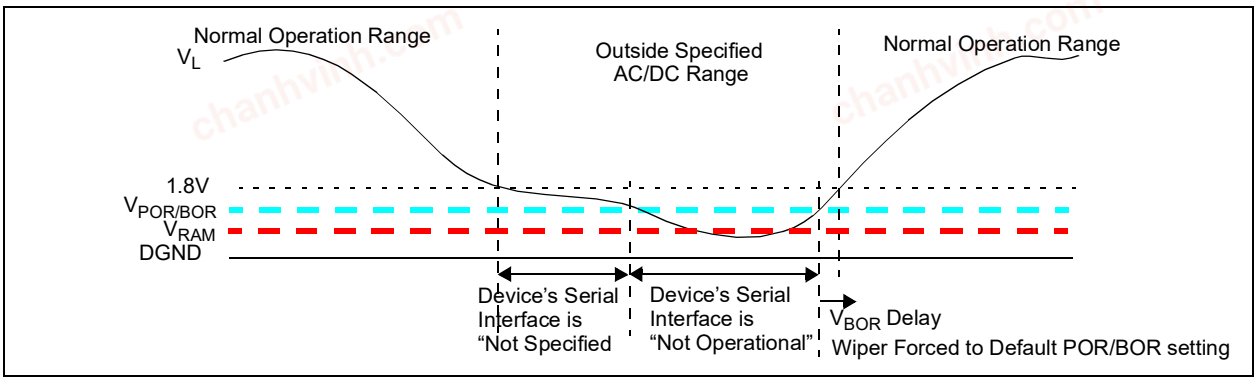


FIGURE 4-4: *Power-up and Brown-out - V+/V- at Normal Operating Voltage.*

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4.3 Control Module

The control module controls the following functionalities:

- **Shutdown**
- **Wiper Latch**

4.3.1 SHUTDOWN

The MCP41HVX1 has two methods to disconnect the terminal's pins (P0A, P0W, and P0B) from the resistor network. These are:

- Hardware Shutdown pin ($\overline{SHDN}$)
- Terminal Control Register (TCON)

4.3.1.1 Hardware Shutdown Pin Operation

The $\overline{SHDN}$ pin has the same functionality as Microchip's family of standard-voltage devices. When the $\overline{SHDN}$ pin is low, the P0A terminal will disconnect (become open) while the P0W terminal simultaneously connects to the P0B terminal (see Figure 4-5).

Note:	When the $\overline{SHDN}$ pin is Active (V_{IL}), the state of the TCON register bits is overridden (ignored). When the state of the $\overline{SHDN}$ pin returns to the Inactive state (V_{IH}), the TCON register bits return to controlling the terminal connection state. This ensures the value in the TCON register is not corrupted

The Hardware Shutdown pin mode does not corrupt the volatile wiper register. When Shutdown is exited, the device returns to the wiper setting specified by the volatile wiper value. See **Section 5.7** for additional description details.

Note:	When the $\overline{SHDN}$ pin is active, the Serial Interface is not disabled and serial interface activity is executed.

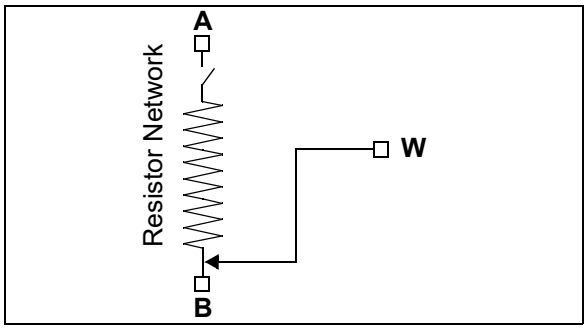


FIGURE 4-5: *Hardware Shutdown Resistor Network Configuration.*

4.3.1.2 Terminal Control Register

The Terminal Control (TCON) register allows the device's terminal pins to be independently removed from the application circuit. These terminal control settings do not modify the wiper setting values. This has no effect on the serial interface, and the memory/wipers are still under full user control.

The resistor network has four TCON bits associated with it: one bit for each terminal (A, W, and B) and one to have a software configuration that matches the configuration of the $\overline{SHDN}$ pin. These bits are named R0A, R0W, R0B and R0HW. Register 4-1 describes the operation of the R0HW, R0A, R0B, and R0W bits.

Note:	When the R0HW bit forces the resistor network into the hardware $\overline{SHDN}$ state, the state of the TCON register R0A, R0W, and R0B bits is overridden (ignored). When the state of the R0HW bit no longer forces the resistor network into the hardware $\overline{SHDN}$ state, the TCON register R0A, R0W, and R0B bits return to controlling the terminal connection state. That is, the R0HW bit does not corrupt the state of the R0A, R0W and R0B bits.

Figure 4-6 shows how the $\overline{SHDN}$ pin signal and the R0HW bit signal interact to control the hardware shutdown of each resistor network (independently).

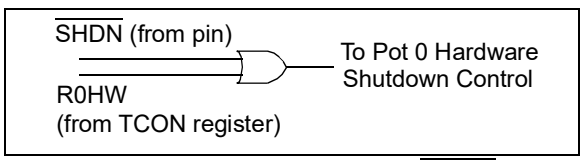


FIGURE 4-6: *R0HW Bit and $\overline{SHDN}$ Pin Interaction.*

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4.3.2 WIPER LATCH

The wiper latch pin is used to control when the new wiper value in the wiper register is transferred to the wiper. This is useful for applications that need to synchronize the wiper updates. This may be for synchronization to an external event, such as zero crossing, or to synchronize the update of multiple digital potentiometers.

When the $\overline{WLAT}$ pin is high, transfers from the wiper register to the wiper are inhibited. When the $\overline{WLAT}$ pin is low, transfers may occur from the Wiper register to the wiper. Figure 4-7 shows the interaction of the $\overline{WLAT}$ pin and the loading of the wiper.

If the external event crossing time is long, then the wiper could be updated the entire time that the $\overline{WLAT}$ signal is low. Once the $\overline{WLAT}$ signal goes high, the transfer from the wiper register is disabled. The wiper register can continue to be updated. Only the $\overline{CS}$ pin is used to enable/disable serial commands.

If the application does not require synchronized wiper register updates, then the $\overline{WLAT}$ pin should be tied low.

Note 1: This feature only inhibits the data transfer from the wiper register to the wiper.

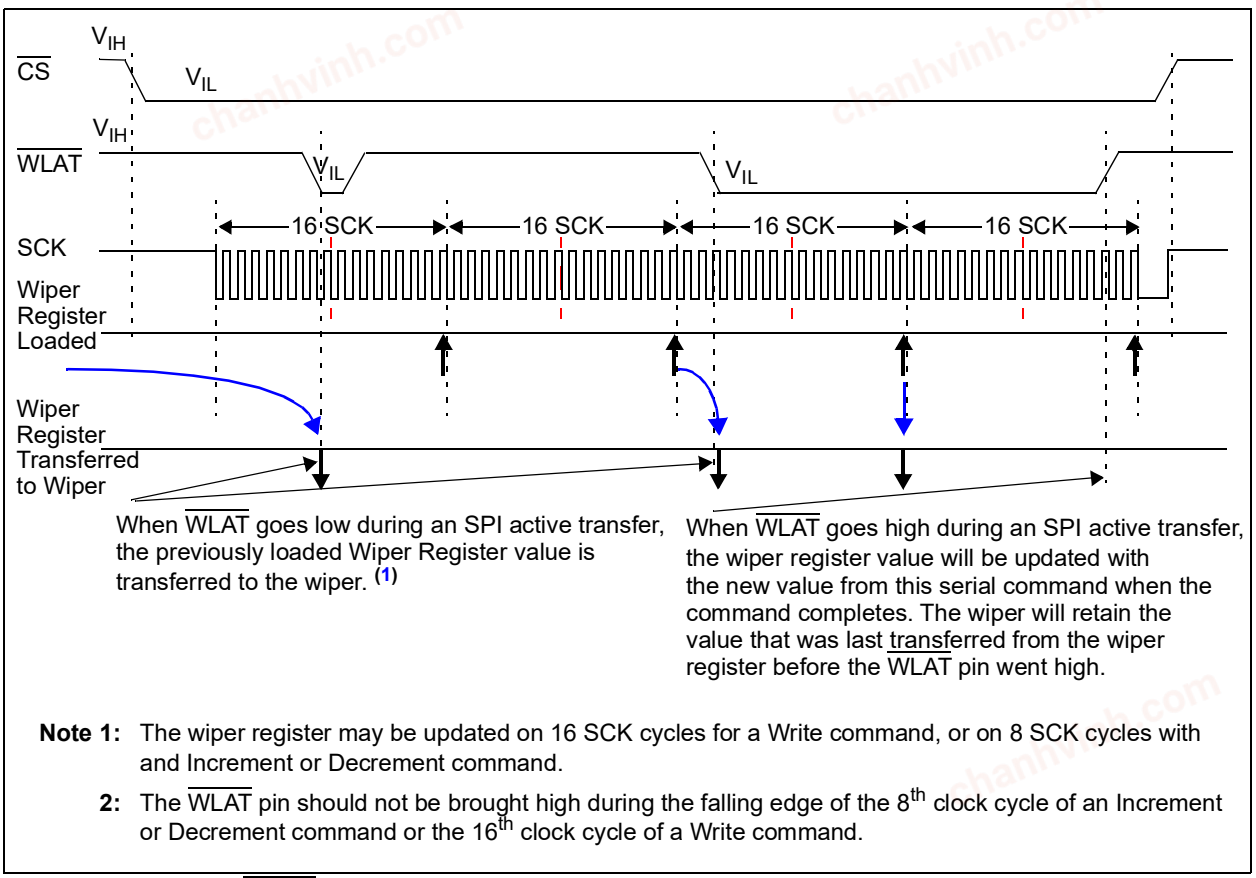
2: When the $\overline{WLAT}$ pin becomes active, data transferred to the wiper will not be corrupted due to the wiper register buffer getting loaded from an active SPI command.

4.3.3 DEVICE CURRENT MODES

There are two current modes for Volatile devices. These are:

- Serial Interface Inactive (Static Operation)
- Serial Interface Active

For the SPI interface, Static Operation occurs when the $\overline{CS}$ pin is at the V_{IH} voltage and the SCK pin is static (high or low).



Note 1: The wiper register may be updated on 16 SCK cycles for a Write command, or on 8 SCK cycles with and Increment or Decrement command.

2: The $\overline{WLAT}$ pin should not be brought high during the falling edge of the 8th clock cycle of an Increment or Decrement command or the 16th clock cycle of a Write command.

FIGURE 4-7: *$\overline{WLAT}$ Interaction with Wiper During Serial Communication – (SPI Mode 1,1).*

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4.4 Memory Map

The device memory supports 16 locations that are eight bits wide (16 x 8 bits). This memory space contains only volatile locations (see Table 4-7).

4.4.1 VOLATILE MEMORY (RAM)

There are two volatile memory locations. These are:

- Volatile Wiper 0
- Terminal Control (TCON0) Register 0

The volatile memory starts functioning at the RAM retention voltage (V_{RAM}). The POR/BOR wiper code is shown in Table 4-6.

Table 4-7 shows this memory map and which serial commands operate (and don't) on each of these locations.

Accessing an "invalid" address (for that device) or an invalid command for that address will cause an error condition (CMDERR) on the serial interface.

TABLE 4-6: WIPER POR STANDARD SETTINGS

Resistance Code	Typical R_{AB} Value	Default POR Wiper Setting	Wiper Code	
			8-bit	7-bit
-502	5.0 kΩ	Mid-Scale	7Fh	3Fh
-103	10.0 kΩ	Mid-Scale	7Fh	3Fh
-503	50.0 kΩ	Mid-Scale	7Fh	3Fh
-104	100.0 kΩ	Mid-Scale	7Fh	3Fh

4.4.1.1 Write to Invalid (Reserved) Addresses

Any write to a reserved address will be ignored and will generate an error condition. To exit the error condition, the user must take the $\overline{CS}$ pin to the V_{IH} level and then back to the active state (V_{IL}).

TABLE 4-7: MEMORY MAP AND THE SUPPORTED COMMANDS

Address	Function	Allowed Commands	Disallowed Commands (1)	Memory Type
00h	Volatile Wiper 0	Read, Write, Increment, Decrement	—	RAM
01h - 03h	Reserved	none	Read, Write, Increment, Decrement	—
04h	Volatile TCON Register	Read, Write	Increment, Decrement	RAM
05h - 0Fh	Reserved	none	Read, Write, Increment, Decrement	—

Note 1: This command on this address will generate an error condition. To exit the error condition, the user must take the $\overline{CS}$ pin to the V_{IH} level and then back to the active state (V_{IL}).

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4.4.1.2 Terminal Control (TCON) Registers

The Terminal Control (TCON) register contains four control bits for Wiper 0. Register 4-1 describes each bit of the TCON register.

The state of each resistor network terminal connection is individually controlled. That is, each terminal connection (A, B and W) can be individually connected/disconnected from the resistor network. This allows the system to minimize the currents through the digital potentiometer.

The value that is written to this register will appear on the resistor network terminals when the serial command has completed.

On a POR/BOR, these registers are loaded with FFh for all terminals connected. The host controller needs to detect the POR/BOR event and then update the volatile TCON register values.

REGISTER 4-1: TCON0 BITS(1)

R-1	R-1	R-1	R-1	R/W-1	R/W-1	R/W-1	R/W-1
D7	D6	D5	D4	R0HW	R0A	R0W	R0B
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **D7-D4:** Reserved. Forced to "1"

bit 3 **R0HW:** Resistor 0 Hardware Configuration Control bit
This bit forces Resistor 0 into the "shutdown" configuration of the Hardware pin
1 = Resistor 0 is **not** forced to the hardware pin "shutdown" configuration
0 = Resistor 0 is forced to the hardware pin "shutdown" configuration

bit 2 **R0A:** Resistor 0 Terminal A (P0A pin) Connect Control bit
This bit connects/disconnects the Resistor 0 Terminal A to the Resistor 0 Network
1 = P0A pin is connected to the Resistor 0 Network
0 = P0A pin is disconnected from the Resistor 0 Network

bit 1 **R0W:** Resistor 0 Wiper (P0W pin) Connect Control bit
This bit connects/disconnects the Resistor 0 Wiper to the Resistor 0 Network
1 = P0W pin is connected to the Resistor 0 Network
0 = P0W pin is disconnected from the Resistor 0 Network

bit 0 **R0B:** Resistor 0 Terminal B (P0B pin) Connect Control bit
This bit connects/disconnects the Resistor 0 Terminal B to the Resistor 0 Network
1 = P0B pin is connected to the Resistor 0 Network
0 = P0B pin is disconnected from the Resistor 0 Network

Note 1: These bits do not affect the wiper register values.

2: The hardware $\overline{\text{SHDN}}$ pin (when active) overrides the state of these bits. When the $\overline{\text{SHDN}}$ pin returns to the inactive state, the TCON register will control the state of the terminals. The $\overline{\text{SHDN}}$ pin does not modify the state of the TCON bits.

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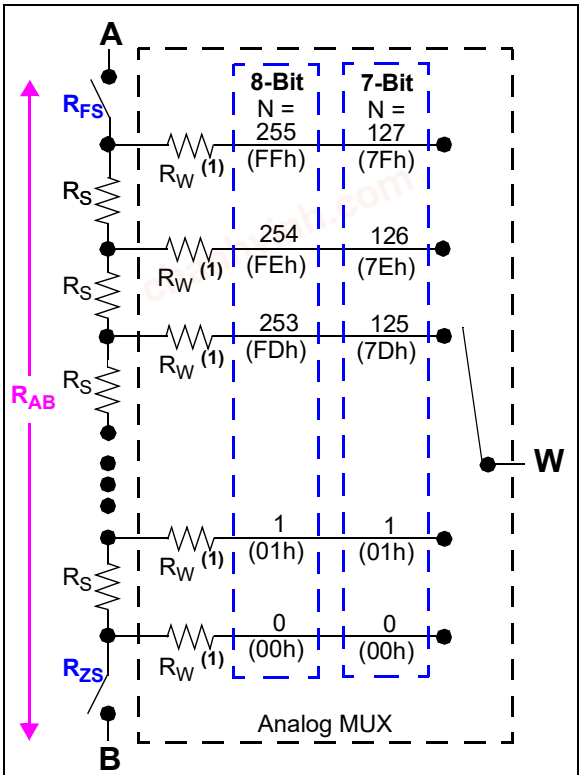
5.0 RESISTOR NETWORK

The resistor network has either 7-bit or 8-bit resolution. Each resistor network allows zero-scale to full-scale connections. Figure 5-1 shows a block diagram for the resistive network of a device. The resistor network has up to three external connections. These are referred to as Terminal A, Terminal B, and the wiper (or Terminal W).

The resistor network is made up of several parts. These include:

- **Resistor Ladder Module**
- **Wiper**
- **Shutdown Control** (Terminal Connections)

Terminals A and B as well as the wiper W do not have a polarity. These terminals can support both positive and negative current.



Note 1: The wiper resistance is dependent on several factors, including wiper code, device V+ voltage, terminal voltages (on A, B and W) and temperature.
Also, for the same conditions, each tap selection resistance has a small variation. This R_W variation has a greater effect on some specifications (such as INL) for the smaller resistance devices (5.0 kΩ) compared to larger resistance devices (100.0 kΩ).

FIGURE 5-1: *Resistor Block Diagram.*

5.1 Resistor Ladder Module

The R_{AB} resistor ladder is composed of the series of equal value Step resistors (R_S) and the Full-Scale (R_{FS}) and Zero-Scale (R_{ZS}) resistances:

$$R_{AB} = R_{ZS} + n \times R_S + R_{FS}$$

Where "n" is determined by the resolution of the device. The R_{FS} and R_{ZS} resistances are discussed in **Section 5.1.3 "RFS and RZS Resistors"**.

There is a connection point (tap) between each R_S resistor. Each tap point is a connection point for an analog switch. The opposite side of the analog switch is connected to a common signal which is connected to the Terminal W (Wiper) pin (see **Section 5.2 "Wiper"**).

Figure 5-1 shows a block diagram of the Resistor Network. The R_{AB} (and R_S) resistance has small variations over voltage and temperature.

The end points of the resistor ladder are connected to analog switches, which are connected to the device Terminal A and Terminal B pins. In the ideal case, these switches would have 0Ω of resistance, that is $R_{FS} = R_{ZS} = 0\Omega$. This will also be referred as the Simplified model.

For an 8-bit device, there are 255 resistors in a string between Terminal A and Terminal B. The wiper can be set to tap onto any of these 255 resistors, thus providing 256 possible settings (including Terminal A and Terminal B). A wiper setting of 00h connects Terminal W (wiper) to Terminal B (Zero-Scale). A wiper setting of 7Fh is the Mid-Scale setting. A wiper setting of FFh connects Terminal W (wiper) to Terminal A (Full-Scale). Table 5-2 illustrates the full wiper setting map.

For a 7-bit device, there are 127 resistors in a string between Terminal A and Terminal B. The wiper can be set to tap onto any of these 127 resistors, thus providing 128 possible settings (including Terminal A and Terminal B). A wiper setting of 00h connects Terminal W (wiper) to Terminal B (Zero-Scale). A wiper setting of 3Fh is the Mid-scale setting. A wiper setting of 7Fh connects the wiper to Terminal A (Full-Scale). Table 5-2 illustrates the full wiper setting map.

5.1.1 R_{AB} CURRENT (I_{RAB})

The current through the R_{AB} resistor (A pin to B pin) is dependent on the voltage on the V_A and V_B pins and the R_{AB} resistance, as shown in Equation 5-1.

EQUATION 5-1: R_{AB}

$$R_{AB} = R_{ZS} + (n \times R_S) + R_{FS} = \frac{|(V_A - V_B)|}{(I_{RAB})}$$

Where:

V_A = the voltage on the V_A pin
V_B = the voltage on the V_B pin
I_{RAB} = the current into the V_{REF} pin

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5.1.2 STEP RESISTANCE (R_S)

Step resistance (R_S) is the resistance from one tap setting to the next. This value will be dependent on the R_{AB} value that has been selected (and the full-scale and zero-scale resistances). The R_S resistors are manufactured so that they should be very consistent with each other and track each other's values as voltage and/or temperature change.

Equation 5-2 shows the simplified and detailed equations for calculating the R_S value. The simplified equation assumes $R_{FS} = R_{ZS} = 0\Omega$. Table 5-1 shows example step resistance calculations for each device, and the variation of the detailed model ($R_{FS} \neq 0\Omega$; $R_{ZS} \neq 0\Omega$) from the simplified model ($R_{FS} = R_{ZS} = 0\Omega$). As the R_{AB} resistance option increases, the effects of the R_{ZS} and R_{FS} resistances decrease.

The total resistance of the device has minimal variation due to operating voltage (see device characterization graphs).

Equation 5-2 shows calculations for the step resistance.

EQUATION 5-2: R_S CALCULATION

Simplified Model (assumes $R_{FS} = R_{ZS} = 0\Omega$)

$$R_{AB} = (n \times R_S)$$

$$R_S = \frac{R_{AB}}{n}$$

8-bit

$$R_S = \frac{R_{AB}}{255}$$

7-bit

$$R_S = \frac{R_{AB}}{127}$$

Detailed Model

$$R_{AB} = R_{FS} + (n \times R_S) + R_{ZS}$$

$$R_S = \frac{R_{AB} - R_{FS} - R_{ZS}}{n}$$

or

$$R_S = \frac{\frac{(V_{FS} - V_{ZS})}{n}}{I_{AB}}$$

Where:

"n" = 255 (8-bit) or 127 (7-bit)
V_{FS} = Wiper voltage at Full-Scale code
V_{ZS} = Wiper voltage at Zero-Scale code
I_{AB} = Current between Terminal A and Terminal B

TABLE 5-1: EXAMPLE STEP RESISTANCES (R_S) CALCULATIONS

Example Resistance (Ω)					Variation%(1)	Resolution	Comment
R_{AB}	R_{ZS}(3)	R_{FS}(3)	R_S				
			Equation	Value			
5,000	0	0	5,000/127	39.37	0	7-bit (127 R_S)	Simplified Model(2)
	80	60	4,860/127	38.27	-2.80		
	0	0	5,000/255	19.61	0	8-bit (255 R_S)	Simplified Model(2)
	80	60	4,860/255	19.06	-2.80		
10,000	0	0	10,000/127	78.74	0	7-bit (127 R_S)	Simplified Model(2)
	80	60	9,860/127	77.64	-1.40		
	0	0	10,000/255	39.22	0	8-bit (255 R_S)	Simplified Model (2)
	80	60	9,860/255	38.67	-1.40		
50,000	0	0	50,000/127	393.70	0	7-bit (127 R_S)	Simplified Model(2)
	80	60	49,860/127	392.60	-0.28		
	0	0	50,000/255	196.08	0	8-bit (255 R_S)	Simplified Model(2)
	80	60	49,860/255	195.53	-0.28		
100,000	0	0	100,000/127	787.40	0	7-bit (127 R_S)	Simplified Model(2)
	80	60	99,860/127	786.30	-0.14		
	0	0	100,000/255	392.16	0	8-bit (255 R_S)	Simplified Model(2)
	80	60	99,860/255	391.61	-0.14		

Note 1: Delta % from Simplified Model R_S calculation value:

2: Assumes $R_{FS} = R_{ZS} = 0\Omega$.

3: Zero-Scale (R_{ZS}) and Full-Scale (R_{FS}) resistances are dependent on many operational characteristics of the device, including the V+ / V- voltage, the voltages on the A, B and W terminals, the wiper code selected, the R_{AB} resistance and the temperature of the device.

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5.1.3 R_{FS} AND R_{ZS} RESISTORS

The R_{FS} and R_{ZS} resistances are artifacts of the R_{AB} resistor network implementation. In the ideal model, the R_{FS} and R_{ZS} resistances would be 0Ω. These resistors are included in the block diagram to help better model the actual device operation. Equation 5-3 shows how to estimate the R_S, R_{FS}, and R_{ZS} resistances based on the measured voltages of V_{REF}, V_{FS}, V_{ZS} and the measured current I_{VREF}.

EQUATION 5-3: ESTIMATING R_S, R_{FS} AND R_{ZS}

$$R_{FS} = \frac{|(V_A - V_{FS})|}{(I_{RAB})}$$

$$R_{ZS} = \frac{|(V_{ZS} - V_B)|}{(I_{RAB})}$$

$$R_S = \frac{V_S}{(I_{RAB})}$$

Where:

$$V_S = \frac{(V_{FS} - V_{ZS})}{255} \quad \text{(8-bit device)}$$

$$V_S = \frac{(V_{FS} - V_{ZS})}{127} \quad \text{(7-bit device)}$$

V_{FS} = V_W voltage when the wiper code is at full-scale

V_{ZS} = V_W voltage when the wiper code is at zero-scale

5.2 Wiper

The wiper terminal is connected to an analog switch MUX, where one side of all the analog switches are connected together via the W terminal. The other side of each analog switch is connected to one of the taps of the R_{AB} resistor string (see Figure 5-1).

The value in the volatile wiper register selects which analog switch to close, connecting the W terminal to the selected node of the resistor ladder. The wiper register is eight bits wide, and Table 5-2 shows the wiper value state for both 7-bit and 8-bit devices.

The wiper resistance (R_W) is the resistance of the selected analog switch in the analog MUX. This resistance is dependent on many operational characteristics of the device, including the V+/V- voltage, the voltages on the A, B and W terminals, the wiper code selected, the R_{AB} resistance and the temperature of the device.

When the wiper value is at zero-scale (00h), the wiper is connected closest to the B terminal. When the wiper value is at full-scale (FFh for 8-bit, 7Fh for 7-bit), the wiper is connected closest to the A terminal.

A zero-scale wiper value connects the W terminal (wiper) to the B terminal (wiper = 00h). A full-scale wiper value connects the W terminal (wiper) to the A terminal (wiper = FFh (8-bit), or wiper = 7Fh (7-bit)). In these configurations, the only resistance between Terminal W and the other terminal (A or B) is that of the analog switches.

TABLE 5-2: VOLATILE WIPER VALUE VS. WIPER POSITION

Wiper Setting		Properties
7-bit	8-bit	
7Fh	FFh	Full-Scale (W = A), Increment commands ignored
7Eh - 40h	FEh - 80h	W = N
3Fh	7Fh	W = N (Mid-Scale)
3Eh - 01h	7Eh - 01h	W = N
00h	00h	Zero-Scale (W = B) Decrement command ignored

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5.2.1 WIPER RESISTANCE (R_W)

Wiper resistance is significantly dependent on:

- The resistor network's supply voltage (V_{RN})
- The resistor network's terminal (A, B, and W) voltages
- Switch leakage (occurs at higher temperatures)
- I_W current

Figure 5-2 shows the wiper resistance characterization data for all four R_{AB} resistances and temperatures. Each R_{AB} resistance determined the maximum wiper current based on worst-case conditions $R_{AB} = R_{AB}$ maximum and at full-scale code, V_{BW} ~= V+ (but not exceeding V+). The V+ targets were 10V, 20V, and 36V. What this graph shows is that at higher R_{AB} resistances (50 kΩ and 100 kΩ) and at the highest temperature (+125°C), the analog switch leakage causes an increase in the measured result of R_W, where R_W is measured in a rheostat configuration with $R_W = (V_{BW} - V_{BA})/I_{BW}$.

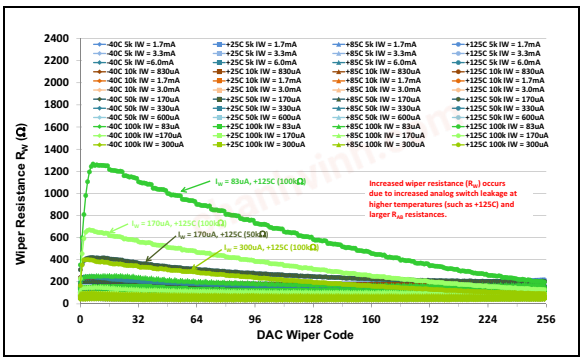


FIGURE 5-2: *R_W Resistance Vs. R_{AB}, Wiper Current (I_W), Temperature and Wiper Code.*

Since there is minimal variation of the total device resistance (R_{AB}) over voltage, at a constant temperature (see device characterization graphs), the change in wiper resistance over voltage can have a significant impact on the R_{INL} and R_{DNL} errors.

5.2.2 POTENTIOMETER CONFIGURATION

In a potentiometer configuration, the wiper resistance variation does not affect the output voltage seen on the W pin, and therefore is not a significant source of error.

5.2.3 RHEOSTAT CONFIGURATION

In a rheostat configuration, the wiper resistance variation creates nonlinearity in the R_{BW} (or R_{AW}) value. The lower the nominal resistance (R_{AB}), the greater the possible relative error. Also, a change in voltage needs to be taken into account. For the 5.0 kΩ device, the maximum wiper resistance at 5.5V is approximately 6% of the total resistance, while at 2.7V it is approximately 6.5% of the total resistance.

5.2.4 LEVEL SHIFTERS (DIGITAL-TO-ANALOG)

Since the digital logic may operate anywhere within the analog power range, level shifters are present so that the digital signals control the analog circuitry. This level shifter logic is relative to the V- and V_L voltages. A delta voltage of 2.7V between V_L and V- is required for the serial interface to operate at the maximum specified frequency.

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5.3 Terminal Currents

The terminal currents are limited by several factors, including the R_{AB} resistance (R_S resistance). The maximum current occurs when the wiper is at either the zero-scale (I_{BW}) or full-scale (I_{AW}) code. In this case, the current is only going through the analog switches (see I_T specification in **Section 1.0 "Electrical Characteristics"**). When the current passes through at least one R_S resistive element, then the maximum terminal current (I_T) has a different limit. The current through the R_{AB} resistor is limited by the R_{AB} resistance. The worst case (max current) occurs when the resistance is at the minimum R_{AB} value.

Higher current capabilities allow a greater delta voltage between the desired terminals for a given resistance. This also allows a more usable range of wiper code values without violating the maximum terminal current specification. Table 5-3 shows resistance and current calculations based on the R_{AB} resistance (R_S resistance) for a system that supports ± 18V (Δ 36V). In Rheostat configuration, the minimum wiper-code value is shown (for V_{BW} = 36V). As the V_{BW} voltage decreases, the minimum wiper-code value also decreases. Using a wiper code less then this value will cause the maximum terminal current (I_T) specification to be violated.

Note:	For high terminal-current applications, it is recommended that proper PCB layout techniques be used to address the thermal implications of this high current. The VQFN package has better thermal properties than the TSSOP package.

TABLE 5-3: TERMINAL (WIPER) CURRENT AND WIPER SETTINGS ($R_W = R_{FS} = R_{ZS} = 0\Omega$)

R_{AB} Resistance (Ω)			$R_{S(MIN)}$ (Ω)		$I_{AB(MAX)}$ (mA) (= 36V/$R_{AB(MIN)}$) (1)	I_T (A, B, or W (I_W)) (mA) ($I_{BW(W=ZS)}$, $I_{AW(W=FS)}$) (1)	R_{BW} (Ω) (= 36V/$I_{T(MAX)}$) (2)	Rheostat Min 'N' when V_{BW} = 36V N * $R_{S(MIN)}$ * 36V ≤ I_T (mA) (3)		Rheostat $V_{BW(MAX)}$ When Wiper = 01h (V) (= $I_{T(MAX)}$ * $R_{S(MIN)}$)	
Typical	**Min.**	**Max.**	**8-bit**	**7-bit**				**8-bit**	**7-bit**	**8-bit**	**7-bit**
5,000	4,000	6,000	15.686	31.496	9.00	25.0	1,440	91	45	0.392	0.787
10,000	8,000	12,000	31.373	62.992	4.50	12.5	2,880	91	45	0.392	0.787
50,000	40,000	60,000	156.863	314.961	0.90	6.5	5539	35	17	1.020	2.047
100,000	80,000	120,000	313.725	629.9	0.45	6.5	5539	17	8	2.039	4.094

Note 1: I_{BW} or I_{AW} currents can be much higher than this depending on the voltage differential between Terminal B and Terminal W or Terminal A and Terminal W.

2: Any R_{BW} resistance greater than this limits the current.

3: If V_{BW} = 36V, then the wiper code value must be greater than or equal to Min 'N'. Wiper codes less than Min 'N' will cause the wiper current (I_W) to exceed the specification. Wiper codes greater than Min 'N' will cause the wiper current to be less than the maximum. The Min 'N' number has been rounded up from the calculated number to ensure that the wiper current does not exceed the maximum specification.

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Figures 5-3 through 5-6 show graphs of the calculated currents (minimum, typical, and maximum) for each resistor option. These graphs are based on 25 mA (5 kΩ), 12.5 mA (10 kΩ), and 6.5 mA (50 kΩ and 100 kΩ) specifications.

To ensure no damage to the resistor network (including long-term reliability) the maximum terminal current must not be exceeded. This means that the application must assume that the R_{AB} resistance is the minimum R_{AB} value ($R_{AB(MIN)}$, see blue lines in graphs).

Looking at the 50 kΩ device, the maximum terminal current is 6.5 mA. That means that any wiper code value greater than 36 ensures that the terminal current is less than 6.5 mA. This is ~14% of the full-scale value. If the application could change to the 100 kΩ device, which has the same maximum terminal current specification, any wiper-code value greater than 18 ensures that the terminal current is less than 6.5 mA. This is ~7% of the full-scale value. Supporting higher terminal current allows a greater wiper code range for a given V_{BW} voltage.

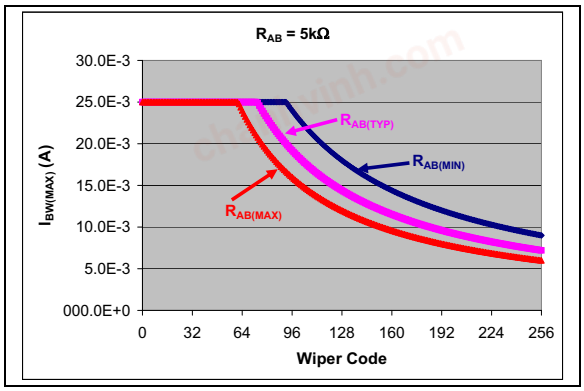


FIGURE 5-3: *Maximum I_{BW} Vs. Wiper Code – 5 kΩ..*

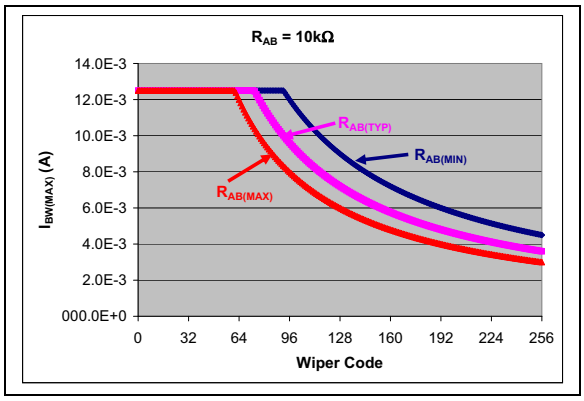


FIGURE 5-4: *Maximum I_{BW} Vs. Wiper Code – 10 kΩ.*

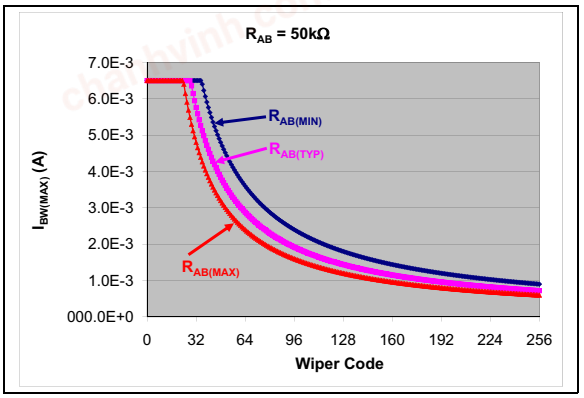


FIGURE 5-5: *Maximum I_{BW} Vs. Wiper Code – 50 kΩ.*

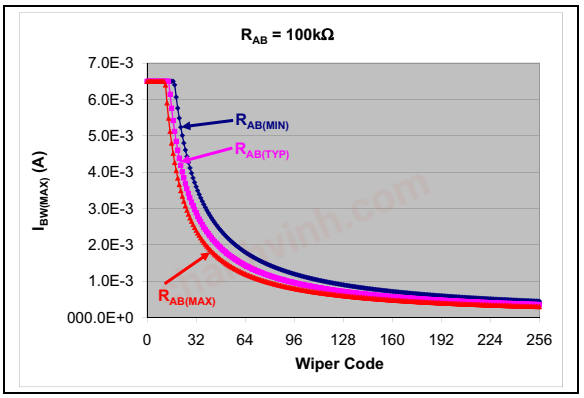


FIGURE 5-6: *Maximum I_{BW} Vs. Wiper Code – 100 kΩ.*

Figure 5-7 shows a graph of the maximum V_{BW} voltage versus wiper code (for 5 kΩ and 10 kΩ devices). To ensure that no damage is done to the resistor network, the $R_{AB(MIN)}$ resistance (blue line) should be used to determine V_{BW} voltages for the circuit. Devices where the R_{AB} resistance is greater than the $R_{AB(MIN)}$ resistance will naturally support a higher voltage limit.

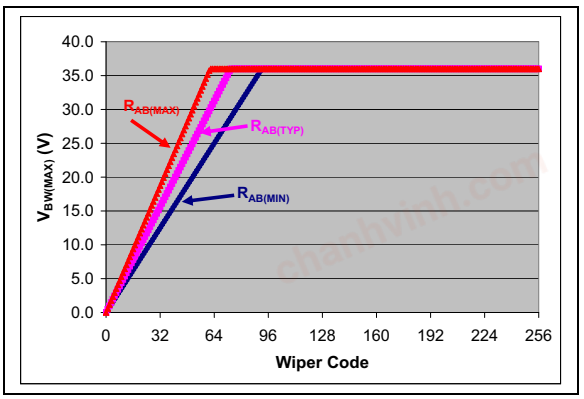


FIGURE 5-7: *Maximum V_{BW} Vs. Wiper Code (5 kΩ and 10 kΩ devices).*

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Table 5-4 shows the maximum V_{BW} voltage that can be applied across the Terminal B to Terminal W pins for a given wiper-code value (for the 5 kΩ and 10 kΩ devices). These calculations assume the ideal model ($R_W = R_{FS} = R_{ZS} = 0\Omega$) and show the calculations based on $R_{S(MIN)}$ and $R_{S(MAX)}$. Table 5-5 shows the same calculations for the 50 kΩ devices, and Table 5-6 shows the calculations for the 100 kΩ devices. These tables are supplied as a quick reference.

TABLE 5-4: MAX V_{BW} AT EACH WIPER CODE ($R_W = R_{FS} = R_{ZS} = 0\Omega$) FOR V+ – V- = 36V, 5 KΩ AND 10 KΩ DEVICES

Code		$V_{BW(MAX)}$		Code		$V_{BW(MAX)}$		Code		$V_{BW(MAX)}$	
Hex.	Dec.	$R_{S(MIN)}$	$R_{S(MAX)}$	Hex.	Dec.	$R_{S(MIN)}$	$R_{S(MAX)}$	Hex.	Dec.	$R_{S(MIN)}$	$R_{S(MAX)}$
00h	0	0.000	0.000	20h	32	12.549	18.824	40h	64	25.098	
01h	1	0.392	0.588	21h	33	12.941	19.412	41h	65	25.490	
02h	2	0.784	1.176	22h	34	13.333	20.000	42h	66	25.882	
03h	3	1.176	1.765	23h	35	13.725	20.588	43h	67	25.275	
04h	4	1.569	2.353	24h	36	14.118	21.176	44h	68	26.667	
05h	5	1.961	2.941	25h	37	14.510	21.765	45h	69	27.059	
06h	6	2.353	3.529	26h	38	14.902	22.353	46h	70	27.451	
07h	7	2.745	4.118	27h	39	15.294	22.941	47h	71	27.843	
08h	8	3.137	4.706	28h	40	15.686	23.529	48h	72	28.235	
09h	9	3.529	5.294	29h	41	16.078	24.118	49h	73	28.627	
0Ah	10	3.922	5.882	2Ah	42	16.471	24.706	4Ah	74	29.020	
0Bh	11	4.314	6.471	2Bh	43	16.863	25.294	4Bh	75	29.412	
0Ch	12	4.706	7.059	2Ch	44	17.255	25.882	4Ch	76	29.804	
0Dh	13	5.098	7.647	2Dh	45	17.647	26.471	4Dh	77	30.196	
0Eh	14	5.490	8.235	2Eh	46	18.039	27.059	4Eh	78	30.588	
0Fh	15	5.882	8.824	2Fh	47	18.431	27.647	4Fh	79	30.980	
10h	16	5.275	9.412	30h	48	18.824	28.235	50h	80	31.373	
11h	17	6.667	10.000	31h	49	19.216	28.824	51h	81	31.765	
12h	18	7.059	10.588	32h	50	19.608	29.412	52h	82	32.157	
13h	19	7.451	11.176	33h	51	20.000	30.000	53h	83	32.549	
14h	20	7.843	11.765	34h	52	20.392	30.588	54h	84	32.941	
15h	21	8.235	12.353	35h	53	20.784	31.176	55h	85	33.333	
16h	22	8.627	12.941	36h	54	21.176	31.765	56h	86	33.725	
17h	23	9.020	13.529	37h	55	21.569	32.353	57h	87	34.118	
18h	24	9.412	14.118	38h	56	21.961	32.941	58h	88	34.510	
19h	25	9.804	14.706	39h	57	22.353	33.529	59h	89	34.902	
1Ah	26	10.196	15.294	3Ah	58	22.745	34.118	5Ah	90	35.294	
1Bh	27	10.588	15.882	3Bh	59	23.137	34.706	5Bh	91	35.686	
1Ch	28	10.980	16.471	3Ch	60	23.529	35.294	5Ch	92 - 255	36.0 (1, 2)	
1Dh	29	11.373	17.059	3Dh	61	23.922	35.882				
1Eh	30	11.765	17.647	3Eh	62	24.314	36.0 (1, 2)				
1Fh	31	12.157	18.235	3Fh	63	24.706					

Note 1: Calculated R_{BW} voltage is greater than 36V (highlighted in color), must be limited to 36V (V+ - V-).

2: This wiper code and greater will limit the I_{BW} current to less than the maximum supported terminal current (I_T).

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TABLE 5-5: MAX VBW AT EACH WIPER CODE ($R_W = R_{FS} = R_{ZS} = 0\Omega$) FOR V+ - V- = 36V, 50 KΩ DEVICES

Code		$V_{BW(MAX)}$		Code		$V_{BW(MAX)}$		Code		$V_{BW(MAX)}$	
Hex.	Dec.	$R_{S(MIN)}$	$R_{S(MAX)}$	Hex.	Dec.	$R_{S(MIN)}$	$R_{S(MAX)}$	Hex.	Dec.	$R_{S(MIN)}$	$R_{S(MAX)}$
00h	0	0.000	0.000	10h	16	16.314	24.471	20h	32	32.627	
01h	1	1.020	1.529	11h	17	17.333	26.000	21h	33	33.647	
02h	2	2.039	3.059	12h	18	18.353	27.529	22h	34	34.667	
03h	3	3.059	4.588	13h	19	19.373	29.059	23h	35	35.686	
04h	4	4.078	6.118	14h	20	20.392	30.588	24h - FFh	36 - 255	36.0(1, 2)	
05h	5	5.098	7.647	15h	21	21.412	32.118				
06h	6	6.118	9.176	16h	22	22.431	33.647				
07h	7	7.137	10.706	17h	23	23.451	35.176				
08h	8	8.157	12.235	18h	24	24.471	36.0(1, 2)				
09h	9	9.176	13.765	19h	25	25.490					
0Ah	10	10.196	15.294	1Ah	26	26.510					
0Bh	11	11.216	16.824	1Bh	27	27.529					
0Ch	12	12.235	18.353	1Ch	28	28.549					
0Dh	13	13.255	19.882	1Dh	29	29.569					
0Eh	14	14.275	21.412	1Eh	30	30.588					
0Fh	15	15.294	22.941	1Fh	31	31.608					

Note 1: Calculated R_{BW} voltage is greater than 36V (highlighted in color), must be limited to 36V (V+ - V-).
2: This wiper code and greater will limit the I_{BW} current to less than the maximum supported terminal current (I_T).

TABLE 5-6: MAX VBW AT EACH WIPER CODE ($R_W = R_{FS} = R_{ZS} = 0\Omega$) FOR V+ - V- = 36V, 100 KΩ DEVICES

Code		$V_{BW(MAX)}$		Code		$V_{BW(MAX)}$	
Hex.	Dec.	$R_{S(MIN)}$	$R_{S(MAX)}$	Hex.	Dec.	$R_{S(MIN)}$	$R_{S(MAX)}$
00h	0	0.000	0.000	10h	16	32.627	
01h	1	2.039	3.059	11h	17	34.667	
02h	2	4.078	6.118	12h - FFh	18 - 255	36.0(1, 2)	
03h	3	6.118	9.176				
04h	4	8.157	12.235				
05h	5	10.196	15.294				
06h	6	12.235	18.353				
07h	7	14.275	21.412				
08h	8	16.314	24.471				
09h	9	18.353	27.529				
0Ah	10	20.392	30.588				
0Bh	11	22.431	33.647				
0Ch	12	24.471	36.0(1, 2)				
0Dh	13	26.510					
0Eh	14	28.549					
0Fh	15	30.588					

Note 1: Calculated R_{BW} voltage is greater than 36V (highlighted in color), must be limited to 36V (V+ - V-).
2: This wiper code and greater will limit the I_{BW} current to less than the maximum supported terminal current (I_T).

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5.4 Variable Resistor (Rheostat)

A variable resistor is created using Terminal W and either Terminal A or Terminal B. Since the wiper-code value of 0 connects the wiper to Terminal B, the R_{BW} resistance increases with increasing wiper-code value. Conversely, the R_{AW} resistance will decrease with increasing wiper-code value. Figure 5-8 shows the connections from a potentiometer to create a rheostat configuration.

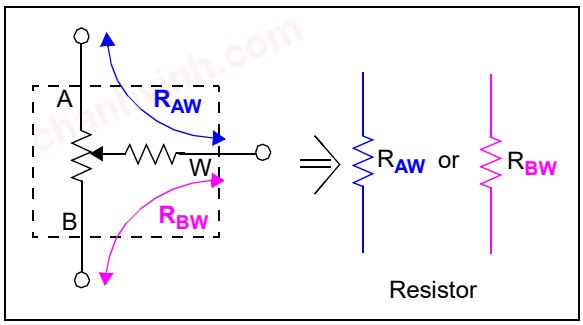


FIGURE 5-8: *Rheostat Configuration.*

Equation 5-4 shows the R_{BW} and R_{AW} calculations. The R_{BW} calculation is for the resistance between the wiper and Terminal B. The R_{AW} calculation is for the resistance between the wiper and Terminal A.

EQUATION 5-4: R_{BW} AND R_{AW} CALCULATION

Simplified Model (assumes $R_{FS} = R_{ZS} = 0\Omega$)

$$R_{BW} = (n \times R_S)$$

$$R_{AW} = ((FSV - n) \times R_S)$$

Where:

$$R_S = \frac{R_{AB}}{Resolution}$$

8-bit	7-bit
$R_S = \frac{R_{AB}}{255}$	$R_S = \frac{R_{AB}}{127}$

n = Wiper code

FSV = Full-scale value
(255 for 8-bit or 127 for 7-bit)

Detailed Model

$$R_{BW} = R_{ZS} + (n \times R_S)$$

$$R_{AW} = R_{FS} + ((FSV - n) \times R_S)$$

Where

n = Wiper code

FSV = The full-scale value
(255 for 8-bit or 127 for 7-bit)

5.5 Analog Circuitry Power Requirements

This device has two power supplies. One is for the digital interface (VL and DGND) and the other is for the high-voltage analog circuitry (V+ and V-). The maximum delta voltage between V+ and V- is 36V. The digital power signals must be between V+ and V-.

If the digital ground (DGND) pin is at half the potential of V+ (relative to V-), then the terminal pins' potentials can be ±(V+/2) relative to DGND.

Figure 5-9 shows the relationship of the four power signals. This shows that the V+/V- signals do not need to be symmetric around the DGND signal.

To ensure that the wiper register has been properly loaded with the POR/BOR value, the V_L voltage must be at the minimum specified operating voltage (referenced to DGND).

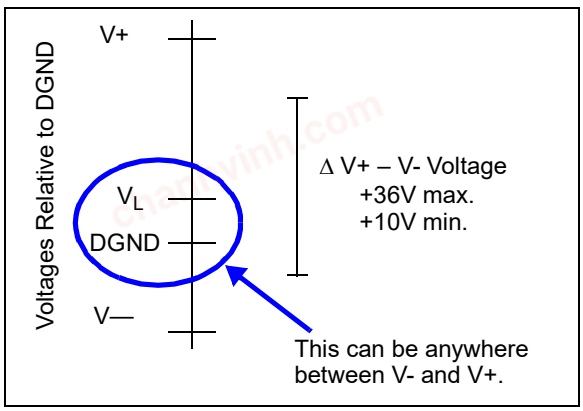


FIGURE 5-9: *Analog Circuitry Voltage Ranges.*

5.6 Resistor Characteristics

5.6.1 V+/V- LOW-VOLTAGE OPERATION

The resistor network is specified from 20V to 36V. At voltages below 20V, the resistor network will function, but the operational characteristics may be outside the specified limits. Please refer to **Section 2.0 "Typical Performance Curves"** for additional information.

5.6.2 RESISTOR TEMPCO

Biasing the ends (Terminal A and Terminal B) near mid-supply ((V+ - |V-|)/2) will give the worst switch resistance temperature coefficient.

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5.7 Shutdown Control

Shutdown is used to minimize the device's current consumption. The MCP41HVX1 has two methods to achieve this:

- **Hardware Shutdown Pin (SHDN)**
- **Terminal Control Register (TCON)**

The Hardware Shutdown pin is backwards compatible with the MCP42X1 devices.

5.7.1 HARDWARE SHUTDOWN PIN ($\overline{SHDN}$)

The $\overline{SHDN}$ pin is available on the potentiometer devices. When the $\overline{SHDN}$ pin is forced active (V_{IL}):

- The P0A terminal is disconnected
- The P0W terminal is connected to the P0B terminal (see Figure 4-5)
- The Serial Interface is NOT disabled, and all Serial Interface activity is executed

The Hardware Shutdown pin mode does **not** corrupt the values in the Volatile Wiper Registers nor the TCON register. When the Shutdown mode is exited ($\overline{SHDN}$ pin is inactive (V_{IH})):

- The device returns to the wiper setting specified by the volatile wiper value
- The TCON register bits return to controlling the terminal connection state

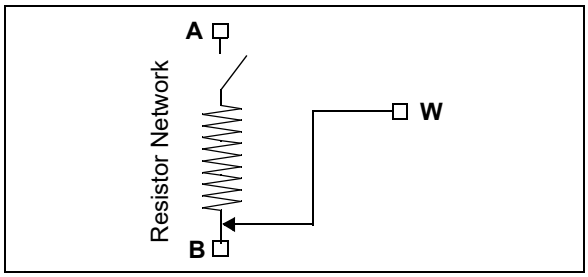


FIGURE 5-10: *Hardware Shutdown Resistor Network Configuration.*

5.7.2 TERMINAL CONTROL REGISTER (TCON)

The Terminal Control (TCON) register is a volatile register used to configure the connection of each resistor network terminal pin (A, B and W) to the resistor network. This register is shown in Register 4-1.

The R0HW bit forces the selected resistor network into the same state as the $\overline{SHDN}$ pin. Alternate low-power configurations may be achieved with the R0A, R0W and R0B bits.

When the R0HW bit is '0':

- The P0A terminal is disconnected
- The P0W terminal is simultaneously connected to the P0B terminal (see Figure 5-11)

Note: When the R0HW bit forces the resistor network into the hardware $\overline{SHDN}$ state, the state of the TCON0 register's R0A, R0W and R0B bits is overridden (ignored). When the state of the R0HW bit no longer forces the resistor network into the hardware $\overline{SHDN}$ state, the TCON0 register's R0A, R0W and R0B bits return to controlling the terminal connection state. In other words, the R0HW bit does not corrupt the state of the R0A, R0W and R0B bits.

The R0HW bit does NOT corrupt the values in the Volatile Wiper registers nor the TCON register. When the Shutdown mode is exited (R0HW bit = 1):

- The device returns to the wiper setting specified by the volatile wiper value
- The TCON register bits return to controlling the terminal connection state

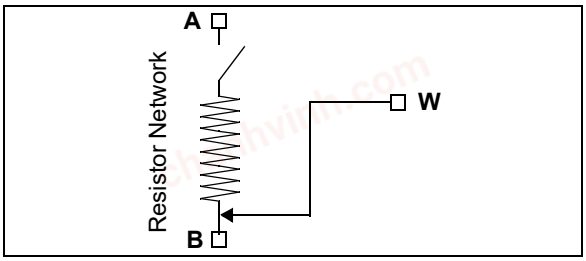


FIGURE 5-11: *Resistor Network Shutdown State (R0HW = 0).*

5.7.3 INTERACTION OF $\overline{SHDN}$ PIN AND TCON REGISTER

Figure 4-6 shows how the $\overline{SHDN}$ pin signal and the R0HW bit signal interact to control the hardware shutdown of the resistor network.

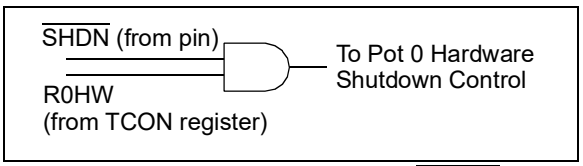


FIGURE 5-12: *R0HW bit and $\overline{SHDN}$ pin Interaction.*

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6.0 SERIAL INTERFACE (SPI)

The MCP41HVX1 devices support the SPI serial protocol. This SPI operates in the Slave mode (does not generate the serial clock). The device's SPI command format operates on multiples of eight bits.

The SPI interface uses up to four pins. These are:

- $\overline{CS}$ – Chip Select
- SCK – Serial Clock
- SDI – Serial Data In
- SDO – Serial Data Out

A typical SPI interface is shown in Figure 6-1. In the SPI interface, the Master's Output pin is connected to the Slave's Input pin, and the Master's Input pin is connected to the Slave's Output pin.

The MCP41HVX1 SPI module supports two (of the four) standard SPI modes. These are Mode 0,0 and 1,1. The SPI mode is determined by the state of the SCK pin (V_{IH} or V_{IL}) when the $\overline{CS}$ pin transitions from inactive (V_{IH}) to active (V_{IL}).

Note:	Some Host Controller SPI modules only operate with 16-bit transfers. For these Host Controllers, only the Read and Write Commands or the Continuous Increment or Decrement Commands that are an even multiple of Increment or Decrement commands may be used.

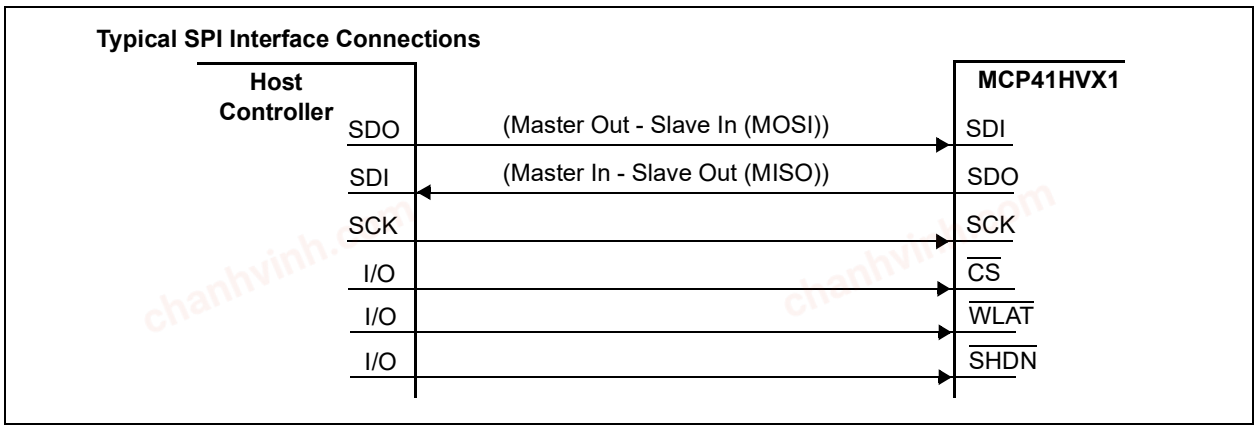


FIGURE 6-1: *Typical SPI Interface Block Diagram.*

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6.1 SDI, SDO, SCK, and $\overline{CS}$ Operation

The operation of the four SPI interface pins are discussed in this section. These pins are:

- **Serial Data In (SDI)**
- **Serial Data Out (SDO)**
- **Serial Clock (SCK)**
- **The Chip Select Signal (CS)**

The serial interface works on either 8-bit or 16-bit boundaries depending on the selected command. The Chip Select ($\overline{CS}$) pin frames the SPI commands.

6.1.1 SERIAL DATA IN (SDI)

The Serial Data In (SDI) signal is the data signal into the device. The value on this pin is latched on the rising edge of the SCK signal.

6.1.2 SERIAL DATA OUT (SDO)

The Serial Data Out (SDO) signal is the data signal out of the device. The value on this pin is driven on the falling edge of the SCK signal.

Once the $\overline{CS}$ pin is forced to the active level (V_{IL}), the SDO pin will be driven. The state of the SDO pin is determined by the serial bit's position in the command, the command selected, and if there is a command error state (CMDERR).

6.1.3 SERIAL CLOCK (SCK)

The Serial Clock (SCK) signal is the clock signal of the SPI module. The frequency of the SCK pin determines the SPI frequency of operation.

The SPI interface is specified to operate up to 10 MHz. The actual clock rate depends on the configuration of the system and the serial command used. Table 6-1 shows the SCK frequency.

TABLE 6-1: SCK FREQUENCY

V_L Voltage	Command		Comment
	Read	Write, Increment, Decrement	
2.7V	10 MHz	10 MHz	
1.8V	1 MHz	1 MHz	DGND = V- + 0.9V
2.0V	1 MHz	1 MHz	DGND = V-

6.1.4 THE CHIP SELECT SIGNAL ($\overline{CS}$)

The Chip Select ($\overline{CS}$) signal is used to select the device and frame a command sequence. To start a command, or sequence of commands, the $\overline{CS}$ signal must transition from the inactive state (V_{IH}) to an active state (V_{IL}).

After the $\overline{CS}$ signal has gone active, the SDO pin is driven and the clock bit counter is reset.

Note:	There is a required delay after the $\overline{CS}$ pin goes active to the 1st edge of the SCK pin.

If an error condition occurs for an SPI command, then the command byte's Command Error (CMDERR) bit (on the SDO pin) will be driven low (V_{IL}). To exit the error condition, the user must take the $\overline{CS}$ pin to the V_{IH} level.

When the $\overline{CS}$ pin returns to the inactive state (V_{IH}), the SPI module resets (including the Address Pointer). While the $\overline{CS}$ pin is in the inactive state (V_{IH}), the serial interface is ignored. This allows the host controller to interface to other SPI devices using the same SDI, SDO and SCK signals.

6.1.5 LOW-VOLTAGE SUPPORT

The Serial Interface is designed to also support 1.8V operation (at reduced specifications – frequency, thresholds, etc.). This allows the MCP41HVX1 device to interface to low-voltage host controllers.

At 1.8V V_L operation, the DGND signal must be 0.9V or greater above the V- signal. If V_L is 2.0V or greater, then the DGND signal can be tied to the V- signal (see Table 6-1).

6.1.6 SPLIT RAIL SUPPORT

The Serial Interface is designed to support split rail systems. In a split rail system, the microcontroller can operate at a lower voltage than the MCP41HXX1 device. This is achieved with the V_{IH} specification.

For $V_L \geq 2.7V$, the minimum $V_{IH} = 0.45 * V_L$. So if the microcontroller V_{OH} at 1.8V is $0.8 * V_{DD}$, then V_L can be a maximum of 3.2V (see Equation 6-1).

See **Section 8.1 "Split Rail Applications"** for additional discussion on split rail support.

EQUATION 6-1: CALCULATING MAX V_L FOR MICROCONTROLLER AT 1.8V

If $V_{OH} = 0.8 \times V_{DD} = 0.8 \times 1.8V = 1.44V$

Then: $V_{IH(MIN)} = 1.44V$

With $V_{IH} = 0.45 \times V_L$

Then: $V_L = 1.44V/0.45 =$ **3.2V**

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6.2 The SPI Modes

The SPI module supports two (of the four) standard SPI modes. These are Mode 0,0 and 1,1. The mode is determined by the state of the SDI pin on the rising edge of the first clock bit (of the 8-bit byte).

6.2.1 MODE 0,0

In **Mode 0,0**: SCK Idle state = low (V_{IL}), data is clocked in on the SDI pin on the rising edge of SCK and clocked out on the SDO pin on the falling edge of SCK.

6.2.2 MODE 1,1

In **Mode 1,1**: SCK Idle state = high (V_{IH}), data is clocked in on the SDI pin on the rising edge of SCK and clocked out on the SDO pin on the falling edge of SCK.

6.3 SPI Waveforms

Figures 6-2 through 6-5 show the different SPI command waveforms. Figure 6-2 and Figure 6-3 are read and write commands. Figure 6-4 and Figure 6-5 are Increment and Decrement commands.

6.4 Daisy Chaining

This SPI Interface does **NOT** support daisy chaining.

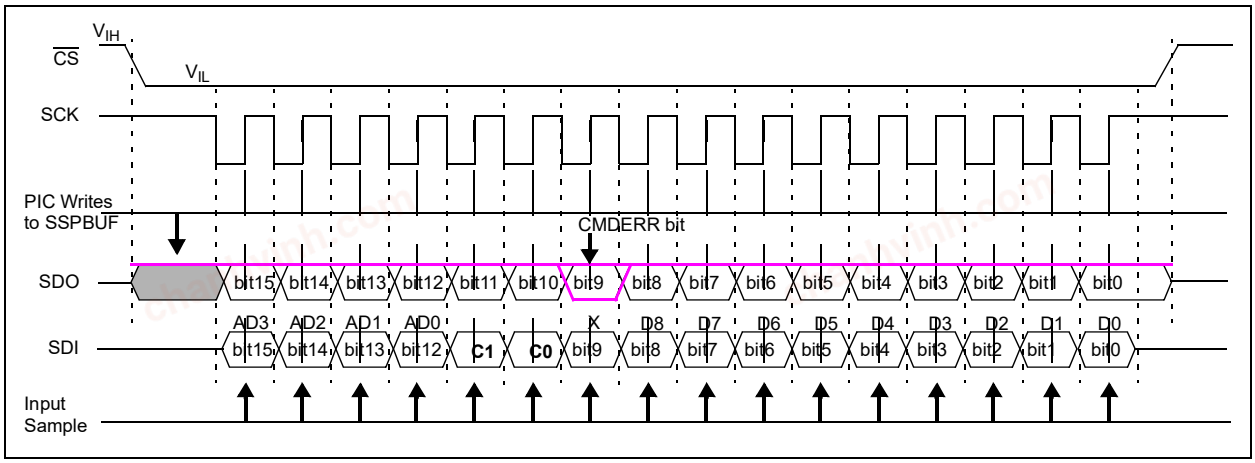


FIGURE 6-2: *16-Bit Commands (Write, Read) – SPI Waveform (Mode 1,1).*

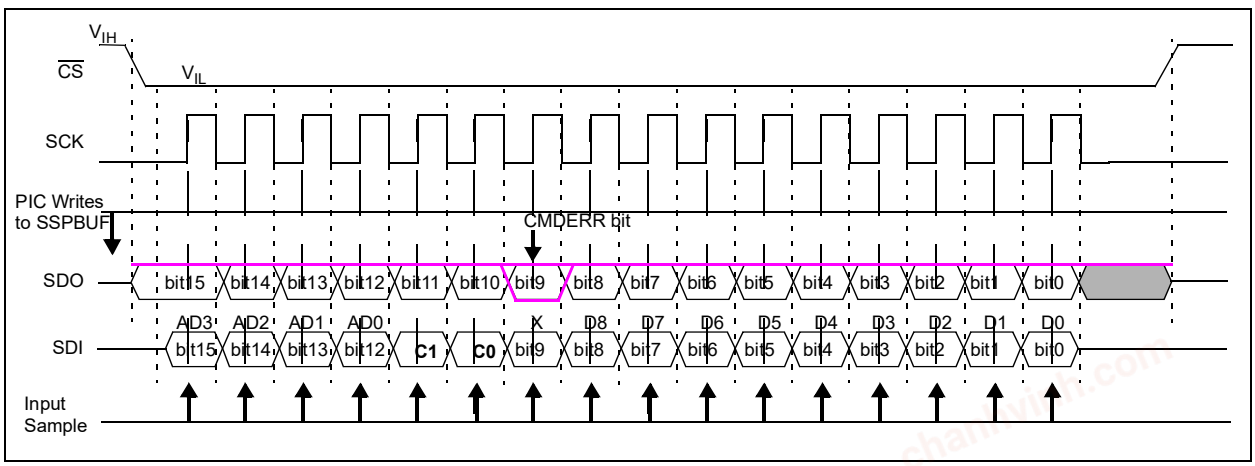


FIGURE 6-3: *16-Bit Commands (Write, Read) – SPI Waveform (Mode 0,0).*

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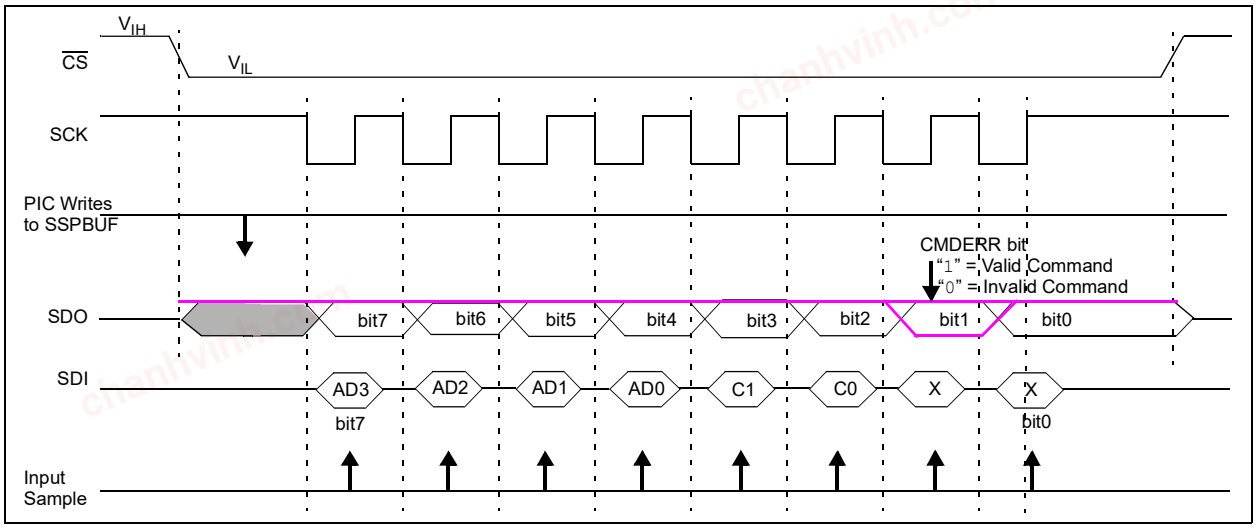


FIGURE 6-4: *8-Bit Commands (Increment, Decrement) – SPI Waveform with PIC MCU (Mode 1,1).*

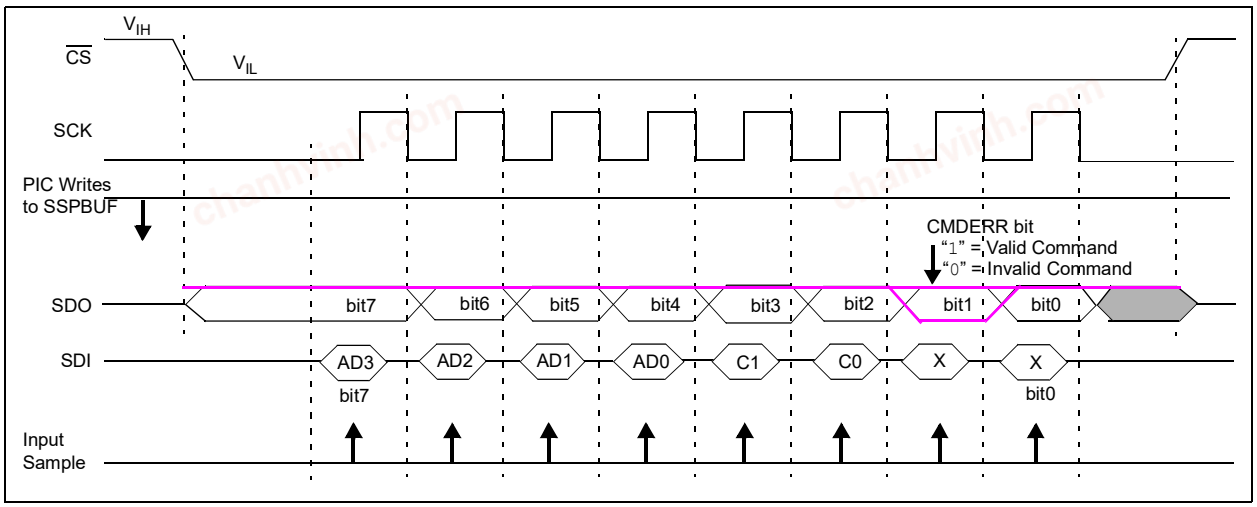


FIGURE 6-5: *8-Bit Commands (Increment, Decrement) – SPI Waveform with PIC MCU (Mode 0,0).*

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7.0 DEVICE COMMANDS

The MCP41HVX1's SPI command format supports sixteen memory address locations and four commands. These commands are shown in Table 7-1.

Commands may be sent when the $\overline{CS}$ pin is driven to V_{IL}. The 8-bit commands (**Increment Wiper** and **Decrement Wiper** commands) contain a command byte, while 16-bit commands (**Read Data** and **Write Data** commands) contain a command byte and a data byte. The command byte contains two data bits (see Figure 7-1).

Table 7-2 shows the supported commands for each memory location and the corresponding values on the SDI and SDO pins.

TABLE 7-1: COMMANDS

C1:C0 Bit States	Command Name	# of Bits
11	**Read Data**	16-Bits
00	**Write Data**	16-Bits
01	**Increment Wiper**	8-Bits
10	**Decrement Wiper**	8-Bits

7.1 Command Format

All commands have a **Command Byte** which specifies the register address and the command. Commands which require data (write and read commands) also have the **Data Byte**.

7.1.1 COMMAND BYTE

The command byte has three fields: the address, the command, and two data bits (see Figure 7-1). Currently, only one of the data bits is defined (D8). This is for the Write command.

The device memory is accessed when the master sends a proper command byte to select the desired operation. The memory location to be accessed is contained in the command byte's AD3:AD0 bits. The action desired is contained in the command byte's C1:C0 bits (see Table 7-1). C1:C0 determines if the desired memory location will be read, written, incremented (wiper setting +1) or decremented (wiper setting -1). The Increment and Decrement commands are only valid on the volatile wiper registers.

As the command byte is being loaded into the device on the SDI pin, the device's SDO pin is driving. The SDO pin will output high bits for the first six bits of that command. On the 7th bit, the SDO pin will output the CMDERR bit state (see **Section 7.1.1.1 "Error Condition"**). The 8th bit state depends on the command selected.

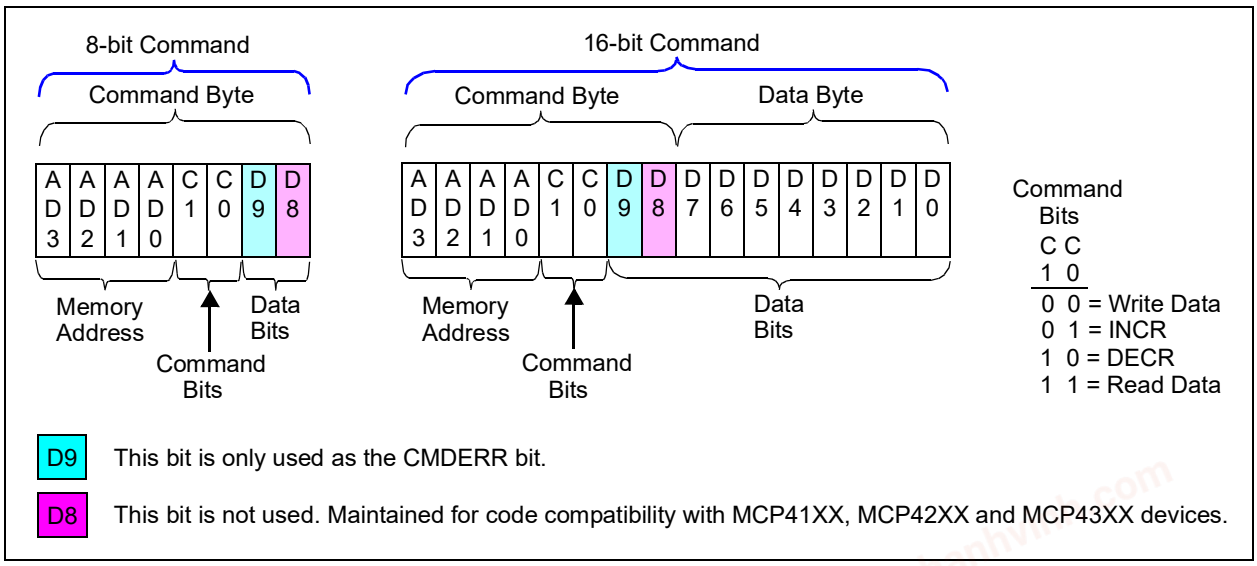


FIGURE 7-1: *General SPI Command Formats.*

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TABLE 7-2: MEMORY MAP AND THE SUPPORTED COMMANDS

Address		Command	Data (10-bits)(1)	SPI String (Binary)	
Value	Function			MOSI (SDI pin)	MISO (SDO pin)(2)
00h	Volatile Wiper 0	Write Data	nn nnnn nnnn	0000 00nn nnnn nnnn	1111 1111 1111 1111
		Read Data	nn nnnn nnnn	0000 11nn nnnn nnnn	1111 111n nnnn nnnn
		Increment Wiper	—	0000 0100	1111 1111
		Decrement Wiper	—	0000 1000	1111 1111
01h – 03h(4)	Reserved	—	—	—	—
04h(3)	Volatile TCON Register	Write Data	nn nnnn nnnn	0100 00nn nnnn nnnn	1111 1111 1111 1111
		Read Data	nn nnnn nnnn	0100 11nn nnnn nnnn	1111 111n nnnn nnnn
05h – 0Fh(4)	Reserved	—	—	—	—

Note 1: The data memory is eight bits wide, so the two MSbs (D9:D8) are ignored by the device.

2: All these address/command combinations are valid, so the CMDERR bit is set. Any other address/command combination is a command error state and the CMDERR bit will be clear.

3: Increment or Decrement commands are invalid for these addresses.

4: **Reserved addresses**: Any command is invalid for these addresses.

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7.1.1.1 Error Condition

The CMDERR bit indicates if the four address bits received (AD3:AD0) and the two command bits received (C1:C0) are a valid combination. The CMDERR bit is high if the combination is valid and low if the combination is invalid (see Table 7-3).

The command error bit will also be low if a write to a Reserved Address has been specified. SPI commands that do not have a multiple of eight clocks are ignored.

Once an error condition has occurred, any following commands are ignored. All following SDO bits will be low until the CMDERR condition is cleared by forcing the $\overline{CS}$ pin to the inactive state (V_{IH}).

TABLE 7-3: COMMAND ERROR BIT

CMDERR Bit States	Description
1	"Valid" Command/Address combination
0	"Invalid" Command/Address combination

Aborting a Transmission

All SPI transmissions must have the correct number of SCK pulses to be executed. The command is not executed until the complete number of clocks have been received. Some commands also require the $\overline{CS}$ pin to be forced inactive (V_{IH}). If the $\overline{CS}$ pin is forced to the inactive state (V_{IH}), the serial interface is reset. Partial commands are not executed.

SPI is more susceptible to noise than other bus protocols. The most likely case is that this noise corrupts the value of the data being clocked into the MCP41HVX1 or the SCK pin is injected with extra clock pulses. This may cause data to be corrupted in the device or cause a command error to occur, since the address and command bits were not a valid combination. The extra SCK pulse will also cause the SPI data (SDI) and clock (SCK) to be out of sync. Forcing the $\overline{CS}$ pin to the inactive state (V_{IH}) resets the serial interface. The SPI interface will ignore activity on the SDI and SCK pins until the $\overline{CS}$ pin transition to the active state is detected (V_{IH} to V_{IL}).

Note 1: When data is not being received by the MCP41HVX1, it is recommended that the $\overline{CS}$ pin be forced to the inactive level (V_{IL})

2: It is also recommended that long continuous command strings should be broken down into single commands or shorter continuous command strings. This reduces the probability of noise on the SCK pin corrupting the desired SPI commands.

7.1.2 DATA BYTE

Only the Read command and the Write command use the data byte (see Figure 7-1). These commands concatenate the eight bits of the data byte with the one data bit (D8) contained in the command byte to form nine bits of data (D8:D0). The command byte format supports up to nine bits of data, but the MCP41HVX1 only uses the lower eight bits. That means that the full-scale code of the 8-bit resistor network is FFh. When at full-scale, the wiper connects to Terminal A. The D8 bit is maintained for code compatibility with the MCP41XX, MCP42XX, and MCP43XX devices.

The D9 bit is currently unused, and corresponds to the position on the SDO data of the CMDERR bit.

7.1.3 CONTINUOUS COMMANDS

The device supports the ability to execute commands continuously while the $\overline{CS}$ pin is in the active state (V_{IL}). Any sequence of valid commands may be received.

The following example is a valid sequence of events:

1. $\overline{CS}$ pin driven active (V_{IL}).
2. Read Command.
3. Increment Command (Wiper 0).
4. Increment Command (Wiper 0).
5. Decrement Command (Wiper 0).
6. Write Command.
7. Read Command.
8. $\overline{CS}$ pin driven inactive (V_{IH}).

Note 1: It is recommended that while the $\overline{CS}$ pin is active, only one type of command should be issued. When changing commands, it is recommended to take the $\overline{CS}$ pin inactive, then force it back to the active state.

2: It is also recommended that long command strings should be broken down into shorter command strings. This reduces the probability of noise on the SCK pin corrupting the desired SPI command string.

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7.2 Write Data

The Write command is a 16-bit command. The format of the command is shown in Figure 7-2.

A Write command to a volatile memory location changes that location after a properly formatted Write command (16-clock) has been received.

7.2.1 SINGLE WRITE TO VOLATILE MEMORY

The write operation requires that the $\overline{CS}$ pin be in the active state (V_{IL}). Typically, the $\overline{CS}$ pin will be in the inactive state (V_{IH}) and is driven to the active state (V_{IL}). The 16-bit Write command (command byte and data byte) is then clocked (SCK pin) in on the SDI pin. Once all 16 bits have been received, the specified volatile address is updated. A write will not occur if the write command isn't exactly 16 clocks pulses.

Figures 6-2 and 6-3 show possible waveforms for a single write.

	COMMAND BYTE								DATA BYTE								
SDI	AD3	AD2	AD1	AD0	0	0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
SDO	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	Valid Address/Command combination
	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	Invalid Address/Command combination (1)

Note 1: If an Error Condition occurs (CMDERR = L), all following SDO bits will be low until the CMDERR condition is cleared (the CS pin is forced to the inactive state).

FIGURE 7-2: *Write Command – SDI and SDO States.*

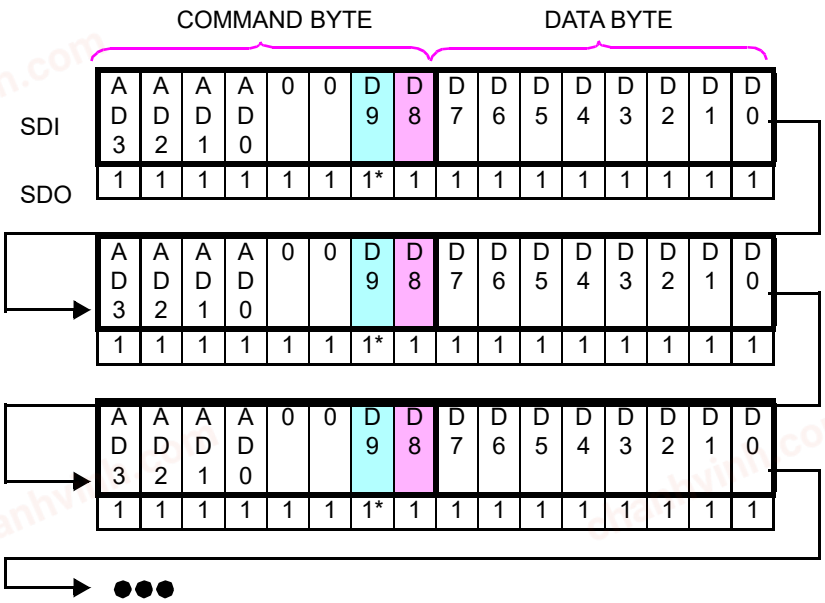
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7.2.2 CONTINUOUS WRITES TO VOLATILE MEMORY

Continuous writes are possible only when writing to the volatile memory registers (address 00h and 04h).

Figure 7-3 shows the sequence for three continuous writes. The writes do not need to be to the same volatile memory address.



Note 1: If a Command Error (CMDERR) occurs at this bit location (*), then all following SDO bits will be driven low until the CS pin is driven inactive (V_{IH}).

FIGURE 7-3: *Continuous Write Sequence.*

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7.3 Read Data

The Read command is a 16-bit command. The format of the command is shown in Figure 7-4.

The first six bits of the Read command determine the address and the command. The 7th clock will output the CMDERR bit on the SDO pin. The 8th clock will be fixed at 1, and with the remaining eight clocks, the device will transmit the eight data bits (D7:D0) of the specified address (AD3:AD0).

Figure 7-4 shows the SDI and SDO information for a Read command.

7.3.1 SINGLE READ

The read operation requires that the $\overline{CS}$ pin be in the active state (V_{IL}). Typically, the $\overline{CS}$ pin will be in the inactive state (V_{IH}) and is driven to the active state (V_{IL}). The 16-bit Read command (command byte and data byte) is then clocked (SCK pin) in on the SDI pin. The SDO pin starts driving data on the 7th bit (CMDERR bit) and the addressed data comes out on the 8th through 16th clocks. Figures 6-2 through 6-3 show possible waveforms for a single read.

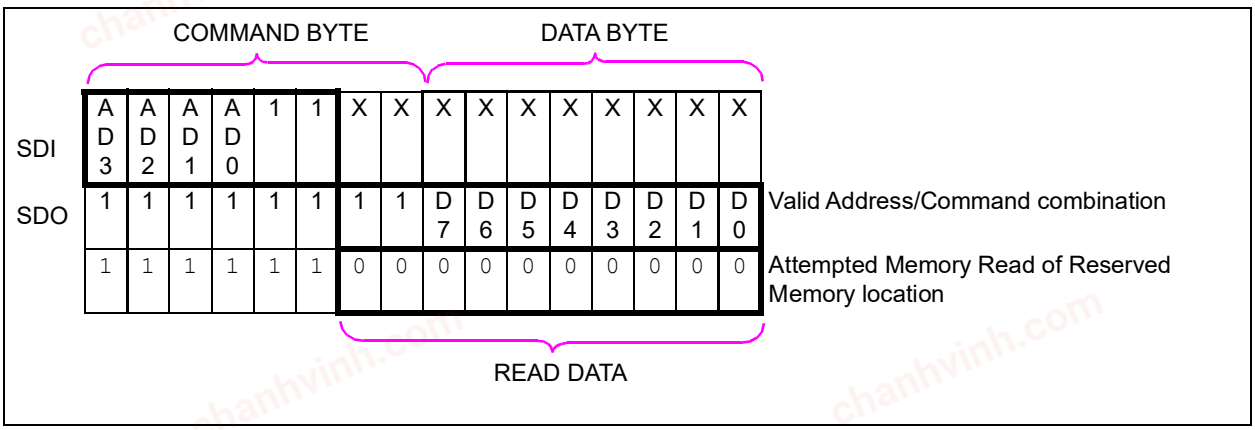


FIGURE 7-4: *Read Command – SDI and SDO States.*

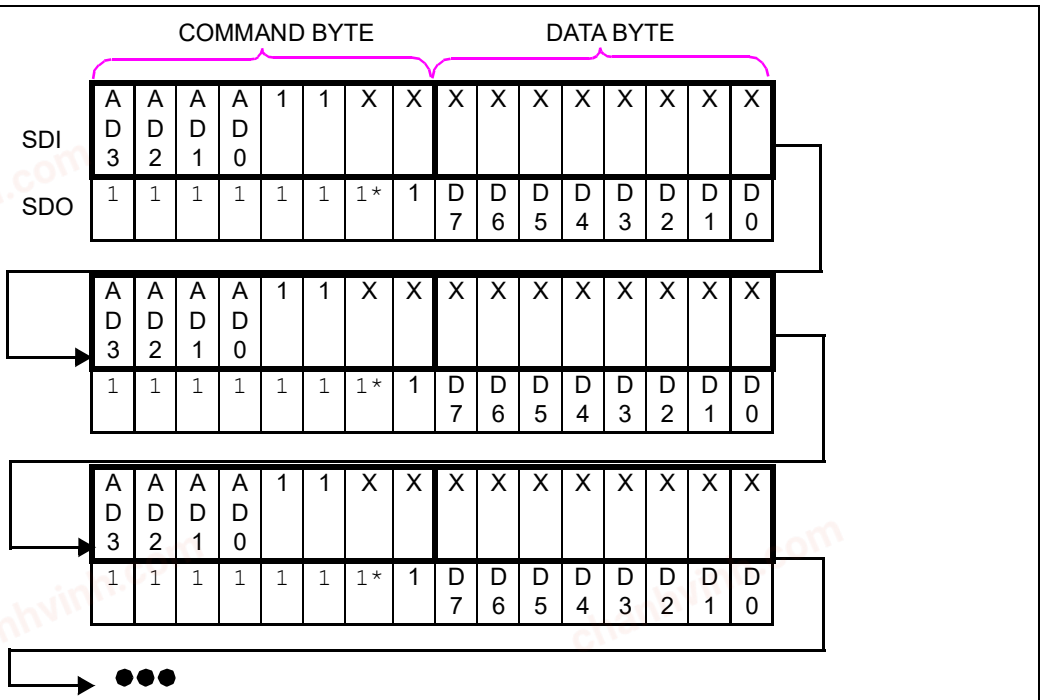
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7.3.2 CONTINUOUS READS

Continuous reads allow the device's memory to be read quickly. Continuous reads are possible to all memory locations.

Figure 7-5 shows the sequence for three continuous reads. The reads do not need to be to the same memory address.



Note 1: If a Command Error (CMDERR) occurs at this bit location (*), then all following SDO bits will be driven low until the $\overline{CS}$ pin is driven inactive (V_{IH}).

FIGURE 7-5: *Continuous Read Sequence.*

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7.4 Increment Wiper

The Increment command is an 8-bit command. The Increment command can only be issued to specific volatile memory locations (the wiper register). The format of the command is shown in Figure 7-6.

An Increment command to the volatile memory location changes that location after a properly formatted command (eight clocks) has been received.

Increment commands provide a quick and easy method to modify the value of the volatile wiper location by +1 with minimal overhead.

COMMAND BYTE

(INCR COMMAND (n+1))

	AD3	AD2	AD1	AD0	0	1	X	X	
SDI									
SDO	1	1	1	1	1	1	1*	1	Note 1, 2
	1	1	1	1	1	1	0	0	Note 1, 3

Note 1: Only functions when writing the volatile wiper register (AD3:AD0 = 0h).

2: Valid Address/Command combination.

3: Invalid Address/Command combination all following SDO bits will be low until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the inactive state).

FIGURE 7-6: *Increment Command – SDI and SDO States.*

Note: Table 7-2 shows the valid addresses for the Increment Wiper command. Other addresses are invalid.

7.4.1 SINGLE INCREMENT

Typically, the $\overline{CS}$ pin starts at the inactive state (V_{IH}), but may already be in the active state due to the completion of another command.

Figures 6-4 through 6-5 show possible waveforms for a single increment. The increment operation requires that the $\overline{CS}$ pin be in the active state (V_{IL}). Typically, the $\overline{CS}$ pin will be in the inactive state (V_{IH}) and is driven to the active state (V_{IL}). The 8-bit Increment command (command byte) is then clocked in on the SDI pin by the SCK pins. The SDO pin drives the CMDERR bit on the 7th clock.

The wiper value will increment up to FFh on 8-bit devices and 7Fh on 7-bit devices. After the wiper value has reached full-scale (8-bit = FFh, 7-bit = 7Fh), the wiper value will not be incremented further. See Table 7-4 for additional information on the Increment command versus the current volatile wiper value.

The increment operations only require the Increment command byte while the $\overline{CS}$ pin is active (V_{IL}) for a single increment.

After the wiper is incremented to the desired position, the $\overline{CS}$ pin should be forced to V_{IH} to ensure that unexpected transitions on the SCK pin do not cause the wiper setting to change. Driving the $\overline{CS}$ pin to V_{IH} should occur as soon as possible (within device specifications) after the last desired increment occurs.

TABLE 7-4: INCREMENT OPERATION VS. VOLATILE WIPER VALUE

Current Wiper Setting		Wiper (W) Properties	Increment Command Operates?
7-bit Pot	8-bit Pot		
7Fh	FFh	Full-Scale (W = A)	No
7Eh 40h	FEh 80h	W = N	Yes
3Fh	7Fh	W = N (Mid-Scale)	
3Eh 01h	7Eh 01h	W = N	
00h	00h	Zero-Scale (W = B)	Yes

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7.4.2 CONTINUOUS INCREMENTS

Continuous increments are possible only when writing to the volatile wiper registers (address 00h).

Figure 7-7 shows a continuous increment sequence.

When executing a continuous Increment command, the selected wiper will be altered from n to n+1 for each Increment command received. The wiper value will increment up to FFh on 8-bit devices and 7Fh on 7-bit devices. After the wiper value has reached full-scale (8-bit = FFh, 7-bit = 7Fh), the wiper value will not be incremented further.

Increment commands can be sent repeatedly without raising $\overline{CS}$ until a desired condition is met.

When executing a continuous command string, the Increment command can be followed by any other valid command.

The wiper terminal will move after the command has been received (8th clock).

After the wiper is incremented to the desired position, the $\overline{CS}$ pin should be forced to V_{IH} to ensure that unexpected transitions on the SCK pin do not cause the wiper setting to change. Driving the $\overline{CS}$ pin to V_{IH} should occur as soon as possible (within device specifications) after the last desired increment occurs.

	COMMAND BYTE (INCR COMMAND (n+1))								COMMAND BYTE (INCR COMMAND (n+2))								COMMAND BYTE (INCR COMMAND (n+3))								
SDI	AD3	AD2	AD1	AD0	0	1	X	X	AD3	AD2	AD1	AD0	0	1	X	X	AD3	AD2	AD1	AD0	0	1	X	X	
	1	1	1	1	1	1	1*	1	1	1	1	1	1	1	1*	1	1	1	1	1	1	1	1*	1	**Note 1, 2**
SDO	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**Note 3, 4**
	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	**Note 3, 4**
	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	**Note 3, 4**

Note 1: Only functions when writing the volatile wiper register (AD3:AD0 = 0h).

2: Valid Address/Command combination.

3: Invalid Address/Command combination.

4: If an error condition occurs (CMDERR = L), all following SDO bits will be low until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the inactive state).

FIGURE 7-7: *Continuous Increment Command – SDI and SDO States.*

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7.5 Decrement Wiper

The Decrement command is an 8-bit command. The Decrement command can only be issued to volatile wiper locations. The format of the command is shown in Figure 7-8.

A Decrement command to the volatile wiper location changes that location after a properly formatted command (eight clocks) has been received.

Decrement commands provide a quick and easy method to modify the value of the volatile wiper location by -1 with minimal overhead.

COMMAND BYTE

(DECR COMMAND (n+1))

	AD3	AD2	AD1	AD0	1	0	X	X	
SDI									
SDO	1	1	1	1	1	1	1*	1	Note 1, 2
	1	1	1	1	1	1	0	0	Note 1, 3

Note 1: Only functions when writing the volatile wiper registers (AD3:AD0 = 0h).

2: Valid Address/Command combination.

3: Invalid Address/Command combination, all following SDO bits will be low until the CMDERR condition is cleared. (the $\overline{CS}$ pin is forced to the inactive state).

FIGURE 7-8: *Decrement Command – SDI and SDO States.*

Note: Table 7-2 shows the valid addresses for the Decrement Wiper command. Other addresses are invalid.

7.5.1 SINGLE DECREMENT

Typically, the $\overline{CS}$ pin starts at the inactive state (V_{IH}), but may already be in the active state due to the completion of another command.

Figures 6-4 through 6-5 show possible waveforms for a single decrement. The decrement operation requires that the $\overline{CS}$ pin be in the active state (V_{IL}). Typically, the $\overline{CS}$ pin will be in the inactive state (V_{IH}) and is driven to the active state (V_{IL}). Then the 8-bit Decrement command (command byte) is clocked in on the SDI pin by the SCK pin. The SDO pin drives the CMDERR bit on the 7th clock.

The wiper value will decrement from the wiper's full-scale value (FFh on 8-bit devices and 7Fh on 7-bit devices). If the wiper register has a zero-scale value (00h), then the wiper value will not decrement. See Table 7-5 for additional information on the Decrement command vs. the current volatile wiper value.

The Decrement commands only require the Decrement command byte while the $\overline{CS}$ pin is active (V_{IL}) for a single decrement.

After the wiper is decremented to the desired position, the $\overline{CS}$ pin should be forced to V_{IH} to ensure that unexpected transitions on the SCK pin do not cause the wiper setting to change. Driving the $\overline{CS}$ pin to V_{IH} should occur as soon as possible (within device specifications) after the last desired decrement occurs.

TABLE 7-5: DECREMENT OPERATION VS. VOLATILE WIPER VALUE

Current Wiper Setting		Wiper (W) Properties	Decrement Command Operates?
7-bit Pot	8-bit Pot		
7Fh	FFh	Full-Scale (W = A)	Yes
7Eh 40h	FEh 80h	W = N	Yes
3Fh	7Fh	W = N (Mid-Scale)	
3Eh 01h	7Eh 01h	W = N	
00h	00h	Zero-Scale (W = B)	No

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7.5.2 CONTINUOUS DECREMENTS

Continuous decrements are possible only when writing to the volatile wiper register (address 00h).

Figure 7-9 shows a continuous decrement sequence.

When executing continuous Decrement commands, the selected wiper will be altered from n to n-1 for each Decrement command received. The wiper value will decrement from the wiper's full-scale value (FFh on 8-bit devices and 7Fh on 7-bit devices). If the Wiper register has a zero-scale value (00h), then the wiper value will not decrement. See Table 7-5 for additional information on the Decrement command vs. the current volatile wiper value.

Decrement commands can be sent repeatedly without raising $\overline{CS}$ until a desired condition is met.

When executing a continuous command string, the Decrement command can be followed by any other valid command.

The wiper terminal will move after the command has been received (8th clock).

After the wiper is decremented to the desired position, the $\overline{CS}$ pin should be forced to V_{IH} to ensure that "unexpected" transitions on the SCK pin do not cause the wiper setting to change. Driving the $\overline{CS}$ pin to V_{IH} should occur as soon as possible (within device specifications) after the last desired decrement occurs.

	COMMAND BYTE (DECR COMMAND (n-1))								COMMAND BYTE (DECR COMMAND (n-1))								COMMAND BYTE (DECR COMMAND (n-1))								
SDI	AD3	AD2	AD1	AD0	1	0	X	X	AD3	AD2	AD1	AD0	1	0	X	X	AD3	AD2	AD1	AD0	1	0	X	X	
	1	1	1	1	1	1	1*	1	1	1	1	1	1	1	1*	1	1	1	1	1	1	1	1*	1	Note 1, 2
SDO	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Note 3, 4
	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	Note 3, 4
	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	Note 3, 4

Note 1: Only functions when writing the volatile wiper registers (AD3:AD0 = 0h).

2: Valid Address/Command combination.

3: Invalid Address/Command combination.

4: If an Error Condition occurs (CMDERR = L), all following SDO bits will be low until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the inactive state).

FIGURE 7-9: *Continuous Decrement Command – SDI and SDO States.*

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8.0 APPLICATIONS EXAMPLES

Digital potentiometers have a multitude of practical uses in modern electronic circuits. The most popular uses include precision calibration of set point thresholds, sensor trimming, LCD bias trimming, audio attenuation, adjustable power supplies, motor control overcurrent trip setting, adjustable gain amplifiers and offset trimming.

8.1 Split Rail Applications

Split rail applications are when one device operates from one voltage level (rail) and the second device operates from a second voltage level (rail). The typical scenario will be when the microcontroller is operating at a lower voltage level (for power savings, etc) and the MCP41HVX1 is operating at a higher voltage level to maximize operational performance. This configuration is shown in Figure 8-1.

To ensure that communication properly occurs between the devices, care must be done to verify the compatibility of the V_{IL}, V_{IH}, V_{OL} and V_{OH} levels of the interface signals between the devices. These interface signals are:

- $\overline{CS}$
- SCK
- SDI
- SDO
- $\overline{SHDN}$
- $\overline{WLAT}$

When the microcontroller is at a lower-voltage rail, the V_{OH} of the microcontroller needs to be greater than the V_{IH} of the MCP41HVX1, and the V_{IL} of the microcontroller needs to be greater than the V_{OL} of the MCP41HVX1.

Table 8-1 shows the calculated maximum MCP41HVX1 V_L based on the microcontroller's minimum V_{OH}.

Note: V_{OH} specifications typically have a current load specified. This is due to the pin expected to drive externally circuitry. If the pin is unloaded (or lightly loaded), then the V_{OH} of the pin could approach the device V_{DD} (this is dependent on the implementation of the output driver circuit). For V_{OL}, unloaded (or lightly loaded) pins could approach the device V_{SS}.
For V_{OH} and V_{OL} characterization graphs from an example microcontroller, see the PIC16F1934 data sheet (DS41364), Figure 31-15 and Figure 31-16.

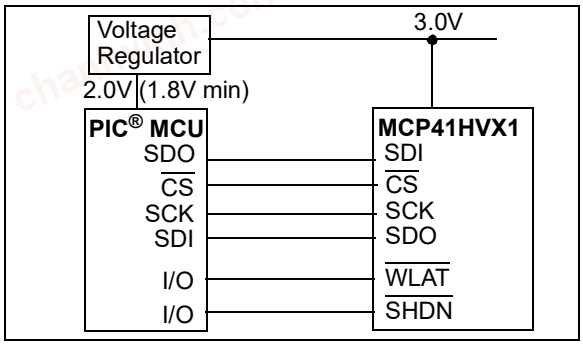


FIGURE 8-1: *Example Split Rail System.*

TABLE 8-1: MCP41HVX1 V_L VOLTAGE BASED ON MICROCONTROLLER V_{OH}

PIC® MCU			MCP41HVX1 Max V_L
V_{DD} (minimum)	V_{OH} (minimum)(1)		
	Formula (with load)	Calculated	
1.8V	0.7 × V_{DD}	1.26V	2.8V
	0.8 × V_{DD}	1.44V	3.2V
	0.85 × V_{DD}	1.53V	3.4V
	0.9 × V_{DD}	1.62V	3.6V
	V_{DD}	1.8V	4.0V
	V_{DD} - 0.7V	1.1V	2.44V
2.7V	0.7 × V_{DD}	1.89V	4.2V
	0.8 × V_{DD}	2.16V	4.8V
	0.9 × V_{DD}	2.43V	5.4V
	V_{DD}	2.7V	5.5V

Note 1: The V_{OH} minimum voltage is determined by the load on the pin. If the load is small, a typical output's voltage should approach the device's V_{DD} voltage. This is dependent on the device's output driver design.

2: Split Rail voltages are dependent on V_{IL}, V_{IH}, V_{OL}, and V_{OH} of the microcontroller and the MCP41HVX1 devices.

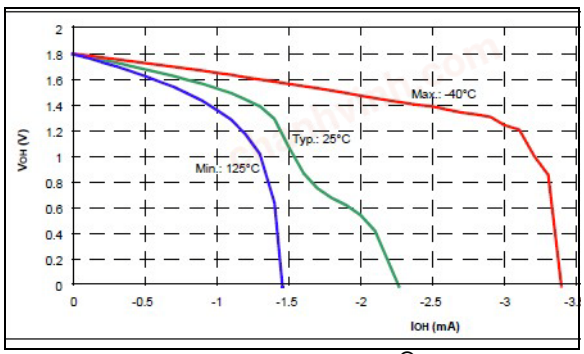


FIGURE 8-2: *Example PIC® Microcontroller V_{OH} Characterization Graph (V_{DD} = 1.8V).*

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8.2 Using Shutdown Modes

Figure 8-3 shows a possible application circuit where the independent terminals could be used. Disconnecting the wiper allows the transistor input to be taken to the bias voltage level (disconnecting A and/or B may be desired to reduce system current). Disconnecting Terminal A modifies the transistor input by the R_{BW} rheostat value to the Common B. Disconnecting Terminal B modifies the transistor input by the R_{AW} rheostat value to the Common A. The Common A and Common B connections could be connected to V+ and V-.

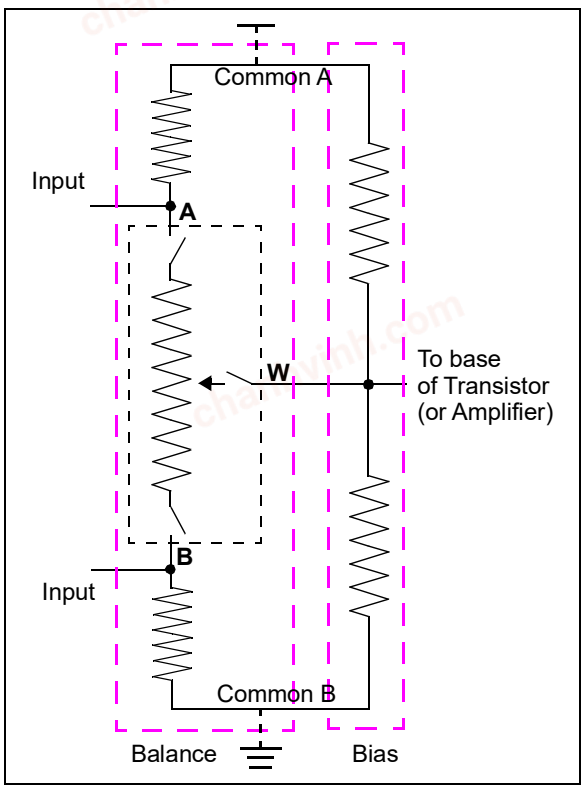


FIGURE 8-3: *Example Application Circuit using Terminal Disconnects.*

8.3 High-Voltage DAC

A high-voltage DAC can be implemented using the MCP41HVXX, with voltages as high as 36V. The circuit is shown in Figure 8-4. The equation to calculate the voltage output is shown in Equation 8-1.

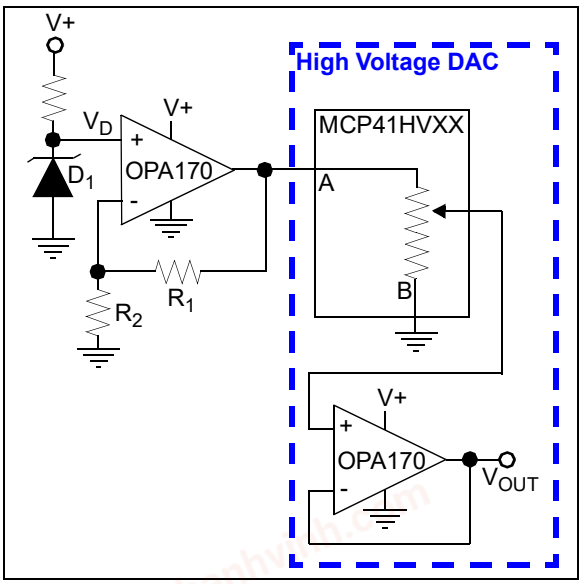


FIGURE 8-4: *High-Voltage DAC.*

EQUATION 8-1: DAC OUTPUT VOLTAGE CALCULATION

8-bit

$$V_{OUT}(N) = \frac{N}{255} \times \left(V_D \times \left(1 + \frac{R1}{R2}\right)\right)$$

N = 0 to 255 (decimal)

7-bit

$$V_{OUT}(N) = \frac{N}{127} \times \left(V_D \times \left(1 + \frac{R1}{R2}\right)\right)$$

N = 0 to 127 (decimal)

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8.4 Variable Gain Instrumentation Amplifier

A variable gain instrumentation amplifier can be implemented using the MCP41HVXX along with a high-voltage dual analog switch and a high-voltage instrumentation amplifier. An example circuit is shown in Figure 8-5. The equation to calculate the voltage output is shown in Equation 8-2.

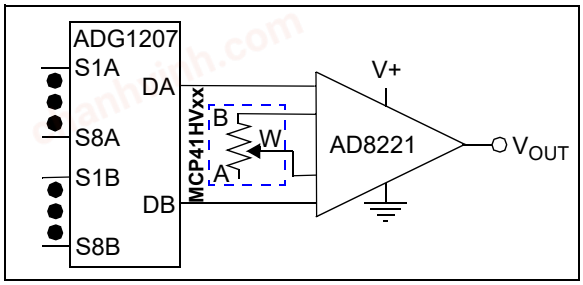


FIGURE 8-5: *Variable Gain Instrumentation Amplifier for Data Acquisition System.*

EQUATION 8-2: DAC OUTPUT VOLTAGE CALCULATION

8-bit

$$Gain(N) = 1 + \frac{49.4\ k\Omega}{\frac{N}{255} \times R_{AB}}$$

N = 0 to 255 (decimal)

7-bit

$$Gain(N) = 1 + \frac{49.4\ k\Omega}{\frac{N}{127} \times R_{AB}}$$

N = 0 to 127 (decimal)

8.5 Audio Volume Control

A digital volume control can be implemented with the MCP41HVXX. Figure 8-6 shows a simple audio volume control implementation.

Figure 8-7 shows a circuit-referenced voltage crossing detect circuit. The output of this circuit could be used to control the wiper latch of the MCP41HVXX device in the audio volume control circuit to reduce zipper noise or to update the different channels at the same time.

The op amp (U1) could be an MCP6001, while the general purpose comparators (U2 and U3) could be an MCP6541. U4 is a simple AND gate.

U1 establishes the signal zero reference. The upper limit of the comparator is set above its offset. The $\overline{WLAT}$ pin is forced high whenever the voltage falls between 2.502V and 2.497V (a 0.005V window).

The capacitor C1 AC couples the V_{IN} signal into the circuit before feeding into the windowed comparator (and MCP41HVXX Terminal A pin).

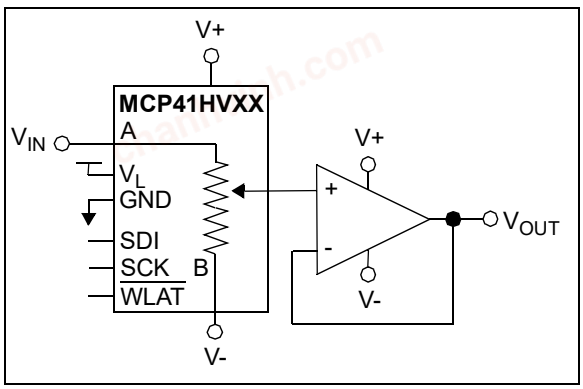


FIGURE 8-6: *Audio Volume Control.*

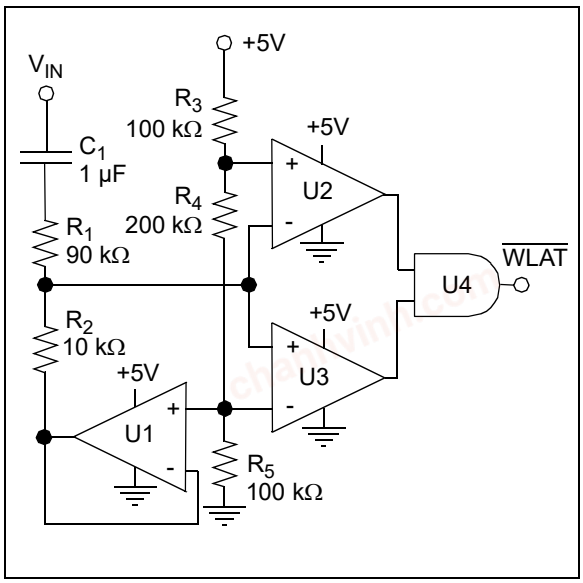


FIGURE 8-7: *Referenced Voltage Crossing Detect.*

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8.6 Programmable Power Supply

The ADP1611 is a step-up DC-to-DC switching converter. Using the MCP41HVXX device allows the power supply to be programmable up to 20V. Figure 8-8 shows a programmable power supply implementation.

Equation 8-3 shows the equation to calculate the output voltage of the programmable power supply. This output is derived from the R_{BW} resistance of the MCP41HVXX device and the R_2 resistor. The ADP1611 will adjust its output voltage to maintain 1.23V on the FB pin.

When power is connected, L1 acts as a short, and V_{OUT} is a diode drop below the +5V voltage. The V_{OUT} voltage will ramp to the programmed value.

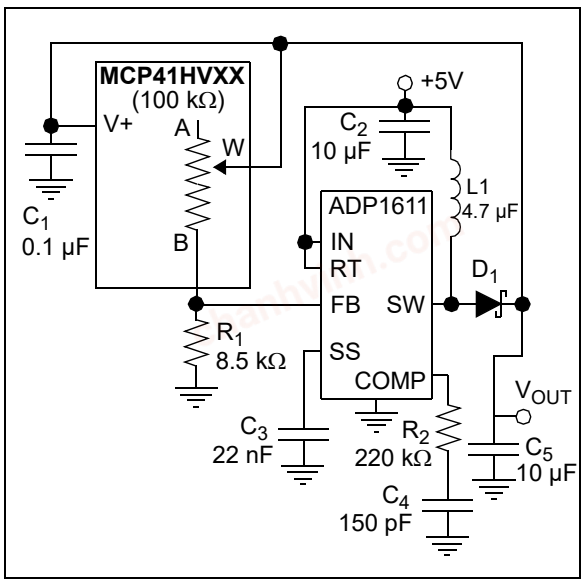


FIGURE 8-8: *Programmable Power Supply.*

EQUATION 8-3: POWER SUPPLY OUTPUT VOLTAGE CALCULATION

8-bit

$$V_{OUT}(N) = 1.23V \times \left(1 + \left(\frac{N \times R_{AB}}{\frac{255}{R_2}}\right)\right)$$

N = 0 to 255 (decimal)

7-bit

$$V_{OUT}(N) = 1.23V \times \left(1 + \left(\frac{N \times R_{AB}}{\frac{127}{R_2}}\right)\right)$$

N = 0 to 127 (decimal)

8.7 Programmable Bidirectional Current Source

A programmable bidirectional current source can be implemented with the MCP41HVXX. Figure 8-9 shows an implementation where U1 and U2 work together to deliver the desired current (dependent on selected device) in both directions. The circuit is symmetrical ($R_{1A} = R_{1B}$, $R_{2A} = R_{2B}$, $R_{3A} = R_{3B}$) in order to improve stability. If the resistors are matched, the load current (I_L) calculation is shown below:

EQUATION 8-4: LOAD CURRENT (I_L)

$$I_L = \frac{(R_{2A} + R_{3A})}{R_{1A} \times R_{3A}} \times V_W$$

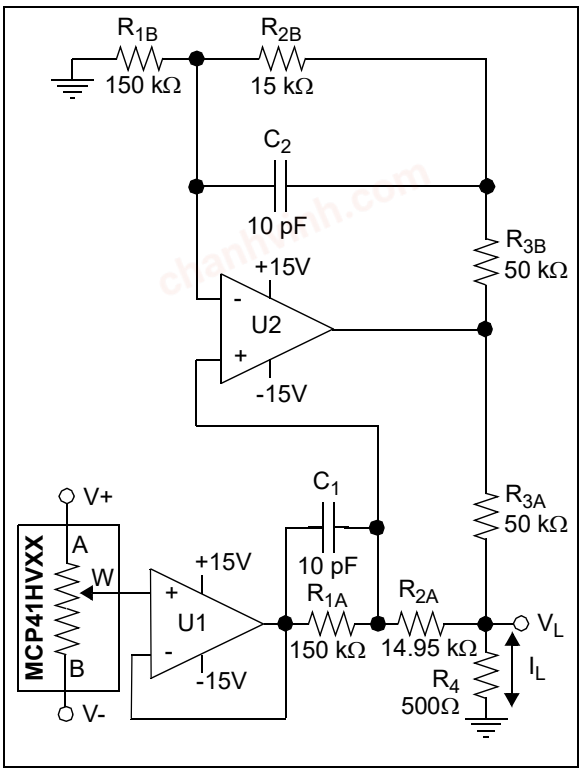


FIGURE 8-9: *Programmable Bidirectional Current Source.*

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8.8 LCD Contrast Control

The MCP41HVXX can be used for LCD contrast control. Figure 8-10 shows a simple programmable LCD contrast control implementation.

Some LCD panels support a fixed power supply of up to 28V. The high voltage digital potentiometer's wiper can support contrast adjustments through the entire voltage range.

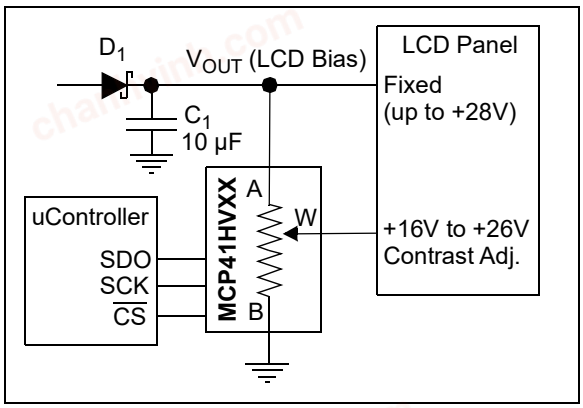


FIGURE 8-10: *Programmable Contrast Control.*

8.9 Serial Interface Communication Times

Table 8-2 shows the time for each SPI serial interface command as well as the effective data update rate that can be supported by the digital interface (based on the two SPI serial interface frequencies). So, the Serial Interface performance, along with the wiper response time, would be used to determine your application's volatile Wiper register update rate.

TABLE 8-2: SERIAL INTERFACE TIMES/FREQUENCIES(1)

Command	# of Serial Interface bits	Example		Command Time (µs)		Effective Data Update Frequency (kHz)(2)	
		# Bytes Transferred	# of Serial Interface bits	1 MHz	10 MHz	1 MHz	10 MHz
Write Single Byte	16	1	16	16	1.6	62,500	625,000
Write Continuous Bytes	N × 16	5	80	80	8	12,500	125,000
Read Byte	16	1	16	16	1.6	62,500	625,000
Read Continuous Bytes	N × 16	5	80	80	8	12,500	125,000
Increment Wiper	8	1	8	8	0.8	125,000	1,250,000
Continuous Increments	N × 8	5	40	40	4	25,000	250,000
Decrement Wiper	8	1	8	8	0.8	125,000	1,250,000
Continuous Decrements	N × 8	5	40	40	4	25,000	250,000

Note 1: Includes the Start or Stop bits.

2: This is the command frequency multiplied by the number of bytes transferred.

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8.10 Implementing Log Steps with a Linear Digital Potentiometer

In audio volume control applications, the use of logarithmic steps is desirable since the human ear hears in a logarithmic manner. The use of a linear potentiometer can approximate a log potentiometer, but with fewer steps. An 8-bit potentiometer can achieve fourteen 3 dB log steps plus a 100% (0 dB) and a mute setting.

Figure 8-11 shows a block diagram of one of the MCP45HVx1 resistor networks being used to attenuate an input signal. In this case, the attenuation will be ground referenced. Terminal B can be connected to a common-mode voltage, but the voltages on the A, B and wiper terminals must not exceed the MCP45HVX1's V+/V- voltage limits.

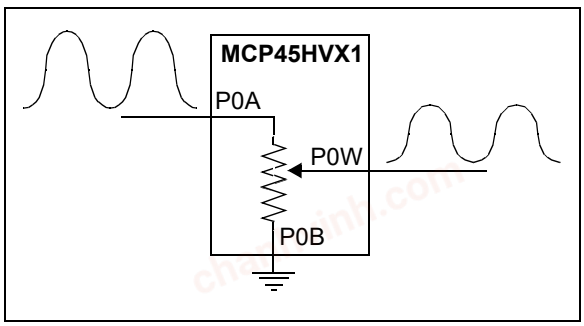


FIGURE 8-11: *Signal Attenuation Block Diagram – Ground Referenced.*

Equation 8-5 shows the equation to calculate voltage dB gain ratios for the digital potentiometer, while Equation 8-6 shows the equation to calculate resistance dB gain ratios. These two equations assume that the B terminal is connected to ground.

If Terminal B is not directly resistively connected to ground, then this Terminal B to ground resistance (R_{B2GND}) must be included into the calculation. Equation 8-7 shows this equation.

EQUATION 8-5: dB CALCULATIONS (VOLTAGE)

$$L = 20 \times \log_{10} (V_{OUT}/V_{IN})$$

dB	V_{OUT}/V_{IN} Ratio
-3	0.70795
-2	0.79433
-1	0.89125

EQUATION 8-6: dB CALCULATIONS (RESISTANCE) – CASE 1

Terminal B connected to Ground (see Figure 8-11)

$$L = 20 \times \log_{10} (R_{BW}/R_{AB})$$

EQUATION 8-7: dB CALCULATIONS (RESISTANCE) – CASE 2

Terminal B through R_{B2GND} to Ground

$$L = 20 \times \log_{10} ((R_{BW} + R_{B2GND})/(R_{AB} + R_{B2GND}))$$

Table 5-3 shows the codes that can be used for 8-bit digital potentiometers to implement the log attenuation. The table shows the wiper codes for -3 dB, -2 dB, and -1 dB attenuation steps. This table also shows the calculated attenuation based on the wiper code's linear step. Calculated attenuation values less than the desired attenuation are shown with red text. At lower wiper code values, the attenuation may skip a step. If this occurs, the next attenuation value is colored magenta to highlight that a skip occurred. For example, in the -3 dB column the -48 dB value is highlighted since the -45 dB step could not be implemented (there are no wiper codes between 2 and 1).

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TABLE 8-3: LINEAR TO LOG ATTENUATION FOR 8-BIT DIGITAL POTENTIOMETERS

# of Steps	-3 dB Steps			-2 dB Steps			-1 dB Steps		
	Desired Attenuation	Wiper Code	Calculated Attenuation (1)	Desired Attenuation	Wiper Code	Calculated Attenuation (1)	Desired Attenuation	Wiper Code	Calculated Attenuation (1)
0	0 dB	255	0 dB	0 dB	255	0 dB	0 dB	255	0 dB
1	-3 dB	180	-3.025 dB	-2 dB	203	-1.981 dB	-1 dB	227	-1.010 dB
2	-6 dB	128	-5.987 dB	-4 dB	161	-3.994 dB	-2 dB	203	-1.981 dB
3	-9dB	90	-9.046 dB	-6 dB	128	-5.987 dB	-3 dB	180	-3.025 dB
4	-12 dB	64	-12.007 dB	-8 dB	101	-8.044 dB	-4 dB	161	-3.994 dB
5	-15 dB	45	-15.067 dB	-10 dB	81	-9.961 dB	-5 dB	143	-5.024 dB
6	-18 dB	32	-18.028 dB	-12 dB	64	-12.007 dB	-6 dB	128	-5.987 dB
7	-21 dB	23	-20.896 dB	-14 dB	51	-13.979 dB	-7 dB	114	-6.993 dB
8	-24 dB	16	-24.048 dB	-16 dB	40	-16.090 dB	-8 dB	101	-8.044 dB
9	-27 dB	11	-27.303 dB	-18 dB	32	-18.028 dB	-9 dB	90	-9.046 dB
10	-30 dB	8	-30.069 dB	-20 dB	25	-20.172 dB	-10 dB	81	-9.961 dB
11	-33 dB	6	-32.568 dB	-22 dB	20	-22.110 dB	-11 dB	72	-10.984 dB
12	-36 dB	4	-36.090 dB	-24 dB	16	-24.048 dB	-12 dB	64	-12.007 dB
13	-39 dB	3	-38.588 dB	-26 dB	13	-25.852 dB	-13 dB	57	-13.013 dB
14	-42 dB	2	-42.110 dB	-28 dB	10	-28.131 dB	-14 dB	51	-13.979 dB
15	-48 dB	1	-48.131 dB	-30 dB	8	-30.069 dB	-15 dB	45	-15.067 dB
16	Mute	0	Mute	-32 dB	6	-32.602 dB	-16 dB	40	-16.090 dB
17				-34 dB	5	-34.151 dB	-17 dB	36	-17.005 dB
18				-36 dB	4	-36.090 dB	-18 dB	32	-18.028 dB
19				-38 dB	3	-38.588 dB	-19 dB	29	-18.883 dB
20				-42 dB	2	-42.110 dB	-20 dB	25	-20.172 dB
21				-48 dB	1	-48.131 dB	-21 dB	23	-20.896 dB
22				Mute	0	Mute	-22 dB	20	-22.110 dB
23							-23 dB	18	-23.025 dB
24							-24 dB	16	-24.048 dB
25							-25 dB	14	-25.208 dB
26							-26 dB	13	-25.852 dB
27							-27dB	11	-27.303 dB
28							-28 dB	10	-28.131 dB
29							-29 dB	9	-29.046 dB
30							-30 dB	8	-30.069 dB
31							-31 dB	7	-31.229 dB
32							-33 dB	6	-32.568 dB
33							-34 dB	5	-34.151 dB
34							-36 dB	4	-36.090 dB
35							-39 dB	3	-38.588 dB
36							-42 dB	2	-42.110 dB
37							-48 dB	1	-48.131 dB
38							Mute	0	Mute

Legend: Calculated Attenuation Value Color Code: **Black** → Above Target Value; **Red** → Below Target Value
Desired Attenuation Value Color Code: **Magenta** → Skipped Desired Attenuation Value(s).

Note 1: Attenuation values do not include errors from digital potentiometer errors, such as Full-Scale Error or Zero-Scale Error.

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8.11 Design Considerations

In the design of a system with the MCP41HVX1 devices, the following considerations should be taken into account:

- **Power Supply Considerations**
- **Layout Considerations**

8.11.1 POWER SUPPLY CONSIDERATIONS

The typical application will require a bypass capacitor in order to filter high-frequency noise, which can be induced onto the power supply's traces. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 8-12 illustrates an appropriate bypass strategy.

In this example, the recommended bypass capacitor value is 0.1 µF. This capacitor should be placed as close (within 4 mm) to the device power pin (V_L) as possible.

The power source supplying these devices should be as clean as possible. If the application circuit has separate digital and analog power supplies, V+ and V- should reside on the analog plane.

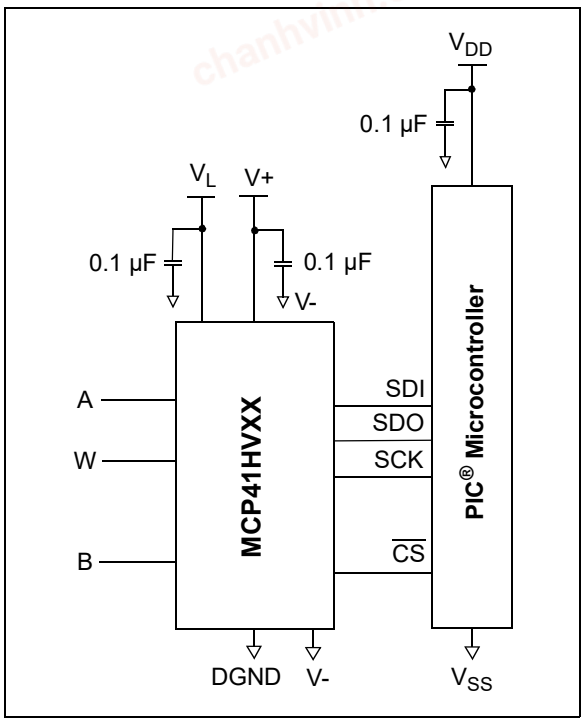


FIGURE 8-12: *Typical Microcontroller Connections.*

8.11.2 LAYOUT CONSIDERATIONS

In the design of a system with the MCP41HVX1 devices, the following layout considerations should be taken into account:

- **Noise**
- **PCB Area Requirements**
- **Power Dissipation**

8.11.2.1 Noise

Inductively-coupled AC transients and digital switching noise can degrade the input and output signal integrity, potentially masking the MCP41HVX1's performance. Careful board layout minimizes these effects and increases the Signal-to-Noise Ratio (SNR). Multi-layer boards utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are critical to achieving the performance that the silicon is capable of providing. Particularly harsh environments may require shielding of critical signals.

If low noise is desired, breadboards and wire-wrapped boards are not recommended.

8.11.2.2 PCB Area Requirements

In some applications, PCB area is a criteria for device selection. Table 8-4 shows the package dimensions and area for the different package options. The table also shows the relative area factor compared to the smallest area. The VQFN package is the suggested package for space critical applications.

TABLE 8-4: PACKAGE FOOTPRINT (1)

Package			Package Footprint			
Pins	Type	Code	Dimensions (mm)		Area (mm^2)	Relative Area
			X	Y		
14	TSSOP	ST	5.10	6.40	32.64	1.31
20	VQFN	MQ	5.00	5.00	25.00	1

Note 1: Does not include recommended land pattern dimensions.

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8.11.3 RESISTOR TEMPERATURE COEFFICIENT

Characterization curves of the resistor temperature coefficient (Tempco) are shown in the device characterization graphs.

These curves show that the resistor network is designed to correct for the change in resistance as temperature increases. This technique reduces the end-to-end change in R_{AB} resistance.

8.11.3.1 Power Dissipation

The power dissipation of the high-voltage digital potentiometer will most likely be determined by the power dissipation through the resistor networks.

Table 8-5 shows the power dissipation through the resistor ladder (R_{AB}) when Terminal A = +18V and Terminal B = -18V. This is not the worst case power dissipation based on the 25 mA terminal current specification. Table 8-6 shows the worst-case current (per resistor network), which is independent of the R_{AB} value).

TABLE 8-5: R_{AB} POWER DISSIPATION

R_{AB} Resistance (Ω)			$\lvert V_A \rvert + \lvert V_B \rvert$ = (V)	Power (mW)[1]
Typical	Min.	Max.		
5,000	4,000	6,000	36	324
10,000	8,000	12,000	36	162
50,000	40,000	60,000	36	32.4
100,000	80,000	120,000	36	16.2

Note 1: Power = V × I = $V^2/R_{AB(MIN)}$.

TABLE 8-6: R_{BW} POWER DISSIPATION

R_{AB} (Ω) (Typical)	$\lvert V_W \rvert + \lvert V_B \rvert$ = (V)	IBW (mA)[2]	Power (mW)[1]
5,000	36	25	900
10,000	36	12.5	450
50,000	36	6.5	234
100,000	36	6.5	234

Note 1: Power = V × I.

2: See Electrical Specifications (max I_W).

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9.0 DEVICE OPTIONS

9.1 Standard Options

9.1.1 POR/BOR WIPER SETTING

The default wiper setting (mid-scale) is indicated to the customer in three digit suffixes: -202, -502, -103 and -503. Table 9-1 indicates the device's default settings.

TABLE 9-1: DEFAULT POR/BOR WIPER SETTING SELECTION

Typical R_{AB} Value	Package Code	Default POR Wiper Setting	Device Resolution	Wiper Code
5.0 kΩ	-502	Mid-Scale	8-bit	7Fh
			7-bit	3Fh
10.0 kΩ	-103	Mid-Scale	8-bit	7Fh
			7-bit	3Fh
50.0 kΩ	-503	Mid-Scale	8-bit	7Fh
			7-bit	3Fh
100.0 kΩ	-104	Mid-Scale	8-bit	7Fh
			7-bit	3Fh

9.2 Custom Options

Custom options can be made available.

9.2.1 CUSTOM WIPER VALUE ON POR/BOR EVENT

Customers can specify a custom wiper setting via the NSCAR process.

Note 1: Non-Recurring Engineering (NRE) charges and minimum ordering requirements apply for custom orders. Please contact Microchip sales for additional information.

2: A custom device will be assigned custom device marking.

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10.0 DEVELOPMENT SUPPORT

10.1 Development Tools

Several development tools are available to assist in your design and evaluation of the MCP41HVX1 devices. The currently available tools are shown in Table 10-1.

Figure 10-1 shows how the TSSOP20EV bond-out PCB can be populated to easily evaluate the MCP41HVX1 devices. Evaluations can use the PICkit™ Serial Analyzer to control the position of the volatile wiper and state of the TCON register.

Figure 10-2 shows how the SOIC14EV bond-out PCB can be populated to evaluate the MCP41HVX1 devices. The use of the PICkit Serial Analyzer would require blue wire since the header H1 is not compatibly connected.

These boards may be purchased directly from the Microchip web site at www.microchip.com.

10.2 Technical Documentation

Several additional technical documents are available to assist you in your design and development. These technical documents include Application Notes, Technical Briefs, and Design Guides. Table 10-2 shows some of these documents.

TABLE 10-1: DEVELOPMENT TOOLS

Board Name	Part #	Comment
20-pin TSSOP and SSOP Evaluation Board	TSSOP20EV	Can easily interface to PICkit Serial Analyzer (Order #: DV164122)
14-pin SOIC/TSSOP/DIP Evaluation Board	SOIC14EV	

TABLE 10-2: TECHNICAL DOCUMENTATION

Application Note Number	Title	Literature #
TB3073	Implementing a 10-bit Digital Potentiometer with an 8-bit Digital Potentiometer	DS93073
AN1316	Using Digital Potentiometers for Programmable Amplifier Gain	DS01316
AN1080	Understanding Digital Potentiometers Resistor Variations	DS01080
AN737	Using Digital Potentiometers to Design Low-Pass Adjustable Filters	DS00737
AN692	Using a Digital Potentiometer to Optimize a Precision Single Supply Photo Detect	DS00692
AN691	Optimizing the Digital Potentiometer in Precision Circuits	DS00691
AN219	Comparing Digital Potentiometers to Mechanical Potentiometers	DS00219
—	Digital Potentiometer Design Guide	DS22017
—	Signal Chain Design Guide	DS21825
—	Analog Solutions for Automotive Applications Design Guide	DS01005

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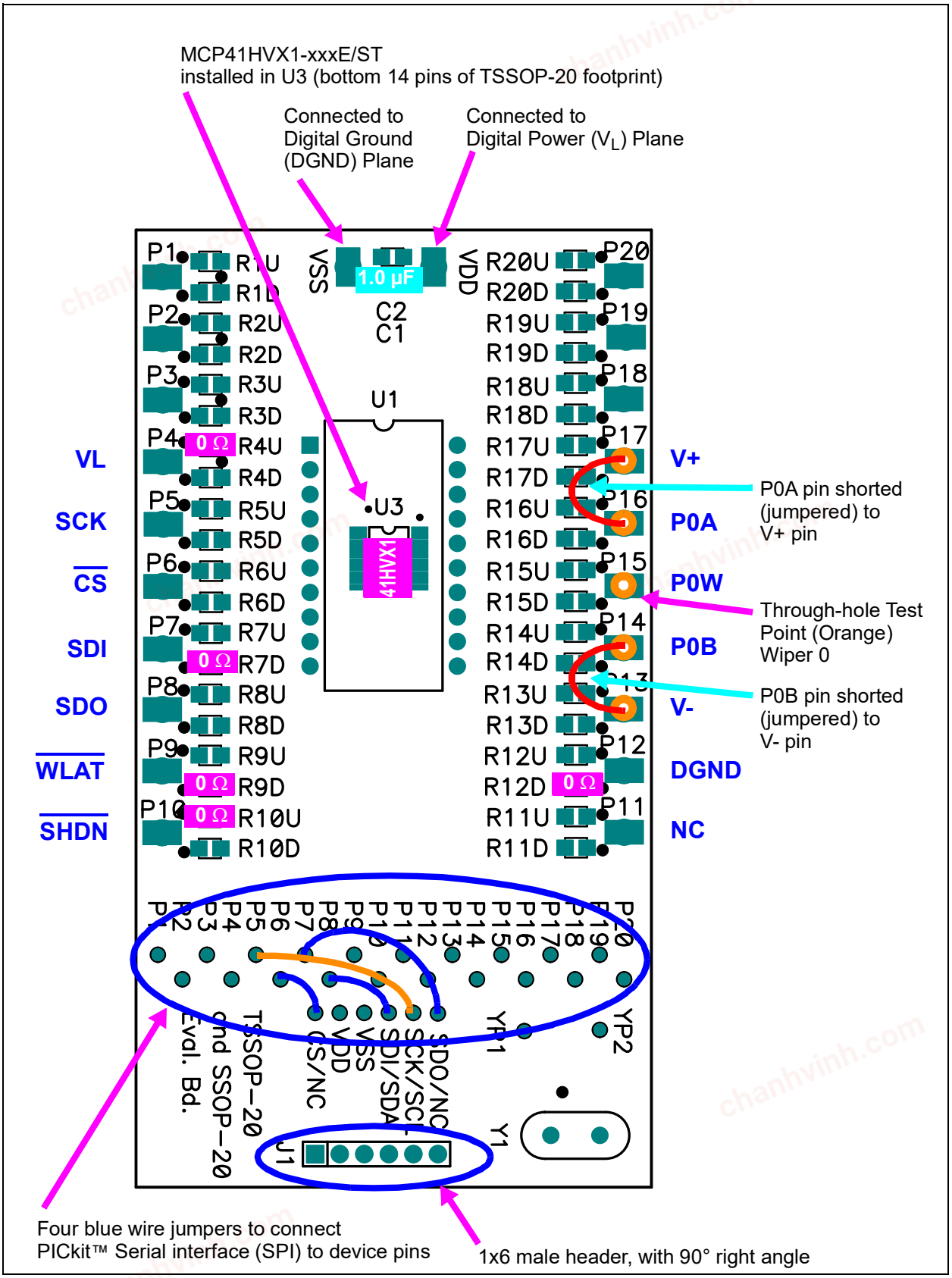


FIGURE 10-1: *Digital Potentiometer Evaluation Board Circuit Using TSSOP20EV.*

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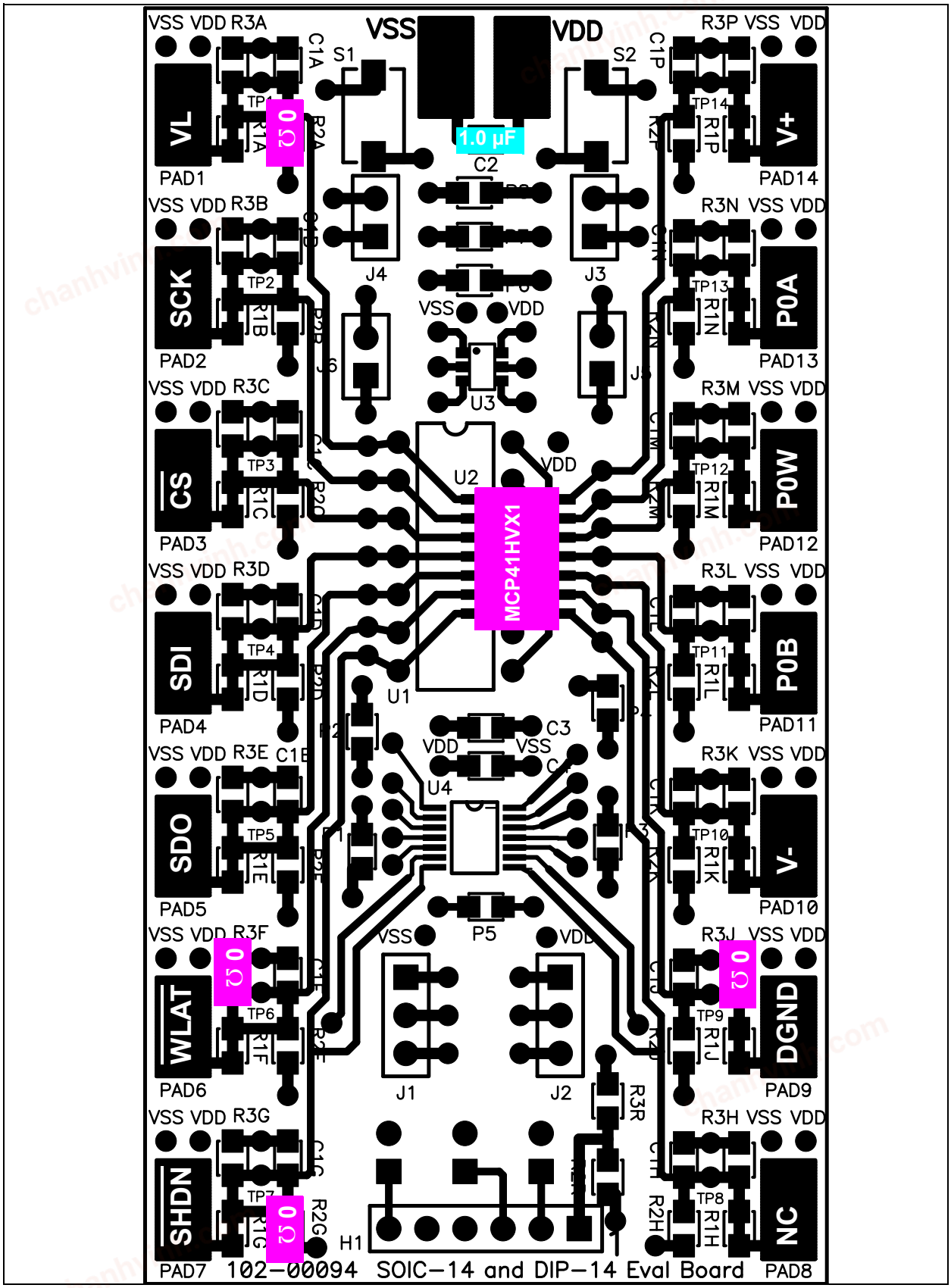


FIGURE 10-2: *Digital Potentiometer Evaluation Board Circuit Using SOIC14EV.*

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NOTES:

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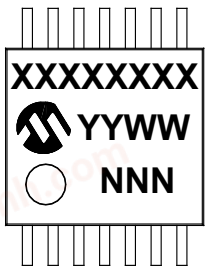
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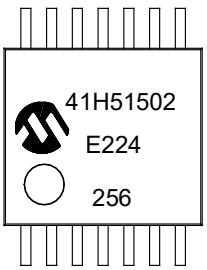
11.0 PACKAGING INFORMATION

11.1 Package Marking Information

14-Lead TSSOP (4.4 mm)

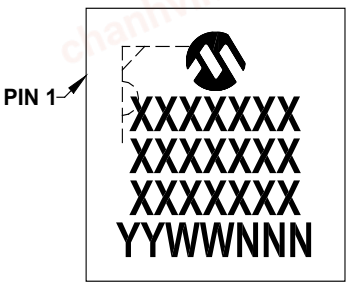


Example

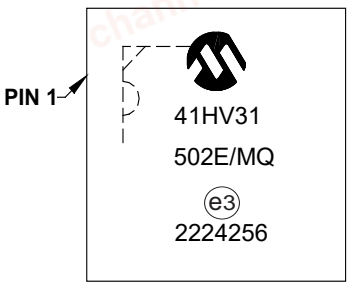


Part Number	Code	Part Number	Code
MCP41HV51-502E/ST	41H51502	MCP41HV31-502E/ST	41H31502
MCP41HV51-103E/ST	41H51103	MCP41HV31-103E/ST	41H31103
MCP41HV51-503E/ST	41H51503	MCP41HV31-503E/ST	41H31503
MCP41HV51-104E/ST	41H51104	MCP41HV31-104E/ST	41H31104

20-Lead VQFN (5x5x0.9 mm)



Example



Part Number	Code	Part Number	Code
MCP41HV51-502E/MQ	502E/MQ	MCP41HV31-502E/MQ	502E/MQ
MCP41HV51-103E/MQ	103E/MQ	MCP41HV31-103E/MQ	103E/MQ
MCP41HV51-503E/MQ	503E/MQ	MCP41HV31-503E/MQ	503E/MQ
MCP41HV51-104E/MQ	104E/MQ	MCP41HV31-104E/MQ	104E/MQ

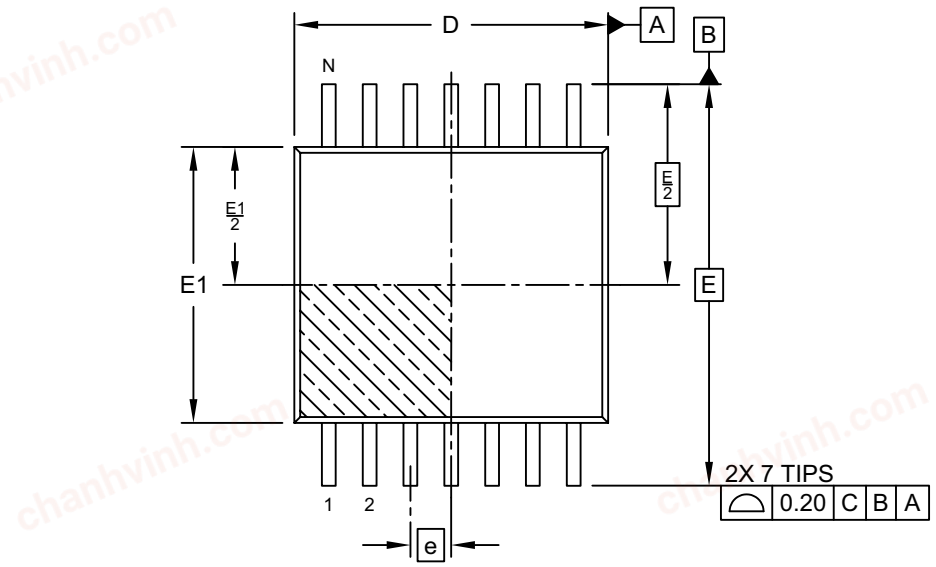
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	RoHS Compliant JEDEC designator for Matte Tin (Sn)
	*	This package is RoHS Compliant. The RoHS Compliant JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

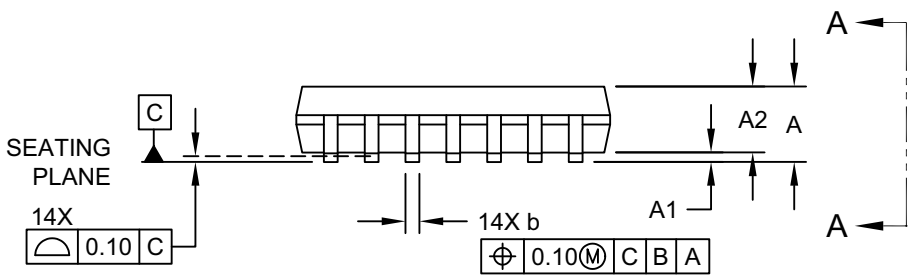
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14-Lead Thin Shrink Small Outline Package [ST] – 4.4 mm Body [TSSOP]

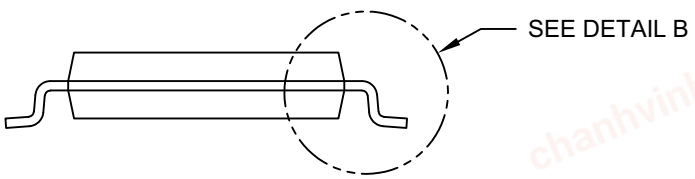
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



VIEW A–A

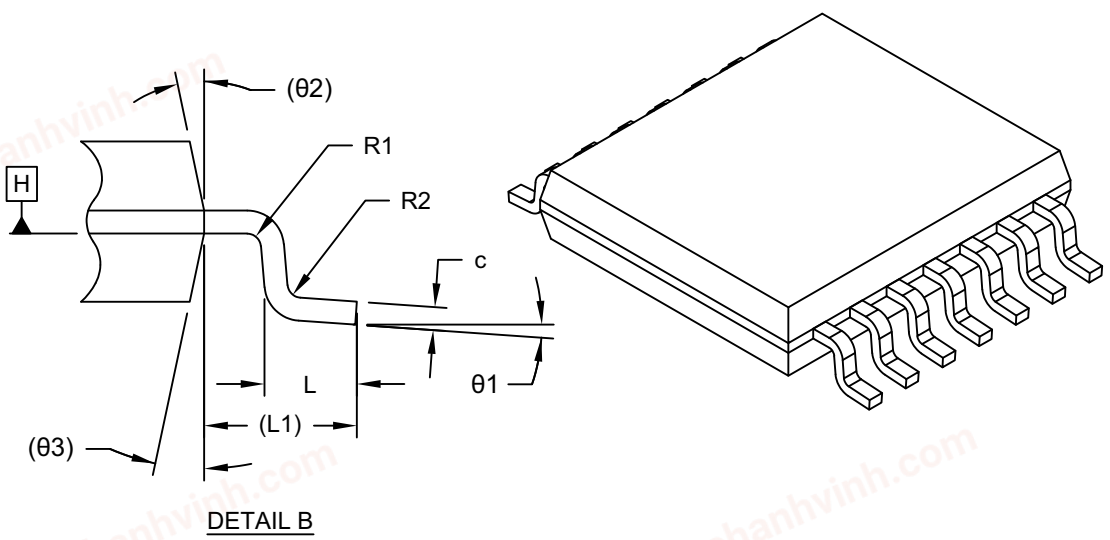
Microchip Technology Drawing C04-087 Rev E Sheet 1 of 2

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14-Lead Thin Shrink Small Outline Package [ST] – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Standoff	A1	0.05	–	0.15
Molded Package Thickness	A2	0.80	1.00	1.05
Overall Length	D	4.90	5.00	5.10
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Terminal Width	b	0.19	–	0.30
Terminal Thickness	c	0.09	–	0.20
Terminal Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Lead Bend Radius	R1	0.09	–	–
Lead Bend Radius	R2	0.09	–	–
Foot Angle	θ1	0°	–	8°
Mold Draft Angle	θ2	–	12° REF	–
Mold Draft Angle	θ3	–	12° REF	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

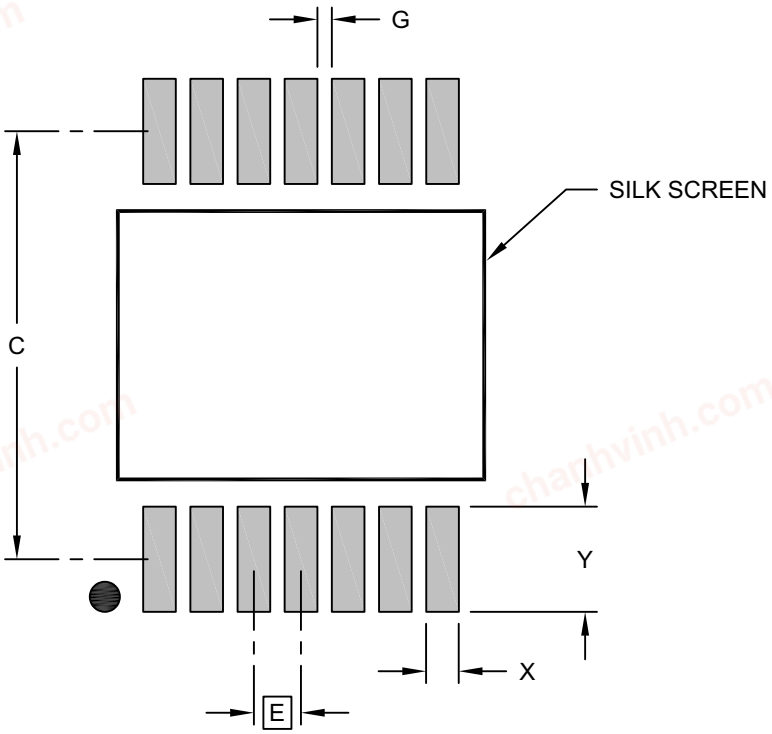
Microchip Technology Drawing C04-087 Rev E Sheet 2 of 2

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14-Lead Thin Shrink Small Outline Package [ST] – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.90	
Contact Pad Width (Xnn)	X			0.45
Contact Pad Length (Xnn)	Y			1.45
Contact Pad to Contact Pad (Xnn)	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

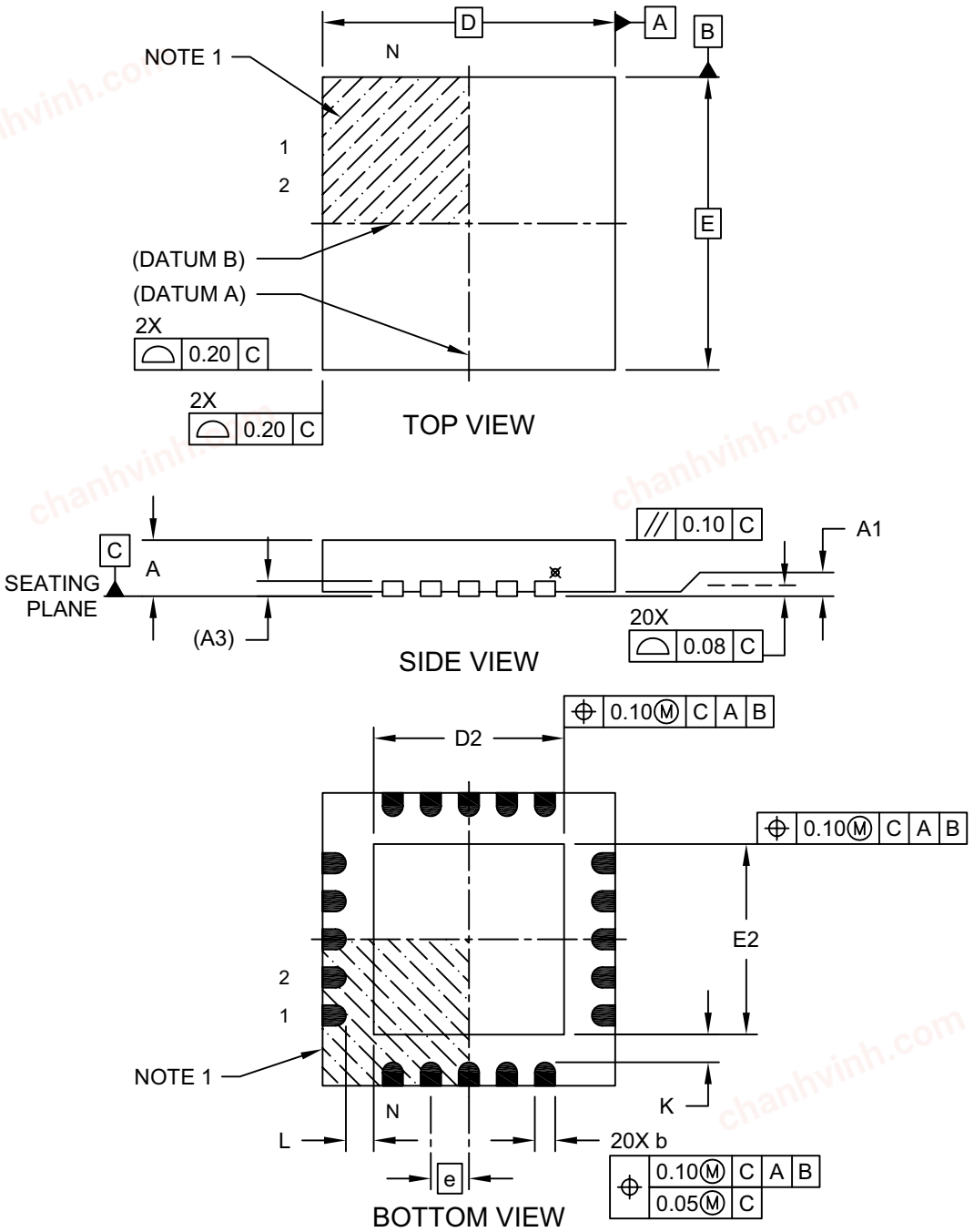
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20-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x1.0 mm Body [VQFN] With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



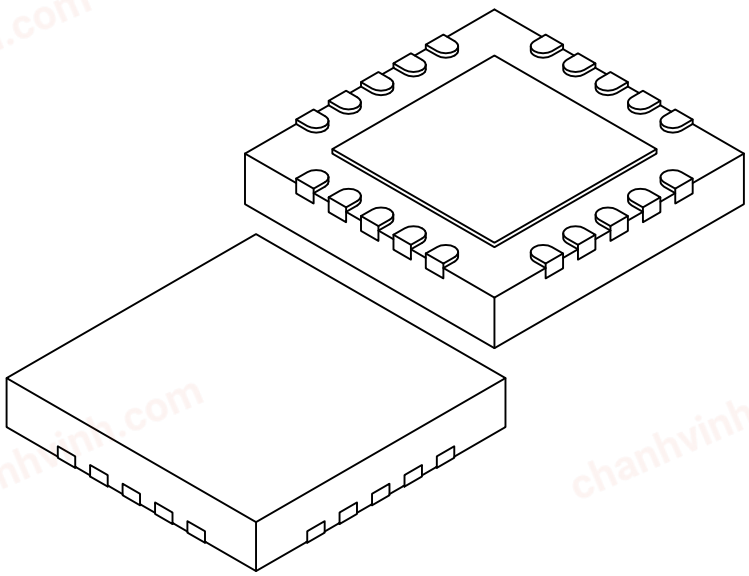
Microchip Technology Drawing C04-139C (MQ) Sheet 1 of 2

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20-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x1.0 mm Body [VQFN] With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	(A3)		0.20 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.15	3.25	3.35
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.15	3.25	3.35
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.35	0.40	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

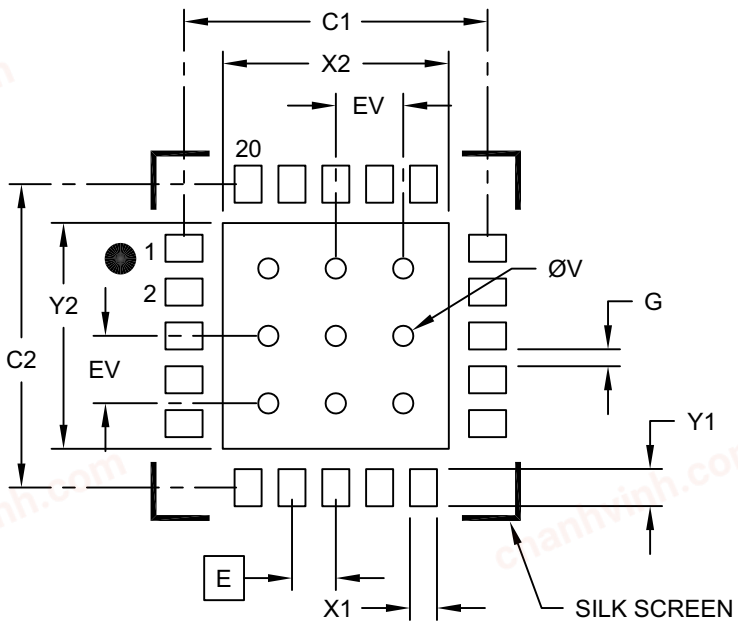
Microchip Technology Drawing C04-139C (MQ) Sheet 2 of 2

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20-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x1.0 mm Body [VQFN] With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			3.35
Optional Center Pad Length	T2			3.35
Contact Pad Spacing	C1		4.50	
Contact Pad Spacing	C2		4.50	
Contact Pad Width (X20)	X1			0.40
Contact Pad Length (X20)	Y1			0.55
Distance Between Pads	G	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2139B (MQ)

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NOTES:

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APPENDIX A: REVISION HISTORY

Revision C (June 2022)

- Updated Table 3-1 with the correct pin description of pins 8 and 9 for the TSSOP package.

Revision B (June 2015)

- Test limits in **Section 1.0 "Electrical Characteristics"** were corrected. The following specifications were updated:
  - **Full-Scale Error**
  - **Zero-Scale Error**
  - **Potentiometer Differential Nonlinearity([10], [17]) (see Appendix B.13)**
  - **Rheostat Integral Nonlinearity([12],[13],[14],[17]) (see Appendix B.5)**
  - **Rheostat Differential Nonlinearity ([12],[13],[14],[17]) (see Appendix B.5)**

Note:	Devices tested after the product marking Date Code of June 30, 2015 are tested to these new limits.

- Corrected the packaging diagram for the VQFN package. The 5 x 5 mm VQFN package is specified, but the 4 x 4 mm QFN package information was shown.
- Updated **Device Features** table to include MCP45HVX1 devices.
- Added **Section 8.10 "Implementing Log Steps with a Linear Digital Potentiometer"**.

Revision A (May 2013)

- Original release of this document.

APPENDIX B: TERMINOLOGY

This appendix discusses the terminology used in this document and describes how a parameter is measured.

B.1 Potentiometer (Voltage Divider)

The potentiometer configuration is when all three terminals of the device are tied to different nodes in the circuit. This allows the potentiometer to output a voltage proportional to the input voltage. This configuration is sometimes called voltage divider mode. The potentiometer is used to provide a variable voltage by adjusting the wiper position between the two endpoints as shown in Figure B-1. Reversing the polarity of the A and B terminals will not affect operation.

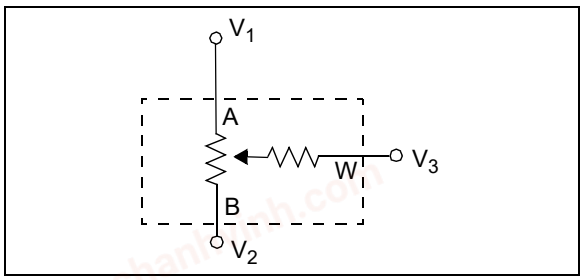


FIGURE B-1: POTENTIOMETER CONFIGURATION.

The temperature coefficient of the R_{AB} resistors is minimal by design. In this configuration, the resistors all change uniformly, so minimal variation should be seen.

B.2 Rheostat (Variable Resistor)

The rheostat configuration is when two of the three digital potentiometer's terminals are used as a resistive element in the circuit. With Terminal W (wiper) and either Terminal A or Terminal B, a variable resistor is created. The resistance will depend on the tap setting of the wiper (and the wiper's resistance). The resistance is controlled by changing the wiper setting. Figure B-2 shows the two possible resistors that can be used. Reversing the polarity of the A and B terminals will not affect operation.

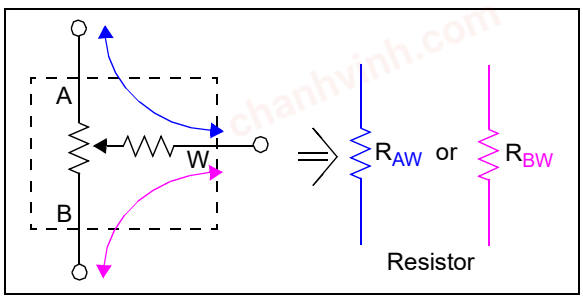


FIGURE B-2: RHEOSTAT CONFIGURATION.

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B.3 Resolution

The resolution is the number of wiper output states that divide the full-scale range. For the 8-bit digital potentiometer, the resolution is 2^8, meaning the digital potentiometer wiper code ranges from 0 to 255.

B.4 Step Resistance (R_S)

The resistance step size (R_S) equates to one LSb of the resistor ladder. Equation B-1 shows the calculation for the step resistance (R_S).

EQUATION B-1: R_S CALCULATION

Ideal

$$R_{S(Ideal)} = \frac{R_{AB}}{2^N - 1} \quad \text{or} \quad \frac{\frac{(V_A - V_B)}{I_{AB}}}{2^N - 1}$$

Measured

$$R_{S(Measured)} = \frac{\frac{(V_{W(@FS)} - V_{W(@ZS)})}{I_{AB}}}{2^N - 1}$$

Where:

$2^N - 1$	=	255 (MCP41HV51/61) 127 (MCP41HV31/41)
V_A	=	Voltage on Terminal A pin
V_B	=	Voltage on Terminal B pin
I_{AB}	=	Measured Current through A and B pins
$V_{W(@FS)}$	=	Measured Voltage on W pin at Full-Scale code (FFh or 7Fh)
$V_{W(@ZS)}$	=	Measured Voltage on W pin at Zero-Scale code (00h)

B.5 Wiper Resistance

Wiper resistance is the series resistance of the analog switch that connects the selected resistor ladder node to the wiper terminal common signal (see Figure 5-1).

A value in the volatile wiper register selects which analog switch to close, connecting the W terminal to the selected node of the resistor ladder.

The resistance is dependent on the voltages on the analog switch source, gate, and drain nodes, as well as the device's wiper code, temperature, and the current through the switch. As the device voltage decreases, the wiper resistance increases.

The wiper resistance is measured by forcing a current through the W and B terminals (I_{WB}) and measuring the voltage on the W and A terminals (V_W and V_A). Equation B-2 shows how to calculate this resistance.

EQUATION B-2: R_W CALCULATION

$$R_{W(Measured)} = \frac{(V_W - V_A)}{I_{WB}}$$

Where:

V_A	=	Voltage on Terminal A pin
V_W	=	Voltage on Terminal W pin
I_{WB}	=	Measured current through W and B pins

The wiper resistance in potentiometer-generated voltage divider applications is not a significant source of error (it does not effect the output voltage seen on the W pin).

The wiper resistance in rheostat applications can create significant nonlinearity as the wiper is moved toward zero scale (00h). The lower the nominal resistance, the greater the possible error.

B.6 R_{ZS} Resistance

The analog switch between the resistor ladder and the Terminal B pin introduces a resistance, which we call the Zero-Scale resistance (R_{ZS}). Equation B-3 shows how to calculate this resistance.

EQUATION B-3: R_{ZS} CALCULATION

$$R_{ZS(Measured)} = \frac{(V_{W(@ZS)} - V_B)}{I_{AB}}$$

Where:

$V_{W(@ZS)}$	=	Voltage on Terminal W pin at Zero-Scale wiper code
V_B	=	Voltage on Terminal B pin
I_{AB}	=	Measured Current through A and B pins

B.7 R_{FS} Resistance

The analog switch between the resistor ladder and the Terminal A pin introduces a resistance, which we call the Full-Scale resistance (R_{FS}). Equation B-4 shows how to calculate this resistance.

EQUATION B-4: R_{FS} CALCULATION

$$R_{FS(Measured)} = \frac{(V_A - V_{W(@FS)})}{I_{AB}}$$

Where:

V_A	=	Voltage on Terminal A pin
$V_{W(@FS)}$	=	Voltage on Terminal W pin at Full-Scale wiper code
I_{AB}	=	Measured Current through A and B pins

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B.8 Least Significant Bit (LSb)

This is the difference between two successive codes (either in resistance or voltage). For a given output range it is divided by the resolution of the device (Equation B-5).

EQUATION B-5: LSb CALCULATION

Ideal

	In Resistance	In Voltage
$LSb(Ideal) =$	$\frac{R_{AB}}{2^N - 1}$	$\frac{V_A - V_B}{2^N - 1}$

Measured

$$LSb(Measured) = \frac{\frac{(V_{W(@FS)} - V_{W(@ZS)})}{I_{AB}}}{2^N - 1} \quad \frac{V_{W(@FS)} - V_{W(@ZS)}}{2^N - 1}$$

Where:

$2^N - 1$	=	255 (MCP41HV51/61) 127 (MCP41HV31/41)
V_A	=	Voltage on Terminal A pin
V_B	=	Voltage on Terminal B pin
V_{AB}	=	Measured Voltage between A and B pins
I_{AB}	=	Measured Current through A and B pins
$V_{W(@FS)}$	=	Measured Voltage on W pin at Full-Scale code (FFh or 7Fh)
$V_{W(@ZS)}$	=	Measured Voltage on W pin at Zero-Scale code (00h)

B.9 Monotonic Operation

Monotonic operation means that the device's output (resistance (R_{BW}) or voltage (V_W)) increases with every one code step (LSb) increment of the wiper register.

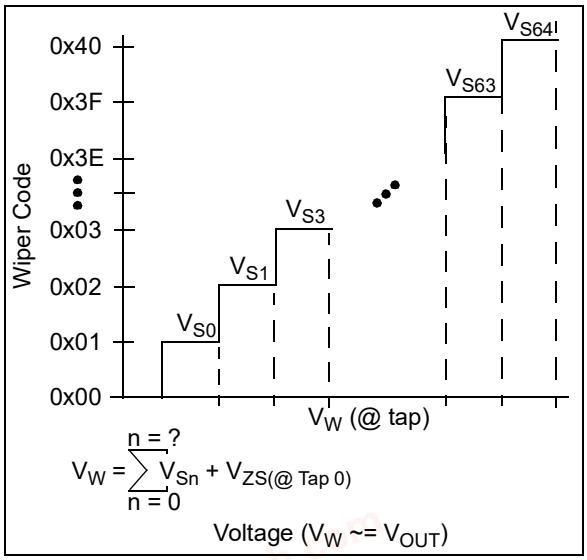


FIGURE B-3: THEORETICAL V_W OUTPUT VS. CODE (MONOTONIC OPERATION).

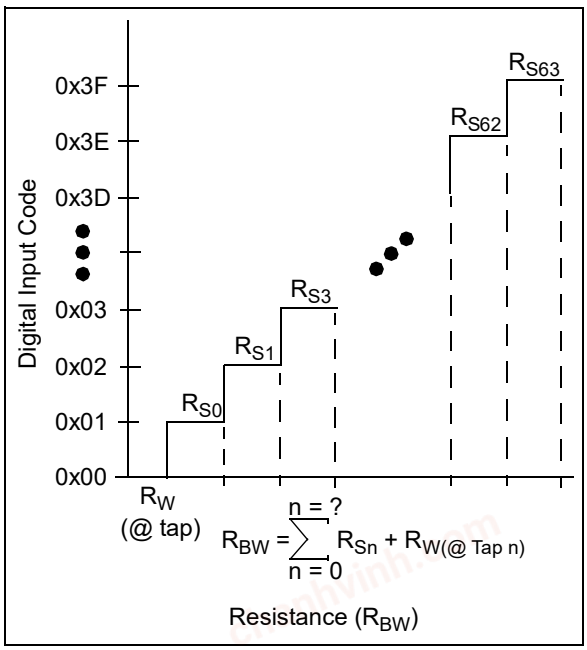


FIGURE B-4: THEORETICAL R_{BW} OUTPUT VS. CODE (MONOTONIC OPERATION).

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B.10 Full-Scale Error (E_{FS})

The Full-Scale Error (see Figure B-5) is the error of the V_W pin relative to the expected V_W voltage (theoretical) for the maximum device wiper register code (code FFh for 8-bit and code 7Fh for 7-bit), see Equation B-6. The error is dependent on the resistive load on the V_{OUT} pin (and where that load is tied to, such as V_{SS} or V_{DD}). For loads (to V_{SS}) greater than specified, the full-scale error will be greater.

The error is determined by the theoretical voltage step size to give an error in LSb.

Note:	Analog switch leakage increases with temperature. This leakage increases substantially at higher temperatures (> ~100°C). As analog switch leakage increases, the full-scale output value decreases, which increases the full-scale error.

EQUATION B-6: FULL-SCALE ERROR

$$E_{FS} = \frac{V_{W(@FS)} - V_A}{V_{LSb(IDEAL)}}$$

Where:

E_{FS}	=	Expressed in LSb
$V_{W@FS)}$	=	The V_W voltage when the wiper register code is at full-scale
$V_{IDEAL(@FS)}$	=	The ideal output voltage when the wiper register code is at full-scale
$V_{LSb(IDEAL)}$	=	The theoretical voltage step size

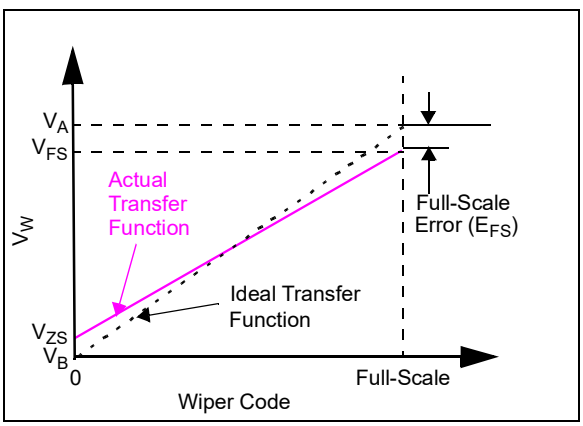


FIGURE B-5: FULL-SCALE ERROR EXAMPLE.

B.11 Zero-Scale Error (E_{ZS})

The Zero-Scale Error (see Figure B-6) is the difference between the ideal and measured V_{OUT} voltage with the Wiper register code equal to 00h (Equation B-7). The error is dependent on the resistive load on the V_{OUT} pin (and where that load is tied to, such as V_{SS} or V_{DD}). For loads (to V_{DD}) greater than specified, the zero-scale error will be greater.

The error is determined by the theoretical voltage step size to give an error in LSb.

Note:	Analog switch leakage increases with temperature. This leakage increases substantially at higher temperatures (> ~100°C). As analog switch leakage increases the zero-scale output value decreases, which decreases the zero-scale error.

EQUATION B-7: ZERO SCALE ERROR

$$E_{ZS} = \frac{V_{W(@ZS)}}{V_{LSb(IDEAL)}}$$

Where:

E_{FS}	=	Expressed in LSb
$V_{W@ZS)}$	=	the V_W voltage when the wiper register code is at zero-scale
$V_{LSb(IDEAL)}$	=	the theoretical voltage step size

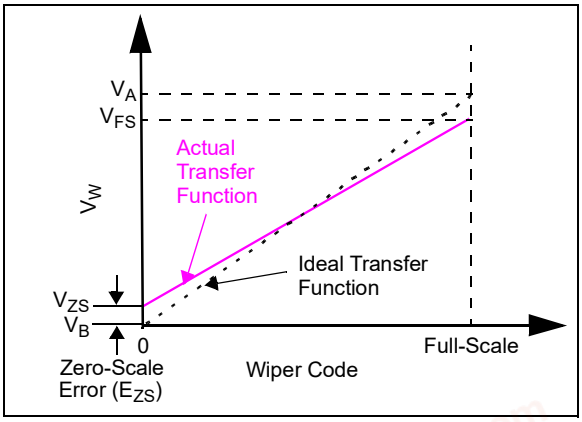


FIGURE B-6: ZERO-SCALE ERROR EXAMPLE.

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B.12 Integral Nonlinearity (P-INL) Potentiometer Configuration

The Potentiometer Integral nonlinearity (P-INL) error is the maximum deviation of an actual V_W transfer function from an ideal transfer function (straight line).

In the MCP41HVX1, P-INL is calculated using the zero-scale and full-scale wiper code end points. P-INL is expressed in LSb. P-INL is also called relative accuracy. Equation B-8 shows how to calculate the P-INL error in LSb, and Figure B-7 shows an example of P-INL accuracy.

Positive P-INL means higher V_W voltage than ideal. Negative P-INL means lower V_W voltage than ideal.

Note:	Analog switch leakage increases with temperature. This leakage increases substantially at higher temperatures (> ~100°C). As analog switch leakage increases, the wiper output voltage (V_W) decreases, which affects the INL Error.

EQUATION B-8: P-INL ERROR

$$E_{INL} = \frac{(V_{W(@Code)} - (V_{LSb(Measured)} \times Code))}{V_{LSb(Measured)}}$$

Where:

INL	=	Expressed in LSb
Code	=	Wiper Register Value
$V_{W(@Code)}$	=	The measured V_W output voltage with a given Wiper register code
V_{LSb}	=	For Ideal: V_{AB} /Resolution For Measured: ($V_{W(@FS)}$ - $V_{W(@ZS)}$)/255

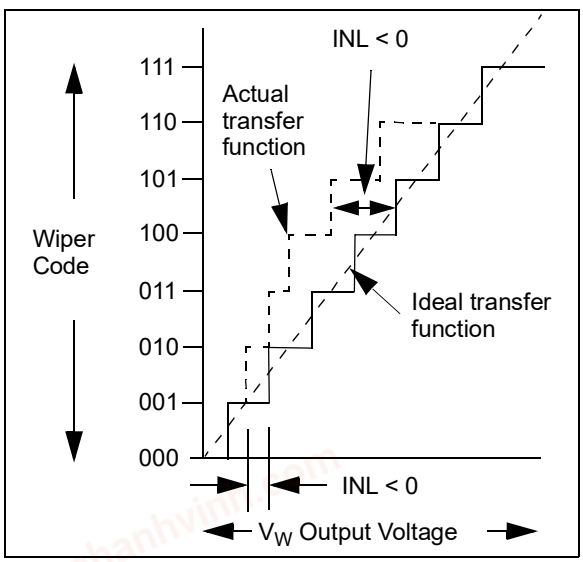


FIGURE B-7: P-INL ACCURACY.

B.13 Differential Nonlinearity (P-DNL) Potentiometer Configuration

The Potentiometer Differential nonlinearity (P-DNL) error (see Figure B-8) is the measure of V_W step size between codes. The ideal step size between codes is 1 LSb. A P-DNL error of zero would imply that every code is exactly 1 LSb wide. If the P-DNL error is less than 1 LSb, the Digital Potentiometer guarantees monotonic output and no missing codes. The P-DNL error between any two adjacent codes is calculated in Equation B-9.

P-DNL error is the measure of variations in code widths from the ideal code width.

Note:	Analog switch leakage increases with temperature. This leakage increases substantially at higher temperatures (> ~100°C). As analog switch leakage increases, the wiper output voltage (V_W) decreases, which affects the DNL Error.

EQUATION B-9: P-DNL ERROR

$$E_{DNL} = \frac{(V_{W(code=n+1)} - V_{W(code=n)} - V_{LSb(Measured)})}{V_{LSb(Measured)}}$$

Where:

DNL	=	Expressed in LSb
$V_{W(Code = n)}$	=	The measured V_W output voltage with a given Wiper register code
V_{LSb}	=	For Ideal: V_{AB} /Resolution For Measured: ($V_{W(@FS)}$ - $V_{W(@ZS)}$)/# of R_S

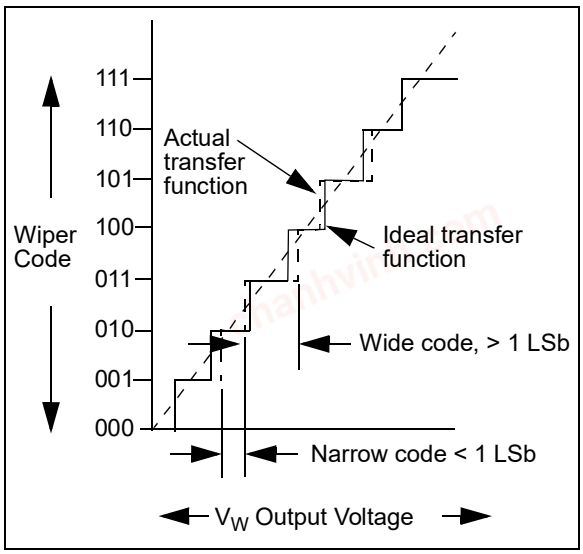


FIGURE B-8: P-DNL ACCURACY.

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B.14 Integral Nonlinearity (R-INL) Rheostat Configuration

The Rheostat Integral nonlinearity (R-INL) error is the maximum deviation of an actual R_{BW} transfer function from an ideal transfer function (straight line).

In the MCP41HVX1, INL is calculated using the Zero-Scale and Full-Scale wiper code end points. R-INL is expressed in LSb. R-INL is also called relative accuracy. Equation B-10 shows how to calculate the R-INL error in LSb and Figure B-9 shows an example of R-INL accuracy.

Positive R-INL means higher V_{OUT} voltage than ideal. Negative R-INL means lower V_{OUT} voltage than ideal.

EQUATION B-10: R-INL ERROR

$$E_{INL} = \frac{(R_{BW(@code)} - R_{BW(Ideal)})}{R_{LSb(Ideal)}}$$

Where:

INL = Expressed in LSb

$R_{BW(Code = n)}$ = The measured R_{BW} resistance with a given wiper register code

R_{LSb} = For Ideal: R_{AB} /Resolution
For Measured: $R_{BW(@FS)}$ /# of R_S

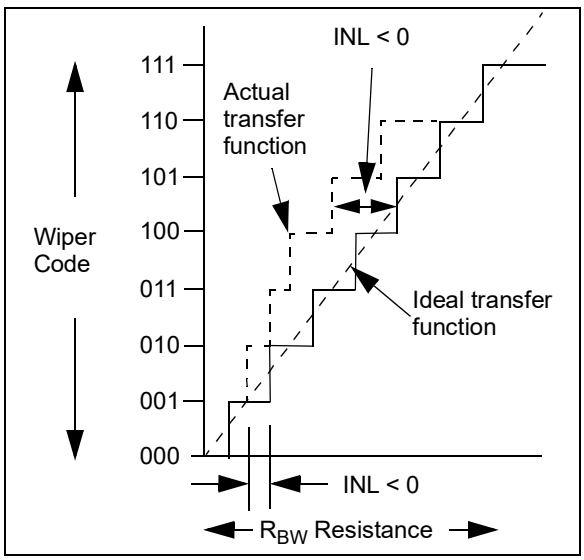


FIGURE B-9: R-INL ACCURACY.

B.15 Differential Nonlinearity (R-DNL) Rheostat Configuration

The Rheostat Differential nonlinearity (R-DNL) error (see Figure B-10) is the measure of R_{BW} step size between codes in actual transfer function. The ideal step size between codes is 1 LSb. A R-DNL error of zero would imply that every code is exactly 1 LSb wide. If the R-DNL error is less than 1 LSb, the R_{BW} Resistance guarantees monotonic output and no missing codes. The R-DNL error between any two adjacent codes is calculated in Equation B-11.

R-DNL error is the measure of variations in code widths from the ideal code width. A R-DNL error of zero would imply that every code is exactly 1 LSb wide.

EQUATION B-11: R-DNL ERROR

$$E_{DNL} = \frac{((V_{OUT(code = n + 1)} - V_{OUT(code = n)}) - V_{LSb(Measured)})}{V_{LSB(Measured)}}$$

Where:

DNL = Expressed in LSb

$R_{BW(Code = n)}$ = The measured R_{BW} resistance with a given wiper register code

R_{LSb} = For Ideal: R_{AB} /Resolution
For Measured: $R_{BW(@FS)}$ /# of R_S

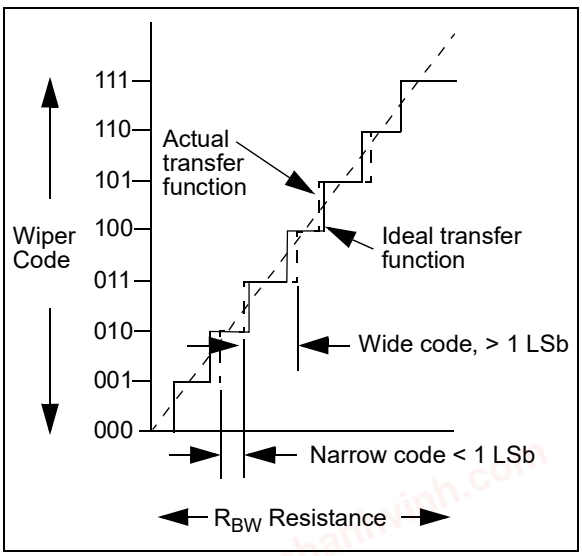


FIGURE B-10: R-DNL ACCURACY.

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B.16 Total Unadjusted Error (E_T)

The Total Unadjusted Error (E_T) is the difference between the ideal and measured V_W voltage. Typically, calibration of the output voltage is implemented to improve system performance.

The error in bits is determined by the theoretical voltage step size to give an error in LSb.

Equation B-12 shows the Total Unadjusted Error calculation.

Note: Analog switch leakage increases with temperature. This leakage increases substantially at higher temperatures (> ~100°C).
As analog switch leakage increases, the wiper output voltage (V_W) decreases, which affects the total Unadjusted Error.

EQUATION B-12: TOTAL UNADJUSTED ERROR CALCULATION

$$E_T = \frac{(V_{W_Actual(@code)} - V_{W_Ideal(@Code)})}{V_{LSb(Ideal)}}$$

Where:

E_T = Expressed in LSb

$V_{W_Actual(@code)}$ = The measured W pin output voltage at the specified code

$V_{W_Ideal(@code)}$ = The calculated W pin output voltage at the specified code (code × $V_{LSb(Ideal)}$)

$V_{LSb(Ideal)}$ = V_{AB}/# R_S
8-bit = V_{AB}/255
7-bit = V_{AB}/127

B.17 Settling Time

The settling time is the time delay required for the V_W voltage to settle into its new output value. This time is measured from the start of code transition to when the V_W voltage is within the specified accuracy. It is related to the RC characteristics of the resistor ladder and wiper switches.

In the MCP41HVX1, the settling time is a measure of the time delay until the V_W voltage reaches within 0.5 LSb of its final value, when the volatile wiper register changes from zero-scale to full-scale (or full-scale to zero-scale).

B.18 Major-Code Transition Glitch

Major-code transition glitch is the impulse energy injected into the Wiper pin when the code in the Wiper register changes state. It is normally specified as the area of the glitch in nV-Sec, and is measured when the digital code is changed by 1 LSb at the major carry transition (Example: `01111111` to `10000000`, or `10000000` to `01111111`).

B.19 Digital Feedthrough

The Digital feedthrough is the glitch that appears at the analog output caused by coupling from the digital input pins of the device. The area of the glitch is expressed in nV-Sec, and is measured with a full-scale change (Example: all `0`s to all `1`s and vice versa) on the digital input pins. The digital feedthrough is measured when the digital potentiometer is not being written to the output register.

B.20 Power-Supply Sensitivity (PSS)

PSS indicates how the output (V_W or R_{BW}) of the digital potentiometer is affected by changes in the supply voltage. PSS is the ratio of the change in V_W to a change in V_{DD} for mid-scale output of the digital potentiometer. The V_W is measured while the V_{DD} is varied from 5.5V to 2.7V as a step, and expressed in %/%, which is the % change of the V_W output voltage with respect to the % change of the V_{DD} voltage.

EQUATION B-13: PSS CALCULATION

$$PSS = \frac{\frac{(V_{W(@5.5V)} - V_{W(@27V)})}{V_{W(@5.5V)}}}{\frac{(5.5V - 2.7V)}{5.5V}}$$

Where:

PSS = Expressed in %/%

$V_{W(@5.5V)}$ = The measured V_W output voltage with V_{DD} = 5.5V

$V_{W(@2.7V)}$ = The measured V_W output voltage with V_{DD} = 2.7V

B.21 Power-Supply Rejection Ratio (PSRR)

PSRR indicates how the output of the digital potentiometer is affected by changes in the supply voltage. PSRR is the ratio of the change in V_W to a change in V_{DD} for full-scale output of the digital potentiometer. The V_W is measured while the V_{DD} is varied ±10% (V_A and V_B voltages held constant), and expressed in dB or µV/V.

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B.22 Ratiometric Temperature Coefficient

The ratiometric temperature coefficient quantifies the error in the ratio R_{AW}/R_{WB} due to temperature drift. This is typically the critical error when using a digital potentiometer in a voltage divider configuration.

B.23 Absolute Temperature Coefficient

The absolute temperature coefficient quantifies the error in the end-to-end resistance (Nominal resistance R_{AB}) due to temperature drift. This is typically the critical error when using the device in an adjustable resistor configuration.

Characterization curves of the resistor temperature coefficient (Tempco) are shown in **Section 2.0 "Typical Performance Curves"**.

B.24 -3 dB Bandwidth

This is the frequency of the signal at the A terminal that causes the voltage at the W pin to be -3 dB from its expected value, based on its wiper code. The expected value is determined by the static voltage value on the A Terminal and the wiper-code value. The output decreases due to the RC characteristics of the resistor network.

B.25 Resistor Noise Density (e_{N_WB})

This is the random noise generated by the device's internal resistances. It is specified as a spectral density (voltage per square root Hertz).

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XXX	X	/XX
Device	Resistance Version	Temperature Range	Package

Device:
- MCP41HV31: Single Potentiometer (7-bit) with SPI Interface
- MCP41HV31T: Single Potentiometer (7-bit) with SPI Interface (Tape and Reel)
- MCP41HV51: Single Potentiometer (8-bit) with SPI Interface
- MCP41HV51T: Single Potentiometer (8-bit) with SPI Interface (Tape and Reel)

Resistance Version:
- 502 = 5 kΩ
- 103 = 10 kΩ
- 503 = 50 kΩ
- 104 = 100 kΩ

Temperature Range:
- E = -40°C to +125°C

Package:
- ST = 14-Lead Plastic Thin Shrink Small Outline, 4.4 mm Body
- MQ = 20-Lead Plastic Quad Flat, No Lead Package, 5 x 5 x 0.9 mm Body

Examples:

a) MCP41HV51T-502E/ST
5 kΩ, 8-bit, 14-LD TSSOP

b) MCP41HV51T-103E/ST
10 kΩ, 8-bit, 14-LD TSSOP

c) MCP41HV31T-503E/ST
50 kΩ, 7-bit, 14-LD TSSOP

d) MCP41HV31T-104E/MQ
100 kΩ, 7-bit, 20-LD VQFN (5x5)

a) MCP41HV51T-502E/MQ
5 kΩ, 8-bit, 20-LD VQFN (5x5)

b) MCP41HV51T-103E/MQ
10 kΩ, 8-bit, 20-LD VQFN (5x5)

c) MCP41HV31T-503E/MQ
50 kΩ, 7-bit, 20-LD VQFN (5x5)

d) MCP41HV31T-104E/MQ
100 kΩ, 7-bit, 20-LD VQFN (5x5)

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