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MCP1711

150 mA Ultra-Low Quiescent Current, Capacitorless LDO Regulator

Features

- Low Quiescent Current: 600 nA
- Input Voltage Range: 1.4V to 6.0V
- Standard Output Voltages: 1.2V, 1.8V, 1.9V, 2.0V, 2.2V, 2.5V, 3.0V, 3.3V, 5.0V
- Output Accuracy: ±20 mV for 1.2V and 1.8V Options and ±1% for $V_R \geq 2.0V$
- Temperature Stability: ±50 ppm/°C
- Maximum Output Current: 150 mA
- Low ON Resistance: 3.3Ω @ V_R = 3.0V
- Standby Current: 10 nA
- Protection Circuits: Current Limiter, Short Circuit, Foldback
- $\overline{SHDN}$ Pin Function: ON/OFF Logic = Enable High
- C_{OUT} Discharge Circuit when SHDN Function is Active
- Output Capacitor: Low Equivalent Series Resistance (ESR) Ceramic, Capacitorless Compatible
- Operating Temperature: -40°C to +85°C (Industrial)
- Available Packages:
  - 4-Lead 1 x 1 mm UQFN
  - 5-Lead SOT-23
- Environmentally Friendly: EU RoHS Compliant, Lead-Free

Applications

- Energy Harvesting
- Long-Life, Battery-Powered Applications
- Portable Electronics
- Ultra-Low Consumption “Green” Products
- Mobile Devices/Terminals
- Wireless LAN
- Modules (Wireless, Cameras)

Related Literature

- **AN765**, *Using Microchip’s Micropower LDOs* (DS00765), Microchip Technology Inc.
- **AN766,** *Pin-Compatible CMOS Upgrades to Bipolar LDOs* (DS00766), Microchip Technology Inc.
- **AN792,** *A Method to Determine How Much Power a SOT23 Can Dissipate in an Application* (DS00792), Microchip Technology Inc.

General Description

The MCP1711 is a highly accurate CMOS low dropout (LDO) voltage regulator that can deliver up to 150 mA of current while consuming only 0.6 µA of quiescent current (typical). The input operating range is specified from 1.4V to 6.0V, making it an ideal choice for mobile applications and one-cell Li-Ion powered applications.

The MCP1711 is capable of delivering 150 mA output current with only 0.32V (typical) for V_R = 5.0V, and 1.41V (typical) for V_R = 1.2V of input-to-output voltages differential. The output voltage accuracy of the MCP1711 is typically ± 0.02V for $V_R < 2.0V$ and ±1% for $V_R \geq 2.0V$ at +25°C. The temperature stability is approximately ±50 ppm/°C. Line regulation is ±0.01%/V typical at +25°C.

The output voltages available for the MCP1711 range from 1.2V to 5.0V. The LDO output is stable even if an output capacitor is not connected, due to an excellent internal phase compensation. However, for better transient responses, the output capacitor should be added. The MCP1711 is compatible with low ESR ceramic output capacitors.

Overcurrent limit and short-circuit protection embedded into the device provide a robust solution for any application.

The MCP1711 has a true current foldback feature. When the load decreases beyond the MCP1711 load rating, the output current and output voltage will foldback toward 80 mA (typical) at approximately 0V output. When the load impedance increases and returns to the rated load, the MCP1711 will follow the same foldback curve as the device comes out of current foldback.

If the device is in Shutdown mode, by inputting a low-level signal to the $\overline{SHDN}$ pin, the current consumption is reduced to less than 0.1 µA (typically 0.01 µA). In Shutdown mode, if the output capacitor is used, it will be discharged via the internal dedicated switch and, as a result, the output voltage quickly returns to 0V.

The package options for the MCP1711 are the 4-lead 1 x 1 mm UQFN and the 5-lead SOT-23, which make the device ideal for small and compact applications.

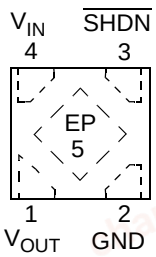
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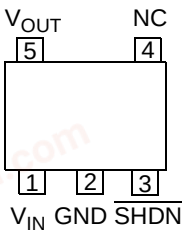
MCP1711

Package Types

MCP1711
1x1 UQFN*
Top View



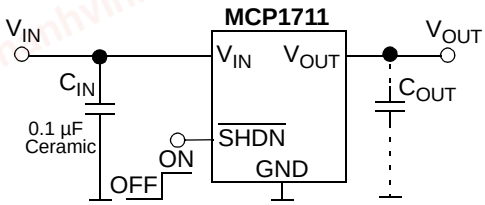
MCP1711
SOT-23
Top View



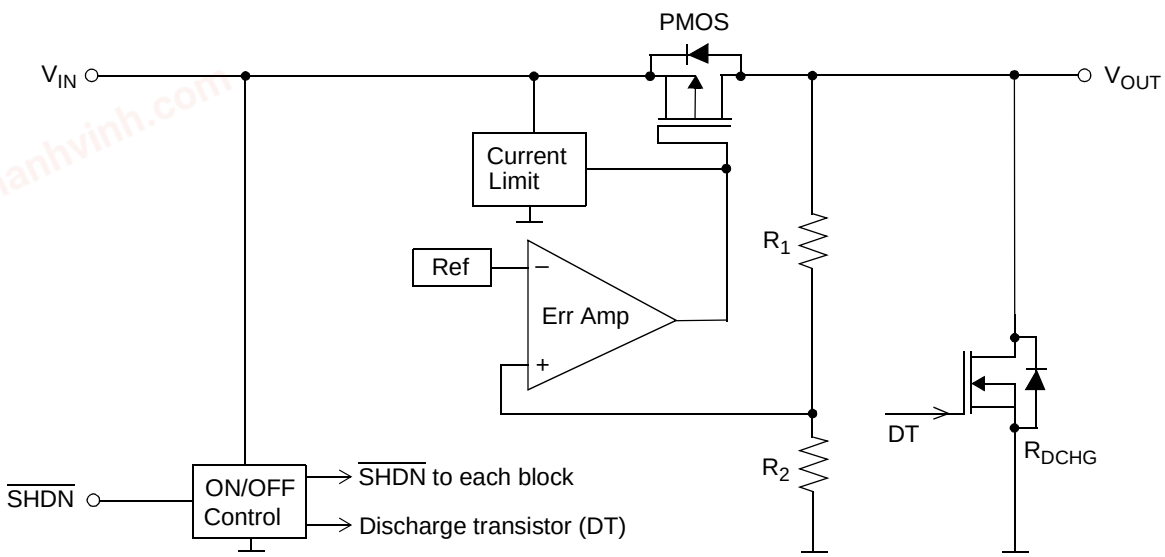
* Includes Exposed Thermal Pad (EP); see Table 3-1

Typical Application Circuit

MCP1711
1x1 UQFN and SOT-23



Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Input Voltage, V_{IN} ..... +6.5V
V_{IN}, $\overline{SHDN}$ ..... -0.3V to +6.5V
Output Current, I_{OUT} (1) ..... 470 mA
Output Voltage, V_{OUT} (2) ..... -0.3V to V_{IN} + 0.3V or +6.5V
Power Dissipation
5-Lead SOT-23 ..... 600 mW (JEDEC 51-7 FR-4 board with thermal vias) or 250 mW (3)
4-Lead 1 x 1 mm UQFN ..... 550 mW (JEDEC 51-7 FR-4 board with thermal vias) or 100 mW (3)
Storage Temperature ..... -55°C to +125°C
Operating Ambient Temperature ..... -40°C to +85°C
ESD Protection on all pins ..... ±1 kV HBM, ±200V MM

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Provided that the device is used in the range of $I_{OUT} \le P_D/(V_{IN} - V_{OUT})$.

2: The maximum rating corresponds to the lowest value between V_{IN} + 0.3V or +6.5V.

3: The device is mounted on one layer PCB with minimal copper that does not provide any additional cooling.

DC CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, $V_{\overline{SHDN}} = V_{IN}$, I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 0 µF, V_{IN} = 3.5V for V_R < 2.5V and $V_{IN} = V_R$ + 1V for $V_R \ge$ 2.5V, T_A = +25°C

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input-Output Characteristics						
Input Voltage	V_{IN}	1.4	—	6.0	V	I_{OUT} = 1 µA
Output Voltage	V_{OUT}	V_R - 0.02	V_R	V_R + 0.02	V	V_R < 2.0V
		V_R x 0.99	V_R	V_R x 1.01		$V_R \ge$ 2.0V
Maximum Output Current	I_{OUT}	150	—	—	mA	
Load Regulation	ΔV_{OUT}	-16	±3	+16	mV	1 µA ≤ I_{OUT} ≤ 1 mA
		-50	±17	+50		1 mA ≤ I_{OUT} ≤ 150 mA
Dropout Voltage (1)	$V_{DROPOUT1}$	—	V_{DROP1} (2)		V	I_{OUT} = 50 mA
	$V_{DROPOUT2}$	—	V_{DROP2} (2)			I_{OUT} = 150 mA
Input Quiescent Current	I_q	—	0.60	1.27	µA	V_R < 1.9V
		—	0.65	1.50		1.9V ≤ V_R < 4.0V
		—	0.80	1.80		$V_R \ge$ 4.0V
Input Quiescent Current for SHDN mode	$I_{\overline{SHDN}}$	—	0.01	0.10	µA	V_{IN} = 6.0V $V_{\overline{SHDN}} = V_{IN}$
Line Regulation	$\Delta V_{OUT}/(\Delta V_{IN} \times V_{OUT})$	-0.13	±0.01	+0.13	%/V	I_{OUT} = 1 µA V_R + 0.5V ≤ V_{IN} ≤ 6.0V
		-0.19	±0.01	+0.19		I_{OUT} = 1 mA VR ≥ 1.2V, V_R + 0.5V ≤ V_{IN} ≤ 6.0V

Note 1: The dropout voltage is defined as the input to output differential at which the output voltage drops 2% below the output voltage value that was measured with an applied input voltage of $V_{IN} = V_R$ + 1V.

2: V_{DROP1}, V_{DROP2}: Dropout Voltage (Refer to the DC Characteristics Voltage Table).

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DC CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, $V_{\overline{SHDN}} = V_{IN}$, I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 0 µF, V_{IN} = 3.5V for V_R < 2.5V and $V_{IN} = V_R$ + 1V for $V_R \geq$ 2.5V, T_A = +25°C

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output Voltage Temperature Stability	$\Delta V_{OUT}/(\Delta T \times V_{OUT})$	—	±50	—	ppm/°C	I_{OUT} = 10 mA -40°C ≤ T_A ≤ +85°C
Current Limit	I_{LIMIT}	150	270	—	mA	$V_{OUT} = 0.95 \times V_R$
Output Short-Circuit Foldback Current	I_{OUT_SC}	—	80	—	mA	V_{OUT} = GND
C_{OUT} Auto-Discharge Resistance	R_{DCHG}	280	450	640	Ω	$\overline{SHDN}$ = GND $V_{OUT} = V_R$
Noise	e_n	—	30	—	µV(rms)	$C_{IN} = C_{OUT}$ = 1 µF, I_{OUT} = 50 mA, f = 10 Hz to 100 kHz
Shutdown Input						
SHDN Logic High Input Voltage	$V_{\overline{SHDN}\text{-HIGH}}$	0.91	—	6.00	V	
SHDN Logic Low Input Voltage	$V_{\overline{SHDN}\text{-LOW}}$	0	—	0.38	V	
SHDN High-Level Current	$I_{\overline{SHDN}\text{-HIGH}}$	-0.1	—	+0.1	µA	V_{IN} = 6.0V
SHDN Low-Level Current	$I_{\overline{SHDN}\text{-LOW}}$	-0.1	—	+0.1	µA	V_{IN} = 6.0V $\overline{SHDN}$ = GND

Note 1: The dropout voltage is defined as the input to output differential at which the output voltage drops 2% below the output voltage value that was measured with an applied input voltage of $V_{IN} = V_R$ + 1V.

2: V_{DROP1}, V_{DROP2}: Dropout Voltage (Refer to the DC Characteristics Voltage Table).

DC CHARACTERISTICS VOLTAGE TABLE

Nominal Output Voltage	Output Voltage (V)		Dropout Voltage (V)			
	V_{OUT}		V_{DROP1}	V_{DROP1}	V_{DROP2}	V_{DROP2}
V_R (V)	Min.	Max.	Typ.	Max.	Typ.	Max.
1.2	1.1800	1.2200	0.87	1.23	1.41	1.93
1.8	1.7800	1.8200	0.47	0.72	0.99	1.40
1.9	1.8800	1.9200	0.42	0.64	0.92	1.29
2.0	1.9800	2.0200	0.37	0.58	0.86	1.20
2.2	2.1780	2.2220	0.31	0.47	0.75	1.05
2.5	2.4750	2.5250	0.26	0.40	0.67	0.92
3.0	2.9700	3.0300	0.17	0.26	0.50	0.67
3.3	3.2670	3.3330	0.17	0.26	0.50	0.67
5.0	4.9500	5.0500	0.10	0.16	0.32	0.43

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TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Ambient Temperature Range	T_A	-40	—	+85	°C	
Junction Operating Temperature	T_J	-40	—	+125	°C	
Storage Temperature Range	T_A	-55	—	+125	°C	
Package Thermal Resistances						
Thermal Resistance, 1 x 1 UQFN-4Ld	θ_{JA}	—	181.82	—	°C/W	JEDEC 51-7 FR4 board with thermal vias
	θ_{JA}	—	1000	—	°C/W	Note 2
	θ_{JC}	—	15	—	°C/W	
Thermal Resistance, SOT-23-5Ld	θ_{JA}	—	166.67	—	°C/W	JEDEC 51-7 FR4 board with thermal vias
	θ_{JA}	—	400	—	°C/W	Note 2
	θ_{JC}	—	81	—	°C/W	

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature, and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2: The device is mounted on one layer PCB with minimal copper that does not provide any additional cooling.

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2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

NOTE: Unless otherwise indicated, V_{IN} = 3.5V for V_R < 2.5V or V_{IN} = V_R + 1V for $V_R \geq$ 2.5V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 0 µF, $V_{\overline{SHDN}}$ = V_{IN}, T_A = +25°C.

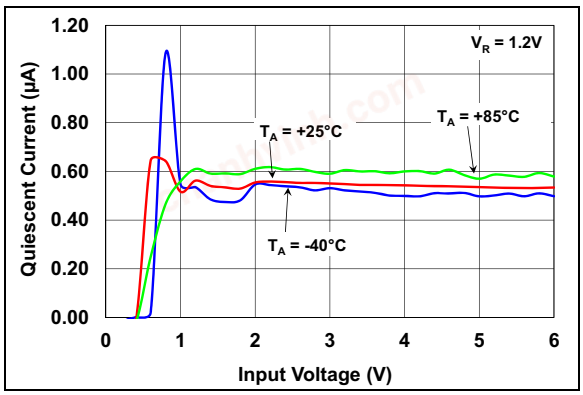


FIGURE 2-1: *Quiescent Current vs. Input Voltage.*

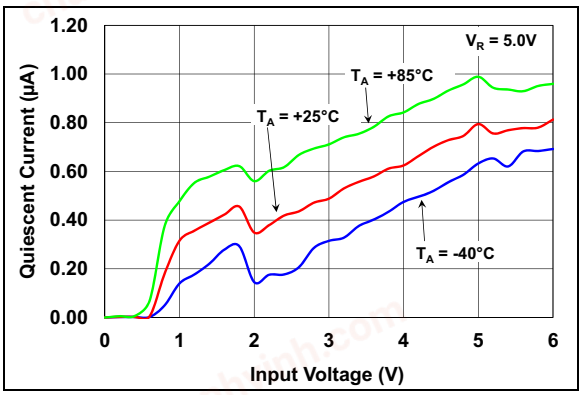


FIGURE 2-4: *Quiescent Current vs. Input Voltage.*

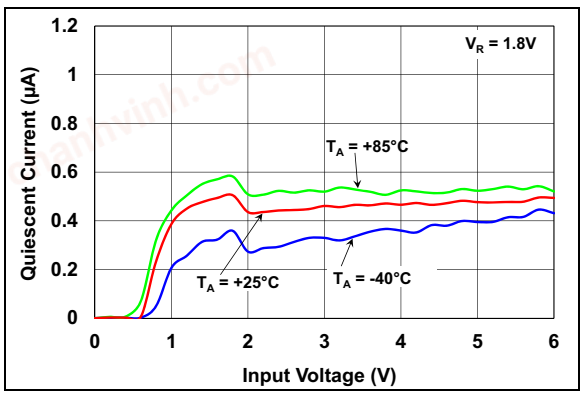


FIGURE 2-2: *Quiescent Current vs. Input Voltage.*

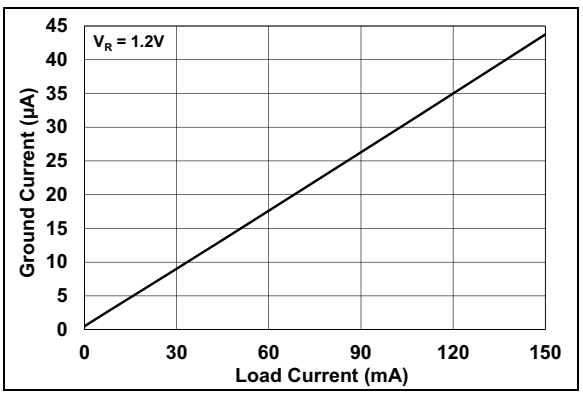


FIGURE 2-5: *Ground Current vs. Load Current.*

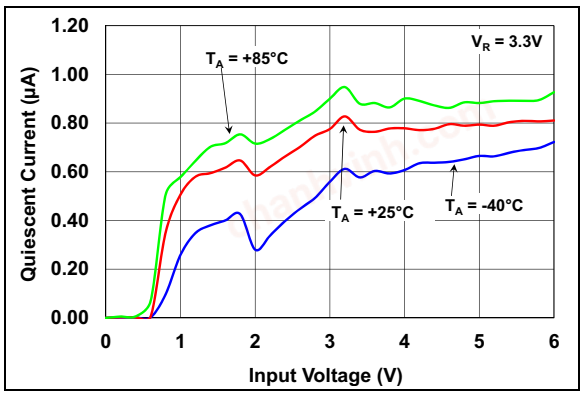


FIGURE 2-3: *Quiescent Current vs. Input Voltage.*

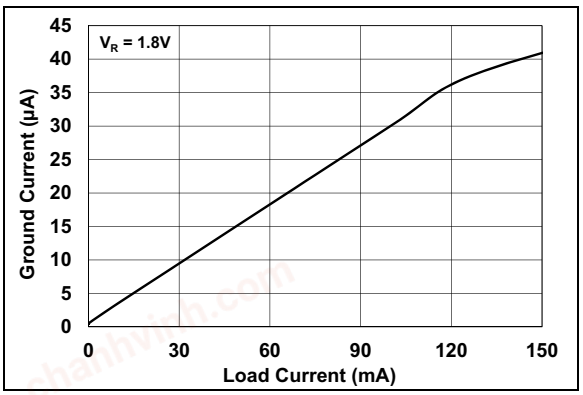


FIGURE 2-6: *Ground Current vs. Load Current.*

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Note: Unless otherwise indicated, V_{IN} = 3.5V for V_R < 2.5V or V_{IN} = V_R + 1V for $V_R \geq$ 2.5V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 0 µF, $V_{\overline{SHDN}}$ = V_{IN}, T_A = +25°C.

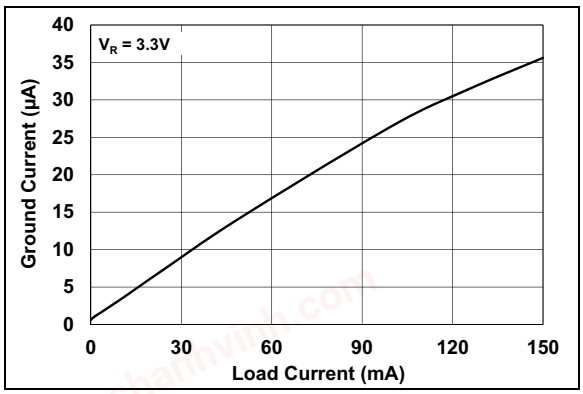


FIGURE 2-7: *Ground Current vs. Load Current.*

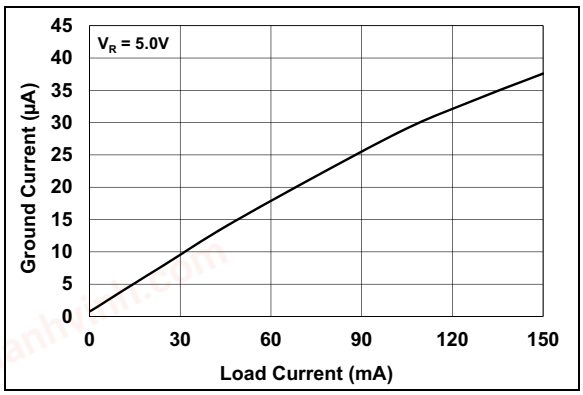


FIGURE 2-8: *Ground Current vs. Load Current.*

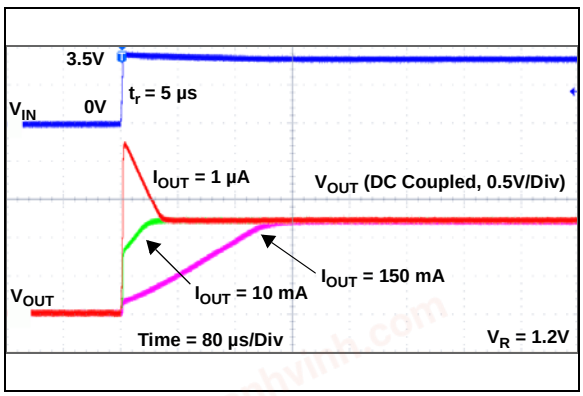


FIGURE 2-9: *Start-Up from V_{IN}.*

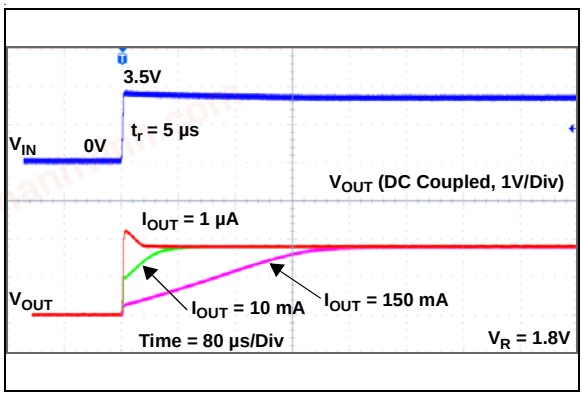


FIGURE 2-10: *Start-Up from V_{IN}.*

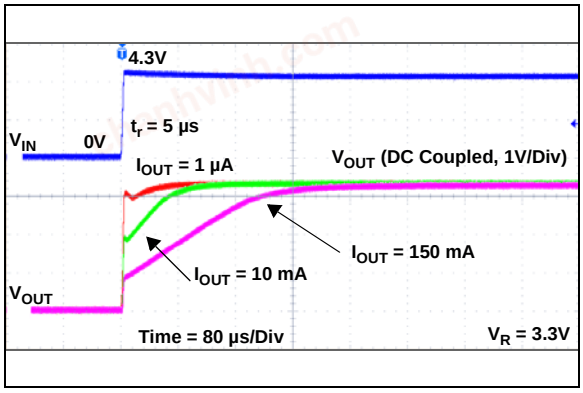


FIGURE 2-11: *Start-Up from V_{IN}.*

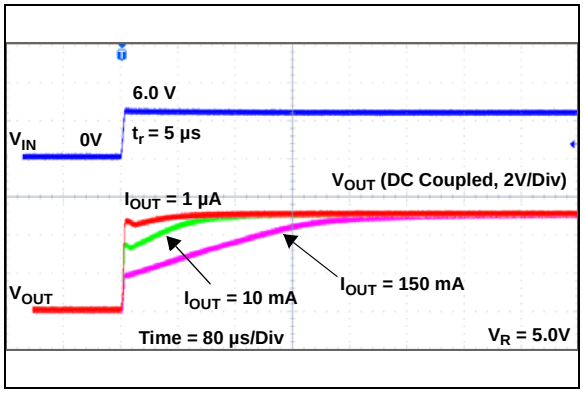


FIGURE 2-12: *Start-Up from V_{IN}.*

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Note: Unless otherwise indicated, V_{IN} = 3.5V for V_R < 2.5V or V_{IN} = V_R + 1V for V_R ≥ 2.5V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 0 µF, $V_{\overline{SHDN}}$ = V_{IN}, T_A = +25°C.

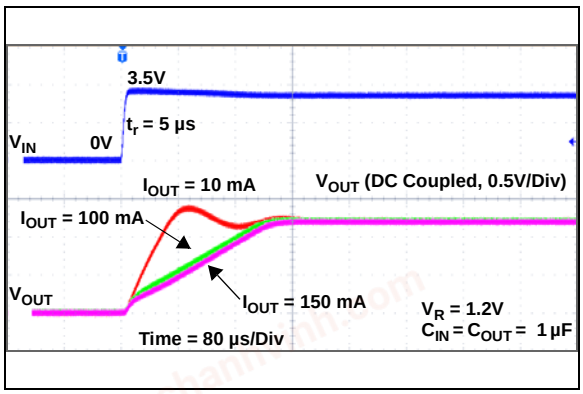


FIGURE 2-13: *Start-Up from V_{IN}.*

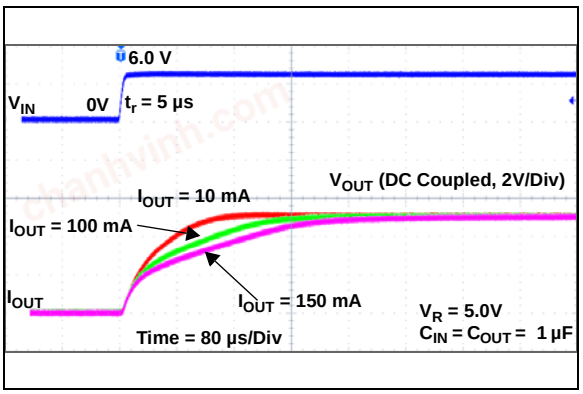


FIGURE 2-16: *Start-Up from V_{IN}.*

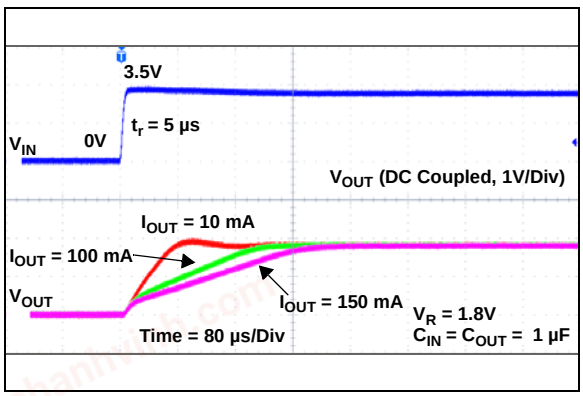


FIGURE 2-14: *Start-Up from V_{IN}.*

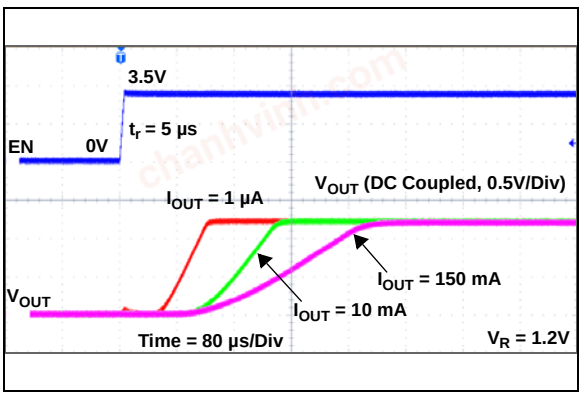


FIGURE 2-17: *Start-Up from SHDN.*

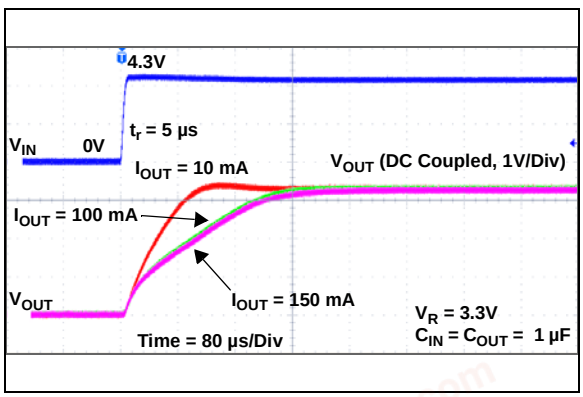


FIGURE 2-15: *Start-Up from V_{IN}.*

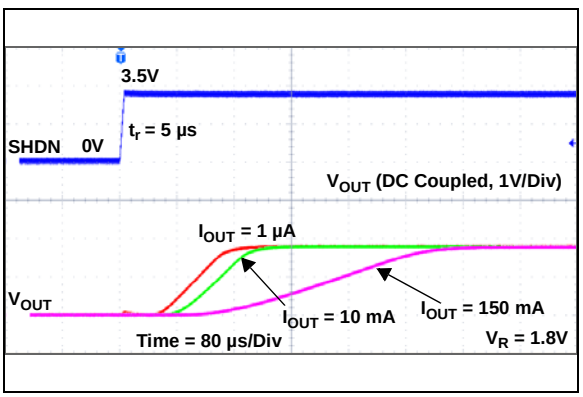


FIGURE 2-18: *Start-Up from SHDN.*

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Note: Unless otherwise indicated, V_{IN} = 3.5V for V_R < 2.5V or V_{IN} = V_R + 1V for V_R ≥ 2.5V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 0 µF, $V_{\overline{SHDN}}$ = V_{IN}, T_A = +25°C.

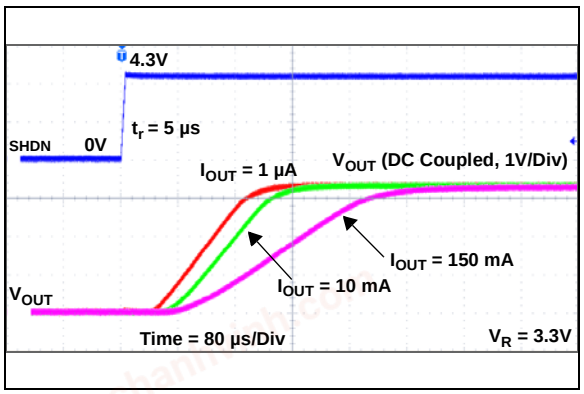


FIGURE 2-19: *Start-Up from SHDN.*

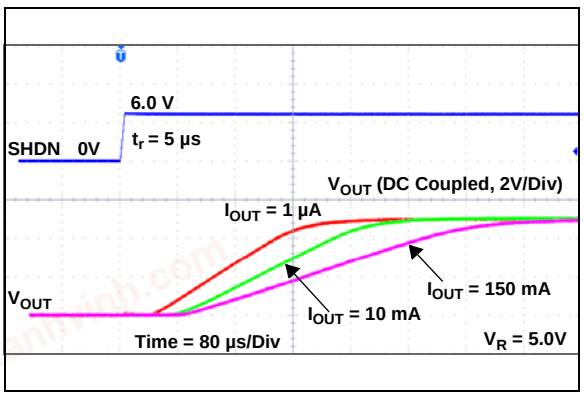


FIGURE 2-20: *Start-Up from SHDN.*

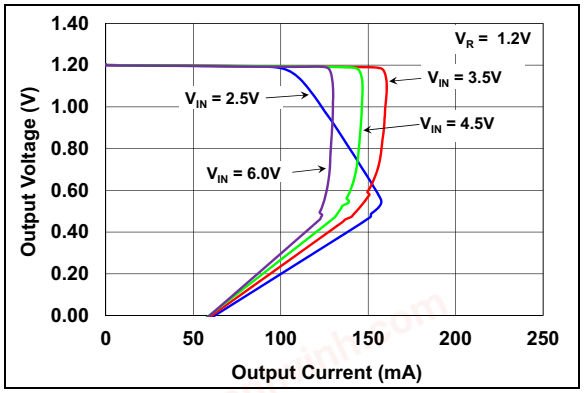


FIGURE 2-21: *Output Voltage vs. Output Current.*

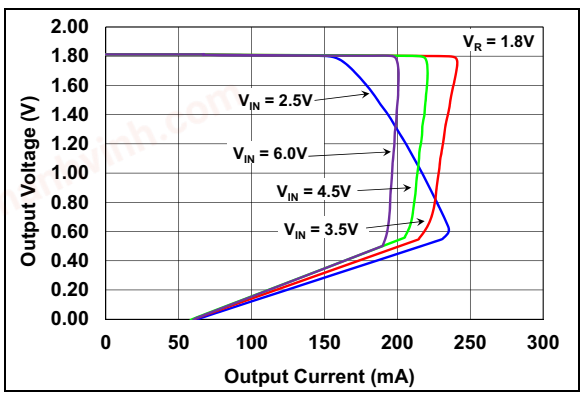


FIGURE 2-22: *Output Voltage vs. Output Current.*

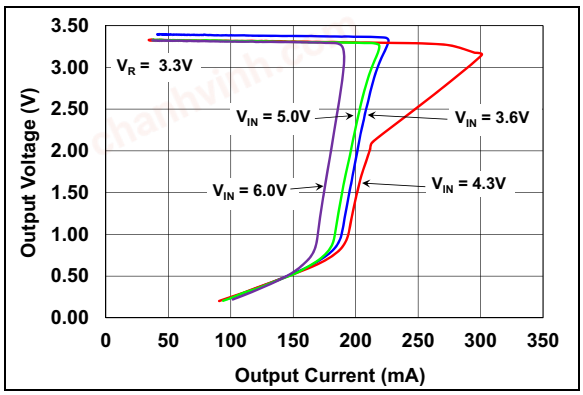


FIGURE 2-23: *Output Voltage vs. Output Current.*

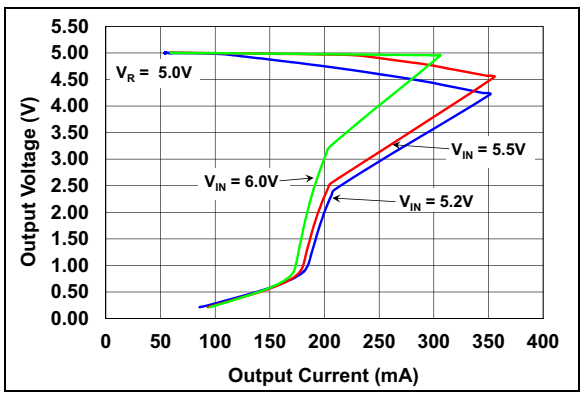


FIGURE 2-24: *Output Voltage vs. Output Current.*

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Note: Unless otherwise indicated, V_{IN} = 3.5V for V_R < 2.5V or V_{IN} = V_R + 1V for $V_R \geq$ 2.5V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 0 µF, $V_{\overline{SHDN}}$ = V_{IN}, T_A = +25°C.

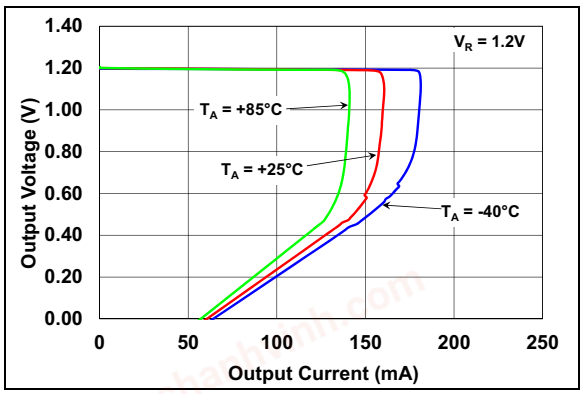


FIGURE 2-25: *Output Voltage vs. Output Current.*

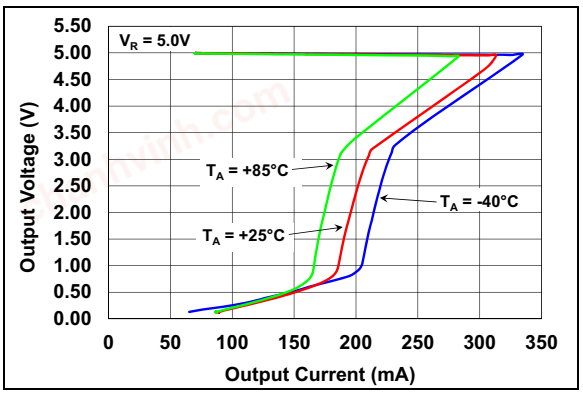


FIGURE 2-28: *Output Voltage vs. Output Current.*

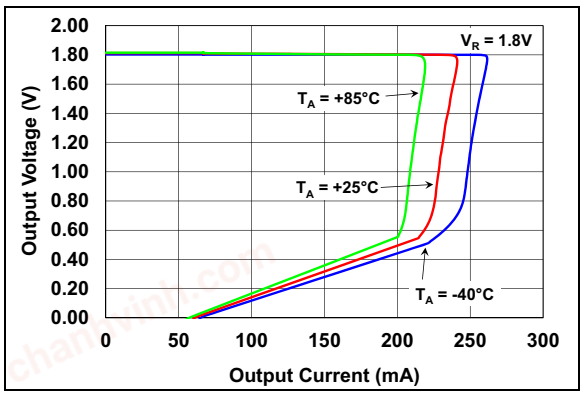


FIGURE 2-26: *Output Voltage vs. Output Current.*

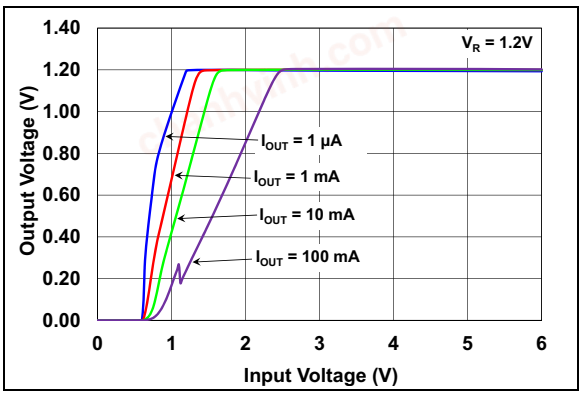


FIGURE 2-29: *Output Voltage vs. Input Voltage.*

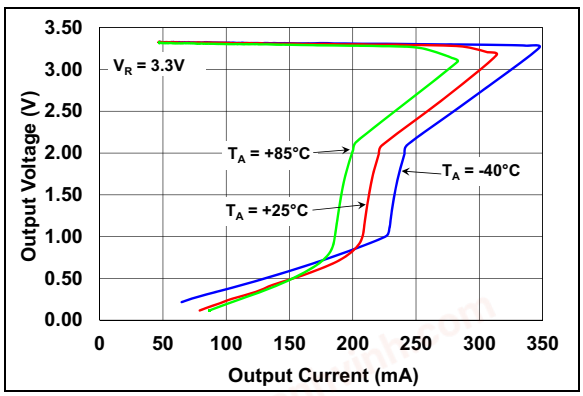


FIGURE 2-27: *Output Voltage vs. Output Current.*

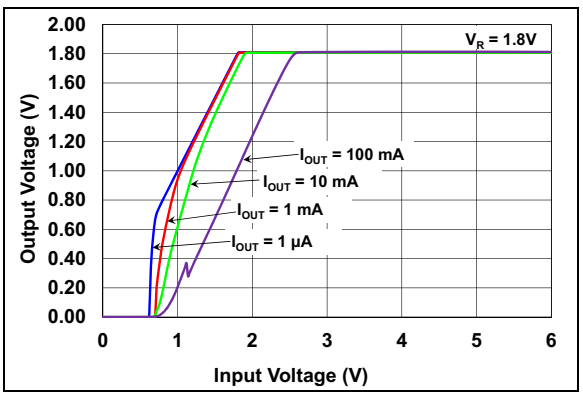


FIGURE 2-30: *Output Voltage vs. Input Voltage.*

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Note: Unless otherwise indicated, V_{IN} = 3.5V for V_R < 2.5V or V_{IN} = V_R + 1V for $V_R \geq$ 2.5V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 0 µF, $V_{\overline{SHDN}}$ = V_{IN}, T_A = +25°C.

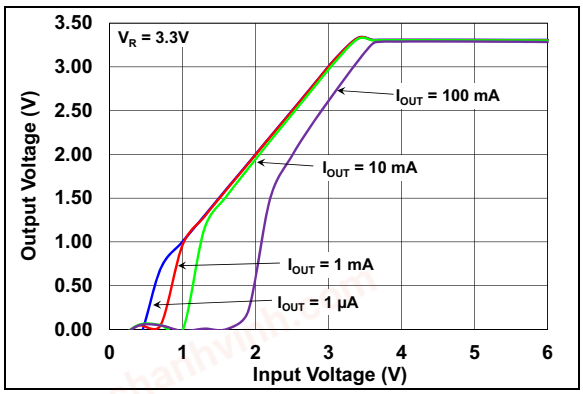


FIGURE 2-31: *Output Voltage vs. Input Voltage.*

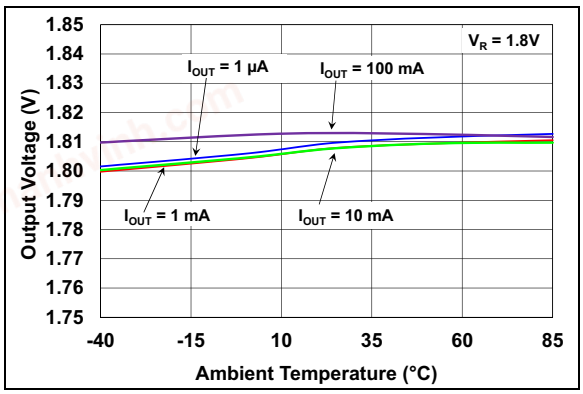


FIGURE 2-34: *Output Voltage vs. Ambient Temperature.*

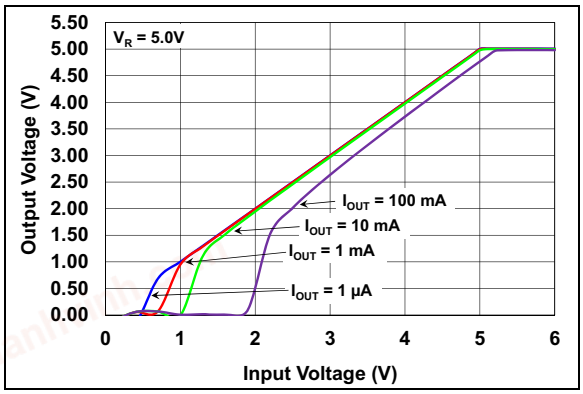


FIGURE 2-32: *Output Voltage vs. Input Voltage.*

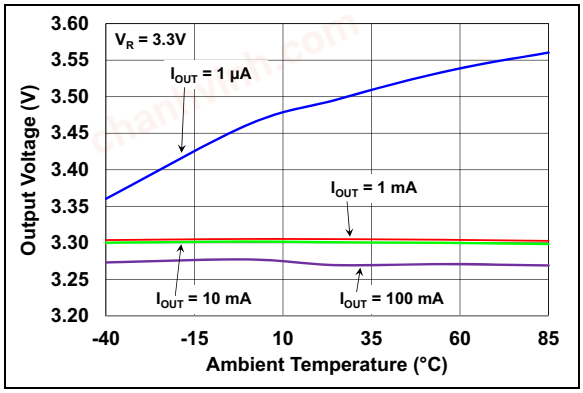


FIGURE 2-35: *Output Voltage vs. Ambient Temperature.*

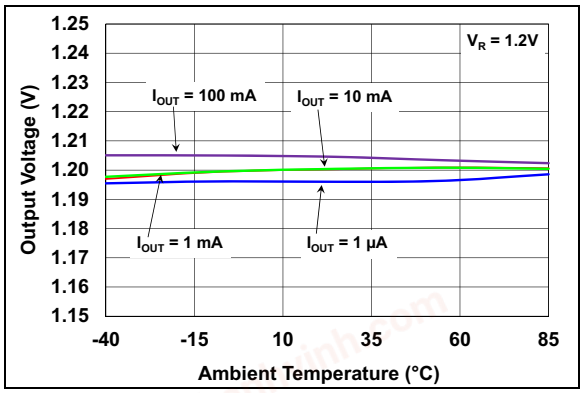


FIGURE 2-33: *Output Voltage vs. Ambient Temperature.*

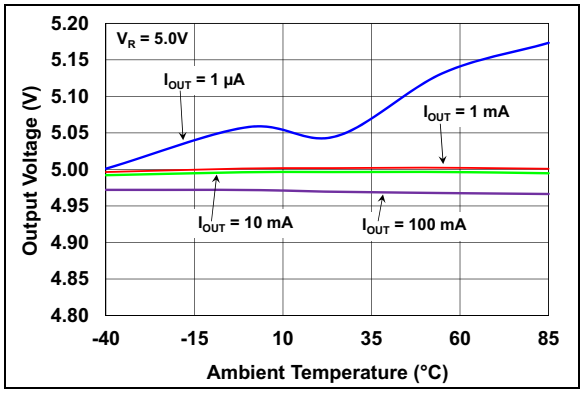


FIGURE 2-36: *Output Voltage vs. Ambient Temperature.*

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Note: Unless otherwise indicated, V_{IN} = 3.5V for V_R < 2.5V or V_{IN} = V_R + 1V for $V_R \geq$ 2.5V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 0 µF, $V_{\overline{SHDN}}$ = V_{IN}, T_A = +25°C.

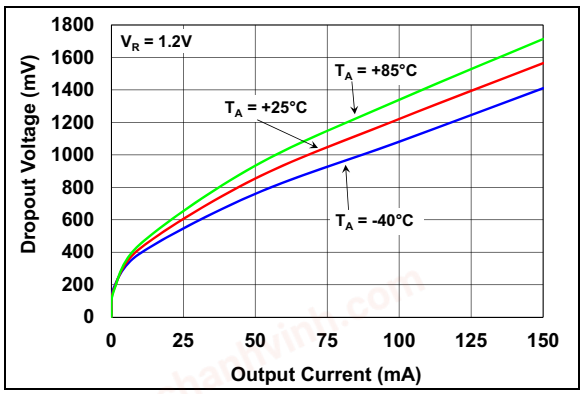


FIGURE 2-37: *Dropout Voltage vs. Output Current.*

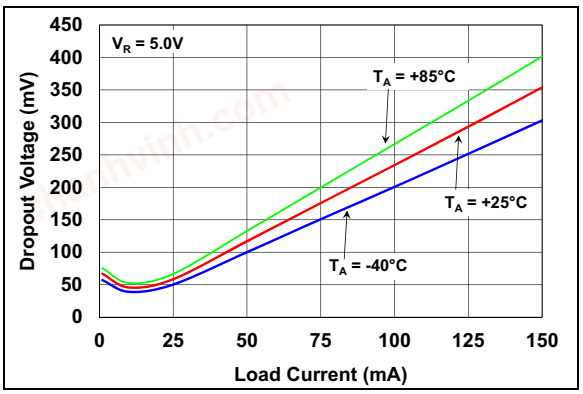


FIGURE 2-40: *Dropout Voltage vs. Output Current.*

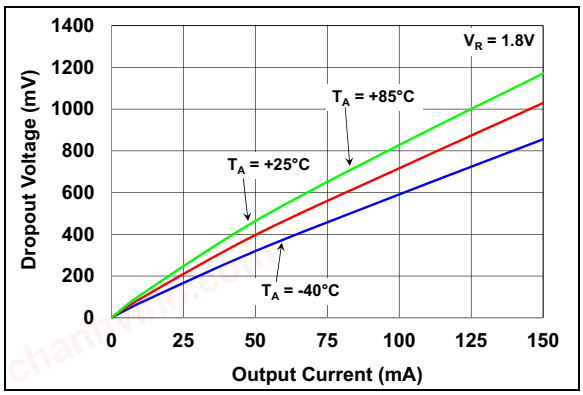


FIGURE 2-38: *Dropout Voltage vs. Output Current.*

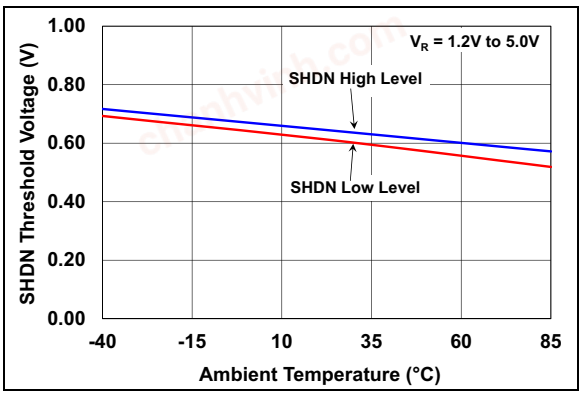


FIGURE 2-41: *Shutdown Threshold Voltage vs. Ambient Temperature.*

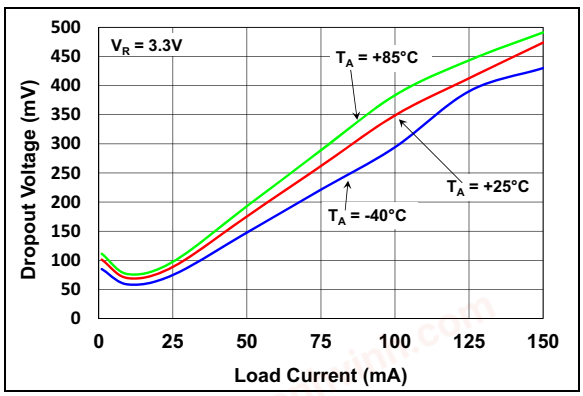


FIGURE 2-39: *Dropout Voltage vs. Output Current.*

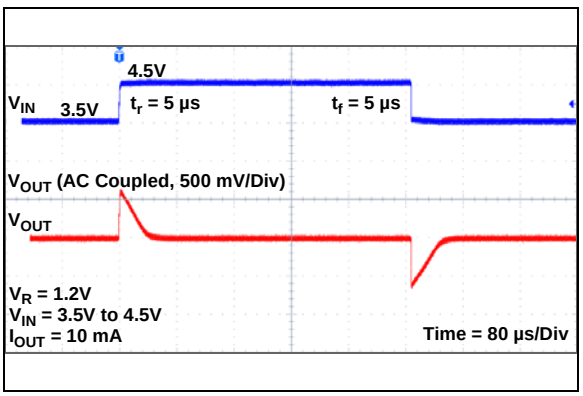


FIGURE 2-42: *Dynamic Line Response.*

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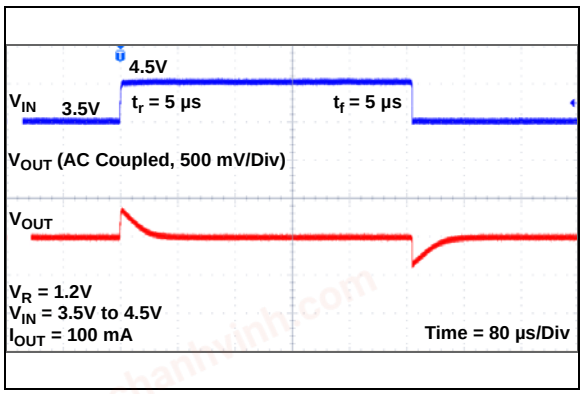


FIGURE 2-43: *Dynamic Line Response.*

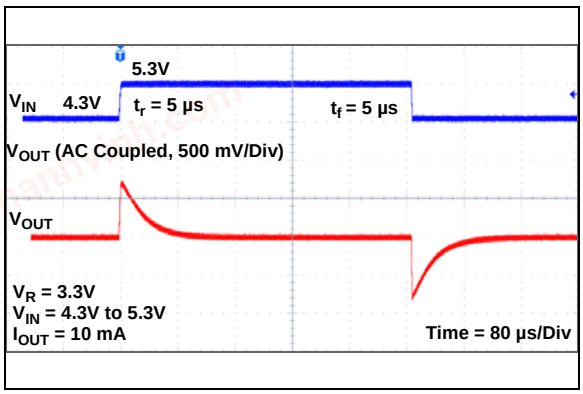


FIGURE 2-46: *Dynamic Line Response.*

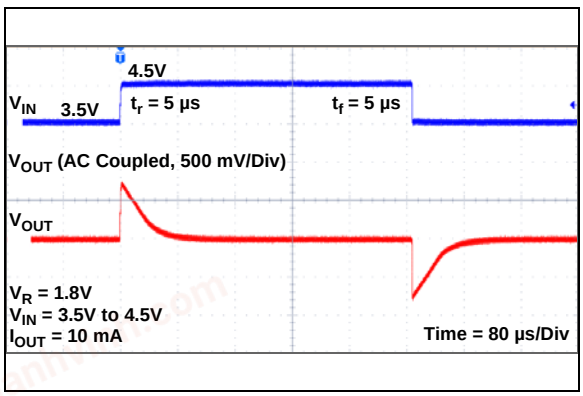


FIGURE 2-44: *Dynamic Line Response.*

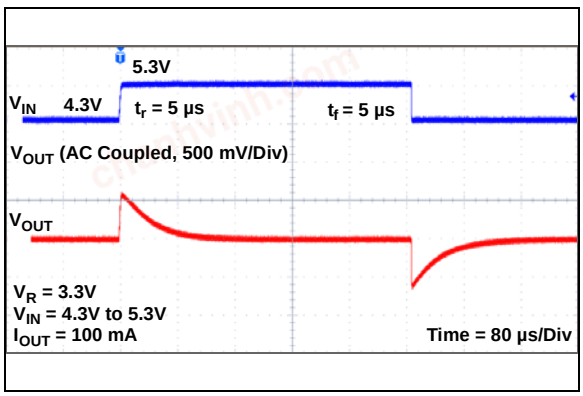


FIGURE 2-47: *Dynamic Line Response.*

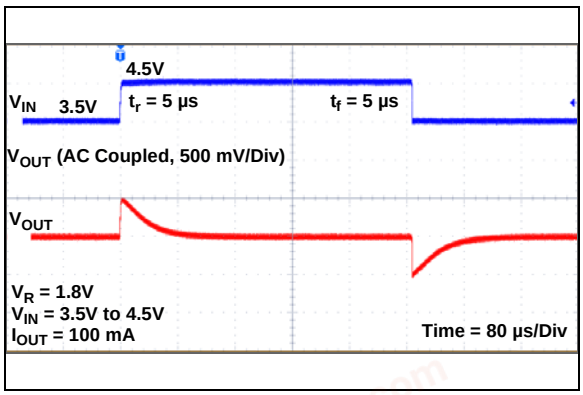


FIGURE 2-45: *Dynamic Line Response.*

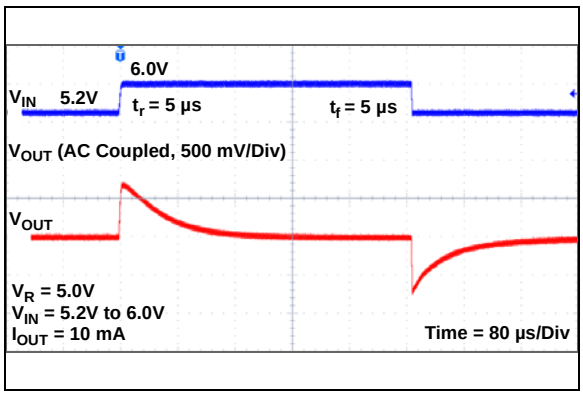


FIGURE 2-48: *Dynamic Line Response.*

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Note: Unless otherwise indicated, V_{IN} = 3.5V for V_R < 2.5V or V_{IN} = V_R + 1V for V_R ≥ 2.5V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 0 µF, $V_{\overline{SHDN}}$ = V_{IN}, T_A = +25°C.

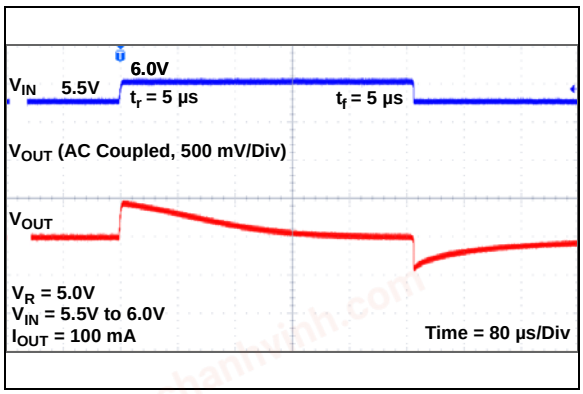


FIGURE 2-49: *Dynamic Line Response.*

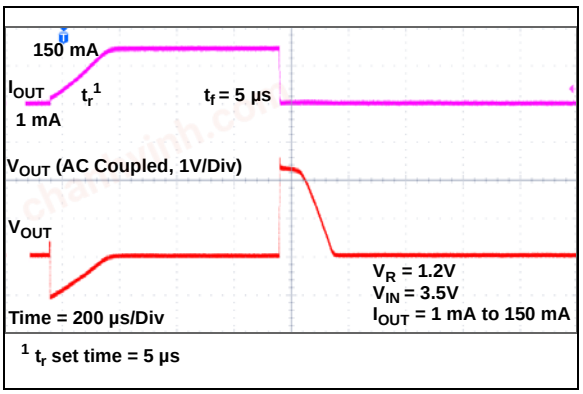


FIGURE 2-52: *Dynamic Load Response.*

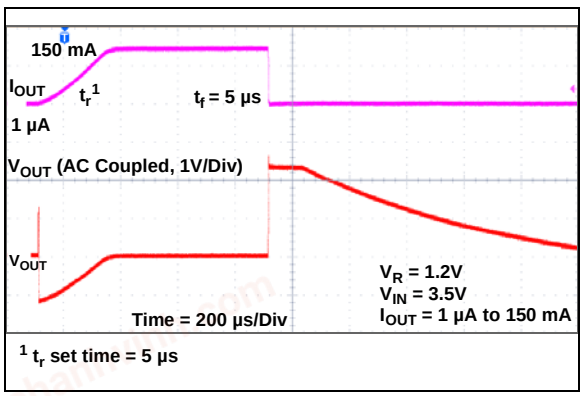


FIGURE 2-50: *Dynamic Load Response.*

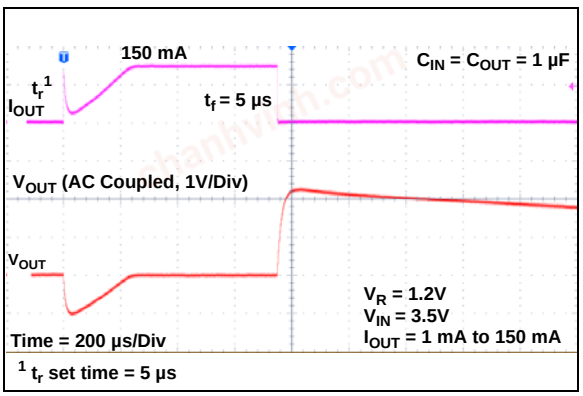


FIGURE 2-53: *Dynamic Load Response.*

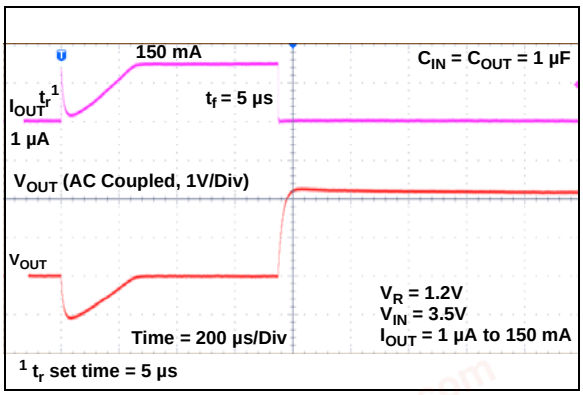


FIGURE 2-51: *Dynamic Load Response.*

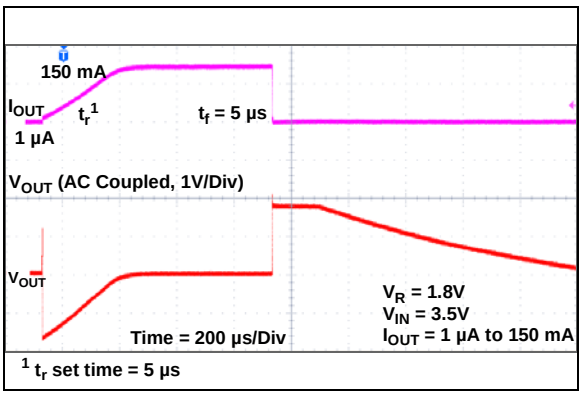


FIGURE 2-54: *Dynamic Load Response.*

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Note: Unless otherwise indicated, V_{IN} = 3.5V for V_R < 2.5V or V_{IN} = V_R + 1V for $V_R \geq$ 2.5V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 0 µF, $V_{\overline{SHDN}}$ = V_{IN}, T_A = +25°C.

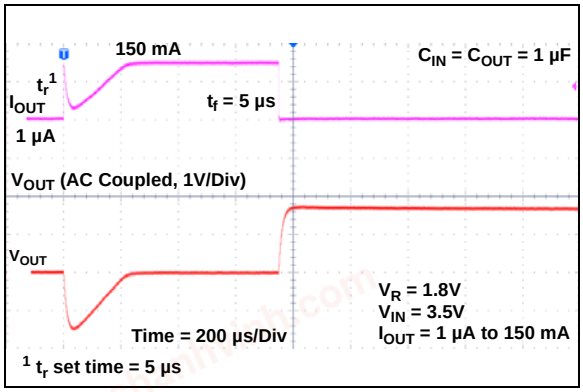


FIGURE 2-55: *Dynamic Load Response.*

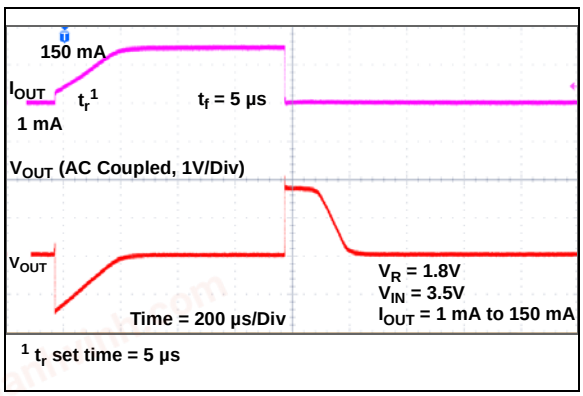


FIGURE 2-56: *Dynamic Load Response.*

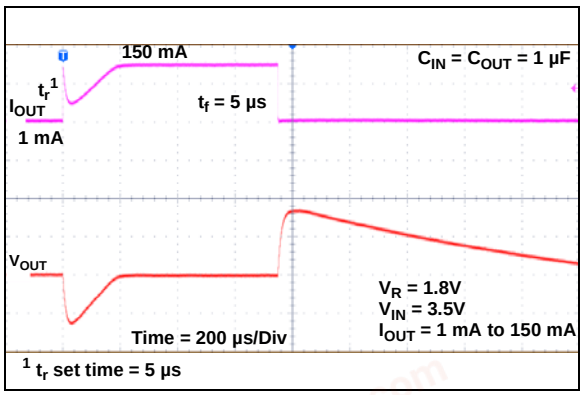


FIGURE 2-57: *Dynamic Load Response.*

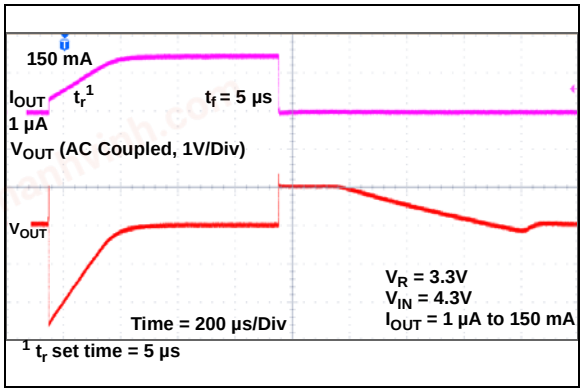


FIGURE 2-58: *Dynamic Load Response.*

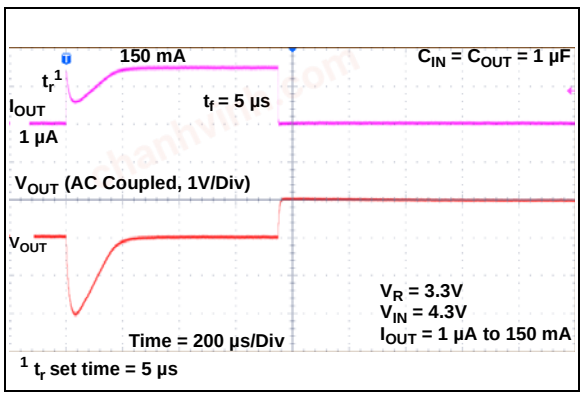


FIGURE 2-59: *Dynamic Load Response.*

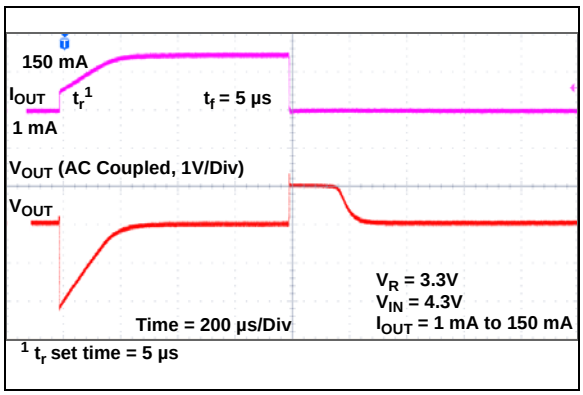


FIGURE 2-60: *Dynamic Load Response.*

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Note: Unless otherwise indicated, V_{IN} = 3.5V for V_R < 2.5V or V_{IN} = V_R + 1V for $V_R \geq$ 2.5V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 0 µF, $V_{\overline{SHDN}}$ = V_{IN}, T_A = +25°C.

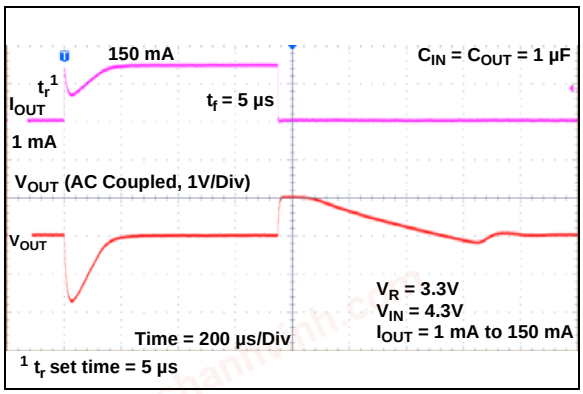


FIGURE 2-61: *Dynamic Load Response.*

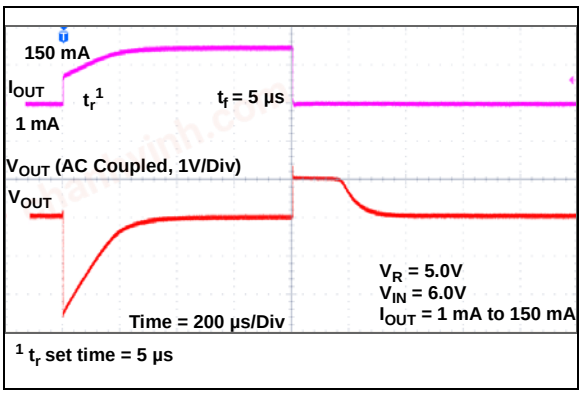


FIGURE 2-64: *Dynamic Load Response.*

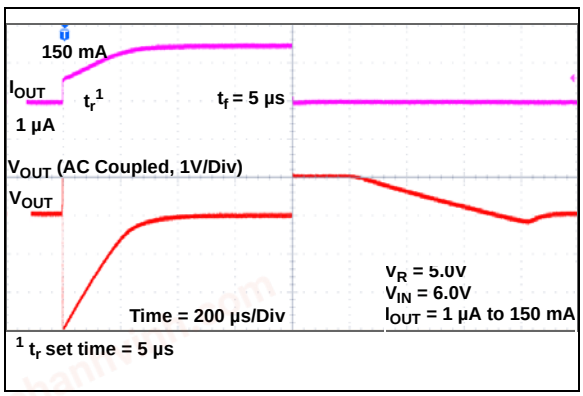


FIGURE 2-62: *Dynamic Load Response.*

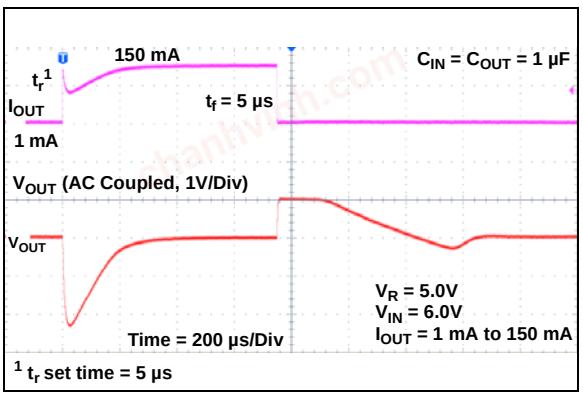


FIGURE 2-65: *Dynamic Load Response.*

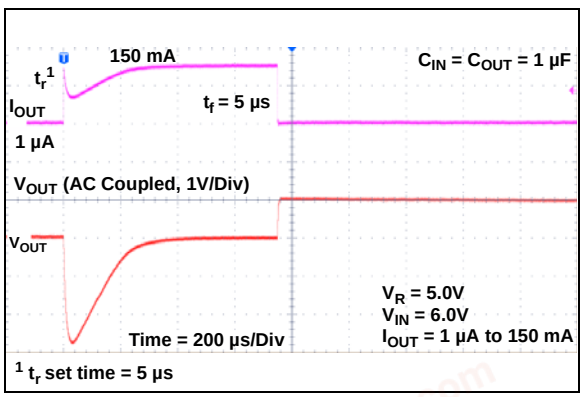


FIGURE 2-63: *Dynamic Load Response.*

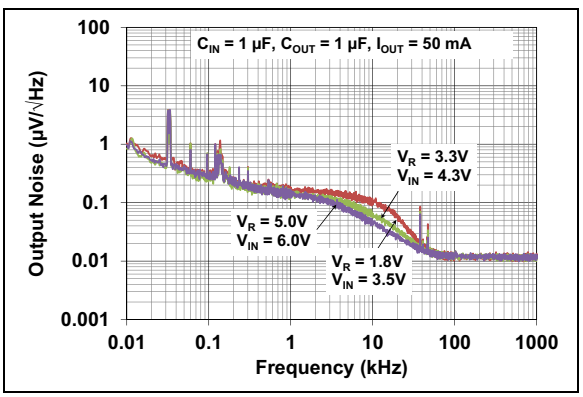


FIGURE 2-66: *Output Noise vs. Frequency.*

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Note: Unless otherwise indicated, V_{IN} = 3.5V for V_R < 2.5V or V_{IN} = V_R + 1V for $V_R \geq$ 2.5V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 0 µF, $V_{\overline{SHDN}}$ = V_{IN}, T_A = +25°C.

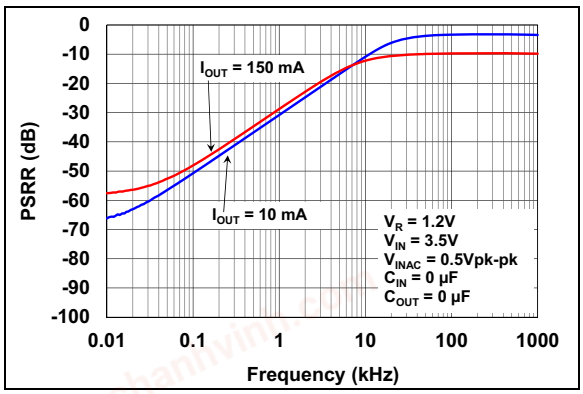


FIGURE 2-67: *Power Supply Ripple Rejection vs. Frequency.*

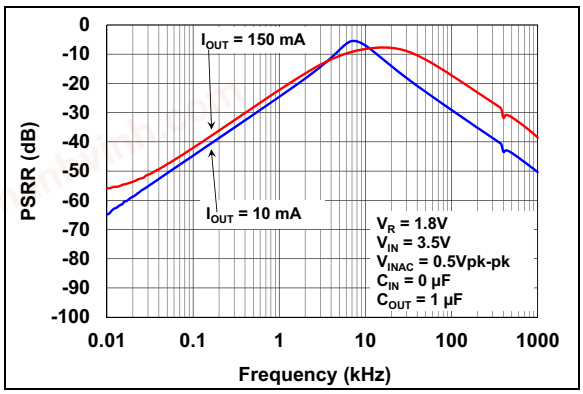


FIGURE 2-70: *Power Supply Ripple Rejection vs. Frequency.*

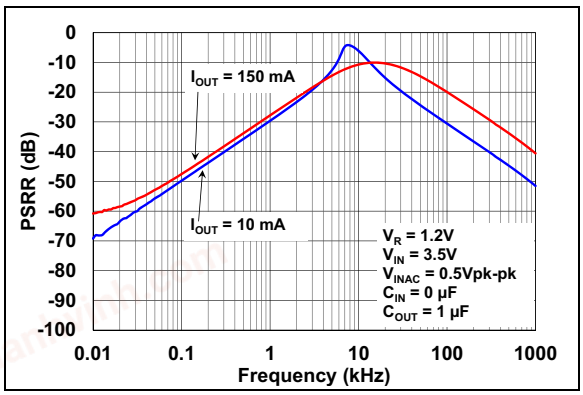


FIGURE 2-68: *Power Supply Ripple Rejection vs. Frequency.*

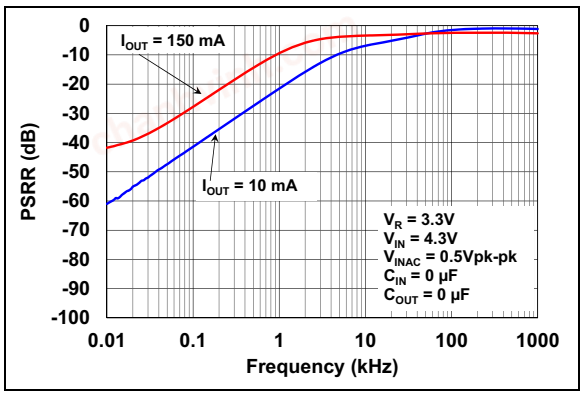


FIGURE 2-71: *Power Supply Ripple Rejection vs. Frequency.*

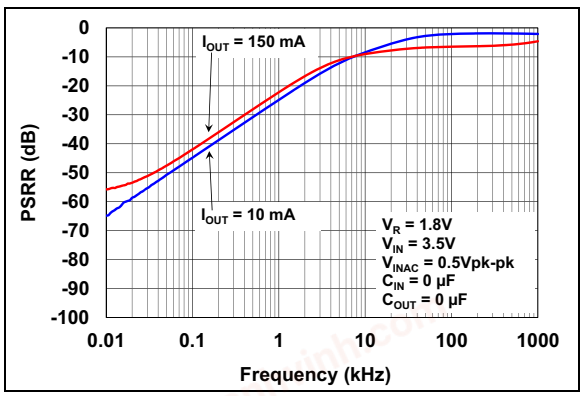


FIGURE 2-69: *Power Supply Ripple Rejection vs. Frequency.*

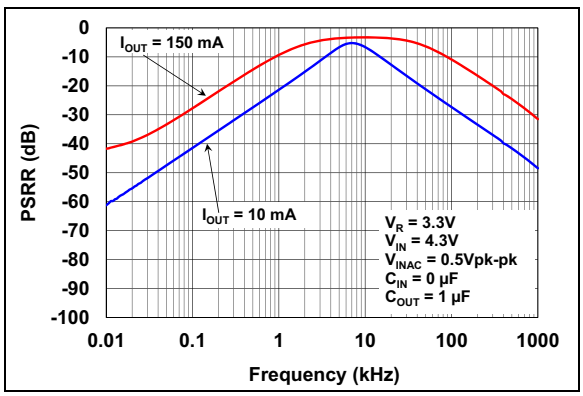


FIGURE 2-72: *Power Supply Ripple Rejection vs. Frequency.*

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Note: Unless otherwise indicated, V_{IN} = 3.5V for V_R < 2.5V or V_{IN} = V_R + 1V for V_R ≥ 2.5V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 0 µF, $V_{\overline{SHDN}}$ = V_{IN}, T_A = +25°C.

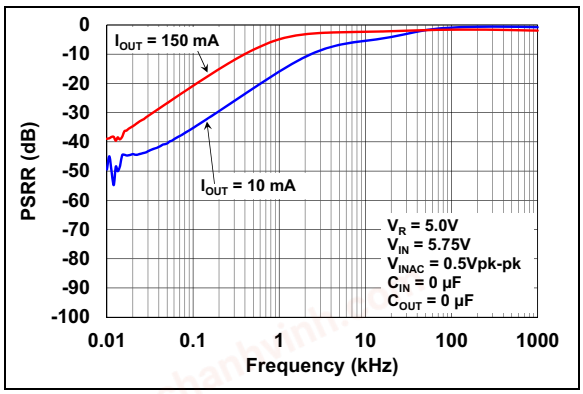


FIGURE 2-73: *Power Supply Ripple Rejection vs. Frequency.*

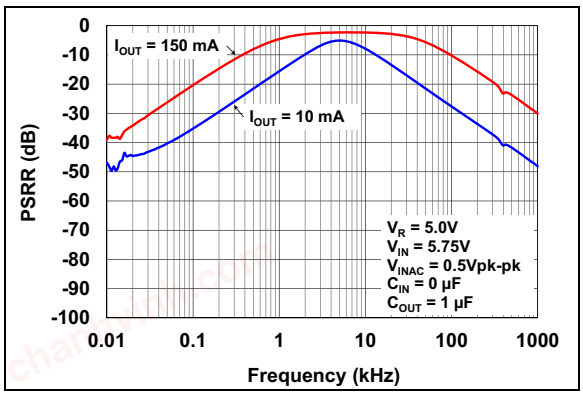


FIGURE 2-74: *Power Supply Ripple Rejection vs. Frequency.*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP1711 1X1 UQFN	MCP1711 SOT-23	Symbol	Description
4	1	V_{IN}	Unregulated Input Supply Voltage
2	2	GND	Ground Terminal
3	3	$\overline{SHDN}$	Shutdown Input
—	4	NC	Not Connected **(SOT-23 only)**
1	5	V_{OUT}	Regulated Voltage Output
5	—	EP	Exposed Thermal Pad **(1x1 UQFN only)**

3.1 Unregulated Input Voltage (V_{IN})

Connect the V_{IN} pin to the output of the unregulated source voltage. Like all low dropout linear regulators, low-source impedance is necessary for ensuring stable operation of the LDO. The amount of capacitance required to ensure low-source impedance will depend on the proximity of the input source capacitors or battery type. For most applications, 0.1 µF of capacitance will ensure stable operation of the LDO circuit. If the output capacitor is used, the input capacitor should have a capacitance value equal to or greater than the output capacitor for performance applications.

The input capacitor will supply the load current during transients and improve performance. For applications that have low load currents, the input capacitance requirement can be lowered.

The type of capacitor used may be ceramic, tantalum or aluminum electrolytic. The low ESR characteristics of the ceramic will yield better noise and Power Supply Rejection Ratio (PSRR) performance at high frequency.

3.2 Ground Terminal (GND)

This is the regulator ground. Tie GND to the negative side of the output capacitor (if used) and to the negative side of the input capacitor. Only the LDO bias current flows out of this pin, so there is no high current. The LDO output regulation is referenced to this pin. Minimize voltage drops between this pin and the negative side of the load. If a PCB ground plane is not used, minimize the length of the trace between the GND pin and the ground line.

3.3 Shutdown Input ($\overline{SHDN}$)

The $\overline{SHDN}$ input is used to turn the LDO output voltage on and off.

When the $\overline{SHDN}$ input is at logic High level, the LDO output voltage is enabled. When the $\overline{SHDN}$ pin is pulled to a logic Low level, the LDO output voltage is disabled. When the $\overline{SHDN}$ pin is pulled low, the V_{OUT} pin is pulled down to the ground level via, parallel to the feedback resistors (R_1 and R_2), and the C_{OUT} discharge resistance (R_{DCHG}).

The output voltage becomes unstable when the $\overline{SHDN}$ pin is left floating.

3.4 Not Connected Pin (NC)

The SOT-23 package has a pin that is not connected.This pin should be either left floating or tied to the ground plane.

3.5 Regulated Output Voltage (V_{OUT})

Connect the V_{OUT} pin to the positive side of the load and to the positive side of the output capacitor (if used). The positive side of the output capacitor should be physically located as close as possible to the LDO V_{OUT} pin. The current flowing out of this pin is equal to the DC load current.

3.6 Exposed Thermal Pad (EP)

The 4-lead 1 x 1 UQFN package has an exposed metal pad on the bottom of the package. The exposed metal pad gives the device better thermal characteristics by providing a good thermal path to either a PCB isolated plane or a PCB ground plane. The exposed pad of the package is not internally connected to GND.

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4.0 DEVICE OVERVIEW

The MCP1711 device is a 150 mA output current, low-dropout (LDO) voltage regulator. The low dropout voltage at high current makes it ideal for battery-powered applications. The input voltage ranges from 1.4V to 6.0V. Unlike other high output current LDOs, the MCP1711 typically draws only 600 nA quiescent current and maximum 45 µA ground current at 150 mA load. MCP1711 has a shutdown control input pin ($\overline{SHDN}$). The output voltage options are fixed.

4.1 LDO Output Voltage

The MCP1711 LDO has a fixed output voltage. The output voltage range is 1.2V to 5.0V.

4.2 Output Current and Current Limiting

The MCP1711 is tested and ensured to supply a maximum of 150 mA of output current. The device can provide a highly accurate output voltage even if the output current is only 1 µA (very light load).

The MCP1711 also features a true output current foldback. If an excessive load, due to a low impedance short-circuit condition at the output load, is detected, the output current and voltage will fold back towards 80 mA and 0V, respectively. The output voltage and current will resume normal levels when the excessive load is removed. If the overload condition is a soft overload, the MCP1711 will supply higher load currents of up to 270 mA typical. This allows for device usage in applications that have pulsed load currents having an average output current value of 150 mA or less.

4.3 Output Capacitor

The MCP1711 can provide a stable output voltage even without an additional output capacitor due to its excellent internal phase compensation, so that a minimum output capacitance is not required. In order to improve the load step response and PSRR, an output capacitor can be added. A value in the range of 0.1 µF to 1.0 µF is recommended for most applications. The capacitor should be placed as close as possible to the V_{OUT} pin and the GND pin. The device is compatible with low ESR ceramic capacitors. Ceramic materials like X7R and X5R have low temperature coefficients and are well within the acceptable ESR range required. A typical 1 µF X7R 0805 capacitor has an ESR of 50 mΩ.

4.4 Input Capacitor

Low-input source impedance is necessary for the LDO output to operate properly. When operating from batteries, or in applications with long lead length (> 10 inches) between the input source and the LDO, some input capacitance is recommended. A minimum of 0.1 µF to 1.0 µF is recommended for most applications. For applications that have output step load requirements, the input capacitance of the LDO is very important. The input capacitance provides the LDO with a good local low-impedance source to pull the transient current from, so it responds quickly to the output load step. For good step response performance, the input capacitor should be of an equivalent or higher value than the output capacitor. The capacitor should be placed as close to the input of the LDO as is practical. Larger input capacitors will also help reduce any high-frequency noise on the input and output of the LDO as well as reduce the effects of any inductance that exists between the input source voltage and the input capacitance of the LDO.

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4.5 Shutdown Input ($\overline{SHDN}$)

The MCP1711 internal circuitry can be shut down via the signal from the $\overline{SHDN}$ pin. The $\overline{SHDN}$ input is an active-low input signal that turns the LDO on and off. The shutdown threshold is a fixed voltage level. The minimum value of this shutdown threshold required to turn the output on is 0.91V. The maximum value required to turn the output off is 0.38V.

In Shutdown mode, the V_{OUT} pin will be pulled down to the ground level via, parallel to feedback resistors and C_{OUT} discharge resistance R_{DCHG}. In this state, the application is protected from a glitch operation caused by the electric charge at the output capacitor. Moreover, the discharge time of the output capacitor is set by the C_{OUT} auto-discharge resistance (R_{DCHG}) and the output capacitor C_{OUT}. By setting the time constant of a C_{OUT} auto-discharge resistance value (R_{DCHG}) and the output capacitor value (C_{OUT}) as $\tau = C_{OUT} \times R_{DCHG}$, the output voltage after discharge via the internal switch is calculated using Equation 4-1:

Note:	The R_{DCHG} depends on V_{IN}; when V_{IN} is high the R_{DCHG} is low.

EQUATION 4-1:

$$V_{OUT}(t) = V_{OUT} \times e^{(-t/\tau)}$$

or

$$t = \tau \times ln(V_{OUT}/V_{OUT}(t))$$

Where:

$V_{OUT}(t)$ = The output voltage during discharging

V_{OUT} = The initial output voltage

t = Discharge time

τ = $C_{OUT} \times R_{DCHG}$

4.6 Dropout Voltage

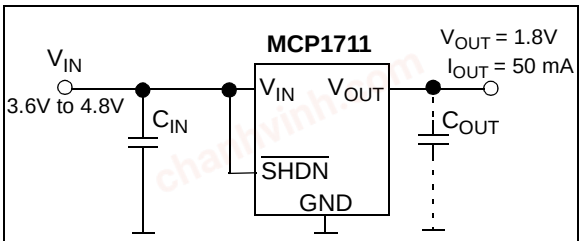
Dropout Voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below the nominal value that was measured with a V_R + 1.0V differential applied. See **Section 1.0 "Electrical Characteristics"**, for minimum and maximum voltage specifications.

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5.0 APPLICATION CIRCUITS AND ISSUES

5.1 Typical Application

The MCP1711 is most commonly used as a voltage regulator. Its low quiescent current and low dropout voltage make it ideal for a multitude of battery-powered applications.



Application Input conditions

Package Type	=	5-Lead SOT-23
Input Voltage Range	=	3.5V to 4.8V
V_{IN} maximum	=	4.8V
V_{OUT} typical	=	1.8V
I_{OUT}	=	50 mA maximum

FIGURE 5-1: *Typical Application Circuit.*

5.2 Power Calculations

5.2.1 POWER DISSIPATION

The internal power dissipation of the MCP1711 is a function of input voltage, output voltage and output current. The power dissipation, as a result of the quiescent current draw, is so low that it is insignificant (0.6 µA x V_{IN}). To calculate the internal power dissipation of the LDO use Equation 5-1:

EQUATION 5-1:

$$P_{LDO} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$$

Where:

P_{LDO}	=	LDO pass device internal power dissipation
$V_{IN(MAX)}$	=	Maximum input voltage
$V_{OUT(MIN)}$	=	LDO minimum output voltage, including the line and load regulations

The maximum continuous operating junction temperature specified for the MCP1711 is +125°C. To estimate the internal junction temperature of the MCP1711, the total internal power dissipation is multiplied by the thermal resistance from junction-to-ambient ($R\theta_{JA}$).

The thermal resistance from junction-to-ambient for the 5-Lead SOT-23 package is estimated at:

- 166.67°C with JEDEC 51-7 FR-4 board with thermal vias and
- 400 °C/W when the device is not mounted on the PCB, or is mounted on the one layer PCB with minimal copper that doesn't provide any additional cooling.

EQUATION 5-2:

$$T_{J(MAX)} = P_{TOTAL} \times R\theta_{JA} + T_{A(MAX)}$$

Where:

$T_{J(MAX)}$	=	Maximum continuous junction temperature
P_{TOTAL}	=	Total device power dissipation
$R\theta_{JA}$	=	Thermal resistance from junction to ambient
$T_{A(MAX)}$	=	Maximum ambient temperature

The maximum power dissipation capability for a package can be calculated if given the junction-to-ambient thermal resistance ($R\theta_{JA}$) and the maximum ambient temperature for the application. Equations 5-3 to 5-5 can be used to determine the package maximum internal power dissipation:

EQUATION 5-3:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{R\theta_{JA}}$$

Where:

$P_{D(MAX)}$	=	Maximum device power dissipation
$T_{J(MAX)}$	=	Maximum continuous junction temperature
$T_{A(MAX)}$	=	Maximum ambient temperature
$R\theta_{JA}$	=	Thermal resistance from junction to ambient

EQUATION 5-4:

$$T_{J(RISE)} = P_{D(MAX)} \times R\theta_{JA}$$

Where:

$T_{J(RISE)}$	=	Rise in device junction temperature over the ambient temperature
$P_{D(MAX)}$	=	Maximum device power dissipation
$R\theta_{JA}$	=	Thermal resistance from junction to ambient

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EQUATION 5-5:

$$T_J = T_{J(RISE)} + T_A$$

Where:

T_J = Junction temperature

$T_{J(RISE)}$ = Rise in device junction temperature over the ambient temperature

T_A = Ambient temperature

5.3 Voltage Regulator

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation are calculated in the following example. The power dissipation, as a result of ground current, is small enough to be neglected.

5.3.1 POWER DISSIPATION EXAMPLE

EXAMPLE 5-1: POWER DISSIPATION

Package

Package Type = SOT-23

Input Voltage

V_{IN} = 3.5V to 4.8V

LDO Output Voltages and Currents

V_{OUT} = 1.8V

I_{OUT} = 50 mA

Maximum Ambient Temperature

$T_{A(MAX)}$ = +40°C

Internal Power Dissipation

Internal Power dissipation is the product of the LDO output current times the voltage across the LDO (V_{IN} to V_{OUT}).

$P_{LDO(MAX)}$ = ($V_{IN(MAX)}$ - $V_{OUT(MIN)}$) x $I_{OUT(MAX)}$

$V_{OUT(MIN)}$ = 1.78V - 0.05V = 1.73V, where 1.78V is the minimum output voltage due to accuracy, and 0.05V is the load regulation; due to very small input voltage range, the line regulation is neglected

P_{LDO} = (4.8V - 1.73V) x 50 mA

P_{LDO} = 153.5 mW

5.3.1.1 Device Junction Temperature Rise

The internal junction temperature rise is a function of internal power dissipation and the thermal resistance from junction to ambient for the application. The thermal resistance from junction to ambient ($R\theta_{JA}$) is derived from an EIA/JEDEC standard for measuring thermal resistance for small surface mount packages.

The EIA/JEDEC specification is JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*. The standard describes the test method and board specifications for measuring the thermal resistance from junction to ambient. The actual thermal resistance for a particular application can vary depending on many factors, such as copper area and thickness. Refer to AN792 – *A Method to Determine How Much Power a SOT-23 Can Dissipate in an Application* (DS00792), for more information regarding this subject.

EXAMPLE 5-2:

$T_{J(RISE)} = P_{TOTAL} \times R\theta_{JA}$

T_{JRISE} = 153.5 mW x 400.0°C/W

T_{JRISE} = 61.4°C

5.3.1.2 Junction Temperature Estimate

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated:

EXAMPLE 5-3:

$T_J = T_{JRISE} + T_{A(MAX)}$

T_J = 61.4°C + 40°C = 101.4°C

5.3.1.3 Maximum Package Power Dissipation Example at +40°C Ambient Temperature

EXAMPLE 5-4:

SOT-23 (400.0 °C/W = $R\theta_{JA}$)

$P_{D(MAX)}$ = (125°C - 40°C)/400°C/W

$P_{D(MAX)}$ = 212 mW

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5.4 Voltage Reference

The MCP1711 can be used not only as a regulator, but also as a low quiescent current voltage reference. In many microcontroller applications, the initial accuracy of the reference can be calibrated using production test equipment or by using a ratio measurement. When the initial accuracy is calibrated, the thermal stability and line regulation tolerance are the only errors introduced by the MCP1711 LDO. The low cost, low quiescent current and small ceramic output capacitor are all advantages when using the MCP1711 as a voltage reference.

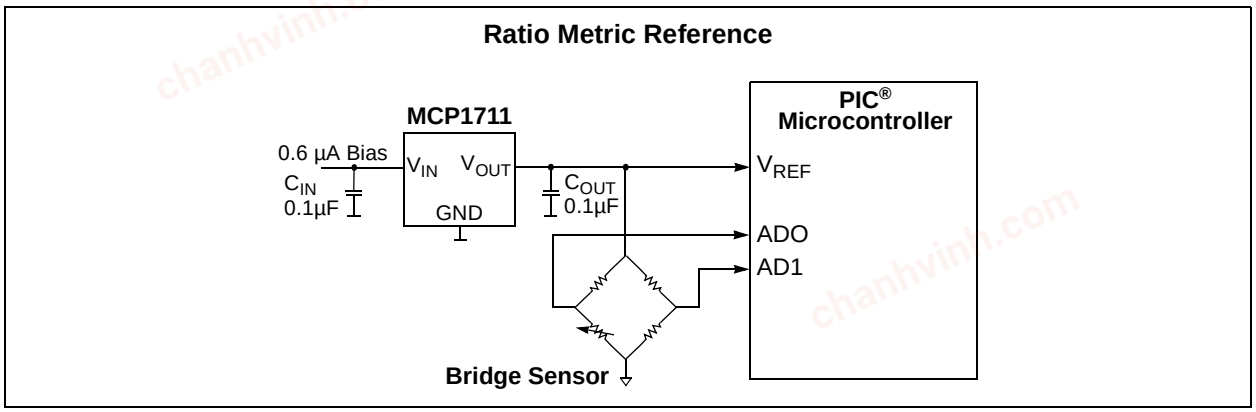


FIGURE 5-2: *Using the MCP1711 as a Voltage Reference.*

5.5 Pulsed Load Applications

For some applications, there are pulsed load current events that may exceed the specified 150 mA maximum specification of the MCP1711. The internal current limit of the MCP1711 will prevent high peak-load demands from causing nonrecoverable damage. The 150 mA rating is a maximum average continuous rating. As long as the average current does not exceed 150 mA, higher pulsed load currents can be applied to the MCP1711. The typical current limit for the MCP1711 is 270 mA (T_A = +25°C).

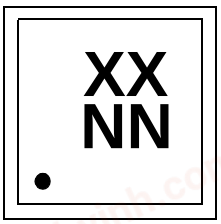
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6.0 PACKAGING INFORMATION

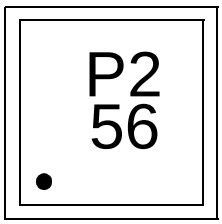
6.1 Package Marking Information

4-Lead UQFN (1x1x0.6 mm)

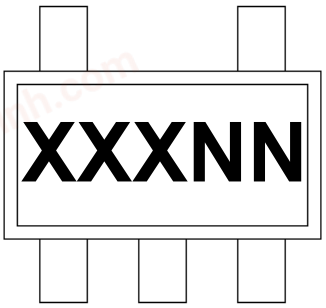


Device	Code
MCP1711T-12I/5X	P2NN
MCP1711T-18I/5X	P8NN
MCP1711T-20I/5X	PANN
MCP1711T-22I/5X	PCNN
MCP1711T-25I/5X	PFNN
MCP1711T-30I/5X	PNNN
MCP1711T-33I/5X	PSNN

Example

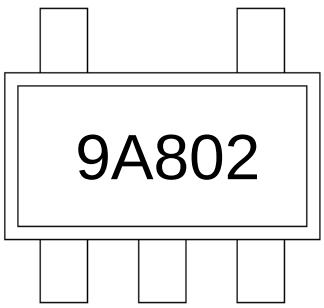


5-Lead SOT-23



Device	Code
MCP1711T-12I/OT	9A2xx
MCP1711T-18I/OT	9A8xx
MCP1711T-19I/OT	9A9xx
MCP1711T-22I/OT	9ACxx
MCP1711T-25I/OT	9AFxx
MCP1711T-30I/OT	9ANxx
MCP1711T-33I/OT	9ASxx
MCP1711T-50I/OT	9BAxx

Example



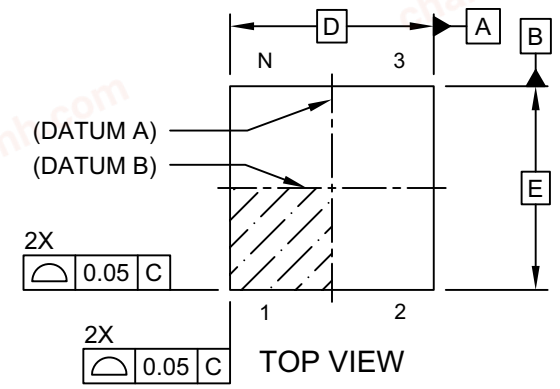
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

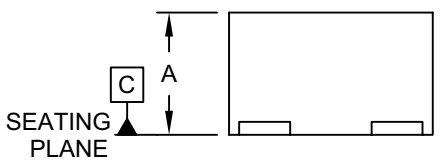
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4-Lead Plastic Ultra Thin Quad Flatpack No-Leads (5X) - 1x1x0.6mm [UQFN] (Formerly USPQ-4B04)

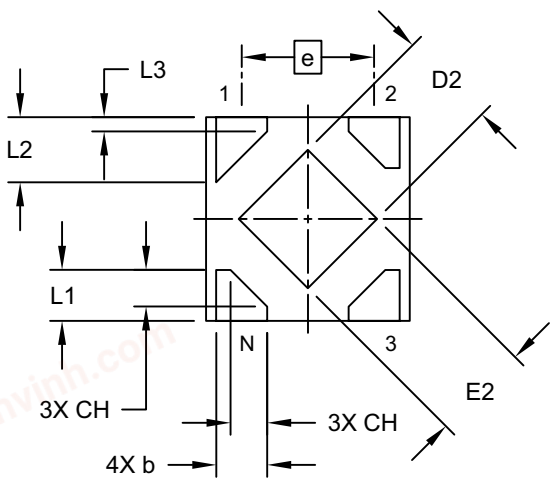
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



BOTTOM VIEW

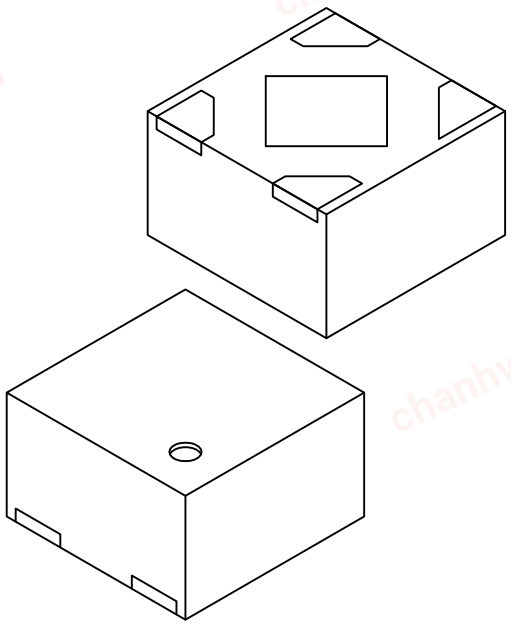
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4-Lead Plastic Ultra Thin Quad Flatpack No-Leads (5X) - 1x1x0.6mm [UQFN] (Formerly USPQ-4B04)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		4	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	0.60
Overall Width	E		1.00 BSC	
Exposed Pad Width	E2	0.43	0.48	0.53
Overall Length	D		1.00 BSC	
Exposed Pad Length	D2	0.43	0.48	0.53
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L1	0.20	0.25	0.30
Terminal Length	L2	0.27	0.32	0.37
-	L3	0.02	0.07	0.12
Terminal Chamfer	CH	-	0.18	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

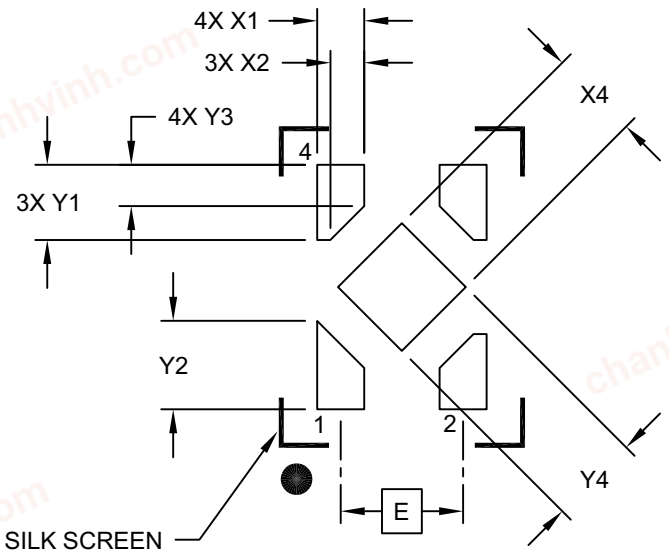
Microchip Technology Drawing C04-393B Sheet 2 of 2

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4-Lead Plastic Ultra Thin Quad Flatpack No-Leads (5X) - 1x1x0.6mm [UQFN] (Formerly USPQ-4B04)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units	MILLIMETERS		
Dimension Limits	MIN	NOM	MAX
E		0.65 BSC	
X1		0.25	
X2		0.18	
X4		0.48	
Y1		0.40	
Y2		0.47	
Y3		0.22	
Y4		0.48	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

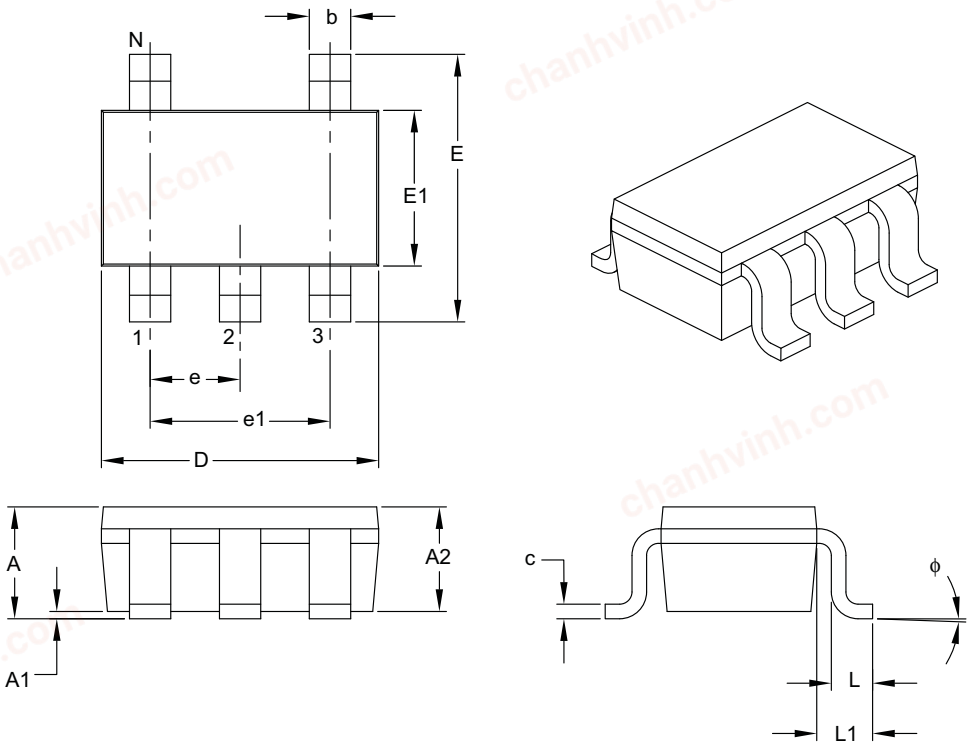
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5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

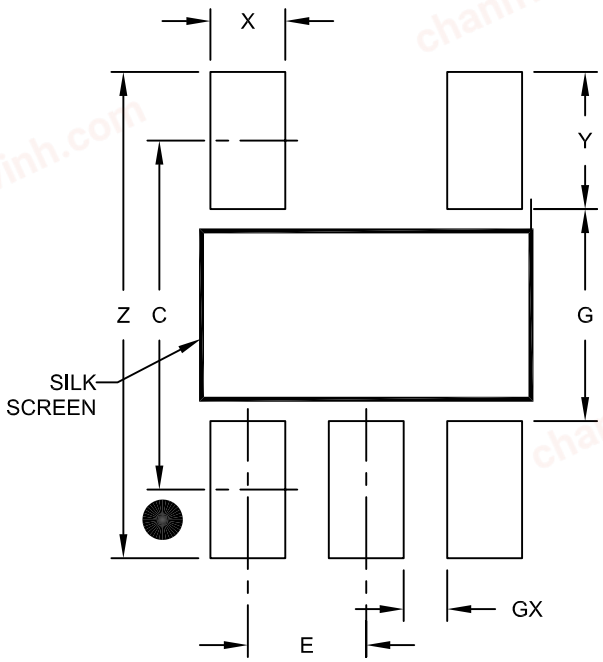
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

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5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091A

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APPENDIX A: REVISION HISTORY

Revision D (October 2016)

The following is the list of modifications:

- Added the 2.0V output voltage option (for the UQFN package) and related information throughout the document
- Minor typographical corrections.

Revision C (March 2016)

- Minor typographical corrections.

Revision B (October 2015)

The following is the list of modifications:

- Updated thermal resistances in **Section 1.0, Electrical Characteristics**.
- Updated **Section 2.0, Typical Performance Curves** with new load step screen-shots.

Revision A (June 2015)

- Original release of this document.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	[X](1)	-X	X	/XX
Device	Tape and Reel Option	Output Voltage	Temperature Range	Package

Device:	MCP1711:		150 mA Ultra-Low Quiescent Current, Capacitorless LDO Regulator
Output Voltage:	12	=	1.2V
	18	=	1.8V
	19	=	1.9V
	20	=	2.0V
	22	=	2.2V
	25	=	2.5V
	30	=	3.0V
	33	=	3.3V
	50	=	5.0V
Temperature Range:	I	=	-40°C to +85°C (Industrial)
Packages:	OT	=	Plastic Small Outline Transistor, 5-Lead SOT-23
	5X	=	Plastic Ultra Thin Quad Flatpack No-Leads, 4-Lead 1x1 UQFN

Examples:

a) MCP1711T-12I/OT: Tape and Reel, 1.2V Output Voltage, Industrial temperature, 5LD SOT-23

b) MCP1711T-18I/OT: Tape and Reel, 1.8V Output Voltage, Industrial temperature, 5LD SOT-23

c) MCP1711T-19I/OT: Tape and Reel, 1.9V Output Voltage, Industrial temperature, 5LD SOT-23

d) MCP1711T-22I/OT: Tape and Reel, 2.2V Output Voltage, Industrial temperature, 5LD SOT-23

e) MCP1711T-25I/OT: Tape and Reel, 2.5V Output Voltage, Industrial temperature, 5LD SOT-23

f) MCP1711T-30I/OT: Tape and Reel, 3.0V Output Voltage, Industrial temperature, 5LD SOT-23

g) MCP1711T-33I/OT: Tape and Reel, 3.3V Output Voltage, Industrial temperature, 5LD SOT-23

h) MCP1711T-50I/OT: Tape and Reel, 5.0V Output Voltage, Industrial temperature, 5LD SOT-23

a) MCP1711T-12I/5X: Tape and Reel, 1.2V Output Voltage, Industrial temperature, 4LD UQFN

b) MCP1711T-18I/5X: Tape and Reel, 1.8V Output Voltage, Industrial temperature, 4LD UQFN

c) MCP1711T-20I/5X: Tape and Reel, 2.0V Output Voltage, Industrial temperature, 4LD UQFN

d) MCP1711T-22I/5X: Tape and Reel, 2.2V Output Voltage, Industrial temperature, 4LD UQFN

e) MCP1711T-25I/5X: Tape and Reel, 2.5V Output Voltage, Industrial temperature, 4LD UQFN

f) MCP1711T-30I/5X: Tape and Reel, 3.0V Output Voltage, Industrial temperature, 4LD UQFN

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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