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MCP16501

Cost and Size Optimized PMIC for SAMA5DX/SAM9X6/SAM9X7/SAMA7G Series MPUs

Features

- Input Voltage: 2.7V to 5.5V
- Three 1A Output Current Buck Channels with 100% Maximum Duty Cycle Capability
- 2 MHz Buck Channels PWM Operation
- One Auxiliary 300 mA Low Dropout Linear Regulator (LDO)
- ±1% Voltage Accuracy for DDR (Buck2 Output) and Core (Buck3 Output)
- Pin-Selectable Output Voltages for Buck2: 1.2V, 1.35V, 1.8V and for Buck3: 1.0V, 1.15V, 1.25V
- MPU-Specific Built-in Default Channel Sequencing and nRSTO Assertion Delay
- Support of MPU Hibernate, Low-Power Modes
- Low Noise, Forced PWM (FPWM) and Low I_Q, Light Load, High-Efficiency Mode Available
- Leakage-Free Interfacing to MPU in any Operating Condition through Optimized ESD Protection
- 250 µA Low-Power Mode Typical Quiescent Current Bucks and LDO ON, No Load
- 6 µA Maximum Shutdown Current (V_{IN} = 4.5V, T_J = +105°C)
- Separate LDO EN Input, Compatible to LV Logic
- Cost and Size-Optimized BOM
- Thermal Shutdown and Current Limit Protection
- 24-Pin 4 mm × 4 mm VQFN Package
- -40°C to +125°C Junction Temperature Range
- Passes Automotive AEC-Q100 Reliability Testing

Applications

- High-Performance MPUs Power Supply Solutions
- µC/µP, FPGA and DSP Power

Description

The MCP16501 is a cost and size optimized integrated PMIC, compatible with Microchip's EMPUs (Embedded Microprocessor Units) and associated DRAM Memories. It is compatible with SAMA5DX, SAM9X6, SAM9X7, and SAMA7G MPUs, which are supported by dedicated device variants.

The MCP16501 integrates three DC-DC Buck regulators and one auxiliary LDO, and provides a comprehensive interface to the MPU.

All Buck channels can support loads up to 1A and are 100% duty cycle-capable.

The 300 mA LDO is provided such that sensitive analog loads can be supported.

The DDR memory voltage (Buck2 output) and MPU core voltage (Buck3 output) are selectable by means of two three-state input pins. This method allows greater precision in the output voltage setting by eliminating inaccuracies due to external feedback resistors while minimizing external component count. The voltage selection set allows easy migration across different generations of memory.

The default power channel sequencing is built-in according to the requirements of the MPU. A dedicated pin (LPM) facilitates the transition to Low-Power modes and the implementation of Backup mode with DDR in self-refresh (Hibernate mode).

The MCP16501 features a low no-load operational quiescent current and it draws less than 6 µA (V_{IN} = 4.5V, T_J = +105°C) in full shutdown.

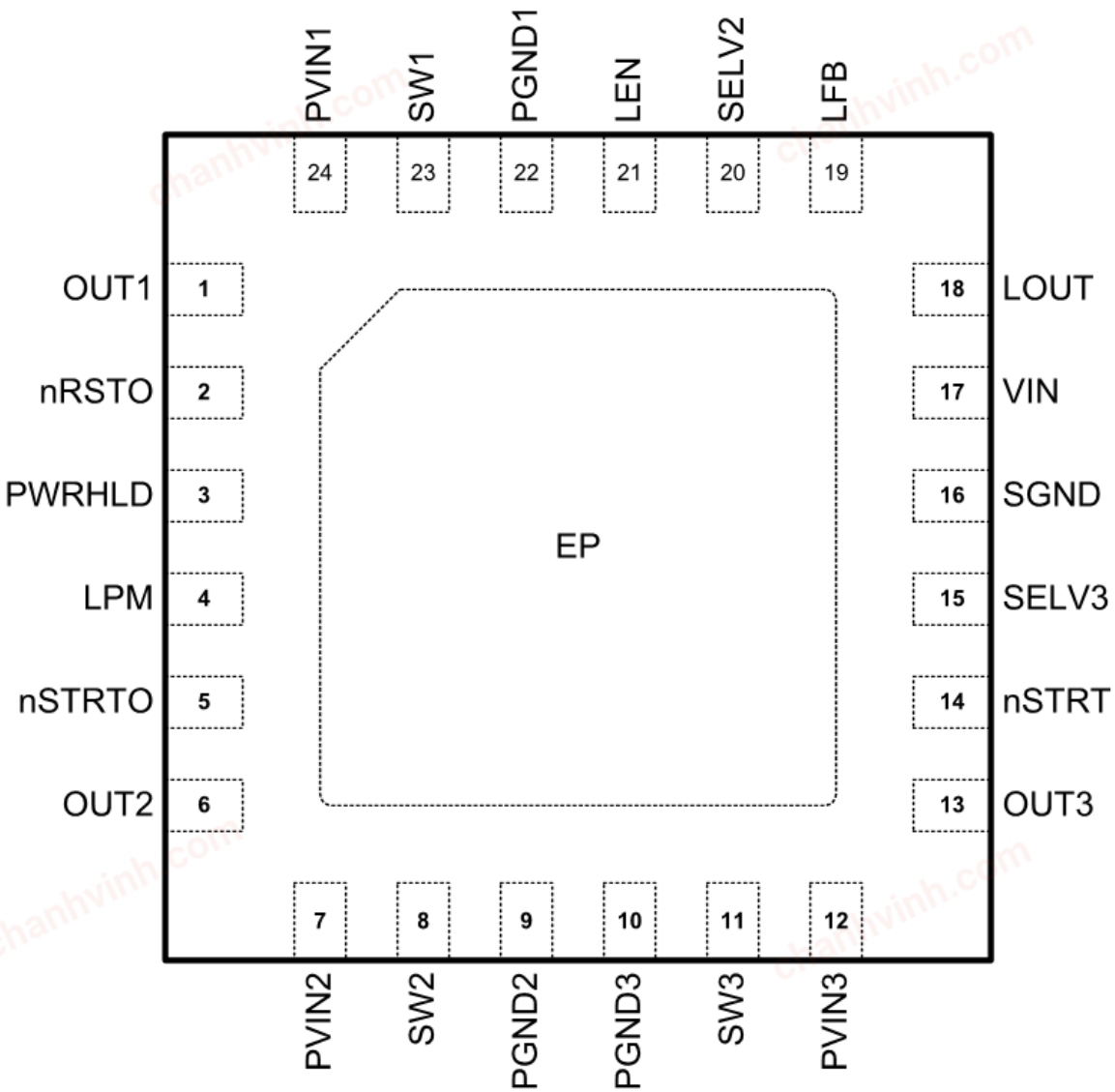
Active discharge resistors are provided on each output. All Buck channels support safe start-up into pre-biased outputs.

The MCP16501 is available in a 24-pin 4 mm x 4 mm VQFN package with an operating junction temperature range from -40°C to +125°C. The MCP16501 also passes automotive AEC-Q100 reliability testing.

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Package Types

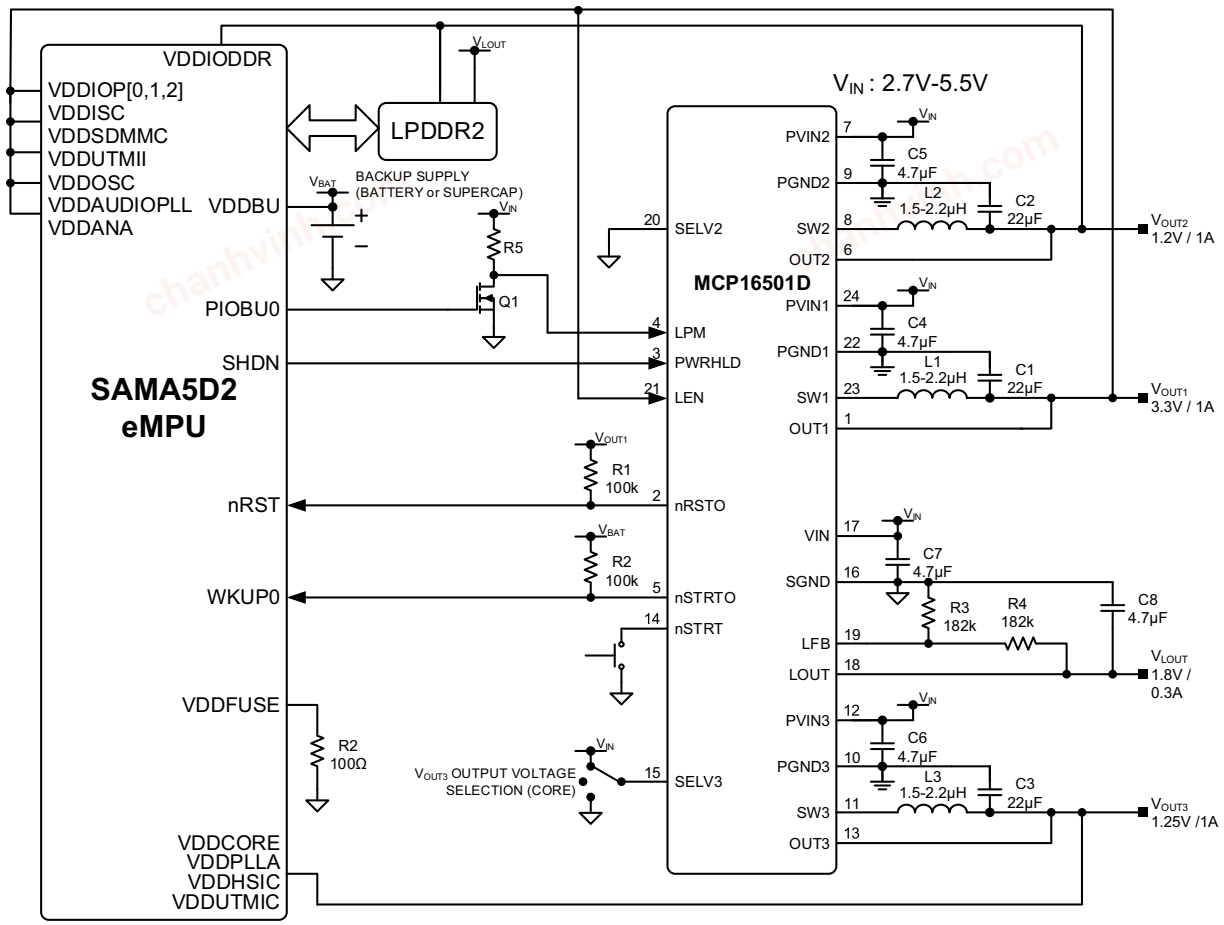


24-Pin 4 mm x 4 mm VQFN – Top View

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Typical Application Circuit

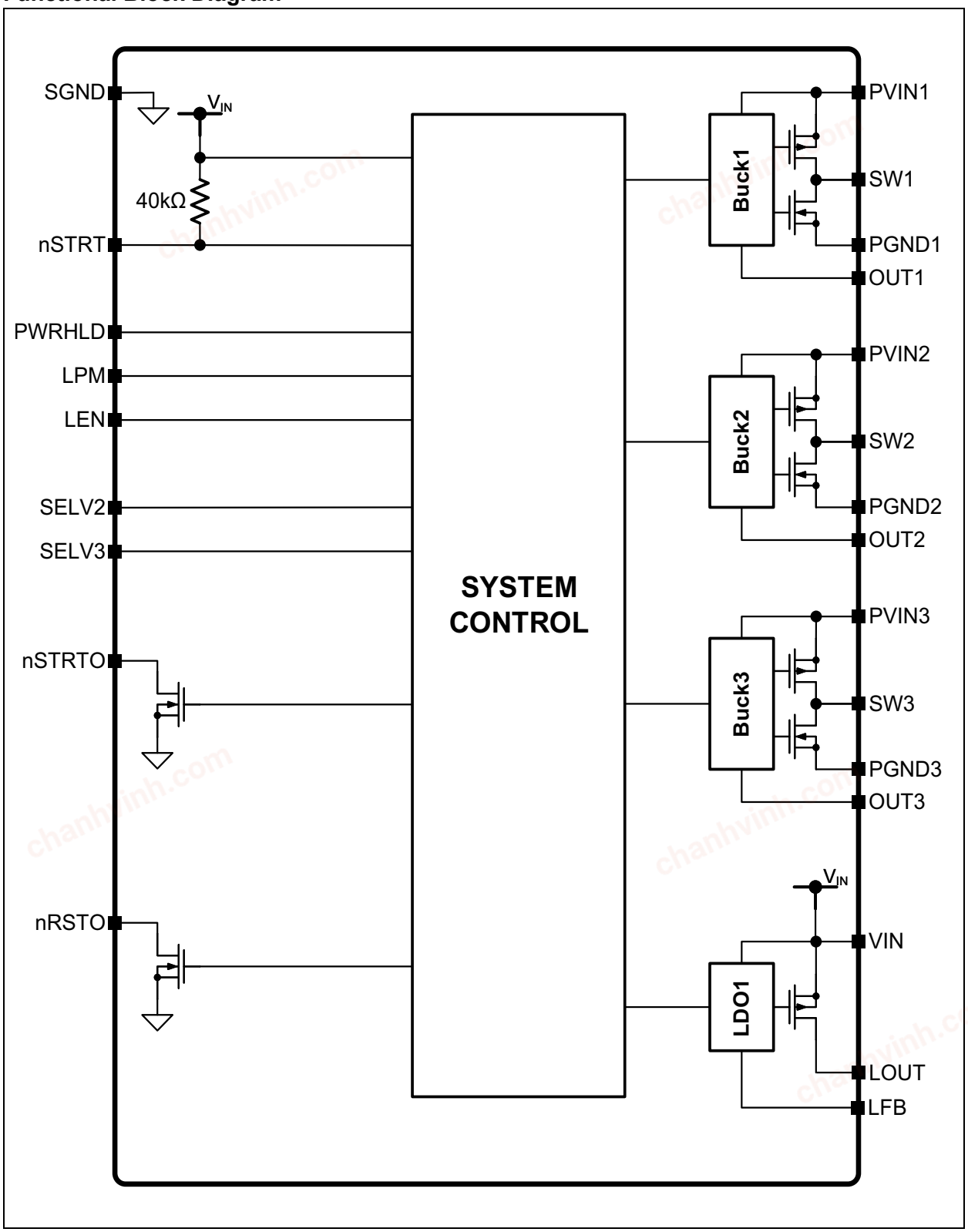


See Table 3-1 for pin information.

Application Schematic of MCP16501D with SAMA5D2 and LPDDR2

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Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

VIN to SGND ..... -0.3V to +6V
Power Supply Voltage Pins PVINx to PGNDx ..... -0.3V to +6V
Power Supply Voltage Pins PVINx to VIN ..... -0.3V to +0.3V
LOUT Pin to GND ..... -0.3V to V_{VIN} + 0.3V
LFB Sense Pins to SGND ..... -0.3V to V_{VIN} + 0.3V
OUTx Sense Pins to SGND ..... -0.3V to +6V
Output Switch Voltage SWx to PGNDx ..... -0.3V to V_{PVINx} + 0.3V
PGNDx to SGND ..... -0.3V to +0.3V
nSTRT, SELV2, SELV3 to SGND ..... -0.3V to V_{VIN} + 0.3V
LPM, LEN, PWRHLD, nRSTO, nSTRTO to SGND ..... -0.3V to +6V
Maximum Junction Temperature ..... 150°C
Storage Temperature ..... -65°C to +150°C
ESD Protection on All Pins:
HBM ..... 2 kV
MM 100V
CDM 750V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise specified: $T_A = T_J$ = +25°C; V_{IN} = VIN = PVINx = 5V; L1 = L2 = L3 = 2.2 µH; C_{OUT1}, C_{OUT2}, C_{OUT3}= 22 µF. **Boldface** type applies for junction temperatures T_J of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
System Input Supply						
Supply Voltage Range	V_{IN}	**2.7**	—	**5.5**	V	—
Undervoltage Lockout Threshold	V_{UVLO_TH}	**2.4**	2.55	**2.7**	V	Turn-on
Undervoltage Lockout Hysteresis	V_{UVLO_HYS}	—	125	—	mV	—
Shutdown (OFF) Current	I_{SHDN}	—	7	**10**	µA	PWRHLD = LPM = 0, nSTRT, nRSTO, nSTRTO floating, V_{IN} = 5.5V
	I_{SHDN_105} (1)	—	4.5	6	µA	PWRHLD = LPM = 0, nSTRT, nRSTO, nSTRTO floating, V_{IN} = 4.5V, T_J = -40°C to +105°C
Hibernate Mode Non-Switching Quiescent Current	I_{QNS_HIB1}	—	110	**150**	µA	I_{OUT2} = 0 mA, Buck2 ON, all other channels off, $V_{OUT2} > V_{OUT2_NOM}$, LPM = 1, PWRHLD = 0
Hibernate Mode Non-Switching Quiescent Current MCP16501D Only	I_{QNS_HIB2}	—	150	**190**	µA	I_{OUT2} = 0 mA, Buck2 ON, LDO ON, all other channels OFF, $V_{OUT2} > V_{OUT2_NOM}$, $V_{LFB} > V_{LFB_NOM}$ LPM = 1, PWRHLD = 0

Note 1: Maximum limit for T_J = -40°C to +105°C based on characterization data.
2: Not production tested.
3: Typical value from bench characterization, maximum value production tested.

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AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified: $T_A = T_J = +25°C$; V_{IN} = VIN = PVINx = 5V; L1 = L2 = L3 = 2.2 µH; C_{OUT1}, C_{OUT2}, C_{OUT3}= 22 µF. **Boldface** type applies for junction temperatures T_J of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Hibernate Mode Operational Quiescent Current (Switching, One Buck Channel ON) **(Note 2)**	I_{QOP_HIB1}	—	110	—	µA	I_{OUT2} = 0 mA, Buck2 ON (V_{OUT2} = 1.2V), all other channels OFF, LPM = 1, PWRHLD = 0
Hibernate Mode Operational Quiescent Current (Switching, One Buck Channel ON and the LDO Channel ON) **(Note 2)**	I_{QOP_HIB2}	—	150	—	µA	I_{OUT2} = I_{LDO} = 0 mA, Buck2 and LDO ON (V_{OUT2} = 1.2V, V_{LDO}= 1.8V), all other channels OFF, LPM = 1, PWRHLD = 0
Low-Power Mode Operational Quiescent Current (Switching) **(Note 2)**	I_{QOP_LPM}	—	205	—	µA	I_{OUTx} = 0 mA, all channels ON excluding LDO, default settings, PWRHLD = LPM = 1
Low-Power Mode Operational Quiescent Current (Switching) **(Note 2)**	I_{QOP_LPM2}	—	250	—	µA	I_{OUTx} = 0 mA, all channels ON including LDO, default settings, PWRHLD = LPM = 1
Active Mode Operational Quiescent Current (Switching) **(Note 2)**	I_{QOP_ACT}	—	14	—	mA	I_{OUTx} = 0 mA, all channels enabled including LDO, default settings, PWRHLD = 1, LPM = 0 SELV2 = LOW, SELV3 = HIGH
Thermal Protection						
Overtemperature Shutdown Threshold **(Note 2)**	T_{TSD}	—	160	—	°C	—
Overtemperature Shutdown Hysteresis **(Note 2)**	T_{TSD_HYS}	—	20	—	°C	—
Buck1						
Input Operating Voltage Range	V_{PVIN1}	**2.7**	—	**5.5**	V	
PVIN1 Shutdown Current	I_{PVIN1_SHDN}	—	0.05	**2**	µA	Regulator disabled, V_{PVIN1} = 5V
Output Voltage Accuracy, FPWM	ACC_OUT_{PWM1}	**-2**	—	**+2**	%	I_{OUT1} = 0 mA
Output Voltage Accuracy, Auto-PFM	ACC_OUT_{PFM1}	**-2**	—	**+2**	%	I_{OUT1} = 0 mA, HCM OFF
Output Voltage Line Regulation **(Note 2)**	$LINE_REG_{PWM1}$	—	0.03	—	%	I_{OUT1} = 0 mA, FPWM, V_{IN} = PVIN1 = VIN = 3.6V to 5.5V
	$LINE_REG_{PFM1}$	—	0.07	—		I_{OUT1} = 0 mA, Auto-PFM, V_{IN} = PVIN1 = VIN = 3.6V to 5.5V
Output Voltage Load Regulation **(Note 2)**	$LOAD_REG_{PWM1}$	—	0.3	—	%	I_{OUT1} = 0A to 1A, FPWM
	$LOAD_REG_{PFM1}$	—	0.5	—	%	I_{OUT1} = 0A to 1A, Auto-PFM
Hysteretic Control Mode Upper Regulation Threshold, Auto-PFM (MCP16501E only)	HCM_TH	**1.7**	2.9	**4.3**	%	I_{OUT1} = 0 mA, PWRHLD = LPM = 1, VIN = PVIN1 = 1.06 x V_{OUT1_NOM}, OUT1 rising, % of V_{OUT1_NOM}
Hysteretic Control Mode Disable Threshold, Auto-PFM (MCP16501E only)	HCM_DIS	—	11.1	—	%	I_{OUT1} = 0 mA, PWRHLD = LPM = 1, VIN = PVIN1 rising, % of V_{OUT1_NOM}

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3: Typical value from bench characterization, maximum value production tested.

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AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified: $T_A = T_J = +25°C$; $V_{IN} = VIN = PVINx = 5V$; L1 = L2 = L3 = 2.2 µH; C_{OUT1}, C_{OUT2}, C_{OUT3}= 22 µF. **Boldface** type applies for junction temperatures T_J of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Hysteretic Control Mode Enable Threshold, Auto-PFM (MCP16501E only)	HCM_EN	**5**	9	**13**	%	I_{OUT1} = 0 mA, PWRHLD = LPM = 1, VIN = PVIN1 falling, % of V_{OUT1_NOM}
Switching Frequency	f_{sw}	**1.8**	2	**2.2**	MHz	FPWM
Maximum Duty Cycle	D_{MAX}	100	—	—	%	Functionality test
Minimum ON Time	T_{ON_MIN1}	—	35	—	ns	FPWM
High-Side Switch On-Resistance	R_{DSonP1}	—	140	160	mΩ	PVIN1 = VIN = 3.6V
Low-Side Switch On-Resistance	R_{DSonN1}	—	120	140	mΩ	PVIN1 = VIN = 3.6V
Start-up POK Bypass Threshold	$V_{POKB_TH_B1}$	**360**	400	**440**	mV	PVIN1 – OUT1, OUT1 rising, PVIN1 = 3.0V, V_{OUT1_NOM} = 3.3V
Start-up POK Bypass Threshold Hysteresis	$V_{POKB_HYS_B1}$	—	50	—	mV	OUT1 falling, PVIN1 = 3.0V
Soft Start Rate	SSR	—	3.125	—	V/ms	—
High-Side Peak Current Limit (Cycle by Cycle)	I_{LIM_HS1}	**1.2**	1.8	**2.4**	A	—
Current Limit Frequency Foldback V_{OUT1} Threshold	V_{TH_FFB1}	—	500	—	mV	—
Hiccup Mode Short-Circuit Protection Wait Time	t_{HICCUP}	—	3x Soft Start Time	—	ms	—
Low-Side Negative Peak Current Limit (FPWM)	I_{LIM_NEG1}	-1.4	-1	-0.8	A	—
Zero Current Detection Threshold	I_{ZCD1}	0	50	110	mA	—
Active Discharge Resistance	R_{DISCH_OUT1}	—	25	—	Ω	DISCH enabled when regulator is disabled
Buck2, Buck3						
Input Operating Voltage Range	V_{PVINx}	**2.7**	—	**5.5**	V	—
PVINx Shutdown Current	I_{PVINx_SHDN}	—	0.05	**2**	µA	Regulator disabled, PVINx = 5V
Output Voltage Accuracy, FPWM	ACC_OUT_{PWMx}	**-1**	—	**+1**	%	I_{OUTx} = 0 mA, 0.9V ≤ V_{OUTx} ≤ 1.3V
		-1.5	—	**+1.5**		I_{OUTx} = 0 mA, V_{OUTx} < 0.9V or V_{OUTx} > 1.3V
Output Voltage Accuracy, Auto-PFM	ACC_OUT_{PFMx}	**-1**	—	**+1**	%	I_{OUTx} = 0 mA, 0.9V ≤ V_{OUTx} ≤ 1.3V
		-1.5	—	**+1.5**		I_{OUTx} = 0 mA, V_{OUTx} < 0.9V or V_{OUTx} > 1.3V
Output Voltage Line Regulation (Note 2)	$LINE_REG_{PWMx}$	—	0.03	—	%	I_{OUT1} = 0 mA, FPWM, V_{IN} = PVIN1 = VIN = 3.6V to 5.5V
	$LINE_REG_{PFMx}$	—	0.07	—		I_{OUT1} = 0 mA, Auto-PFM, V_{IN} = PVIN1 = VIN = 3.6V to 5.5V
Output Voltage Load Regulation (Note 2)	$LOAD_REG_{PWMx}$	—	0.3	—	%	I_{OUTx} = 0A to 1A, FPWM
	$LOAD_REG_{PFMx}$	—	0.5	—		I_{OUTx} = 0A to 1A, Auto-PFM
Switching Frequency	f_{sw}	**1.8**	2	**2.2**	MHz	FPWM

Note 1: Maximum limit for T_J = -40°C to +105°C based on characterization data.

2: Not production tested.

3: Typical value from bench characterization, maximum value production tested.

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AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified: $T_A = T_J = +25°C$; $V_{IN} = VIN = PVINx = 5V$; L1 = L2 = L3 = 2.2 µH; C_{OUT1}, C_{OUT2}, C_{OUT3}= 22 µF. **Boldface** type applies for junction temperatures T_J of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Maximum Duty Cycle	D_{MAX}	100	—	—	%	Functionality test
Minimum ON Time	T_{ON_MINx}	—	35	—	ns	FPWM
High-Side Switch On-Resistance	R_{DSonPx}	—	140	160	mΩ	PVINx = VIN = 3.6V
Low-Side Switch On-Resistance	R_{DSonNx}	—	120	140	mΩ	PVINx = VIN = 3.6V
Soft Start Rate	SSR	—	3.125	—	V/ms	—
High-Side Peak Current Limit (Cycle-by-Cycle)	I_{LIM_HSx}	**1.2**	1.8	**2.4**	A	—
Current Limit Frequency Foldback V_{OUTx} Threshold	V_{TH_FFBx}	—	500	—	mV	—
Hiccup Mode Short-Circuit Protection Wait Time	t_{HICCUP}	—	3x Soft Start Time	—	ms	—
Low-Side Negative Peak Current Limit (FPWM)	I_{LIM_NEGx}	-1.4	-1	-0.8	A	—
Zero Current Detection Threshold	I_{ZCDx}	0	33	110	mA	—
Active Discharge Resistance	R_{DISCH_OUTx}	—	25	—	Ω	DISCH enabled when regulator is disabled
LDO						
Input Operating Voltage Range	V_{LVIN}	**2.7**	—	**5.5**	V	—
Output Voltage Range	V_{LOUT}	0.9	—	3.7	V	Recommended application settings
Stable Output Capacitor Range (**Note 2**)	C_{LOUT}	2.2	—	20	µF	I_{LOUT} ≤ 150 mA – application requirement
		4.7	—	20	µF	I_{LOUT} ≤ 300 mA – application requirement
Operational Quiescent Current	I_{VIN_Q}	—	110	—	µA	I_{LOUT}= 0 mA; only LDO ON; Bucks OFF
LDO Operation Quiescent Current	$I_{VIN_Q_LDO}$	—	45	—	µA	I_{LOUT}= 0 mA; all channels ON including LDO, ΔVIN current when turning on LDO
Feedback Voltage	V_{LFB}	**0.8865**	0.9	**0.9135**	V	VIN = 3.6V
Dropout Voltage (**Note 3**)	V_{DO}	—	170	**500**	mV	I_{LOUT} = 300 mA
Output Voltage Line Regulation	LINE_REG	—	0.024	—	%	VIN = 3.6V to 5.5V, I_{LOUT} = 0.1 mA
Output Voltage Load Regulation	LOAD_REG	—	0.3	—	%	I_{LOUT} = 0.1 mA to 300 mA
PSRR (**Note 2**)	PSRR	—	63	—	dB	f = 1 kHz, I_{OUT} = 20 mA, V_{LOUT} = 1.8V, VIN modulated
		—	46	—	dB	f = 10 kHz, I_{OUT} = 20 mA, V_{LOUT} = 1.8V, VIN modulated
Soft Start Rate	SSR_LFB	—	3.125	—	V/ms	measured on LFB

Note 1: Maximum limit for T_J = -40°C to +105°C based on characterization data.

2: Not production tested.

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AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified: $T_A = T_J = +25°C$; $V_{IN} = VIN = PVINx = 5V$; L1 = L2 = L3 = 2.2 µH; C_{OUT1}, C_{OUT2}, C_{OUT3}= 22 µF. **Boldface** type applies for junction temperatures T_J of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Current Limit	I_{LIM_LOUT}	**310**	420	**550**	mA	VIN = 4.5V, V_{LOUT} = 80% of nominal
Active Discharge Resistance	R_{DISCH_LOUT}	—	25	—	Ω	DISCH =enabled when regulator is disabled
LEN Input						
LEN Logic High Input Voltage, V_{IH}	V_{IH_LEN}	**1.15**	—	—	V	—
LEN Logic Low Input Voltage, V_{IL}	V_{IL_LEN}	—	—	**0.4**	V	—
LEN Input leakage current	I_{LK_LENT}	**-1**	—	**1**	µA	—
nSTRT Input						
Logic High Input Voltage, V_{IH}	V_{IH_nSTRT}	**0.66 V_{VIN}**	—	—	V	VIN = 3.6V – 5.5V
Logic Low Input Voltage, V_{IL}	V_{IL_nSTRT}	—	—	**0.36 V_{VIN}**	V	VIN = 3.6V – 5.5V
Pull-up Resistance	R_{PU_nSTRT}	—	40	—	kΩ	—
nSTRT Deglitch Time	t_{DT_nSTRT}	—	10	—	µs	Falling edge of nSTRT pin
SELV2, SELV3 Three-State Inputs (x = 2, 3)						
High State Threshold Voltage, V_{IHT}	V_{IHT_SELVx}	**V_{VIN} – 0.9V**	—	**V_{VIN} – 0.4V**	V	—
Low State Threshold Voltage, V_{ILT}	V_{ILT_SELVx}	**0.5**	—	**1.0**	V	—
Input Leakage Current High	I_{lkgH_SELVx}	—	0.7	**1**	µA	SELVx = VIN – 0.4V
Input Leakage Current Low	I_{lkgL_SELVx}	**-1**	0.7	—	µA	SELVx = 0.4V
PWRHLD, LPM Logic Inputs (x= PWRHLD, LPM)						
Logic High Input Voltage, V_{IH}	V_{IH_x}	**1.5**	—	—	V	VIN = 3.6V – 5.5V
Logic Low Input Voltage, V_{IL}	V_{IL_x}	—	—	**0.4**	V	VIN = 3.6V – 5.5V
Input Leakage Current	I_{lkg_x}	**-1**	—	**1**	µA	—
Deglitch Time	t_{DT_x}	—	10	—	µs	—
nRSTO, nSTRTO Logic Outputs (x = nRSTO, nSTRTO)						
Output Voltage Low, V_{OL}	V_{OL_x}	—	—	**0.4**	V	VIN = 3.6V – 5.5V, I_{OL} = 2 mA
Leakage Current	I_{lkg_x}	—	—	**1**	µA	5.5V applied, output driver OFF

Note 1: Maximum limit for T_J = -40°C to +105°C based on characterization data.
2: Not production tested.
3: Typical value from bench characterization, maximum value production tested.

TEMPERATURE SPECIFICATIONS(1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_J	-40	—	+125	°C	Steady state
Maximum Junction Temperature	T_{J_MAX}	—	—	+150	°C	Transient
Package Thermal Resistance	θ_{JA}	—	38	—	°C/W	—

Note 1: $T_A = +25°C$; $V_{IN} = PVINx = 5V$; unless otherwise specified.
Bold values indicate -40°C ≤ T_J ≤ +125°C.

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise specified: V_{IN} = VIN= PVINx = 5V; L1 = L2 = L3 = 2.2 µH; C_{OUT1} = C_{OUT2} = C_{OUT3}= 22 µF, T_A = +25°C

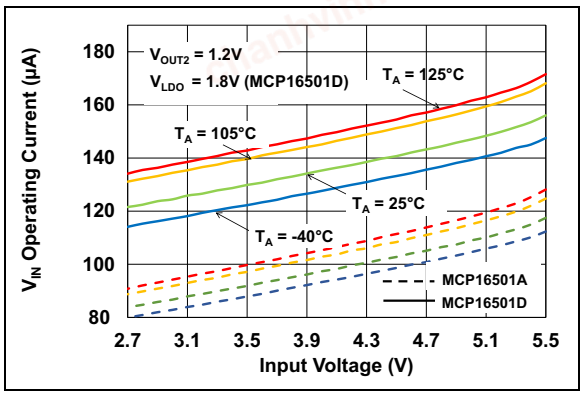


FIGURE 2-1: *V_{IN} Operating Current vs. Input Voltage and Temperature – Hibernate Mode (LPM = High, PWRHLD = Low).*

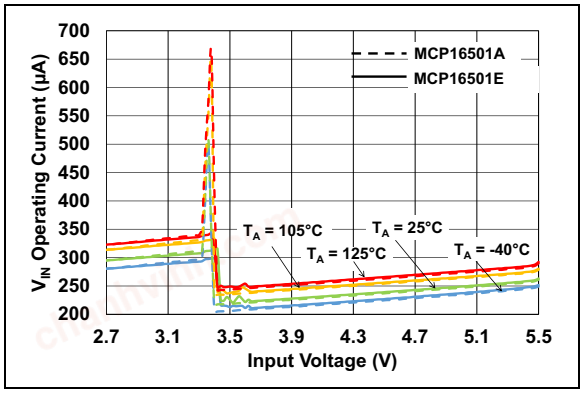


FIGURE 2-2: *V_{IN} Quiescent Current vs. Input Voltage and Temperature – Low-Power Mode (LPM = PWRHLD = High).*

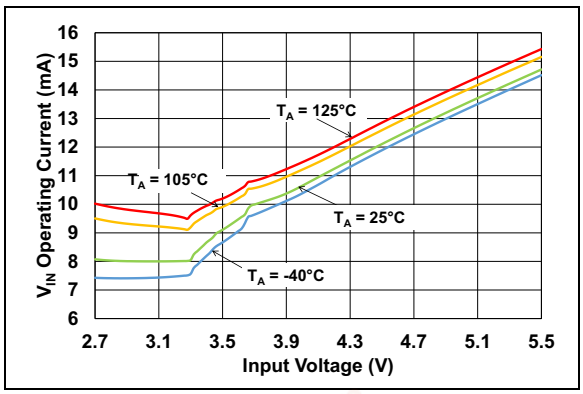


FIGURE 2-3: *V_{IN} Quiescent Current vs. Input Voltage and Temperature – Active Mode (LPM = Low, PWRHLD = High).*

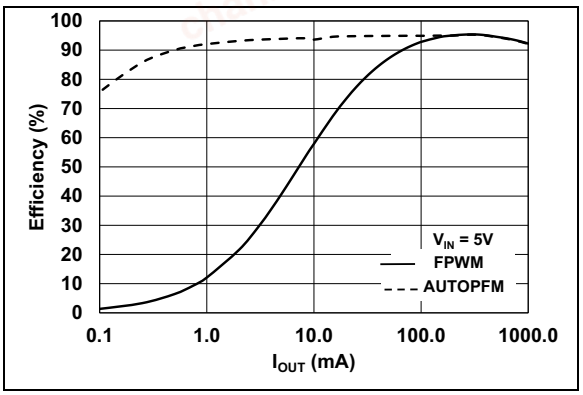


FIGURE 2-4: *Buck1 Efficiency vs. Load Current Measured on PVIN1 (V_{OUT1} = 3.3V).*

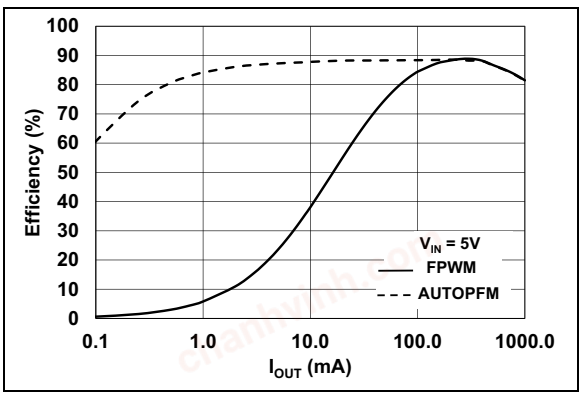


FIGURE 2-5: *Buck2 Efficiency vs. Load Current Measured on PVIN2 (V_{OUT2} = 1.2V).*

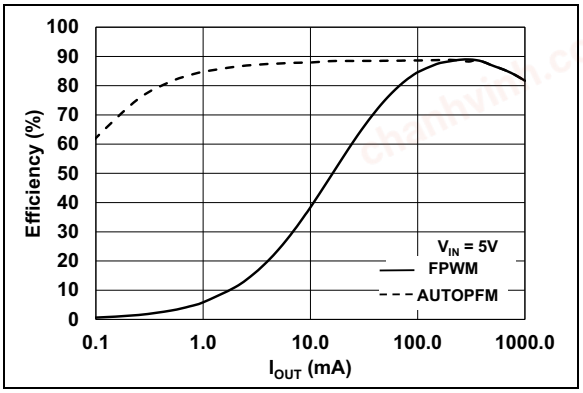


FIGURE 2-6: *Buck3 Efficiency vs. Load Current Measured on PVIN3 (V_{OUT3} = 1.25V).*

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Note: Unless otherwise specified: V_{IN} = VIN = PVINx = 5V; L1 = L2 = L3 = 2.2 µH; C_{OUT1} = C_{OUT2} = C_{OUT3} = 22 µF, T_A = +25°C

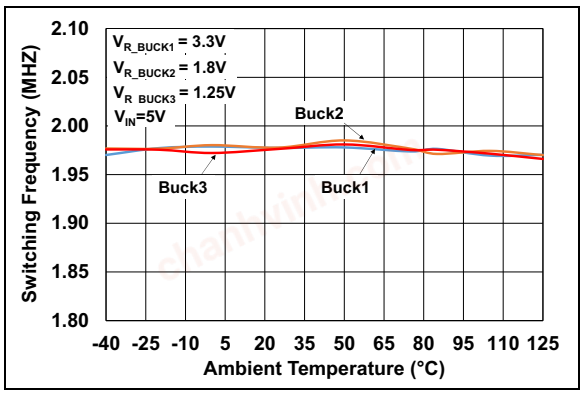


FIGURE 2-7: *Switching Frequency vs. Temperature – Active Mode (LPM = Low, PWRHLD = High).*

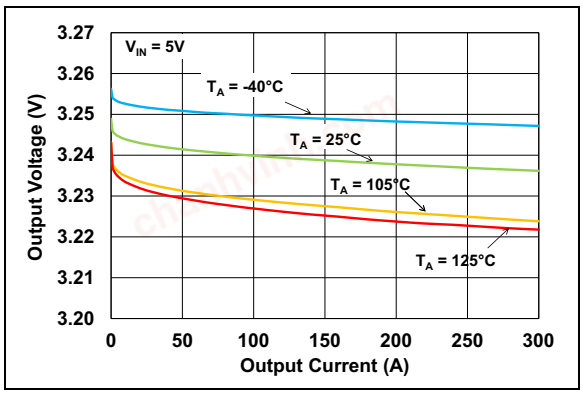


FIGURE 2-10: *LDO Output Voltage vs. Output Current and Temperature (Load Regulation – V_{LOUT} = 3.3V).*

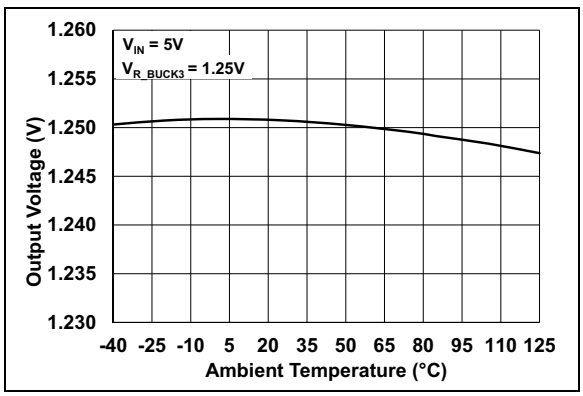


FIGURE 2-8: *Buck3 Output Voltage vs. Temperature – V_{OUT3} = 1.25V, Active Mode (LPM = Low, PWRHLD = High).*

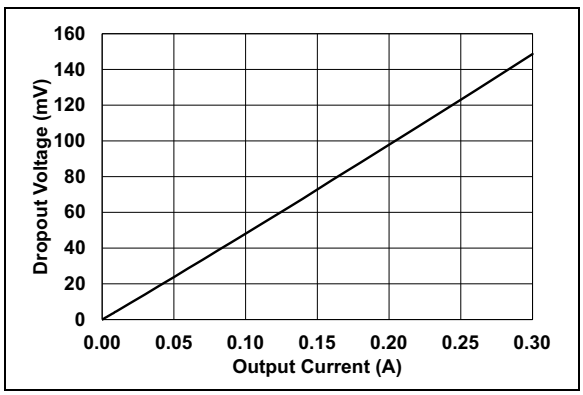


FIGURE 2-11: *LDO Dropout Voltage vs. Load Current.*

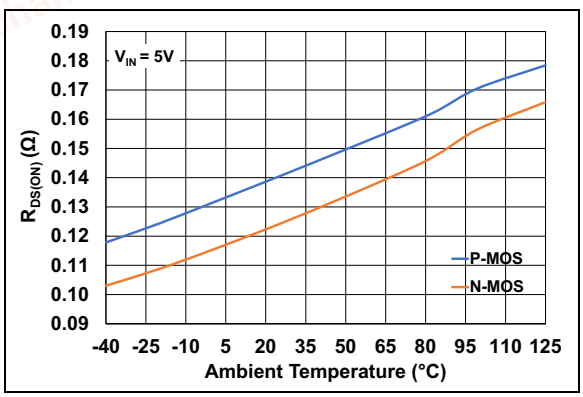


FIGURE 2-9: *MOSFET $R_{DS(ON)}$ vs. Temperature.*

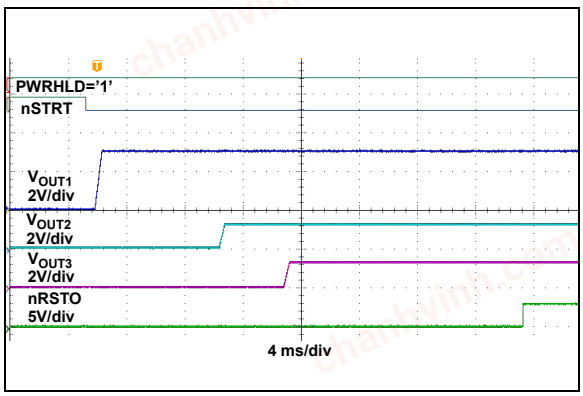


FIGURE 2-12: *nSTRT Start-Up Sequence.*

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Note: Unless otherwise specified: V_{IN} = VIN= PVINx = 5V; L1 = L2 = L3 = 2.2 µH; C_{OUT1} = C_{OUT2} = C_{OUT3} = 22 µF, T_A = +25°C

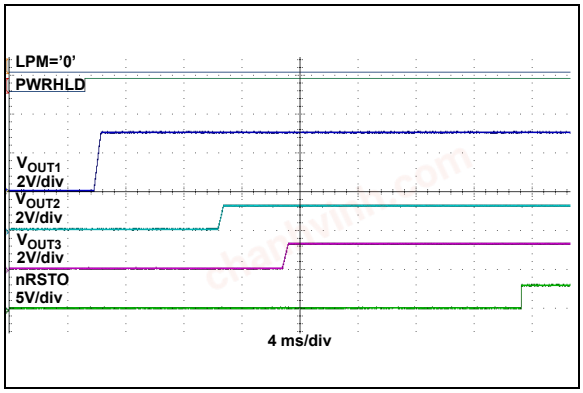


FIGURE 2-13: *PWRHLD Start-Up Sequence.*

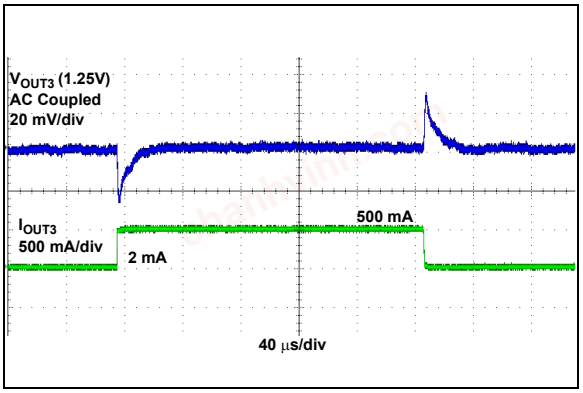


FIGURE 2-16: *Buck3 Transient Response (Active Mode, V_{OUT3} = 1.25V).*

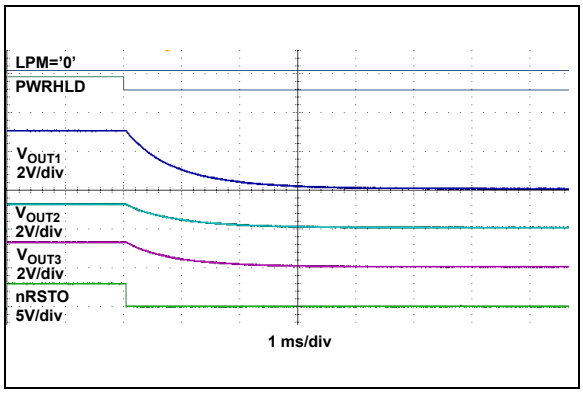


FIGURE 2-14: *PWRHLD Shutdown Sequence.*

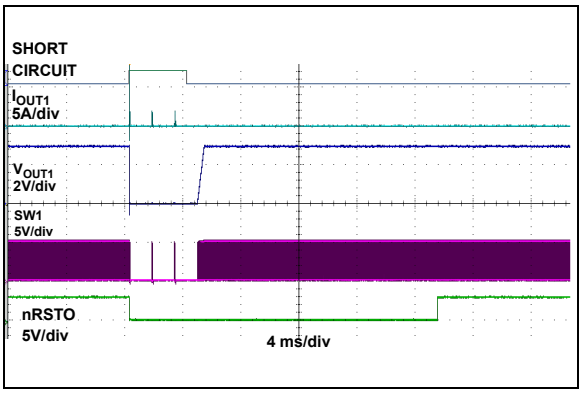


FIGURE 2-17: *Output Short Circuit on V_{OUT1}.*

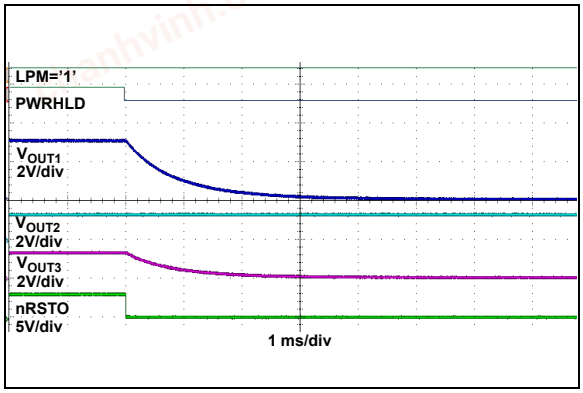


FIGURE 2-15: *Entering Hibernate Mode.*

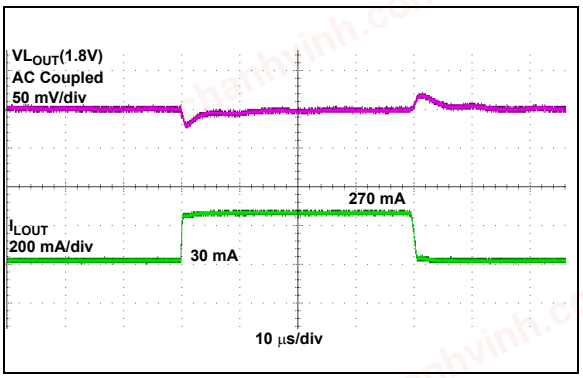


FIGURE 2-18: *LDO Load Transient Response.*

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Note: Unless otherwise specified: V_{IN} = VIN= PVINx = 5V; L1 = L2 = L3 = 2.2 µH; C_{OUT1} = C_{OUT2} = C_{OUT3} = 22 µF, T_A = +25°C

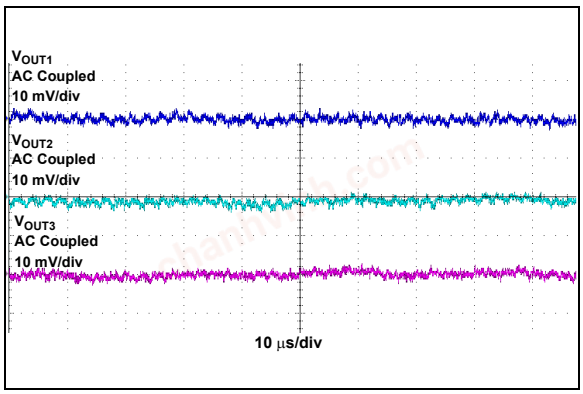


FIGURE 2-19: *Buck Channels Output Voltage Ripple, Active (FPWM) Mode.*

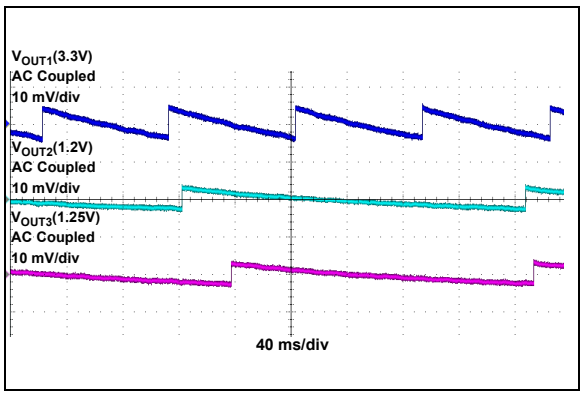


FIGURE 2-20: *Buck Channels Output Voltage Ripple, Low-Power (Auto-PFM) Mode.*

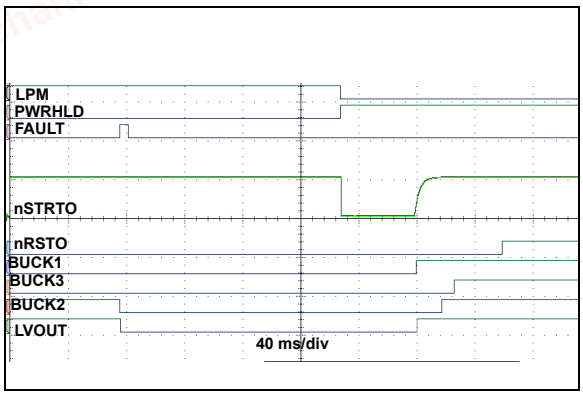


FIGURE 2-21: *MCP16501D Automatic Wake-Up Pulse upon Fault on Active Channels, Hibernate Mode.*

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3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	OUT1	Output Sensing for Buck Channel 1. Connect to the regulation point for V_{OUT1}.
2	nRSTO	Active-Low, Open-Drain Reset Output.
3	PWRHLD	Power Hold Input. Typically asserted as high by the MPU to maintain power after the initial start-up is triggered by nSTRT. PWRHLD is to be asserted as low by the MPU to initiate a PMIC shutdown sequence.
4	LPM	Low-Power Mode Input pin. In combination with PWRHLD, this pin defines the power mode status of the MCP16501.
5	nSTRTO	Active-Low, Open-Drain Start Event Output. nSTRTO is asserted low whenever nSTRT is low.
6	OUT2	Output Sensing for Buck Channel 2. Connect to the regulation point for V_{OUT2}.
7	PVIN2	Power Input Voltage of Buck Channel 2. Connect a ceramic capacitor from PVIN2 to the PGND2 pin to localize pulsed current loops and decouple switching noise.
8	SW2	Switch Node of Buck Channel 2. Internal power MOSFET switches and external inductor connection.
9	PGND2	Power Ground of Buck Channel 2.
10	PGND3	Power Ground of Buck Channel 3.
11	SW3	Switch Node of Buck Channel 3. Internal power MOSFET switches and external inductor connection.
12	PVIN3	Power Input Voltage of Buck Channel 3. Connect a ceramic capacitor from PVIN3 to the PGND3 pin to localize pulsed current loops and decouple switching noise.
13	OUT3	Output Sensing for Buck Channel 3. Connect to the regulation point for V_{OUT3}.
14	nSTRT	Start Event Input. Drive nSTRT to low to initiate a start-up sequence. nSTRT is pulled up internally. A capacitor can be connected to nSTRT to automatically initiate a power-up sequence when the main supply rises.
15	SELV3	Buck Channel 3 Output Voltage Selection pin. Three-state input.
16	SGND	Signal Ground. Connect to reference ground plane.
17	VIN	Input voltage for the LDO and for the analog control circuitry. Decouple VIN to SGND with a 2.2uF (minimum) ceramic capacitor.
18	LOUT	LDO Output. Decouple LOUT to ground with a 2.2 µF (minimum) ceramic capacitor.
19	LFB	LDO FB pin. Connect to an external resistor divider to LOUT for output voltage adjustment.
20	SELV2	Buck Channel 2 Output Voltage Selection pin. Three-state input.
21	LEN	LDO Enable input.
22	PGND1	Power Ground of Buck Channel 1.
23	SW1	Switch Node of Buck Channel 1. Internal power MOSFET switches and external inductor connection.
24	PVIN1	Power Input Voltage of Buck Channel 1. Connect a ceramic capacitor from PVIN1 to the PGND1 pin to localize pulsed current loops and decouple switching noise.
—	EP	Exposed Pad. Connect to ground plane with vias to ensure good thermal properties.

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4.0 DEVICE OPTIONS

The MCP16501 is offered in different options, depending on the target I/O voltage needed external memory type and behavior in bypass situations. Table 4-1 shows the device options that are currently available.

Note: All device variants are generated at the factory with One-Time-Programmable memory, which configures default settings at power-up. Contact your nearest Microchip Sales Office for further assistance on the development of customized device variants.

TABLE 4-1: DEFAULT CONFIGURATIONS

Device Options	MCP16501A	MCP16501B	MCP16501C	MCP16501D	MCP16501E
V_{OUT1}	3.3V	2.8V	3V	3.3V	3.3V
LPDDR2/3	Not supported	Not supported	Not supported	Supported	Not supported
Hysteretic Control Mode (HCM)	Not supported	Not supported	Not supported	Not supported	Supported

4.1 Buck Channels and Related External Components

The MCP16501 Buck channels are based on Peak Current mode control architecture and have internal frequency compensation for the voltage regulation loop. The slope compensation is optimized for inductors in the 1.5 µH to 2.2 µH range. A minimum output capacitor of 22 µF is required for stability. Output capacitance can be increased if necessary; however, it is recommended that the maximum output capacitance value be limited to avoid engaging the Hiccup mode overcurrent protection during the initial soft start ramp. Further details are given in **Section 5.6 "Maximum Simultaneous Capacitive and DC Loading in Soft Start"**.

The recommended input decoupling capacitance on each Buck channel is 4.7 µF.

The Buck channels can operate in either Forced PWM mode (Continuous Inductor Current mode), where the inductor current is allowed to go negative, or in Automatic PFM mode, where the inductor current is prevented from going negative through Zero-Current Detection (ZCD) and diode emulation of the low-side MOSFET.

The switching frequency in Forced PWM mode is nominally 2 MHz.

4.2 LDO Channel and Related External Components

The MCP16501 LDO is designed for operation with low-ESR ceramic output capacitors of 2.2 µF (minimum value) for loads up to 150 mA, and of 4.7 µF (minimum value) for loads up to 300 mA. The total output capacitance must not exceed 20 µF. Recommended capacitor part numbers are given in **Section 5.1 "Recommended External Components"**.

4.3 Control Signals and Power States

4.3.1 INTERFACING SIGNALS

The MCP16501 is interfaced to the host MPU by means of the following signals: nSTRTO (open-drain output), nRSTO (open-drain output), PWRHLD (input) and LPM (input).The ESD protection on each interfacing signal is purposely designed to prevent any leakage from the MPU I/Os, even in the case where the main input power is removed from the MCP16501.

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4.3.2 nSTRT, nSTRTO, PWRHLD FUNCTIONALITY

The nSTRT (push button input) serves as an external wake-up input to the PMIC+MPU system. nSTRT is internally pulled up to VIN and monitored. When the nSTRT is pulled/detected as low (e.g., by means of a push button or any other pull-down device) for longer than a minimum debouncing time, the MCP16501 initiates the turn-on sequence.

The nSTRTO signal is asserted low whenever the nSTRT is detected to be low; otherwise, it is High-Z (typically, nSTRTO has an external pull-up resistor). The only exception to this input (nSTRT)/output (nSTRTO) relationship is the so called Automatic Wake-up Pulse (AWKP) that is described in **Section 4.4.6 "Restart Sequence After Fault and Automatic Wake-up Pulse (AWKP) Generation-MCP16501D only"**(applicable to MCP16501D only).

After the start-up sequence has been initiated, the MCP16501 expects the assertion of the PWRHLD signal (Power-Hold) from the MPU to validate the start-up. PWRHLD could already be high in a typical application using a backup supply. If PWRHLD has not been asserted high by the MPU before the completion of the start-up sequence (i.e., when nRSTO is about to be asserted high), the MCP16501 will automatically initiate a turn-off sequence.

During run time (PWRHLD = High), the nSTRT (thus nSTRTO) can again be asserted low. No automatic action is taken by the MCP16501 in this case.

4.3.3 nSTRT/PWRHLD TYPICAL USE CASES

Depending on the presence of a backup supply and the availability of an external wake-up signal connected at nSTRT (push button input), four different scenarios can be defined for the turn-on of the MCP16501 as described in Figure 4-1.

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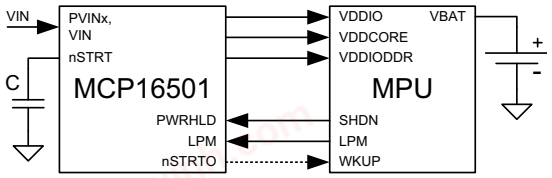
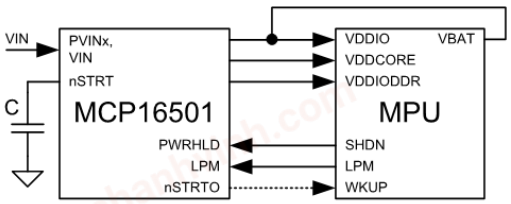
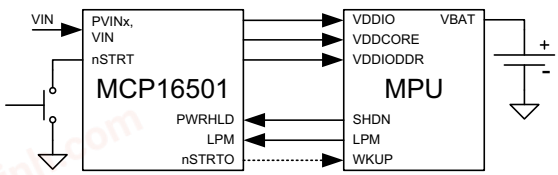
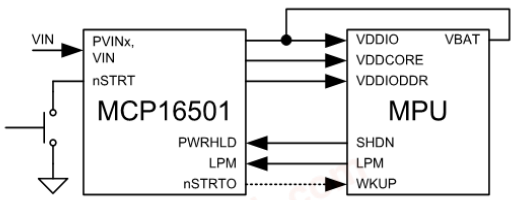
	Applications With a Backup Supply	Applications Without a Backup Supply
Applications Without Start-up Push Button		
	The application starts when V_{IN} ramps up because of the capacitor C, which delays the rise of nSTRT with respect to V_{IN} and causes nSTRT to appear low as soon as the MCP16501 is powered. Note that PWRHLD (= SHDN from MPU) was set to '1' at the time the battery was mounted on the PCB (i.e., at the time of manufacturing). The power channels of MCP16501 are turned off by the MPU by setting SHDN = 0. The MPU is then in Backup mode. If supported, the DDR can also be placed in Backup Self-Refresh (BSR) mode by setting LPM = 1 before SHDN = 0. To wake up the application from Backup mode, a wake-up event must be generated for the SHDWC (Shutdown and Wake-up Controller) of the MPU. This can be an internal event (e.g., RTC, RTT alarm, TAMPER detection) or an event on an I/O of the SHDWC (e.g., wake-up from a wireless module). The MPU will then set SHDN = 1 and the low-to-high transition of PWRHLD will cause the MCP16501 to restart. If V_{IN} is cycled while the MPU is in Backup mode (SHDN = 0), the MCP16501 restarts automatically and sends a wake-up event to the MPU on nSTRTO (WKUP). If this wake-up event was not enabled in the MPU SHDWC configuration, SHDN will stay low and the MCP16501 will turn off at the end of the start-up sequence, because PWRHLD has not been set high. If this wake-up event is enabled, SHDN will immediately go high, thus confirming the start-up sequence for the MCP16501 and the application will restart.	The application starts when V_{IN} ramps up because of the capacitor C, which delays the rise of nSTRT with respect to V_{IN} and causes nSTRT to appear low as soon as the MCP16501 is powered. PWRHLD (= SHDN from MPU) is set to '1' as soon as VBAT (= VDDIO) is above its internal POR threshold (around 1.5V). The power channels of MCP16501 are turned off by the MPU by setting SHDN = 0. In this case, the MPU is not in Backup mode; it is simply completely off. LPM cannot be used, nor can SHDN be set to '1' because the supply voltage of the SHDWC controller is missing. From the OFF state, the application can only be restarted by cycling power on V_{IN}.
Applications With Start-up Push Button (at nSTRT)		
	The application does not immediately start when V_{IN} ramps up. The button must be pressed (nSTRT = Low) to start the MCP16501. Note that PWRHLD (= SHDN from MPU) was set to '1' at the time the battery was mounted on the PCB (i.e., at the time of manufacturing). The power channels of MCP16501 are turned off by the MPU by setting SHDN = 0. The MPU is then in Backup mode. If supported, the DDR can also be placed in Backup Self-Refresh (BSR) mode by setting LPM = 1 before SHDN = 0. To wake up the application from Backup mode, a wake-up event must be generated for the SHDWC (Shutdown and Wake-up Controller) of the MPU. This can be an internal event (e.g., RTC, RTT alarm, TAMPER detection) or an event on an I/O of the SHDWC (e.g., wake-up from a wireless module). The MPU will then set SHDN = 1 and the low-to-high transition of PWRHLD will cause the MCP16501 to restart. If V_{IN} is cycled while the MPU is in Backup mode (SHDN = 0), the MCP16501 does not restart automatically. To restart the application, the button must be pressed and nSTRTO (WKUP) be an enabled wake-up event. The DDR supply loss, due to an input power loss while in BSR mode, will be managed by software (i.e., by reloading the contents of the DDR).	The application does not immediately start when V_{IN} ramps up. The button must be pressed to start the MCP16501. PWRHLD (= SHDN from MPU) is set to '1' as soon as VBAT (= VDDIO) is above its internal POR threshold (around 1.5V). The power channels of MCP16501 are turned off by the MPU by setting SHDN = 0. In this case, the MPU is not in Backup mode; it is simply completely off. LPM cannot be used, nor can SHDN be set to '1' because the supply voltage of the SHDWC controller is missing. To restart the application, the push button must be pressed.

FIGURE 4-1: *Illustration of Start-Up Mechanisms for Various MPU Configurations.*

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4.3.4 PWRHLD, LPM, LEN AND POWER STATES DEFINITIONS

PWRHLD and LPM define different power states which are illustrated in Table 4-2. These are default definitions for the MCP16501A. Other default definitions are possible for different or customized product variants.

The LDO operation is completely independent of the power states and is controlled by the LEN pin. The only exception to this is in the case of MCP16501D, used in LPDDR2 applications where the LDO is used to power the memory alongside Buck2. For more details on this see **Section 5.3, LPDDR2 Support with Hibernate Mode-MCP16501D Only**.

Other logic combinations of PWRHLD and LPM are forbidden. The initial state is the OFF state (shutdown).

The process by which the MCP16501 abandons the OFF state and enters the other possible power states is defined as the power-up sequence, which is described in **Section 4.4.1 "Typical Power-up Sequence and Timing"**. The following state diagram in Figure 4-2 illustrates the power states of MCP16501 and their typical and/or permissible dynamic transitions.

TABLE 4-2: DEFAULT POWER STATES DEFINITION (MCP16501A)

PWRHLD	LPM	Buck1	Buck2	Buck3	LDO	nRSTO	Power State
0	0	OFF	OFF	OFF	LEN Controlled	Low	OFF
0	1	OFF	ON Auto-PFM	OFF	LEN Controlled	Low	Hibernate mode
1	1	ON Auto-PFM	ON Auto-PFM	ON Auto-PFM	LEN Controlled	High-Z	Low-Power mode
1	0	ON FPWM	ON FPWM	ON FPWM	LEN Controlled	High-Z	Active mode

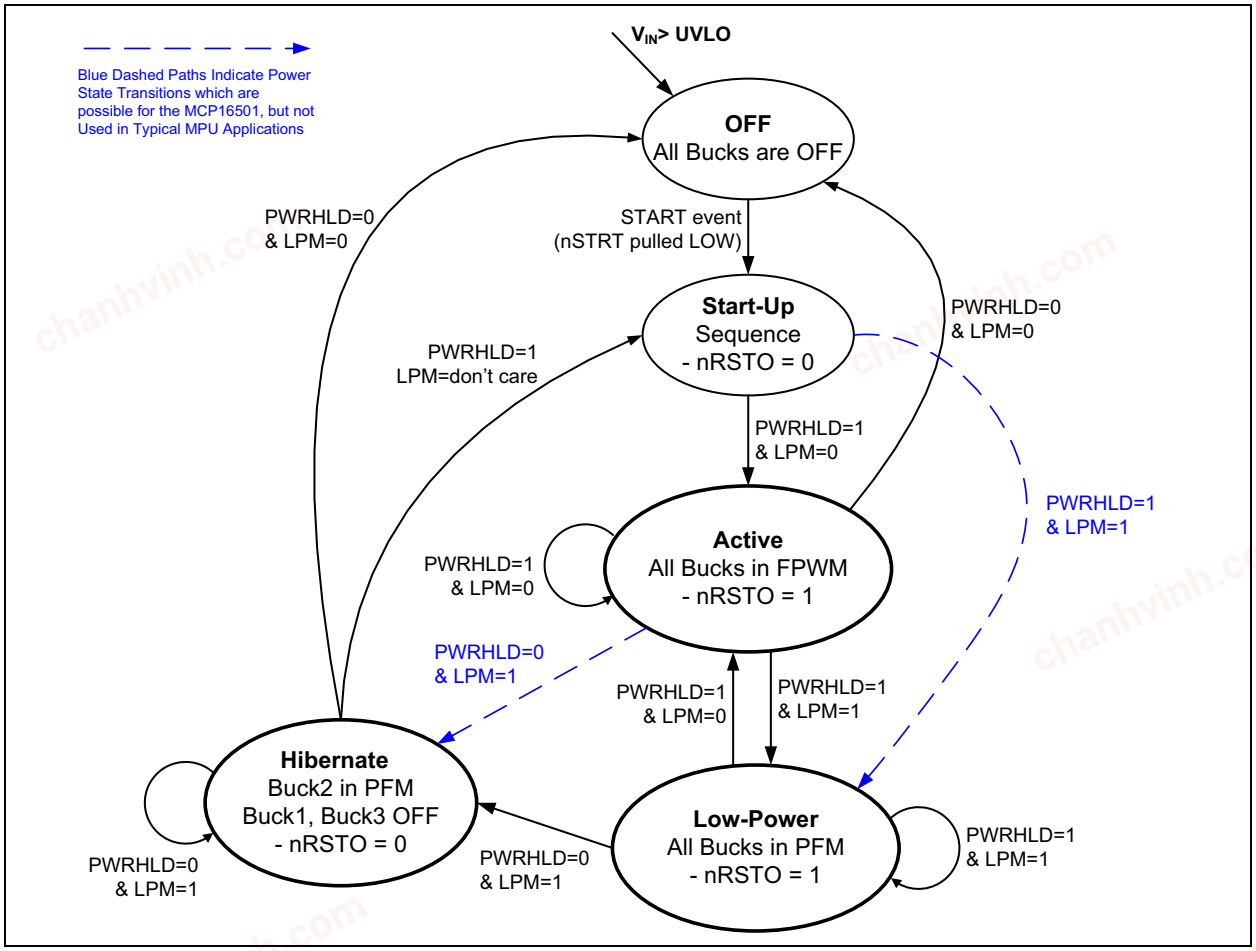


FIGURE 4-2: *Finite State Machine (FSM) States Diagram for MCP16501.*

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4.3.5 SELV2 AND SELV3 PINS

SELV2 and SELV3 pins are meant to program the default settings of some rails that must be activated during the power-up sequence, but whose voltage values are application-dependent. These are Buck2 and Buck3, the first being dedicated to DDRx/LPDDRx power, while the latter being dedicated to core power.

The default values are selectable among three options, corresponding to three different states of the relevant pin: connected to ground (Low), connected to input supply (High) or left unconnected (High-Z).

The Buck2 default voltage can be selected by means of the SELV2 pin as follows:

TABLE 4-3: V_{OUT2} DEFAULT VOLTAGE VS. SELV2 PIN

SELV2 Status	V_{OUT2} Voltage	DDR Type
Low	1.2V	LPDDR2, LPDDR3
High-Z	1.35V	DDR3L
High	1.8V	DDR2

The Buck3 default voltage can be selected by means of the SELV3 pin as follows:

TABLE 4-4: V_{OUT3} DEFAULT VOLTAGE VS. SELV3 PIN

SELV3 Status	V_{OUT3} Voltage	eMPU Type
Low	1V	SAM9-5
High-Z	1.15V	SAM9-6, SAM9-7 and SAMA7G
High	1.25V	SAMA5D2x

Note: SELV2 and SELV3 are always hardwired in the final application and they cannot be changed on-the-fly during operation.

The statuses of SELV2 and SELV3 are frozen in a snapshot as soon as the VIN voltage exceeds the turn-on Undervoltage Lockout Threshold (UVLO) as specified in the **"Electrical Characteristics"** table. Any changes of the SELV2 and SELV3 pins will have no effect after the snapshot, and VIN must fall under the turn-off (lower) UVLO threshold to unfreeze the snapshot.

Both pins are intended to be connected to GND (0V), to VIN or left floating in the application. When left floating, internal circuitry is initially activated to bias SELV2 and SELV3 at start-up for proper three-state (floating state) detection.

For **"Electrical Characteristics"** table specification purposes, the High State Threshold Voltage (V_{IHT}) and Low State Threshold Voltage (V_{ILT}) of SELV2 and SELV3 pins are given. They have both a minimum and a maximum value specification.

At the time the snapshot is taken, it is recommended that those Min. and Max. values be used and interpreted as follows:

- If $V_{IHT}(MAX) < V(SELVx) \leq V(VIN)$ → SELVx is considered HIGH
- If $0V \leq V(SELVx) < V_{ILT}(MIN)$ → SELVx is considered LOW
- If $V_{ILT}(MAX) < V(SELVx) < V_{IHT}(MIN)$ → SELVx is considered floating

If $V_{IHT}(MIN) \leq V(SELVx) \leq V_{IHT}(MAX)$ or $V_{ILT}(MIN) \leq V(SELVx) \leq V_{ILT}(MAX)$, then the logic status of SELVx may not be interpreted correctly. Therefore, if the end user chooses a connection different than the recommended connection to GND, VIN or no connection, then any usage of the SELVx pins within those boundaries must be avoided. This is also illustrated in Figure 4-3.

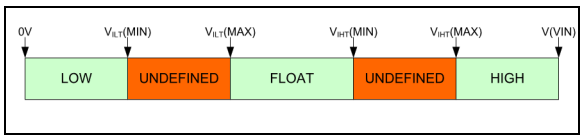


FIGURE 4-3: *SELVx High, Low and Float States Threshold.*

4.3.6 nRSTO (RESET OUTPUT) PIN

The nRSTO pin is an active-low, open-drain output pin that keeps the MPU in a Reset state. The nRSTO pin is released (i.e., goes High-Z) with a 16ms delay upon successful completion of a start-up sequence. nRSTO is immediately asserted low when either the VIN voltage falls below the UVLO threshold, or a Fault condition is detected at system level (such as a Thermal Shutdown) or an overcurrent condition is detected on the Buck channels. See **Section 5.5 "Protections"** for more details on the Faults that would cause the nRSTO signal low assertion. nRSTO also goes low when the Hibernate mode is entered.

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4.4 Power-up/Power-Down/Hibernate Sequences and Timings

4.4.1 TYPICAL POWER-UP SEQUENCE AND TIMING

The typical scenario applies to MPU applications, where:

- I/O voltage (VDDIO) and, if applicable, auxiliary LDO rail is started first (at time t_1), by connecting LEN to the VDDIO output (MCP16501D only).
- DDR supply/DDRIO voltage (VDDIODDR) is started next after delay t_2. From the MPU perspective, t_2 is not mandatory, but it facilitates the use of an external 1.8V DC-DC or LDO for LPDDR2/3 (VDDIODDR being the 1.2V supply of the LPDDR2/3). This DC-DC can be initially sequenced to VDDIO at start-up and maintained ON by VDDIODDR for Hibernate mode (backup self-refresh).
- VDDCORE (and VDDCPU for other MPUs) voltages are started last, after a delay of t_3.
- Upon successful start-up of all the rails in the power-up sequence, after delay t_4, the Reset signal (nRSTO) is deasserted and software execution can start.

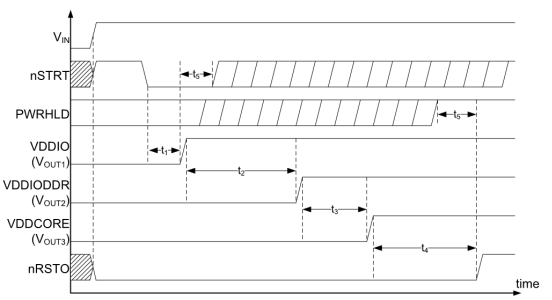
The start-up sequence can be initiated in two different ways, also depending on the presence of a backup supply in the application:

1. **nSTRT event (nSTRT pin pulled low), maintained by PWRHLD assertion.** In applications with a backup battery, the PWRHLD signal is typically already high before the nSTRT event.
2. **A low-to-high transition of the PWRHLD signal, regardless of the nSTRT event.** This is only possible in applications with backup supply. This mode is typically originated by an external wake-up event asserted by a peripheral device to the MPU Shutdown and Wake-up Controller (SHDWC), which is still powered in Backup mode.

Note:	The nSTRT event needs the assertion of PWRHLD to have the power-up sequence completed successfully. If PWRHLD is not yet high at the time nRSTO is to be asserted, the MCP16501 automatically initiates a turn-off sequence without any positive glitches on nRSTO.

Delay t_1 acts as a debouncing delay of the nSTRT event. Therefore, nSTRT must be detected as low continuously during t_1 to validate the start-up event and initiate the first sequence step. After the first sequence step is started (at t_1), nSTRT can be released to its high level at any time. Also, subsequent high-low-high toggling of nSTRT during the execution of the start-up sequence, while visible at the nSTRTO output, will be ignored by the sequencer and it will *not* reset the start-up sequence under execution.

The following timing diagram in Figure 4-4 shows the typical sequence for Case 1:



Where:

t_1 = Delay from nSTRT falling to first output V_{OUT1} starting (default 0.5 ms + device wake-up time, about 100 µs)

t_2 = Time from V_{OUT1} established to V_{OUT2} starting (default 8 ms)

t_3 = Time from V_{OUT2} established to V_{OUT3} starting (default 4 ms)

t_4 = Time from V_{OUT3} established to nRSTO deassertion (default 16 ms)

t_5 = Setup/hold times, min. 0 µs (internal filtering applies)

FIGURE 4-4: *Start-Up from nSTRT Timing Diagram.*

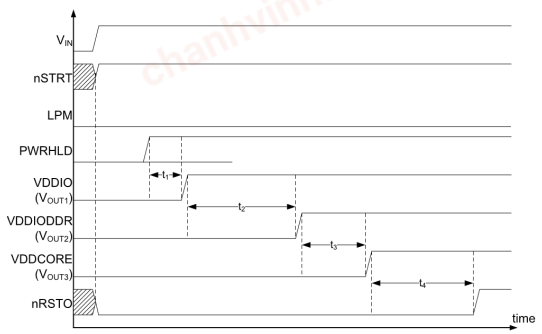
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For the different OTP options for the t_1 to t_4 timings, see the respective values in **"Configuration Options"**.

For power supplies starting at t_1, additional delay time interval is added to the device wake-up time.

The following timing diagram in Figure 4-5 shows the typical sequence for Case 2:



Where:

t_1 = Delay from PWRHLD asserted to first output V_{OUT1} starting (default 0.5 ms + device wake-up time, about 100 µs)

t_2 = Time from V_{OUT1} established to V_{OUT2} starting (default 8 ms)

t_3 = Time from V_{OUT2} established to V_{OUT3} starting (default 4 ms)

t_4 = Time from V_{OUT3} established to nRSTO deassertion (default 16 ms)

FIGURE 4-5: *Start-Up from PWRHLD Timing Diagram.*

For all sequences described above, LPM can be assumed to be low. The MPU will assert LPM after some time, based on software decision, to enter the Low-Power mode.

4.4.2 POWER-UP SEQUENCE FLOWCHART

The start-up sequence is divided into three steps and each Buck regulator is assigned to a specific sequence step:

- Step 1 (Buck1) regulator is started after a delay (t_1) from the start-up event. If the start-up event is no longer valid as the instant t_1 expires, the start-up sequence is aborted before the first regulator is started.
- Step 2 (Buck2) regulator is started after a delay (t_2) since the completion of the sequence Step 1 (regulator enabled at Step 1 has been powered up correctly).
- Step 3 (Buck3) regulator is started after a delay (t_3) from the completion of the sequence Step 2 (regulator enabled at Step 2 has been powered up correctly).

The subsequent assertion of nRSTO is determined by the status of all regulators that have been turned on during the power-up sequence Their status is checked before starting counter t_4 and again checked at the expiration of t_4 to have nRSTO deasserted.

After the completion of the power-up sequence (i.e., at the time instant nRSTO is deasserted), the MCP16501 will enter the Power modes state machine operation defined by the LPM and PWRHLD signals, and the corresponding device setting.

Some regulators which are supposed to turn on in the power-up sequence may fail to power-up correctly.

In this case, the sequencing engine adds a 32 ms waiting time to allow the affected regulators to recover. After the expiration of the 32 ms period, if the affected regulators have still not recovered, the start-up sequence is aborted and the MCP16501 returns to its OFF state.

The start-up sequence flowchart is described in Figure 4-6.

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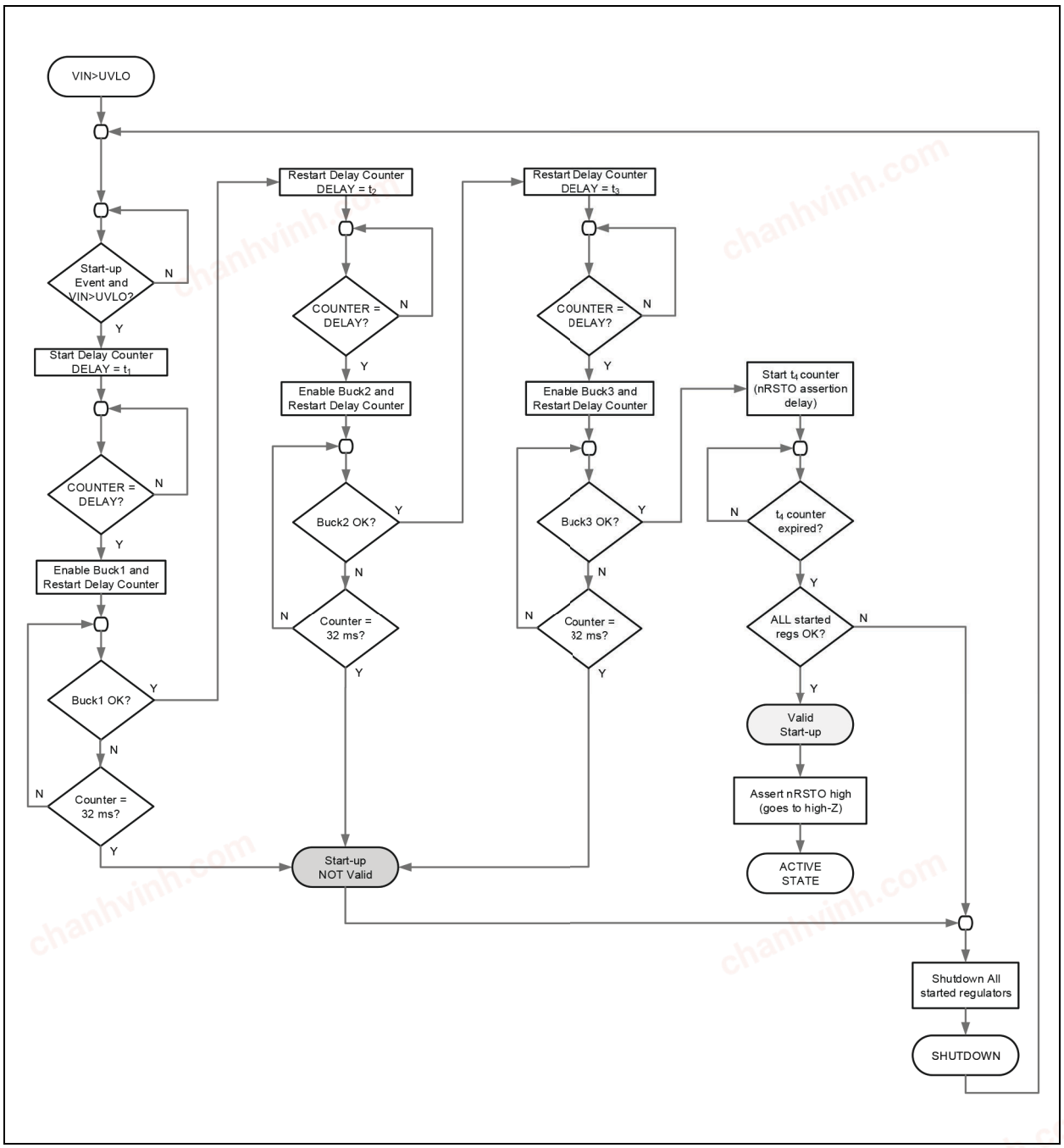


FIGURE 4-6: *Start-Up Sequence Flowchart.*

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4.4.3 DROPOUT SAFE START-UP SEQUENCE FEATURE

The start-up sequence management of MCP16501 ensures predictable timing between subsequent steps, even if some power channels may operate in dropout conditions with moderate loading.

This situation might occur for Buck1 because its output voltage range (up to 3.7V) is overlapping the input supply range (2.7V – 5.5V).

This operating condition is frequently encountered in battery-powered applications. For example, some loads designed for a 3.3V nominal supply voltage may not be able to withstand the fully replenished battery voltage (around 4.2V), and therefore, require a front-end regulator. However, some loads could still operate when the battery voltage has decreased low enough to push their front-end regulator into dropout.

For example, if the battery voltage is around 3.1V and the Buck1 output voltage is also set to 3.3V, it is still desirable to start Buck1 and proceed throughout the start-up sequence, even if the POK (Power OK) threshold for Buck1 may not be reached, since Buck1 is still delivering a voltage within the I/O operating voltage range. This would allow a better exploitation of the battery because the cutoff voltage is no longer dictated by the onset of the dropout of the 3.3V regulator (Buck1) and by its POK threshold.

By means of a dedicated circuit that monitors the input-output differential during start-up of the potentially affected regulators, the MCP16501 can still ensure a proper start-up. The MPU can then detect the anomaly (e.g. by measuring the output of Buck1) and decide either to continue operation or to shut down the system.

The Start-up POK Bypass Threshold is the relevant **"Electrical Characteristics"** parameter that defines the acceptable level of input-output differential, to continue through the start-up sequence, in lack of the normal POK.

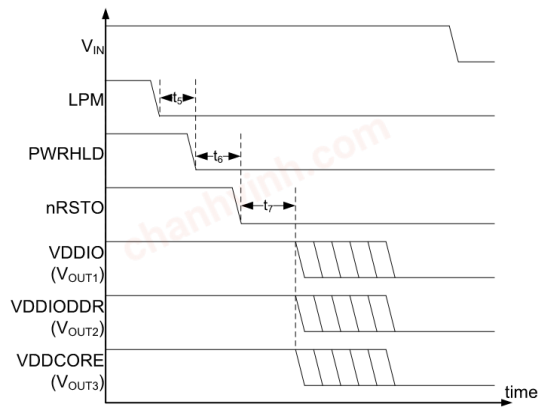
4.4.4 TYPICAL POWER-DOWN SEQUENCE AND TIMING

The power-down (shutdown) sequence can be initiated by the MPU by deasserting PWRHLD (LPM being already low or deasserted simultaneously). This method assumes that the MCP16501 is in any operating state (i.e., is outside the start-up sequence).

After PWRHLD has been deasserted nRSTO will immediately be asserted low by the MCP16501. After that, all active channels will be turned off, with the exception of the LDO which is controlled by LEN. For the MCP16501D, the LDO will be turned off by virtue of the connection of LEN to VOUT1.

The turn-off of each channel also activates the active discharge (if enabled) on the same channel.

The timing diagram in Figure 4-7 shows the typical sequence for the power-down.



Where:

t_5 = Setup time, LPM = 0 to PWRHLD = 0: Min. 0 µs (internal filtering applies)

t_6 = Delay from PWRHLD deasserted to nRSTO asserted: Min. 0 µs, max. 10 µs (not a strict requirement)

t_7 = Delay from nRSTO asserted to first V_{OUTx} turn-off: Min. 0 µs, max. 10 µs (not a strict requirement)

FIGURE 4-7: *Power-Down (Shutdown) Sequence Timing Diagram.*

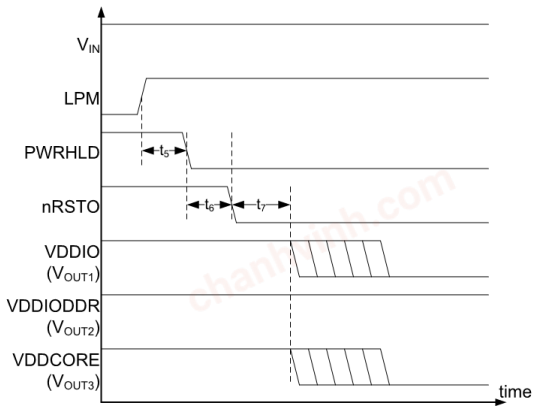
4.4.5 TYPICAL HIBERNATE SEQUENCES AND TIMING

The Hibernate mode entering sequence is similar to the power-down, with the only difference is that LPM will be asserted high by the MPU before deassertion of PWRHLD, or at least at the same time PWRHLD is deasserted (due to internal filtering, the setup time t_5 can be as low as 0 µs). For example, taking the MCP16501A variant into consideration, the V_{OUT2} rail (and/or other rails which are defined as ON state in Hibernate mode by overwriting the default settings) will remain active, while V_{OUT1} and V_{OUT3}, will be immediately disabled. In Hibernate mode, the DDRx/LPDDRx will typically be in Backup Self-Refresh mode (BSR).

The following timing diagram in Figure 4-8 shows the typical Hibernate mode sequence for a device variant that keeps only V_{OUT2} turned on in Hibernate mode (such as MCP16501A).

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Where:

t_5 = Setup time, LPM = 1 to PWRHLD = 0: Min. 0 µs (internal filtering applies)

t_6 = Delay from PWRHLD deasserted to nRSTO asserted: Min. 0 µs, max. 10 µs (not a strict requirement)

t_7 = Delay from nRSTO asserted to first V_{OUTX} turn-off: Min. 0 µs, max. 10 µs (not a strict requirement)

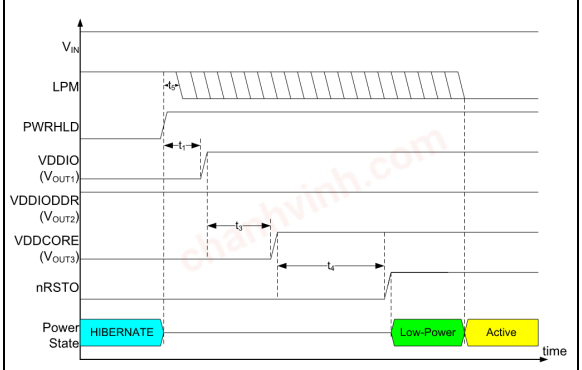
FIGURE 4-8: *Entering Hibernate Mode Timing Diagram.*

From the Hibernate state, the system can:

1. Move to OFF state (if LPM also goes low, the V_{OUT2} can be immediately turned off); or
2. Initiate another start-up sequence (with the exception of Buck2 which is already active) by a low-to-high transition of PWRHLD.

The timing diagram of a start-up sequence from Hibernate mode is shown in Figure 4-9. After the assertion of PWRHLD, the MPU may deassert LPM at any time. Due to internal filtering, simultaneous transition of LPM and PWRHLD is allowed (hold time t_5 can be 0 µs).

Depending on the time at which LPM is deasserted, the MCP16501 may transition through the Low-Power state or not.



Where:

t_1 = Delay from PWRHLD asserted to first supply V_{OUT1} starting (default 0.5 ms)

t_3 = Time from V_{OUT1} established to V_{OUT3} starting (default 4 ms)

t_4 = Time from V_{OUT3}, established to nRSTO deassertion (default 16 ms)

t_5 = Minimum hold time, PWRHLD = 1 to LPM = 0: Min. 0 µs (internal filtering applies)

FIGURE 4-9: *Start-Up Sequence Exiting Hibernate Mode Timing Diagram.*

Note: Upon exit of Hibernate mode, Buck2 is not part of the sequence because it is already turned on (being in Auto-PFM mode). However, also depending on the instant at which the MPU deasserts LPM, it can toggle to FPWM mode at the time nRSTO is deasserted.

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4.4.6 RESTART SEQUENCE AFTER FAULT AND AUTOMATIC WAKE-UP PULSE (AWKP) GENERATION-MCP16501D ONLY

Due to the support for LPDDRx, which require correct sequencing between the LPDDRx memory rails, the MCP16501D features a different Fault management sequence. The correct Fault management sequence consists in the turn-off of all channels followed by an automatically executed restart sequence, which ensures that the power rails will be restarted in the correct order.

See **Section 5.5 "Protections"** for information on which Faults may trigger a new restart sequence. In the default configuration of the MCP16501D as soon as a Fault is detected, the power delivery on all channels is terminated and the MCP16501D waits for 100 ms. After this wait time, a new start-up sequence is generated in the attempt to restart the system correctly.

A special feature is provided to enable system recovery if there is a restart sequence after a Fault occurs while in Hibernate mode. In Hibernate mode, the PWRHLD had been previously set to low by the MPU and the MPU expects a wake-up event in order to set PWRHLD to high again. This must be a hardware event which is flagged to some I/O inside the MPU Shutdown and Wake-up Controller (SHDWC) block (e.g., a logic transition on a WKUPx or PIOBUx pin).

However, if a Fault causes a restart sequence while in Hibernate mode, the restart sequence is not successfully completed until a wake-up event is generated for the MPU SHDWC, because the PWRHLD remains low. It is necessary for the PWRHLD signal to be high just prior to the completion of the start-up sequence so that nRSTO can be deasserted. This is solved by generating from the MCP16501 an Automatic Wake-up Pulse (AWKP) on the nSTRTO output if the Fault that generates a restart sequence has occurred while in Hibernate mode.

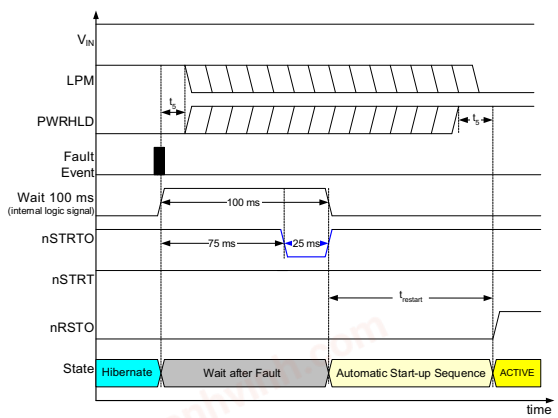
In the MCP16501D, the AWKP function is enabled by default.

The timing diagram of a restart sequence caused by a Fault while in Hibernate mode is shown in Figure 4-10.

Just before initiating the restart sequence, the MCP16501D generates a 25 ms (nominal duration) Automatic Wake-up Pulse on the nSTRTO output, even in lack of a low level on the nSTRT input. This is the only situation where the nSTRTO logic level does not reflect the nSTRT input status. The duration of the AWK Pulse erodes into the 100 ms waiting time that precedes the automatic restart sequence.

PWRHLD will typically return high as soon as the nSTRTO signal is detected to be low by the MPU SHDWC. If LPM stays high for any reason, the MCP16501D will go in Low-Power mode immediately after the automatic start-up sequence. This behavior is shown in Figure 2-21 in **Section 2.0 "Typical Performance Curves"**.

If the restart sequence after a Fault is executed in any other operational state but Hibernate, PWRHLD will either be already high (in applications with backup power) or it would return high as soon as the VDDIO rail is started, thus making the generation of the Automatic Wake-up Pulse not necessary.



Where:

$t_{restart}$ = Duration of the automatic start-up (restart) sequence

t_5 = Minimum setup/hold time: Min. 0 µs (internal filtering applies)

FIGURE 4-10: *Automatic Wake-Up Pulse Generation Timing Diagram (Fault during Hibernate).*

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4.5 Configuration Options

The device variants highlighted in **Section 4.0 "Device Options"** are generated at the factory with One-Time-Programmable memory which configures default settings at power-up.

To accommodate future possible MPUs or application architectures, the following configurations as shown in Table 4-5 can be taken into account to define other device options.

Note: Contact your nearest Microchip Sales Office for further assistance on the development of customized device variants.

TABLE 4-5: DEVICE CONFIGURATION

Setting	Description
RSTDLY	nRSTO assertion delay (t_4 in the start-up sequence); options are: 1 ms, 2 ms, 4 ms, 8 ms, 16 ms, 32 ms, 64 ms and 128 ms; default is 16 ms.
AWKPDIS	Enables or disables the automatic wake-up pulse; default is enabled.
VOUT[1,2,3]	Buck output voltage, Buck1 output range is between 1.2V and 3.7V with a 50 mV resolution, while Buck2 and Buck3 have an output range between 0.6V and 1.85V with a 25mV resolution.
EN[1,2,3]	Enables or disables each Buck converters for all individual power state.
MODE[1,2,3]	FPWM or Auto PFM for each Buck converters for all individual power state.
SSR[1,2,3]	Soft Start rate for Buck converters; options are: 3.125 V/ms, 1.563 V/ms, 1.042 V/ms and 0.781 V/ms; default is 3.125 V/ms.
SEQ[1,2,3]	Start-up sequence step for each Buck converter.
DELAY[1,2,3]	Time delay from the completion of the previous Start-Up Sequence Step or Start-Up Event to the turn-on (beginning of Soft Start); options are:0 ms, 0.5 ms, 1 ms, 2 ms, 4 ms, 8 ms, 12 ms, 16 ms.
B1HCEN	Enables or disables the Hysteretic Control Mode for Buck1 in AutoPFM operation; only enabled for MCP16501E.
HCPEN[1,2,3]	Enables or disables the Hiccup short-circuit protection for each Buck converter; default is enabled with the exception of MCP16501D. When disabled, a short circuit will cause the immediate turn-off of all channels followed by a 100 ms wait time and an automatic restart sequence.
DISCH[1,2,3]	Enables or disables the active output discharge when the channel is turned off; default is enabled.
PHASE[1,2,3]	Enables operation 180° out of phase with the oscillator for each Buck.

Note: [1,2,3] – refers to each individual Buck channel setting.

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4.6 Device Variants Default Settings

The summary of all currently available device variants with their default register settings is shown in Table 4-6.

TABLE 4-6: DEFAULT REGISTERS SETTINGS VS. MCP16501 DEVICE VARIANTS

Setting	Power State	SELVx Status	Default Settings of MCP16501 Variants				
			A	B	C	D	E
RSTDLY	Irrelevant	Irrelevant	16ms	16ms	16ms	16ms	16ms
AWKPDIS	Irrelevant	Irrelevant	Enabled	Enabled	Enabled	Enabled	Enabled
VOUT[1]	Irrelevant	Irrelevant	3.3V	2.8V	3V	3.3V	3.3V
VOUT[2]	Irrelevant	SELV2 = Low	1.2V	1.2V	1.2V	1.2V	1.2V
VOUT[2]	Irrelevant	SELV2 = High-Z	1.35V	1.35V	1.35V	1.35V	1.35V
VOUT[2]	Irrelevant	SELV2 = High	1.8V	1.8V	1.8V	1.8V	1.8V
VOUT[3]	Irrelevant	SELV3 = Low	1V	1V	1V	1V	1V
VOUT[3]	Irrelevant	SELV3 = High-Z	1.15V	1.15V	1.15V	1.15V	1.15V
VOUT[3]	Irrelevant	SELV3 = High	1.25V	1.25V	1.25V	1.25V	1.25V
EN[1,2,3]	Active	Irrelevant	Enabled	Enabled	Enabled	Enabled	Enabled
EN[1,2,3]	Low Power	Irrelevant	Enabled	Enabled	Enabled	Enabled	Enabled
EN[1,3]	Hibernate	Irrelevant	Disabled	Disabled	Disabled	Disabled	Disabled
EN[2]	Hibernate	Irrelevant	Enabled	Enabled	Enabled	Enabled	Enabled
MODE[1,2,3]	Active	Irrelevant	FPWM	FPWM	FPWM	FPWM	FPWM
MODE[1,2,3]	Low Power	Irrelevant	Auto-PFM	Auto-PFM	Auto-PFM	Auto-PFM	Auto-PFM
MODE[1,2,3]	Hibernate	Irrelevant	Auto-PFM	Auto-PFM	Auto-PFM	Auto-PFM	Auto-PFM
SSR[1,2,3]	Irrelevant	Irrelevant	3.125V/ms	3.125V/ms	3.125V/ms	3.125V/ms	3.125V/ms
SEQ[1]	Irrelevant	Irrelevant	1st	1st	1st	1st	1st
SEQ[2]	Irrelevant	Irrelevant	2nd	2nd	2nd	2nd	2nd
SEQ[3]	Irrelevant	Irrelevant	3rd	3rd	3rd	3rd	3rd
DELAY[1]	Irrelevant	Irrelevant	0.5ms	0.5ms	0.5ms	0.5ms	0.5ms
DELAY[2]	Irrelevant	Irrelevant	8ms	8ms	8ms	8ms	8ms
DELAY[3]	Irrelevant	Irrelevant	4ms	4ms	4ms	4ms	4ms
B1HCEN	Irrelevant	Irrelevant	Disabled	Disabled	Disabled	Disabled	Enabled
HCPEN[1,3]	Irrelevant	Irrelevant	Enabled	Enabled	Enabled	Disabled	Enabled
HCPEN[2]	Irrelevant	Irrelevant	Enabled	Enabled	Enabled	Disabled	Enabled
DISCH[1,2,3]	Irrelevant	Irrelevant	Enabled	Enabled	Enabled	Enabled	Enabled
PHASE[1,3]	Irrelevant	Irrelevant	180°	180°	180°	180°	180°
PHASE[2]	Irrelevant	Irrelevant	0°	0°	0°	0°	0°

Note: [1,2,3] – refers to each individual Buck channel setting.

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5.0 APPLICATION INFORMATION

5.1 Recommended External Components

Table 5-1 lists possible part numbers that can be used in the MCP16501 application. Refer to the **"Typical Application Circuit"** section for component designators' reference.

TABLE 5-1: RECOMMENDED EXTERNAL COMPONENTS

Item	Part Number	Manufacturer	Description
C1-C3	C1608X5R1A226M080AC	TDK Corporation	Capacitor, 22 µF, 6.3V/10V, X5R, 20%, Size 0603
	GRM188R61A226ME15D	Murata Electronics®	
	C1608X5R0J226M080AC	TDK Corporation	
	GRM188R60J226MEA0	Murata Electronics	
	JMK107BBJ226MA	Taiyo Yuden Co., Ltd.	
	CL10A226MQ8NRNC	Samsung Electro-Mechanics America, Inc.	
	06036D226MAT2A	AVX Corporation	
C4-C6, C8 (for 300 mA max. LDO current),	C1005X5R1A475M050BC	TDK Corporation	Capacitor, 4.7 µF, 10V, X5R, 10%/20%, Size 0402
	GRM155R61A475MEAA	Murata Electronics	
	LMK105BBJ475MV	Taiyo Yuden Co., Ltd.	
	CL05A475M(K)P5NRNC	Samsung Electro-Mechanics America, Inc.	
	0402ZD475MAT2A	AVX Corporation	
C7, C8 (for 150 mA max. LDO current)	C1005X5R1A225K050BC	TDK Corporation	Capacitor, 2.2 µF, 10V/16V, X5R, 10%, Size 0402
	GRM155R61C225KE11	Murata Electronics	
	LMK105BJ225KV	Taiyo Yuden Co., Ltd.	
	CL05A225KP5NSNC	Samsung Electro-Mechanics America, Inc.	
	0402ZD225KAT2A	AVX Corporation	
R1	RC0402KR-07100KL	Yageo Corporation	Resistor, 100 kΩ, 5%, Size 0402
R2	RC0402KR-0710K0L	Yageo Corporation	Resistor, 10 kΩ, 5%, Size 0402
R3	MCMR04X1823FTL	Multicomp Inc.	Resistor, 182 kΩ, 1%, Size 0402
R4	MCMR04X1823FTL	Multicomp Inc.	Resistor, 182 kΩ, 1%, Size 0402
L1, L2, L3	MLP2520V1R5MT0S1	TDK Corporation	1.5 µH, 1.4A, 100 mΩ, Size 2520, Multilayer Ferrite
	LQM2HPN1R5MGH	Murata Electronics	1.5 µH, 1.6A, 65 mΩ, Size 2520, Multilayer Ferrite
	VLS252012CX-1R5M-1	TDK Corporation	1.5 µH, 2.3A, 62 mΩ, Size 2520, Wirewound Ferrite
	LQH2HPN1R5MGR	Murata Electronics	1.5 µH, 1.85A, 87 mΩ, Size 2520, Wirewound Ferrite
	CDPH28D11FNP-1R5MC	Sumida Corporation	1.5 µH, 1.74A, 69 mΩ, Size 3.0 mm x 3.2 mm, Wirewound Ferrite
	DFE252012P-1R5M=P2	Murata Electronics	1.5 µH, 2.6A, 60 mΩ Max, Size 2520, Metal Alloy
	DFE252012P-2R2M=P2	Murata Electronics	2.2 µH, 2.2A, 84 mΩ Max, Size 2520, Metal Alloy
	VLS252012HBX-1R5M-1	TDK Corporation	1.5 µH, 2.5A, 68 mΩ, Size 2520, Metal Alloy
	VLS252012HBX-2R2M-1	TDK Corporation	2.2 µH, 2.04A, 85 mΩ, Size 2520, Metal Alloy
	74438324015	Würth Elektronik	1.5 µH, 2.2A, 82 mΩ, Size 2520, Metal Alloy
	74438324022	Würth Elektronik	2.2 µH, 1.6A, 123 mΩ, Size 2520, Metal Alloy
	74404024015	Würth Elektronik	1.5 µH, 1.9A, 65 mΩ, Size 2520, Wirewound Ferrite
	74405024022	Würth Elektronik	2.2 µH, 1.6A, 100 mΩ, Size 2520, Wirewound Ferrite

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5.2 Buck1 Hysteretic Control Mode (HCM)/B1HCEN-MCP16501E only

If Buck1 is set in Auto-PFM mode while the input voltage (e.g., a discharging battery) is decreasing and eventually pushing Buck1 to 100% duty cycle (Bypass mode), the operational no-load quiescent current shows some increase due to the augmented switching activity of Buck1.

This is intrinsic to the Auto-PFM architecture. The peaking in the quiescent current is in the 1 mA range, and it may or may not be detrimental to the overall system efficiency and/or battery life, depending mostly on the minimum loading of Buck1.

If the increase in quiescent current when approaching Bypass mode on Buck1 is an important factor for the application, the user can choose MCP16501E which features a different mode of light load, high-efficiency operation (called Hysteretic Control mode, HCM), where the output voltage is controlled in a hysteretic fashion between the nominal output voltage and 2.9% of it. This control method significantly reduces the average switching activity of Buck1, especially in the proximity of the bypass operation, at the expense of an increase of the output ripple amplitude.

It is recommended that the user, therefore, carefully evaluate the need for Hysteretic Control Mode and balance the increase in output ripple against the real benefit achieved in prolonging battery life. If the minimum loading on Buck1 is always significantly higher than 1 mA, HCM is typically not needed.

The relevant **"Electrical Characteristics"** parameter that defines the upper voltage regulation threshold (typically +2.9% of the nominal output voltage) is the Hysteretic Control Mode Upper Regulation Threshold.

HCM mode will only be activated when the input-to-output voltage differential decreases below a certain value. This is done to prevent fast inductor charging, which in turn may cause a poorer control of the effective upper regulation voltage.

The relevant **"Electrical Characteristics"** parameter that defines the input voltage threshold (falling input voltage), below which HCM is enabled, is the Hysteretic Control Mode Enable Threshold and it is also expressed as a percentage of the nominal output voltage value (typically, +9%).

5.3 LPDDR2 Support with Hibernate Mode-MCP16501D Only

To support LPDDR2 applications, which require two power supplies, the LDO block is used for the generation of the 1.8V of LPDDR2.

In the case of the MCP16501D, the LDO is partially included in the internal States machine such that the LDO stays turned on during Hibernate mode.

The LDO LEN pin must be connected to rail V_{OUT1} (VDDIO) such that the LDO (1.8V for LPDDR2) will immediately turn on after the VDDIO rail and before Buck2 (1.2V for LPDDR2), according to the LPDDR2 power-up specifications.

In this particular application the SELV2 will be connected to GND in order to have V_{OUT2} regulated to 1.2V for VDD2/VDDCA/VDDQ of LPDDR2, while the LDO feedback resistors (R3 and R4) will be selected to be equal, so that the LDO output is regulated to 1.8V for the LPDDR2 VDD1 rail.

The **"Typical Application Circuit"** section highlights this specific use case.

In the particular case of the MCP16501D, HCPEN is disabled, such that any short circuit event on one of the channels will trigger a turn off of all the channels and a start-up procedure. This method ensures proper re-sequencing of the LPDDR2 supply rails, regardless of the particular channel being affected by short-circuit.

5.4 Adjustable LDO Output Voltage

To calculate the resistor divider values for the MCP16501 LDO, Equation 5-1 can be used. R4 is connected to V_{LOUT}, R3 is connected to GND and both are connected to the LFB input pin.

EQUATION 5-1: RESISTOR DIVIDER CALCULATION

$$R4 = R3 \times \left(\frac{V_{LOUT}}{V_{LFB}} - 1\right)$$

Where:

V_{LFB} = 0.9V

It is recommended that the current through the external feedback divider be limited to about 5 µA; therefore, the bottom feedback resistor could typically be around 150-190 kΩ.

5.5 Protections

The MCP16501 offers the following:

- Thermal Shutdown
- Overcurrent Protection

Thermal Shutdown protection will immediately terminate power delivery on all channels when the die temperature exceeds the upper Thermal Shutdown threshold. At the same time, nRSTO will be asserted low.

After the die temperature has decreased below the lower Thermal Shutdown threshold (hysteresis = 20°C) and an additional 100 ms delay, the MCP16501 will automatically attempt a new start-up sequence without the need of an external Start condition (from nSTRT or PWRLHD).

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5.5.1 OVERCURRENT PROTECTION (BUCK CHANNELS)

The overcurrent protection consists of a cycle-by-cycle, high-side current limit with digital filtering, followed by the Hiccup mode for protection against short-circuit conditions.

The cycle-by-cycle, high-side current limit includes frequency foldback. Because of Leading-Edge Blanking (LEB) in Peak Current mode control, frequency foldback (with a factor = 4) is used to allow more time for inductor discharge and prevent current runaway in a deep overload condition.

Frequency foldback operation is entered when:

1. A high-side current limit event has been detected; and
2. The feedback voltage is less than 500 mV (typical).

Cycle-by-cycle overcurrent protection with frequency foldback is always active and it is the first current limit protection mechanism.

The second current limit mechanism is Hiccup mode protection, which is also always enabled, including during the soft start ramp.

Since the Hiccup mode protection is also active during soft start, there will be a limitation on the maximum simultaneous DC and capacitive loading to ensure that the Hiccup mode protection will not be engaged during the soft start ramp. This is further explained in **Section 5.6 "Maximum Simultaneous Capacitive and DC Loading in Soft Start"**.

Hiccup mode is invoked based on digital counting of High-Side Overcurrent (HS OC) events, regardless of the frequency at which they take place (full switching frequency or foldback switching frequency).

Each time the overcurrent protection detects a high-side current limit event, the current on-time is terminated and a HS OC event counter is incremented. The length of the counter is four bits.

If the counter reaches its End-of-Count (EOC) while the instantaneous value of the POK signal is still low, the Buck converter is turned off (both high-side and low-side transistors are turned off) and Hiccup mode protection is triggered.

The intervention of Hiccup mode on any of the Buck channels can have two different behaviors, depending on the HCPEN status of the channel affected by overcurrent conditions. By default, all device options of the MCP16501 come with HCPEN enabled, with the exception of MCP16501D.

If HCPEN is disabled, the intervention of Hiccup mode will immediately terminate the power delivery on all channels, including LDO. At the same time, nRSTO will be asserted low.

After a 100 ms delay, the MCP16501D will automatically attempt a new start-up sequence without the need of an external Start condition (from nSTRT or PWRHLD).

If HCPEN is enabled, the intervention of Hiccup mode only affects the responsible Buck channel. All other channels will continue to operate normally. If the affected channel is part of the power-up sequence, nRSTO will be asserted low.

The affected channel will be kept off for a certain Hiccup time (t_{HICCUP}), which corresponds to 3x soft start time on that channel, and after the Hiccup time, a new soft start is attempted.

If the short-circuit condition is removed and the affected channel resumes normal operation, nRSTO will be asserted high after the Reset delay (t_4).

The HS OC event counter is reset only after 15 consecutive HS turn-on pulses without any overcurrent event. This counting is done by the Reset counter.

Note that all counting is switching event-based, so it is not relevant if the switching takes place at f_{sw} or at $f_{sw}/4$ (i.e., in frequency foldback).

The Hiccup mode flowchart is detailed in Figure 5-1.

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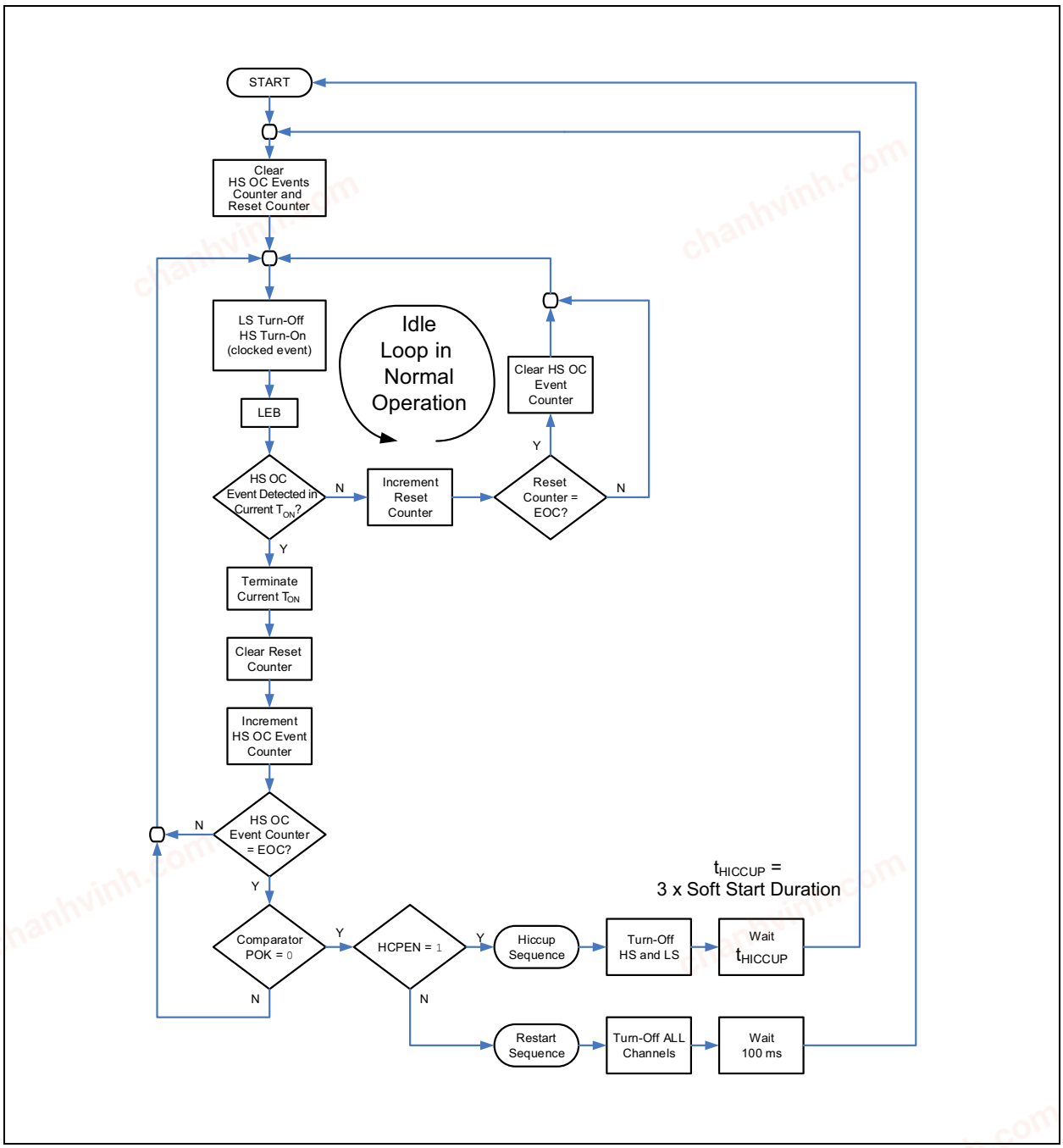


FIGURE 5-1: *Hiccup Mode Protection Flowchart.*

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5.5.2 PWM MODE NEGATIVE CURRENT LIMIT PROTECTION (BUCK CHANNELS)

The Buck channels of the MCP16501 also feature a negative inductor current limit protection when operating in Forced PWM mode. This prevents dangerous current levels in the power train. If the inductor current reaches the low-side Negative Peak Current Limit (I_{LIM_NEGx}) while the low-side MOSFET is conducting, the low-side MOSFET is turned off and the inductor current is pushed to the input voltage, either through the body diode of the high-side MOSFET (if turned off) or its channel (when turned on by the control loop). The intervention of this protection does not cause the assertion of the nRSTO (Reset) signal.

This protection must never be exercised continuously and/or without a large input bulk capacitor because it may quickly destroy the device.

When this protection is engaged, energy is pumped back from the output into the input voltage. If the input supply has no sinking capability and/or the input bulk decoupling cap is not large enough, the input voltage will rise to the point where the device is permanently damaged.

5.5.3 LDO CURRENT LIMIT PROTECTION

The LDO is protected against short circuit by a linear constant-voltage/constant-current (i.e., brick wall) output characteristic. The output current under short-circuit conditions is not intermittent. Therefore, the internal power dissipation in the MCP16501 can reach high levels under LDO short-circuit conditions. The intervention of the LDO current limit protection by itself does not cause the assertion of the nRSTO (Reset) signal.

5.6 Maximum Simultaneous Capacitive and DC Loading in Soft Start

The Current-mode architecture of the Buck channels in the MCP16501 make them tolerant to additional capacitive loads from the stability point of view.

However, since the Hiccup mode overcurrent protection is also enabled during soft start, the user needs to be aware that additional load capacitance, distributed on the application board, may cause the intervention of the Hiccup mode protections under dynamic conditions (rising output voltage).

This is especially important for Buck1 since the I/O rail (typically 3.3V) can be used for a wide variety of loads and its total distributed capacitive load could significantly exceed the minimum recommended nominal capacitance value (i.e., 22 µF).

Using the symbols listed in the **"AC/DC Characteristics"** table, Equation 5-2 establishes the maximum allowable capacitive load, C_{add_max}, to prevent the cycle-by-cycle current limit from being engaged.

Complying with this condition will ensure that Hiccup mode overcurrent protection will not be activated during the soft start ramp.

Failing to comply with the condition formulated below does not necessarily mean that Hiccup mode protection will be engaged. The digital filtering provided in the Hiccup mode overcurrent algorithm, as described in **Section 5.5.1 "Overcurrent Protection (Buck Channels)"**, provides immunity to single, and even multiple cycle-by-cycle current limit events and allows operation in proximity of the high-side current limit for a significant amount of time during the soft start.

EQUATION 5-2:

$$C_{add_max} = \left(\frac{I_{LIM_HS}}{r} - I_{OUT}\right) \cdot \frac{1}{SSR} - C_{OUT}$$

Where:

- I_{LIM_HS} = High-Side MOSFET Current Limit
- r = Ratio of the peak inductor current, I_{Lpk}, to average inductor current at the point where $I_{Lpk} = I_{LIM_HS}$. For simplicity, assume r = 1 since the peak-to-peak inductor current ripple will be small in comparison to the average inductor current value when the high-side current limit is engaged.
- I_{OUT} = Output Current of the Buck Converter
- SSR = Soft Start Rate
- C_{OUT} = Output capacitance already present on the Buck converter output (typically, C_{OUT} = 22 µF)

As a consequence, the maximum value of additional capacitance, C_{add_max}, that can be observed by experiments is significantly higher than the limit calculated with the aforementioned formula.

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5.7 nSTRT Capacitor for Automatic Turn-On on V_{IN} Ramping

As shown in Figure 4-1, it is possible to configure the MCP16501 for automatic start-up upon input voltage (V_{IN}) ramping/power cycling by connecting a capacitor on nSTRT pin. The purpose of the capacitor (C in Figure 4-1) is to delay the rise of the nSTRT pin when V_{IN} ramps up, such that after the V_{IN} pin voltage (connected to V_{IN}) has stabilized, the logic level of the nSTRT pin will still be low for a long time which is enough to be interpreted as a valid start-up event (i.e., longer than t_1; see **Section 4.4.1 "Typical Power-up Sequence and Timing"**).

Under the assumption that the V_{IN} ramping is much shorter than the rise time of the nSTRT pin voltage, the recommended amount of capacitance needed for generation of a valid start-up event is given by the formula in Equation 5-3.

After the selection of capacitor C, the resulting C R_{PU_nSTRT} time constant must be compared to the actual V_{IN} ramping time to verify that indeed the nSTRT rise time is much slower.

It is recommended that the time constant C R_{PU_nSTRT} be at least one order of magnitude larger than the slowest V_{IN} ramping time expected in the application. If this is not true, the capacitor value C must be increased further. Using a 1 µF capacitor for C, the C R_{PU_nSTRT} time constant will be 40 ms, which is adequate for V_{IN} ramping times in the ms range.

In atypical application in which the input voltage is unreliable or the ramp-up time is unknown or too long, an alternative to the startup using the nSTRT capacitor is to use a voltage supervisor circuit whose output will drive the PWRHLD directly.

EQUATION 5-3:

$$C > \frac{t_1 + \Delta t}{R_{PU_nSTRT} \cdot \log e\left(\frac{V_{IN}}{V_{IN} - V_{IL_nSRT}}\right)} = \frac{t_1 + \Delta t}{R_{PU_nSTRT} \cdot \log e\left(\frac{1}{1 - 0.36}\right)} = 2.24 \cdot \frac{t_1 + \Delta t}{R_{PU_nSTRT}}$$

Where:

R_{PU_nSTRT} = nSTRT Pin Pull-up Resistance (40 kΩ typical value)

V_{IL_nSTRT} = nSTRT Logic Low Input Voltage (0.36 V_{IN}, maximum value)

V_{IN} = Input Voltage (VIN pin is connected to the voltage V_{IN})

t_1 = Delay from nSTRT Falling to First Output V_{OUT1} Starting (≈ 0.5 ms); see **Section 4.4.1 "Typical Power-up Sequence and Timing"**

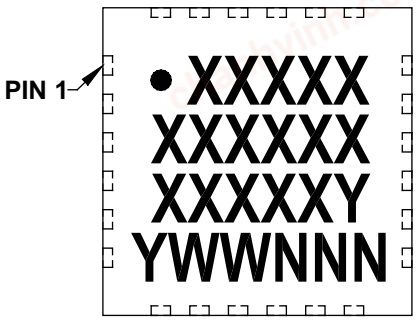
Δt = Additional Delay from VIN Voltage established to the Detection of a Logic Low Level on nSTRT (due to internal logic wake-up time): ≈ 100 µs

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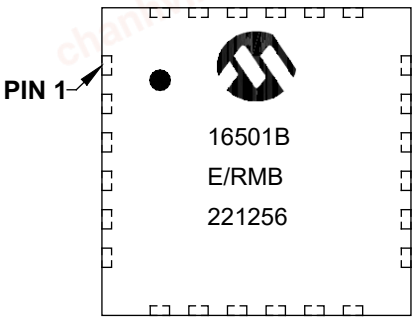
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6.0 PACKAGE MARKING INFORMATION

MCP16501
4 x 4 mm VQFN-24



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

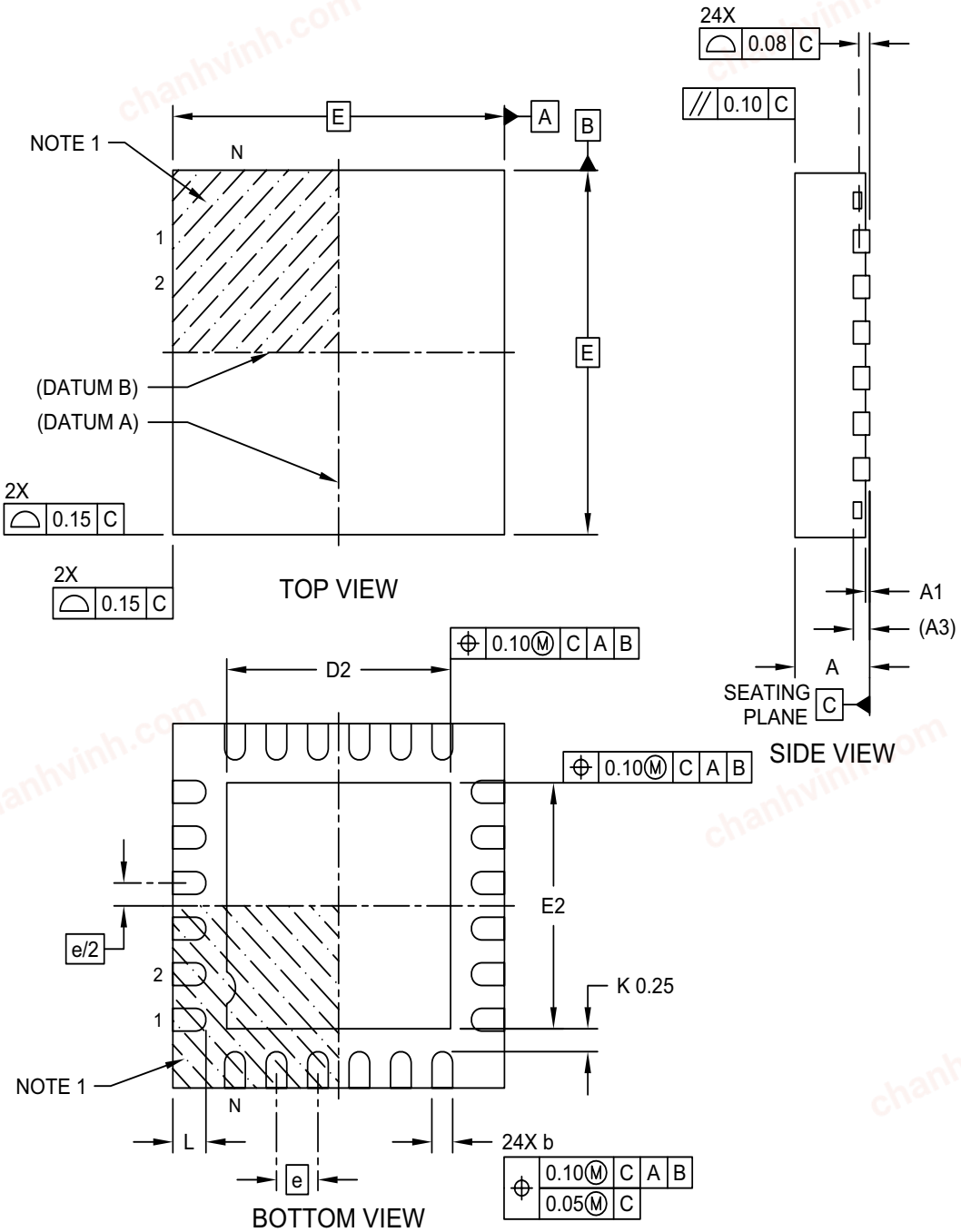
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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24-Lead Very Thin Plastic Quad Flat, No Lead Package (RMB) - 4x4 mm Body [VQFN]
Atmel Legacy Global Package Code ZZP

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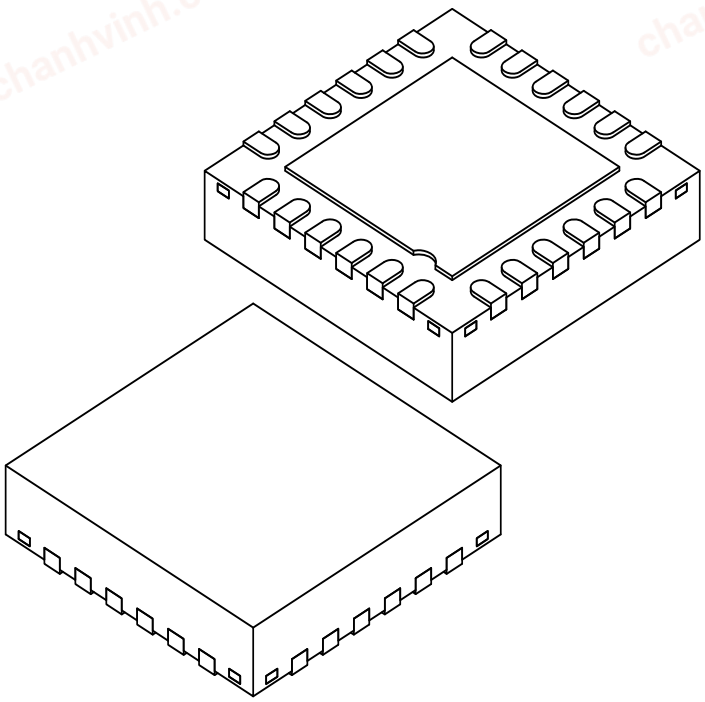


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Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		24	
Pitch	e		0.50 BSC	
Overall Height	A	-	-	0.90
Standoff	A1	0.00	-	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.60	2.70	2.80
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

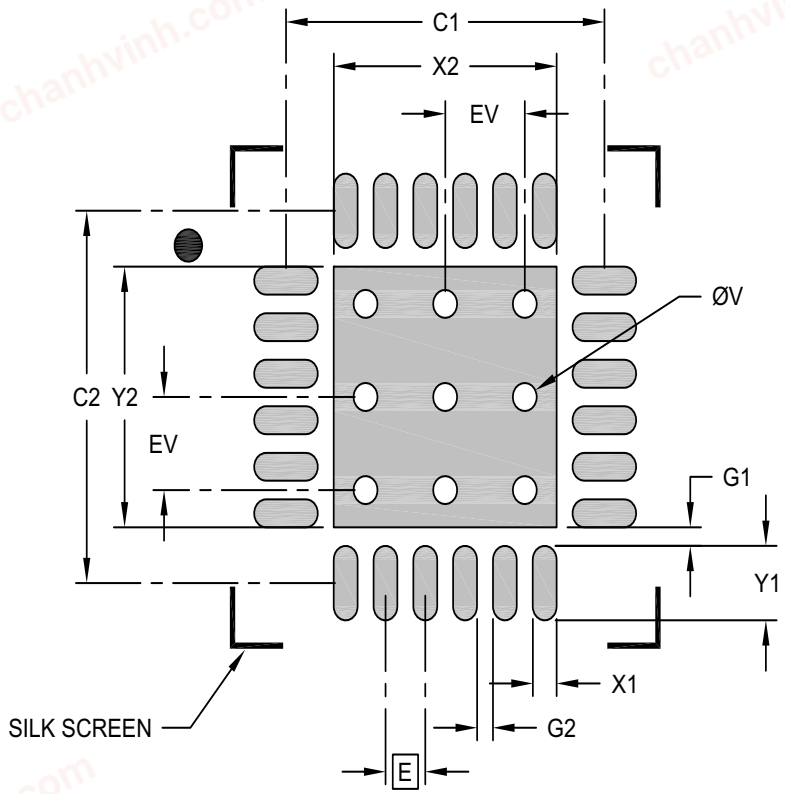
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RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			2.80
Optional Center Pad Length	Y2			2.80
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X24)	X1			0.30
Contact Pad Length (X24)	Y1			0.80
Contact Pad to Center Pad (X24)	G1	0.20		
Contact Pad to Contact Pad (X20)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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APPENDIX A: REVISION HISTORY

Revision E (September 2022)

- Added the SAM9X7 MPU throughout the document.

Revision D (April 2022)

- Updated **Typical Application Circuit**.
- Updated **Figure 4-2**.
- Updated **Table 4-6**.
- Added **Section 5.4, Adjustable LDO Output Voltage**.
- Updated **Section 5.7, nSTRT Capacitor for Automatic Turn-On on V_{IN} Ramping**.

Revision C (December 2020)

- Added AEC-Q100 qualification.
- Updated **"Product Identification System"**.
- Made minor editorial corrections.

Revision B (August 2020)

- Minor modifications to **"Product Identification System"** section.

Revision A (July 2020)

- Initial release of this document.

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MCP16501

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X(1)	X	–	X	/XX	XXX
Device	Tape and Reel Option	Device Option		Junction Temperature Range	Package	Qualification

Device:	MCP16501 Cost and Size Optimized PMIC		
Tape and Reel Option:	T	=	Tape and Reel(1)
Device Option:	A	=	A option
	B	=	B option
	C	=	C option
	D	=	D option
	E	=	E option
Junction Temperature Range:	E	=	-40°C to +125°C (Extended)
Package:	RMB	=	24-Lead Very Thin Plastic Quad Flat, No Lead (VQFN) Package- 4x4 mm Body
Qualification:	Blank	=	Standard Qualification
	VAO	=	AEC-Q100 Automotive Qualification
	VXX	=	AEC-Q100 Automotive Qualification, custom device, additional terms or conditions may apply

Examples:

a) MCP16501TA-E/RMB: Cost and Size Optimized PMIC, Tape and Reel, A Option, -40°C to +125°C, 24-Lead 4 x 4 VQFN package

b) MCP16501TA-E/RMBVAO: Cost and Size Optimized PMIC, Tape and Reel, A Option, -40°C to +125°C, 24-Lead 4 x 4 VQFN package, Automotive qualified

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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