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LAN9360

AVB Audio Endpoint

Highlights

- Supports the implementation of an Automotive Ethernet Audio Device (AED-A) to transmit and/or receive uncompressed audio over an Ethernet Audio Video Bridging (AVB) network

Target Applications

- Automotive in-vehicle networking
- Infotainment
- Telematics

Features

- generalized Precision Time Protocol (gPTP)
  - Grandmaster
  - Slave
  - Precise time synchronization
  - 1PPS measurement support
- Audio Video Transport Protocol (AVTP)
  - AVTP Audio Format (AAF) Listener or Talker
  - AVTP Clock Reference Format (CRF) Listener or Talker
- Real-time Transport Protocol (RTP)
  - Extended with AVB RTCP support
  - Configurable Payload Type ID for fitting to custom RTP profile specifications
- Stream routing
  - Up to 8 streams in parallel
  - Processing of up to 40 audio channels
  - Parallel processing of incoming and outgoing streams
  - PDM to PCM decimation
- Media Clock recovery, from an:
  - AVTP AAF stream
  - AVTP CRF stream
  - RTP stream
- Media Clock generation, based on:
  - Local crystal
  - External FSY signal
- Configuration
  - Avnu entity model based
  - Tool assisted by MPLAB® Network Creator
- Bootloader
  - Remote firmware update over Ethernet and Universal Serial Bus (USB)
  - Remote configuration update over Ethernet and USB
- External MCU connectivity
  - MCU connected as Layer 2 device
  - Ethernet frame pass through on Serial Peripheral Interface (SPI) and USB
- Secure element (optional)
  - High-bandwidth Digital Content Protection (HDCP) receiver
  - Secure boot
  - Secure update
- Ethernet MAC 10/100 Mbps in Reduced Media Independent Interface (RMII) mode
- Two I²C Ports
  - PLL and TA100 control
  - User-specific external modules
- SPI Port
- USB Port
- Two Audio Ports supporting:
  - Inter-IC Sound (I^2S)
  - Time-Division Multiplexing (TDM)
  - Pulse-Density Modulation (PDM)
- System
  - Embedded voltage regulator for single-supply operation
  - Power-on-Reset (POR), Brown-out Detector (BOD)
  - AEC-Q100 Grade 2 qualified
- Package
  - 100-ball TFBGA, 9x9 mm, pitch 0.8 mm

Conformity

- Automotive Ethernet AVB Functional and Interoperability Specification
- IEEE 1722™-2016 (AVTP)
- RFC 3550-2003 (RTP/RTP Control Protocol (RTCP))
- IEEE 1733™-2011 (AVB RTCP packet extension)
- IEEE 802.1AS™-2011 (gPTP)

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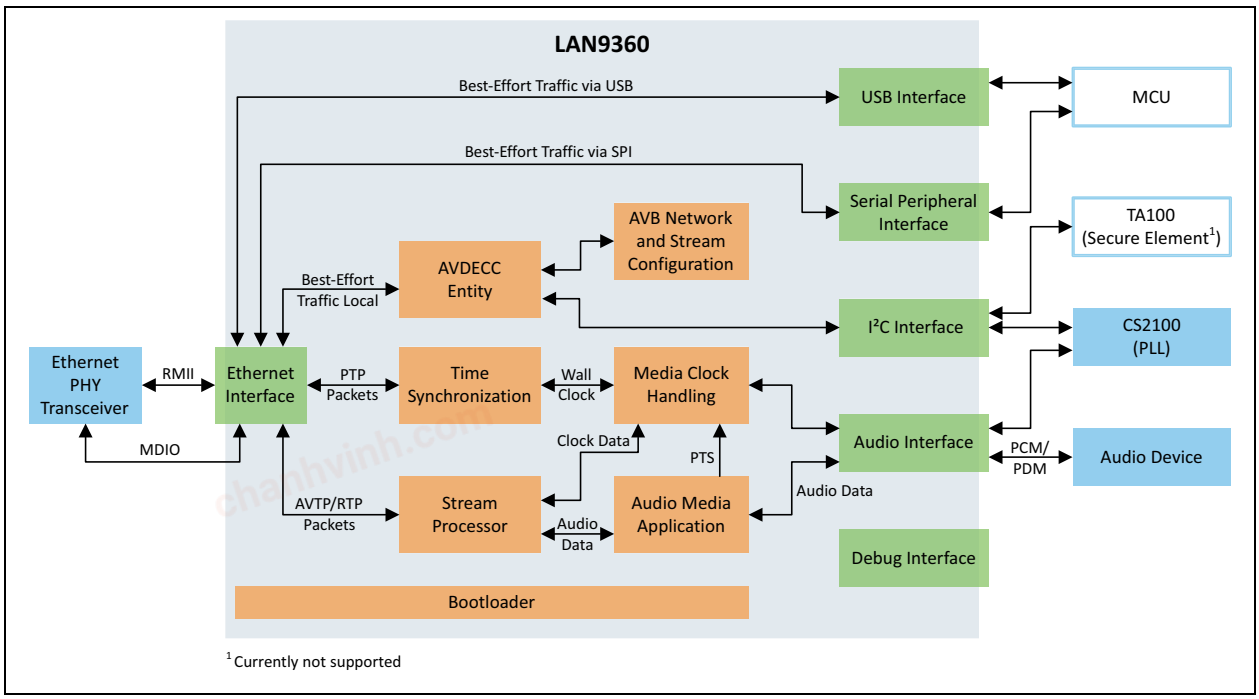
1.0 INTRODUCTION

The LAN9360 supports the implementation of an Automotive Ethernet Audio Device enabling uncompressed audio data transfers over an Ethernet Audio Video Bridging network. It is designed to route audio data between an AVB/TSN Media Stream on the Ethernet network and an Audio Interface that connects to digital audio sources and sinks.

The LAN9360 provides an Ethernet Interface. By connection to an external Ethernet PHY Transceiver, it can be used with several Ethernet physical layers.

Figure 1-1 depicts the block diagram of the LAN9360.

FIGURE 1-1: LAN9360 BLOCK DIAGRAM



As outlined in Figure 1-1, the LAN9360 consists of functional blocks. Each functional block contains one or multiple components that provide specific functionality.

1.1 LAN9360 Functional Blocks

The LAN9360 functional blocks are described in the LAN9360 data sheet.

Functional blocks, which interfere with external devices via physical pins are called interfaces.

1.2 External Devices

Ethernet PHY Transceiver

100BASE-T1 or 100BASE-TX may be selected by configuration. 10BASE-T1S is supported for evaluation.

PLL

The LAN9360 requires an external PLL of type CS2100 to generate the Bit-Clock for the Audio Interface.

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Audio Device

An external audio device, e.g., a DSP or a CODEC, is connected to the Audio Interface to transfer digital audio data. It is used as sink and/or source of Pulse-Code Modulation/Pulse-Density Modulation (PCM/PDM) coded audio data.

The Codec WM8904 is supported with volume control.

Secure Element (Optional)

A TA100 is used for HDCP, secure boot and secure update.

MCU (Optional)

An external MCU may be connected to the USB Interface or SPI to send and receive Ethernet frames.

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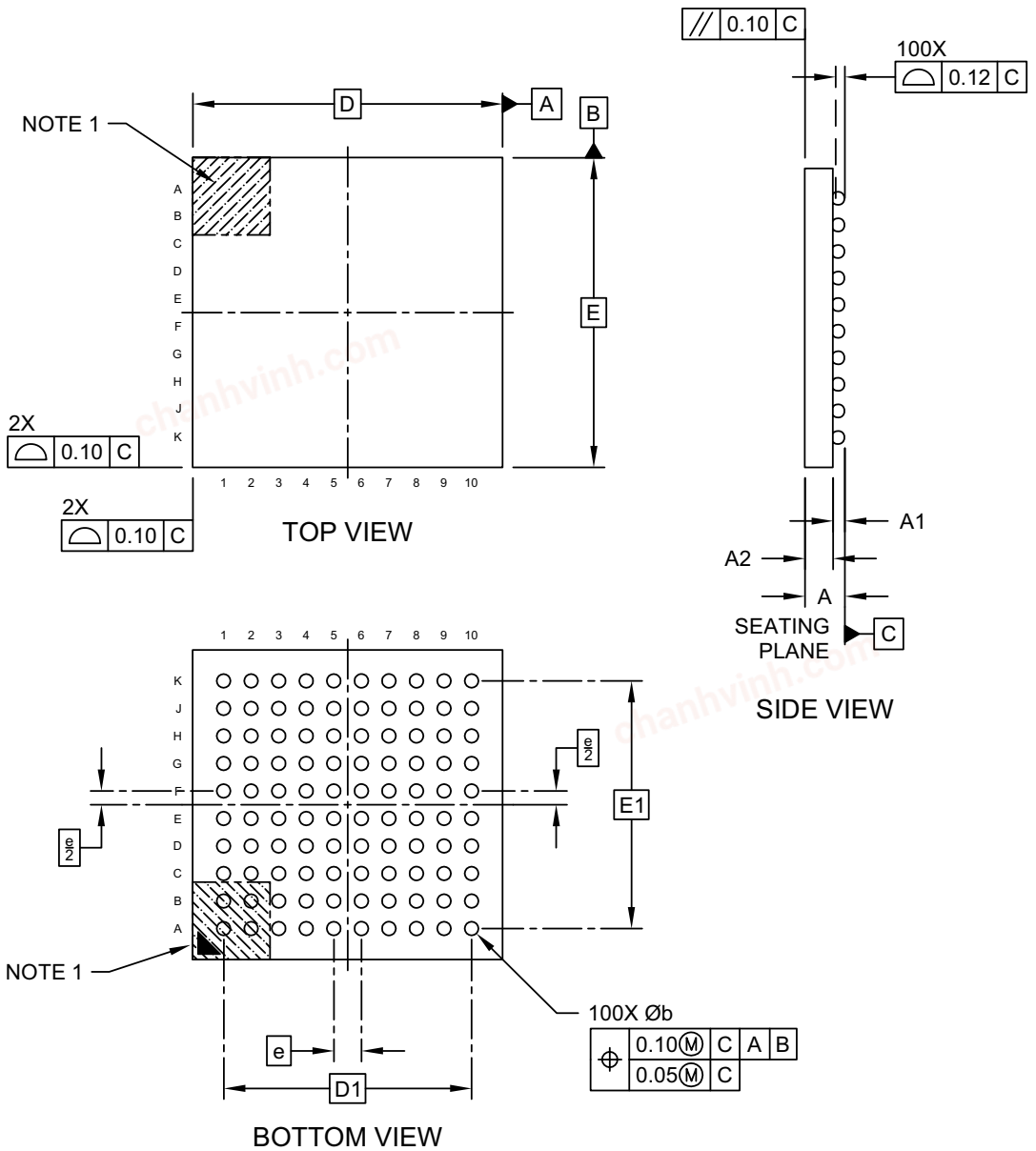
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2.0 PACKAGE AND PINOUT

2.1 100-Ball TFBGA Package Outline

100-Ball Ceramic Ball Grid Array Package (CQB) - 9x9 mm Body [TFBGA]
Atmel Legacy Global Package Code CPR

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

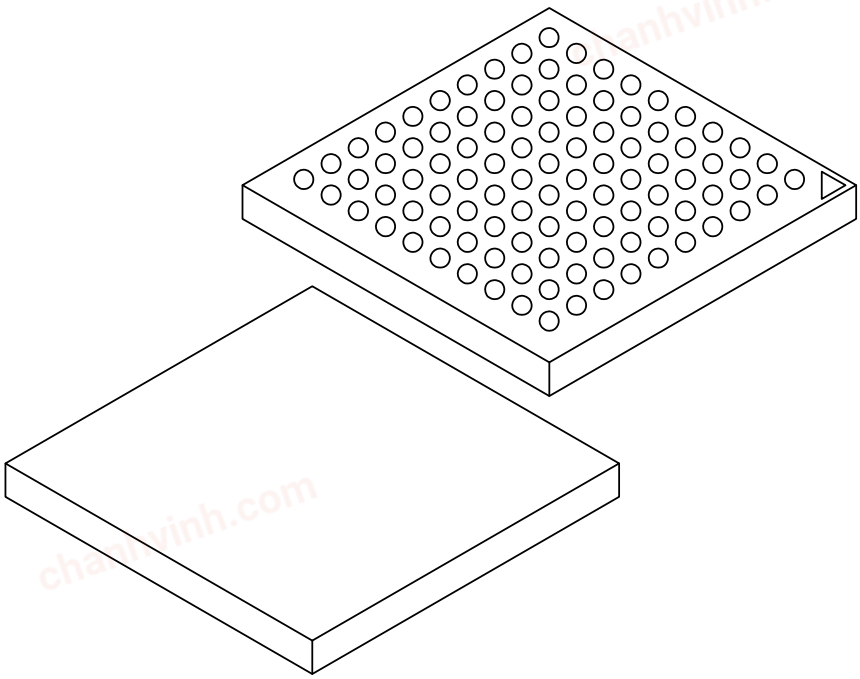


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Atmel Legacy Global Package Code CPR

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		100	
Pitch	e		0.80 BSC	
Overall Height	A	1.10	-	1.20
Ball Height	A1	0.20	-	-
Molded Package Height	A2	0.65	-	-
Overall Length	D		9.00 BSC	
Overall Pitch	D1		7.20 BSC	
Overall Width	E		9.00 BSC	
Overall Pitch	E1		7.20 BSC	
Terminal Diameter	b	0.40	0.45	0.50

Notes:

1. Terminal A1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

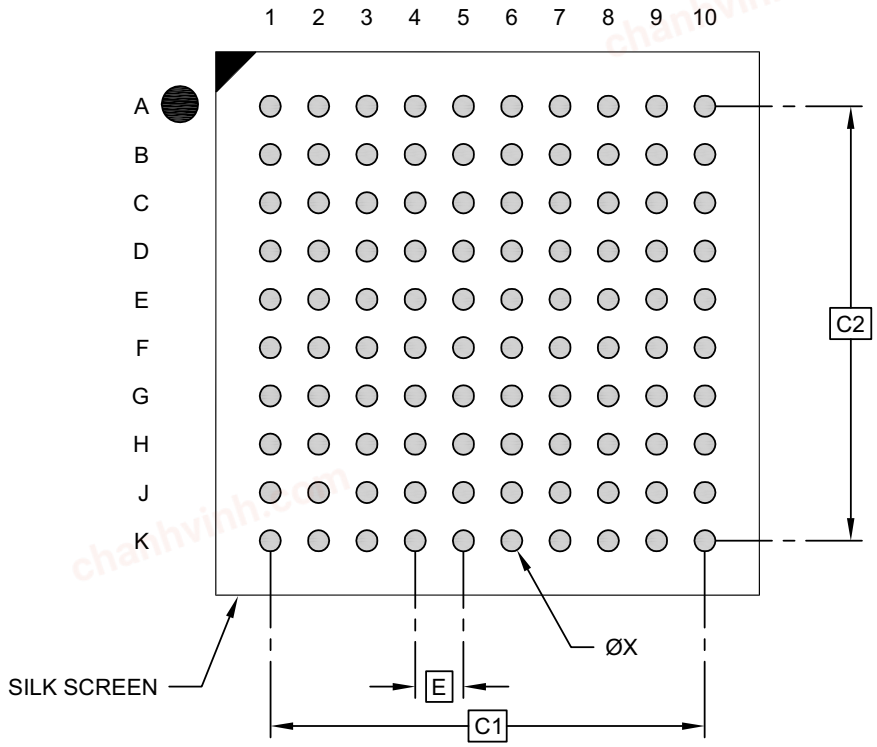
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Atmel Legacy Global Package Code CPR

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Overall Pitch	C1		7.20 BSC	
Contact Pad Spacing	C2		7.20 BSC	
Contact Pad Diameter (X100)	X1			0.35

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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2.2 100-Lead Package Pinout

TABLE 2-1: 100-LEAD PACKAGE PINOUT

TFBGA Ball	Signal	Conditions/ I/O Type	Pin Description	Type	Reset State[1]	Note
Audio Interface Audio Port						
E2	SCKA	GPIO	Serial Clock	Input/Output	I, PU, ST	—
E1	FSYA		Word Select			
G4	RF	GPIO_AD	FSYA Receive	Input		
K9	SRA		Serial Data Input			
G3	SXA	GPIO	Serial Data Output	Output		
C10	SCKB	GPIO_AD	Serial Clock	Input/Output		
J6	FSYB		Word Select			
J5	SRB		Serial Data Input	Input		
C7	SXB	GPIO	Serial Data Output	Output		
Audio Interface Clock Port						
F8	REFCLK0	GPIO	Reference Clock 0	Output	I, PD, ST	Signal is used to drive the clock reference of the external PLL for the audio clock.
			1PPS Measurement Signal			1PPS method for clock accuracy measurement
	ERASE		—	Input		—
K8	REFCLK1		Reference Clock 1	Output	I, PU, ST	
G2	MCLK	GPIO_AD	Master Clock			
J1	PLLDIVSEL		PLL Divider Select			
H8	REFCLKIN		Reference Clock 0 Input	Input		
J3	PLLIN/RK		Reference Clock Input			
A9	EVIN	GPIO	Event Input for Time-stamping			
H7	UNLOCK	GPIO_AD	Media Clock Unlock	Output		Signals synchronization failures at startup and during runtime
Serial Peripheral Interface						
H1	$\overline{\text{PCS}}$	GPIO	Peripheral Chip Select	Master: Output, Slave: Input	I, PU, ST	—
K3	MISO		Master In Slave Out	Master: Input, Slave: Output		
H5	MOSI	GPIO_AD	Master Out Slave In	Master: Output, Slave: Input		
J4	SPCK		Serial Clock			
G1	IRQ		Interrupt Request	Output		
K1	FC		Flow Control			

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TABLE 2-1: 100-LEAD PACKAGE PINOUT (CONTINUED)

TFBGA Ball	Signal	Conditions/ I/O Type	Pin Description	Type	Reset State[1]	Note
Crystal 12 MHz						
A2	XOUT	CLOCK	—	Output	HiZ	—
A1	XIN			Input		
Ethernet Interface						
C1	GTXCK	GPIO_AD	Transmit Clock	Input	I, PU, ST	Input only. GTXCK must be provided with a 50 MHz external oscillator.
D2	GTXEN	GPIO	Transmit Enable	Output		—
E3	GTX0		Transmit Data			
B5	GTX1					
A5	GRXDV	GPIO_CLK	Receive Data Valid	Input		
D5	GRX0		Receive Data			
B6	GRX1					
A6	GRXER		Receive Error			
B7	GMDC		Management Data Clock	Output		
B8	GMDIO		Management Data Input/ Output	Input/Output		
F1	$\overline{\text{GINT}}$	GPIO_AD	LAN interrupt	Input		From LAN PHY
J8	$\overline{\text{GRST}}$		LAN reset	Output		To LAN PHY
I²C Interface						
H4	SDA0	GPIO_AD	Serial Data	Input/Output	I, PU, ST	Interface to host
J7	SCK0		Serial Clock	Output		
F9	SDA1	GPIO_AD	Serial Data	Input/Output		Interface to connect a PLL and an optional Secure Element
H10	SCK1	GPIO	Serial Clock	Output		
H6	TA100RST	GPIO_CLK	TA100 reset			—
USB Interface						
A4	DM	USBHS	USB High Speed Data	Input/Output	—	—
B4	DP					
A3	VBG	VBG	Bias Voltage Reference for USB	Input		Refer to the USB 2.0 specification for additional information.
F2	VBUS	GPIO_AD	USB Signal		I, PU, ST	
Debug Interface						
C8	SWO	GPIO	Serial Wire Output	Output	O, PU	—
G8	SWDIO		Serial Wire Debug Input/ Output	Input	I, ST	
E9	SWCLK	GPIO	Serial Wire Debug Clock	Input		

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TABLE 2-1: 100-LEAD PACKAGE PINOUT (CONTINUED)

TFBGA Ball	Signal	Conditions/ I/O Type	Pin Description	Type	Reset State[1]	Note
Miscellaneous						
G10	RST	RST	—	Input	I, PU	—
K5	IDENTIFY	GPIO_AD	Toggles if the device identification feature is used	Output	I, PU, ST	—
G5	CFG		When detected to be high at reset, the configuration image 0 is loaded. Otherwise, image 1 is loaded.	Input		
Power and Ground						
C5, F3, G7	VDDIO	POWER	Power	—	—	—
C6, D6, G6	VDDCORE					
D7	VDDPLL					
E5	VDDUTMII					
B3	VDDUTMIC					
E6	VDDPLLUSB					
C3	VDDOUT					
C2	VDDIN					
D1	VREFP					
D3	VREFN	GROUND				
A8, C4, D4, E4, E7, F4, F5, F6	GND		Ground			

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TABLE 2-1: 100-LEAD PACKAGE PINOUT (CONTINUED)

TFBGA Ball	Signal	Conditions/ I/O Type	Pin Description	Type	Reset State[1]	Note
Not Connected						
A7	Not connected	—	—	—	I, PU, ST	—
A10					I, PD	
B1, B2, B10					I, PU, ST	
B9					I, PD, ST	
C9					I, PU, ST	
D8, D9, D10						
E8, E10						
F7					I, PD	
F10					I, PU, ST	
G9						
H2, H3, H9						
J2					HiZ	
J9, J10					I, PU, ST	
K2					HiZ	
K4, K6, K7, K10					I, PU, ST	

Note 1: In reset state the following applies:
"I" indicates a pin configured as input.
"O" indicates a pin configured as output.
"PU" indicates a pin with internal pull-up resistor.
"PD" indicates a pin with internal pull-down resistor.
"ST" indicates if Schmitt Trigger is enabled.
"HiZ" indicates high impedance state.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	-	X	/	XX	[X](1)	-	XXX	-	[XXX]
Device Family	Device Variant		Operating Temperature Range		Package Type	Tape and Reel Option		Revision Code		Automotive Code Option

Device Family:	LAN9360	
Device Variant:	A or C	= Basis feature set
Operating Temperature Range:	V I	= -40°C to +105°C (AEC-Q100 Grade 2) = -40°C to +85°C (Industrial)
Package Type:	CQB	= TFBGA (100-ball)
Tape and Reel Option:	Blank T	= Standard packaging (tray)(2) = Tape and Reel(1)
Revision Code:	XXX	= Unique 3-digit number
Automotive Code Option:	Blank VXX	= Industrial grade = Automotive grade

Examples:

a) LAN9360A-V/CQBT-100-VAO,
Basis feature set,
-40°C to +105°C,
TFBGA (100 ball),
Tape and Reel,
Revision code 100,
Automotive grade

b) LAN9360A-I/CQB-101,
Basis feature set,
-40°C to +85°C,
TFBGA (100 ball),
Tray,
Revision code 101,
Industrial grade

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
Reel size is 2,000.

2: Tray size is 260.

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APPENDIX A: REVISION HISTORY

Revision	Date	Comment
DS60001577E	Feb. 2022	• General: - Added USB Port related information - Removed EEPROM related contents • Section 1.0: - Reworked Figure 1-1 - Added WM8904 CODEC information • Section 2.2: Reworked Table 2-1, added Reset State information • Product Identification System: reworked section
DS60001577D	Jan. 2021	Initial release of this document
DS60001577C	July 2020	Updated draft document. For details refer to the respective document revision.
DS60001577B	Nov. 2019	
DS60001577A	July 2019	Initial version of draft document

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