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KSZ9131RNX

Gigabit Ethernet Transceiver with RGMII Support

Features

- Single-Chip 10/100/1000 Mbps Ethernet Transceiver Suitable for IEEE 802.3 Applications
- RGMII Timing Supports On-Chip Delay According to RGMII Version 2.0, with Programming Options for External Delay and Making Adjustments and Corrections to TX and RX Timing Paths
- RGMII with 3.3V/2.5V/1.8V Tolerant I/Os
- Auto-Negotiation to Automatically Select the Highest Link-Up Speed (10/100/1000 Mbps) and Duplex (Half/Full)
- On-Chip Termination Resistors for the Differential Pairs
- On-Chip LDO Controller to Support Single 3.3V Supply Operation – Requires Only One External FET to Generate 1.2V for the Core
- Jumbo Frame Support Up to 16 KB
- 125 MHz Reference Clock Output
- Energy-Detect Power-Down Mode for Reduced Power Consumption When Cable is Not Attached
- Energy Efficient Ethernet (EEE) Support with Low-Power Idle (LPI) Mode and Clock Stoppable for 100BASE-TX/1000BASE-T and Transmit Amplitude Reduction with 10BASE-Te Option
- Wake-On-LAN (WOL) Support with Robust Custom-Packet Detection
- Programmable LED Outputs for Link, Activity, and Speed
- Baseline Wander Correction
- Quiet-WIRE® EMI Reduction (100BASE-TX)
- LinkMD® TDR-based Cable Diagnostic to Identify Faulty Copper Cabling
- Signal Quality Indication
- Parametric NAND Tree Support to Detect Faults Between Chip I/Os and Board
- Loopback Modes for Diagnostics
- Automatic MDI/MDI-X Crossover to Detect and Correct Pair Swap at All Speeds of Operation
- Automatic Detection and Correction of Pair Swaps, Pair Skew, and Pair Polarity
- MDC/MDIO Management Interface for PHY Register Configuration
- Interrupt Pin Option
- Power-Down and Power-Saving Modes
- Operating Voltages
  - Core (DVDDL, AVDDL, AVDDL_PLL): 1.2V (External FET or Regulator)
  - VDD I/O (DVDDH): 3.3V, 2.5V, or 1.8V
  - Transceiver (AVDDH): 3.3V or 2.5V
- AEC-Q100 Grade 3 (KSZ9131RNXU) and Grade 2 (KSZ9131RNXV) Qualified for Automotive Applications
- 48-pin QFN (7 mm × 7 mm) Package

Target Applications

- Laser/Network Printer
- Network Attached Storage (NAS)
- Network Server
- Gigabit LAN on Motherboard (GLOM)
- Broadband Gateway
- Gigabit SOHO/SMB Router
- IPTV
- IP Set-Top Box
- Game Console
- Triple-Play (Data, Voice, Video) Media Center
- Industrial Control
- Automotive In-Vehicle Networking

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1.0 PREFACE

1.1 General Terms

TABLE 1-1: GENERAL TERMS

Term	Description
1000BASE-T	1 Gbps Ethernet over twisted pair, IEEE 802.3 compliant
100BASE-TX	100 Mbps Ethernet over twisted pair, IEEE 802.3 compliant
10BASE-T	10 Mbps Ethernet over twisted pair, IEEE 802.3 compliant
ADC	Analog-to-Digital Converter
AFE	Analog Front End
AN, ANEG	Auto-Negotiation
AOAC	Always on Always Connected
ARP	Address Resolution Protocol
BELT	Best Effort Latency Tolerance
BYTE	8-bits
CSMA/CD	Carrier Sense Multiple Access/Collision Detect
CSR	Control and Status Register
DA	Destination Address
DCQ	Dynamic Channel Quality
DWORD	32-bits
EC	Embedded Controller
EEE	Energy Efficient Ethernet
FCS	Frame Check Sequence
FIFO	First In First Out buffer
FSM	Finite State Machine
FW	Firmware
GPIO	General Purpose I/O
HOST	External system (Includes processor, application software, etc.)
HW	Hardware. Refers to function implemented by digital logic.
IGMP	Internet Group Management Protocol
LDO	Linear Drop-Out Regulator
Level-Triggered Sticky Bit	This type of status bit is set whenever the condition that it represents is asserted. The bit remains set until the condition is no longer true, and the status bit is cleared by writing a zero.
LFSR	Linear Feedback Shift Register
LPM	Link Power Management
lsb	Least Significant Bit
LSB	Least Significant Byte

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TABLE 1-1: GENERAL TERMS (CONTINUED)

Term	Description
LTM	Latency Tolerance Messaging
MAC	Media Access Controller
MDI	Medium Dependent Interface
MDIX	Media Independent Interface with Crossover
MEF	Multiple Ethernet Frames
MII	Media Independent Interface
MLT-3	Multi-Level Transmission Encoding (3-Levels). A tri-level encoding method where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”.
MSI / MSI-X	Message Signaled Interrupt
N/A	Not Applicable
OTP	One Time Programmable
PCS	Physical Coding Sublayer
PLL	Phase Locked Loop
PMIC	Power Management IC
POR	Power on Reset.
PTP	Precision Time Protocol
QWORD	64-bits
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
RGMII	Reduced Gigabit Media Independent Interface
RMON	Remote Monitoring
SA	Source Address
SCSR	System Control and Status Registers
SEF	Single Ethernet Frame
SFD	Start of Frame Delimiter - The 8-bit value indicating the end of the preamble of an Ethernet frame
SMNP	Simple Network Management Protocol
SQI	Signal Quality Indicator
UDP	User Datagram Protocol - A connectionless protocol run on top of IP networks
WORD	16-bits

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1.2 Buffer Types

TABLE 1-2: BUFFER TYPE DESCRIPTIONS

BUFFER	DESCRIPTION
AI	AI Analog input
AO	AI Analog output
AIO	AIO Analog bidirectional
ICLK	ICLK Crystal oscillator input pin
OCLK	OCLK Crystal oscillator output pin
VI	Variable voltage input
VIS	Variable voltage Schmitt-triggered input
VO8	Variable voltage output with 8 mA sink and 8 mA source
VOD8	Variable voltage open-drain output with 8 mA sink
VO24	Variable voltage output with 24 mA sink and 24 mA source
PU	44/59/96 KΩ (typical @3.3/2.5/1.8V) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	47/58/86 KΩ (typical @3.3/2.5/1.8V) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
P	Power pin

Note: Digital signals are not 5V tolerant unless specified.

Note: Sink and source capabilities are dependent on the supplied voltage.

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1.3 Register Bit Types

Table 1-3 describes the register but attributes used throughout this document.

TABLE 1-3: REGISTER BIT TYPES

Register Bit Type Notation	Register Bit Description
R	**Read:** A register or bit with this attribute can be read.
W	**Write:** A register or bit with this attribute can be written.
RO	**Read only:** Read only. Writes have no effect.
WO	**Write only:** If a register or bit is write-only, reads will return unspecified data.
W1S	**Write One to Set:** Writing a one sets the value. Writing a zero has no effect.
W1C	**Write One to Clear:** Writing a one clears the value. Writing a zero has no effect.
WAC	**Write Anything to Clear:** Writing anything clears the value.
RC	**Read to Clear:** Contents is cleared after the read. Writes have no effect.
LL	**Latch Low:** Clear on read of register.
LH	**Latch High:** Clear on read of register.
SC	**Self-Clearing:** Contents is self-cleared after being set. Writes of zero have no effect. Contents can be read.
SS	**Self-Setting:** Contents is self-setting after being cleared. Writes of one have no effect. Contents can be read.
RO/LH	**Read Only, Latch High:** This mode is used by the Ethernet PHY registers. Bits with this attribute will stay high until the bit is read. After it a read, the bit will remain high, but will change to low if the condition that caused the bit to go high is removed. If the bit has not been read the bit will remain high regardless of if its cause has been removed.
NASR	**Not Affected by Software Reset.** The state of NASR bits does not change on assertion of a software reset.
STKY	This field is “Sticky” in that it is neither initialized nor modified by hot reset or Function Level Reset.
RESERVED	**Reserved Field:** Reserved fields must be written with zeros, unless otherwise indicated, to ensure future compatibility. The value of reserved bits is not guaranteed on a read.

Many of these register bit notations can be combined. Come examples of this are:

- **R/W**: Can be written. Will return current setting on a read.
- **R/WAC**: Will return current setting on a read. Writing anything clears the bit.

1.4 Reference Documents

1. *IEEE 802.3™-2015 IEEE Standard for Ethernet,*
   http://standards.ieee.org/about/get/802/802.3.html
2. *IEEE 802.3bw™-2015 IEEE Standard for Ethernet Amendment 1,*
   https://standards.ieee.org/findstds/standard/802.3bw-2015.html
3. *Reduced Gigabit Media Independent Interface (RGMII) Specification Version 2.0,*
   https://web.archive.org/web/20160303171328/http://www.hp.com/rnd/pdfs/RGMIIv2_0_final_hp.pdf
4. *OPEN Alliance TC1 - Advanced diagnostics features for 100BASE-T1 automotive Ethernet PHYs Version 1.0*
   http://www.opensig.org/download/document/218/Advanced_PHY_features_for_automotive_Ethernet_V1.0.pdf

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2.0 INTRODUCTION

2.1 General Description

The KSZ9131RNX is a completely integrated triple-speed (10BASE-T/100BASE-TX/1000BASE-T) Ethernet physical-layer transceiver for transmission and reception of data on standard CAT-5 as well as CAT-5e and CAT-6 unshielded twisted pair (UTP) cables.

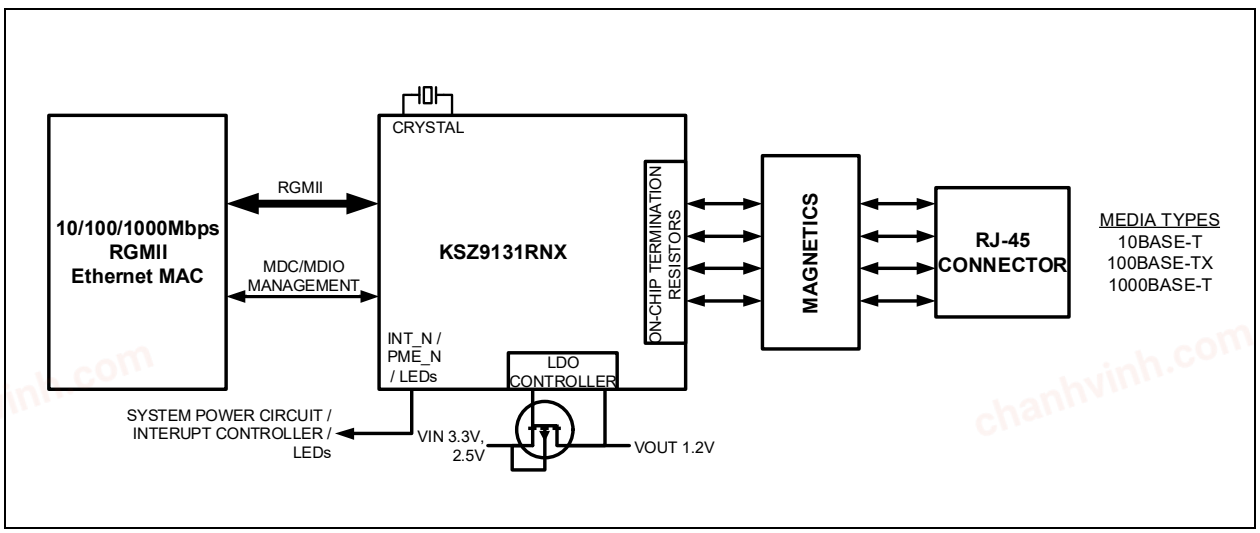
The KSZ9131RNX provides the Reduced Gigabit Media Independent Interface (RGMII) for direct connection to RGMII MACs in Gigabit Ethernet processors and switches for data transfer at 10/100/1000 Mbps.

The KSZ9131RNX reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating an LDO controller to drive a low-cost MOSFET to supply the 1.2V core.

The KSZ9131RNX offers diagnostic features to facilitate system bring-up and debugging in production testing and in product deployment. Parametric NAND tree support enables fault detection between KSZ9131RNX I/Os and the board. The LinkMD® TDR-based cable diagnostic identifies faulty copper cabling. Remote, external, and local loopback functions verify analog and digital data paths.

The KSZ9131RNX is available in a 48-pin, RoHS Compliant QFN package. The AEC-Q100 automotive qualified parts, KSZ9131RNXU and KSZ9131RNXV, are available in a 48-pin RoHS compliant VQFN (wettable) package.

FIGURE 2-1: SYSTEM BLOCK DIAGRAM



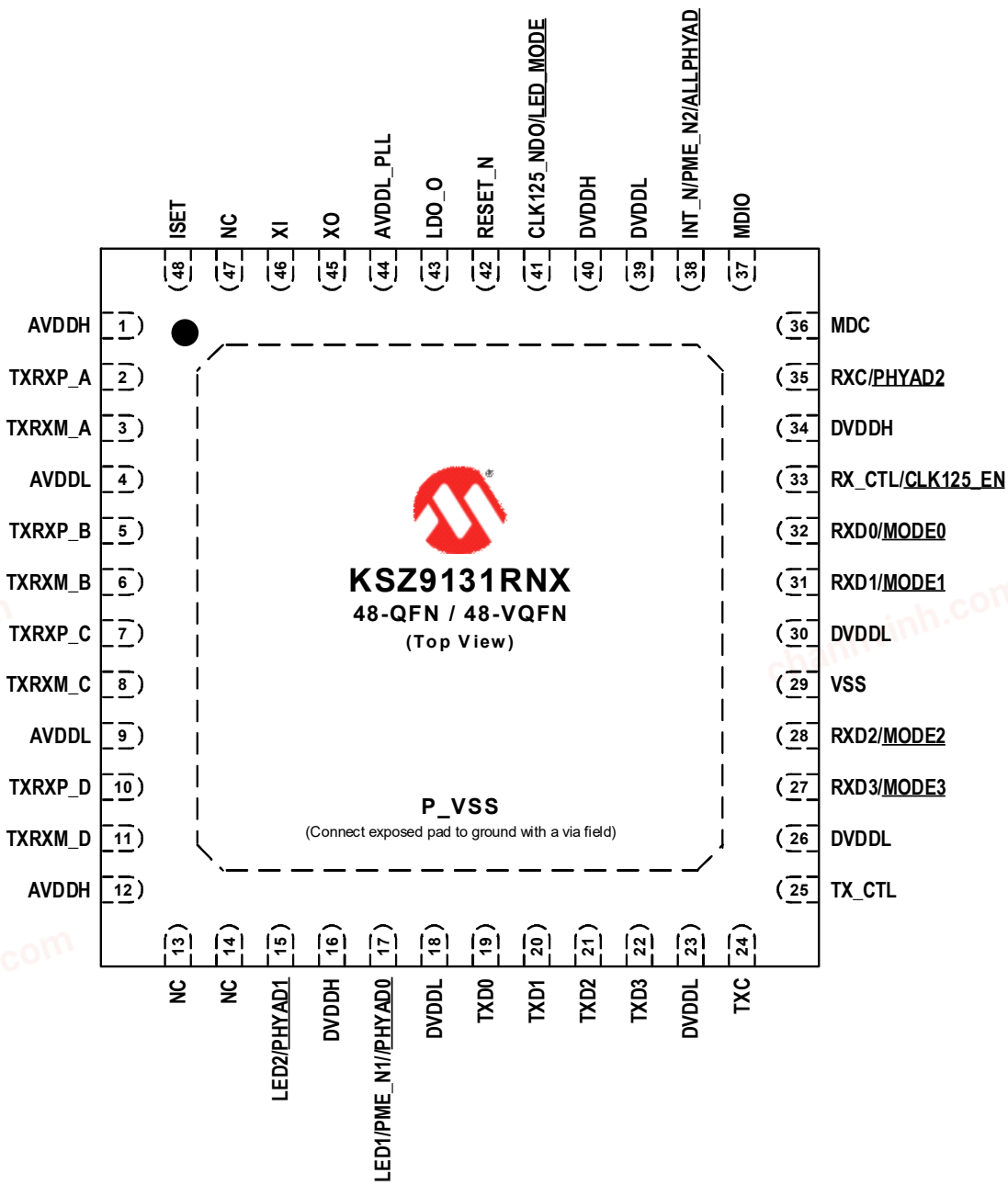
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3.0 PIN DESCRIPTIONS AND CONFIGURATION

3.1 Pin Assignments

FIGURE 3-1: PIN ASSIGNMENTS (TOP VIEW)



Note: Exposed pad (P_VSS) on bottom of package must be connected to ground with a via field.

Note: Configuration strap inputs are indicated with an underline.

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TABLE 3-1: KSZ9131RNX PIN ASSIGNMENTS

Pin Num	Pin Name	Pin Num	Pin Name
1	AVDDH	25	TX_CTL
2	TXRXP_A	26	DVDDL
3	TXRXM_A	27	RXD3/MODE3
4	AVDDL	28	RXD2/MODE2
5	TXRXP_B	29	VSS
6	TXRXM_B	30	DVDDL
7	TXRXP_C	31	RXD1/MODE1
8	TXRXM_C	32	RXD0/MODE0
9	AVDDL	33	RX_CTL/CLK125_EN
10	TXRXP_D	34	DVDDH
11	TXRXM_D	35	RXC/PHYAD2
12	AVDDH	36	MDC
13	NC	37	MDIO
14	NC	38	INT_N/PME_N2/ALLPHYAD
15	LED2/PHYAD1	39	DVDDL
16	DVDDH	40	DVDDH
17	LED1/PME_N1/PHYAD0	41	CLK125_NDO/LED_MODE
18	DVDDL	42	RESET_N
19	TXD0	43	LDO_O
20	TXD1	44	AVDDL_PLL
21	TXD2	45	XO
22	TXD3	46	XI
23	DVDDL	47	NC
24	TXC	48	ISET
Exposed Pad (P_VSS) must be connected to ground.			

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3.2 Pin Descriptions

This section contains descriptions of the various KSZ9131RNX pins. The "_N" symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, **RESET_N** indicates that the reset signal is active low. When "_N" is not present after the signal name, the signal is asserted when at the high voltage level.

The pin function descriptions have been broken into functional groups as follows:

- Analog Front End
- RGMII Interface
- Crystal
- Miscellaneous
- Strap Inputs
- I/O Power, Core Power and Ground

TABLE 3-2: ANALOG FRONT END

Name	Symbol	BUFFER TYPE	DESCRIPTION
Ethernet TX/RX Positive Channel A	TXRXP_A	AIO	Media Dependent Interface[0], positive signal of differential pair 1000BT mode: TXRXP_A corresponds to BI_DA+. 10BT/100BT mode: TXRXP_A is the positive transmit signal (TX+) for MDI configuration and the positive receive signal (RX+) for MDI-X configuration, respectively.
Ethernet TX/RX Negative Channel A	TXRXM_A	AIO	Media Dependent Interface[0], negative signal of differential pair 1000BT mode: TXRXM_A corresponds to BI_DA-. 10BT/100BT-TX mode: TXRXM_A is the negative transmit signal (TX-) for MDI configuration and the negative receive signal (RX-) for MDI-X configuration, respectively.
Ethernet TX/RX Positive Channel B	TXRXP_B	AIO	Media Dependent Interface[1], positive signal of differential pair 1000BT mode: TXRXP_B corresponds to BI_DB+. 10BT/100BT mode: TXRXP_B is the positive receive signal (RX+) for MDI configuration and the positive transmit signal (TX+) for MDI-X configuration, respectively.
Ethernet TX/RX Negative Channel B	TXRXM_B	AIO	Media Dependent Interface[1], negative signal of differential pair 1000BT mode: TXRXM_B corresponds to BI_DB-. 10BT/100BT mode: TXRXP_B is the negative receive signal (RX-) for MDI configuration and the negative transmit signal (TX-) for MDI-X configuration, respectively.
Ethernet TX/RX Positive Channel C	TXRXP_C	AIO	Media Dependent Interface[2], positive signal of differential pair 1000BT mode: TXRXP_C corresponds to BI_DC+. 10BT/100BT mode: TXRXP_C is not used.

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TABLE 3-2: ANALOG FRONT END (CONTINUED)

Name	Symbol	BUFFER TYPE	DESCRIPTION
Ethernet TX/RX Negative Channel C	TXRXM_C	AIO	Media Dependent Interface[2], negative signal of differential pair 1000BT mode: TXRXM_C corresponds to BI_DC-. 10BT/100BT mode: TXRXM_C is not used.
Ethernet TX/RX Positive Channel D	TXRXP_D	AIO	Media Dependent Interface[3], positive signal of differential pair 1000BT mode: TXRXP_D corresponds to BI_DD+. 10BT/100BT mode: TXRXP_D is not used.
Ethernet TX/RX Negative Channel D	TXRXM_D	AIO	Media Dependent Interface[3], negative signal of differential pair 1000BT mode: TXRXM_D corresponds to BI_DD-. 10BT/100BT mode: TXRXM_D is not used.

TABLE 3-3: RGMII INTERFACE

Name	Symbol	BUFFER TYPE	DESCRIPTION
Transmit Data	TXD3 TXD2 TXD1 TXD0	VI	The MAC transmits data to the PHY using these signals.
Transmit Control	TX_CTL	VI	Indicates both the transmit data enable (TXEN) and transmit error (TXER) functions per the RGMII specification.
RGMII Transmit Clock	TXC	VI	Used to latch data from the MAC into the PHY in RGMII mode. 1000BASE-T: 125MHz 100BASE-TX: 25MHz 10BASE-T: 2.5MHz
Receive Data	RXD3 RXD2 RXD1 RXD0	VO24	The PHY transfers data to the MAC using these signals. The PHY's link status (speed, duplex and link) are indicated on these signals whenever Normal Data, Data Error, Carrier Extend, Carrier Sense, False Carrier or Lower Power Idle are not present.
Receive Control	RX_CTL	VO24	Indicates both the receive data valid (RXDV) and receive error (RXER) functions per the RGMII specification.
RGMII Receive Clock	RXC	VO24	Used to transfer data from the PHY to the MAC in RGMII mode. 1000BASE-T: 125MHz 100BASE-TX: 25MHz 10BASE-T: 2.5MHz

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TABLE 3-4: CRYSTAL

Name	Symbol	BUFFER TYPE	DESCRIPTION
Crystal Input	XI	ICLK	When using a 25MHz crystal, this input is connected to one lead of the crystal. When using an clock source, this is the input from the oscillator. **Note:** The crystal or oscillator should have a tolerance of ±50ppm.
Crystal Output	XO	OCLK	When using a 25MHz crystal, this output is connected to one lead of the crystal. When using an external oscillator, this pin is not connected.

TABLE 3-5: MISCELLANEOUS

Name	Symbol	BUFFER TYPE	DESCRIPTION
Indicator LEDs	LED2 LED1	VO8	Programmable LED outputs.
Management Interface Data	MDIO	VIS/ VO8 VOD8 (PU)	This is the management data from/to the MAC. **Note:** An external pull-up resistor to DVDDH in the range of 1.0 kΩ to 4.7 kΩ is required.
Management Interface Clock	MDC	VIS (PU)	This is the management clock input from the MAC.
Power Management Event	PME_N2 PME_N1	VO8	Programmable PME_N output. When asserted low, this pin signals that a WOL event has occurred. PME_N can be mapped to either (or both) pins.
PHY Interrupt	INT_N	VO8	Programmable interrupt output.
CLK125 MHz	CLK125_NDO	VO24	125 MHz clock output. This pin provides a 125 MHz reference clock output option for use by the MAC. This pin may also provide a 125 MHz clock output synchronous to the receive data for use in Synchronous Ethernet (SyncE) applications.
System Reset	RESET_N	VIS (PU)	Chip reset (active low). Hardware pin configurations are strapped-in at the de-assertion (rising edge) of RESET_N. See the Strap Inputs section for details.

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TABLE 3-5: MISCELLANEOUS (CONTINUED)

Name	Symbol	BUFFER TYPE	DESCRIPTION
LDO Controller Output	LDO_O	AO	On-chip 1.2V LDO controller output. This pin drives the input gate of a P-channel MOSFET to generate 1.2V for the chip's core voltages. **Note:** If the system provides 1.2V, this pin is not used and can be left unconnected.
PHY Bias Resistor	ISET	AI	This pin should be connect to ground through a 6.04KΩ 1% resistor. **APPLICATION NOTE:** The resistor value is different from the 12.1KΩ used on the KSZ9031.
No Connect	NC	-	For normal operation, these pins should be left unconnected. **Note:** Pin 13 is not bonded and can be connected to ground for footprint compatibility with older generation devices. **Note:** Pin 14 is not bonded and can be connected to DVDDL power for footprint compatibility with older generation devices. **Note:** Pin 47 is not bonded and can be connected to AVDDH power for footprint compatibility with older generation devices.

TABLE 3-6: STRAP INPUTS

Name	Symbol	BUFFER TYPE	DESCRIPTION
PHY Address	PHYAD2 PHYAD1 PHYAD0	VI	The PHY address, PHYAD[2:0], is sampled and latched at power-up/reset and is configurable to any value from 0 to 7. Each PHY address bit is configured as follows: Pulled-up = 1 Pulled-down = 0 PHY Address Bits [4:3] are always set to '00'.
All PHY Address Enable	ALLPHYAD	VI	The ALLPHYAD strap-in pin is sampled and latched at power-up/reset and are defined as follows: 0 = PHY will respond to PHY address 0 as well as it's assigned PHY address 1= PHY will respond to only it's assigned PHY address **Note:** This strap input is inverted compared to the All-PHYAD Enable register bit.
Device Mode	MODE3 MODE2 MODE1 MODE0	VI	**Note:** The MODE[3:0] strap-in pins are sampled and latched at power-up/reset and are defined in Section 3.3.1, "Device Mode Select"

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TABLE 3-6: STRAP INPUTS (CONTINUED)

Name	Symbol	BUFFER TYPE	DESCRIPTION
125MHz Output Clock Enable	CLK125_EN	VI	CLK125_EN is sampled and latched at power-up/reset and is defined as follows: Pulled-up (1) = Enable 125 MHz clock output Pulled-down (0) = Disable 125 MHz clock output CLK125_NDO provides the 125 MHz reference clock output option for use by the MAC.
LED Mode	LED_MODE	VI	LED_MODE is sampled and latched at power-up/reset and is defined as follows: Pulled-up (1) = Individual-LED mode Pulled-down (0) = Tri-color-LED mode

TABLE 3-7: I/O POWER, CORE POWER AND GROUND

Name	Symbol	BUFFER TYPE	DESCRIPTION
+2.5/3.3V Analog Power Supply	AVDDH	P	+2.5/3.3V analog power supply V_{DD} **APPLICATION NOTE:** Automotive Grade 2 temperature range requires +2.5V.
+1.2V Analog Power Supply	AVDDL	P	+1.2V analog power supply V_{DD}
+1.2V Analog PLL Power Supply	AVDDL_PLL	P	+1.2V analog PLL power supply V_{DD}
+3.3/2.5/1.8V Variable I/O Power Supply Input	DVDDH	P	+3.3/2.5/1.8V variable I/O digital power supply V_{DD_IO} **APPLICATION NOTE:** Automotive Grade 2 temperature range requires +1.8V or +2.5V.
+1.2V Digital Core Power Supply Input	DVDDL	P	+1.2V digital core power supply input
Paddle Ground	P_VSS	GND	Common ground. This exposed paddle must be connected to the ground plane with a via array.
Digital Ground	VSS	GND	Digital ground

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3.3 Configuration Straps

Configuration straps allow various features of the device to be automatically configured to user defined values. Configuration straps are latched upon the release of pin reset (RESET_N). Configuration straps do not include internal resistors and require the use of external resistors.

Note:

- The system designer must ensure that configuration strap pins meet the timing requirements specified in Section 6.6.3, "Reset Pin Configuration Strap Timing". If configuration strap pins are not at the correct voltage level prior to being latched, the device may capture incorrect strap values.
- When externally pulling configuration straps high, the strap should be tied to DVDDH.

APPLICATION NOTE: All straps should be pulled-up or pulled-down externally on the PCB to enable the desired operational state.

3.3.1 DEVICE MODE SELECT

The MODE[3:0] configuration straps selects the device mode as follows:

TABLE 3-8: DEVICE MODE SELECTIONS

Functional Modes						
MODE[3:0]	Mode	PME Pin Enable	Auto-negotiation Advertisement			
			1000BT Full Duplex	1000BT Half Duplex	10/100BT Full Duplex	10/100BT Half Duplex
0000	RESERVED		-	-	-	-
0001	RESERVED		-	-	-	-
1000	RGMII	LED1 (PME_N1)	yes	no	yes	yes
1001	RESERVED		-	-	-	-
1010	RGMII	INT_N (PME_N2)	yes	no	yes	yes
1011	RESERVED		-	-	-	-
1100	RGMII		yes	no	no	no
1101	RESERVED		-	-	-	-
1110	RGMII		yes	no	yes	yes
1111	RESERVED		-	-	-	-
Test Modes						
MODE[3:0]	**Mode**					
0010	RESERVED					
0011	RESERVED					
0100	NAND tree mode					
0101	RESERVED					
0110	RESERVED					
0111	Device power down mode					

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3.3.2 PHY ADDRESS

The PHYAD2:0 configuration straps set the value of the PHY's management address. PHY Address Bits [4:3] are always set to '00'.

3.3.3 ALL PHYs ADDRESS

The ALLPHYAD configuration strap sets the default of the All-PHYAD Enable bit in the Common Control Register which enables or disables the PHY's ability to respond to PHY address 0 as well as it's assigned PHY address.

Note: This strap input is inverted compared to the register bit.

3.3.4 125MHZ OUTPUT CLOCK ENABLE

The CLK125_EN configuration strap enables the 125 MHz clock output onto the CLK125_NDO pin.
The output clock defaults to a locally generated 125MHz clock. The recovered 125MHz RX clock can be selected for use in Synchronous Ethernet (SyncE) applications.

3.3.5 LED MODE SELECT

The LED_MODE configuration strap selects between Individual-LED (1) or Tri-color-LED (0) modes. LED operation is described in Section 4.12, "LED Support".

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4.0 FUNCTIONAL DESCRIPTION

The KSZ9131RNX is a completely integrated triple-speed (10BASE-T/100BASE-TX/1000BASE-T) Ethernet physical layer transceiver solution for transmission and reception of data over a standard CAT-5 unshielded twisted pair (UTP) cable.

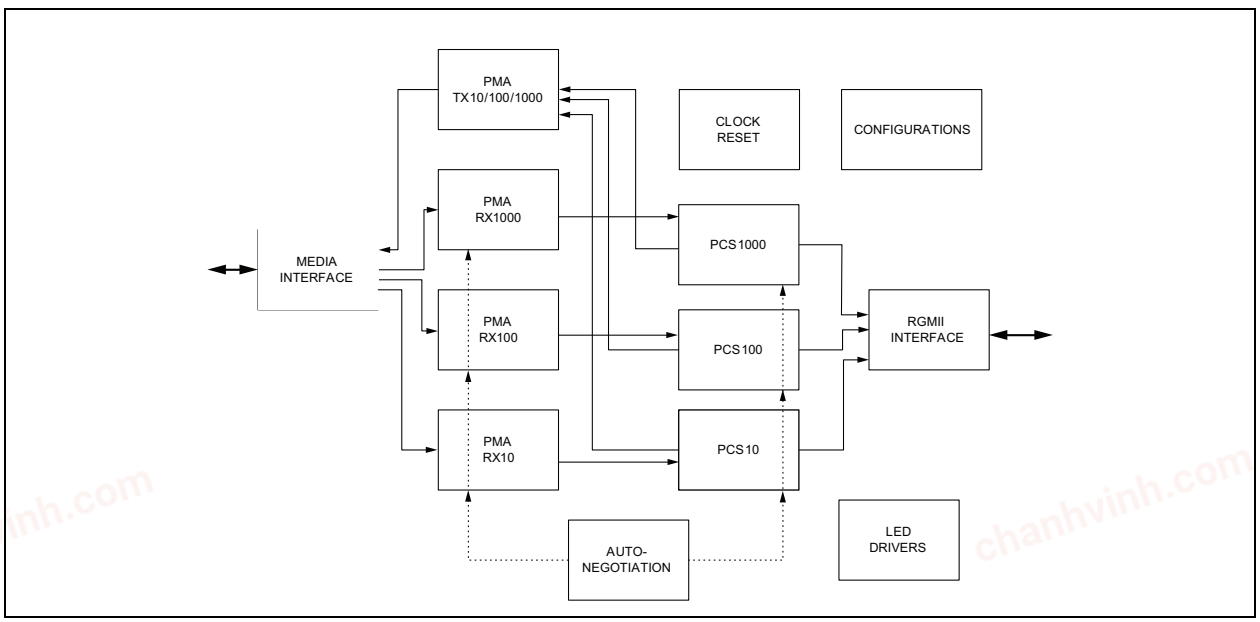
The KSZ9131RNX reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating an LDO controller to drive a low-cost MOSFET to supply the 1.2V core.

On the copper media interface, the KSZ9131RNX can automatically detect and correct for differential pair misplacements and polarity reversals, and correct propagation delays and re-sync timing between the four differential pairs, as specified in the IEEE 802.3 standard for 1000BASE-T operation.

The KSZ9131RNX provides the RGMII interface for connection to RGMII MACs in Gigabit Ethernet processors and switches for data transfer at 10/100/1000 Mbps.

Figure 4-1 shows a high-level block diagram of the KSZ9131RNX.

FIGURE 4-1: KSZ9131RNX BLOCK DIAGRAM



4.1 10BASE-T/100BASE-TX Transceiver

4.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT-3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT-3 current output. The output current is set by an external 6.04 kΩ 1% resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, and overshoot. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

4.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT-3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

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The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion are a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC-restoration and data-conversion block. The DC-restoration circuit compensates for the effect of baseline wander and improves the dynamic range. The differential data conversion circuit converts the MLT-3 format back to NRZI. The slicing threshold is also adaptive.

The clock-recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the RGMII format and provided as the input data to the MAC.

4.1.3 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. Transmitted data is scrambled using an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence, then the receiver de-scrambles the incoming data stream using the same sequence as at the transmitter.

4.1.4 10BASE-T TRANSMIT

The 10BASE-T output drivers are incorporated into the 100BASE-TX drivers to allow for transmission with the same magnetic. The drivers perform internal wave-shaping and pre-emphasis, and output signals with typical amplitude of 2.5V peak for standard 10BASE-T mode and 1.75V peak for energy-efficient 10BASE-Te mode. The 10BASE-T/10BASE-Te signals have harmonic contents that are at least 31 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

4.1.5 10BASE-T RECEIVE

On the receive side, input buffer and level-detecting squelch circuits are used. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 300 mV or with short pulse widths to prevent noises at the receive inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ9131RNX decodes a data frame. The receiver clock is maintained active during idle periods between receiving data frames.

The KSZ9131RNX removes all 7 bytes of the preamble and presents the received frame starting with the SFD (start of frame delimiter) to the MAC.

Auto-polarity correction is provided for the receiving differential pair to automatically swap and fix the incorrect +/– polarity wiring in the cabling.

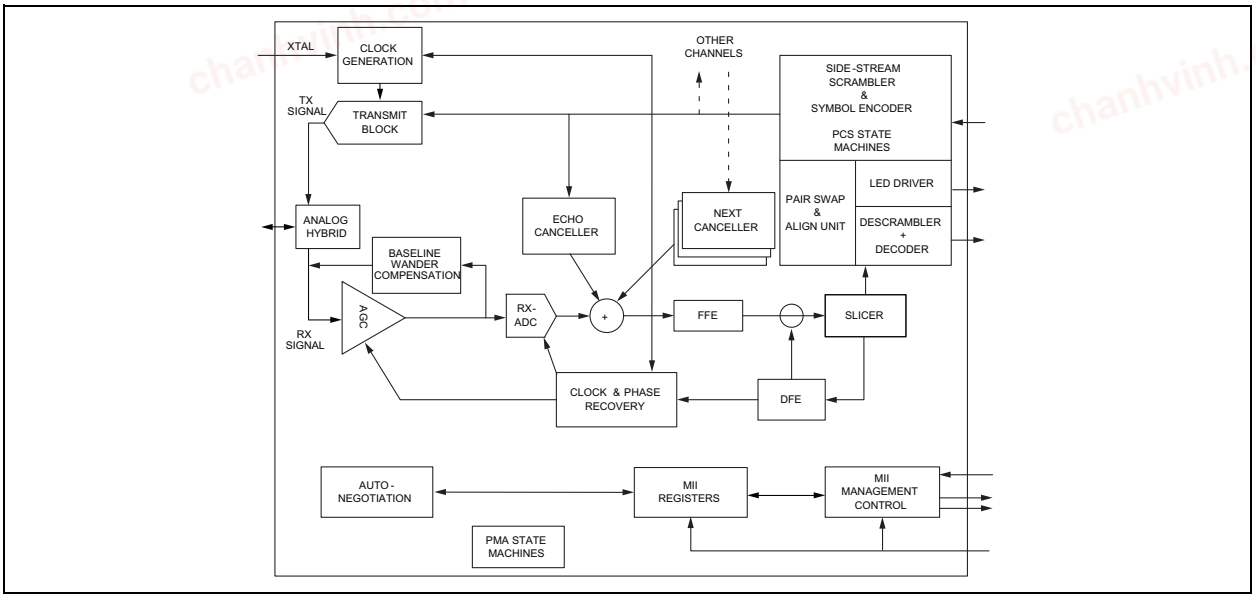
4.2 1000BASE-T Transceiver

The 1000BASE-T transceiver is based-on a mixed-signal/digital-signal processing (DSP) architecture, which includes the analog front-end, digital channel equalizers, trellis encoders/decoders, echo cancelers, cross-talk cancelers, precision clock recovery scheme, and power-efficient line drivers.

Figure 4-2 shows a high-level block diagram of a single channel of the 1000BASE-T transceiver for one of the four differential pairs.

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FIGURE 4-2: KSZ9131 1000BASE-T BLOCK DIAGRAM - SINGLE CHANNEL



4.2.1 ANALOG ECHO-CANCELLATION CIRCUIT

In 1000BASE-T mode, the analog echo-cancellation circuit helps to reduce the near-end echo. This analog hybrid circuit relieves the burden of the ADC and the adaptive equalizer.

This circuit is disabled in 10BASE-T/100BASE-TX mode.

4.2.2 AUTOMATIC GAIN CONTROL (AGC)

In 1000BASE-T mode, the automatic gain control (AGC) circuit provides initial gain adjustment to boost up the signal level. This pre-conditioning circuit is used to improve the signal-to-noise ratio of the receive signal.

4.2.3 ANALOG-TO-DIGITAL CONVERTER (ADC)

In 1000BASE-T mode, the analog-to-digital converter (ADC) digitizes the incoming signal. ADC performance is essential to the overall performance of the transceiver.

This circuit is disabled in 10BASE-T/100BASE-TX mode.

4.2.4 TIMING RECOVERY CIRCUIT

In 1000BASE-T mode, the mixed-signal clock recovery circuit together with the digital phase-locked loop is used to recover and track the incoming timing information from the received data. The digital phase-locked loop has very low long-term jitter to maximize the signal-to-noise ratio of the receive signal.

The 1000BASE-T slave PHY must transmit the exact receive clock frequency recovered from the received data back to the 1000BASE-T master PHY. Otherwise, the master and slave will not be synchronized after long transmission. This also helps to facilitate echo cancellation and NEXT removal.

4.2.5 ADAPTIVE EQUALIZER

In 1000BASE-T mode, the adaptive equalizer provides the following functions:

- Detection for partial response signaling
- Removal of NEXT and ECHO noise
- Channel equalization

Signal quality is degraded by residual echo that is not removed by the analog hybrid because of impedance mismatch. The KSZ9131RNX uses a digital echo canceler to further reduce echo components on the receive signal.

In 1000BASE-T mode, data transmission and reception occurs simultaneously on all four pairs of wires (four channels). This results in high-frequency cross-talk coming from adjacent wires. The KSZ9131RNX uses three NEXT cancelers on each receive channel to minimize the cross-talk induced by the other three channels.

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In 10BASE-T/100BASE-TX mode, the adaptive equalizer needs only to remove the inter-symbol interference and recover the channel loss from the incoming data.

4.2.6 TRELLIS ENCODER AND DECODER

In 1000BASE-T mode, the transmitted 8-bit data is scrambled into 9-bit symbols and further encoded into 4D-PAM5 symbols. The initial scrambler seed is determined by the specific PHY address to reduce EMI when more than one KSZ9131 is used on the same board. On the receiving side, the idle stream is examined first. The scrambler seed, pair skew, pair order, and polarity must be resolved through the logic. The incoming 4D-PAM5 data is then converted into 9-bit symbols and de-scrambled into 8-bit data.

4.3 Auto MDI/MDI-X

The Automatic MDI/MDI-X feature eliminates the need to determine whether to use a straight cable or a crossover cable between the KSZ9131RNX and its link partner. This auto-sense function detects the MDI/MDI-X pair mapping from the link partner, and assigns the MDI/MDI-X pair mapping of the KSZ9131RNX accordingly.

Table 4-1 shows the KSZ9131RNX 10/100/1000 pin configuration assignments for MDI/MDI-X pin mapping.

TABLE 4-1: MDI/MDI-X PIN MAPPING

Pin (RJ-45 Pair)	MDI			MDI-X		
	1000BASE-T	100BASE-T	10BASE-T	1000BASE-T	100BASE-T	10BASE-T
TXRXP/M_A (1, 2)	A+/–	TX+/–	TX+/–	A+/–	RX+/–	RX+/–
TXRXP/M_B (3, 6)	B+/–	RX+/–	RX+/–	B+/–	TX+/–	TX+/–
TXRXP/M_C (4, 5)	C+/–	Not Used	Not Used	C+/–	Not Used	Not Used
TXRXP/M_D (7, 8)	D+/–	Not Used	Not Used	D+/–	Not Used	Not Used

Auto MDI/MDI-X is enabled by default. It is disabled by writing a one to the Swap-Off bit in the Auto-MDI/MDI-X Register. MDI and MDI-X mode is set by the MDI Set bit in the Auto-MDI/MDI-X Register if Auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support Auto MDI/MDI-X.

4.4 Pair-Swap, Alignment, and Polarity Check

In 1000BASE-T mode, the KSZ9131RNX

- Detects incorrect channel order and automatically restores the pair order for the A, B, C, D pairs (four channels).
- Supports 50 ns ±10 ns difference in propagation delay between pairs of channels in accordance with the IEEE 802.3 standard, and automatically corrects the data skew so the corrected four pairs of data symbols are synchronized.

Incorrect pair polarities of the differential signals are automatically corrected for all speeds.

4.5 Wave Shaping, Slew-Rate Control, and Partial Response

In communication systems, signal transmission encoding methods are used to provide the noise-shaping feature and to minimize distortion and error in the transmission channel.

- For 1000BASE-T, a special partial-response signaling method is used to provide the band-limiting feature for the transmission path.
- For 100BASE-TX, a simple slew-rate control method is used to minimize EMI.
- For 10BASE-T, pre-emphasis is used to extend the signal quality through the cable.

4.6 PLL Clock Synthesizer

The KSZ9131RNX generates 125 MHz, 25 MHz, and 10 MHz clocks for system timing. Internal clocks are generated from the external 25 MHz crystal or reference clock.

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4.7 Auto-Negotiation

The KSZ9131RNX conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3 Specification.

Auto-negotiation allows UTP (unshielded twisted pair) link partners to select the highest common mode of operation.

During auto-negotiation, link partners advertise capabilities across the UTP link to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the operating mode.

The following list shows the speed and duplex operation mode from highest-to-lowest:

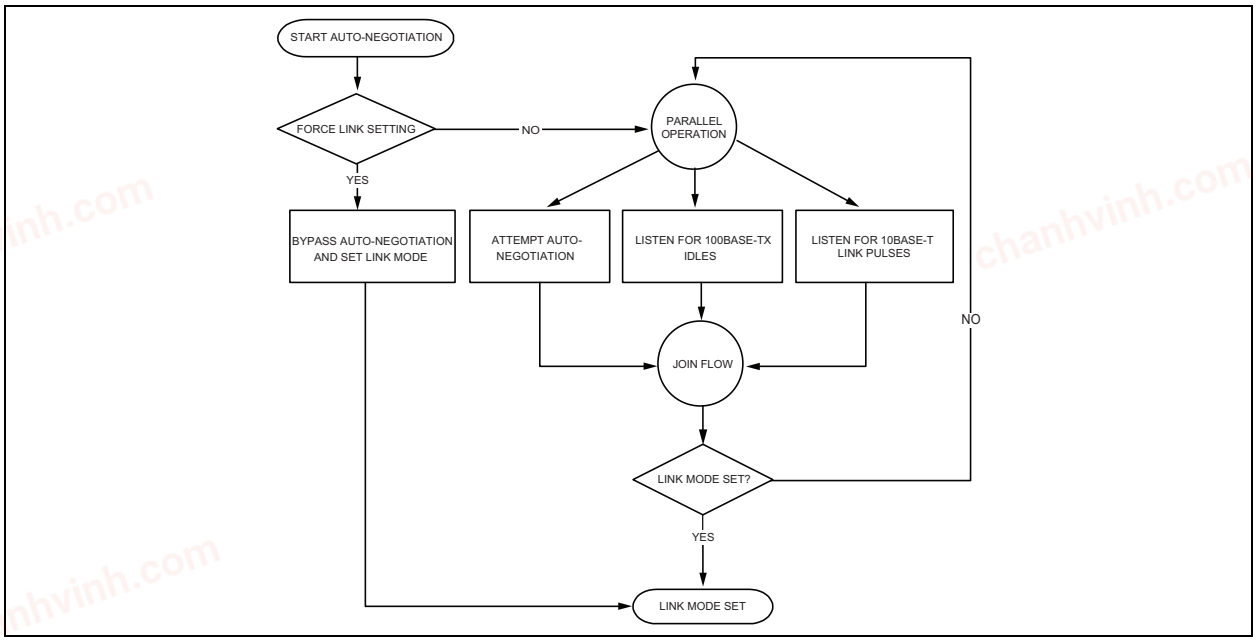
- Priority 1: 1000BASE-T, full-duplex
- Priority 2: 1000BASE-T, half-duplex

  Note: The device does not support 1000BASE-T, half-duplex and should not be enabled to advertise such.
- Priority 3: 100BASE-TX, full-duplex
- Priority 4: 100BASE-TX, half-duplex
- Priority 5: 10BASE-T, full-duplex
- Priority 6: 10BASE-T, half-duplex

If auto-negotiation is not supported or the KSZ9131RNX link partner is forced to bypass auto-negotiation for 10BASE-T and 100BASE-TX modes, the KSZ9131RNX sets its operating mode by observing the input signal at its receiver. This is known as parallel detection, and allows the KSZ9131RNX to establish a link by listening for a fixed signal protocol in the absence of the auto-negotiation advertisement protocol.

The auto-negotiation link-up process is shown in Figure 4-3.

FIGURE 4-3: AUTO-NEGOTIATION FLOW CHART



For 1000BASE-T mode, auto-negotiation is required and always used to establish a link. During 1000BASE-T auto-negotiation, the master and slave configuration is first resolved between link partners. Then the link is established with the highest common capabilities between link partners.

Auto-negotiation is enabled by default after power-up or hardware reset. After that, auto-negotiation can be enabled or disabled through the Auto-Negotiation Enable bit in the Basic Control Register. If auto-negotiation is disabled, the speed is set by the Speed Select[0] and Speed Select[1] bits and the duplex is set by the Duplex Mode, all in the Basic Control Register.

If the speed is changed on the fly, the link goes down and either auto-negotiation or parallel detection initiates until a common speed between KSZ9131RNX and its link partner is re-established for a link.

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If the link is already established and there is no change of speed on the fly, the changes (for example, duplex and pause capabilities) will not take effect unless either auto-negotiation is restarted through the Restart Auto-Negotiation (PHY_RST_AN) bit in the Basic Control Register, or a link-down to link-up transition occurs (that is, disconnecting and reconnecting the cable).

After auto-negotiation is completed, the link status is updated in the Link Status bit of the Basic Status Register and the link partner capabilities are updated in the Auto-Negotiation Link Partner Base Page Ability Register, Auto-Negotiation Expansion Register, and Auto-Negotiation Master Slave Status Register.

The auto-negotiation finite state machines use interval timers to manage the auto-negotiation process. The duration of these timers under normal operating conditions is summarized in Table 4-2.

TABLE 4-2: AUTO-NEGOTIATION TIMERS

Auto-Negotiation Interval Timers	Time Duration
Transmit Burst Interval	16 ms
Transmit Pulse Interval	68 µs
FLP Detect Minimum Time	17.2 µs
FLP Detect Maximum Time	185 µs
Receive Minimum Burst Interval	6.8 ms
Receive Maximum Burst Interval	112 ms
Data Detect Minimum Interval	35.4 µs
Data Detect Maximum Interval	95 µs
NLP Test Minimum Interval	4.5 ms
NLP Test Maximum Interval	30 ms
Link Loss Time	52 ms
Break Link Time	1480 ms
Parallel Detection Wait Time	830 ms
Link Enable Wait Time	1000 ms

4.7.1 AUTO-NEGOTIATION NEXT PAGE USAGE

The device supports “Next Page” capability which is used to negotiate Gigabit Ethernet and Energy Efficient Ethernet functionality as well as to support software controlled pages.

As described in IEEE 802.3 Annex 40C “Add-on interface for additional Next Pages”, the device will autonomously send and receive the Gigabit Ethernet and Energy Efficient Ethernet next pages and then optionally send and receive software controlled next pages.

Gigabit Ethernet next pages consist of one message and two unformatted pages. The message page contains an 8 as the message code. The first unformatted page contains the information from the Auto-Negotiation Master Slave Control Register. The second unformatted page contains the Master-Slave Seed value used to resolve the Master-Slave selection. The result of the Gigabit Ethernet next pages exchange is stored in Auto-Negotiation Master Slave Status Register.

Gigabit Ethernet next pages are always transmitted, regardless of the advertised settings in the Auto-Negotiation Master Slave Control Register.

Energy Efficient Ethernet (EEE) next pages consist of one message and one unformatted page. The message page contains a 10 as the message code (this value can be overridden in the EEE Message Code Register). The unformatted page contains the information from the EEE Advertisement Register. The result of the Gigabit Ethernet next pages exchange is stored in EEE Link Partner Ability Register.

EEE next pages are transmitted only if the advertised setting in the EEE Advertisement Register is not zero.

APPLICATION NOTE: The Gigabit Ethernet and EEE next pages may be viewed in Auto-Negotiation Next Page RX Register as they are exchanged.

Following the EEE next page exchange, software controlled next pages are exchanged when the Next Page bit in the Auto-Negotiation Advertisement Register is set. Software controlled next page status is monitored via the Auto-Negotiation Expansion Register and Auto-Negotiation Next Page RX Register.

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4.8 10/100 Mbps Speeds Only

Some applications require link-up to be limited to 10/100 Mbps speeds only.

After power-up/reset, the KSZ9131RNX can be restricted to auto-negotiate and link-up to 10/100 Mbps speeds only by programming the following register settings:

1. Configure the Speed Select[1] bit in the Basic Control Register to '0' to disable the 1000 Mbps speed.
2. Configure the 1000BASE-T Full Duplex and 1000BASE-T Half Duplex bits in the Auto-Negotiation Master Slave Control Register to '00' to remove Auto-Negotiation advertisements for 1000 Mbps full/half duplex.
3. Write a '1' to the Restart Auto-Negotiation (PHY_RST_AN) bit in the Basic Control Register, a self-clearing bit, to force a restart of Auto-Negotiation.

Auto-Negotiation and 10BASE-T/100BASE-TX speeds use only differential pairs A and B. Differential pairs C and D can be left as no connects.

4.9 RGMII Interface

The Reduced Gigabit Media Independent Interface (RGMII) supports on-chip data-to-clock delay timing according to the RGMII Version 2.0 Specification, with programming options for external delay timing and to adjust and correct TX and RX timing paths.

RGMII provides a common interface between RGMII PHYs and MACs, and has the following key characteristics:

- Pin count is reduced from 24 pins for the IEEE Gigabit Media Independent Interface (GMII) to 12 pins for RGMII.
- All speeds (10 Mbps, 100 Mbps, and 1000 Mbps) are supported at both half- and full-duplex.

Note:	The device does not support 1000BASE-T, half-duplex and should not be enabled to advertise such.

- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each four bits wide, a nibble.

In RGMII operation, the RGMII pins function as follows:

- The MAC sources the transmit reference clock, TXC, at 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps, and 2.5 MHz for 10 Mbps.
- The PHY recovers and sources the receive reference clock, RXC, at 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps, and 2.5 MHz for 10 Mbps.
- For 1000BASE-T, the transmit data, TXD[3:0], is presented on both edges of TXC, and the received data, RXD[3:0], is clocked out on both edges of the recovered 125 MHz clock, RXC.
- For 10BASE-T/100BASE-TX, the MAC holds TX_CTL low until both PHY and MAC operate at the same speed. During the speed transition, the receive clock is stretched on either a positive or negative pulse to ensure that no clock glitch is presented to the MAC.
- TX_ER and RX_ER are combined with TX_EN and RX_DV, respectively, to form TX_CTL and RX_CTL. These two RGMII control signals are valid at the falling clock edge.

After power-up or reset, the KSZ9131 is configured to RGMII mode if the MODE[3:0] strap-in pins are set to one of the RGMII mode capability options. See Section 3.3, "Configuration Straps" for additional information.

The KSZ9131RNX has the option to output a 125 MHz reference clock on the CLK125_NDO pin. This clock provides a lower-cost reference clock alternative for RGMII MACs that require a 125 MHz crystal or oscillator. The 125 MHz clock output is enabled after power-up or reset if the CLK125_EN strap-in pin is pulled high or the clk125 Enable bit is set in the Common Control Register.

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4.9.1 RGMII SIGNAL DEFINITION

Table 4-3 describes the RGMII signals. Refer to the RGMII Version 2.0 Specification for more detailed information.

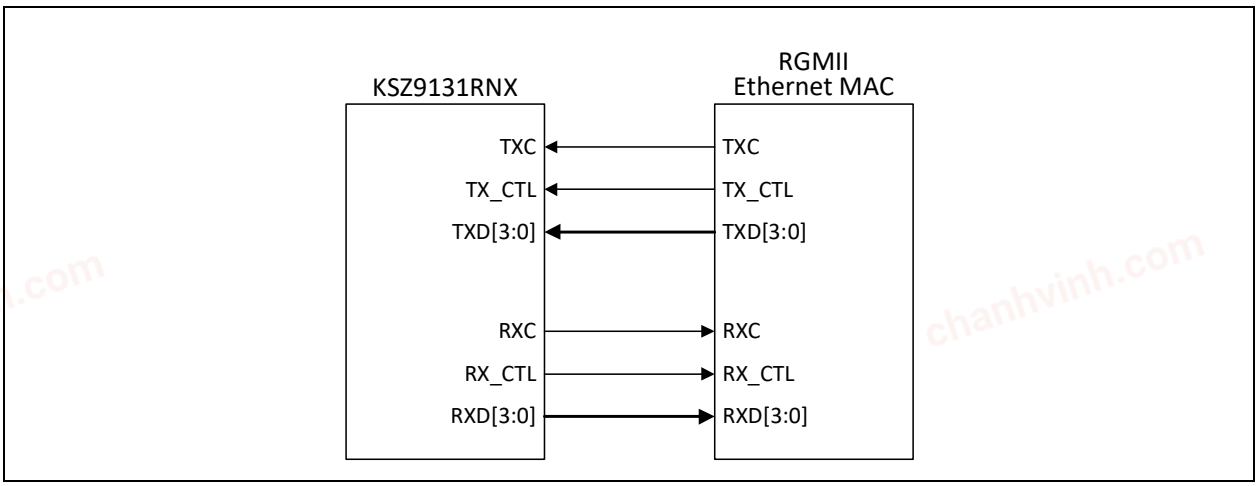
TABLE 4-3: RGMII SIGNAL DEFINITION

RGMII Signal Name	Pin Type (with respect to PHY)	Pin Type (with respect to MAC)	Description
TXC	Input	Output	Transmit Reference Clock (125MHz for 1000Mbps, 25MHz for 100Mbps, 2.5MHz for 10Mbps)
TX_CTL	Input	Output	Transmit Control
TXD[3:0]	Input	Output	Transmit Data[3:0]
RXC	Output	Input	Receive Reference Clock (125 MHz for 1000 Mbps, 25 MHz for 100 Mbps, 2.5 MHz for 10 Mbps)
RX_CTL	Output	Input	Receive Control
RXD[3:0]	Output	Input	Receive Data[3:0]

4.9.2 RGMII SIGNAL DIAGRAM

The KSZ9131RNX RGMII pin connections to the MAC are shown in Figure 4-4.

FIGURE 4-4: KSZ9131RNX RGMII INTERFACE



4.9.3 RGMII TIMING

As the default, after power-up or reset, the RGMII timing conforms to the timing requirements in the RGMII Version 2.0 Specification for internal PHY chip delay.

For the transmit path (MAC to PHY), the device does not add any delay locally at its TXC, TX_CTL and TXD[3:0] input pins, and expects the TXC delay to be provided on-chip by the MAC. If MAC does not provide any delay or insufficient delay for the TXC, the device has two options. The device may add a fixed 2ns, DLL based delay to the TXC input. In addition to this fixed delay, pad skew registers that can provide up to ~1.9 ns n-chip delay (~1.4 ns additional can be added to TXC, ~0.5 ns can be subtracted from TX_CTL and TXD[3:0]).

For the receive path (PHY to MAC), the device adds a fixed 2ns, DLL based delay to the RXC output pin with respect to RX_CTL and RXD[3:0] output pins. If necessary, the device has pad skew registers that can adjust the RXC on-chip delay by up to an additional ~1.9 ns (~1.4 ns additional can be added to RXC, ~0.5 ns can be subtracted from RX_CTL and TXD[3:0]).

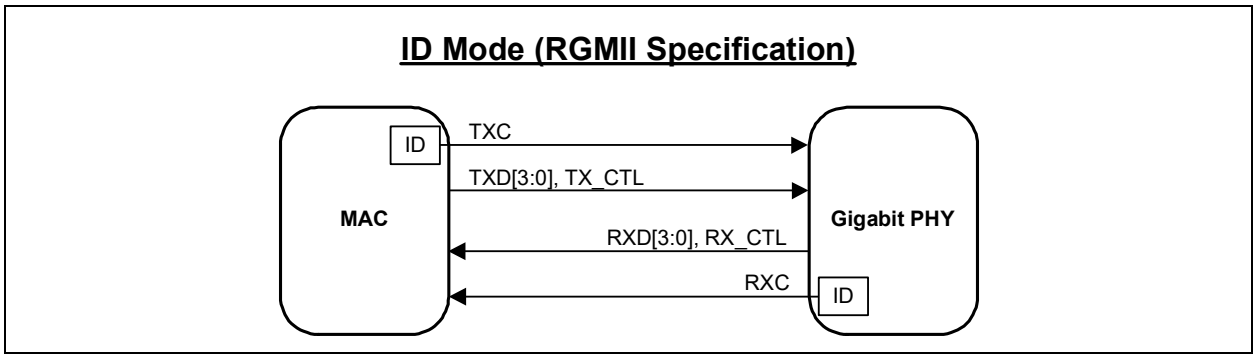
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The default RGMII timings imply:

- RXC clock skew is set by the default register settings.
- TXC clock skew is provided by the MAC.
- No PCB delay is required for TXC and RXC clocks.

Figure 4-5 illustrates the RGMII Version 2.0 Specification Internal Delay operation.

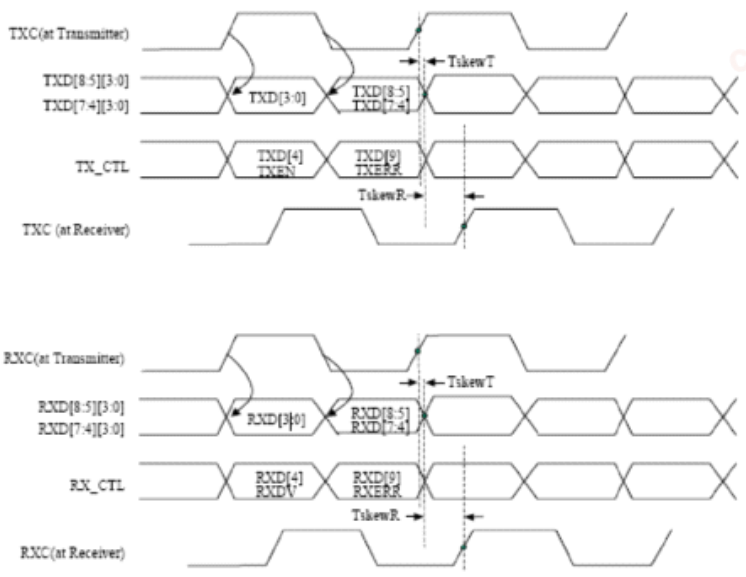
FIGURE 4-5: RGMII VERSION 2.0 INTERNAL DELAY OPERATION



When computing the RGMII timing relationships, delays along the entire data path must be aggregated to determine the total delay to be used for comparison between RGMII pins within their respective timing group. For the transmit data path, total delay includes MAC output delay, MAC-to-PHY PCB routing delay, and PHY input delay and skew setting (if any). For the receive data path, the total delay includes PHY output delay, PHY-to-MAC PCB routing delay, and MAC input delay and skew setting (if any).

Figure 4-6 and Figure 4-7, from the RGMII v2.0 Specification, are provided as references to understanding RGMII v1.3 external delay and RGMII v2.0 on-chip delay timings.

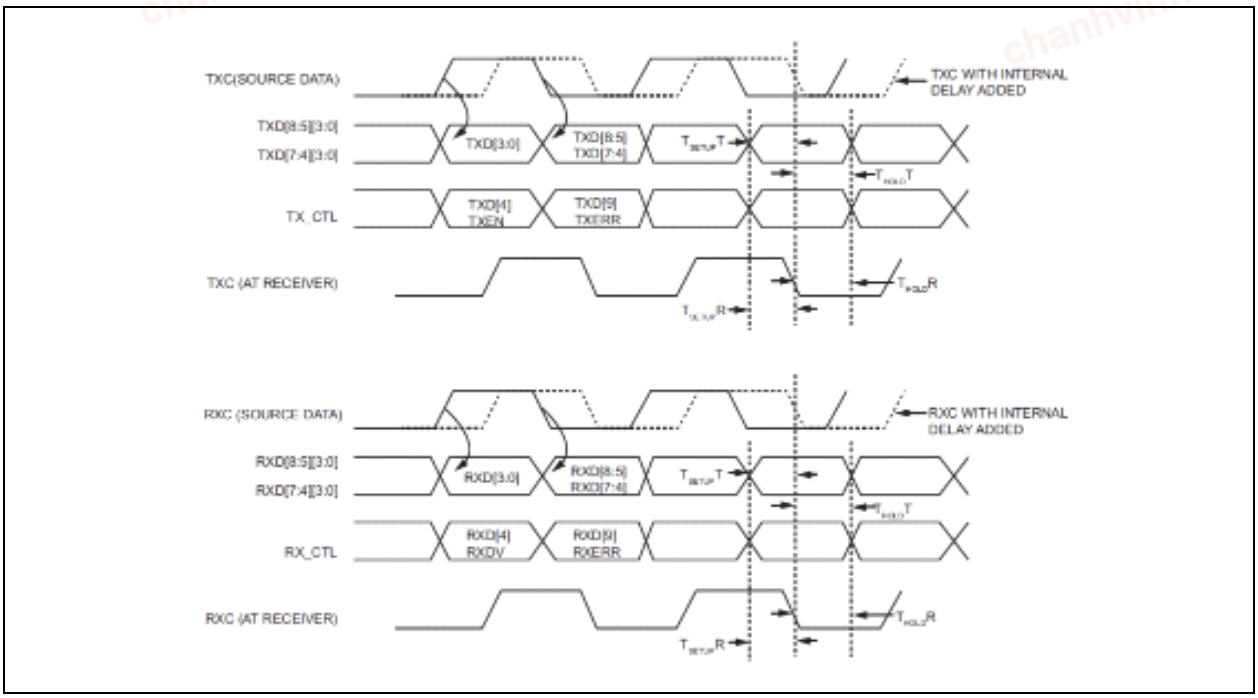
FIGURE 4-6: RGMII V2.0 SPEC (MULTIPLEXING AND TIMING DIAGRAM - ORIGINAL RGMII (V1.3) WITH EXTERNAL DELAY



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FIGURE 4-7: RGMII V2.0 SPEC (MULTIPLEXING AND TIMING DIAGRAM - ORIGINAL RGMII (V2.0) WITH INTERNAL DELAY



The following notes provide clarification for Figure 4-7.

TXC (SOURCE DATA), solid line, is the MAC GTX_CLK clock output timing per RGMII v1.3 Specification (PCB delay line required or PHY internal delay required)

TXC (SOURCE DATA) WITH INTERNAL DELAY ADDED, dotted line, is the MAC GTX_CLK clock output timing per RGMII v2.0 Specification (no PCB delay required and no PHY internal delay required)

RXC (SOURCE DATA), solid line, is the PHY RX_CLK clock output timing per RGMII v1.3 Specification (PCB delay line required or MAC internal delay required)

RXC (SOURCE DATA) WITH INTERNAL DELAY ADDED, dotted line, is the PHY RX_CLK clock output timing per RGMII v2.0 Specification (no PCB delay required and no MAC internal delay required)

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TABLE 4-4: RGMII V2.0 SPECIFICATION

Parameter	Description	Min.	Typ.	Max.	Units
$T_{skew}T$	Data-to-clock output skew (at transmitter) per RGMII v1.3 (external delay)	-500	—	500	ps
$T_{skew}R$	Data-to-clock input skew (at receiver) per RGMII v1.3 (external delay)	1.0	—	2.6	ns
$T_{setup}T$	Data-to-clock output setup (at transmitter – integrated delay)	1.2	2.0	—	ns
$T_{hold}T$	Clock-to-data output hold (at transmitter – integrated delay)	1.2	2.0	—	ns
$T_{setup}R$	Data-to-clock input setup (at receiver – integrated delay)	1.0	2.0	—	ns
$T_{hold}R$	Clock-to-data input hold (at receiver – integrated delay)	1.0	2.0	—	ns
t_{cyc} (1000BASE-T)	Clock cycle duration for 1000BASE-T	7.2	8.0	8.8	ns
t_{cyc} (100BASE-TX)	Clock cycle duration for 100BASE-TX	36	40	44	ns
t_{cyc} (10BASE-T)	Clock cycle duration for 10BASE-T	360	400	440	ns

The RGMII Version 2.0 Specification defines the RGMII data-to-clock skews only for 1000 Mbps operation, which uses both clock edges for sampling the data and control signals at the 125 MHz clock frequency (8 ns period). For 10/100 Mbps operations, the data signals are sampled on the rising clock edge and the control signals are sampled on both clock edges. With slower clock frequencies, 2.5 MHz (400 ns period) for 10 Mbps and 25 MHz (40 ns period) for 100 Mbps, the RGMII data-to-clock skews for 10/100 Mbps operations will have greater timing margins than for 1000 Mbps operation, and therefore can be relaxed from 2.6 ns (maximum) for 1000 Mbps to 160 ns (maximum) for 10 Mbps and 16 ns (maximum) for 100 Mbps.

4.9.3.1 RGMII DLL Based Clock Skew

The delays on RXC (enabled by default) and optionally on TXC (disabled by default) are provided by internal DLLs.

When the RGMII delay is bypassed, the delay chain is completely omitted and the DLL output clock is the same as the DLL input clock. DLL bypass is controlled by the bypass rxdll and bypass txdll bits of the RX DLL Control Register and the TX DLL Control Register for RXC and TXC respectively.

When DLL tuning is enabled (normal operation) the DLL is dynamically tuned. The txdll_tap_adj and rxdll_tap_adj fields in the TX DLL Control Register and the RX DLL Control Register are used to statically account for the output multiplexer stage in the delay chain. The DLL tap select value is dynamically calculated and adjusts the delay chain.

When DLL tuning is disabled, by setting the rxdll_tune_disable or txdll_tune_disable bits in the RX DLL Control Register or TX DLL Control Register respectively, the DLL is not dynamically tuned but is still used to provide a fixed delay. The txdll_tap_sel and rxdll_tap_sel settings are used as fixed delay values. The txdll_tap_adj and rxdll_tap_adj fields are not used.

The DLL must be reset whenever a new value is programmed into the txdll_tap_sel or rxdll_tap_sel field. This is accomplished by the respective rxdll_reset or rxdll_reset bit.

Note: These bits are not self-clearing and must be set then reset by software.

4.9.3.2 RGMII Pad Skew Registers

It is common to implement RGMII PHY-to-MAC designs that either PHY, MAC, or both PHY and MAC are not fully RGMII v2.0 compliant with on-chip clock delay. These combinations of mixed RGMII v1.3/v2.0 designs and plus sometimes non-matching RGMII PCB trace routings require a review of the entire RGMII system timings (PHY on-chip, PCB trace delay, MAC on-chip) to compute the aggregate clock delay and determine if the clock delay timing is met.

If timing adjustment is needed, pad skew registers are available for all RGMII pins (clocks, control signals, and data bits) to provide programming options to adjust or correct the timing relationship for each RGMII pin. Because RGMII is a source-synchronous bus interface, the timing relationship needs to be maintained only within the RGMII pin's respective timing group.

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- RGMII transmit timing group pins: TXC, TX_CTL, TXD[3:0]
- RGMII receive timing group pins: RXC, RX_CTL, RXD[3:0]

The following four registers located at MMD Address 2h are provided for pad skew programming:

- Clock Invert and Control Signal Pad Skew Register
- RGMII RX Data Pad Skew Register
- RGMII TX Data Pad Skew Register
- Clock Pad Skew Register

The RGMII control signals and data bits have 4-bit skew settings, while the RGMII clocks have 5-bit skew settings.

Each register value increment is approximately:

- Data and control: 28ps (min) to 73ps (max)
- RXC and TXC: 24ps (min) to 58ps (max)

A lower value decreases the delay, while a higher value increases the delay.

Table 4-5 and Table 4-6 list the approximate absolute delay for each pad skew (value) setting.

TABLE 4-5: ABSOLUTE DELAY FOR 5-BIT PAD SKEW SETTING

Pad Skew Value	Delay (ns)
0_0000	-0.17(min) / -0.41(max)
0_0001	-0.14(min) / -0.35(max)
0_0010	-0.12(min) / -0.29(max)
0_0011	-0.1(min) / -0.23(max)
0_0100	-0.07(min) / -0.17(max)
0_0101	-0.05(min) / -0.12(max)
0_0110	-0.02(min) / -0.06(max)
0_0111	No delay adjustment (default value)
0_1000	0.02(min) / 0.06(max)
0_1001	0.05(min) / 0.12(max)
0_1010	0.07(min) / 0.17(max)
0_1011	0.1(min) / 0.23(max)
0_1100	0.12(min) / 0.29(max)
0_1101	0.14(min) / 0.35(max)
0_1110	0.17(min) / 0.41(max)
0_1111	0.19(min) / 0.46(max)
1_0000	0.22(min) / 0.52(max)
1_0001	0.24(min) / 0.58(max)
1_0010	0.26(min) / 0.64(max)
1_0011	0.29(min) / 0.7(max)
1_0100	0.31(min) / 0.75(max)
1_0101	0.34(min) / 0.81(max)
1_0110	0.36(min) / 0.87(max)
1_0111	0.38(min) / 0.93(max)
1_1000	0.41(min) / 0.99(max)
1_1001	0.43(min) / 1.04(max)
1_1010	0.46(min) / 1.1(max)
1_1011	0.48(min) / 1.16(max)
1_1100	0.5(min) / 1.22(max)
1_1101	0.53(min) / 1.28(max)

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TABLE 4-5: ABSOLUTE DELAY FOR 5-BIT PAD SKEW SETTING (CONTINUED)

Pad Skew Value	Delay (ns)
1_1110	0.55(min) / 1.33(max)
1_1111	0.58(min) / 1.39(max)

TABLE 4-6: ABSOLUTE DELAY FOR 4-BIT PAD SKEW SETTING

Pad Skew Value	Delay (ns)
0000	-0.20(min) / -0.51(max)
0001	-0.17(min) / -0.44(max)
0010	-0.14(min) / -0.37(max)
0011	-0.11(min) / -0.29(max)
0100	-0.08(min) / -0.22(max)
0101	-0.06(min) / -0.15(max)
0110	-0.03(min) / -0.07(max)
0111	No delay adjustment (default value)
1000	0.03(min) / 0.07(max)
1001	0.06(min) / 0.15(max)
1010	0.08(min) / 0.22(max)
1011	0.11(min) / 0.29(max)
1100	0.14(min) / 0.37(max)
1101	0.17(min) / 0.44(max)
1110	0.20(min) / 0.51(max)
1111	0.22(min) / 0.58(max)

The following examples show how to read/write to the Clock Pad Skew Register for the RGMII TXC and RXC skew settings. MMD register access is through the direct portal MMD Access Control Register and MMD Access Address/Data Register. For more programming details, refer to Section 5.3, "MDIO Manageable Device (MMD) Registers".

- Example: Read back the value of the Clock Pad Skew Register.
  - Write MMD Access Control Register = 0x0002 / / Select MMD Device Address 2h
  - Write MMD Access Address/Data Register = 0x0008 / / Select Clock Pad Skew Register
  - Write MMD Access Control Register = 0x4002 / / Select register data for Clock Pad Skew Register
  - Read MMD Access Address/Data Register / / Read value of Clock Pad Skew Register

- Example: Write a value of 0x03FF (delay TXC and RXC pad skews to their maximum values) to the Clock Pad Skew Register
  - Write MMD Access Control Register = 0x0002 / / Select MMD Device Address 2h
  - Write MMD Access Address/Data Register = 0x0008 / / Select Clock Pad Skew Register
  - Write MMD Access Control Register = 0x4002 / / Select register data for Clock Pad Skew Register
  - Write MMD Access Address/Data Register = 0x03FF / / Write value 0x03FF to Clock Pad Skew Register

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4.9.4 RGMII IN-BAND STATUS

The KSZ9131RNX provides in-band status to the MAC during the inter-frame gap when RX_DV is de-asserted. RGMII in-band status is always enabled after power-up.

The in-band status is sent to the MAC using the RXD[3:0] data pins, and is described in Table 4-7.

TABLE 4-7: RGMII IN-BAND STATUS

RX_CTL	RXD3	RXD[2:1]	RXD0
0 / 0 (equivalent to RX_DV = 0 / RX_ER = 0)	Duplex Status 0 = Half-duplex 1 = Full-duplex	RX_CLK clock speed 00 = 2.5 MHz (10 Mbps) 01 = 25 MHz (100 Mbps) 10 = 125 MHz (1000 Mbps) 11 = Reserved	Link Status 0 = Link down 1 = Link up

4.9.5 RGMII EEE LOW POWER IDLE

The KSZ9131RNX supports EEE Low Power Idle on the RGMII interface. This is encoded as RX_CTL = 0/1 (equivalent to RX_DV = 0 / RX_ER = 1) and RXD[3:0] = 0x1 / 0x0 (equivalent to RXD[7:0] = 0x01) for receive and as TX_CTL = 0/1 (equivalent to TX_EN = 0 / TX_ER = 1) and TXD[3:0] = 0x1 / 0x0 (equivalent to TXD[7:0] = 0x01) for transmit.

4.10 MII Management (MIIM) Interface

The KSZ9131RNX supports the IEEE 802.3 MII management interface, also known as the Management Data Input/Output (MDIO) interface. This interface allows upper-layer devices to monitor and control the state of the KSZ9131RNX. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. More details about the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the physical connection mentioned earlier, which allows an external controller to communicate with one or more KSZ9131RNX devices. Each KSZ9131RNX device is assigned a unique PHY address between 0h and 7h by the PHYAD[2:0] strapping pins.
- A 32-register address space for direct access to IEEE-defined registers and vendor-specific registers, and for indirect access to MMD addresses and registers. See the Register Map section.

Table 4-8 shows the MII management frame format for the KSZ9131RNX.

TABLE 4-8: MII MANAGEMENT FRAME FORMAT FOR THE KSZ9131MNX

	Preamble	Start of Frame	Read/Write OP Code	PHY Address Bits [4:0]	REG Address Bits [4:0]	TA	Data Bits [15:0]	Idle
Read	32 1's	01	10	00AAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	00AAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

4.10.1 ALL PHYS ADDRESS

Normally, the Ethernet PHY is accessed at the PHY address set by the PHYAD[2:0] strapping pins.

PHY Address 0h is optionally supported as the broadcast PHY address, which allows for a single write command to simultaneously program an identical PHY register for two or more PHY devices (for example, using PHY Address 0h to set the Basic Control Register to a value of 0x1940 to set Bit [11] to a value of one to enable software power-down).

PHY address 0 is enabled (in addition to the PHY address set by the PHYAD[2:0] strapping pins) when the All-PHYAD Enable bit in the Common Control Register is a 1.

4.10.2 MDIO OUTPUT DRIVE MODE

The MDIO output pin drive mode is controlled by the MDIO Drive bit in MDIO Drive Register. When set to a 0, the MDIO output is open-drain. When set to a 1, the MDIO output is push-pull.

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4.11 Interrupt (INT_N)

The INT_N pin is an optional interrupt signal that is used to inform the external controller that there has been a status update in the KSZ9131RNX PHY register. Bits [15:8] of the Interrupt Control/Status Register are the interrupt control bits that enable and disable the conditions for asserting the INT_N signal. Bits [7:0] of the Interrupt Control/Status Register are the interrupt status bits that indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading the Interrupt Control/Status Register.

The Interrupt Polarity Invert bit of the Control Register sets the interrupt level to active high or active low. The default is active low.

The MII management bus option gives the MAC processor complete access to the KSZ9131RNX control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll the PHY for status change.

4.12 LED Support

The KSZ9131RNX provides two programmable LED output pins, LED2 and LED1, which are configurable to support three LED modes. The LED mode is configured by the LED_MODE strap-in as well as the KSZ9031 LED Mode bit in the KSZ9031 LED Mode Register. It is latched at power-up/reset and is defined as follows:

- KSZ9031 LED Mode = 1, LED_MODE strap input high (pulled up): Individual-LED Mode
- KSZ9031 LED Mode = 1, LED_MODE strap input low (pulled down): Tri-Color-LED Mode
- KSZ9031 LED Mode = 0, LED_MODE strap is unused: Enhanced LED Mode

Each LED output pin can directly drive an LED with a series resistor (typically 220Ω to 470Ω).

4.12.1 INDIVIDUAL-LED MODE

In individual-LED mode, the LED2 pin indicates the link status while the LED1 pin indicates the activity status, as shown in Table 4-9.

Note:

- The LEDs are forced OFF when the Isolate (PHY_ISO) bit in the Basic Control Register is set.
- The LEDs are forced OFF when the Power Down bit in the Basic Control Register is set.

TABLE 4-9: INDIVIDUAL-LED MODE - PIN DEFINITION

LED Pin	Pin State	LED Definition	Link/Activity
LED2	H	OFF	Link Off
	L	ON	Link On (any speed)
LED1	H	OFF	No Activity
	Toggle	Blinking	Activity (RX, TX)

4.12.2 TRI-COLOR-LED MODE

In tri-color-LED mode, the link and activity status are indicated by the LED2 pin for 1000BASE-T; by the LED1 pin for 100BASE-TX; and by both LED2 and LED1 pins, working in conjunction, for 10BASE-T. This is summarized in Table 4-10.

Note:

- The LEDs are forced OFF when the Isolate (PHY_ISO) bit in the Basic Control Register is set.
- The LEDs are forced OFF when the Power Down bit in the Basic Control Register is set.

TABLE 4-10: TRI-COLOR-LED MODE - PIN DEFINITION

LED Pin (State)		LED Pin (Definition)		Link/Activity
LED2	LED1	LED2	LED1	
H	H	OFF	OFF	Link Off
L	H	ON	OFF	1000 Link/No Activity

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TABLE 4-10: TRI-COLOR-LED MODE - PIN DEFINITION (CONTINUED)

LED Pin (State)		LED Pin (Definition)		Link/Activity
LED2	LED1	LED2	LED1	
Toggle	H	Blinking	OFF	1000 Link/Activity (RX, TX)
H	L	OFF	ON	100 Link/No Activity
H	Toggle	OFF	Blinking	100 Link/Activity (RX, TX)
L	L	ON	ON	10 Link/No Activity
Toggle	Toggle	Blinking	Blinking	10 Link/Activity (RX, TX)

4.12.3 ENHANCED LED MODE

Enhanced LED mode is enabled when the KSZ9031 LED Mode bit in the KSZ9031 LED Mode Register is cleared. In Enhanced LED mode, each LED can be configured to display different status information that can be selected by setting the corresponding LED Configuration field of the LED Mode Select Register. The modes are shown in Table 4-11. The blink/pulse-stretch and other LED settings can be configured via the LED Behavior Register.

Note: The LEDs are forced OFF when the Power Down bit in the Basic Control Register is set.

TABLE 4-11: LED MODE AND FUNCTION SUMMARY

Mode	Name	Description
0	Link/Activity	1 (led off) = No link in any speed on any media interface. 0 (led on) = Valid link at any speed on any media interface. Blink or pulse stretch (led turns off) = Valid link at any speed on any media interface with activity present.
1	Link1000/Activity	1 (led off) = No link at 1000BASE-T. 0 (led on) = Valid link at 1000BASE-T. Blink or pulse stretch (led turns off) = Valid link at 1000BASE-T with activity present.
2	Link100/Activity	1 (led off) = No link at 100BASE-TX. 0 (led on) = Valid link at 100BASE-TX. Blink or pulse stretch (led turns off) = Valid link at 100BASE-TX with activity present.
3	Link10/Activity	1 (led off) = No link at 10BASE-T. 0 (led on) = Valid link at 10BASE-T. Blink or pulse stretch (led turns off) = Valid link at 10BASE-T with activity present.
4	Link100/1000/Activity	1 (led off) = No link at 100BASE-TX or 1000BASE-T. 0 (led on) = Valid link at 100BASE-TX or 1000BASE-T. Blink or pulse stretch (led turns off) = Valid link at 100BASE-TX or 1000BASE-T, with activity present.
5	Link10/1000/Activity	1 (led off) = No link at 10BASE-T or 1000BASE-T. 0 (led on) = Valid link at 10BASE-T or 1000BASE-T. Blink or pulse stretch (led turns off) = Valid link at 10BASE-T or 1000BASE-T, with activity present.
6	Link10/100/Activity	1 (led off) = No link at 10BASE-T or 100BASE-TX. 0 (led on) = Valid link at 10BASE-T or 100BASE-TX. Blink or pulse stretch (led turns off) = Valid link at 10BASE-T or 100BASE-TX, with activity present.

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TABLE 4-11: LED MODE AND FUNCTION SUMMARY (CONTINUED)

Mode	Name	Description
7	RESERVED	RESERVED
8	Duplex/Collision	1 (led off) = Link established in half-duplex mode, or no link established. 0 (led on) = Link established in full-duplex mode. Blink or pulse stretch (led turns on) = Link established in half-duplex mode but collisions are present.
9	Collision	1 (led off) = No collisions detected. Blink or pulse stretch (led turns on) = Collision detected.
10	Activity	1 (led off) = No activity present. Blink or pulse stretch (led turns on) = Activity present. (becomes TX activity present if the LED Activity Output Select bit in the LED Behavior Register is set to 1.)
11	RESERVED	RESERVED
12	Auto-Negotiation Fault	1 (led off) = No Auto-Negotiation fault present. 0 (led on) = Auto-Negotiation fault occurred.
13	RESERVED	RESERVED
14	Force LED Off	1 (led off) = De-asserts the LED.
15	Force LED On	0 (led on) = Asserts the LED.

4.12.3.1 LED Behavior

Using the LED Behavior Register, the following LED behaviors can be configured.:

- LED Combine
- LED Blink or Pulse-Stretch
- Rate of LED Blink or Pulse-Stretch
- LED Pulsing Enable

4.12.3.1.1 LED Combine

Enables an LED to display the status for a combination of primary and secondary modes. This can be enabled or disabled for each LED pin via the LED Combination Disables field of the LED Behavior Register. For example, a copper link running in 1000BASE-T mode with activity present can be displayed with one LED by configuring an LED pin to Link1000/Activity mode. The LED asserts when linked to a 1000BASE-T partner and also blinks or performs pulse-stretch when activity is either transmitted by the PHY or received by the Link Partner. When disabled, the combine feature only provides status of the selected primary function. In this example, only Link1000 asserts the LED, and the secondary mode, activity, does not display if the combine feature is disabled.

4.12.3.1.2 LED Blink or Pulse-Stretch

This behavior is used for activity and collision indication. This can be uniquely configured for each LED pin via the LED Pulse Stretch Enables field of the LED Behavior Register. Activity and collision events can occur randomly and intermittently throughout the link-up period.

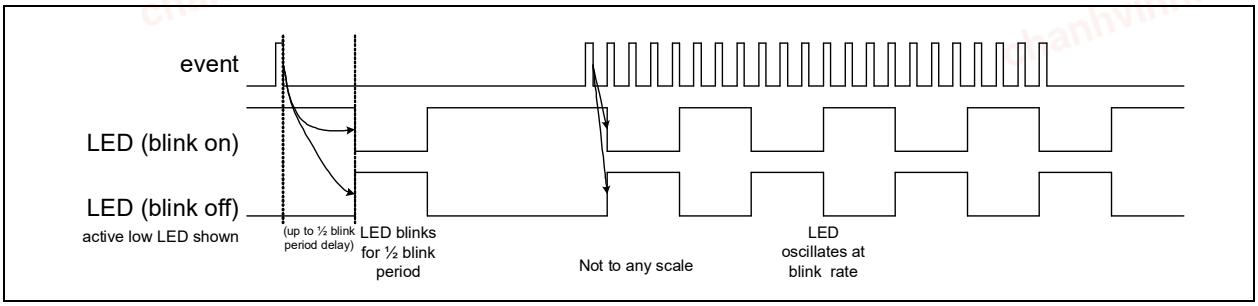
Blink is a 50% duty cycle oscillation of asserting and de-asserting an LED pin.

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As shown in Figure 4-8, for a single event, the LED will blink (either on or off depending on the LED function) for half of the blink period. For continual events, the LED will oscillate at the blink rate.

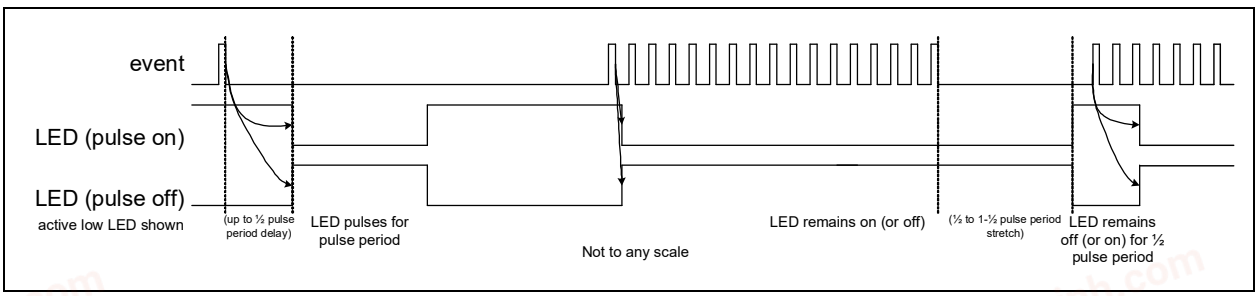
FIGURE 4-8: LED BLINK PATTERN



Pulse-stretch ensures that an LED is asserted and de-asserted for a specific period of time when activity is either present or not present.

As shown in Figure 4-9, for a single event, the LED will pulse (either on or off depending on the LED function) for the full pulse period. For continual events, the LED will remain on (or off) and will extend from a half to one and a half pulse periods once the events terminate. Once off (or on), the LED will remain in that state for at least a half pulse period.

FIGURE 4-9: LED PULSE PATTERN



The blink / pulse stretch rate can be configured, as detailed in Section 4.12.3.1.3, "Rate of LED Blink or Pulse-Stretch".

4.12.3.1.3 Rate of LED Blink or Pulse-Stretch

This behavior controls the LED blink rate or pulse-stretch length when the blink/pulse-stretch is enabled (LED Pulse Stretch Enables) on an LED pin. This can be uniquely configured for each LED pin via the LED Blink / Pulse-Stretch Rate field of the LED Behavior Register. The blink rate, which alternates between a high and low voltage level at a 50% duty cycle, can be set to 2.5 Hz, 5 Hz, 10 Hz, or 20 Hz. For pulse-stretch, the rate can be set to 50 ms, 100 ms, 200 ms, or 400 ms.

4.12.3.1.4 LED Pulsing Enable

To provide additional power savings, the LEDs (when asserted) can be modulated at 5 kHz, 20% duty cycle, by setting the LED Pulsing Enable bit of the LED Behavior Register.

4.13 Loopback Modes

The KSZ9131RNX supports the following loopback operations to verify analog and/or digital data paths.

- Digital (near-end) loopback
- Remote (far-end) loopback
- External connector loopback

4.13.1 DIGITAL (NEAR-END) LOOPBACK

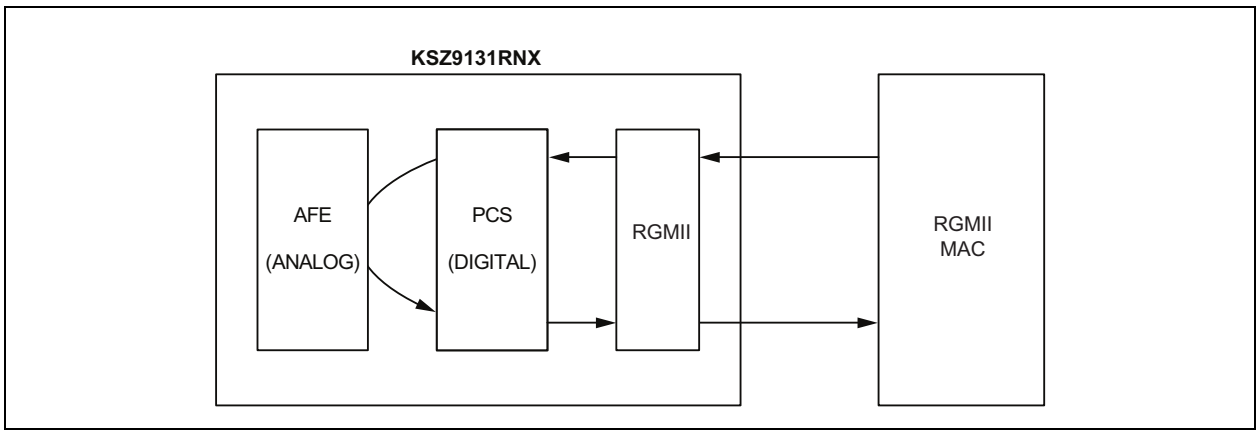
This loopback mode checks the RGMII transmit and receive data paths between the KSZ9131RNX and the external MAC, and is supported for all three speeds (10/100/1000 Mbps) at full-duplex.

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The loopback data path is shown in Figure 4-10.

1. RGMII MAC transmits frames to KSZ9131RNX.
2. Frames are wrapped around inside KSZ9131RNX.
3. KSZ9131RNX transmits frames back to RGMII MAC.

FIGURE 4-10: DIGITAL (NEAR-END) LOOPBACK



The following programming steps and register settings are used for local loopback mode.

For 1000 Mbps loopback,

1. Configure the following registers:
   - MMD 1C, Register 15 = EEEE
   - MMD 1C, Register 16 = EEEE
   - MMD 1C, Register 18 = EEEE
   - MMD 1C, Register 1B = EEEE
2. Configure the Basic Control Register:
   - Bit [14] = 1 // Enable local loopback mode
   - Bits [6, 13] = 10 // Select 1000 Mbps speed
   - Bit [12] = 0 // Disable auto-negotiation
   - Bit [8] = 1 // Select full-duplex mode
3. Configure the Auto-Negotiation Master Slave Control Register:
   - Bit [12] = 1 // Enable master-slave manual configuration
   - Bit [11] = 0 // Select slave configuration (required for loopback mode)

For 10/100 Mbps loopback,

1. Configure the following registers:
   - MMD 1C, Register 15 = EEEE
   - MMD 1C, Register 16 = EEEE
   - MMD 1C, Register 18 = EEEE
   - MMD 1C, Register 1B = EEEE
2. Configure the Basic Control Register:
   - Bit [14] = 1 // Enable local loopback mode
   - Bits [6, 13] = 00 / 01 // Select 10 Mbps/100 Mbps speed
   - Bit [12] = 0 // Disable auto-negotiation
   - Bit [8] = 1 // Select full-duplex mode

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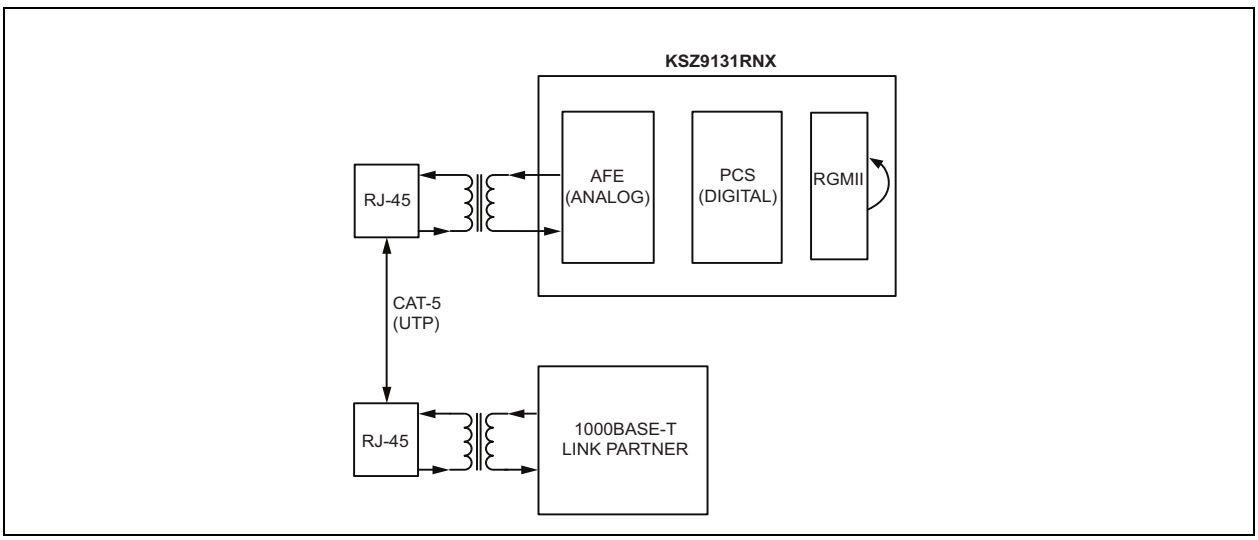
4.13.2 REMOTE (FAR-END) LOOPBACK

This loopback mode checks the line (differential pairs, transformer, RJ-45 connector, Ethernet cable) transmit and receive data paths between the KSZ9131RNX and its link partner, and is supported for 1000BASE-T full-duplex mode only.

The loopback data path is shown in Figure 4-11.

1. The Gigabit PHY link partner transmits frames to KSZ9131RNX.
2. Frames are wrapped around inside KSZ9131RNX.
3. KSZ9131RNX transmits frames back to the Gigabit PHY link partner.

FIGURE 4-11: REMOTE (FAR-END) LOOPBACK



The following programming steps and register settings are used for remote loopback mode.

1. Configure the Basic Control Register:
   - Bits [6, 13] = 10 // Select 1000 Mbps speed
   - Bit [12] = 0 // Disable auto-negotiation
   - Bit [8] = 1 // Select full-duplex mode

   Or just auto-negotiate and link up at 1000BASE-T full-duplex mode with the link partner.
2. Configure the Remote Loopback Register:
   - Bit [8] = 1 // Enable remote loopback mode
3. Connect RX_CLK to TX_CLK

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4.13.3 EXTERNAL CONNECTOR LOOPBACK

The connector loopback testing feature allows the twisted pair interface to be looped back externally. When using this feature, the PHY must be connected to a loopback connector or a loopback cable. Pair A should be connected to pair B, and pair C to pair D, as shown in Figure 4-12. The connector loopback feature functions at all available interface speeds.

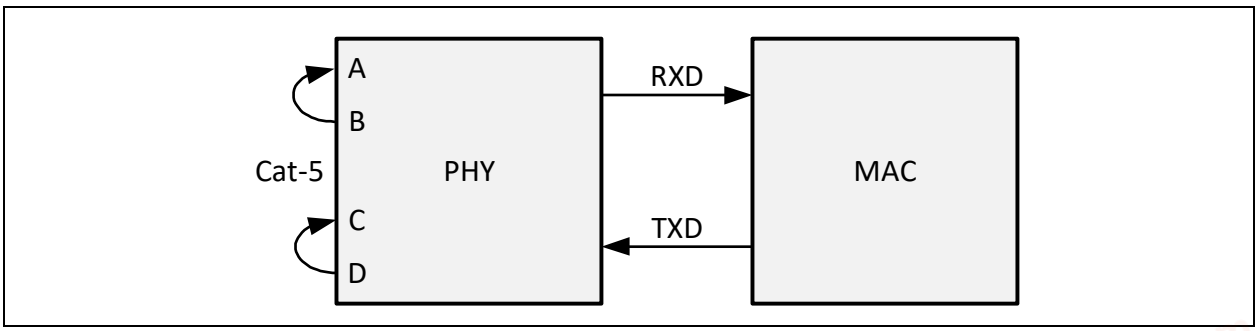
This loopback tests the PHY digital and MAC connectivity.

When using the connector loopback testing feature, the device Auto-Negotiation, speed, and duplex configuration is set using the Basic Control Register, Auto-Negotiation Advertisement Register, and Auto-Negotiation Master Slave Control Register.

For 1000BASE-T connector loopback, the following additional writes are required to be executed in the following order:

- Disable Auto-Negotiation and set the speed to 1000Mbps and the duplex to full by setting the Basic Control Register to a value of 0140h.
- Set the Master-Slave configuration to master by setting the Master/Slave Manual Configuration Enable and Master/Slave Manual Configuration Value bits in the Auto-Negotiation Master Slave Control Register.
- Enable the 1000BASE-T connector loopback by setting the Ext_lpbk bit in the External Loopback Register.

FIGURE 4-12: EXTERNAL CONNECTOR LOOPBACK



4.14 LinkMD® Cable Diagnostic

The LinkMD function uses time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems, such as open circuits, short circuits, and impedance mismatches as well as the distance to the fault. Each of the four twisted pairs is tested separately.

LinkMD operates by sending a pulse of known amplitude and duration down the selected differential pair, then analyzing the polarity and shape of the reflected signal to determine the type of fault: open circuit for a positive/non-inverted amplitude reflection and short circuit for a negative/inverted amplitude reflection. The time duration for the reflected signal to return provides the approximate distance to the cabling fault. The LinkMD function processes this TDR information and presents it as a numerical value that can be translated to a cable distance.

LinkMD is initiated by accessing the LinkMD Cable Diagnostic Register in conjunction with the Auto-MDI/MDI-X Register. The latter register is needed to disable the Auto MDI/MDI-X function before running the LinkMD test. Additionally, a software reset (PHY Soft Reset (RESET) bit in the Basic Control Register = 1) should be performed before and after running the LinkMD test. The reset helps to ensure the KSZ9131RNX is in the normal operating state before and after the test.

Prior to running the cable diagnostics, Auto-negotiation should be disabled, full duplex set and the link speed set to 1000Mbps via the Basic Control Register. The Master-Slave configuration should be set to Slave by writing a value of 0x1000 to the Auto-Negotiation Master Slave Control Register.

To test each individual cable pair, set the cable pair in the Cable Diagnostics Test Pair (VCT_PAIR[1:0]) field of the LinkMD Cable Diagnostic Register, along with setting the Cable Diagnostics Test Enable (VCT_EN) bit. The Cable Diagnostics Test Enable (VCT_EN) bit will self clear when the test is concluded.

The test results (for the pair just tested) are available in the LinkMD Cable Diagnostic Register. With the Bit[9:0] Definition (VCT_SEL[1:0]) field set to 0, the Cable Diagnostics Status (VCT_ST[1:0]) field will indicate a Normal (properly terminated), Open or Short condition.

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If the test result was Open or Short, the Cable Diagnostics Data or Threshold (VCT_DATA[7:0]) field indicates the distance to the fault in meters as approximately:

- distance to fault = (VCT_DATA - 22) * 4 / cable propagation velocity

With an accuracy of +/- 2% to 3% for short and medium cables and +/- 5% to 6% for long cables.

APPLICATION NOTE: If the Cable Diagnostics Status (VCT_ST[1:0]) field indicates Failed, it is possible the link partner is forced to 100BASE-TX or 1000BASE-T mode.

4.15 Self-Test Frame Generation and Checking

The device is capable of generating and checking frames. The device must be connected to a loopback connector or a loopback cable. Pair A should be connected to pair B, and pair C to pair D, as shown in Figure 4-12.

Normally, the device does not require a 125MHz clock to be supplied into the TXC input pin. An external clock may be used when the Self_test_external_clk_sel bit in the Self-Test Enable Register is set high.

Auto-negotiation should be disabled, full duplex set and the desired link speed set via the Basic Control Register.

For 10BASE-T and 100BASE-TX:

- Auto-MDIX should be disabled and the desired configuration (MDI vs. MDIX) selected via the Swap-Off and MDI Set bits in the Auto-MDI/MDI-X Register. Selecting MDI vs. MDIX will test different sections of the PHY.

For 1000BASE-T:

- Set the Master-Slave configuration to master by setting the Master/Slave Manual Configuration Enable and Master/Slave Manual Configuration Value bits in the Auto-Negotiation Master Slave Control Register.
- Enable the 1000BASE-T connector loopback by setting the Ext_lpbk bit in the External Loopback Register.
- Set the Ethernet MAC to 1000 Mbps operation (this is necessary so that a 125MHz clock is provided to the TXC input pin).

The Self-Test mode is enabled by setting a frame count into the Self-Test Packet Count LO Register and Self-Test Packet Count HI Register and then setting the following in order:

- Self_test_frame_cnt_en bit in the Self-Test Frame Count Enable Register
- Self_test_en bit in the Self-Test Enable Register
- Self_test_pgen_en bit in the Self-Test PGEN Enable Register

Once the Self_test_done bit in the Self-Test Status Register is set, the results can be determined through the following:

- Self-Test Correct Count HI Register / Self-Test Correct Count LO Register
- Self-Test Error Count HI Register / Self-Test Error Count LO Register
- Self-Test Bad SFD Count HI Register / Self-Test Bad SFD Count LO Register

4.16 NAND Tree Support

The KSZ9131RNX provides parametric NAND tree support for fault detection between chip I/Os and board. NAND tree mode is enabled at power-up/reset with the MODE[3:0] strap-in pins set to ‘0100’. Table 4-12 lists the NAND tree pin order. To test any given pin, the pin is toggled while holding the lower ranked pins low and the higher ranked pins high, causing a toggle on the output of the tree.

APPLICATION NOTE: Since the NAND tree output is on the CLK125_NDO pin, the pin must be enabled for output by using the CLK125_EN strap input.

TABLE 4-12: NAND TREE TEST PIN ORDER FOR KSZ9131

Pin	Description
LED2	Input
LED1/PME_N1	Input
TXD0	Input
TXD1	Input
TXD2	Input

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TABLE 4-12: NAND TREE TEST PIN ORDER FOR KSZ9131 (CONTINUED)

Pin	Description
TXD3	Input
TXC	Input
TX_CTL	Input
RXD3	Input
RXD2	Input
RXD1	Input
RXD0	Input
RX_CTL	Input
RXC	Input
INT_N/PME_N2	Input
MDC	Input
MDIO	Input
CLK125_NDO	Output

4.17 Power Management

The KSZ9131RNX incorporates a number of power-management modes and features that provide methods to consume less energy. These are discussed in the following sections.

4.17.1 SMART POWER SAVING

For shorter cable lengths (< ~70 meters) the signal to noise ratio is sufficiently high to allow the reduction of ADC resolution as well as DPS taps, Based on the detected cable length, the device automatically reduces power consumption by approximately 20mW.

4.17.2 ENERGY-DETECT POWER-DOWN MODE (EDPD)

Energy-detect power-down (EDPD) mode is used to further reduce the transceiver power consumption when the cable is unplugged. It is enabled by writing a one to the EDPD Mode Enable bit in the EDPD Control Register, and is in effect when auto-negotiation mode is enabled and the cable is disconnected (no link).

In EDPD Mode, the KSZ9131RNX shuts down all transceiver blocks, except for the transmitter and energy detect circuits. Power can be reduced further by extending the time interval between the transmissions of link pulses to check for the presence of a link partner. The periodic transmission of link pulses is needed to ensure the KSZ9131RNX and its link partner, when operating in the same low-power state and with Auto MDI/MDI-X disabled, can wake up when the cable is connected between them. By default, EDPD mode is disabled after power-up. Previous register setting are maintained when EDPD mode is cleared. EDPD operation may be adjusted via the p_edpd_mask_timer[1:0], p_edpd_timer[1:0] and p_EDPD_random_dis fields in the EDPD Control Register within the MMD address space.

4.17.3 SOFTWARE POWER-DOWN MODE (SPD)

The KSZ9131RNX supports a software power down (SPD) mode. This mode is used to power down the device when it is not in use after power-up. Software power-down mode is enabled by writing a one to the Power Down bit in the Basic Control Register. The device exits the SPD state after a zero is written to the Power Down bit.

In the SPD state, the device disables most internal functions.

During SPD, the crystal oscillator and PLL are enabled and the internal (125MHz and 250MHz) clocks are gated, The standard registers (0 through 31) and the MII Management Interface operate using the crystal clock.

Previous register settings are maintained during and following the removal of SPD.

APPLICATION NOTE: The internal (125MHz and 250MHz) clock gating maybe overridden by setting the spd_clock_gate_override bit in the Software Power Down Control Register at the cost of increased power.

The following remain operational during SPD:

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- MII Management Interface
  - Only access to the standard registers (0 through 31) is supported.
  - Access to MMD address spaces other than MMD address space 1 is possible if the spd_clock_gate_override bit is set.
  - Access to MMD address space 1 is not possible.
- Voltage Regulator Controller (LDO)
  - The LDO controller can be disabled by setting the active low LDO enable bit in LDO Control Register. An external source of 1.2V is necessary for operation in this case.
- PLL
  - Normally the PLL is enabled during SPD. It may be disabled by setting the spd_pll_disable bit described in Section 4.17.3.1, "SPD Extra Power Savings".
- Crystal Oscillator
  - Normally the Crystal Oscillator is enabled during SPD. It may be disabled by setting the XTAL Disable bit described in Section 4.17.3.1, "SPD Extra Power Savings".

The following are normally disabled during SPD:

- TX and RX clocks
  - If the above mentioned spd_clock_gate_override bit is set, TX and RX clocks would be enabled. They may alternately be stopped by setting the Isolate (PHY_ISO) bit in the Basic Control Register.
- CLK125_NDO pin
  - If the above mentioned spd_clock_gate_override bit is set, CLK125_NDO would be enabled (if previously enabled for clock output). It may alternately be disabled by clearing the clk125 Enable bit in Common Control Register

4.17.3.1 SPD Extra Power Savings

To achieve a lower power usage, the PLL maybe disable during SPD by setting the spd_pll_disable bit in the Software Power Down Control Register prior to entering SPD.

APPLICATION NOTE: A full device reset occurs following the removal of SPD, therefore previous register settings are not maintained for this option.

To further reduce power usage, the crystal oscillator maybe disable by setting the XTAL Disable bit in the XTAL Control Register after setting the spd_pll_disable bit and entering SPD.

Since the MII Management Interface operates using the crystal clock, once this bit is set, the device will become inaccessible. A pin reset or power cycle is required to resume operation.

4.17.4 CHIP POWER-DOWN MODE (CPD)

This mode provides the lowest power state for the KSZ9131RNX device when it is mounted on the board but not in use. Chip power-down (CPD) mode is enabled after power-up/reset with the MODE[3:0] strap-in pins set to '0111'. Chip power-down mode can only be exited by removing device power.

4.18 Energy Efficient Ethernet

The KSZ9131RNX implements Energy Efficient Ethernet (EEE) as described in IEEE Standard 802.3az for line signaling by the four differential pairs (analog side) and according to the multi-source agreement (MSA) of collaborating Gigabit Ethernet chip vendors for the RGMII (digital side). This agreement is based on the IEEE Standard's EEE implementation for GMII (1000 Mbps) and MII (100 Mbps). The specification is defined around an EEE-compliant MAC on the host side and an EEE-compliant link partner on the line side that support the special signaling associated with EEE. EEE saves power by keeping the AC signal on the copper Ethernet cable at approximately 0V peak-to-peak as often as possible during periods of no traffic activity, while maintaining the link-up status. This is referred to as low-power idle (LPI) mode or state.

The KSZ9131RNX has the EEE function enabled as the power-up default setting. The EEE function can be disabled by configuring the following EEE advertisement bits in the EEE Advertisement Register, followed by restarting auto-negotiation (writing a '1' to the Restart Auto-Negotiation (PHY_RST_AN) bit in the Basic Control Register:

- 1000BASE-T EEE bit = 0 // Disable 1000 Mbps EEE mode
- 100BASE-TX EEE bit = 0 // Disable 100 Mbps EEE mode

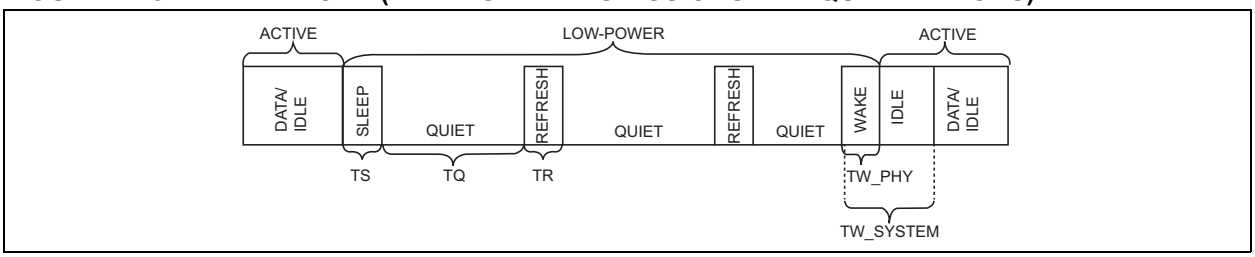
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During LPI mode, the copper link responds automatically when it receives traffic and resumes normal PHY operation immediately, without blockage of traffic or loss of packet. This involves exiting LPI mode and returning to normal 100/1000 Mbps operating mode. The LPI state is controlled independently for transmit and receive paths, allowing the LPI state to be active (enabled) for:

- Transmit cable path only
- Receive cable path only
- Both transmit and receive cable paths

During LPI mode, refresh transmissions are used to maintain the link; power savings occur in quiet periods. Approximately every 20 to 22 milliseconds, a refresh transmission of 200 to 220 microseconds is sent to the link partner. The refresh transmissions and quiet periods are shown in Figure 4-13.

FIGURE 4-13: LPI MODE (REFRESH TRANSMISSIONS AND QUIET PERIODS)



4.18.1 TRANSMIT DIRECTION CONTROL (MAC-TO-PHY)

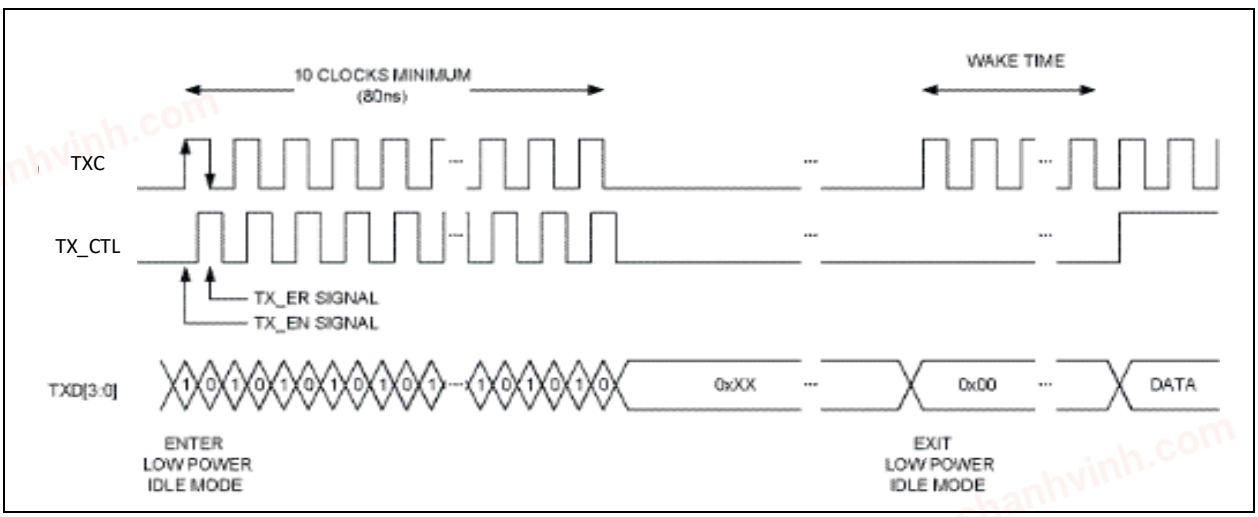
RGMII 1000 Mbps transmission from MAC-to-PHY uses both rising and falling edges of the TXC clock. The KSZ9131RNX uses the TX_CTL pin to clock in the TX_EN signal on the rising edge and the TX_ER signal on the falling edge. It also uses the TXD[3:0] pins to clock in the TX data low nibble bits [3:0] on the rising edge and the TX data high nibble Bits [7:4] on the falling edge.

The KSZ9131RNX enters LPI mode for the transmit direction when its attached EEE-compliant MAC de-asserts the TX_EN signal (the TX_CTL pin outputs low on the rising edge), asserts the TX_ER signal (the TX_CTL pin outputs high on the falling edge), and sets TX data Bits [7:0] to 0000_0001 (TXD[3:0] pins output 0001 on the rising edge and 0000 on the falling edge). The KSZ9131RNX remains in the 1000Mbps transmit LPI state while the MAC maintains the states of these signals. When the MAC changes any of the TX_EN, TX_ER, or TX data signals from their LPI state values, the KSZ9131RNX exits the LPI transmit state.

To save more power, as indicated by the Clock stop capable bit in the PCS Status 1 Register, the MAC can stop the TXC clock after the RGMII signals for the LPI state have been asserted for 10 or more TXC clock cycles.

Figure 4-14 shows the LPI transition for RGMII transmit in 1000 Mbps mode.

FIGURE 4-14: LPI TRANSITION - RGMII (1000 MBPS) TRANSMIT



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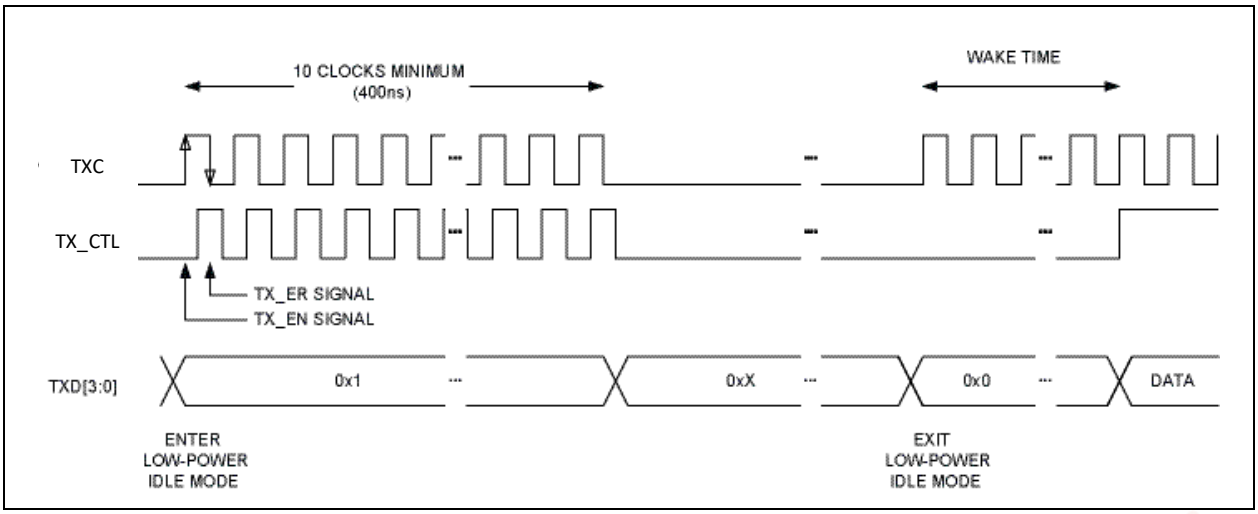
RGMII 100 Mbps transmission from MAC-to-PHY uses both rising and falling edges of the TXC clock. The KSZ9131RNX uses the TX_CTL pin to clock in the TX_EN signal on the rising edge and the TX_ER signal on the falling edge. It also uses the TXD[3:0] pins to clock in the TX data Bits [3:0] on the rising edge.

The KSZ9131RNX enters LPI mode for the transmit direction when its attached EEE-compliant MAC de-asserts the TX_EN signal (the TX_CTL pin outputs low on the rising edge), asserts the TX_ER signal (the TX_CTL pin outputs high on the falling edge), and sets TX data Bits [3:0] to 0001 (the TXD[3:0] pins output 0001). The KSZ9131 remains in the 100 Mbps transmit LPI state while the MAC maintains the states of these signals. When the MAC changes any of the TX_EN, TX_ER, or TX data signals from their LPI state values, the KSZ9131RNX exits the LPI transmit state.

To save more power, as indicated by the Clock-stop enable bit in the PCS Control 1 Register, the MAC can stop the TXC clock after the RGMII signals for the LPI state have been asserted for 10 or more TXC clock cycles.

Figure 4-15 shows the LPI transition for RGMII transmit in 100 Mbps mode.

FIGURE 4-15: LPI TRANSITION - RGMII (100 MBPS) TRANSMIT



4.18.2 RECEIVE DIRECTION CONTROL (PHY-TO-MAC)

RGMII 1000 Mbps reception from PHY-to-MAC uses both rising and falling edges of the RXC clock. The KSZ9131RNX uses the RX_CTL pin to clock out the RX_DV signal on the rising edge and the RX_ER signal on the falling edge. It also uses the RXD[3:0] pins to clock out the RX data low nibble Bits [3:0] on the rising edge and the RX data high nibble Bits [7:4] on the falling edge.

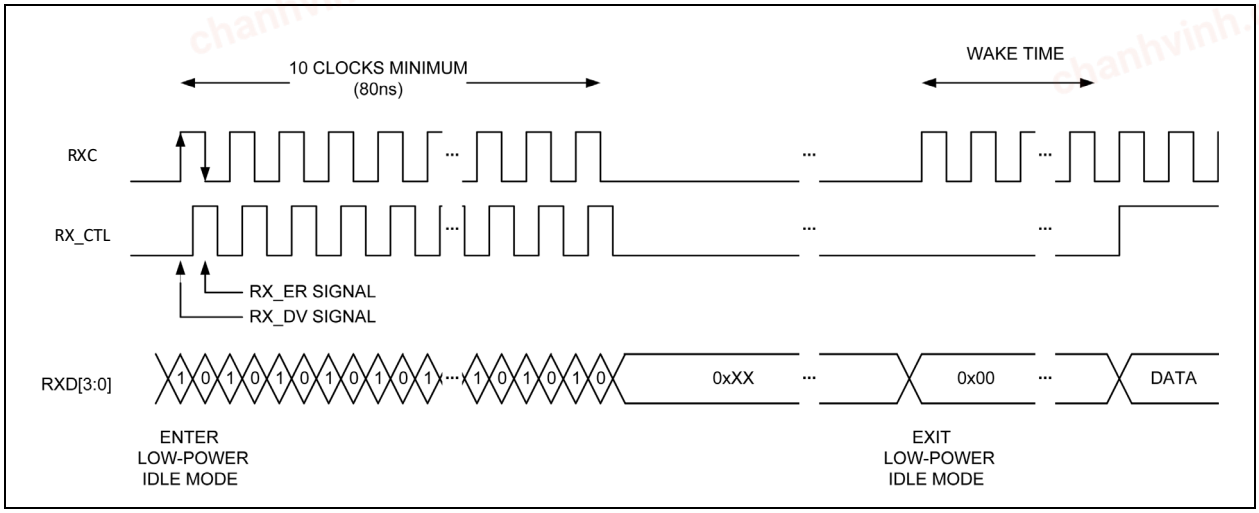
The KSZ9131RNX enters LPI mode for the receive direction when it receives the /P/ code bit pattern (sleep/refresh) from its EEE-compliant link partner. It then drives the RX_CTL pin low on the rising clock edge and high on the falling clock edge to de-assert the RX_DV signal and assert the RX_ER signal, respectively, to the MAC. Also, the RXD[3:0] pins are driven to 0001 on the rising clock edge and 0000 on the falling clock edge to set the RX data Bits [7:0] to 0000_0001. The KSZ9131RNX remains in the 1000 Mbps receive LPI state while it continues to receive the refresh from its link partner, so it will continue to maintain and drive the LPI output states for the RGMII receive output pins to inform the attached EEE-compliant MAC that it is in the receive LPI state. When the KSZ9131 receives a non /P/ code bit pattern (non-refresh), it exits the receive LPI state and sets the RX_CTL and RXD[3:0] output pins accordingly for a normal frame or normal idle.

To save more power, the KSZ9131RNX stops the RXC clock output to the MAC after 10 or more RXC clock cycles have occurred in the receive LPI state. The Clock-stop enable bit in the PCS Control 1 Register controls if the device stops the RXC clock output.

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Figure 4-16 shows the LPI transition for RGMII receive in 1000 Mbps mode.

FIGURE 4-16: LPI TRANSITION - RGMII (1000 MBPS) RECEIVE



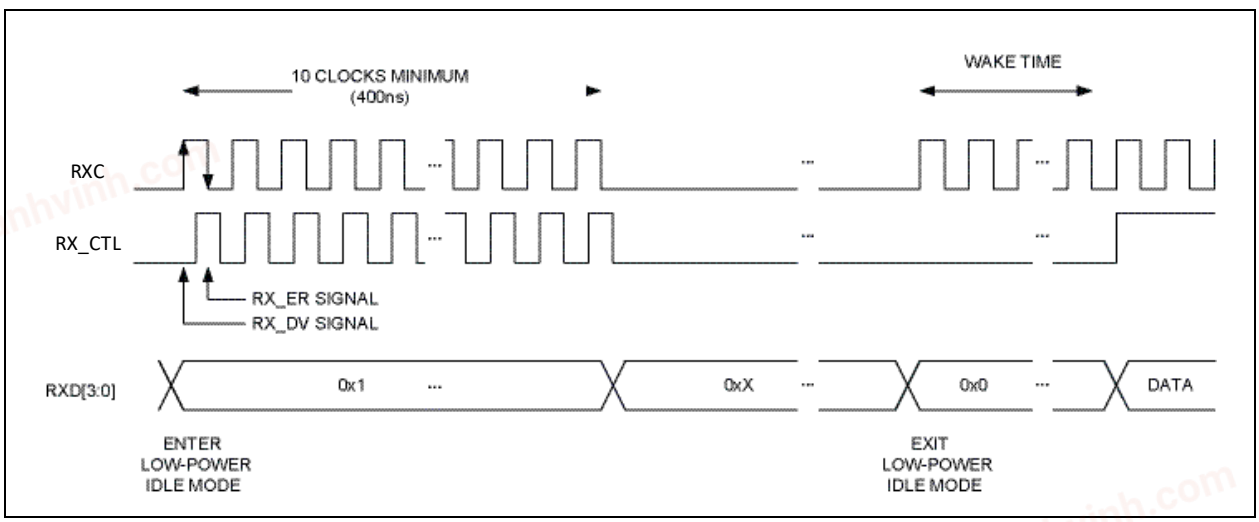
RGMII 100 Mbps reception from PHY-to-MAC uses both rising and falling edges of the RXC clock. The KSZ9131RNX uses the RX_CTL pin to clock out the RX_DV signal on the rising edge and the RX_ER signal on the falling edge. It also uses the RXD[3:0] pins to clock out the RX data Bits [3:0] on the rising edge.

The KSZ9131RNX enters LPI mode for the receive direction when it receives the /P/ code bit pattern (sleep/refresh) from its EEE-compliant link partner. It then drives the RX_CTL pin low on the rising clock edge and high on the falling clock edge to de-assert the RX_DV signal and assert the RX_ER signal, respectively, to the MAC. Also, the RXD[3:0] pins are driven to 0001. The KSZ9131RNX remains in the 100 Mbps receive LPI state while it continues to receive the refresh from its link partner, so it will continue to maintain and drive the LPI output states for the RGMII receive output pins to inform the attached EEE-compliant MAC that it is in the receive LPI state. When the KSZ9131RNX receives a non /P/ code bit pattern (non-refresh), it exits the receive LPI state and sets the RX_CTL and RXD[3:0] output pins accordingly for a normal frame or normal idle.

The KSZ9131RNX stops the RX_CLK clock output to the MAC after 10 or more RX_CLK clock cycles have occurred in the receive LPI state to save more power. The Clock-stop enable bit in the PCS Control 1 Register controls if the device stops the RXC clock output.

Figure 4-17 shows the LPI transition for RGMII receive in 100 Mbps mode.

FIGURE 4-17: LPI TRANSITION - RGMII (100 MBPS) RECEIVE



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4.18.3 10BASE-Te MODE

For standard (non-EEE) 10BASE-T mode, normal link pulses (NLPs) with long periods of no AC signal transmission are used to maintain the link during the idle period when there is no traffic activity. To save more power, the device provides the option to enable 10BASE-Te mode, which saves additional power by reducing the transmitted signal amplitude from 2.5V to 1.75V. 10BASE-Te mode is enabled by default and can be disabled by setting the p_cat3 bit in the AFED Control Register in MMD space.

4.18.4 REGISTERS ASSOCIATED WITH EEE

The following MMD registers are provided for EEE configuration and management:

- MMD Address 3h, Register 0h — PCS Control 1 Register
- MMD Address 3h, Register 1h — PCS Status 1 Register
- MMD Address 7h, Register 3Ch — EEE Advertisement Register
- MMD Address 7h, Register 3Dh — EEE Link Partner Ability Register

4.19 Dynamic Channel Quality (DCQ) (TC1)

The KSZ9131RNX provides dynamic channel quality features that include Mean Square Error (MSE), Signal Quality Indicator (SQI), and peak Mean Square Error (pMSE) values. These features are designed to be compliant with Sections 6.1.1, 6.1.2, and 6.1.3 of the *OPEN Alliance TC1 - Advanced diagnostics features for 100BASE-T1 automotive Ethernet PHYs Version 1.0* specification, respectively. These DCQ features are detailed in the following sections:

- Mean Square Error (MSE)
- Signal Quality Indicator (SQI)
- Peak Mean Square Error (pMSE)

MLT-3 modulation is used for data transmission in 100BASE-TX and PAM5 modulation is used for data transmission in 1000BASE-T.

Logically, 100BASE-TX (MLT-3) and 1000BASE-T (PAM5) have signal values of {-1, 0, +1} and {-2, -1, 0, +1, +2}, respectively. These logic levels are mapped to slicer reference levels of {-128, 0, 128} for 100BASE-TX and {-128, -64, 0, 64, 128} for 1000BASE-T. The middle points (the compare thresholds) are {-64, 64} for 100BASE-TX and are {-96, -32, 32, 96} for 1000BASE-T.

Ideally, each receive data sample would be the maximum distance from the compare thresholds, with error values of 0. But because of noise and imperfection in real applications, the sampled data may be off from its ideal. The closer to the compare threshold, the worse the signal quality.

The slicer error is a measurement of how far the processed data off from its ideal location. The largest instantaneous slicer error for 1000BASE-T is +/-32. The largest instantaneous slicer error for 100BASE-TX is +/-64. A higher absolute slicer error means a degraded signal receiving condition.

4.19.1 MEAN SQUARE ERROR (MSE)

This section defines the implementation of section 6.1.1 of the TC1 specification. The KSZ9131RNX can provide detailed information of the dynamic signal quality by means of a MSE value. This mode is enabled by setting the sqi_enable bit in the DCQ Configuration Register. This bit must be set for all DCQ measurements.

With this method, the slicer error is converted into a squared value and then filtered by a programmable low pass filter. This is similar to taking the average of absolute slicer error over a long moving time window. For each data sample, the difference between the absolute slicer error (scaled by x2 (before squaring) for 1000BASE-T) and the current filtered value is added back into the current filtered value.

Note: The sqi_squ_mode_en bit in the DCQ Configuration Register must be set to choose square mode.

The sqi_kp field in the DCQ Configuration Register sets the weighting of the add back as a divide by $2^{\wedge sqi_kp}$, effectively setting the filter bandwidth. As the sqi_kp value is increased, the weighing is decreased, and the mean slicer error value takes a longer time to settle to a stable value. Also as the sqi_kp value is increased, there will be less variation in the mean slicer error value reported.

The scale611 field in the DCQ Configuration Register is used to set a divide by factor (divide by $2^{\wedge scale611)}$ such that the MSE value is linearly scaled to the range of 0 to 511. If the divide by factor is too small, the MSE value is capped at a maximum of 511.

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In order to capture the MSE Value, the DCQ Read Capture bit in the DCQ Configuration Register needs to be written as a high with the desired cable pair specified in the DCQ Channel Number field of the same register. The DCQ Read Capture bit will immediately self-clear and the result will be available in the DCQ Mean Square Error Register. The filtered error value is saved every 1.0 ms (125,000 symbols).

In addition to the current MSE Value, the worst case MSE value since the last read of DCQ Mean Square Error Register is stored in DCQ Mean Square Error Worst Case Register.

4.19.2 SIGNAL QUALITY INDICATOR (SQI)

The KSZ9131RNX provides two SQI methods:

- SQI Method A: TC1 Section 6.1.2 compliant
- SQI Method B: Proprietary method

4.19.2.1 SQI Method A

This section defines the implementation of section 6.1.2 of the TC1 specification. This mode builds upon the Mean Square Error (MSE) method by mapping the MSE value onto a simple quality index. This mode is enabled by setting the sqi_enable bit, in the DCQ Configuration Register.

Note:	As in the Mean Square Error (MSE) method, the sqi_squ_mode_en bit in the DCQ Configuration Register must be set to choose square mode and the scale611 field in the DCQ Configuration Register is used to set the divide by factor (divide by $2^{\wedge scale611)}$ such that the MSE value is linearly scaled to the range of 0 to 511.

The MSE value is compared to the thresholds set in the DCQ SQI Table Registers to provide a SQI value between 0 (worst value) and 7 (best value) as follows:

TABLE 4-13: MSE TO SQI MAPPING

MSE Value		SQI Value
Greater Than	Less Than or Equal To	
	SQI_TBL7.SQI_VALUE	7
SQI_TBL7.SQI_VALUE	SQI_TBL6.SQI_VALUE	6
SQI_TBL6.SQI_VALUE	SQI_TBL5.SQI_VALUE	5
SQI_TBL5.SQI_VALUE	SQI_TBL4.SQI_VALUE	4
SQI_TBL4.SQI_VALUE	SQI_TBL3.SQI_VALUE	3
SQI_TBL3.SQI_VALUE	SQI_TBL2.SQI_VALUE	2
SQI_TBL2.SQI_VALUE	SQI_TBL1.SQI_VALUE	1
SQI_TBL1.SQI_VALUE		0

In order to capture the SQI value, the DCQ Read Capture bit in the DCQ Configuration Register needs to be written as a high with the desired cable pair specified in the DCQ Channel Number field of the same register. The DCQ Read Capture bit will immediately self-clear and the result will be available in the DCQ SQI Register.

In addition to the current SQI the worst case (lowest) SQI since the last read is available in the SQI Worst Case field.

The correlation between the SQI values stored in the DCQ SQI Register and an according signal to noise ratio (SNR) based on AWG noise (bandwidth of 80MHz) is shown in Table 4-14. The bit error rates to be expected in the case of white noise as interference signal is shown in the table as well for information purposes.

A link loss only occurs if the SQI value is 0.

TABLE 4-14: SQI VALUE CORRELATION

SQI Value	SNR Value @ MDI - AWG Noise	Recommended BER for AWG Noise Model
0	< 18 dB	BER>10^-10
1	18 dB <= SNR < 19 dB	
2	19 dB <= SNR < 20 dB	

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TABLE 4-14: SQI VALUE CORRELATION

SQI Value	SNR Value @ MDI - AWG Noise	Recommended BER for AWG Noise Model
3	20 dB <= SNR < 21 dB	BER<10^-10
4	21 dB <= SNR < 22 dB	
5	22 dB <= SNR < 23 dB	
6	23 dB <= SNR < 24 dB	
7	SNR <= 24 dB	

4.19.2.2 SQI Method B

With the SQI Method B, the slicer error is converted into an absolute value and then filtered by a programmable low pass filter. This is similar to taking the average of absolute slicer error over a long moving time window. This mode is enabled by setting the sqi_enable bit, in the DCQ Configuration Register.

For each data sample, the difference between the absolute slicer error (scaled by x2 (before squaring) for 1000BASE-T) and the current filtered value is added back into the current filtered value. The sqi_squ_mode_en bit in the DCQ Configuration Register is used to square the (scaled) slicer error.

The sqi_kp field in the DCQ Configuration Register sets the weighting of the add back as a divide by $2^{\wedge sqi_kp}$, effectively setting the filter bandwidth. As the sqi_kp value is increased, the weighing is decreased, and the mean slicer error value takes a longer time to settle to a stable value. Also as the sqi_kp value is increased, there will be less variation in the mean slicer error value reported.

In order to capture the current error value, the DCQ Read Capture bit in the DCQ Configuration Register needs to be written as a high with the desired cable pair specified in the DCQ Channel Number field of the same register. The DCQ Read Capture bit immediately self-clears and the result is available in the Mean Slicer Error Register. The filtered error value is saved every 1.0 ms (125,000 symbols).

A software based lookup table (derived empirically in lab conditions) may be used to report a SQI number.

4.19.3 PEAK MEAN SQUARE ERROR (PMSE)

This section defines the implementation of section 6.1.3 of the TC1 specification. The peak MSE value is intended to identify transient disturbances which are typically in the microsecond range. This mode is enabled by setting the sqi_enable bit, in the DCQ Configuration Register.

With this method, the slicer error is converted into a squared value and then filtered by a programmable low pass filter. This is similar to taking the average of absolute slicer error over a moving time window.

For each data sample, the difference between the absolute slicer error (scaled by x2 (before squaring) for 1000BASE-T) and the current filtered value is added back into the current filtered value.

Note:	The sqi_squ_mode_en bit in the DCQ Configuration Register must be set to choose square mode.

The sqi_kp3 field in the DCQ Configuration Register sets the weighting of the add back as a divide by $2^{\wedge (sqi_kp3)}$, effectively setting the filter bandwidth. As the sqi_kp3 value is increased, the weighing is decreased, and the mean slicer error value takes a longer time to settle to a stable value.

Every 1.0ms (125,000 symbols), the highest filtered value over that previous 1.0ms period is saved.

The scale613 field in the DCQ Configuration Register is used to set a divide by factor (divide by $2^{\wedge scale613+3)}$ such that the peak MSE value is linearly scaled to the range of 0 to 63. If the divided by factor is too small, the peak MSE value is capped at a maximum of 63.

In order to capture the Peak MSE Value, the DCQ Read Capture bit in the DCQ Configuration Register needs to be written as a high with the desired cable pair specified in the DCQ Channel Number field of the same register. The DCQ Read Capture bit will immediately self-clear and the result will be available in the DCQ Peak MSE Register.

In addition to the current Peak MSE Value the worst case Peak MSE value since the last read of DCQ Peak MSE Register is stored in the same register.

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4.20 Quiet-WIRE® EMI Reduction

Quiet-WIRE® patented technology, delivers fully programmable, integrated noise filtering to reduce Ethernet line emissions without need for additional external BoM components.

Quiet-WIRE® is enabled by setting the Quiet-WIRE Enable bit in MMD31 Register 19. Once the Quiet-WIRE Enable bit is set, the transmit parameters must be configured through the EMITX Control Register and EMITX Coefficient Registers in MMD address space. The values must be set as shown in the default column.

Quiet-WIRE® applies only to 100BASE-TX.

4.21 Wake-On-LAN

Wake-On-LAN (WOL) is normally a MAC-based function to wake up a host system (for example, an Ethernet end device, such as a PC) that is in standby power mode. Wake-up is triggered by receiving and detecting a special packet (commonly referred to as the “magic packet”) that is sent by the remote link partner. The KSZ9131RNX can perform the same WOL function if the MAC address of its associated MAC device is entered into the KSZ9131RNX PHY registers for magic-packet detection. When the KSZ9131RNX detects the magic packet, it wakes up the host by driving its power management event (PME) output pin low.

By default, the WOL function is disabled. It is enabled by setting the enabling bit and configuring the associated registers for the selected PME wake-up detection method.

The KSZ9131RNX provides three methods to trigger a PME wake-up:

- Magic-packet detection
- Customized-packet detection
- Link status change detection

4.21.1 MAGIC-PACKET DETECTION

The magic packet’s frame format starts with 6 bytes of 0xFFh and is followed by 16 repetitions of the MAC address of its associated MAC device (local MAC device).

When the magic packet is detected from its link partner, the KSZ9131RNX asserts its PME output pin low.

The following MMD registers are provided for magic-packet detection:

- Magic-packet detection is enabled by writing a ‘1’ to the Enable Magic Packet Detection Wake Event bit of the Wake-On-LAN Control Register
- The MAC address (for the local MAC device) is written to and stored in the Wake-On-LAN-MAC-LO Register, Wake-On-LAN-MAC-MI Register, and Wake-On-LAN-MAC-HI Register

The KSZ9131RNX does not generate the magic packet. The magic packet must be provided by the external system. Magic packet detection status can be read from the Wake-on-LAN Magic Packet Receive Status Register.

4.21.2 CUSTOMIZED-PACKET DETECTION

The customized packet has associated register/bit masks to select which byte, or bytes, of the first 64 bytes of the packet to use in the CRC calculation. After the KSZ9131RNX receives the packet from its link partner, the selected bytes for the received packet are used to calculate the CRC. The calculated CRC is compared to the expected CRC value that was previously written to and stored in the KSZ9131RNX PHY registers. If there is a match, the KSZ9131RNX asserts its PME output pin low.

Four customized packets are provided to support four types of wake-up scenarios. A dedicated set of registers is used to configure and enable each customized packet.

The following MMD registers are provided for customized-packet detection:

- Each of the four customized packets is enabled via the Enable Customized Frame Filter Wake Event field of the Wake-On-LAN Control Register,
  - Bit [2] // For customized packets, type 0
  - Bit [3] // For customized packets, type 1
  - Bit [4] // For customized packets, type 2
  - Bit [5] // For customized packets, type 3
- 32-bit expected CRCs are written to and stored in:
  - Customized-Pkt-0-CRC-LO Register and Customized-Pkt-0-CRC-HI Register (Type 0 customized packets)

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  - Customized-Pkt-1-CRC-LO Register and Customized-Pkt-1-CRC-HI Register (Type 1 customized packets)
  - Customized-Pkt-2-CRC-LO Register and Customized-Pkt-2-CRC-HI Register (Type 2 customized packets)
  - Customized-Pkt-3-CRC-LO Register and Customized-Pkt-3-CRC-HI Register (Type 3 customized packets)
- Masks to indicate which of the first 64-bytes to use in the CRC calculation are set in:
  - Customized-Pkt-0-MASK_LL Register, Customized-Pkt-0-MASK_LH Register, Customized-Pkt-0-MASK_HL Register, and Customized-Pkt-0-MASK_HH Register (Type 0 customized packets)
  - Customized-Pkt-1-MASK_LL Register, Customized-Pkt-1-MASK_LH Register, Customized-Pkt-1-MASK_HL Register, and Customized-Pkt-1-MASK_HH Register (Type 1 customized packets)
  - Customized-Pkt-2-MASK_LL Register, Customized-Pkt-2-MASK_LH Register, Customized-Pkt-2-MASK_HL Register, and Customized-Pkt-2-MASK_HH Register (Type 2 customized packets)
  - Customized-Pkt-3-MASK_LL Register, Customized-Pkt-3-MASK_LH Register, Customized-Pkt-3-MASK_HL Register, and Customized-Pkt-3-MASK_HH Register (Type 3 customized packets)

4.21.3 LINK STATUS CHANGE DETECTION

If link status change detection is enabled, the KSZ9131RNX asserts its PME output pin low whenever there is a link status change using the following bits in the Wake-On-LAN Control Register:

- Enable Link Up Wake Event // For link-up detection
- Enable Link Down Wake Event // For link-down detection

The link change status can be read from the Interrupt Control/Status Register.

4.21.4 PME OUTPUT SIGNAL

The PME output signal is available on either LED1 as PME_N1 or INT_N as PME_N2, and is selected and enabled using the rgmii_pme_on_led1_mode and rgmii_pme_on_int_mode fields in the Operation Mode Strap Override Register.

Additionally, the PME Output Select field in the Wake-On-LAN Control Register defines the output functions for PME_N1 and PME_N2.

When asserted, the PME output is cleared by disabling the register bit that enabled the PME trigger source (magic packet, customized packet, link status change).

The PME output is active low.

Note:	When mapped to INT_N, the polarity can be inverted by use of the Interrupt Polarity Invert bit in the Control Register.

APPLICATION NOTE: When mapped to LED1, Enhanced LED mode must be disabled.

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5.0 REGISTER DESCRIPTIONS

This chapter describes the various control and status registers (CSRs).

Note: RESERVED address space must not be written under any circumstances. Failure to heed this warning may result in untoward operation and unexpected results.

5.1 Register Map

The register space within the KSZ9131RNX consists of two distinct areas.

- Standard Registers (Direct register access)
- MDIO Manageable Device (MMD) Registers (Indirect register access)

The KSZ9131RNX supports the following standard registers.

TABLE 5-1: STANDARD REGISTERS

Index (in decimal)	Index (in hex)	Register Name
IEEE-Defined Registers		
0	0	Basic Control Register
1	1	Basic Status Register
2	2	Device Identifier 1 Register
3	3	Device Identifier 2 Register
4	4	Auto-Negotiation Advertisement Register
5	5	Auto-Negotiation Link Partner Base Page Ability Register
6	6	Auto-Negotiation Expansion Register
7	7	Auto-Negotiation Next Page TX Register
8	8	Auto-Negotiation Next Page RX Register
9	9	Auto-Negotiation Master Slave Control Register
10	Ah	Auto-Negotiation Master Slave Status Register
11-12	Bh-Ch	RESERVED
13	Dh	MMD Access Control Register
14	Eh	MMD Access Address/Data Register
15	Fh	Extended Status Register
Vendor-Specific Registers		
16	10h	RESERVED
17	11h	Remote Loopback Register
18	12h	LinkMD Cable Diagnostic Register
19	13h	Digital PMA/PCS Status Register
20	14h	RESERVED
21	15h	RXER Counter Register
22	16h	LED Mode Select Register
23	17h	LED Behavior Register
24	18h	RESERVED
25	19h	MDIO Drive Register
26	1Ah	KSZ9031 LED Mode Register
27	1Bh	Interrupt Control/Status Register
28	1Ch	Auto-MDI/MDI-X Register
29	1Dh	Software Power Down Control Register
30	1Eh	External Loopback Register
31	1Fh	Control Register

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The device supports the following MMD device addresses and their associated register addresses, which make up the indirect MMD registers.

TABLE 5-2: MMD CONTROL AND STATUS REGISTERS MAP

MMD Device Address (in decimal)	Index (in decimal)	Index (in hex)	Register Name
1	225	E1h	Mean Slicer Error Register
	226	E2h	DCQ Mean Square Error Register
	227	E3h	DCQ Mean Square Error Worst Case Register
	228	E4h	DCQ SQI Register
	229	E5h	DCQ Peak MSE Register
	230	E6h	DCQ Control Register
	231	E7h	DCQ Configuration Register
	232-238	E8h-EEh	DCQ SQI Table Registers
2	0	0h	Common Control Register
	1	1h	Strap Status Register
	2	2h	Operation Mode Strap Override Register
	3	3h	Operation Mode Strap Register
	4	4h	Clock Invert and Control Signal Pad Skew Register
	5	5h	RGMII RX Data Pad Skew Register
	6	6h	RGMII TX Data Pad Skew Register
	7	7h	RESERVED
	8	8	Clock Pad Skew Register
	9	9	Self-Test Packet Count LO Register
	10	Ah	Self-Test Packet Count HI Register
	11	Bh	Self-Test Status Register
	12	Ch	Self-Test Frame Count Enable Register
	13	Dh	Self-Test PGEN Enable Register
	14	Eh	Self-Test Enable Register
	15	Fh	RESERVED
	16	10h	Wake-On-LAN Control Register
	17	11h	Wake-On-LAN-MAC-LO Register
	18	12h	Wake-On-LAN-MAC-MI Register
	19	13h	Wake-On-LAN-MAC-HI Register
	20	14h	Customized-Pkt-0-CRC-LO Register
	21	15h	Customized-Pkt-0-CRC-HI Register
	22	16h	Customized-Pkt-1-CRC-LO Register
	23	17h	Customized-Pkt-1-CRC-HI Register
	24	18h	Customized-Pkt-2-CRC-LO Register
	25	19h	Customized-Pkt-2-CRC-HI Register
	26	1Ah	Customized-Pkt-3-CRC-LO Register
	27	1Bh	Customized-Pkt-3-CRC-HI Register
	28	1Ch	Customized-Pkt-0-MASK_LL Register
	29	1Dh	Customized-Pkt-0-MASK_LH Register
	30	1Eh	Customized-Pkt-0-MASK_HL Register
	31	1Fh	Customized-Pkt-0-MASK_HH Register
	32	20h	Customized-Pkt-1-MASK_LL Register
	33	21h	Customized-Pkt-1-MASK_LH Register

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TABLE 5-2: MMD CONTROL AND STATUS REGISTERS MAP (CONTINUED)

MMD Device Address (in decimal)	Index (in decimal)	Index (in hex)	Register Name
2 (cont.)	34	22h	Customized-Pkt-1-MASK_HL Register
	35	23h	Customized-Pkt-1-MASK_HH Register
	36	24h	Customized-Pkt-2-MASK_LL Register
	37	25h	Customized-Pkt-2-MASK_LH Register
	38	26h	Customized-Pkt-2-MASK_HL Register
	39	27h	Customized-Pkt-2-MASK_HH Register
	40	28h	Customized-Pkt-3-MASK_LL Register
	41	29h	Customized-Pkt-3-MASK_LH Register
	42	2Ah	Customized-Pkt-3-MASK_HL Register
	43	2Bh	Customized-Pkt-3-MASK_HH Register
	44	2Ch	Wake-on-LAN Control Status Register
	45	2Dh	Wake-on-LAN Custom Packet Receive Status Register
	46	2Eh	Wake-on-LAN Magic Packet Receive Status Register
	47	2Fh	Wake-on-LAN Data Module Status Register
	48	30h	Customized Pkt-0 Received CRC-L Register
	49	31h	Customized Pkt-0 Received CRC-H Register
	50	32h	Customized Pkt-1 Received CRC-L Register
	51	33h	Customized Pkt-1 Received CRC-H Register
	52	34h	Customized Pkt-2 Received CRC-L Register
	53	35h	Customized Pkt-2 Received CRC-H Register
	54	36h	Customized Pkt-3 Received CRC-L Register
	55	37h	Customized Pkt-3 Received CRC-H Register
	56-59	38h-3B	RESERVED
	60	3Ch	Self-Test Correct Count LO Register
	61	3Dh	Self-Test Correct Count HI Register
	62	3Eh	Self-Test Error Count LO Register
	63	3Fh	Self-Test Error Count HI Register
	64	40h	Self-Test Bad SFD Count LO Register
	65	41h	Self-Test Bad SFD Count HI Register
	66-75	42h-4Bh	RESERVED
	76	4Ch	RX DLL Control Register
	77	4Dh	TX DLL Control Register

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TABLE 5-2: MMD CONTROL AND STATUS REGISTERS MAP (CONTINUED)

MMD Device Address (in decimal)	Index (in decimal)	Index (in hex)	Register Name
3	0	0	PCS Control 1 Register
	1	1	PCS Status 1 Register
	8	8	EEE Quiet Timer Register
	9	9	EEE Update Timer Register
	10	Ah	EEE Link-Fail Timer Register
	11	Bh	EEE Post-Update Timer Register
	12	Ch	EEE WaitWQ Timer Register
	13	Dh	EEE Wake Timer Register
	14	Eh	EEE WakeTX Timer Register
	15	Fh	EEE WakeMz Timer Register
	16	10h	RESERVED
	20	14h	EEE Control and Capability Register
	22	16h	EEE Wake Error Counter Register
	24	18h	EEE 100 Timer-0 Register
	25	19h	EEE 100 Timer-1 Register
	26	1Ah	EEE 100 Timer-2 Register
	27	1Bh	EEE 100 Timer-3 Register
7	60	3Ch	EEE Advertisement Register
	61	3Dh	EEE Link Partner Ability Register
	62	3Eh	EEE Link Partner Ability Override Register
	63	3Fh	EEE Message Code Register
28 (1Ch)	1	1h	XTAL Control Register
	2-8	2h-8h	RESERVED
	9	9h	AFED Control Register
	10-13	Ah-Dh	RESERVED
	14	Eh	LDO Control Register
	15-35	Fh-23h	RESERVED
	36	24h	EDPD Control Register
	37	25h	EMITX Control Register
	38-52	26h-34h	EMITX Coefficient Registers
31 (1Fh)	19	13h	MMD31 Register 19

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5.2 Standard Registers

Standard registers provide direct read/write access to a 32-register address space, as defined in Clause 22 of the IEEE 802.3 Specification. Within this address space, the first 16 registers (Registers 0 to 15 (Fh)) are defined according to the IEEE specification, while the remaining 16 registers (Registers 16 (10h) to 31 (1Fh)) are defined specific to the PHY vendor.

5.2.1 BASIC CONTROL REGISTER

Index (In Decimal): 0 Size: 16 bits

This read/write register is used to configure the PHY.

Bits	Description	Type	Default
15	**PHY Soft Reset (RESET)** When set, this bit resets all the PHY and all its registers to their default state. This bit is self clearing. 1 = PHY software reset.	R/W1S/ SC	0b
14	**Loopback (PHY_LOOPBACK)** This bit enables/disables the loopback mode. When enabled, transmissions are not sent to network. Instead, they are looped back into the PHY. 0 = Loopback mode disabled (normal operation) 1 = Loopback mode enabled	R/W	0b
13	**Speed Select[0]** Together with Speed Select[1], sets speed per the following table: [Speed Select1][Speed Select0] 00 = 10Mbps 01 = 100Mbps 10 = 1000Mbps 11 = Reserved **Note:** Ignored if the Auto-Negotiation Enable bit of this register is 1.	R/W	0b
12	**Auto-Negotiation Enable** This bit enables/disables Auto-Negotiation. 0 = disable auto-negotiate process 1 = enable auto-negotiate process (overrides the Speed Select[0], Speed Select[1] and Duplex Mode bits of this register)	R/W	1b
11	**Power Down** This bit controls the power down mode of the PHY. 0 = Normal operation 1 = General power down mode	R/W	0b
10	**Isolate (PHY_ISO)** This bit controls the isolation of the PHY from the MII interface. 0 = Non-Isolated (Normal operation) 1 = Isolated	R/W	0b

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Bits	Description	Type	Default
9	**Restart Auto-Negotiation (PHY_RST_AN)** When set, this bit restarts the Auto-Negotiation process. This bit is self clearing. 1 = Auto-Negotiation restarted	R/W1S/ SC	0b
8	**Duplex Mode** This bit is used to set the duplex. 0 = Half Duplex 1 = Full Duplex **Note:** Ignored if the Auto-Negotiation Enable bit of this register is 1.	R/W	1b
7	**Collision Test Mode (PHY_COL_TEST)** This bit enables/disables the collision test mode of the PHY. When set, the collision signal is active during transmission. It is recommended that this feature be used only in loopback mode. 0 = Collision test mode disabled 1 = Collision test mode enabled	R/W	0b
6	**Speed Select[1]** See description for Speed Select[0] for details.	R/W	1b
5:0	**RESERVED**	R/W	-

5.2.2 BASIC STATUS REGISTER

Index (In Decimal): 1 Size: 16 bits

This register is used to monitor the status of the PHY.

Bits	Description	Type	Default
15	**100BASE-T4** This bit displays the status of 100BASE-T4 compatibility. 0 = PHY not able to perform 100BASE-T4 1 = PHY able to perform 100BASE-T4	RO	0b
14	**100BASE-X Full Duplex** This bit displays the status of 100BASE-X full duplex compatibility. 0 = PHY not able to perform 100BASE-X full duplex 1 = PHY able to perform 100BASE-X full duplex	RO	1b
13	**100BASE-X Half Duplex** This bit displays the status of 100BASE-X half duplex compatibility. 0 = PHY not able to perform 100BASE-X half duplex 1 = PHY able to perform 100BASE-X half duplex	RO	1b

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Bits	Description	Type	Default
12	**10BASE-T Full Duplex** This bit displays the status of 10BASE-T full duplex compatibility. 0 = PHY not able to perform 10BASE-T full duplex 1 = PHY able to perform 10BASE-T full duplex	RO	1b
11	**10BASE-T Half Duplex** This bit displays the status of 10BASE-T half duplex compatibility. 0 = PHY not able to perform 10BASE-T half duplex 1 = PHY able to perform 10BASE-T half duplex	RO	1b
10	**100BASE-T2 Full Duplex** This bit displays the status of 100BASE-T2 full duplex compatibility. 0 = PHY not able to perform 100BASE-T2 full duplex 1 = PHY able to perform 100BASE-T2 full duplex	RO	0b
9	**100BASE-T2 Half Duplex** This bit displays the status of 100BASE-T2 half duplex compatibility. 0 = PHY not able to perform 100BASE-T2 half duplex 1 = PHY able to perform 100BASE-T2 half duplex	RO	0b
8	**Extended Status** This bit displays whether extended status information is in register 15 (per IEEE 802.3 clause 22.2.4). 0 = No extended status information in Register 15 1 = Extended status information in Register 15	RO	1b
7	**Unidirectional Ability** This bit indicates whether the PHY is able to transmit regardless of whether the PHY has determined that a valid link has been established. 0 = Can only transmit when a valid link has been established 1 = Can transmit regardless	RO	0b
6	**MF Preamble Suppression** This bit indicates whether the PHY accepts management frames with the preamble suppressed. 0 = Management frames with preamble suppressed not accepted 1 = Management frames with preamble suppressed accepted	RO	1b
5	**Auto-Negotiation Complete** This bit indicates the status of the Auto-Negotiation process. 0 = Auto-Negotiation process not completed 1 = Auto-Negotiation process completed	RO	0b
4	**Remote Fault** This bit indicates if a remote fault condition has been detected. 0 = No remote fault condition detected 1 = Remote fault condition detected	RO/LH	0b

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Bits	Description	Type	Default
3	**Auto-Negotiation Ability** This bit indicates the PHY's Auto-Negotiation ability. 0 = PHY is unable to perform Auto-Negotiation 1 = PHY is able to perform Auto-Negotiation	RO	1b
2	**Link Status** This bit indicates the status of the link. 0 = Link is down 1 = Link is up	RO/LL	0b
1	**Jabber Detect** This bit indicates the status of the jabber condition. 0 = No jabber condition detected 1 = Jabber condition detected	RO/LH	0b
0	**Extended Capability** This bit indicates whether extended register capability is supported. 0 = Basic register set capabilities only 1 = Extended register set capabilities	RO	1b

5.2.3 DEVICE IDENTIFIER 1 REGISTER

Index (In Decimal): 2 Size: 16 bits

This register contains the MSB of the Organizationally Unique Identifier (OUI) for the PHY. The LSB of the PHY OUI is contained in the Device Identifier 2 Register.

Bits	Description	Type	Default
15:0	**PHY ID Number** Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively.	RO	0022h

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5.2.4 DEVICE IDENTIFIER 2 REGISTER

Index (In Decimal): 3 Size: 16 bits

This register contains the LSB of the Organizationally Unique Identifier (OUI) for the PHY. The MSB of the PHY OUI is contained in the Device Identifier 1 Register.

Bits	Description	Type	Default
15:10	**PHY ID Number** Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI), respectively.	RO	000101b
9:4	**Model Number** Six-bit manufacturer's model number.	RO	100100b
3:0	**Revision Number** Four-bit manufacturer's revision number.	RO	Note 5-1

Note 5-1 The default value of the Revision Number field varies dependent on the silicon revision number.

Note: The hexadecimal equivalent of this register is 1640h (A0) or 1641h (B0).

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5.2.5 AUTO-NEGOTIATION ADVERTISEMENT REGISTER

Index (In Decimal): 4 Size: 16 bits

This read/write register contains the advertised ability of the PHY and is used in the Auto-Negotiation process with the link partner.

Bits	Description	Type	Default
15	**Next Page** 0 = No next page ability 1 = Next page capable	R/W	0b
14	**RESERVED**	RO	-
13	**Remote Fault** This bit determines if remote fault indication will be advertised to the link partner. 0 = Remote fault indication not advertised 1 = Remote fault indication advertised	R/W	0b
12	**Extended Next Page** **Note:** This bit should be written as 0.	R/W	0b
11	**Asymmetric Pause** This bit determines the advertised asymmetric pause capability. 0 = No Asymmetric PAUSE toward link partner advertised 1 = Asymmetric PAUSE toward link partner advertised	R/W	1b
10	**Symmetric Pause** This bit determines the advertised symmetric pause capability. 0 = No Symmetric PAUSE toward link partner advertised 1 = Symmetric PAUSE toward link partner advertised	R/W	1b
9	**100BASE-T4** 0 = no T4 ability 1 = T4 able **Note:** The device does not support this mode and this bit should always be written as a 0.	R/W	0
8	**100BASE-X Full Duplex** This bit determines the advertised 100BASE-X full duplex capability. 0 = 100BASE-X full duplex ability not advertised 1 = 100BASE-X full duplex ability advertised	R/W	Note 5-2
7	**100BASE-X Half Duplex** This bit determines the advertised 100BASE-X half duplex capability. 0 = 100BASE-X half duplex ability not advertised 1 = 100BASE-X half duplex ability advertised	R/W	Note 5-2

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Bits	Description	Type	Default
6	**10BASE-T Full Duplex** This bit determines the advertised 10BASE-T full duplex capability. 0 = 10BASE-T full duplex ability not advertised 1 = 10BASE-T full duplex ability advertised	R/W	Note 5-2
5	**10BASE-T Half Duplex** This bit determines the advertised 10BASE-T half duplex capability. 0 = 10BASE-T half duplex ability not advertised 1 = 10BASE-T half duplex ability advertised	R/W	Note 5-2
4:0	**Selector Field** This field identifies the type of message being sent by Auto-Negotiation. 00001 = IEEE 802.3	R/W	00001b

Note 5-2 Set by the MODE[3:0] strapping pins. Refer to Section 3.3, "Configuration Straps" for details.

5.2.6 AUTO-NEGOTIATION LINK PARTNER BASE PAGE ABILITY REGISTER

Index (In Decimal): 5 Size: 16 bits

This read-only register contains the advertised ability of the link partner's PHY and is used in the Auto-Negotiation process between the link partner and the PHY.

Bits	Description	Type	Default
15	**Next Page** This bit indicates the link partner PHY page capability. 0 = Link partner PHY does not advertise next page capability 1 = Link partner PHY advertises next page capability	RO	0b
14	**Acknowledge** This bit indicates whether the link code word has been received from the partner. 0 = Link code word not yet received from partner 1 = Link code word received from partner	RO	0b
13	**Remote Fault** This bit indicates whether a remote fault has been detected. 0 = No remote fault 1 = Remote fault detected	RO	0b
12	**Extended Next Page** 0 = Link partner PHY does not advertise extended next page capability 1 = Link partner PHY advertises extended next page capability	RO	0b

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Bits	Description	Type	Default
11	**Asymmetric Pause** This bit indicates the link partner PHY asymmetric pause capability. 0 = No Asymmetric PAUSE toward link partner 1 = Asymmetric PAUSE toward link partner	RO	0b
10	**Pause** This bit indicates the link partner PHY symmetric pause capability. 0 = No Symmetric PAUSE toward link partner 1 = Symmetric PAUSE toward link partner	RO	0b
9	**100BASE-T4** This bit indicates the link partner PHY 100BASE-T4 capability. 0 = 100BASE-T4 ability not supported 1 = 100BASE-T4 ability supported	RO	0b
8	**100BASE-X Full Duplex** This bit indicates the link partner PHY 100BASE-X full duplex capability. 0 = 100BASE-X full duplex ability not supported 1 = 100BASE-X full duplex ability supported	RO	0b
7	**100BASE-X Half Duplex** This bit indicates the link partner PHY 100BASE-X half duplex capability. 0 = 100BASE-X half duplex ability not supported 1 = 100BASE-X half duplex ability supported	RO	0b
6	**10BASE-T Full Duplex** This bit indicates the link partner PHY 10BASE-T full duplex capability. 0 = 10BASE-T full duplex ability not supported 1 = 10BASE-T full duplex ability supported	RO	0b
5	**10BASE-T Half Duplex** This bit indicates the link partner PHY 10BASE-T half duplex capability. 0 = 10BASE-T half duplex ability not supported 1 = 10BASE-T half duplex ability supported	RO	0b
4:0	**Selector Field** This field identifies the type of message being sent by Auto-Negotiation. 00001 = IEEE 802.3	RO	00000b

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5.2.7 AUTO-NEGOTIATION EXPANSION REGISTER

Index (In Decimal): 6 Size: 16 bits

This read/write register is used in the Auto-Negotiation process between the link partner and the PHY.

Bits	Description	Type	Default
15:7	**RESERVED**	RO	-
6	**Receive Next Page Location Able** 0 = Received next page storage location is not specified by bit 6.5 1 = Received next page storage location is specified by bit 6.5	RO	1b
5	**Received Next Page Storage Location** 0 = Link partner next pages are stored in the Auto-Negotiation Link Partner Base Page Ability Register (PHY register 5) 1 = Link partner next pages are stored in the Auto-Negotiation Next Page RX Register (PHY register 8)	RO	1b
4	**Parallel Detection Fault** This bit indicates whether a Parallel Detection Fault has been detected. 0 = A fault hasn't been detected via the Parallel Detection function 1 = A fault has been detected via the Parallel Detection function	RO/LH	0b
3	**Link Partner Next Page Able** This bit indicates whether the link partner has next page ability. 0 = Link partner does not contain next page capability 1 = Link partner contains next page capability	RO	0b
2	**Next Page Able** This bit indicates whether the local device has next page ability. 0 = Local device does not contain next page capability 1 = Local device contains next page capability	RO	1b
1	**Page Received** This bit indicates the reception of a new page. 0 = A new page has not been received 1 = A new page has been received	RO/LH	0b
0	**Link Partner Auto-Negotiation Able** This bit indicates the Auto-Negotiation ability of the link partner. 0 = Link partner is not Auto-Negotiation able 1 = Link partner is Auto-Negotiation able	RO	0b

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5.2.8 AUTO-NEGOTIATION NEXT PAGE TX REGISTER

Index (In Decimal): 7 Size: 16 bits

Bits	Description	Type	Default
15	**Next Page** 0 = No next page ability 1 = Next page capable	R/W	0b
14	**RESERVED**	RO	-
13	**Message Page** 0 = Unformatted page 1 = Message page	R/W	1b
12	**Acknowledge 2** 0 = Device cannot comply with message. 1 = Device will comply with message.	R/W	0b
11	**Toggle** 0 = Previous value was HIGH. 1 = Previous value was LOW.	RO	0b
10:0	**Message Code** Message/Unformatted Code Field	R/W	000 0000 0001b

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5.2.9 AUTO-NEGOTIATION NEXT PAGE RX REGISTER

Index (In Decimal): 8 Size: 16 bits

Bits	Description	Type	Default
15	**Next Page** 0 = No next page ability 1 = Next page capable	RO	0b
14	**Acknowledge** This bit indicates whether the link code word has been received from the partner. 0 = Link code word not yet received from partner 1 = Link code word received from partner	RO	0
13	**Message Page** 0 = Unformatted page 1 = Message page	RO	0b
12	**Acknowledge 2** 0 = Device cannot comply with message. 1 = Device will comply with message.	RO	0b
11	**Toggle** 0 = Previous value was HIGH. 1 = Previous value was LOW.	RO	0b
10:0	**Message Code** Message/Unformatted Code Field	RO	000 0000 0000b

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5.2.10 AUTO-NEGOTIATION MASTER SLAVE CONTROL REGISTER

Index (In Decimal): 9 Size: 16 bits

Bits	Description	Type	Default
15:13	**Test Mode** IEEE 802.3 clause 40.6.1.1.2 transmitter test mode. 000 = Normal mode 001 = Test Mode 1 - Transmit waveform test 010 = Test Mode 2 - Transmit jitter test in Master mode 011 = Test Mode 3 - Transmit jitter test in Slave mode 100 = Test Mode 4 - Transmitter distortion test 101 = Reserved 110 = Reserved 111 = Reserved	R/W	000b
12	**Master/Slave Manual Configuration Enable** 0 = disable MASTER-SLAVE manual configuration value 1 = enable MASTER-SLAVE manual configuration value	R/W	0b
11	**Master/Slave Manual Configuration Value** Active only when the Master/Slave Manual Configuration Enable bit of this register is 1. 0 = Configure PHY as slave 1 = Configure PHY as master	R/W	0b
10	**Port Type** 0 = single-port device 1 = multi-port device	R/W	0b
9	**1000BASE-T Full Duplex** 0 = advertise PHY is not 1000BASE-T full duplex capable 1 = advertise PHY is 1000BASE-T full duplex capable	R/W	1b
8	**1000BASE-T Half Duplex** 0 = advertise PHY is not 1000BASE-T half duplex capable 1 = advertise PHY is 1000BASE-T half duplex capable **Note:** The device does not support this mode and this bit should always be written as a 0.	R/W	0b
7:0	**RESERVED**	RO	-

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5.2.11 AUTO-NEGOTIATION MASTER SLAVE STATUS REGISTER

Index (In Decimal): 10 Size: 16 bits

Bits	Description	Type	Default
15	**Master/Slave Configuration Fault** 0 = No MASTER-SLAVE configuration fault detected 1 = MASTER-SLAVE configuration fault detected	RO/LH	0b
14	**Master/Slave Configuration Resolution** 0 = Local PHY configuration resolved to SLAVE 1 = Local PHY configuration resolved to MASTER	RO	0b
13	**Local 1000BASE-T Receiver Status** 0 = Local Receiver not OK 1 = Local Receiver OK	RO	0b
12	**Remote (Link Partner) Receiver Status** 0 = Remote Receiver not OK 1 = Remote Receiver OK	RO	0b
11	**Link Partner Advertised 1000BASE-T Full Duplex Capability** 0 = Link Partner is not capable of 1000BASE-T full duplex 1 = Link Partner is capable of 1000BASE-T full duplex	RO	0b
10	**Link Partner Advertised 1000BASE-T Half Duplex Capability** 0 = Link Partner is not capable of 1000BASE-T half duplex 1 = Link Partner is capable of 1000BASE-T half duplex	RO	0b
9:8	**RESERVED**	RO	-
7:0	**1000BASE-T Idle Error Count** Cumulative count of the errors detected when the receiver is receiving idles. **Note:** This counter halts at a value of 0xFF.	RO/RC	00h

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5.2.12 MMD ACCESS CONTROL REGISTER

Index (In Decimal): 13 Size: 16 bits

Bits	Description	Type	Default
15:14	**MMD Function** This field is used to select the desired MMD function: 00 = Address 01 = Data, no post increment 10 = Data, post increment on reads and writes 11 = Data, post increment on writes only	R/W	00b
13:5	**RESERVED**	RO	-
4:0	**MMD Device Address (DEVAD)** This field is used to select the desired MMD device address.	R/W	00000b

5.2.13 MMD ACCESS ADDRESS/DATA REGISTER

Index (In Decimal): 14 Size: 16 bits

Bits	Description	Type	Default
15:0	**MMD Register Address/Data** If the MMD Function field of the MMD Access Control Register is “00”, this field is used to indicate the MMD register address to read/write of the device specified in the MMD Device Address (DEVAD) field. Otherwise, this register is used to read/write data from/to the previously specified MMD address.	R/W	0000h

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5.2.14 EXTENDED STATUS REGISTER

Index (In Decimal): 15 Size: 16 bits

This register is used to monitor the status of the PHY.

Bits	Description	Type	Default
15	**1000BASE-X Full Duplex** This bit displays the status of 1000BASE-X full duplex compatibility. 0 = PHY not able to perform 1000BASE-X full duplex 1 = PHY able to perform 1000BASE-X full duplex	RO	0b
14	**1000BASE-X Half Duplex** This bit displays the status of 1000BASE-X half duplex compatibility. 0 = PHY not able to perform 1000BASE-X half duplex 1 = PHY able to perform 1000BASE-X half duplex	RO	0b
13	**1000BASE-T Full Duplex** This bit displays the status of 1000BASE-T full duplex compatibility. 0 = PHY not able to perform 1000BASE-T full duplex 1 = PHY able to perform 1000BASE-T full duplex	RO	1b
12	**1000BASE-T Half Duplex** This bit displays the status of 1000BASE-T half duplex compatibility. 0 = PHY not able to perform 1000BASE-T half duplex 1 = PHY able to perform 1000BASE-T half duplex	RO	0b
11:0	**RESERVED**	RO	-

5.2.15 REMOTE LOOPBACK REGISTER

Index (In Decimal): 17 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	-
8	**Remote Loopback** 1 = Enable remote loopback 0 = Disable remote loopback	R/W	0b
7:0	**RESERVED**	RO	-

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5.2.16 LINKMD CABLE DIAGNOSTIC REGISTER

Index (In Decimal): 18 Size: 16 bits

Bits	Description	Type	Default
15	**Cable Diagnostics Test Enable (VCT_EN)** Writing a 1 enables the test. This bit is self-cleared when the test is complete. Writing a 0 will disable the test. Reading a 0 indicates the cable diagnostic test is completed and the status information is valid. Reading a 1 indicates the cable diagnostic test is in progress and the status information is NOT valid.	R/W/SC	0b
14	**Cable Diagnostic Disable Transmitter (VCT_DIS_TX)** [0] = The transmitter is enabled to start cable diagnostic. [1] = The transmitter is disabled and cable diagnostic is on hold to break down the link.	R/W	0b
13:12	**Cable Diagnostics Test Pair (VCT_PAIR[1:0])** This field defines which channel to be tested. 00 = Pair A 01 = Pair B 10 = Pair C 11 = Pair D	R/W	00b
11:10	**Bit[9:0] Definition (VCT_SEL[1:0])** Defines the meaning of bit[9:0] as: 00 = bit[9:0] is VCT result, i.e., VCT_ST[1:0] and VCT_DATA[7:0]. 01 = bit[9:0] is the threshold for generating high pulse from ADC2VCT[8:0]. Default value is 64. 10 = bit[9:0] is the threshold for generating low pulse from ADC2VCT[8:0]. Default value is -64. 11 = Reserved.	R/W	00b
9:8	**Cable Diagnostics Status (VCT_ST[1:0])** When VCT_SEL= 00, this is the status of cable diagnostics. Valid only when VCT_EN = 0. 00 = Normal, no fault has been detected 01 = Open Fault has been detected 10 = Short Fault has been detected 11 = Cable diagnostic test failed When VCT_SEL!= 00, see details in VCT_SEL.	RO	00b

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Bits	Description	Type	Default
7:0	**Cable Diagnostics Data or Threshold (VCT_DATA[7:0])** When VCT_SEL!= 00, see details in VCT_SEL. When VCT_SEL = 00, this is the data of cable diagnostics. Valid only when VCT_EN = 0. (1) If cable is normal, i.e., VCT_ST = 00, VCT_DATA don't care. (2) If cable is open or short, i.e., VCT_ST = 01 or 10, the distance to fault is approximately 0.8 * (VCT_DATA - 22) (Meters) (see Section 4.14) (3) If cable diagnostics failed, i.e., VCT_ST = 11, Bit[7] = 1 means invalid reflected pulse width, i.e. equal or greater than 152ns, equal or less than 48ns. Bit[6] = 1 means cable has signal for too long time during WAIT state. It's unusual and for debug only. Bit[5] = 1 means mask100 detected and no silent time window can be found for diagnostics. It means high frequency signal is found on the line. The link partner probably is in forced 100BT or 1000BT mode. Bit[4] = 1 means signals faster than NLP and FLP exists and no silent time window can be found for diagnostics. It's unusual and for debug only. Bit[3:2] = number of low pulses detected. If more than 3, stay at 3. Bit[1:0] = number of high pulses detected. If more than 3, stay at 3.	RO	00h

5.2.17 DIGITAL PMA/PCS STATUS REGISTER

Index (In Decimal): 19 Size: 16 bits

Bits	Description	Type	Default
15:2	**RESERVED**	RO	-
1	**1000BT link status** 1000 BT link status 1 = link status OK 0 = link status not OK	RO	0b
0	**100BT link status** 100 BT link status 1 = link status OK 0 = link status not OK	RO	0b

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5.2.18 RXER COUNTER REGISTER

Index (In Decimal): 21 Size: 16 bits

Bits	Description	Type	Default
15:0	**RXER Counter** RX Error counter for the RX_ER signal **Note:** This counter halts at a value of 0xFFFF.	RC	0000h

5.2.19 LED MODE SELECT REGISTER

Index (In Decimal): 22 Size: 16 bits

This register selects the operating mode of the PHY LEDs when in extended mode. This register is only used when the KSZ9031 LED Mode bit in the KSZ9031 LED Mode Register is clear.

Bits	Description	Type	Default
15:8	**RESERVED**	R/W	-
7:4	**LED2 Configuration** This field configures the LED2 pin function. Refer to Table 4-11 for definitions.	R/W	0010b
3:0	**LED1 Configuration** This field configures the LED1 pin function. Refer to Table 4-11 for definitions.	R/W	0001b

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5.2.20 LED BEHAVIOR REGISTER

Index (In Decimal): 23 Size: 16 bits

This register selects the operating parameters of the PHY LEDs when in extended mode. This register is only used when the KSZ9031 LED Mode bit in the KSZ9031 LED Mode Register is clear.

Bits	Description	Type	Default
15	**RESERVED**	R/W	-
14	**LED Activity Output Select**	R/W	0b
13	**RESERVED**	R/W	-
12	**LED Pulsing Enable**	R/W	1b
11:10	**LED Blink / Pulse-Stretch Rate** 00 = 2.5 Hz Blink Rate / 400 ms pulse-stretch 01 = 5 Hz Blink Rate / 200 ms pulse-stretch 10 = 10 Hz Blink Rate / 100 ms pulse-stretch 11 = 20 Hz Blink Rate / 50 ms pulse-stretch	R/W	00b
9:7	**RESERVED**	R/W	-
6:5	**LED Pulse Stretch Enables** Configures LED2 (bit 6) and LED1 (bit 5) to either pulse-stretch when 1, or blink when 0.	R/W	00b
4:2	**RESERVED**	R/W	-
1:0	**LED Combination Disables** Configures LED2 (bit 1) and LED1 (bit 0) to either combine link/activity and duplex/collision when 0, or disable combination, providing link-only and duplex-only when 1.	R/W	00b

5.2.21 MDIO DRIVE REGISTER

Index (In Decimal): 25 Size: 16 bits

Bits	Description	Type	Default
15:2	**RESERVED**	R/W	-
1	**MDIO Drive** When set to a 0, the MDIO output is open-drain When set to a 1, the MDIO output is push-pull	R/W	0b
0	**RESERVED**	R/W	-

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5.2.22 KSZ9031 LED MODE REGISTER

Index (In Decimal): 26 Size: 16 bits

Bits	Description	Type	Default
15	**RESERVED**	R/W	-
14	**KSZ9031 LED Mode** 1 = KSZ9031 LED mode 0 = Extended LED mode **Note:** For normal LED operation, this bit should always be written as a 1.	R/W	1b
13:0	**RESERVED**	R/W	-

5.2.23 INTERRUPT CONTROL/STATUS REGISTER

Index (In Decimal): 27 Size: 16 bits

Bits	Description	Type	Default
15	**Jabber Interrupt Enable** 1 = Enable jabber interrupt 0 = Disable jabber interrupt	R/W	0b
14	**Receive Error Interrupt Enable** 1 = Enable receive error interrupt 0 = Disable receive error interrupt	R/W	0b
13	**Page Received Interrupt Enable** 1 = Enable page received interrupt 0 = Disable page received interrupt	R/W	0b
12	**Parallel Detect Fault Interrupt Enable** 1 = Enable parallel detection fault interrupt 0 = Disable parallel detection fault interrupt	R/W	0b
11	**Link Partner Acknowledge Interrupt Enable** 1 = Enable link partner acknowledge interrupt 0 = Disable link partner acknowledge interrupt	R/W	0b
10	**Link Down Interrupt Enable** 1 = Enable link down interrupt 0 = Disable link down interrupt	R/W	0b
9	**Remote Fault Interrupt Enable** 1 = Enable remote fault interrupt 0 = Disable remote fault interrupt	R/W	0b
8	**Link Up Interrupt Enable** 1 = Enable link up interrupt 0 = Disable link up interrupt	R/W	0b

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Bits	Description	Type	Default
7	**Jabber Interrupt** 1 = Jabber interrupt 0 = No jabber interrupt	RC	0b
6	**Receive Error Interrupt** 1 = Receive error interrupt 0 = No receive error interrupt	RC	0b
5	**Page Receive Interrupt** 1 = Page receive interrupt 0 = No page receive interrupt	RC	0b
4	**Parallel Detect Fault Interrupt** 1 = Parallel detection fault interrupt 0 = No parallel detection fault interrupt	RC	0b
3	**Link Partner Acknowledge Interrupt** 1 = Link partner acknowledge interrupt 0 = No link partner acknowledge interrupt	RC	0b
2	**Link Down Interrupt** 1 = Link down interrupt 0 = No link down interrupt	RC	0b
1	**Remote Fault Interrupt** 1 = Remote fault interrupt 0 = No remote fault interrupt	RC	0b
0	**Link Up Interrupt** 1 = Link up interrupt 0 = No link up interrupt	RC	0b

5.2.24 AUTO-MDI/MDI-X REGISTER

Index (In Decimal): 28 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	RO	-
7	**MDI Set** When the Swap-Off bit of this register is asserted (1), 1 = PHY is set to operate in MDI mode 0 = PHY is set to operate in MDI-X mode	R/W	0b
6	**Swap-Off** 1 = Disable Auto-MDI/MDI-X function 0 = Enable Auto-MDI/MDI-X function	R/W	0b
5:0	**RESERVED**	RO	-

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5.2.25 SOFTWARE POWER DOWN CONTROL REGISTER

Index (In Decimal): 29 Size: 16 bits

Bits	Description	Type	Default
15:12	**RESERVED**	R/W	-
11	**spd_clock_gate_override** 0 = internal clocks are gated during the Software Power Down (SPD) mode. 1 = internal clock gating is overridden during the SPD mode.	R/W	0b
10	**spd_pll_disable** 0 = PLL is enabled during the Software Power Down (SPD) mode. 1 = PLL is disabled during the SPD mode.	R/W	0b
9:8	**RESERVED**	R/W	-
7	**IO_DC_test_en** 1 = enable IO test	R/W	0b
6	**VOH** 1 = “VDD” to output IO 0 = “GND” to IO	R/W	0b

5.2.26 EXTERNAL LOOPBACK REGISTER

Index (In Decimal): 30 Size: 16 bits

Bits	Description	Type	Default
15:4	**RESERVED**	R/W	-
3	**Ext_lpbk** External loopback enable	R/W	0b
2:0	**RESERVED**	R/W	-

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5.2.27 CONTROL REGISTER

Index (In Decimal): 31 Size: 16 bits

Bits	Description	Type	Default
15	**RESERVED**	RO	-
14	**Interrupt Polarity Invert** 1 = invert 0 = normal	R/W	0b
13:10	**RESERVED**	RO	-
9	**Enable Jabber** 1 = Enable jabber counter 0 = Disable	R/W	1b
8	**Enable SQE Test** 1 = Enable SQE test 0 = Disable	R/W	1b
7	**RESERVED**	RO	-
6	**Speed status 1000T** Indicates speed is 1000T	RO	0b
5	**Speed status 100TX** Indicates speed is 100TX	RO	0b
4	**Speed status 10BT** Indicates speed is 10BT	RO	0b
3	**Duplex status** Indicates duplex status	RO	0b
2	**1000BASE-T Mater/Slave status** 1 = Indicates 1000BASE-T Master mode 0 = Indicates 1000BASE-T Slave mode	RO	0b
1	**Software Reset** 1 = Reset PHY except all registers 0 = Disable reset	W1S/RC	0b
0	**Link Status Check Fail** 1 = Fail 0 = Not Failing	RC	0b

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5.3 MDIO Manageable Device (MMD) Registers

MMD registers provide indirect read/write access to up to 32 MMD device addresses with each device supporting up to 65,536 16-bit registers, as defined in Clause 22 of the IEEE 802.3 Specification. This device, however, uses only a small fraction of the available registers. See Table 5-2 for a list of supported MMD device addresses and their associated register addresses.

The following two standard registers serve as the portal registers to access the indirect MMD registers.

- MMD Access Control Register
- MMD Access Address/Data Register

Example: MMD Register Write

Write MMD - Device Address 2h, Register 10h = 0001h to enable link-up detection to trigger PME for WOL.

1. Write the MMD Access Control Register with 0002h // Select address register for MMD – Device Address 2h.
2. Write the MMD Access Address/Data Register with 0010h // Set address register = 10h.
3. Write the MMD Access Control Register with 4002h // Select data register for MMD – Device Address 2h.
4. Write the MMD Access Address/Data Register with 0001h // Write value 0001h to MMD – Device Address 2h, Register 10h.

Example: MMD Register Read

Read MMD - Device Address 3h, Register 14h EEE Control and Capability.

1. Write the MMD Access Control Register with 0003h // Select address register for MMD – Device Address 3h.
2. Write the MMD Access Address/Data Register with 0014h // Set address register = 14h.
3. Write the MMD Access Control Register with 4003h // Select data register for MMD – Device Address 3h.
4. Read the MMD Access Address/Data Register // Read data in MMD – Device Address 3h, Register 14h.

It is also possible to automatically increment the register address for reads and/or writes

Example: MMD Register Writes with Post Increment

Write MMD - Device Address 2h, Register 11h – 13h = 0123_4567_89ABh for the magic packet's MAC address.

1. Write the MMD Access Control Register with 0002h // Select address register for MMD – Device Address 2h.
2. Write the MMD Access Address/Data Register with 0011h // Set address register = 11h.
3. Write the MMD Access Control Register with 8002h or C002h // Select data register with post increment for MMD – Device Address 2h.
4. Write the MMD Access Address/Data Register with 0123h // Write value 0123h to MMD – Device Address 2h, Register 11h.
5. Write the MMD Access Address/Data Register with 4567h // Write value 4567h to MMD – Device Address 2h, Register 12h.
6. Write the MMD Access Address/Data Register with 89ABh // Write value 89ABh to MMD – Device Address 2h, Register 13h.

Example: MMD Register Reads with Post Increment

Read MMD - Device Address 2h, Register 11h – 13h for the magic packet's MAC address.

1. Write the MMD Access Control Register with 0002h // Select address register for MMD – Device Address 2h.
2. Write the MMD Access Address/Data Register with 0011h // Set address register = 11h.
3. Write the MMD Access Control Register with 8002h // Select data register with post increment for MMD – Device Address 2h.
4. Read the MMD Access Address/Data Register // Read data in MMD – Device Address 2h, Register 11h.
5. Read the MMD Access Address/Data Register // Read data in MMD – Device Address 2h, Register 12h.
6. Read the MMD Access Address/Data Register // Read data in MMD – Device Address 2h, Register 13h.

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5.3.1 MEAN SLICER ERROR REGISTER

Index (In Decimal): 1.225 Size: 16 bits

Bits	Description	Type	Default
15:0	**Mean Slicer Error** This field provides the current mean error value. Either absolute or square mode values can be provided. **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	0000h

5.3.2 DCQ MEAN SQUARE ERROR REGISTER

Index (In Decimal): 1.226 Size: 16 bits

Bits	Description	Type	Default
15:10	**RESERVED**	RO	-
9	**MSE Value Valid** This field provides the mean square error valid indication. 1 = invalid 0 = valid **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	0b
8:0	**MSE Value** This field provides the current mean square error value. **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	000h

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5.3.3 DCQ MEAN SQUARE ERROR WORST CASE REGISTER

Index (In Decimal): 1.227 Size: 16 bits

Bits	Description	Type	Default
15:10	**RESERVED**	RO	-
9	**MSE Worst Case Value Valid** This field provides the worst case mean square error valid indication. 1 = invalid 0 = valid **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	0b
8:0	**MSE Worst Case Value** This field provides the worst case mean square error value since the last time the channel was captured for reading. **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	000h

5.3.4 DCQ SQI REGISTER

Index (In Decimal): 1.228 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	RO	-
7:5	**SQI Worst Case** This field indicates the worst case SQI value since the last time the channel was captured for reading. **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	000b
4	**RESERVED**	RO	-

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Bits	Description	Type	Default
3:1	**SQI** This field indicates the current SQI value. **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	000b
0	**RESERVED**	RO	-

5.3.5 DCQ PEAK MSE REGISTER

Index (In Decimal): 1.229 Size: 16 bits

Bits	Description	Type	Default
15:8	**Peak MSE Worst Case** This field indicates the worst case peak MSE value since the last time the channel was captured for reading. 0-63 = Peak MSE 64-254 = Invalid 255 = measurement not ready **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	00h
7:0	**Peak MSE Value** This field provides the current peak MSE value. 0-63 = Peak MSE 64-254 = Invalid 255 = measurement not ready **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	00h

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5.3.6 DCQ CONTROL REGISTER

Index (In Decimal): 1.230 Size: 16 bits

Bits	Description	Type	Default
15	**DCQ Read Capture** When this bit is set the DCQ values are captured.	R/W/SC	0b
14:2	**RESERVED**	R/W	-
1:0	**DCQ Channel Number** This field specifies which channel's (wire pair) values are captured into the DCQ registers. 00 = Channel A 01 = Channel B 10 = Channel C 11 = Channel D **Note:** Channel A is used for both 100BASE-TX and 1000BASE-T. Channels B-D are only used for 1000BASE-T.	R/W	00b

5.3.7 DCQ CONFIGURATION REGISTER

Index (In Decimal): 1.231 Size: 16 bits

Bits	Description	Type	Default
15:14	**scale613** Scaling factor for SQI method 5 (TC1 peak MSE).	R/W	00b
13:10	**sqi_kp3** LPF bandwidth control.for SQI method 5 (TC1 peak MSE).	R/W	101b
9:8	**scale611** Scaling factor for SQI methods 3 (TC1 MSE) and 4 (TC1 SQI).	R/W	00b
7	**sqi_reset** When set the SQI logic is reset. **Note:** This bit does not self-clear.	R/W	0b
6	**sqi_squ_mode_en** 0 = Absolute mode 1 = Square mode	R/W	1b
5	**sqi_enable** When set SQI measurements are enabled.	R/W	1b
4:0	**sqi_kp** LPF bandwidth control.for SQI methods 2 (non TC1 LPF mean), 3 (TC1 MSE) and 4 (TC1 SQI).	R/W	0Dh

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5.3.8 DCQ SQI TABLE REGISTERS

Index (In Decimal): 1.232-238 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	-
8:0	**SQI_VALUE** Lookup table utilized for implement of SQI method 4 (TC1 SQI). These registers set the thresholds to map the error value to a SQI level.	R/W	Table 5-3

TABLE 5-3: SQI VALUE DEFAULTS

Register	Default (Hexadecimal)
SQI_TBL1.SQI_VALUE	A3h
SQI_TBL2.SQI_VALUE	82h
SQI_TBL3.SQI_VALUE	67h
SQI_TBL4.SQI_VALUE	52h
SQI_TBL5.SQI_VALUE	41h
SQI_TBL6.SQI_VALUE	34h
SQI_TBL7.SQI_VALUE	29h

5.3.9 COMMON CONTROL REGISTER

Index (In Decimal): 2.0 Size: 16 bits

Bits	Description	Type	Default
15:5	**RESERVED**	RO	-
4	**Single LED** 1 = Individual-LED mode 0 = Tri-color-LED mode By default, this bit reflects the value of the LED_MODE strapping pin. If written as a 1, the value of the LED_MODE strapping pin is overridden and Single-LED mode is selected.	R/W	Note 5-3
3:2	**RESERVED**	R/W	-
1	**clk125 Enable** A 1 enables the 125 MHz clock output onto the CLK125_NDO pin.	R/W	Note 5-4
0	**All-PHYAD Enable** When this bit is set, the PHY will respond to PHY address 0 as well as it's assigned PHY address.	R/W	Note 5-5

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Note 5-3 Set by the LED_MODE strapping pin. See Section 3.3, "Configuration Straps" for details.

Note 5-4 Set by the CLK125_EN strapping pin. See Section 3.3, "Configuration Straps" for details.

Note 5-5 Set by the inverse of the ALLPHYAD strapping pin. See Section 3.3, "Configuration Straps" for details.

5.3.10 STRAP STATUS REGISTER

Index (In Decimal): 2.1 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	RO	-
7	**LED_MODE Strap-In Status** 1 = Individual LED mode 0 = Tri-color LED mode	RO	Note 5-6
6	**RESERVED**	RO	-
5	**CLK125_EN Strap-In Status** 1 = CLK125_EN strap-in is enabled 0 = CLK125_EN strap-in is disabled	RO	Note 5-7
4:0	**PHYAD[2:0] Strap-In Status** Strap-in value for PHY address **Note:** Bits [4:3] of PHY address are always set to '00'.	RO	Note 5-8

Note 5-6 Set by the LED_MODE strapping pin. See Section 3.3, "Configuration Straps" for details.

Note 5-7 Set by the CLK125_EN strapping pin. See Section 3.3, "Configuration Straps" for details

Note 5-8 Set by the PHYAD[2:0] strapping pins. See Section 3.3, "Configuration Straps" for details.

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5.3.11 OPERATION MODE STRAP OVERRIDE REGISTER

Index (In Decimal): 2.2 Size: 16 bits

This register may be used to override the value of the MODE[3:0] configuration straps.

Bits	Description	Type	Default
15	**RESERVED**	RO	-
14	**an_all_ng_h_cap** 1 = RGMII mode. Advertise all capabilities except 1000BASE-T half duplex	R/W	Note 5-9
13	**RESERVED**	RO	-
12	**an_g_f_cap** 1 = RGMII mode. Advertise 1000BASE-T full duplex only	R/W	Note 5-9
11	**RESERVED**	RO	-
10	**rgmii_pme_on_int_mode** 1 = RGMII mode with PME_N2 mapped onto INT_N	R/W	Note 5-9
9	**RESERVED**	RO	-
8	**rgmii_pme_on_led1_mode** 1 = RGMII mode with PME_N1 mapped onto LED1	R/W	Note 5-9
7	**iddq_mode** Chip IDDQ Power-Down 1 = Chip power-down mode	RO	Note 5-9
6:5	**RESERVED**	RO	-
4	**ntree_mode** NAND Tree mode 1 = NAND Tree mode	R/W	Note 5-9
3:2	**RESERVED**	RO	-
1	**RESERVED**	RO	-
0	**RESERVED**	RO	-

Note 5-9 Set by the MODE[3:0] strapping pins. See Section 3.3, "Configuration Straps" for details.

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5.3.12 OPERATION MODE STRAP REGISTER

Index (In Decimal): 2.3 Size: 16 bits

This register indicates the value of the MODE[3:0] configuration straps that were latched into the device at reset.

Bits	Description	Type	Default
15	**RESERVED**	RO	-
14	**Strap_an_all_ng_h_cap** 1 = RGMII mode. Advertise all capabilities except 1000BASE-T half duplex	RO	Note 5-10
13	**RESERVED**	RO	-
12	**Strap_an_g_f_cap** 1 = RGMII mode. Advertise 1000BASE-T full duplex only	RO	Note 5-10
11	**RESERVED**	RO	-
10	**Strap_rgmii_pme_on_int_mode** 1 = RGMII mode with PME_N2 mapped onto INT_N	RO	Note 5-10
9	**RESERVED**	RO	-
8	**Strap_rgmii_pme_on_led1_mode** 1 = RGMII mode with PME_N1 mapped onto LED1	RO	Note 5-10
7	**Strap_iddq_mode** Chip IDDQ Power-Down Strap-In Status 1 = Chip power-down mode	RO	Note 5-10
6:5	**RESERVED**	RO	-
4	**Strap_ntree_mode** NAND Tree Strap-In Status 1 = NAND Tree mode	RO	Note 5-10
3:2	**RESERVED**	RO	-
1	**RESERVED**	RO	-
0	**RESERVED**	RO	-

Note 5-10 Set by the MODE[3:0] strapping pins. See Section 3.3, "Configuration Straps" for details.

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5.3.13 CLOCK INVERT AND CONTROL SIGNAL PAD SKEW REGISTER

Index (In Decimal): 2.4 Size: 16 bits

Bits	Description	Type	Default
15:10	**RESERVED**	R/W	0h
9	**Inverse RGMII RXC Output** 0 = no change 1 = inverse on RXC for RGMII	R/W	0b
8	**Inverse RGMII TXC Input** 0 = no change 1 = inverse on TXC for RGMII	R/W	0b
7:4	**RX_CTL Skew** RX_CTL output skew Control (~28 min to ~73 max ps/step)	R/W	7h
3:0	**TX_CTL Skew** TX_CTL input skew Control (~28 min to ~73 max ps/step)	R/W	7h

5.3.14 RGMII RX DATA PAD SKEW REGISTER

Index (In Decimal): 2.5 Size: 16 bits

Bits	Description	Type	Default
15:12	**RXD3 Pad Skew** RGMII RXD3 output pad skew control (~28 min to ~73 max ps/step)	R/W	7h
11:8	**RXD2 Pad Skew** RGMII RXD2 output pad skew control (~28 min to ~73 max ps/step)	R/W	7h
7:4	**RXD1 Pad Skew** RGMII RXD1 output pad skew control (~28 min to ~73 max ps/step)	R/W	7h
3:0	**RXD0 Pad Skew** RGMII RXD0 output pad skew control (~28 min to ~73 max ps/step)	R/W	7h

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5.3.15 RGMII TX DATA PAD SKEW REGISTER

Index (In Decimal): 2.6 Size: 16 bits

Bits	Description	Type	Default
15:12	**TXD3 Pad Skew** RGMII TXD3 output pad skew control (~28 min to ~73 max ps/step)	R/W	7h
11:8	**TXD2 Pad Skew** RGMII TXD2 output pad skew control (~28 min to ~73 max ps/step)	R/W	7h
7:4	**TXD1 Pad Skew** RGMII TXD1 output pad skew control (~28 min to ~73 max ps/step)	R/W	7h
3:0	**TXD0 Pad Skew** RGMII TXD0 output pad skew control (~28 min to ~73 max ps/step)	R/W	7h

5.3.16 CLOCK PAD SKEW REGISTER

Index (In Decimal): 2.8 Size: 16 bits

Bits	Description	Type	Default
15:10	**RESERVED**	RO	-
9:5	**TXC Pad Input Skew** TXC input Skew Control (~24 min to ~58 max ps/step)	R/W	07h
4:0	**RXC_pad_oskew** RXC output Skew Control (~24 min to ~58 max ps/step)	R/W	07h

5.3.17 SELF-TEST PACKET COUNT LO REGISTER

Index (In Decimal): 2.9 Size: 16 bits

Bits	Description	Type	Default
15:0	**Self_test_frame_cnt[15:0]**	R/W	0000h

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5.3.18 SELF-TEST PACKET COUNT HI REGISTER

Index (In Decimal): 2.10 Size: 16 bits

Bits	Description	Type	Default
15:0	**Self_test_frame_cnt[31:16]**	R/W	0001h

5.3.19 SELF-TEST STATUS REGISTER

Index (In Decimal): 2.11 Size: 16 bits

Bits	Description	Type	Default
15:1	**RESERVED**	RO	-
0	**Self_test_done** 0 = Self test running 1 = Self test finished	RO	0b

5.3.20 SELF-TEST FRAME COUNT ENABLE REGISTER

Index (In Decimal): 2.12 Size: 16 bits

Bits	Description	Type	Default
15:1	**RESERVED**	RO	-
0	**Self_test_frame_cnt_en** 0 = disabled 1 = enabled	R/W	0b

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5.3.21 SELF-TEST PGEN ENABLE REGISTER

Index (In Decimal): 2.13 Size: 16 bits

Bits	Description	Type	Default
15:1	**RESERVED**	RO	-
0	**Self_test_pgen_en** 0 = disabled 1 = enabled	R/W	0b

5.3.22 SELF-TEST ENABLE REGISTER

Index (In Decimal): 2.14 Size: 16 bits

Bits	Description	Type	Default
15	**Self_test_external_clk_sel** When this bit is high, the self-test function requires a clock to be supplied onto the GTX_CLK input pin. When this bit is low, the self-test function does not require a clock to be supplied.	R/W	0b
14:1	**RESERVED**	RO	-
0	**Self_test_en** 0 = disabled 1 = enabled	R/W	0b

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5.3.23 WAKE-ON-LAN CONTROL REGISTER

Index (In Decimal): 2.16 Size: 16 bits

Bits	Description	Type	Default
15:14	**PME Output Select** Controls definition of PME signal when assigned to INT_N. 00 = PME 01 = Interrupt 10 = Interrupt ORed with PME 11 = always 0 Controls definition of PME signal when assigned to LED1. 00 = PME 01 = LED 10 = LED ORed with PME 11 = always 1	R/W	00b
13:8	**RESERVED**	R/W	-
7	**Wake-on-LAN Reset (Wol_reset)** Write a 1 then a 0 to reset the WoL module.	R/W	0b
6	**Enable Magic Packet Detection Wake Event** Enables magic packet detection as a wake event	R/W	0b
5:2	**Enable Customized Frame Filter Wake Event** Enables customized frame filters as wake events	R/W	0h
1	**Enable Link Down Wake Event** Enables link down as a wake event	R/W	0b
0	**Enable Link Up Wake Event** Enables link up as a wake event	R/W	0b

5.3.24 WAKE-ON-LAN-MAC-LO REGISTER

Index (In Decimal): 2.17 Size: 16 bits

Bits	Description	Type	Default
15:0	**m-pkt-mac-lo** MAC-Address[15:0] of magic packet	R/W	0000h

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5.3.25 WAKE-ON-LAN-MAC-MI REGISTER

Index (In Decimal): 2.18 Size: 16 bits

Bits	Description	Type	Default
15:0	**m-pkt-mac-mi** MAC-Address[31:16] of magic packet	R/W	0000h

5.3.26 WAKE-ON-LAN-MAC-HI REGISTER

Index (In Decimal): 2.19 Size: 16 bits

Bits	Description	Type	Default
15:0	**m-pkt-mac-hi** MAC-Address[47:32] of magic packet	R/W	0000h

5.3.27 CUSTOMIZED-PKT-0-CRC-LO REGISTER

Index (In Decimal): 2.20 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-0-crc-lo** Customized frame filter 0 CRC[15:0]	R/W	0000h

5.3.28 CUSTOMIZED-PKT-0-CRC-HI REGISTER

Index (In Decimal): 2.21 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-0-crc-hi** Customized frame filter 0 CRC[31:16]	R/W	0000h

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5.3.29 CUSTOMIZED-PKT-1-CRC-LO REGISTER

Index (In Decimal): 2.22 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-1-crc-lo** Customized frame filter 1 CRC[15:0]	R/W	0000h

5.3.30 CUSTOMIZED-PKT-1-CRC-HI REGISTER

Index (In Decimal): 2.23 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-1-crc-hi** Customized frame filter 1 CRC[31:16]	R/W	0000h

5.3.31 CUSTOMIZED-PKT-2-CRC-LO REGISTER

Index (In Decimal): 2.24 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-2-crc-lo** Customized frame filter 2 CRC[15:0]	R/W	0000h

5.3.32 CUSTOMIZED-PKT-2-CRC-HI REGISTER

Index (In Decimal): 2.25 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-2-crc-hi** Customized frame filter 2 CRC[31:16]	R/W	0000h

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5.3.33 CUSTOMIZED-PKT-3-CRC-LO REGISTER

Index (In Decimal): 2.26 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-3-crc-lo** Customized frame filter 3 CRC[15:0]	R/W	0000h

5.3.34 CUSTOMIZED-PKT-3-CRC-HI REGISTER

Index (In Decimal): 2.27 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-3-crc-hi** Customized frame filter 3 CRC[31:16]	R/W	0000h

5.3.35 CUSTOMIZED-PKT-0-MASK_LL REGISTER

Index (In Decimal): 2.28 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-0-mask-ll** Customized frame filter 0 mask[15:0]	R/W	0000h

5.3.36 CUSTOMIZED-PKT-0-MASK_LH REGISTER

Index (In Decimal): 2.29 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-0-mask-lh** Customized frame filter 0 mask[31:16]	R/W	0000h

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5.3.37 CUSTOMIZED-PKT-0-MASK_HL REGISTER

Index (In Decimal): 2.30 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-0-mask-hl** Customized frame filter 0 mask[47:32]	R/W	0000h

5.3.38 CUSTOMIZED-PKT-0-MASK_HH REGISTER

Index (In Decimal): 2.31 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-0-mask-hh** Customized frame filter 0 mask[63:48]	R/W	0000h

5.3.39 CUSTOMIZED-PKT-1-MASK_LL REGISTER

Index (In Decimal): 2.32 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-1-mask-ll** Customized frame filter 1 mask[15:0]	R/W	0000h

5.3.40 CUSTOMIZED-PKT-1-MASK_LH REGISTER

Index (In Decimal): 2.33 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-1-mask-lh** Customized frame filter 1 mask[31:16]	R/W	0000h

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5.3.41 CUSTOMIZED-PKT-1-MASK_HL REGISTER

Index (In Decimal): 2.34 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-1-mask-hl** Customized frame filter 1 mask[47:32]	R/W	0000h

5.3.42 CUSTOMIZED-PKT-1-MASK_HH REGISTER

Index (In Decimal): 2.35 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-1-mask-hh** Customized frame filter 1 mask[63:48]	R/W	0000h

5.3.43 CUSTOMIZED-PKT-2-MASK_LL REGISTER

Index (In Decimal): 2.36 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-2-mask-ll** Customized frame filter 2 mask[15:0]	R/W	0000h

5.3.44 CUSTOMIZED-PKT-2-MASK_LH REGISTER

Index (In Decimal): 2.37 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-2-mask-lh** Customized frame filter 2 mask[31:16]	R/W	0000h

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5.3.45 CUSTOMIZED-PKT-2-MASK_HL REGISTER

Index (In Decimal): 2.38 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-2-mask-hl** Customized frame filter 2 mask[47:32]	R/W	0000h

5.3.46 CUSTOMIZED-PKT-2-MASK_HH REGISTER

Index (In Decimal): 2.39 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-2-mask-hh** Customized frame filter 2 mask[63:48]	R/W	0000h

5.3.47 CUSTOMIZED-PKT-3-MASK_LL REGISTER

Index (In Decimal): 2.40 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-3-mask-ll** Customized frame filter 3 mask[15:0]	R/W	0000h

5.3.48 CUSTOMIZED-PKT-3-MASK_LH REGISTER

Index (In Decimal): 2.41 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-3-mask-lh** Customized frame filter 3 mask[31:16]	R/W	0000h

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5.3.49 CUSTOMIZED-PKT-3-MASK_HL REGISTER

Index (In Decimal): 2.42 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-3-mask-hl** Customized frame filter 3 mask[47:32]	R/W	0000h

5.3.50 CUSTOMIZED-PKT-3-MASK_HH REGISTER

Index (In Decimal): 2.43 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-3-mask-hh** Customized frame filter 3 mask[63:48]	R/W	0000h

5.3.51 WAKE-ON-LAN CONTROL STATUS REGISTER

Index (In Decimal): 2.44 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_ctrl_status** Wake-on-LAN Control module status	RO	0000h

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5.3.52 WAKE-ON-LAN CUSTOM PACKET RECEIVE STATUS REGISTER

Index (In Decimal): 2.45 Size: 16 bits

Bits	Description	Type	Default
15	**cpkt_pmen** custom packet 0 enabled and custom packet 0 found	RO	0b
14:12	**mismatch code**	RO	000b
11	**good_pkt_crc**	RO	0b
10:7	**crc_match** crc matched bit 10 = custom packet 3 bit 9 = custom packet 2 bit 8 = custom packet 1 bit 7 = custom packet 0	RO	0000b
6:3	**cpkt_found** custom packet found bit 6 = custom packet 3 bit 5 = custom packet 2 bit 4 = custom packet 1 bit 3 = custom packet 0	RO	0000b
2:0	**cpkt_state** custom packet detection state	RO	000b

5.3.53 WAKE-ON-LAN MAGIC PACKET RECEIVE STATUS REGISTER

Index (In Decimal): 2.46 Size: 16 bits

Bits	Description	Type	Default
15	**mpkt_pmen** magic packet enabled and magic packet found	RO	0b
14:12	**byte count**	RO	000b
11:9	**mismatch code**	RO	000b
8:5	**macda_match_count**	RO	0h
4	**good_pkt_crc**	RO	0b
3	**mpkt_found** magic packet found	RO	0b
2:0	**mpkt_state** magic packet detection state	RO	000b

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5.3.54 WAKE-ON-LAN DATA MODULE STATUS REGISTER

Index (In Decimal): 2.47 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_data_status** Wake-on-LAN Data module status	RO	0000h

5.3.55 CUSTOMIZED PKT-0 RECEIVED CRC-L REGISTER

Index (In Decimal): 2.48 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_0 [15:0]** Wake-on-LAN CRC [15:0] calculated on Customized frame filter 0	RO	0000h

5.3.56 CUSTOMIZED PKT-0 RECEIVED CRC-H REGISTER

Index (In Decimal): 2.49 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_0 [31:16]** Wake-on-LAN CRC [31:16] calculated on Customized frame filter 0	RO	0000h

5.3.57 CUSTOMIZED PKT-1 RECEIVED CRC-L REGISTER

Index (In Decimal): 2.50 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_1 [15:0]** Wake-on-LAN CRC [15:0] calculated on Customized frame filter 1	RO	0000h

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5.3.58 CUSTOMIZED PKT-1 RECEIVED CRC-H REGISTER

Index (In Decimal): 2.51 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_1 [31:16]** Wake-on-LAN CRC [31:16] calculated on Customized frame filter 1	RO	0000h

5.3.59 CUSTOMIZED PKT-2 RECEIVED CRC-L REGISTER

Index (In Decimal): 2.52 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_2 [15:0]** Wake-on-LAN CRC [15:0] calculated on Customized frame filter 2	RO	0000h

5.3.60 CUSTOMIZED PKT-2 RECEIVED CRC-H REGISTER

Index (In Decimal): 2.53 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_2 [31:16]** Wake-on-LAN CRC [31:16] calculated on Customized frame filter 2	RO	0000h

5.3.61 CUSTOMIZED PKT-3 RECEIVED CRC-L REGISTER

Index (In Decimal): 2.54 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_3 [15:0]** Wake-on-LAN CRC [15:0] calculated on Customized frame filter 3	RO	0000h

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5.3.62 CUSTOMIZED PKT-3 RECEIVED CRC-H REGISTER

Index (In Decimal): 2.55 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_3 [31:16]** Wake-on-LAN CRC [31:16] calculated on Customized frame filter 3	RO	0000h

5.3.63 SELF-TEST CORRECT COUNT LO REGISTER

Index (In Decimal): 2.60 Size: 16 bits

Following a self-test, this register along with Self-Test Correct Count HI Register indicate the count of frames with a correct FCS.

Bits	Description	Type	Default
15:0	**Self_test_correct_cnt[15:0]**	RO	-

5.3.64 SELF-TEST CORRECT COUNT HI REGISTER

Index (In Decimal): 2.61 Size: 16 bits

Following a self-test, this register along with Self-Test Correct Count LO Register indicate the count of frames with a correct FCS.

Bits	Description	Type	Default
15:0	**Self_test_correct_cnt[31:16]**	RO	-

5.3.65 SELF-TEST ERROR COUNT LO REGISTER

Index (In Decimal): 2.62 Size: 16 bits

Following a self-test, this register along with Self-Test Error Count HI Register indicate the count of frames with an incorrect FCS.

Bits	Description	Type	Default
15:0	**Self_test_error_cnt[15:0]**	RO	-

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5.3.66 SELF-TEST ERROR COUNT HI REGISTER

Index (In Decimal): 2.63 Size: 16 bits

Following a self-test, this register along with Self-Test Error Count LO Register indicate the count of frames with an incorrect FCS.

Bits	Description	Type	Default
15:0	**Self_test_error_cnt[31:16]**	RO	-

5.3.67 SELF-TEST BAD SFD COUNT LO REGISTER

Index (In Decimal): 2.64 Size: 16 bits

Following a self-test, this register along with Self-Test Bad SFD Count HI Register indicate the count of frames with a bad SFD.

Bits	Description	Type	Default
15:0	**Self_test_bad_sfd_cnt[15:0]**	RO	-

5.3.68 SELF-TEST BAD SFD COUNT HI REGISTER

Index (In Decimal): 2.65 Size: 16 bits

Following a self-test, this register along with Self-Test Bad SFD Count LO Register indicate the count of frames with a bad SFD.

Bits	Description	Type	Default
15:0	**Self_test_bad_sfd_cnt[31:16]**	RO	-

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5.3.69 RX DLL CONTROL REGISTER

Index (In Decimal): 2.76 Size: 16 bits

Bits	Description	Type	Default
15	**RESERVED**	RO	-
14	**rxdll_tune_disable** When this bit is set the DLL is not dynamically tuned. It is, however, still used to provide a fixed delay as set by rxdll_tap_sel.	R/W	0b
13	**rxdll_reset** When this bit is set the DLL is reset. **Note:** This bit does not self-clear and must be written back to a 0	R/W	0b
12	**bypass rxdll** 1 = RXC DLL delay is not used	R/W	0b
11:6	**rxdll_tap_sel** Used as the initial DLL tap setting before the first tuning cycle. Also used to set the delay value during manual tuning mode. **Note:** The rxdll_reset bit must be set following a change to this field.	R/W	1Bh
5:0	**rxdll_tap_adj** Used to statically account for the output multiplexer stage in the delay chain when DLL tuning is enabled.	R/W	11h

5.3.70 TX DLL CONTROL REGISTER

Index (In Decimal): 2.77 Size: 16 bits

Bits	Description	Type	Default
15	**RESERVED**	RO	-
14	**txdll_tune_disable** When this bit is set the DLL is not dynamically tuned. It is, however, still used to provide a fixed delay as set by txdll_tap_sel.	R/W	0b
13	**txdll_reset** When this bit is set the DLL is reset. **Note:** This bit does not self-clear and must be written back to a 0	R/W	0b
12	**bypass txdll** 1 = TXC DLL delay is not used	R/W	1b
11:6	**txdll_tap_sel** Used as the initial DLL tap setting before the first tuning cycle. Also used to set the delay value during manual tuning mode. **Note:** The txdll_reset bit must be set following a change to this field.	R/W	1Bh

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Bits	Description	Type	Default
5:0	**txdll_tap_adj** Used to statically account for the output multiplexer stage in the delay chain when DLL tuning is enabled.	R/W	11h

5.3.71 PCS CONTROL 1 REGISTER

Index (In Decimal): 3.0 Size: 16 bits

Bits	Description	Type	Default
15	**RESET** 1=PCS reset 0=Normal Operation This bit is not used	R/W	0b
14	**Loop Back** 1 = enable loop-back mode 0 = Normal Operation This bit is not used	R/W	0b
13	**Speed Selection** (bit13 / bit6) 11 = bit 5:2 select speed 0x = unspecified x0 = unspecified This bit is not used	R/W	0b
12	**EEE100_idle_sel** 0 = 9031 1 = 8050	R/W	0b
11	**Low power** 1 = low-power-mode 0 = normal operation	R/W	0b
10	**Clock-stop enable** 1 = the PHY may stop the clock during LPI 0 = clock not stoppable	R/W	0b
9:7	**TX FIFO threshold**	R/W	111b
6	**Speed Selection** (bit13 / bit6) 11 = bit 5:2 select speed 0x = unspecified x0 = unspecified This bit is not used	R/W	0b

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Bits	Description	Type	Default
5:2	**Speed Selection** (bits [5:2]) 1 x x x = Reserved 0 1 1 x = Reserved 0 1 0 1 = Reserved 0 1 0 0 = 100Gb/s 0 0 1 1 = 40Gb/s 0 0 1 0 = 10/1Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10Gb/s These bits are not used	R/W	0000b
1	**RESERVED**	R/W	-
0	**Dbg_pcs100_sel** 1 = select eee100 RX signals 0 = original	R/W	0b

5.3.72 PCS STATUS 1 REGISTER

Index (In Decimal): 3.1 Size: 16 bits

Bits	Description	Type	Default
15:12	**RESERVED**	RO	-
11	**TX LPI received** 1 = TX PCS has received LPI 0 = LPI not received	RO/LH	0b
10	**RX LPI received** 1 = RX PCS has received LPI 0 = LPI not received	RO/LH	0b
9	**TX LPI indication** 1 = TX PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO	0b
8	**RX LPI indication** 1 = RX PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO	0b
7	**Fault** 1 = Fault condition detected 0 = No fault condition detected	RO	0b
6	**Clock stop capable** 1 = The MAC may stop the clock during LPI 0 = Clock not stoppable	RO	1b
5:3	**RESERVED**	RO	-

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Bits	Description	Type	Default
2	**PCS receive link status** 1 = PCS receive link up 0 = PCS receive link down	RO	0b
1	**Low-power ability** 1 = PCS supports low-power mode 0 = PCS does not support low-power mode	RO	Note 5-11
0	**RESERVED**	RO	-

Note 5-11 This bit is a 1 if either the 1000BASE-T EEE or 100BASE-TX EEE bit in the EEE Advertisement Register is set. Otherwise it is a 0.

5.3.73 EEE QUIET TIMER REGISTER

Index (In Decimal): 3.8 Size: 16 bits

Bits	Description	Type	Default
15:0	**Quiet-Timer** 1G-EEE quieter Timer Max Value	R/W	006Eh

5.3.74 EEE UPDATE TIMER REGISTER

Index (In Decimal): 3.9 Size: 16 bits

Bits	Description	Type	Default
15:0	**Update-Timer** 1G-EEE Update Timer Max Value	R/W	005Fh

5.3.75 EEE LINK-FAIL TIMER REGISTER

Index (In Decimal): 3.10 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	R/W	-
7:0	**Link-Fail-Timer** 1G-EEE Link-Fail Timer Max Value	R/W	5Ah

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5.3.76 EEE POST-UPDATE TIMER REGISTER

Index (In Decimal): 3.11 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	R/W	-
7:0	**Post-Update-Timer** 1G-EEE Post-Update Timer Max Value	R/W	50h

5.3.77 EEE WAITWQ TIMER REGISTER

Index (In Decimal): 3.12 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	R/W	-
7:0	**WaitWQ-Timer** 1G-EEE WaitWQ Timer Max Value	R/W	5Bh

5.3.78 EEE WAKE TIMER REGISTER

Index (In Decimal): 3.13 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	R/W	-
7:0	**Wake-Timer** 1G-EEE Wake Timer Max Value	R/W	89h

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5.3.79 EEE WAKETX TIMER REGISTER

Index (In Decimal): 3.14 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	R/W	-
7:0	**WakeTX-Timer** 1G-EEE WakeTX Timer Max Value	R/W	21h

5.3.80 EEE WAKEMZ TIMER REGISTER

Index (In Decimal): 3.15 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	R/W	-
7:0	**WakeMz-Timer** 1G-EEE WakeMz Timer Max Value	R/W	6Eh

5.3.81 EEE CONTROL AND CAPABILITY REGISTER

Index (In Decimal): 3.20 Size: 16 bits

Bits	Description	Type	Default
15:14	**RESERVED**	RO	-
13	**100GBASE-R deep sleep** 1 = EEE deep sleep is supported for 100GBASE-R 0 = EEE deep sleep is not supported for 100GBASE-R **Note:** The device does not support this mode.	RO	0b
12	**100GBASE-R fast wake** 1 = EEE fast wake is supported for 100GBASE-R 0 = EEE fast wake is not supported for 100GBASE-R **Note:** The device does not support this mode.	RO	0b
11:10	**RESERVED**	RO	-
9	**40GBASE-R deep sleep** 1 = EEE deep sleep is supported for 40GBASE-R 0 = EEE deep sleep is not supported for 40GBASE-R **Note:** The device does not support this mode.	RO	0b

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Bits	Description	Type	Default
8	**40GBASE-R fast wake** 1 = EEE fast wake is supported for 40GBASE-R 0 = EEE fast wake is not supported for 40GBASE-R **Note:** The device does not support this mode.	RO	0b
7	**RESERVED**	RO	-
6	**10GBASE-KR EEE** 0 = EEE is not supported for 10GBASE-KR. 1 = EEE is supported for 10GBASE-KR. **Note:** The device does not support this mode.	RO	0b
5	**10GBASE-KX4 EEE** 0 = EEE is not supported for 10GBASE-KX4. 1 = EEE is supported for 10GBASE-KX4. **Note:** The device does not support this mode.	RO	0b
4	**10GBASE-KX EEE** 0 = EEE is not supported for 10GBASE-KX. 1 = EEE is supported for 10GBASE-KX. **Note:** The device does not support this mode.	RO	0b
3	**10GBASE-T EEE** 0 = EEE is not supported for 10GBASE-T. 1 = EEE is supported for 10GBASE-T. **Note:** The device does not support this mode.	RO	0b
2	**1000BASE-T EEE** 0 = EEE is not supported for 1000BASE-T. 1 = EEE is supported for 1000BASE-T.	RO	0b
1	**100BASE-TX EEE** 0 = EEE is not supported for 100BASE-TX. 1 = EEE is supported for 100BASE-TX.	RO	0b
0	**RESERVED**	RO	-

5.3.82 EEE WAKE ERROR COUNTER REGISTER

Index (In Decimal): 3.22 Size: 16 bits

Bits	Description	Type	Default
15:0	**EEE Wake Error Counter** This counter is cleared to zeros on read and is held to all ones on overflow.	RC	0000h

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5.3.83 EEE 100 TIMER-0 REGISTER

Index (In Decimal): 3.24 Size: 16 bits

Bits	Description	Type	Default
15:8	**TX_SLEEP_TIMER_ADD** tx_sleep_time = (5250 + TX_SLEEP_TIMER_ADD * 32) * 40ns	R/W	00h
7:1	**TX_WAKE_TIMER_ADD** tx_wake_time = (512 + TX_WAKE_TIMER_ADD * 32) * 40ns	R/W	00h
0	**RESERVED**	R/W	0b

5.3.84 EEE 100 TIMER-1 REGISTER

Index (In Decimal): 3.25 Size: 16 bits

Bits	Description	Type	Default
15:8	**RX_SLEEP_TIMER_ADD** rx_sleep_time = (6250 + RX_SLEEP_TIMER_ADD * 32) * 40ns	R/W	00h
7:1	**TX_QUIET_TIMER_ADD** tx_quiet_time = (525000 + TX_QUIET_TIMER_ADD * 8192) * 40ns	R/W	00h
0	**eee_100_test** 1 = force TX LPI	R/W	0b

5.3.85 EEE 100 TIMER-2 REGISTER

Index (In Decimal): 3.26 Size: 16 bits

Bits	Description	Type	Default
15:12	**RX_WAIT_IDLE_EXIT_TIMER_ADD** rx_wait_idle_exit_time = (16 + RX_WAIT_IDLE_EXIT_TIMER_ADD * 2) * 40ns	R/W	0h
11:8	**RX_IDLE_WAIT_TIMER_ADD** rx_idle_wait_time = (20 + RX_IDLE_WAIT_TIMER_ADD * 2) * 40ns	R/W	0h
7:0	**RX_QUIET_TIMER_ADD** rx_quiet_time = (625000 + RX_QUIET_TIMER_ADD * 4096) * 40ns	R/W	00h

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5.3.86 EEE 100 TIMER-3 REGISTER

Index (In Decimal): 3.27 Size: 16 bits

Bits	Description	Type	Default
15:8	**RX_WAKE_TIMER_ADD** rx_wake_time = (512 + RX_WAKE_TIMER_ADD * 4) * 40ns	R/W	00h
7:0	**RX_LINK_FAIL_TIMER_ADD** rx_link_fail_time = (2500 + RX_LINK_FAIL_TIMER_ADD * 16) * 40ns	R/W	00h

5.3.87 EEE ADVERTISEMENT REGISTER

Index (In Decimal): 7.60 Size: 16 bits

Bits	Description	Type	Default
15:14	**RESERVED**	R/W	-
13	**100GBASE-CR4 EEE** 0 = Do not advertise EEE capability for 100GBASE-CR4 deep sleep 1 = Advertise EEE capability for 100GBASE-CR4 deep sleep **Note:** The device does not support this mode. This bit is not used.	R/W	0b
12	**100GBASE-KR4 EEE** 0 = Do not advertise EEE capability for 100GBASE-KR4 deep sleep 1 = Advertise EEE capability for 100GBASE-KR4 deep sleep **Note:** The device does not support this mode. This bit is not used.	R/W	0b
11	**100GBASE-KP4 EEE** 0 = Do not advertise EEE capability for 100GBASE-KP4 deep sleep 1 = Advertise EEE capability for 100GBASE-KP4 deep sleep **Note:** The device does not support this mode. This bit is not used.	R/W	0b
10	**100GBASE-CR10 EEE** 0 = Do not advertise EEE capability for 100GBASE-CR10 deep sleep 1 = Advertise EEE capability for 100GBASE-CR10 deep sleep **Note:** The device does not support this mode.	R/W	0b
9	**RESERVED**	R/W	-
8	**40GBASE-CR4 EEE** 0 = Do not advertise EEE capability for 40GBASE-CR4 deep sleep 1 = Advertise EEE capability for 40GBASE-CR4 deep sleep **Note:** The device does not support this mode.	R/W	0b

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Bits	Description	Type	Default
7	**40GBASE-KR4 EEE** 0 = Do not advertise EEE capability for 40GBASE-KR4 deep sleep 1 = Advertise EEE capability for 40GBASE-KR4 deep sleep **Note:** The device does not support this mode.	R/W	0b
6	**10GBASE-KR EEE** 0 = Do not advertise EEE capability for 10GBASE-KR 1 = Advertise EEE capability for 10GBASE-KR **Note:** The device does not support this mode.	R/W	0b
5	**10GBASE-KX4 EEE** 0 = Do not advertise EEE capability for 10GBASE-KX4 1 = Advertise EEE capability for 10GBASE-KX4 **Note:** The device does not support this mode.	R/W	0b
4	**10GBASE-KX EEE** 0 = Do not advertise EEE capability for 10GBASE-KX 1 = Advertise EEE capability for 10GBASE-KX **Note:** The device does not support this mode.	R/W	0b
3	**10GBASE-T EEE** 0 = Do not advertise EEE capability for 10GBASE-T 1 = Advertise EEE capability for 10GBASE-T **Note:** The device does not support this mode.	R/W	0b
2	**1000BASE-T EEE** 0 = Do not advertise EEE capability for 1000BASE-T 1 = Advertise EEE capability for 1000BASE-T	R/W	1b
1	**100BASE-TX EEE** 0 = Do not advertise EEE capability for 100BASE-TX. 1 = Advertise EEE capability for 100BASE-TX.	R/W	1b
0	**RESERVED**	R/W	-

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5.3.88 EEE LINK PARTNER ABILITY REGISTER

Index (In Decimal): 7.61 Size: 16 bits

Bits	Description	Type	Default
15:11	**RESERVED**	R/W	-
10	**100GBASE-CR10 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 100GBASE-CR10. 1 = Link partner advertises EEE deep sleep capability for 100GBASE-CR10. **Note:** This device does not support this mode.	RO	0b
9	**RESERVED**	RO	0b
8	**40GBASE-CR4 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 40GBASE-CR4. 1 = Link partner advertises EEE deep sleep capability for 40GBASE-CR4. **Note:** This device does not support this mode.	RO	0b
7	**40GBASE-KR4 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 40GBASE-KR4. 1 = Link partner advertises EEE deep sleep capability for 40GBASE-KR4. **Note:** This device does not support this mode.	RO	0b
6	**10GBASE-KR EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KR. 1 = Link partner advertises EEE capability for 10GBASE-KR. **Note:** This device does not support this mode.	RO	0b
5	**10GBASE-KX4 EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KX4. 1 = Link partner advertises EEE capability for 10GBASE-KX4. **Note:** This device does not support this mode.	RO	0b
4	**10GBASE-KX EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KX. 1 = Link partner advertises EEE capability for 10GBASE-KX. **Note:** This device does not support this mode.	RO	0b
3	**10GBASE-T EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-T. 1 = Link partner advertises EEE capability for 10GBASE-T. **Note:** This device does not support this mode.	RO	0b
2	**1000BASE-T EEE** 0 = Link partner does not advertise EEE capability for 1000BASE-T. 1 = Link partner advertises EEE capability for 1000BASE-T.	RO	0b
1	**100BASE-TX EEE** 0 = Link partner does not advertise EEE capability for 100BASE-TX. 1 = Link partner advertises EEE capability for 100BASE-TX.	RO	0b
0	**RESERVED**	RO	-

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5.3.89 EEE LINK PARTNER ABILITY OVERRIDE REGISTER

Index (In Decimal): 7.62 Size: 16 bits

Bits	Description	Type	Default
15	**LP AN Override** 0 = Use Link partner AN results 1 = Use bits 10:0 as Link partner results	R/W	0b
14:11	**RESERVED**	R/W	-
10	**100GBASE-CR10 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 100GBASE-CR10. 1 = Link partner advertises EEE deep sleep capability for 100GBASE-CR10. **Note:** This device does not support this mode.	R/W	0b
9	**RESERVED**	R/W	-
8	**40GBASE-CR4 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 40GBASE-CR4. 1 = Link partner advertises EEE deep sleep capability for 40GBASE-CR4. **Note:** This device does not support this mode.	R/W	0b
7	**40GBASE-KR4 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 40GBASE-KR4. 1 = Link partner advertises EEE deep sleep capability for 40GBASE-KR4. **Note:** This device does not support this mode.	R/W	0b
6	**10GBASE-KR EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KR. 1 = Link partner advertises EEE capability for 10GBASE-KR. **Note:** This device does not support this mode.	R/W	0b
5	**10GBASE-KX4 EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KX4. 1 = Link partner advertises EEE capability for 10GBASE-KX4. **Note:** This device does not support this mode.	R/W	0b
4	**10GBASE-KX EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KX. 1 = Link partner advertises EEE capability for 10GBASE-KX. **Note:** This device does not support this mode.	R/W	0b
3	**10GBASE-T EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-T. 1 = Link partner advertises EEE capability for 10GBASE-T. **Note:** This device does not support this mode.	R/W	0b
2	**1000BASE-T EEE** 0 = Link partner does not advertise EEE capability for 1000BASE-T. 1 = Link partner advertises EEE capability for 1000BASE-T.	R/W	0b

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Bits	Description	Type	Default
1	**100BASE-TX EEE** 0 = Link partner does not advertise EEE capability for 100BASE-TX. 1 = Link partner advertises EEE capability for 100BASE-TX.	R/W	0b
0	**RESERVED**	R/W	-

5.3.90 EEE MESSAGE CODE REGISTER

Index (In Decimal): 7.63 Size: 16 bits

Bits	Description	Type	Default
15:11	**RESERVED**	R/W	-
10:0	**EEE_message_code** Programmable EEE specific message code for AN	R/W	00Ah

5.3.91 XTAL CONTROL REGISTER

Index (In Decimal): 28.1 Size: 16 bits

Bits	Description	Type	Default
15:14	**RESERVED**	R/W	-
13	**XTAL Disable** Crystal oscillator disable 0 = XTAL enabled 1 = XTAL disabled	R/W	0b
12:0	**RESERVED**	R/W	-

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5.3.92 AFED CONTROL REGISTER

Index (In Decimal): 28.9 Size: 16 bits

Bits	Description	Type	Default
15:10	**RESERVED**	RO	-
9	**p_cat3** 0 = cat5 parameter for 10 Base-T TX 1 = cat3 parameter for 10 Base-T TX	R/W	0b
8:0	**RESERVED**	RO	-

5.3.93 LDO CONTROL REGISTER

Index (In Decimal): 28.14 Size: 16 bits

Bits	Description	Type	Default
15	**LDO enable** turn off VDD regulator by software 1 = off 0 = on	R/W	0b
14:0	**RESERVED**	R/W	-

5.3.94 EDPD CONTROL REGISTER

Index (In Decimal): 28.36 Size: 16 bits

Bits	Description	Type	Default
15:6	**RESERVED**	RO	-
5:4	**p_edpd_mask_timer[1:0]** 00 = EDPD mask for 2.6us 01 = 3.2us 10 = 4.0us 11 = 5.0us	R/W	00b
3:2	**p_edpd_timer[1:0]** 00 = EDPD pulse separation for 1s 01 = 1.3s 10 = 1.6s 11 = 1.9s	R/W	00b

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Bits	Description	Type	Default
1	**p_EDPD_random_dis** 1 = use edpd_timer value as EDPD pulse separation selection 0 = use random seed value as EDPD pulse separation selection	R/W	0b
0	**EDPD Mode Enable** 0 = EDPD mode disabled 1 = EDPD mode enabled	R/W	0b

5.3.95 EMITX CONTROL REGISTER

Index (In Decimal): 28.37 Size: 16 bits

Bits	Description	Type Note 5-12	Default Note 5-12
15:2	**RESERVED**	RO	-
1:0	**p_scale**	RO / R/W	00b / 01b

Note 5-12 The type and default value depends on the Quiet-WIRE Enable bit in MMD31 Register 19. The values are listed as Quiet-WIRE Enable = 0 / Quiet-WIRE Enable = 1.

5.3.96 EMITX COEFFICIENT REGISTERS

Index (In Decimal): 28.38-52 Size: 16 bits

Register	Bits	Description	Type Note 5-13	Default Note 5-13
38	15	**RESERVED**	RO	-
	14:8	**p_coeff1**	RO / R/W	31d / 14d
	7	**RESERVED**	RO	-
	6:0	**p_coeff0**	RO / R/W	15d / 3d
39	15	**RESERVED**	RO	-
	14:8	**p_coeff3**	RO / R/W	31d / 48d
	7	**RESERVED**	RO	-
	6:0	**p_coeff2**	RO / R/W	31d / 32d

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Register	Bits	Description	Type Note 5-13	Default Note 5-13
40	15	**RESERVED**	RO	-
	14:8	**p_coeff5**	RO / R/W	0d / 46d
	7	**RESERVED**	RO	-
	6:0	**p_coeff4**	RO / R/W	16d / 54d
41	15	**RESERVED**	RO	-
	14:8	**p_coeff7**	RO / R/W	0d / 11d
	7	**RESERVED**	RO	-
	6:0	**p_coeff6**	RO / R/W	0d / 28d
42	15	**RESERVED**	RO	-
	14:8	**p_coeff9**	RO / R/W	0d / 126d (-2d)
	7	**RESERVED**	RO	-
	6:0	**p_coeff8**	RO / R/W	0d / 1d
43	15	**RESERVED**	RO	-
	14:8	**p_coeff11**	RO / R/W	0d / 127d (-1d)
	7	**RESERVED**	RO	-
	6:0	**p_coeff10**	RO / R/W	0d / 126d (-2d)
44	15	**RESERVED**	RO	-
	14:8	**p_coeff13**	R/W / R/W	0d / 0d
	7	**RESERVED**	RO	-
	6:0	**p_coeff12**	R/W / R/W	0d / 0d
45	15	**RESERVED**	RO	-
	14:8	**p_coeff15**	R/W / R/W	0d / 0d
	7	**RESERVED**	RO	-
	6:0	**p_coeff14**	R/W / R/W	0d / 0d
46	15	**RESERVED**	RO	-
	14:8	**p_coeff17**	R/W / R/W	0d / 0d
	7	**RESERVED**	RO	-
	6:0	**p_coeff16**	R/W / R/W	0d / 0d

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Register	Bits	Description	Type Note 5-13	Default Note 5-13
47	15	**RESERVED**	RO	-
	14:8	**p_coeff19**	R/W / R/W	0d / 0d
	7	**RESERVED**	RO	-
	6:0	**p_coeff18**	R/W / R/W	0d / 0d
48	15	**RESERVED**	RO	-
	14:8	**p_coeff21**	R/W / R/W	0d / 0d
	7	**RESERVED**	RO	-
	6:0	**p_coeff20**	R/W / R/W	0d / 0d
49	15	**RESERVED**	RO	-
	14:8	**p_coeff23**	R/W / R/W	0d / 0d
	7	**RESERVED**	RO	-
	6:0	**p_coeff22**	R/W / R/W	0d / 0d
50	15	**RESERVED**	RO	-
	14:8	**p_coeff25**	R/W / R/W	0d / 0d
	7	**RESERVED**	RO	-
	6:0	**p_coeff24**	R/W / R/W	0d / 0d
51	15	**RESERVED**	RO	-
	14:8	**p_coeff27**	R/W / R/W	0d / 0d
	7	**RESERVED**	RO	-
	6:0	**p_coeff26**	R/W / R/W	0d / 0d
52	15	**RESERVED**	RO	-
	14:8	**p_coeff29**	R/W / R/W	0d / 0d
	7	**RESERVED**	RO	-
	6:0	**p_coeff28**	R/W / R/W	0d / 0d

Note 5-13 The type and default value depends on the Quiet-WIRE Enable bit in MMD31 Register 19. The values are listed as Quiet-WIRE Enable = 0 / Quiet-WIRE Enable = 1.

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5.3.97 MMD31 REGISTER 19

Index (In Decimal): 31.19 Size: 16 bits

Bits	Description	Type	Default
15:11	**RESERVED**	RO	-
10	**Quiet-WIRE Enable** 1 = Enable Quiet-WIRE® 0 = Disable Quiet-WIRE®	R/W	0b
9:0	**RESERVED**	RO	-

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6.0 OPERATIONAL CHARACTERISTICS

6.1 Absolute Maximum Ratings*

Supply Voltage (V_{IN})
(DVDDL, AVDDL, AVDDL_PLL) ..... –0.5V to +1.8V
(AVDDH) ..... –0.5V to +5.0V
(DVDDH) ..... –0.5V to +5.0V
Input Voltage (all inputs) ..... –0.5V to +5.0V
Output Voltage (all outputs) ..... –0.5V to +5.0V
Lead Temperature (soldering, 10s) ..... +260°C
Storage Temperature (T_S) ..... –55°C to +150°C
HBM ESD Performance ..... +/-5kV

*Exceeding the absolute maximum rating may damage the device. Stresses greater than the absolute maximum rating may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

6.2 Operating Ratings**

Supply Voltage
(DVDDL, AVDDL, AVDDL_PLL) ..... +1.140V to +1.320V
(AVDDH @ 3.3V) (Note 6-1) ..... +3.135V to +3.630V
(AVDDH @ 2.5V) ..... +2.375V to +2.750V
(DVDDH @ 3.3V) (Note 6-2) ..... +3.135V to +3.630V
(DVDDH @ 2.5V) ..... +2.375V to +2.750V
(DVDDH @ 1.8V) ..... +1.710V to +1.980V
Input voltage (all inputs) ..... -0.3 V to +3.63 V
Output voltage (all outputs) ..... -0.3 V to +3.63 V
Ambient Temperature
(T_A Commercial: KSZ9131RNXC) ..... 0°C to +70°C
(T_A Industrial: KSZ9131RNXI) ..... –40°C to +85°C
(T_A Automotive: KSZ9131RNXU) ..... –40°C to +85°C
(T_A Automotive: KSZ9131RNXV) ..... –40°C to +105°C
Maximum Junction Temperature (T_J max.) ..... +125°C

**The device is not guaranteed to function outside its operating ratings.

Note 6-1 Automotive Grade 2 temperature range requires +2.5V.

Note 6-2 Automotive Grade 2 temperature range requires +1.8V or +2.5V.

Note: Do not drive input signals without power supplied to the device.

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6.3 Package Thermal Specifications

Thermal parameters are measured or estimated for devices with the ground soldered to thermal vias in a multilayer 2S2P PCB per JESD51. Thermal resistance is measured from the die to the ambient air. The values provided are based on the package body, die size, maximum power consumption.

TABLE 6-1: PACKAGE THERMAL PARAMETERS

Parameter	Symbol	Value	Units	Notes
Junction-to-Ambient	Θ_{JA}	31	°C/W	0 Meters/second
		27	°C/W	1 Meters/second
		24	°C/W	2.5 Meters/second
Junction-to-Top-of-Package	Ψ_{JT}	0.3	°C/W	0 Meters/second
Junction-to-Board	Ψ_{JB}	16	°C/W	0 Meters/second
Junction-to-Case	Θ_{JC}	3.5	°C/W	-
Junction-to-Board	Θ_{JB}	17	°C/W	-
Maximum Power Dissipation	P_{MAX}	663	mW	1000BASE-T Traffic, 3.3V I/O

Use the following formulas to calculate the junction temperature:

$$T_J = P \times \Theta_{JA} + T_A$$

$$T_J = P \times \Psi_{JT} + T_T$$

$$T_J = P \times \Theta_{JC} + T_C$$

TABLE 6-2: PACKAGE THERMALS LEGEND

Symbol	Description
T_J	Junction temperature
P	Power dissipated
Θ_{JA}	Junction-to-ambient-temperature
Θ_{JC}	Junction-to-top-of-package
Ψ_{JT}	Junction-to-bottom-of-case
T_A	Ambient temperature
T_C	Temperature of the bottom of the case
T_T	Temperature of the top of the case

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6.4 Power Consumption

This section details the device power measurements taken over various operating conditions. Unless otherwise noted, all measurements were taken with power supplies at nominal values. Refer to Section 4.17, Power Management for a description of the power down modes.

TABLE 6-3: POWER CONSUMPTION

Mode	Typical Power (mW) DVDDH=3.3V, AVDDH=3.3V	Typical Power (mW) DVDDH=2.5V, AVDDH=2.5V
1000BASE-T Traffic (RGMII)	623.7	489.1
100BASE-TX Traffic (RGMII)	270.9	199.1
10BASE-T Traffic (RGMII)	144.9	105.3
10BASE-Te Traffic (RGMII)	141.6	95.3
Chip Power-Down (CPD)	3.4	3.4
Energy-Detect Power-Down (EDPD)	63.9	21.2
EEE 1000BASE-T Idle	280.5	175.3
EEE 100BASE-TX Idle	119.1	81.3
Normal Operation (No Link)	175.8	128.6
RESET	61.2	40.9
Software Power-Down (SPD)	26.4	12.5
Max Power (85°C w/AVDDH/DVDDH +10°)	908	780
Max Power (105°C w/AVDDH/DVDDH +10°)	911	801.9

6.5 DC Specifications

TABLE 6-4: NON-VARIABLE I/O DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Notes
ICLK Type Input Buffer						Note 6-3
Low Input Level	V_{IL}			0.5	V	
High Input Level	V_{IH}	2.0			V	
Input Leakage	I_{IH}	-10		10	µA	

Note 6-3 XI can optionally be driven from a 25 MHz single-ended clock oscillator to which these specifications apply.

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TABLE 6-5: VARIABLE I/O DC ELECTRICAL CHARACTERISTICS DVDDH = 3.3/2.5/1.8V

Parameter	Symbol	Min	Typ	Max	Units	Notes
VI Type Input Buffer						
Low Input Level	V_{IL}			0.9/0.9/0.6	V	
High Input Level	V_{IH}	2.1/1.7/1.3			V	
Input Leakage (V_{IN} = VSS or DVDDH)	I_{IH}	-10		10	µA	Note 6-4
Input Capacitance (generic guess)	C_{IN}			3	pF	
Effective Pull-Up Resistance (V_{IN} = VSS)	R_{PU}		44/59/96		KΩ	
Effective Pull-Down Resistance (V_{IN} = DVDDH)	R_{PD}		47/58/86		KΩ	
VIS Type Input Buffer						
Low Input Level	V_{IL}			0.9/0.9/0.6	V	
High Input Level	V_{IH}	2.1/1.7/1.3			V	
Schmitt Falling Trip Point	V_{T-}	1.0/0.8/0.6	1.2/1.0/0.7	1.5/1.1/0.8	V	
Schmitt Rising Trip Point	V_{T+}	1.5/1.2/0.9	1.7/1.4/1.1	1.9/1.6/1.3	V	
Schmitt Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	0.4/0.3/0.3	0.5/0.4/0.4	0.6/0.5/0.5	V	
Input Leakage (V_{IN} = VSS or DVDDH)	I_{IH}	-10		10	µA	Note 6-4
Input Capacitance (generic guess)	C_{IN}			3	pF	
Effective Pull-Up Resistance (V_{IN} = VSS)	R_{PU}		44/59/96		KΩ	
Effective Pull-Down Resistance (V_{IN} = DVDDH)	R_{PD}		47/58/86		KΩ	
VO8 Type Buffer						
Low Output Level	V_{OL}			0.4/0.4/0.2	V	I_{OL} = -8/-8/-6 mA I_{OH} = -8/-8/-6 mA
High Output Level	V_{OH}	2.4/1.9/1.5			V	Note 6-4
Output Tri-State Leakage	I_{OZ}	-10		10	µA	

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TABLE 6-5: VARIABLE I/O DC ELECTRICAL CHARACTERISTICS DVDDH = 3.3/2.5/1.8V

Parameter	Symbol	Min	Typ	Max	Units	Notes
VOD8 Type Buffer						
Low Output Level	V_{OL}			0.4/0.4/0.2	V	I_{OL} = -8/-8/-6 mA Note 6-4
Output Tri-State Leakage	I_{OZ}	-10		10	µA	
VO24 Type Buffer						
Low Output Level	V_{OL}			0.4/0.4/0.2	V	I_{OL} = -24/-24/-14 mA
High Output Level	V_{OH}	2.4/1.9/1.5			V	I_{OH} = 24/-24/-14 mA
Output Tri-State Leakage	I_{OZ}	-10		10	µA	Note 6-4

Note 6-4 This specification applies to all inputs without pull-ups or pull-downs and three-stated bi-directional pins.

TABLE 6-6: 1000BASE-T TRANSCEIVER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Notes
Peak Differential Output Voltage IEEE 802.3 clause 40.6.1.2.1	V_{OP}	670		820	mV	Note 6-5
Signal Amplitude Symmetry IEEE 802.3 clause 40.6.1.2.1	V_{SS}			1	%	Note 6-5
Signal Scaling IEEE 802.3 clause 40.6.1.2.1	V_{SC}			2	%	Note 6-6
Output Droop IEEE 802.3 clause 40.6.1.2.2	V_{OD}	73.1			%	Note 6-5
Transmission Distortion IEEE 802.3 clause 40.6.1.2.4				10	mV	Note 6-7

Note 6-5 IEEE 802.ab Test Mode 1

Note 6-6 From 1/2 of average V_{OP}, Test Mode 1

Note 6-7 IEEE 802.ab distortion processing

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TABLE 6-7: 100BASE-TX TRANSCEIVER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Notes
Peak Differential Output Voltage ANSI X3.263 clause 9.1.2.2	V_{OUT}	±0.95		±1.05	V	Note 6-8
Signal Amplitude Symmetry ANSI X3.263 clause 9.1.4	V_{SS}			2	%	Note 6-8
Signal Rise and Fall Time ANSI X3.263 clause 9.1.6	T_{RF}	3		5	ns	Note 6-8
Rise and Fall Symmetry ANSI X3.263 clause 9.1.6	T_{RFS}	0		0.5	ns	Note 6-8
Duty Cycle Distortion ANSI X3.263 clause 9.1.8	D_{CD}			±0.25	ns	Note 6-9
Overshoot and Undershoot ANSI X3.263 clause 9.1.3	V_{OS}			5	%	
Output Jitter ANSI X3.263 clause 9.1.9			0.7	1.4	ns	Note 6-10
Reference Voltage of ISET (using 6.04kΩ - 1% resistor)	V_{SET}		0.61		V	

Note 6-8 Measured at line side of transformer, line replaced by 100Ω (+/- 1%) resistor.

Note 6-9 Offset from 16ns pulse width at 50% of pulse peak.

Note 6-10 Peak to Peak, measured differentially.

TABLE 6-8: 10BASE-T/10BASE-Te TRANSCEIVER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter Peak Differential Output Voltage IEEE 802.3 clause 14.3.1.2.1	V_{OUT} 10BASE-T	2.2	2.5	2.8	V	Note 6-11
	V_{OUT} 10BASE-Te	1.54		1.96	V	Note 6-11
Output Jitter IEEE 802.3 clause 14.3.1.2.3			1.8	3.5	ns	Note 6-12
Signal Rise and Fall Time	T_{RF}		25		ns	
Receiver Differential Squelch Threshold IEEE 802.3 clause 14.3.1.3.2	V_{DS}	300	400		mV	Note 6-13

Note 6-11 Measured with 100Ω resistive load.

Note 6-12 Measured differentially following the twisted-pair model with a 100Ω resistive load.

Note 6-13 5MHz square wave.

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TABLE 6-9: LDO CONTROLLER

Parameter	Symbol	Min	Typ	Max	Units	Notes
Output drive range for LDO_O to gate input of P-channel MOSFET	V_{LDO_O}	1.2		3.11	V	AVDDH = 3.3V for MOSFET source voltage
		1.2		2.0	V	AVDDH = 2.5V for MOSFET source voltage
Output of P-channel MOSFET		1.23	1.25	1.32	V	

TABLE 6-10: POR THRESHOLDS

POR	Conditions	Rising threshold volts			Falling threshold volts			Hysteresis millivolts		
		min	typ	max	min	typ	max	min	typ	max
1.2V Ethernet PHY Analog (AVDDL)	AVDDH = 2.5V	0.73	0.76	0.80	0.64	0.68	0.80	0	80	114
	AVDDH = 3.3V	0.73	0.76	0.82	0.63	0.70	0.82	0	65	120
2.5V / 3.3V Ethernet PHY Analog (AVDDH)		1.9	2.1	2.2	1.9	2.0	2.1	65	110	145
3.3V / 2.5V / 1.8V Variable I/O (DVDDH)		1.40	1.48	1.57	1.35	1.42	1.51	45	58	73

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6.6 AC Specifications

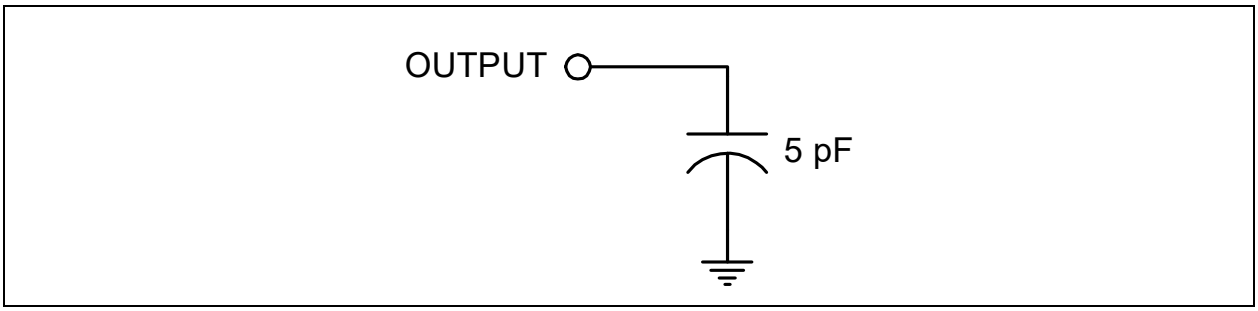
This section details the various AC timing specifications of the device.

Note:	The RGMII timing adheres to or exceeds the HP RGMII Specification Version 2.0. Refer to this specification for additional RGMII timing information.

6.6.1 EQUIVALENT TEST LOAD

Output timing specifications assume a 5pF equivalent test load, unless otherwise noted, as illustrated in Figure 6-1.

FIGURE 6-1: OUTPUT EQUIVALENT TEST LOAD



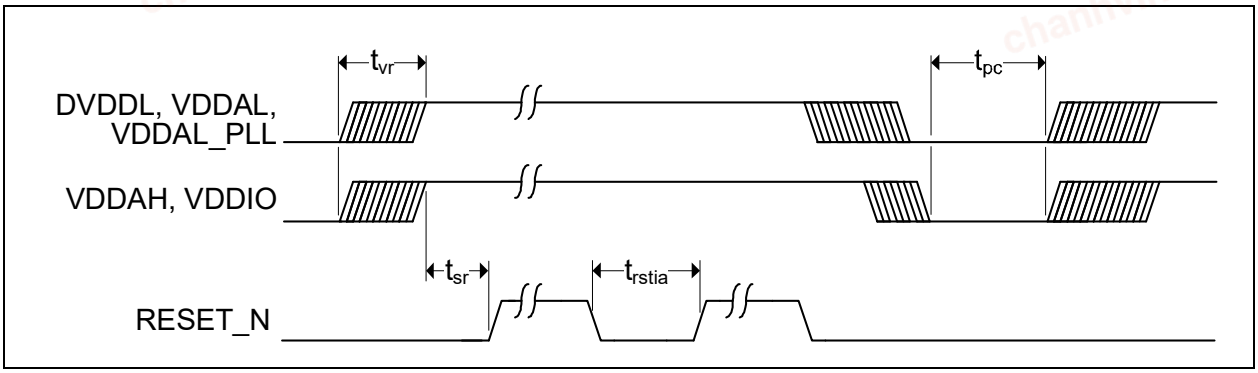
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6.6.2 POWER SEQUENCE TIMING

These diagrams illustrates the device power sequencing requirements.

FIGURE 6-2: POWER SEQUENCE TIMING INTERNAL REGULATORS



The recommended power-up sequence is to have the transceiver (AVDDH) and digital I/O (DVDDH) voltages power up before the 1.2V core (DVDDL, AVDDL, AVDDL_PLL) voltage. If the 1.2V core must power up first, the maximum lead time for the 1.2V core voltage with respect to the transceiver and digital I/O voltages should be 200 µs.

There is no power sequence requirement between transceiver (AVDDH) and digital I/O (DVDDH) power rails.

The power-up waveforms must be monotonic for all supply voltages to the device.

RESET_N must be held asserted following stable voltages for the minimum period specified and if re-asserted, for the minimum period specified.

The recommended power-down sequence is to have the 1.2V core voltage power-down before powering down the transceiver and digital I/O voltages.

Before the next power-up cycle, all supply voltages to the device should reach less than 0.4V and there should be a minimum wait time of 150 ms from power-off to power-on.

TABLE 6-11: POWER SEQUENCING TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{vr}	Supply voltages rise time (must be monotonic)			200	µs
t_{sr}	Stable supply voltages to de-assertion of reset	10			ms
t_{rstia}	RESET_N input assertion time	1			µs
t_{pc}	Supply voltages cycle off-to-on time	150			ms

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6.6.3 RESET PIN CONFIGURATION STRAP TIMING

Figure 6-3 illustrates the RESET_N timing requirements and its relation to the configuration straps. RESET_N must be asserted for the minimum period specified.

FIGURE 6-3: RESET_N CONFIGURATION STRAP TIMING

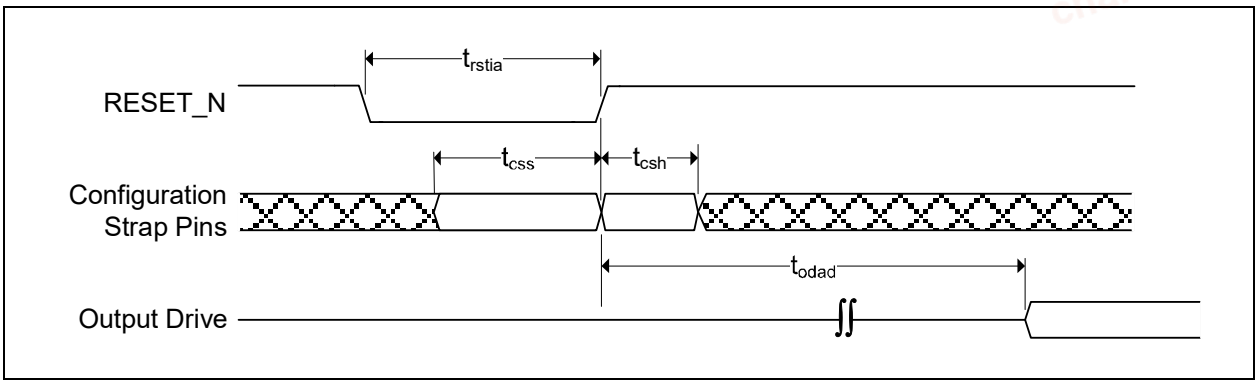


TABLE 6-12: RESET_N CONFIGURATION STRAP TIMING

Symbol	Description	Min	Typ	Max	Units
t_{rstia}	RESET_N input assertion time	1			µs
t_{css}	Configuration strap setup before RESET_N de-assertion	5			ns
t_{csh}	Configuration strap hold after RESET_N de-assertion	5			ns
t_{odad}	Output drive after RESET_N de-assertion	1			us

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6.6.4 RGMII TIMING

This section specifies the RGMII interface transmit and receive timing. By default the device supports the Internal Delay mode specified by version 2.0 of the RGMII specification.

Note:

- All RGMII timing specifications assume a point-to-point test circuit as defined in Figure 3 of the RGMII specification 2.0.
- The below timing parameters assume default values for the following registers:
  Clock Invert and Control Signal Pad Skew Register
  RGMII RX Data Pad Skew Register
  RGMII TX Data Pad Skew Register
  Clock Pad Skew Register
  RX DLL Control Register
  TX DLL Control Register

6.6.4.1 TXC Internal Delay Disabled Timing (RGMII ID Mode - MAC provides delayed clock)

FIGURE 6-4: TXC INTERNAL DELAY DISABLED (RGMII ID MODE) TIMING

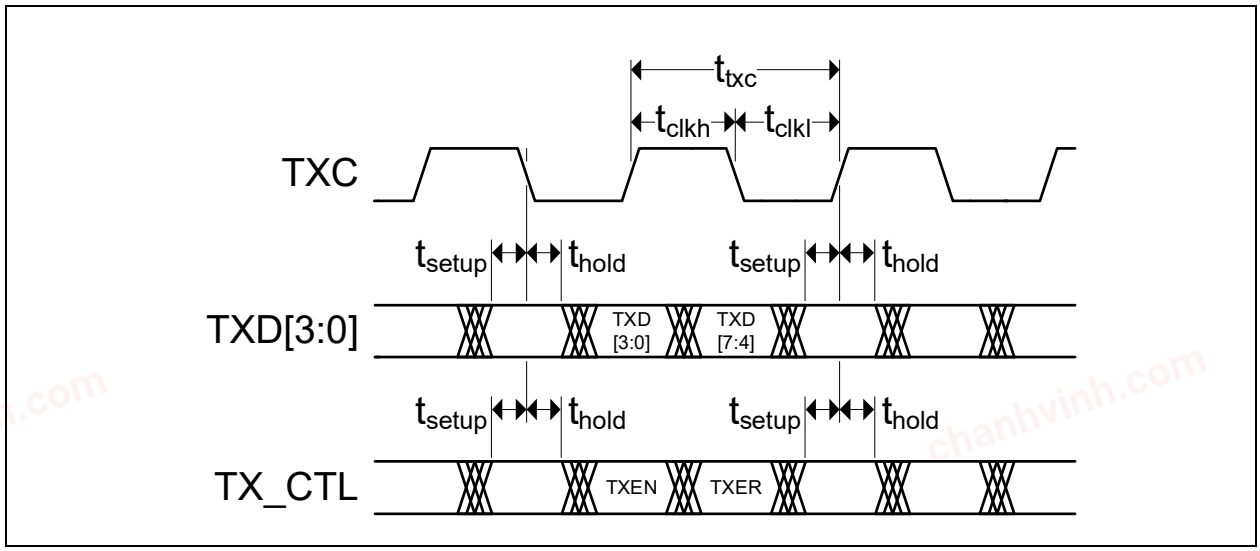


TABLE 6-13: RGMII TXC INTERNAL DELAY DISABLED (RGMII ID MODE) TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{txc}	TXC period	Note 6-14	Note 6-15	Note 6-16	ns
t_{clkh}	TXC high time	Note 6-17	50	Note 6-18	%
t_{clkl}	TXC low time	Note 6-17	50	Note 6-18	%
t_{setup}	TXD[3:0], TX_CTL setup time to edge of TXC (at inputs)	0.8	2.0		ns
t_{hold}	TXD[3:0], TX_CTL hold time after edge of TXC (at inputs)	0.8	2.0		ns

Note 6-14 7.2ns for 1000BASE-T operation, 36ns for 100BASE-TX operation, 360ns for 10BASE-T operation. Minimum limits are non-sustainable long term.

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Note 6-15 8ns for 1000BASE-T operation, 40ns for 100BASE-TX operation, 400ns for 10BASE-T operation.

Note 6-16 8.8ns for 1000BASE-T operation, 44ns for 100BASE-TX operation, 440ns for 10BASE-T operation. Maximum limits are non-sustainable long term.

Note 6-17 45% for 1000BASE-T operation, 40% for 100BASE-TX or 10BASE-T operation.

Note 6-18 55% for 1000BASE-T operation, 60% for 100BASE-TX or 10BASE-T operation.

6.6.4.2 RXC Internal Delay Enabled Timing (RGMII ID Mode - PHY provides delayed clock)

FIGURE 6-5: RXC INTERNAL DELAY ENABLED (RGMII ID MODE) TIMING

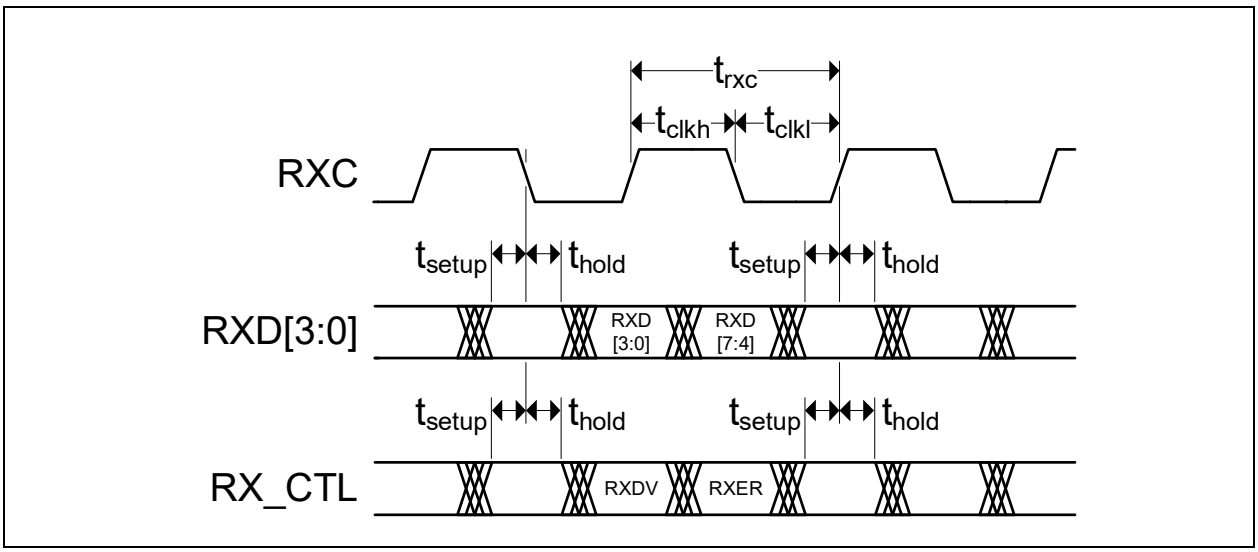


TABLE 6-14: RGMII RXC INTERNAL DELAY ENABLED (RGMII ID MODE) TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{rxc}	RXC period	Note 6-19	Note 6-20	Note 6-21	ns
t_{clkh}	RXC high time	Note 6-22	50	Note 6-23	%
t_{clkl}	RXC low time	Note 6-22	50	Note 6-23	%
t_{setup}	RXD[3:0], RX_CTL setup to edge of RXC (at outputs)	1.2	2.0		ns
t_{hold}	RXD[3:0], RX_CTL hold from edge of RXC (at outputs)	1.2	2.0		ns

Note 6-19 7.2ns for 1000BASE-T operation, 36ns for 100BASE-TX operation, 360ns for 10BASE-T operation. Minimum limits are non-sustainable long term.

Note 6-20 8ns for 1000BASE-T operation, 40ns for 100BASE-TX operation, 400ns for 10BASE-T operation.

Note 6-21 8.8ns for 1000BASE-T operation, 44ns for 100BASE-TX operation, 440ns for 10BASE-T operation. Maximum limits are non-sustainable long term.

Note 6-22 45% for 1000BASE-T operation, 40% for 100BASE-TX or 10BASE-T operation.

Note 6-23 55% for 1000BASE-T operation, 60% for 100BASE-TX or 10BASE-T operation.

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6.6.5 AUTO-NEGOTIATION FAST LINK PULSE (FLP) TIMING

FIGURE 6-6: AUTO-NEGOTIATION FAST LINK PULSE (FLP) TIMING

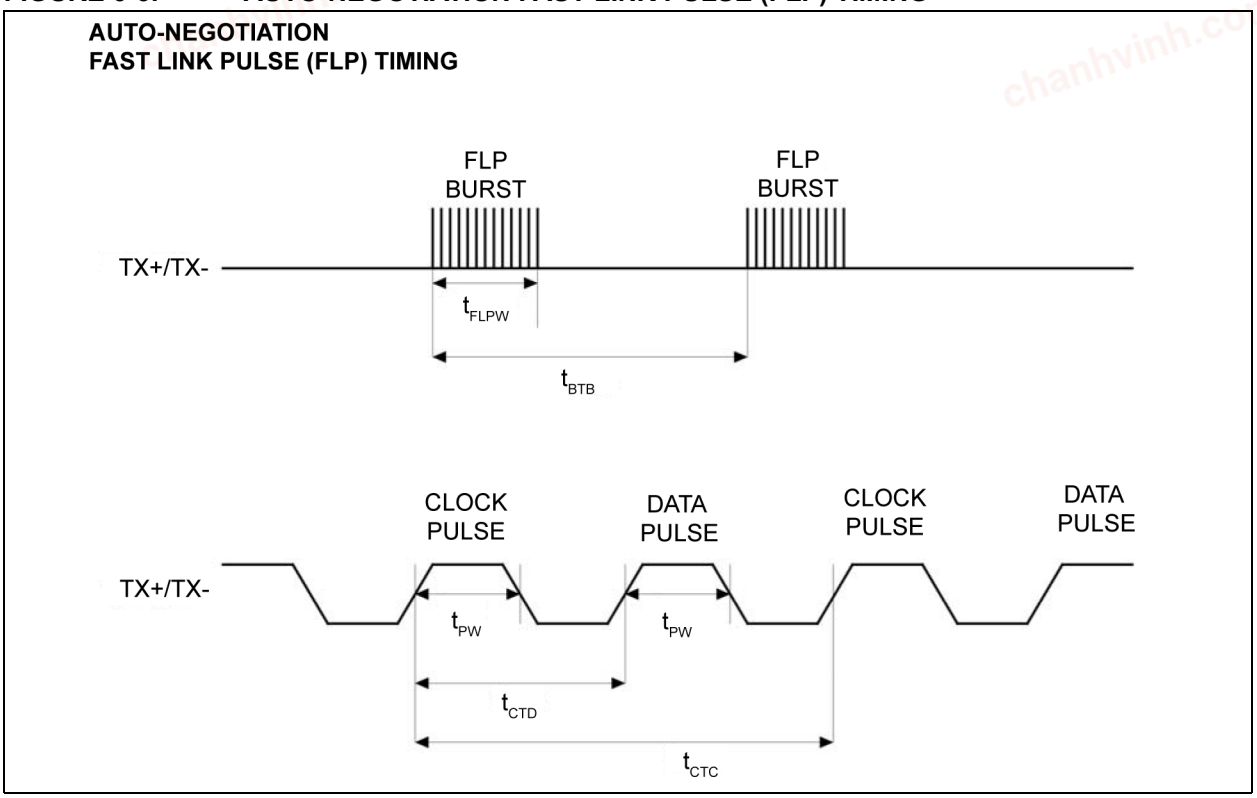


TABLE 6-15: AUTO-NEGOTIATION FAST LINK PULSE (FLP) TIMING PARAMETERS

Symbol	Description	Min	Typ	Max	Units
t_{BTB}	FLP burst to FLP burst	8	16	24	ms
t_{FLPW}	FLP burst width		2		ms
t_{PW}	Clock/Data pulse width		100		ns
t_{CTD}	Clock pulse to data pulse	55.5	64	69.5	µs
t_{CTC}	Clock pulse to clock pulse	111	128	139	µs
	Number of clock/data pulses per FLP burst	17		33	

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6.6.6 MDC/MDIO TIMING

This section specifies the MDC/MDIO timing of the device.

FIGURE 6-7: MDC/MDIO TIMING

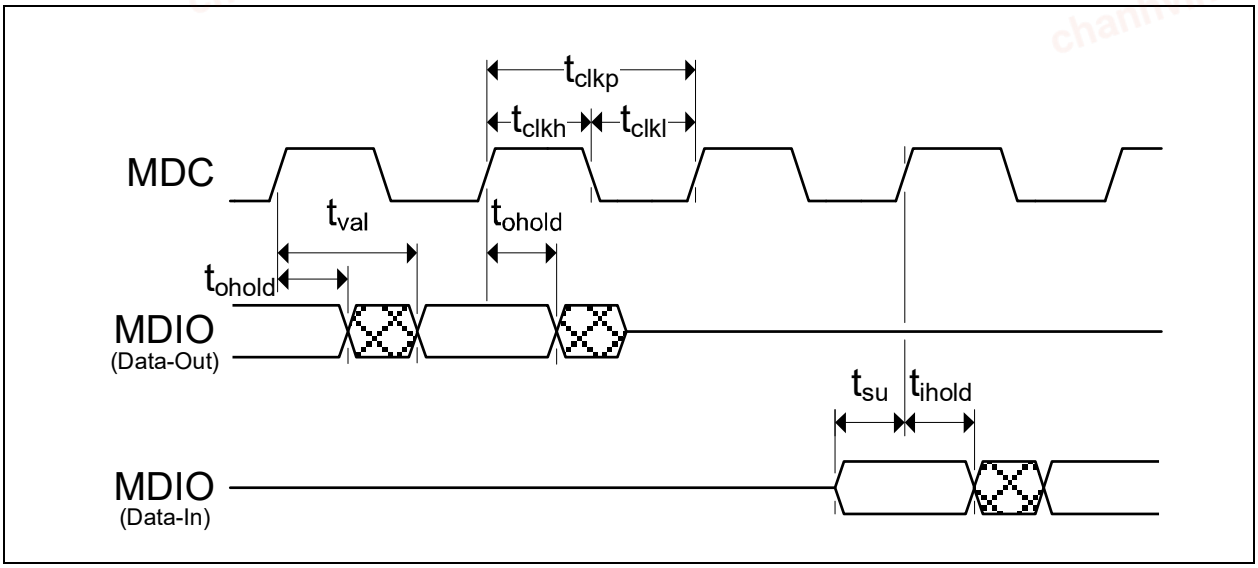


TABLE 6-16: MDC/MDIO TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{clkp}	MDC period	120 Note 6-24	400	Note 6-25	ns
t_{clkh}	MDC high time	40			ns
t_{clkl}	MDC low time	40			ns
t_{val}	MDIO (read from PHY) output valid from rising MDIO of MDC			80	ns
t_{ohold}	MDIO (read from PHY) output hold from rising edge of MDC	0			ns
t_{su}	MDIO (write to PHY) input setup time to rising edge of MDC	8			ns
t_{ihold}	MDIO (write to PHY) input hold time after rising edge of MDC	8			ns

Note 6-24 Test condition for 8.33 MHz (120 ns) is for one device PHY on the MDIO line with a 1.0 kΩ pull-up to the DVDDH supply rail.

Note 6-25 The device can operate with MDC clock frequencies generated from bit banging with GPIO pin in the 10s/100s of Hertz.

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6.7 Clock Circuit

The device can accept either a 25MHz crystal (preferred) or a 25 MHz single-ended clock oscillator (+/- 50ppm) input. If the single-ended clock oscillator method is implemented, XO should be left unconnected and XI should be driven with a nominal 0-3.3V clock signal. The input clock duty cycle is 40% minimum, 50% typical and 60% maximum.

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (XI/XO). See Table 6-17 for the recommended crystal specifications.

TABLE 6-17: CRYSTAL SPECIFICATIONS

Parameter	Symbol	Min	Nom	Max	Units	Notes
Crystal Cut	AT, typ					
Crystal Oscillation Mode	Fundamental Mode					
Crystal Calibration Mode	Parallel Resonant Mode					
Frequency	F_{fund}	-	25.000	-	MHz	
Frequency Tolerance @ 25°C	F_{tol}	-	-	+/-50	PPM	Note 6-26
Frequency Stability Over Temp	F_{temp}	-	-	+/-50	PPM	Note 6-26
Frequency Deviation Over Time	F_{age}	-	+/-3 to 5	-	PPM	Note 6-27
Total Allowable PPM Budget		-	-	+/-50	PPM	Note 6-28
Shunt Capacitance	C_O	-	-	6	pF	
Load Capacitance	C_L	-	-	25	pF	
Motional Inductance	LM			10	mH	
Drive Level	P_W	-	-	100	µW	
Equivalent Series Resistance	R_1	-	-	50	Ohm	
Operating Temperature Range		Note 6-29	-	Note 6-30	°C	
XI Pin Capacitance		-	2 typ	-	pF	Note 6-31
XO Pin Capacitance		-	2 typ	-	pF	Note 6-31

Note 6-26 The maximum allowable values for Frequency Tolerance and Frequency Stability are application dependent. Since any particular application must meet the IEEE +/-50 PPM Total PPM Budget, the combination of these two values must be approximately +/-45 PPM (allowing for aging).

Note 6-27 Frequency Deviation Over Time is also referred to as Aging.

Note 6-28 The total deviation for the Transmitter Clock Frequency is specified by IEEE 802.3u as +/- 50 PPM.

Note 6-29 0°C for commercial version, -40°C for industrial and automotive.

Note 6-30 +70°C for commercial version, +85°C for industrial/ automotive grade 3 versions, +105°C for automotive grade 2 version.

Note 6-31 This number includes the pad, the bond wire and the lead frame. PCB capacitance is not included in this value. The XO/XI pin and PCB capacitance values are required to accurately calculate the value of the two external load capacitors. These two external load capacitors determine the accuracy of the 25.000 MHz frequency.

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6.8 Reset Circuit

The following are some reset circuit suggestions.

Figure 6-8 illustrates the reset circuit for powering up the KSZ9131RNX if reset is triggered by the power supply.

FIGURE 6-8: RESET CIRCUIT IF TRIGGERED BY THE POWER SUPPLY

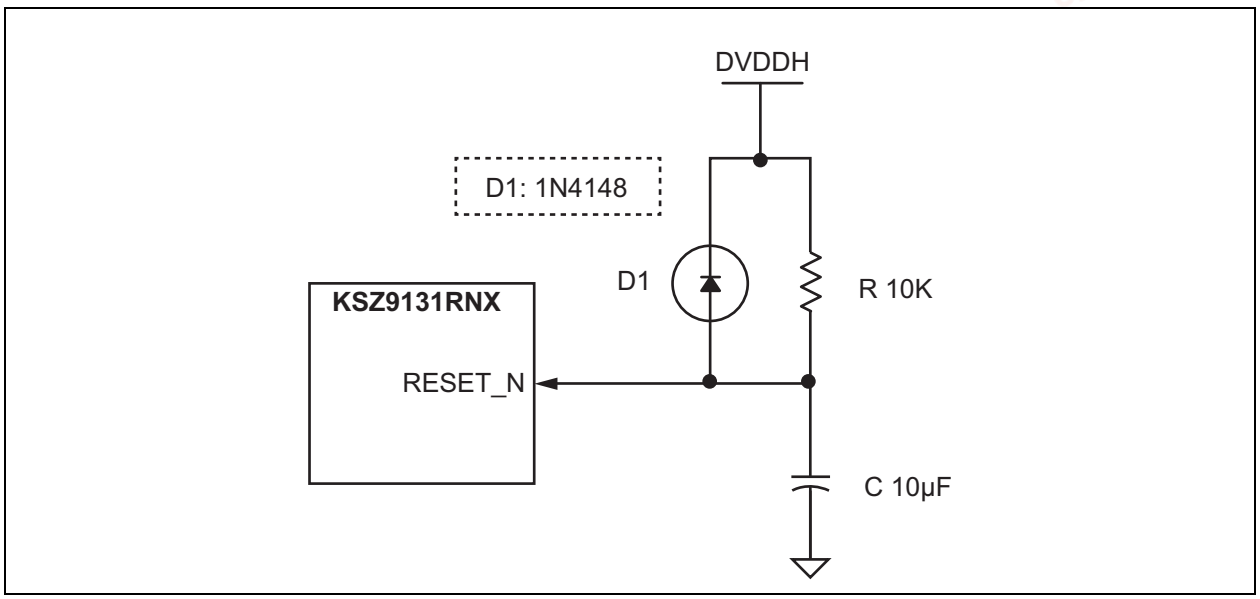
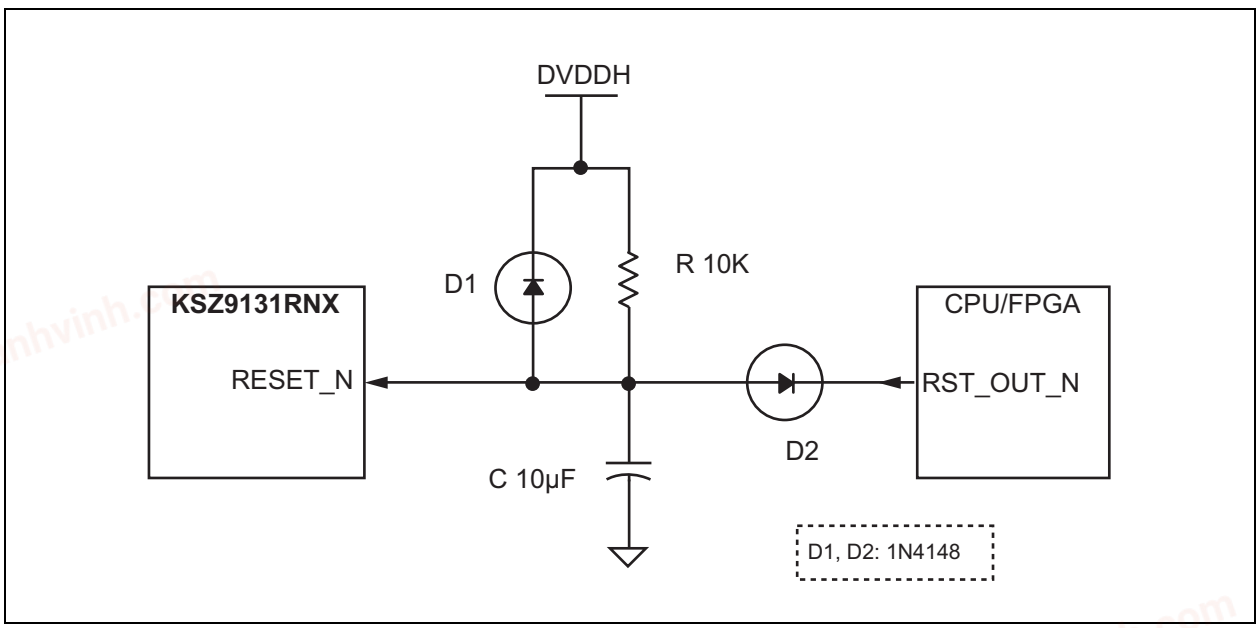


Figure 6-9 illustrates the reset circuit for applications where reset is driven by another device (for example, the CPU or an FPGA). At power-on-reset, R, C, and D1 provide the monotonic rise time to reset the KSZ9131RNX device. The RST_OUT_N from the CPU/FPGA provides the warm reset after power-up.

The KSZ9131RNX and CPU/FPGA references the same digital I/O voltage (DVDDH).

FIGURE 6-9: RECOMMENDED RESET CIRCUIT FOR CPU/FPGA RESET OUTPUT

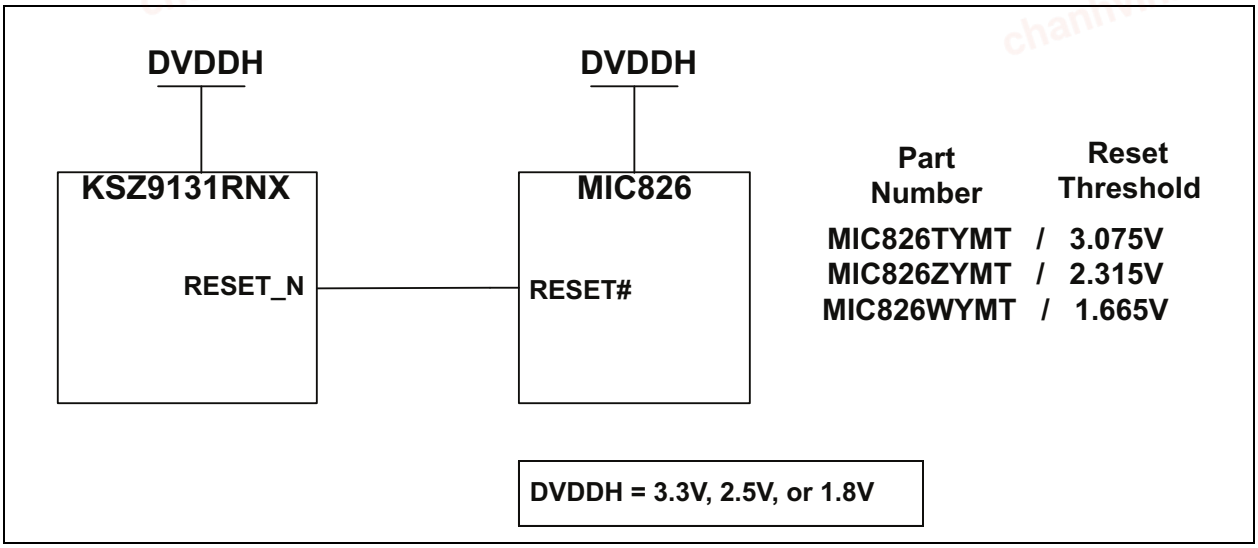


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Figure 6-10 illustrates the reset circuit with an MIC826 voltage supervisor driving the KSZ9131RNX reset input.

FIGURE 6-10: RESET CIRCUIT WITH MIC826 VOLTAGE SUPERVISOR

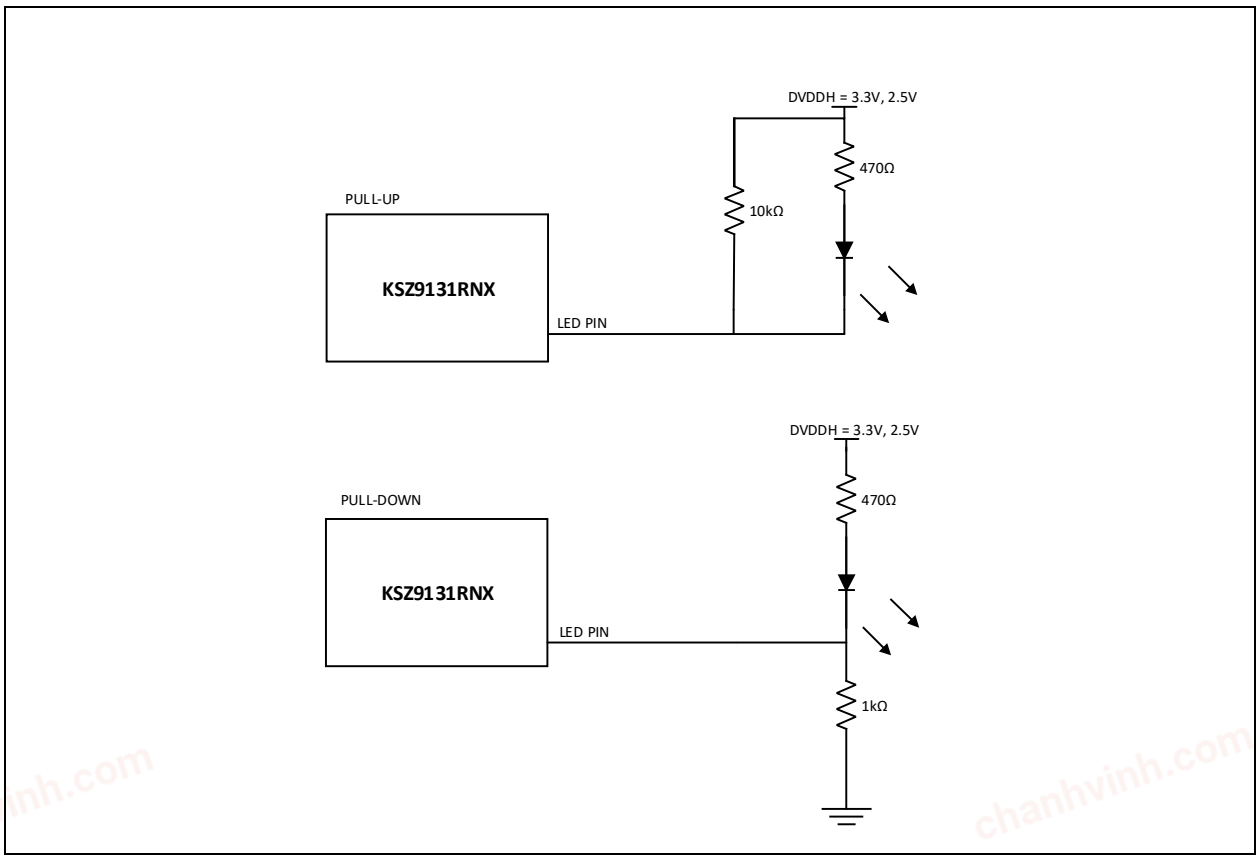


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6.9 Reference Circuits — LED Strap-In Pins

The pull-up and pull-down reference circuits for the LED2/PHYAD1 and LED1/PHYAD0 strapping pins are shown in Figure 6-11 for 3.3V and 2.5V DVDDH.

FIGURE 6-11: REFERENCE CIRCUITS FOR LED STRAPPING PINS



For 1.8V DVDDH, LED indication support requires voltage level shifters between LED[2:1] pins and LED indicator diodes to ensure the multiplexed PHYAD[1:0] strapping pins are latched in high/low correctly. If LED indicator diodes are not implemented, the PHYAD[1:0] strapping pins just need 10 kΩ pull-up to 1.8V DVDDH for a value of 1, and 1.0 kΩ pull-down to ground for a value of 0.

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6.10 On-Chip LDO Controller - MOSFET Selection

If the optional LDO controller is used to generate 1.2V for the core voltage, the selected MOSFET should exceed the following minimum requirements:

- P-channel
- 500 mA (continuous current)
- 3.3V or 2.5V (source – input voltage)
- 1.2V (drain – output voltage)
- V_{GS} in the range of:
  - (–1.2V to –1.5V) @ 500 mA for 3.3V source voltage
  - (–1.0V to –1.1V) @ 500 mA for 2.5V source voltage

The V_{GS} for the MOSFET needs to be operating in the constant current saturated region, and not towards the $V_{GS(th)}$, the threshold voltage for the cut-off region of the MOSFET.

6.11 Magnetic - Connection and Selection

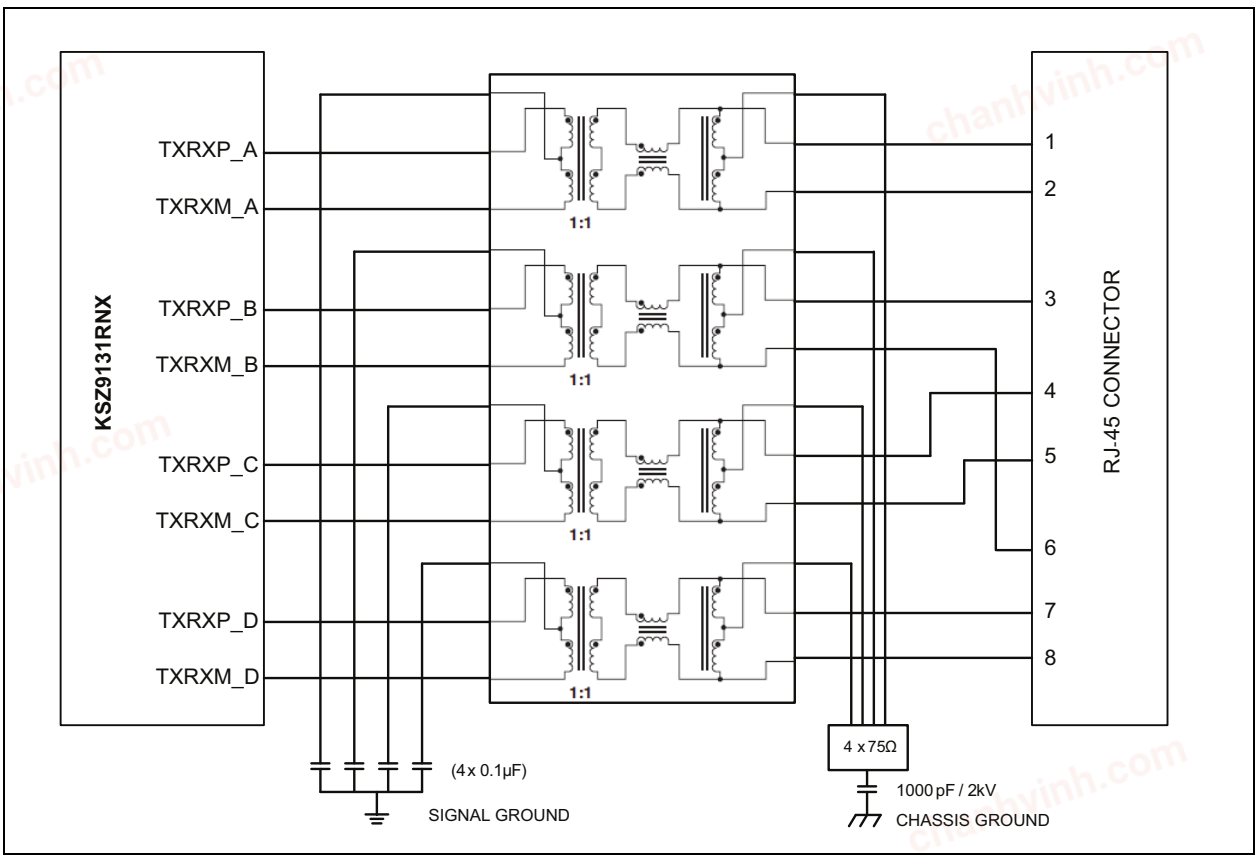
A 1:1 isolation transformer is required at the line interface. Use one with integrated common-mode chokes for designs exceeding FCC requirements. An optional auto-transformer stage following the chokes provides additional common-mode noise and signal attenuation.

The KSZ9131RNX design incorporates voltage-mode transmit drivers and on-chip terminations.

With the voltage-mode implementation, the transmit drivers supply the common-mode voltages to the four differential pairs. Therefore, the four transformer center tap pins on the KSZ9131RNX side should not be connected to any power supply source on the board; rather, the center tap pins should be separated from one another and connected through separate 0.1 µF common-mode capacitors to ground. Separation is required because the common-mode voltage could be different between the four differential pairs, depending on the connected speed mode.

Figure 6-12 shows the typical Gigabit magnetic interface circuit for the KSZ9131RNX.

FIGURE 6-12: TYPICAL GIGABIT MAGNETIC INTERFACE CIRCUIT



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Table 6-18 lists recommended magnetic characteristics.

TABLE 6-18: MAGNETICS SELECTION CRITERIA

Parameter	Value	Test Conditions
Turns Ratio	1 CT : 1 CT	—
Open-Circuit Inductance (min.)	350 µH	100 mV, 100 kHz, 8 mA
Insertion Loss (max.)	1.0 dB	0 MHz to 100 MHz
HIPOT (min.)	1500 V_{RMS}	—

Table 6-19 is a list of compatible single-port magnetics with separated transformer center tap pins on the G-PHY chip side that can be used with the KSZ9131RNX.

TABLE 6-19: COMPATIBLE SINGLE-PORT 10/100/1000 MAGNETICS

Manufacturer	Part Number	Auto-Transformer	Temperature Range	Magnetic + RJ-45
Bel Fuse	0826-1G1T-23-F	Yes	0°C to 70°C	Yes
HALO	TG1G-E001NZRL	No	–40°C to 85°C	No
HALO	TG1G-S001NZRL	No	0°C to 70°C	No
HALO	TG1G-S002NZRL	Yes	0°C to 70°C	No
Pulse	H5007NL	Yes	0°C to 70°C	No
Pulse	H5062NL	Yes	0°C to 70°C	No
Pulse	HX5008NL	Yes	–40°C to 85°C	No
Pulse	JK0654219NL	Yes	0°C to 70°C	Yes
Pulse	JK0-0136NL	No	0°C to 70°C	Yes
TDK	TLA-7T101LF	No	0°C to 70°C	No
Wurth/Midcom	000-7093-37R-LF1	Yes	0°C to 70°C	No

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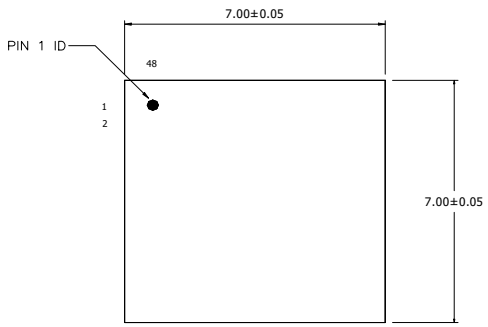
7.0 PACKAGE OUTLINE

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

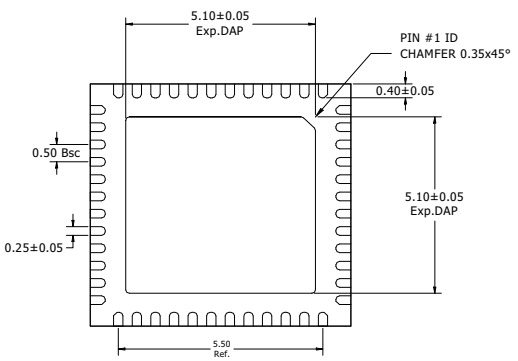
FIGURE 7-1: 48-LEAD QFN 7 MM X 7 MM PACKAGE WITH 5.1 MM X 5.1 MM EXPOSED PAD AREA

TITLE
48 LEAD QFN 7x7mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

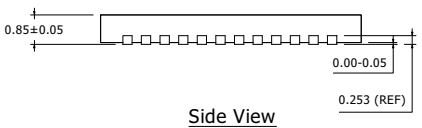
DRAWING #	QFN77-48LD-PL-1	UNIT	MM



Top View
NOTE: 1, 2, 3



Bottom View
NOTE: 1, 2, 3



Side View
NOTE: 1, 2, 3

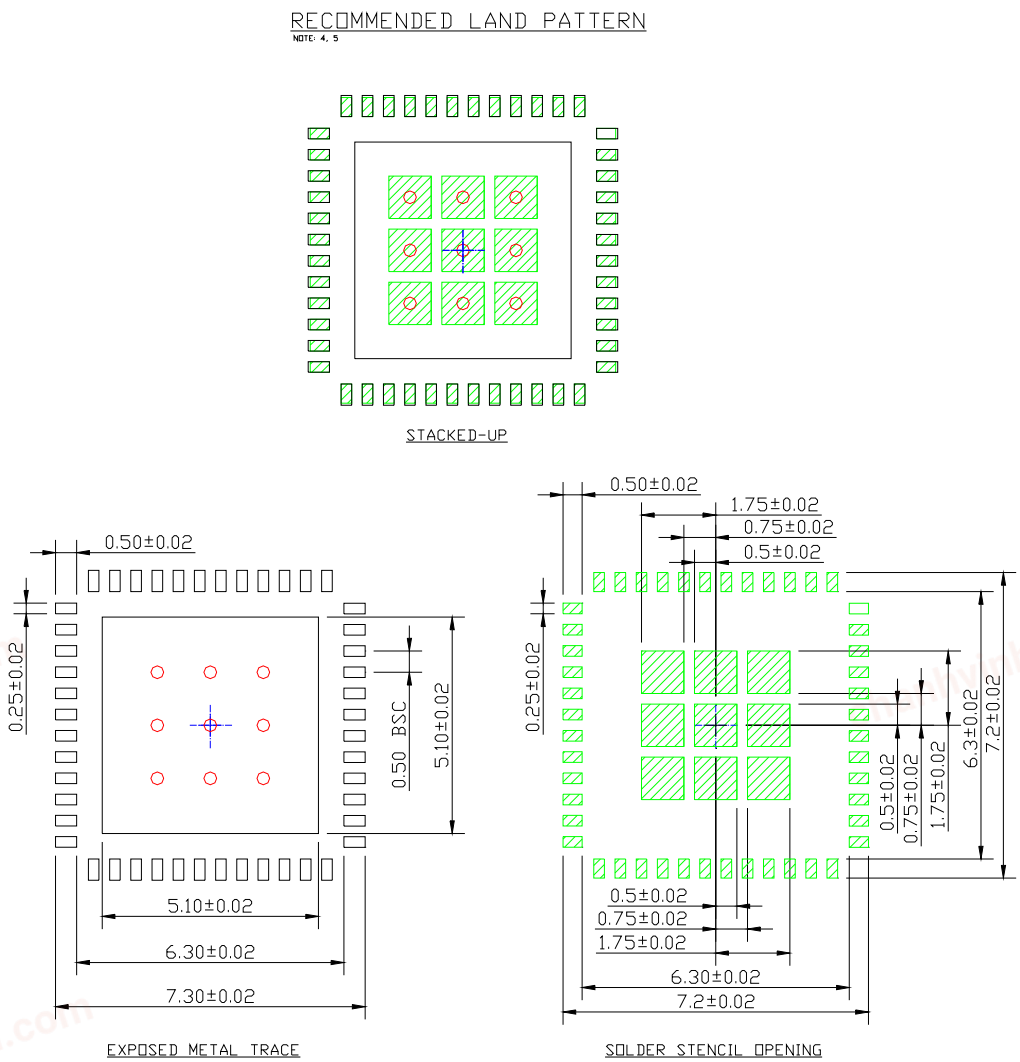
NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. RED CIRCLE IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.35mm IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE. PITCH is 1.00mm.
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA. RECOMMENDED SIZE IS 1.00x1.00mm, SPACING IS 0.25mm.

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FIGURE 7-2: 48-LEAD QFN 7 MM X 7 MM PACKAGE WITH 5.1 MM X 5.1 MM EXPOSED PAD AREA RECOMMENDED LAND PATTERN

POD-Land Pattern drawing #: QFN77-48LD-PL-1-C

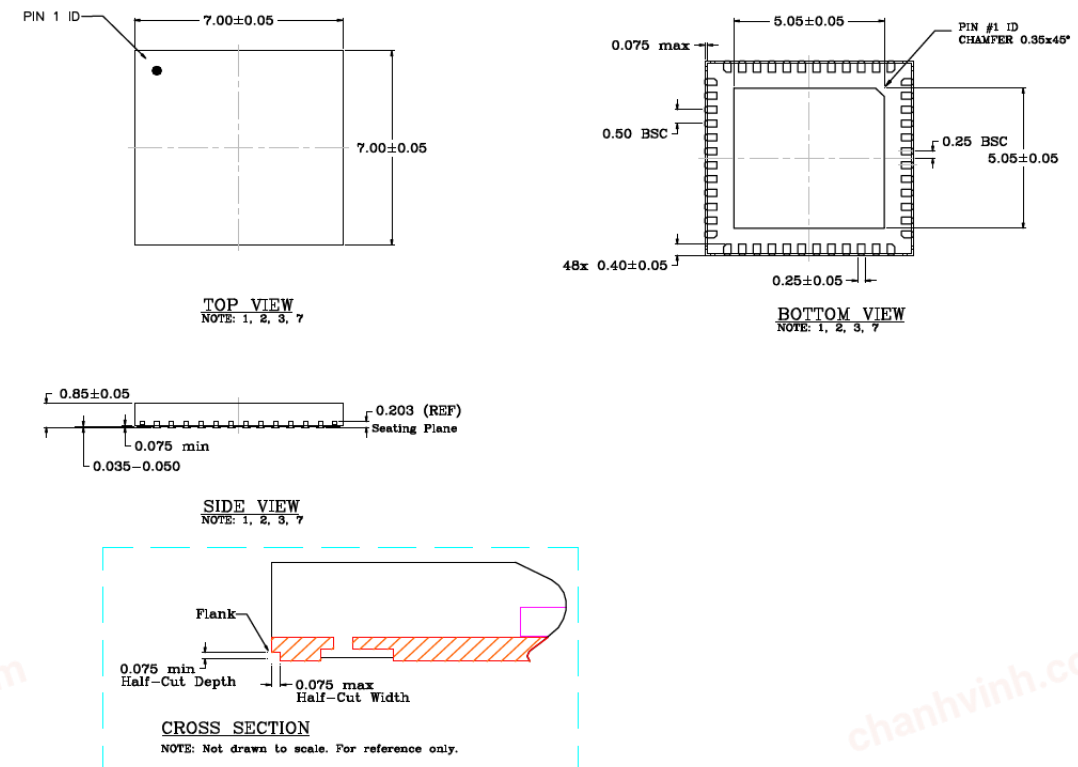


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FIGURE 7-3: 48-LEAD VQFN 7 MM X 7 MM PACKAGE (WETTABLE FLANK) WITH 5.05 MM X 5.05 MM EXPOSED PAD AREA

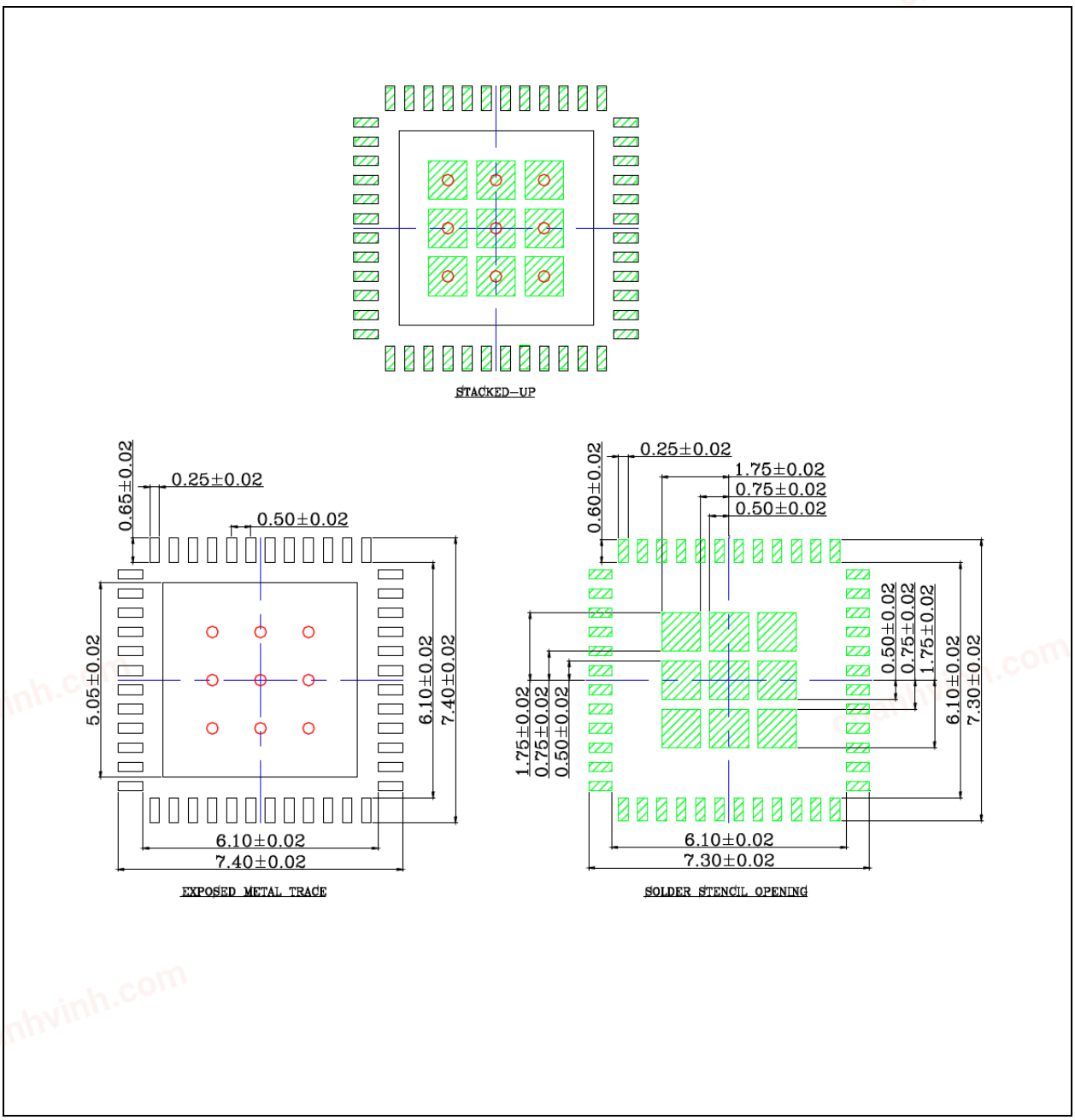


NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. RED CIRCLES IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.35mm IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE. PITCH = 1.00mm
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA. RECOMMENDED SIZE IS 1.0x1.0mm, SPACING = 0.25mm.

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FIGURE 7-4: 48-LEAD VQFN 7 MM X 7 MM PACKAGE (WETTABLE FLANK) WITH 5.05 MM X 5.05 MM EXPOSED PAD AREA RECOMMENDED LAND PATTERN



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APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00002841B (10-09-19	Section 4.13.1, "Digital (near-end) Loopback"	Revised loopback steps
	Section 4.13.2, "Remote (far-end) Loopback"	Added step 3
	Table 6-3, "Power Consumption"	Updated values
	Figure 6-11, "Reference Circuits For LED Strapping Pins"	Modified figure
DS00002841A (11-08-18)	All	Initial release.

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Device	Interface	Package	Temp.	Bond Wire / Media Type	Automotive Option

Device:	KSZ9131	
Interface:	R	= RGMII
Package:	NX	= 48-pin QFN or VQFN
Temperature:	C	= 0°C to +70°C (Commercial)
	I	= -40°C to +85°C (Industrial)
	U	= -40°C to +85°C (Automotive Grade 3)
	V	= -40°C to +105°C (Automotive Grade 2)
Media Type:	Blank	= Standard packaging (tray)
	TR	= Tape and Reel(Note 1)
Automotive Option:	VAO	= Automotive Option

Examples:

a) KSZ9131RNXC
RGMII Interface
48-pin QFN (Pb-Free, 5.1 mm x 5.1 mm ePad)
Commercial Temperature
Tray

b) KSZ9131RNXC-TR
RGMII Interface
48-pin QFN (Pb-Free, 5.1 mm x 5.1 mm ePad)
Commercial Temperature
Tape and reel

c) KSZ9131RNXI
RGMII Interface
48-pin QFN (Pb-Free, 5.1 mm x 5.1 mm ePad)
Industrial Temperature
Tray

d) KSZ9131RNXI-TR
RGMII Interface
48-pin QFN (Pb-Free, 5.1 mm x 5.1 mm ePad)
Industrial Temperature
Tape and reel

e) KSZ9131RNXU-VAO
RGMII Interface
48-pin VQFN wettable flank lead frame
(Pb-Free, 5.05 mm x 5.05 mm ePad)
Automotive Grade 3 Temperature
Tray

f) KSZ9131RNXU-TRVAO
RGMII Interface
48-pin VQFN wettable flank lead frame
(Pb-Free, 5.05 mm x 5.05 mm ePad)
Automotive Grade 3 Temperature
Tape and reel

g) KSZ9131RNXV-VAO
RGMII Interface
48-pin VQFN wettable flank lead frame
(Pb-Free, 5.05 mm x 5.05 mm ePad)
Automotive Grade 2 Temperature
Tray

h) KSZ9131RNXV-TRVAO
RGMII Interface
48-pin VQFN wettable flank lead frame
(Pb-Free, 5.05 mm x 5.05 mm ePad)
Automotive Grade 2 Temperature
Tape and reel

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