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High Side Current Monitor
8.0 to 450V
Voltage Gain of 1

Features

- Supply voltages from 8V to 450V
- Voltage output device
- Typical gain 1±1%
- Max V_{SENSE} 500mV
- Fast rise and fall time, 700ns to 2.0µs
- Maximum quiescent current 50µA
- 5-Lead SOT-23 Package

Applications

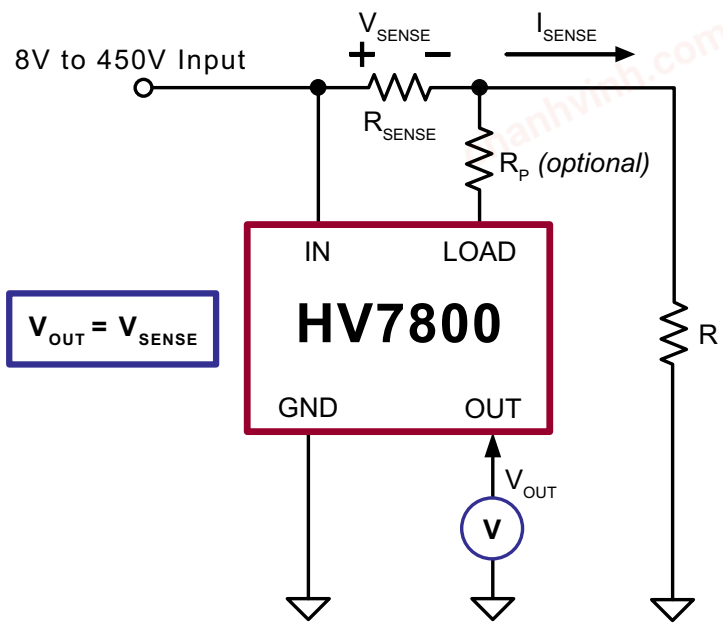
- SMPS current monitor
- Battery current monitor
- Motor controls
- Telecom

General Description

The HV7800 high side current monitor IC transfers a high-side current measurement voltage to its ground referenced output with an accurate voltage gain of one. The measurement voltage typically originates at a current sense resistor which is located in a “high side” circuit, such as the positive supply line.

This monitor IC features a very wide input voltage range, high accuracy of transfer ratio, small size, low component count, low power consumption, ease of use, and low cost. Offline, battery and portable applications can be served equally well due to the wide input voltage range and the low quiescent current of the HV7800.

Typical Application Circuit



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Ordering Information

Part Number	Package Option	Packing
HV7800K1-G	5-Lead SOT-23	2500/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings

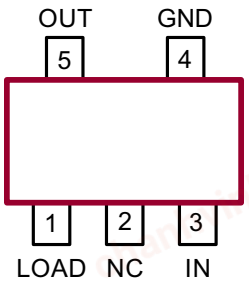
Parameter	Value
V_{IN}, V_{LOAD} [1]	-0.5V to +460V
V_{OUT} [1]	-0.5V to +10V
V_{SENSE} [2]	-0.5V to +5.0V
I_{LOAD}	±10mA
Operating ambient temperature	-40°C to +85°C
Operating junction temperature	-40°C to +125°C
Storage temperature	-65°C to +150°C

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Notes:

1. *Referenced to GND*
2. $V_{SENSE} = V_{IN} - V_{LOAD}$

Pin Configuration



5-Lead SOT-23
(top view)

Product Marking



Y = Last Digit of Year Sealed
W = Code for Week Sealed
— = "Green" Packaging

Package may or may not include the following marks: Si or ⏻

5-Lead SOT-23

Typical Thermal Resistance

Package	θ_{ja}
5-Lead SOT-23	253°C/W

Note:
Thermal testboard per JEDEC JESD51-7

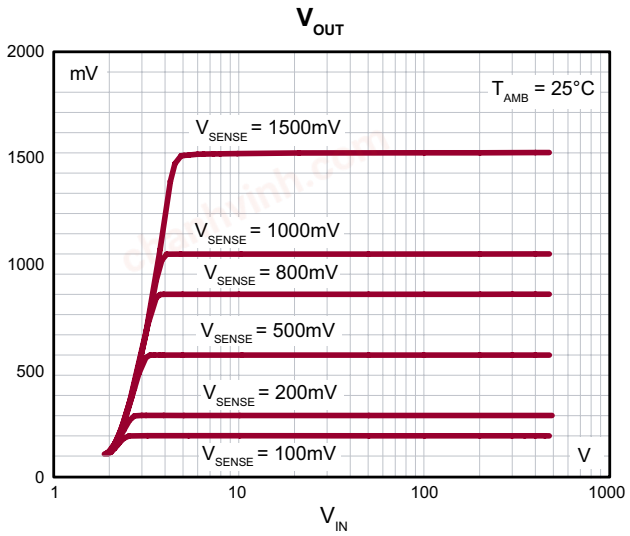
Electrical Characteristics *(T_A = 25°C unless otherwise specified, V_{IN} = 8V to 450V)*

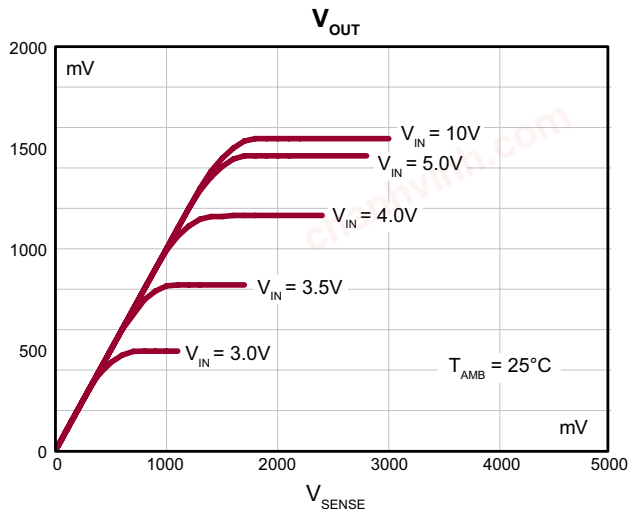
Sym	Parameter	Min	Typ	Max	Units	Conditions
Supply						
V_{IN}	Supply voltage	8.0	-	450	V	*	---
I_Q	Quiescent supply current	-	-	50	µA	-	V_{IN} = 8.0V to 450V, V_{SENSE} = 0mV
Input and Output						
R_{OUT}	OUT pin output resistance	-	3.6	-	kΩ	-	---
V_{OUT}	Output voltage	0	-	15	mV	-	V_{SENSE} = 0mV
		79	-	121		-	V_{SENSE} = 100mV
		177	-	223		-	V_{SENSE} = 200mV
		470	-	530		-	V_{SENSE} = 500mV
Dynamic Characteristics						
t_{RISE}	Output rise time, 10% to 90%	-	0.7	-	µs	-	V_{SENSE} step 5.0mV to 500mV
		-	-	2.0		-	V_{SENSE} step 0mV to 500mV
t_{FALL}	Output fall time, 90% to 10%	-	0.7	2.0	µs	*	V_{SENSE} step 500mV to 0mV

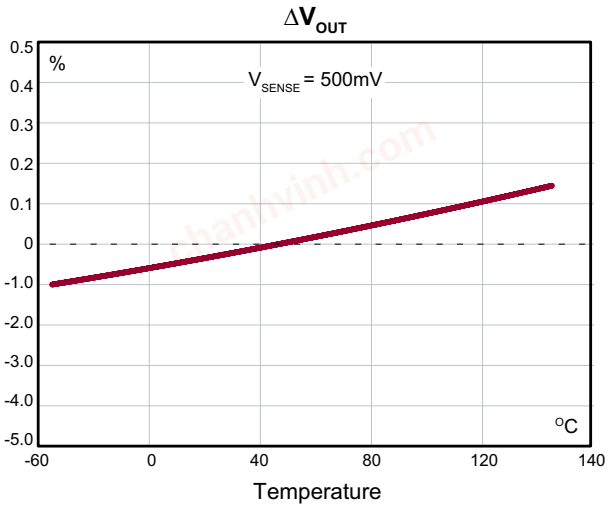
** Values apply over the full temperature range*

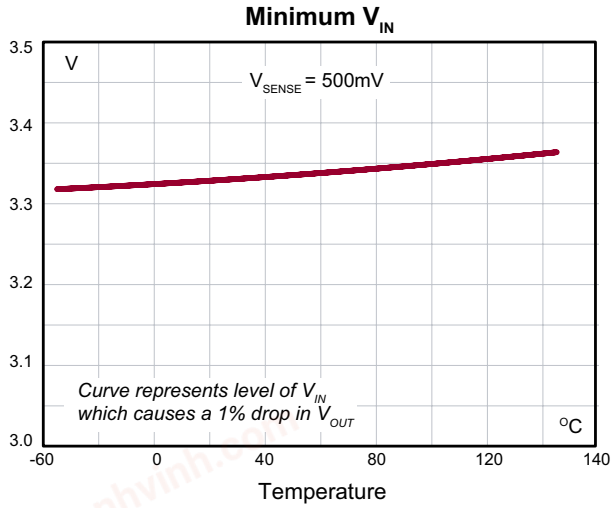
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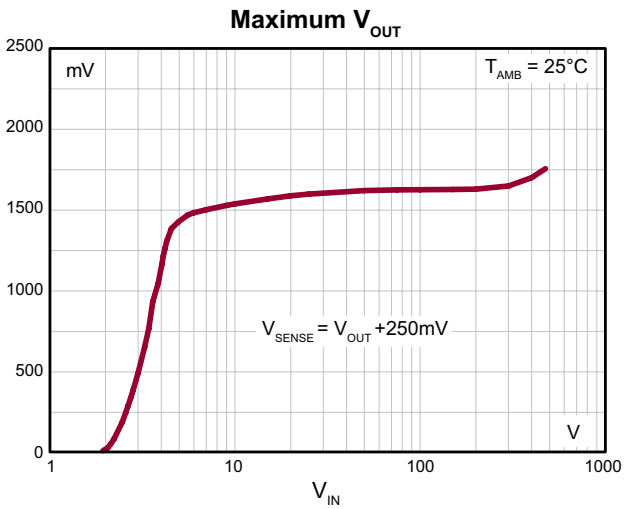
Typical Performance Characteristics







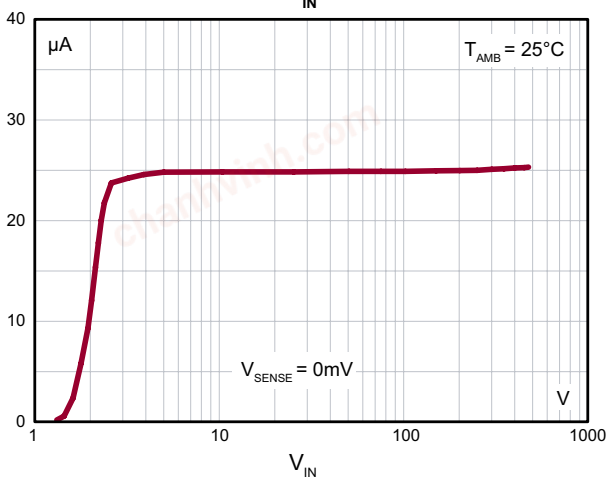




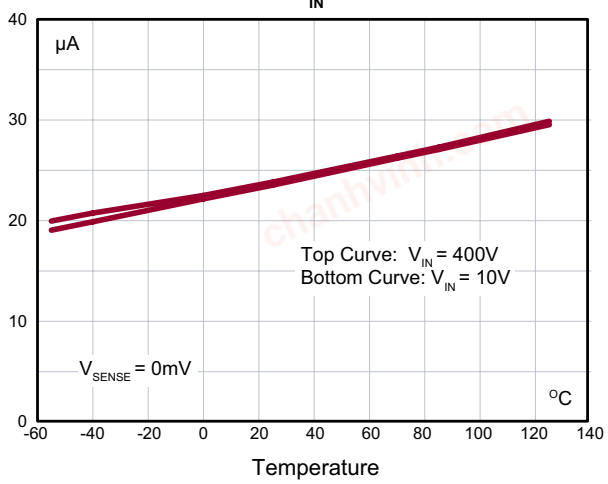
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Typical Performance Characteristics *(cont.)*

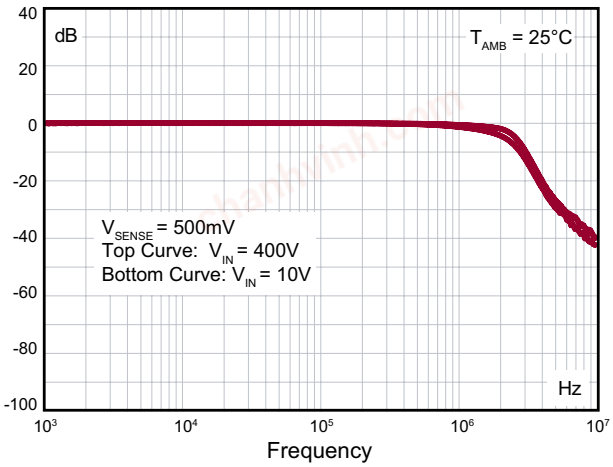
I_{IN}



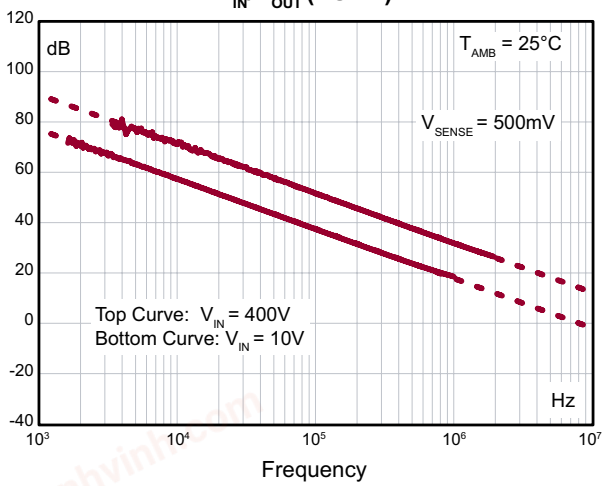
I_{IN}



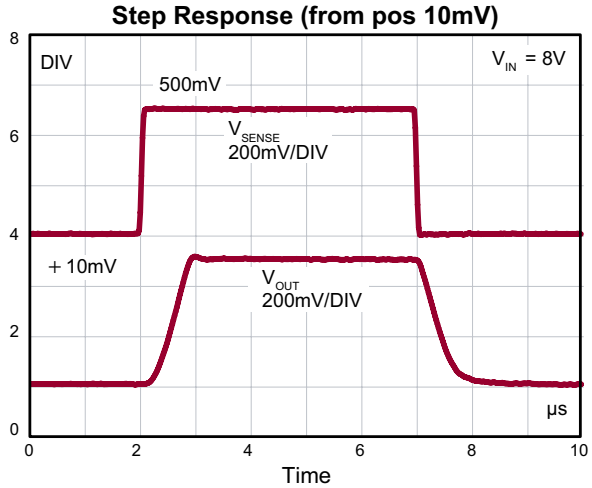
V_{OUT}/V_{SENSE} (Gain)



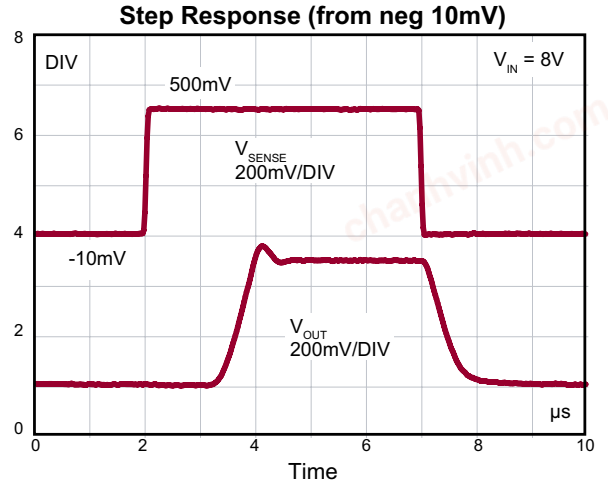
V_{IN}/V_{OUT} (PSRR)



Step Response (from pos 10mV)

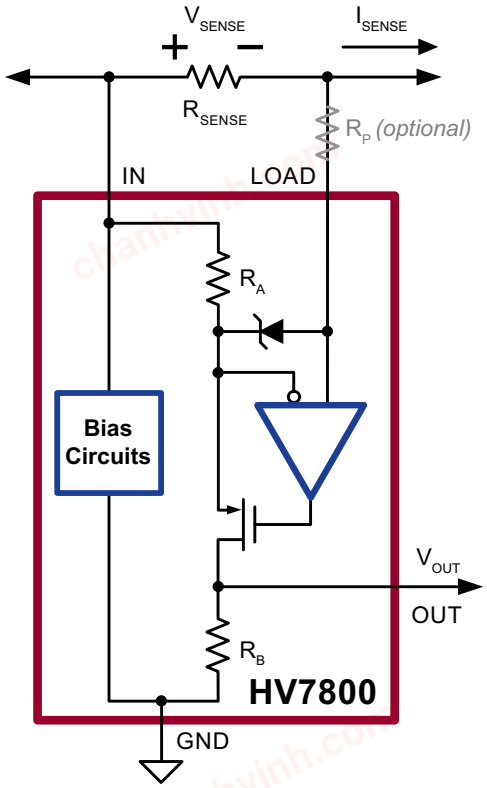


Step Response (from neg 10mV)



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Block Diagram



Application Information

General

The HV7800 high side current monitor IC features accurate current sensing, small size, low component count, low power consumption, exceptional input voltage range, ease of use and low cost.

The part typically performs the measurement of line or load current for overcurrent protection, metering or current regulation.

High side current sensing, as opposed to ground referenced or low side current sensing, is desirable or required when:

- The current to be measured does not flow in a circuit associated with ground.
- The measurement at ground level can lead to ambiguity due to changes in the grounding arrangement during field use.
- Introduction of a sense resistor in the system ground is undesirable due to issues with safety, EMI, or signal degradation caused by common impedance coupling.

Principle of Operation

The operational amplifier and MOSFET force the voltage across R_A to track V_{SENSE} within the limit of the offset voltage of the opamp, i.e. $V_{RA} = V_{SENSE}$.

The current through R_A returns to ground through R_B. R_A and R_B are integrated, exhibiting tight matching and excellent tracking. By design, R_A and R_B have the same resistance. Consequently, V_{RA} is equal to V_{RB}, resulting in a voltage gain of 1.

OUT Pin Loading Effects

Note that the OUT pin has a typical output resistance of 3.6kΩ. Loading the output causes the voltage gain to drop and rise/fall time to increase.

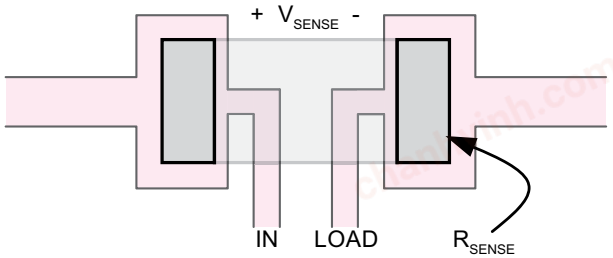
For example, assuming an output resistance of 3.6kΩ, the load resistance should exceed 3.6MΩ in order to limit the drop in gain to 1 part in 1000.

Again assuming an output resistance of 3.6kΩ, capacitive loading of 30pF results in a response pole with a time constant of 100ns, not yet high enough to materially affect the output rise and fall time (about 700ns).

Sense Resistor Considerations

Choose a sense resistor that will not exceed 500mV during normal operating conditions. Limit the power dissipation in the sense resistor to whatever is practical; a high sense voltage benefits accuracy, but increases power dissipation.

Consider the use of Kelvin connections for applications where considerable voltage drops may occur in the PCB traces that carry the current to be measured to the sense resistor. A layout pattern that minimizes voltage across the sense lines is shown below.



Choose a low inductance type sense resistor if preservation of bandwidth is important. The use of Kelvin connections helps by excluding the inductive voltage drop across the traces leading to the sense resistor. The inductive voltage drop may be substantial when operating at high frequencies.

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A trace or component inductance of just 10nH contributes an impedance of 6.2mΩ at 100kHz, which constitutes a 6% error when using a 100mΩ sense resistor.

Transient Protection

Add a protection resistor (R_P) in series with the LOAD pin if V_{SENSE} can exceed 5.0V in a positive sense or 600mV in a negative sense, whether in a steady state or in transient conditions.

A large V_{SENSE} may occur during system startup or shutdown due to the charging and discharging of bulk storage capacitors. V_{SENSE} may be large due to fault conditions, such as a short circuit condition, or a broken or missing sense resistor.

An internal 5.0V Zener diode with a current rating of 10mA protects the sense amplifier inputs. The block diagram shows the orientation of this diode. The Zener diode provides clamping at 5.0V for a positive V_{SENSE} and at 600mV for a negative V_{SENSE}.

Under worst case conditions, limit the Zener current to 10mA. A 100kΩ resistor limits the Zener diode current to 4.5mA when V_{SENSE} is 450V, whether positive or negative. Note that the protection resistor may affect the bandwidth. The resistor forms a RC network with the trace and pin capacitance at the LOAD pin. A capacitance of 5.0pF results in a time constant of 500ns.

The protection resistor may cause an offset due to bias current at the LOAD input. Under worst case bias current (1.0nA), a 100kΩ protection resistor could cause an offset of 100μV or 0.2% of full scale. Note that the bias current is nominally zero as the LOAD is a high impedance CMOS input.

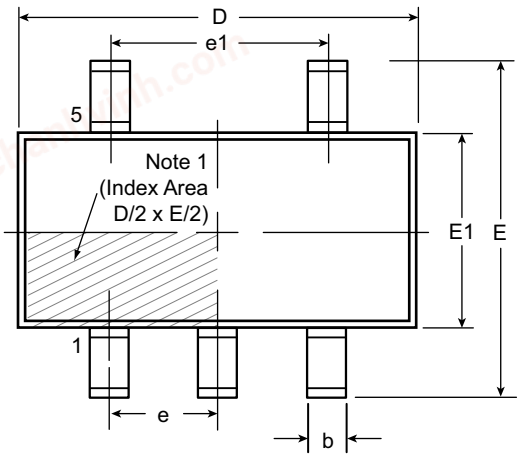
Pin Description

Pin #	Pin Name	Description
1	LOAD	Sense amplifier input. High impedance input with Zener diode protection. Add an external protection resistor in series with LOAD if V_{SENSE} exceeds the range of -600mV to +5V.
2	NC	No connect. This pin must be left floating for proper operation.
3	IN	Sense amplifier input and supply.
4	GND	Supply return.
5	OUT	Output with a nominal output resistance of 3.6kΩ. Preservation of accuracy may require an external buffer amplifier to prevent excessive loading.

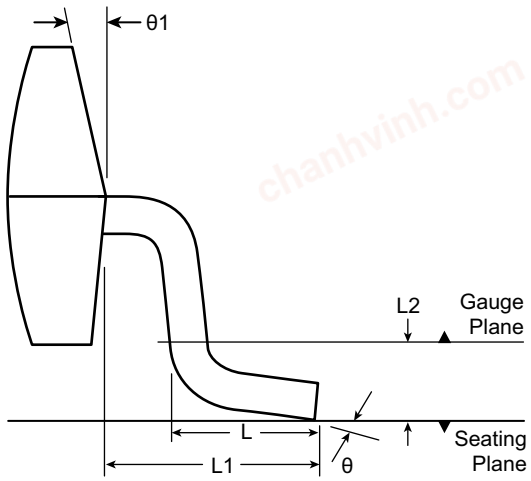
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5-Lead SOT-23 Package Outline (K1)

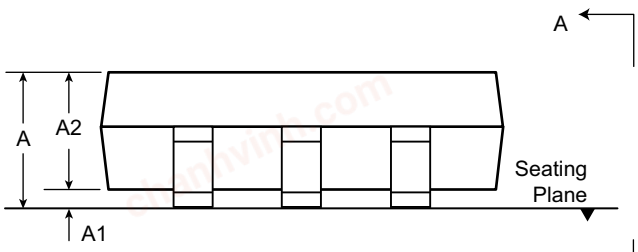
2.90x1.60mm body, 1.45mm height (max), 0.95mm pitch



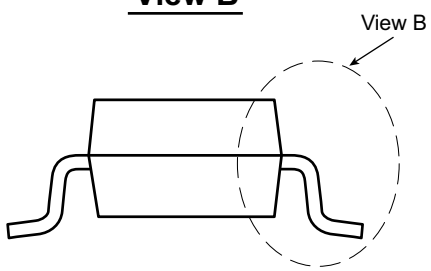
Top View



View B



Side View



View A - A

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	e1	L	L1	L2	θ	θ1
Dimension (mm)	MIN	0.90*	0.00	0.90	0.30	2.75*	2.60*	1.45*	0.95 BSC	1.90 BSC	0.30	0.60 REF	0.25 BSC	0°	5°
	NOM	-	-	1.15	-	2.90	2.80	1.60			0.45			4°	10°
	MAX	1.45	0.15	1.30	0.50	3.05*	3.00*	1.75*			0.60			8°	15°

JEDEC Registration MO-178, Variation AA, Issue C, Feb. 2000.
** This dimension is not specified in the JEDEC drawing.*
Drawings not to scale.
***Supertex Doc. #:** DSPD-5SOT23K1, Version A041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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