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HV56022

Dual High Voltage Operational Amplifiers

Features

- **Dual High Voltage Operational Amplifiers**
  - Up to +225V
  - 40 mA Minimum Peak Output Sink/Source Current
  - Output Voltage Comparators for Short Circuit Detection
  - 124 Hz, -3 dB Bandwidth with 0.22 µF Load

Applications

- Haptic Drivers
- Power Amplifiers

Related Devices

- HV56020-Dual High Voltage Operation Amplifier with Step-Up Converter and Power MOSFET

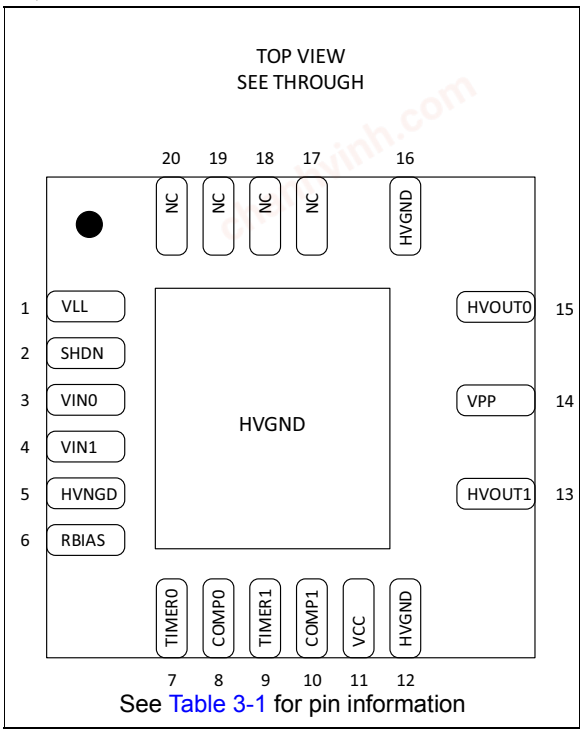
Description

The HV56022 is a Dual High Voltage Operational Amplifiers designed to drive haptic (piezo) actuators at 225V with 40 mA minimum source/sink current. Amplifiers are designed for a -3 dB bandwidth of 124 Hz for 225V sinusoidal waveforms driving 0.22 µF capacitive loads.

In addition, the amplifiers are paired with Output Voltage Comparators for load Short Circuit Detection.

Package

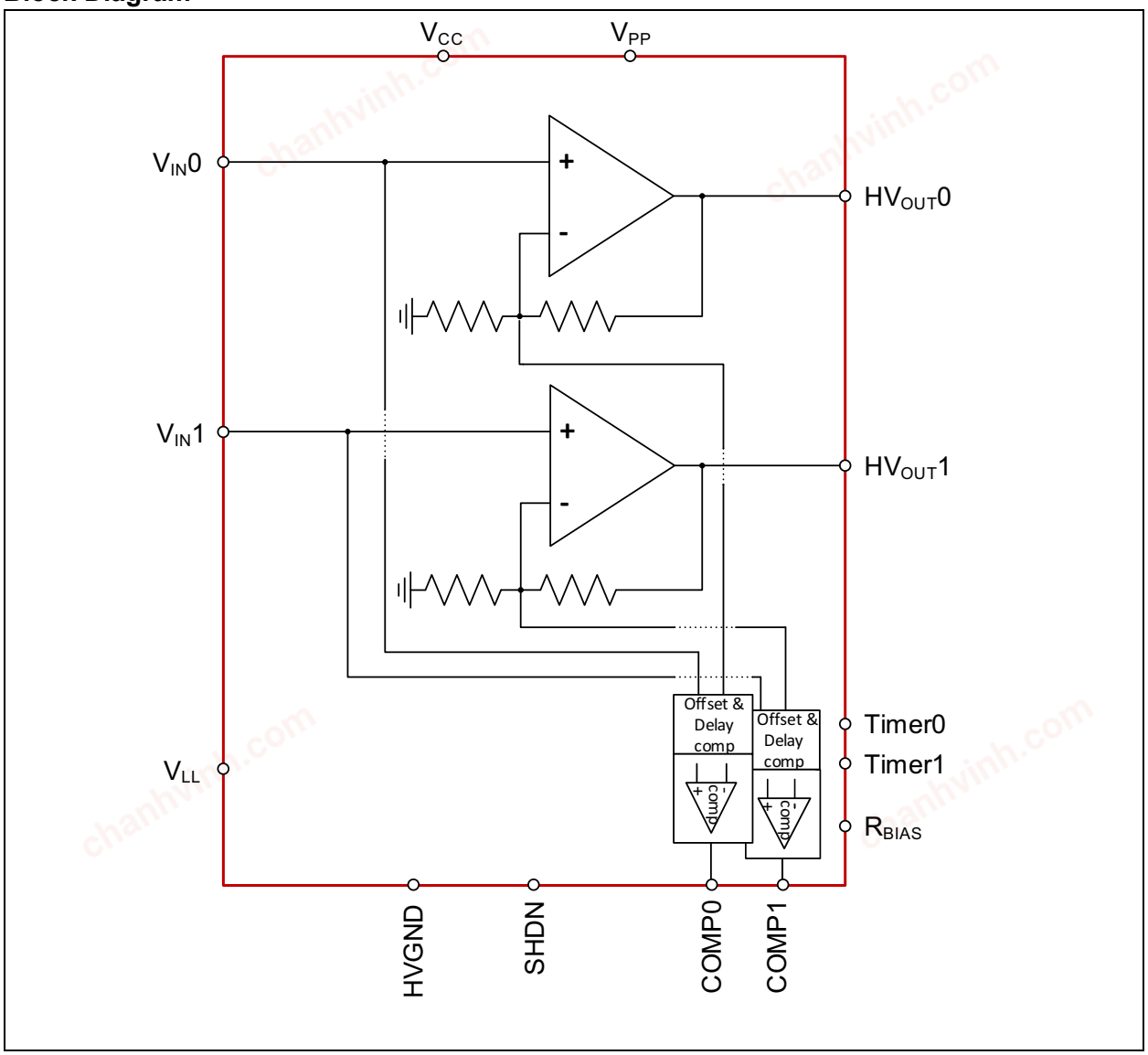
VQFN 20-Lead 4 x 4 x 0.9 mm



See Table 3-1 for pin information

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Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{LL}, Low Voltage Logic Supply.....-0.3V to 5.5V
V_{IN}0,1, High Voltage Op-Amps Inputs.....-0.3V to 5.5V
V_{CC}, Low Voltage Supply for High Voltage Op-Amps.....-0.3V to 8.0V
V_{PP}, High Voltage Supply for Op-Amps.....-0.3V to 250V
Storage Temperature.....-55 °C to +150 °C
Operating Junction Temperature.....0 °C to +125 °C

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
HIGH VOLTAGE OPERATIONAL AMPLIFIERS						
High Voltage Supply	V_{PP}	50	—	225	V	
Low Voltage Supply	V_{CC}	6.0	6.5	7.0	V	
Logic Supply Voltage	V_{LL}	3.0	3.3	3.6	V	
High Level Input Logic	V_{IH}	2.0	—	V_{LL}	V	for SHDN
Low Level Input Logic	V_{IL}	0	—	0.8	V	
Inputs for High Voltage Op-Amps	V_{IN}0,1	0	—	2.98	V	

POWER SEQUENCE

Power-Up Sequence:

1. Connect ground
2. Set all HV Amplifier inputs to 0V
3. Apply V_{LL}
4. Apply V_{CC}
5. Apply V_{PP}

Power-Down Sequence:

1. Disable V_{IN}0 and V_{IN}1 (set to 0V)
2. Disable V_{PP}
3. Disable V_{CC}
4. Disable V_{LL}
5. Disconnect ground

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HV OPERATIONAL AMPLIFIERS: DC AND AC CHARACTERISTICS

Unless otherwise specified $T_A = T_j = 25°C$. **Boldface** specifications apply over the full operating temperature range $T_A=T_J = 0°C$ to 125°C. Typical values are at +25°C, V_{CC} = 6.5V,V_{LL} = 3.3V unless otherwise specified.

Parameter	Symbol	Min	Typ.	Max	Units	Conditions
HV Op-Amps Low Voltage Supply	V_{CC}	6	6.5	7	V	
HV Op-Amps Low Voltage Supply Current	I_{CC}	—	0.2	—	mA	V_{CC}= 6.5V, V_{PP} = 225V (**Note 1**), f_{HVOUT} = 124Hz, sine wave $V_{IN0,1}$= 0 to 2.98V, C_L = 0.22µF
HV Op-Amps Input Analog Voltage	$V_{IN}0,1$	0	—	2.98	V	V_{PP} = 225V, V_{CC}= 6.5V
High Voltage Supply	V_{PP}	50	—	225	V	
V_{PP} Quiescent Supply Current	I_{PPQ}	—	—	**4.5**	mA	$V_{IN}0,1$= 0V, SHDN = 0
V_{PP} Supply Current	I_{PP}	—	16.5	—	mA	V_{CC}= 6.5V, V_{PP} = 225V, f_{HVOUT} = 124Hz (**Note 1**), sine wave $V_{IN}0,1$= 0 to 2.98V, C_L = 0.22µF
V_{PP} Shutdown Supply Current	I_{PPDN}	—	—	2	µA	SHDN = 1
HV_{OUT} High Level Output	V_{OH}	214	—	—	V	V_{CC}= 6.5V, V_{PP} = 225V, I_{HVOUT} = 100uA
HV_{OUT} Low Level Output	V_{OL}	—	—	1	V	V_{CC}= 6.5V, V_{PP} = 225V, I_{HVOUT} = -100uA
HV Op-Amps Output Offset Voltage	$HV_{OFF-SET}$	**-1.1**	—	**+1.1**	V	
HV_{OUT} Output Source Current	I_{HVOUT} (SOURCE)	40	—	—	mA	100V ≤ V_{PP} ≤ 225V, V_{CC}= 6.5V
HV_{OUT} Output Sink Current	I_{HVOUT} (SINK)	40	—	—	mA	100V ≤ V_{PP} ≤ 225V, V_{CC}= 6.5V
HV_{OUT} -3 dB Bandwidth	BW_{124Hz}	—	124	—	Hz	V_{PP} = 225V, V_{CC}= 6.5V, C_L = 0 to 0.22µF, HV_{OUT} = Full scale output, 25°C ≤ T_J ≤ 60°C, R_{BIAS}= 150 kΩ (**Note 1**)
HV_{OUT} Slew Rate	SR_{HV}	**0.09**	—	—	V/µs	V_{PP} = 225V, V_{CC}= 6.5V, C_L = 0.22µF
Closed Loop Gain	A_V	**72**	**75**	**78**	V/V	V_{PP} = 225V, V_{CC}= 6.5V, No Load
Shut Down Input Pin	SHDN	0.3	—	3.3	V	—
HV Op-Amps Shutdown Time	t_{SHDN}	—	300	—	ns	V_{PP} = 225V, V_{CC}= 6.5V, SHDN = 0 to 1, V_{IN}0,1 = 0 (**Note 2**)
HV Op-Amps Wake-Up Time from Shutdown	t_{WKUP}	—	2	—	ms	V_{PP} = 225V, V_{CC}= 6.5V, SHDN = 1 to 0, V_{IN}0,1 = 0 (**Note 2**)
HV Op-Amp Output Preload Capacitor	C_{PRE}	—	10	—	nF	**Note 2**
Output Voltage Comparators						
Comparator Output High Logic (VOH)	COMP0, COMP1	2	—	3.3	V	
Comparator Output Low Logic (VOL)		0	—	0.8		
Comparator Output Sink Current	C_{ISINK}	—	-2	—	mA	**Note 1**
Comparator Output Source Current	$C_{IS-OURCE}$	—	2	—	mA	**Note 1**
Comparator Input Offset	V_{OFFSET}	—	110	—	mV	**Note 1**
Comparator Delay	t_{DELAY}	0.6	1.6	2.6	ms	1.5 nF at Timer0, 1 pins, R_{BIAS} = 150 kΩ

Note 1: Specification is obtained by characterization and is not 100% tested.

2: Design guidance only.

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TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise specified, for all specifications $T_A = T_J = +25°C$						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperatures Ranges						
Operating Junction Temperature	T_J	0	—	+125	°C	
Storage Temperature	T_A	-55	—	+150	°C	
Package Thermal Resistances						
Thermal Resistance (20-Lead VQFN)	θ_{JC}	—	2.2	—	°C/W	Note 1
	θ_{JA}	—	43	—	°C/W	

Note 1: 4 Layers FR4 4” X 4” PCB.

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2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated: T_A = +25°C; Junction Temperature (T_J) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in Junction temperature over the Ambient temperature is not significant.

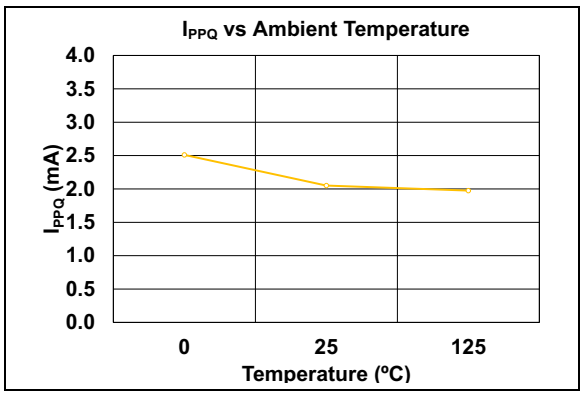


FIGURE 2-1: *I_{PPQ} vs Ambient Temperature.*

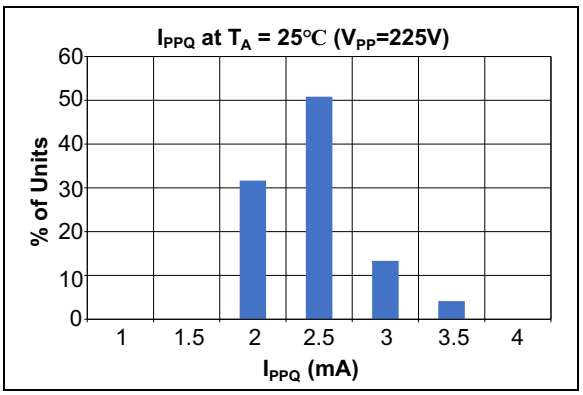


FIGURE 2-4: *I_{PPQ} Distribution at T_A = 25°C.*

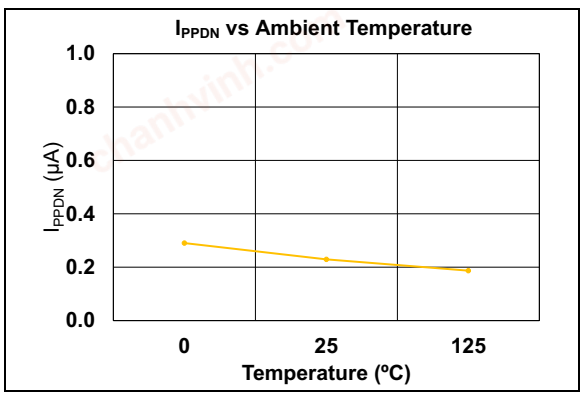


FIGURE 2-2: *I_{PPDN} vs Ambient Temperature.*

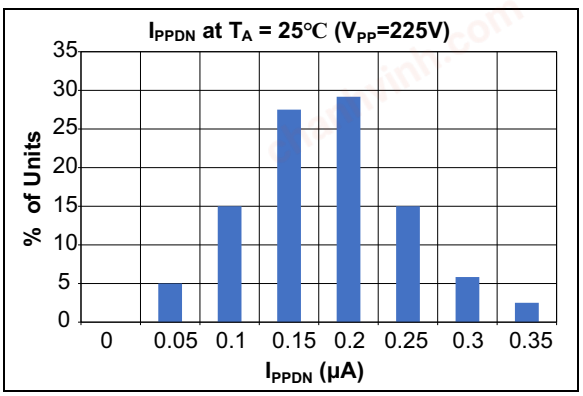


FIGURE 2-5: *I_{PPDN} Distribution at T_A = 25°C*

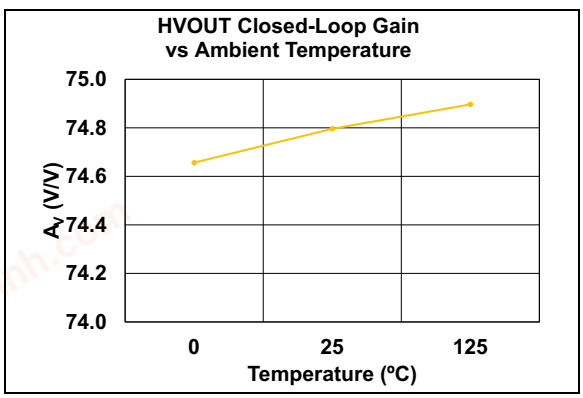


FIGURE 2-3: *HVOUT Closed-Loop Gain vs Ambient Temperature.*

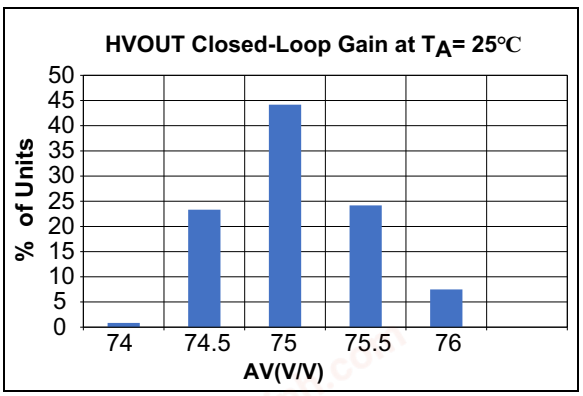


FIGURE 2-6: *HVOUT Closed-Loop Gain Distribution at T_A = 25°C.*

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Note: Unless otherwise indicated: TA = +25°C; Junction Temperature (TJ) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in Junction temperature over the Ambient temperature is not significant.

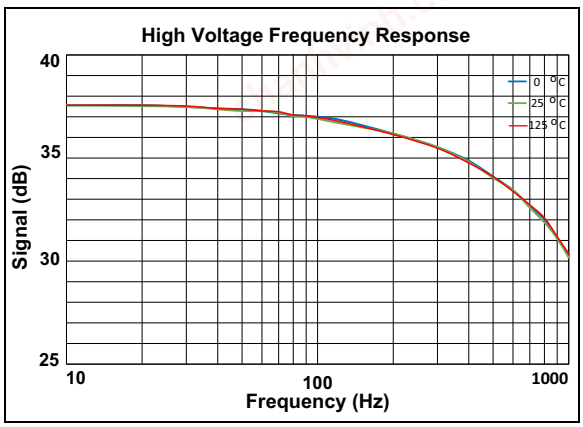


FIGURE 2-7: *High Voltage Frequency Response: Signal vs Frequency (V_{PP} = 225V, V_{CC} = 6.5V, V_{LL} = 3.3V, R_{BIAS} = 150 kΩ, V_{IN} = 0 to 2.98V, Load = 0.22 µF).*

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3.0 PACKAGE PIN CONFIGURATION AND FUNCTION DESCRIPTION

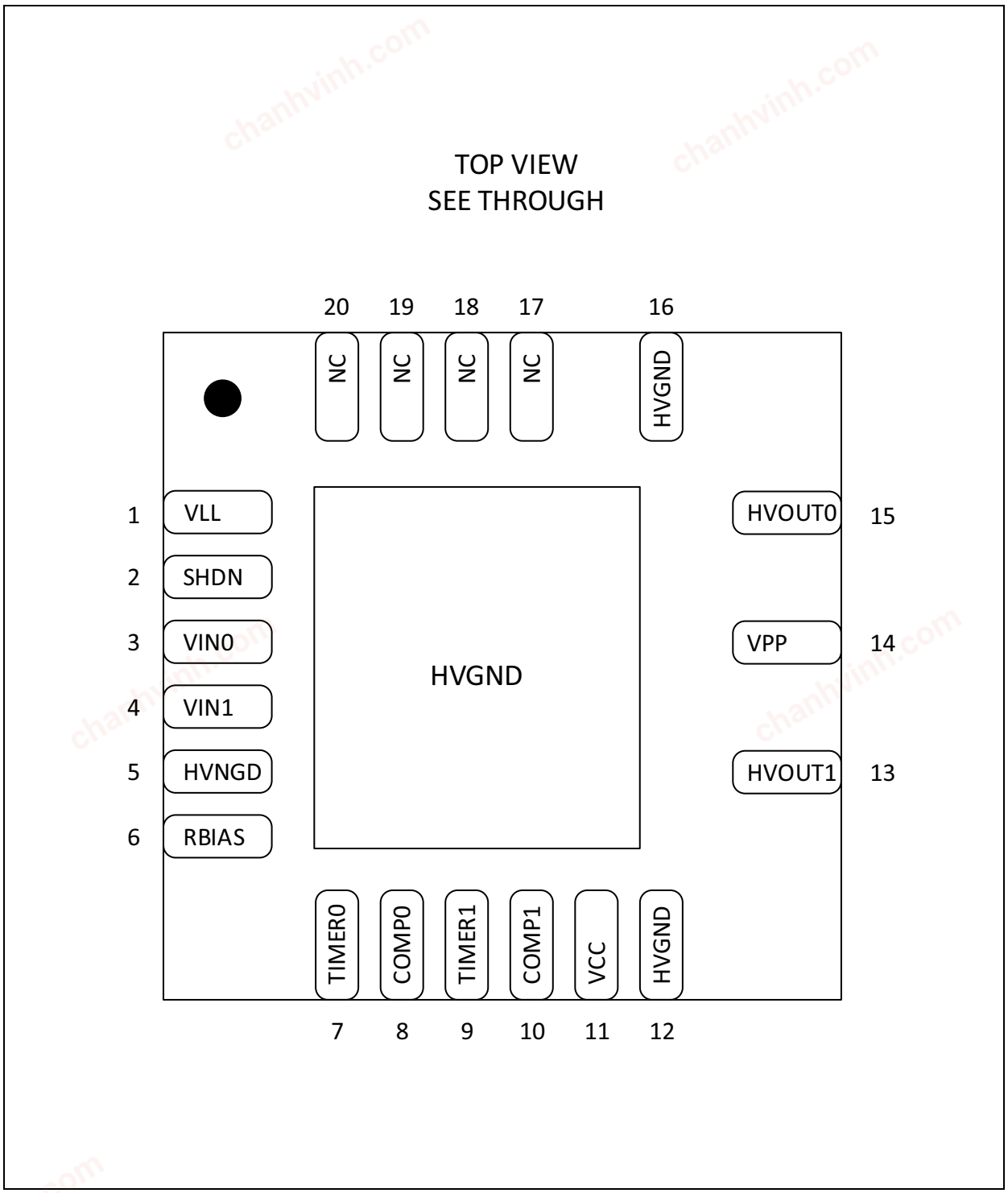


FIGURE 3-1: *VQFN 20-Lead 4x4 mm.*

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The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

PIN	NAME	FUNCTION
1	V_{LL}	Logic Input Voltage Supply
2	SHDN	Shutdown Input Pin
3	$V_{IN}0$	CH0 Amplifier Input
4	$V_{IN}1$	CH1 Amplifier Input
5	HVGND	High Voltage Ground
6	R_{BIAS}	Bias Reference for High Voltage Amplifiers
7	Timer0	Delay Timer 0
8	Comp0	Comparator Output 0
9	Timer1	Delay Timer 1
10	Comp1	Comparator Output 1
11	V_{CC}	Low Voltage Amplifier Supply
12	HVGND	High Voltage Ground
13	$HV_{OUT}1$	CH1 High Voltage Amplifier Output
14	V_{PP}	High Voltage Amplifier Supply
15	$HV_{OUT}0$	CH0 High Voltage Amplifier Output
16	HVGND	High Voltage Ground
17,18 19,20	NC	No Connection
Pad	HVGND	High Voltage Ground

Note: NC pins can be connected to HVGND to reduce the overall thermal resistance from the IC package to the PCB ground plane.

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3.1 Logic Voltage Supply Input Pin (V_{LL})

V_{LL} is the (3.3V) voltage source required for the comparator pins. A 1 µF bypass capacitor is recommended to be connected at the VLL input pin.

3.2 High Voltage Ground (HVGND)

Ground reference pins for the High Voltage Amplifiers.

3.3 Shutdown Input Pin (SHDN)

The Shutdown input pin is used to deactivate the High Voltage Amplifiers.

3.4 High Voltage Amplifiers Inputs ($V_{IN}0$, $V_{IN}1$)

Input data signals for the High Voltage Operational Amplifiers.

3.5 Amplifiers Bias Reference Pin (R_{BIAS})

High Voltage Amplifiers bias reference input pin. A 150 kΩ resistor will set the bias currents for a 124 Hz, -3 dB bandwidth for 225V sinusoidal waveforms driving 0.22 µF capacitive loads.

3.6 Output Voltage Comparator Output Pins (COMP0, COMP1)

The internal voltage comparators monitors the input data signals, $V_{IN}0/V_{IN}1$, and the High Voltage Amplifier's feedback signals for a short at the amplifiers outputs. The comparators monitor for a 20% (or greater) voltage drop in the output against the input signal before reporting a short flag, COMP0,1 = High or 3.3V.

3.7 Output Voltage Comparators Delay Timer Pins (Timer0, Timer1)

The output voltage comparators monitor the input data signals, $V_{IN}0/V_{IN}1$, against the HV Op-Amp feedback signals. If there is a heavy capacitive load the HVOUT signals will slowly increase, appearing to the comparator as a possible short. False triggering is avoided by adding a delay to the input signals of the comparators. A 1.5 nF capacitor will add a 1.6 ms delay time when R_{BIAS} is set to 150 kΩ.

Time Delay = $7.55*R_{BIAS}*C$ (Timer)

3.8 Low Voltage Supply Input Pin for High Voltage Amplifiers (V_{CC})

V_{CC} is the low voltage supply input pin for the High Voltage Op-Amps, with an operational voltage range of 6V to 7V. When HV56020 and HV56022 are used in the same solution, V_{CC} is intended to be powered from the HV56020 V_{DD} output pin. A 2 µF bypass capacitor is recommended to be added close to the V_{CC} pin.

3.9 High Voltage Amplifiers Outputs ($HV_{OUT}0$, $HV_{OUT}1$)

High Voltage Amplifiers Output channels.

3.10 High Voltage Amplifiers Supply Input Pin (V_{PP})

Input power supply pin for the High Voltage Op-Amps. V_{PP} is generated by the flyback configuration formed by the internal power MOSFET, the DC-to-DC Controller and the external transformer. The maximum operating voltage is 225V. A 0.1 µF bypass capacitor is recommended to be added close to the V_{PP} pin.

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4.0 FUNCTIONAL DESCRIPTION

The High Voltage Operational Amplifiers operate up to 225V and can source/sink 40 mA minimum peak currents. Amplifiers are designed for a -3 dB bandwidth of 124 Hz for 225V sinusoidal waveforms driving 0.22 µF capacitive loads. In addition, the amplifiers are paired with output voltage comparators to monitor and report short circuit conditions.

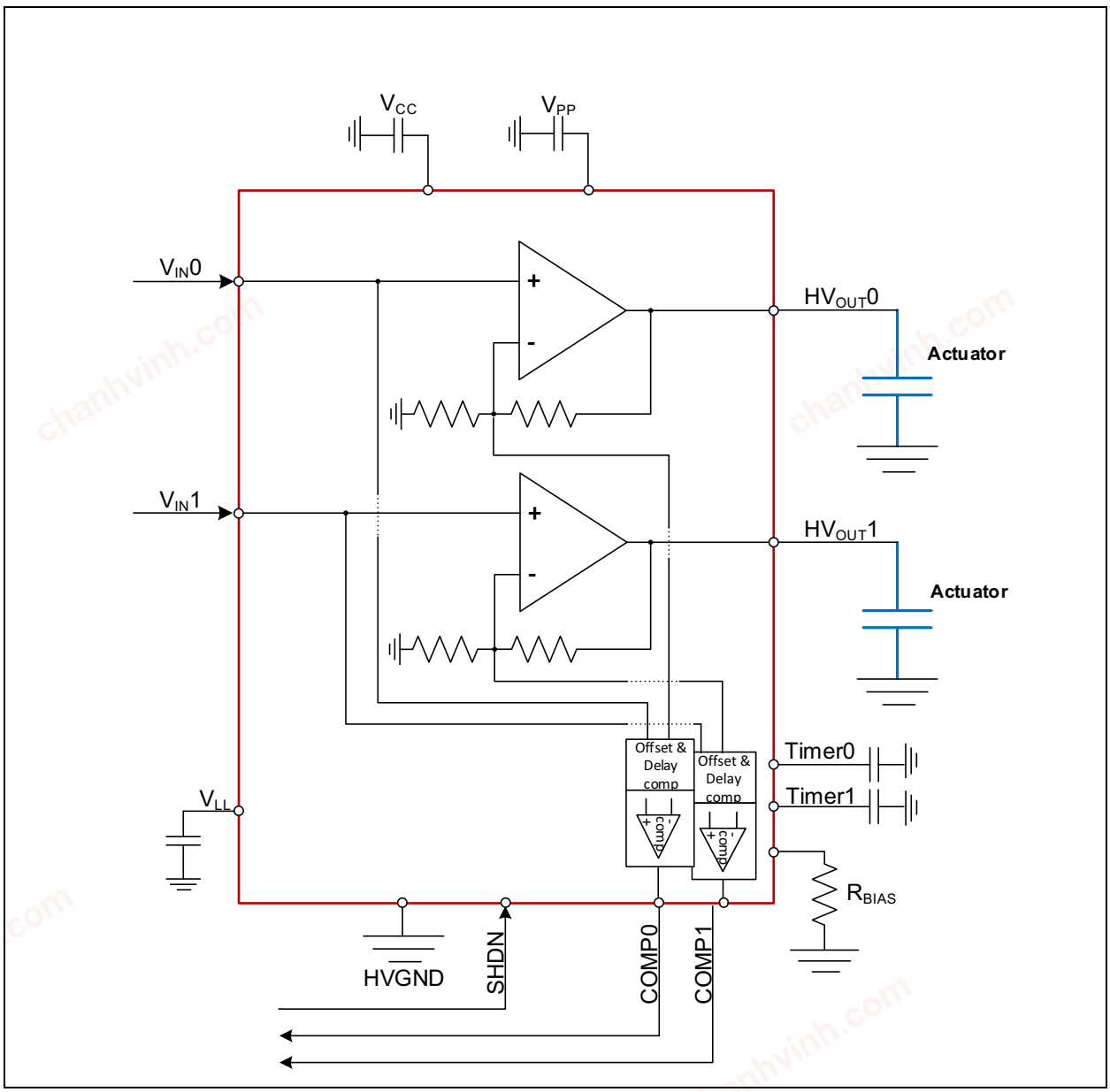


FIGURE 4-1: *Functional Block Diagram.*

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4.1 HIGH VOLTAGE OPERATIONAL AMPLIFIERS

The High Voltage Operational Amplifiers operate up to 225V (unipolar) with 40 mA minimum source/sink peak current capabilities and are designed with a fixed 75 V/V gain.

4.1.1 BANDWIDTH

The amplifiers' bandwidth is controlled in part by the internal bias currents set by an external resistor, **R_{BIAS}**. The internal bias currents can be increased by reducing R_{BIAS} to achieve higher bandwidth. Increasing the bandwidth will lead to higher power consumption. A 150 kΩ R_{BIAS} will set the bias currents to a 124 Hz -3 dB bandwidth for 225V sinusoidal waveforms driving 0.22 µF capacitive loads.

4.1.2 STABILITY

Amplifiers are designed to operate for a wide range of capacitive loads and to maintain stability when light or no loads are present. 10 nF preload capacitors, **C_{PRE}**, are recommended to be added in parallel with the outputs **$HV_{OUT}0$** and **$HV_{OUT}1$**. Figure 4-2 illustrates the application diagram using 10 nF preload capacitors.

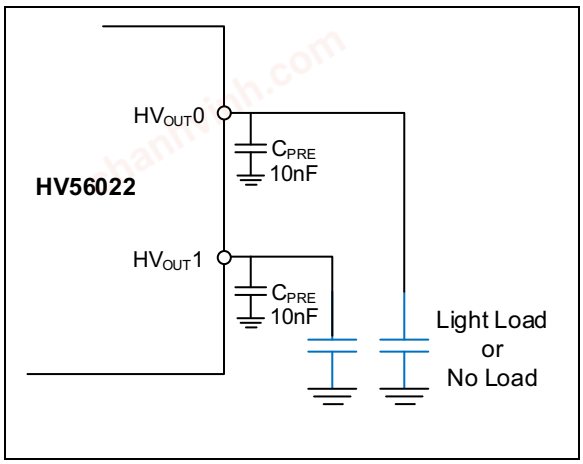


FIGURE 4-2: *Preload Capacitors.*

4.1.3 SHORT CIRCUIT DETECTION

Amplifiers are paired with voltage comparators for output short circuit detection. The Output Voltage Comparators, **COMP0** and **COMP1,** are a safety feature designed to check the voltage across the load (haptic actuator) during operation. Comparators monitor the amplifiers' feedback signals against 80% of the input signals, **$V_{IN}0$** and **$V_{IN}1$**. If there is a short or failing load (drooping voltage) at the output, a flag (High or 3.3V) will be raised by the comparators for the MCU (controlling host).

Comparators are designed with internal voltage offset, **V_{OFFSET}** (~110 mV) and delay timer pins, **Timer0** and **Timer1**, to prevent false triggering.

The internal voltage offsets are designed to avoid false triggering due to ground noise when input signals swing close to zero level.

Timer pins add delay compensation to the comparators inputs, **$V_{IN}0$** and **$V_{IN}1$**, by using capacitors at the Timer0 and Timer1 pins. When input signals are step functions (for example square waves), the amplifiers' outputs will slowly charge, producing trapezoidal waveforms. If input signals are not delayed, amplifiers' feedback signals will appear as short when compared to the input signals. A 150 kΩ R_{BIAS} and timer pins with 1.5 nF capacitors will provide a 1.6 ms delay. Figure 4-3 illustrates a false detection event when timer capacitors are not being used.

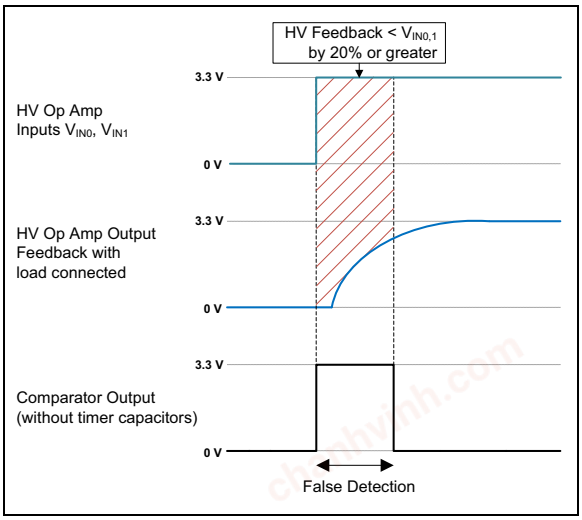


FIGURE 4-3: *False Detection.*

4.1.4 SHUTDOWN MODE

The shutdown mode, **SHDN**, disables the internal bias current, allowing for power saving when the amplifiers are not operating. SHDN = High or 3.3 V, disables the amplifiers.

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5.0 APPLICATION INFORMATION

The HV56022 is designed for haptic applications where high voltage drive and integration are required.

In haptic applications, communication with the user occurs via the skin's haptic sensory system. Electro-Mechanical Polymer (EMP) Actuators are used in the low frequency band to stimulate the skin's sensory system. The haptic sensory system band frequency range is targeted around 1 Hz to 200 Hz and greater frequencies are used for audible feedback. The HV56022 is designed to drive 0.22 µF actuators at 124 Hz (-3 dB Bandwidth) with 225V sinusoidal waveforms.

Haptic applications require multiple channels to cover parts of the body with susceptible haptic sensory systems. For multiple channel solutions where simultaneous data transmission is not a strict requirement, the HV56020 and HV56022 can be used to add extra channel drive capacity. The HV56020 is a Dual High Voltage Operational Amplifier with a Step-Up Converter and Power MOSFET. The HV56020 is used to add extra dual HV Amplifiers and to generate the required high voltage source, V_{PP}. The HV56020's V_{DD} and V_{LL} output voltages can be used to power HV56022's input voltage sources: V_{CC} (V_{DD}) and V_{LL}.

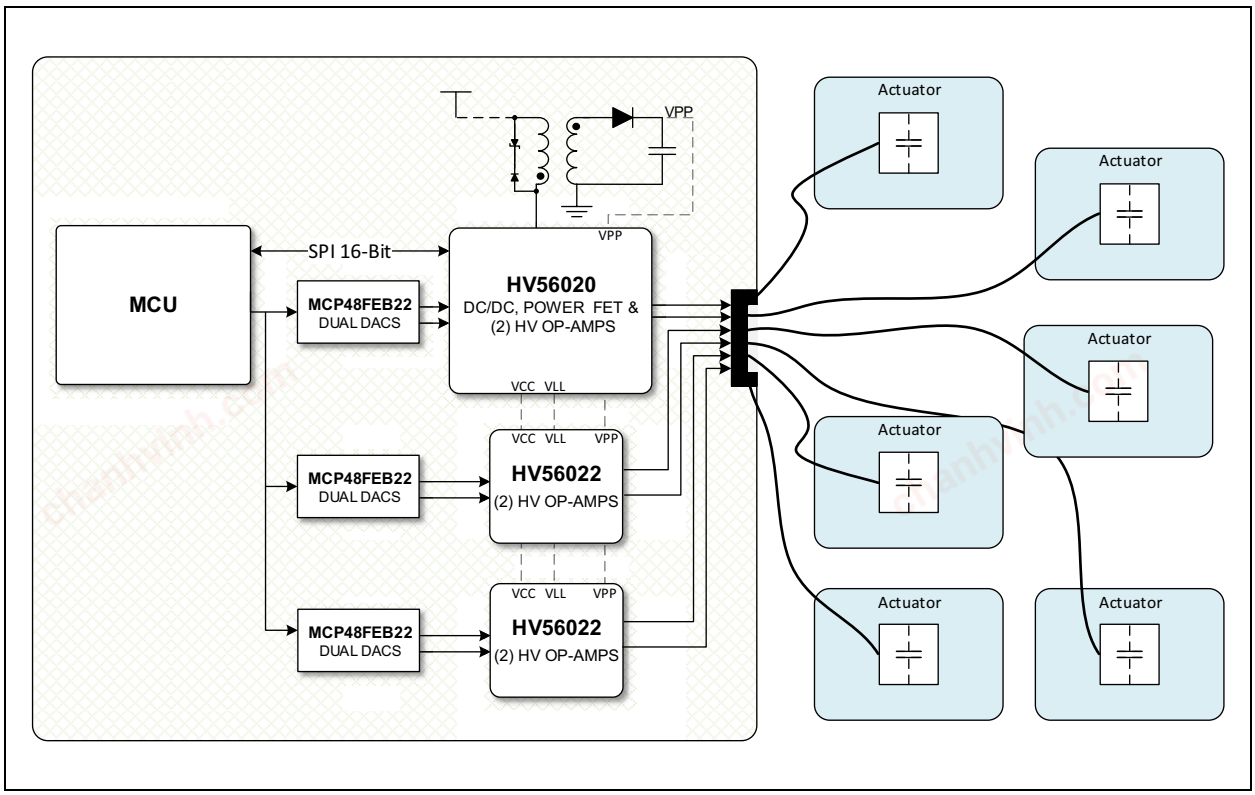


FIGURE 5-1: *Application Block Diagram.*

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5.1 PCB Layout Guidelines

The High Voltage Amplifiers can operate up to 225V with a 2.5 mA quiescent current (I_{PPQ}) during the idle state mode, dissipating 0.56 watts. During the transmission mode, the peak power can reach up to 3.7 watts (I_{PP} 16.5 mA typical) when driving both HV Amplifiers simultaneously with a 0.22 µF load using a 124 Hz sine wave. Average and peak power levels depend on the load capacitance and the input data waveform characteristics; frequency, amplitude, rise/fall times, and duration. The printed circuit board (PCB) layout design must accommodate for high power dissipation by having a low thermal resistance with the device, HV56022.

During normal operation actuators are expected to operate in burst modes with intermittent idle times, allowing for moderate power consumptions. Power consumption becomes a concern for the continuous mode of operation, where each amplifier can dissipate up to 1.8 watts of instantaneous power. Continuous operation modes will lead to high power consumption and in case of a poorly designed PCB, thermal runaway.

5.1.1 HV56022

The HV56022 consists of dual High Voltage Operational Amplifiers. The HV Amplifiers sit on the package lead frame **Pad** connected to High Voltage Ground, **HVGND**. Most of the heat generated by the device will flow via the package lead frame Pad and a minor heat portion via the package mold compound and to the air via convention.

5.1.2 PCB LAYOUT

The thermal resistance from the device's silicon→die attach→Pad→PCB must be minimal to pull the heat out of the package as fast as possible. Low thermal resistance is achieved by the exposure of the pad's connections to great quantity of copper. It is recommended to use numerous via connections to the internal planes (HVGND connections) and by employing copper pour technique at the Top and Bottom Layers connecting the pads. Figure 5-2 illustrates the suggested layout for the copper pour and via connections in the Top-Layer.

The HVGND copper pour must be continuous throughout most of the PCB Top-Layer and regions containing the HV56022. HVGND connection pathways 1, 2, 3, and 4 must be cleared of components and signal traces to avoid cutting the ground plane and reducing the copper content in the Top Layer (see Figure 5-2). Small footprint components, e.g. 0402 EIA size code, and routing signal traces in the inner layers are recommended. Components for the **RT**, **TON**, **Timer Delay**, and **R_{BIAS}** pins must be placed out of the HVGND pathways, or at the Bottom-Layer. Trace routing for V_{IN}0,1 can be placed in the inner layers to avoid cutting the top ground plane.

Note: The standoff –spacing– for high voltage signal must be maintained in all layers/planes in accordance with the UL840 pollution level 1; where a 0.56 mm minimum creepage spacing is recommended for 250V DC or AC RMS operation.

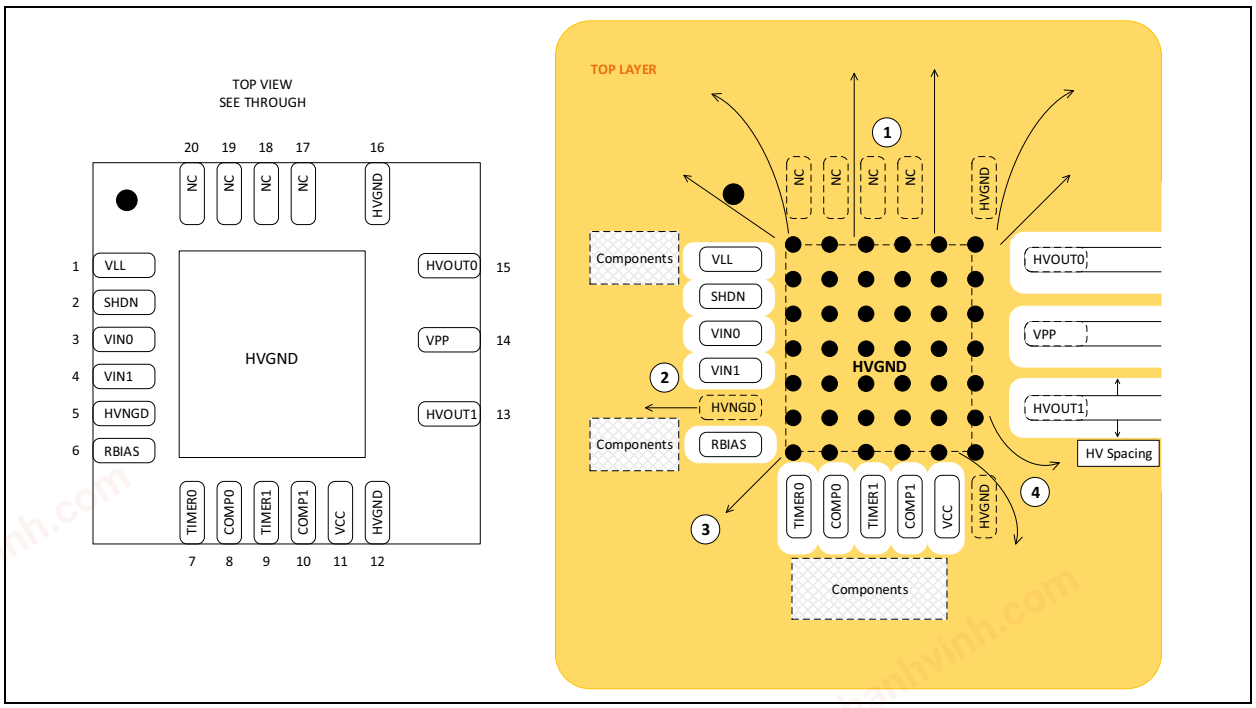


FIGURE 5-2: *HV56022 Layout.*

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5.1.3 PCB STACK-UP

The PCB is recommended to have a Stack-Up with at least 4 layers - or higher count preferably - to increase the ground, HVGND, copper content and help with the heat dissipation. The **Top** and **Bottom Layers** must be **2 Oz** while the rest of the planes and layers can be 1 Oz.

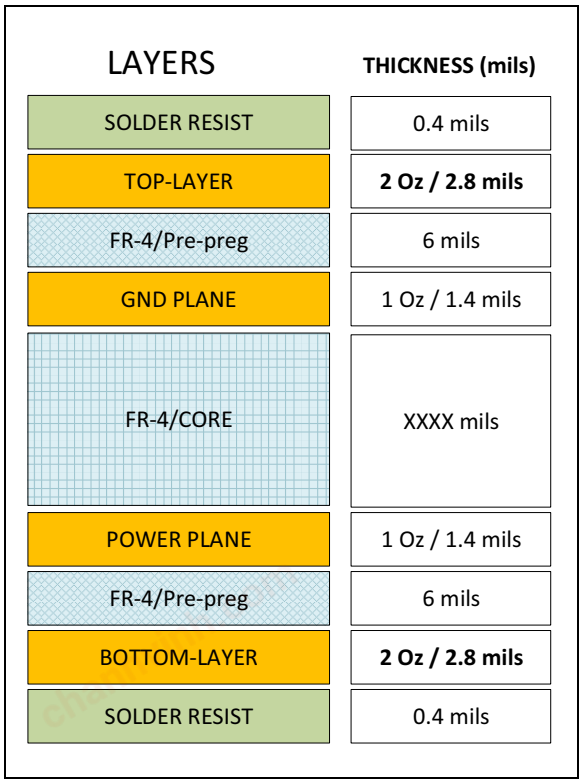


FIGURE 5-3: *PCB Stack-Up.*

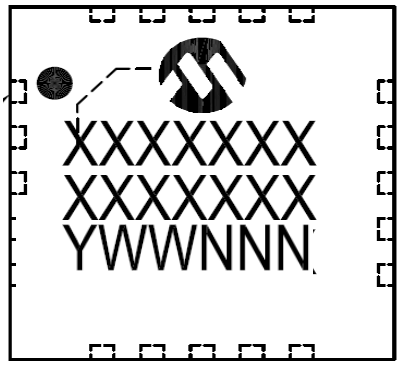
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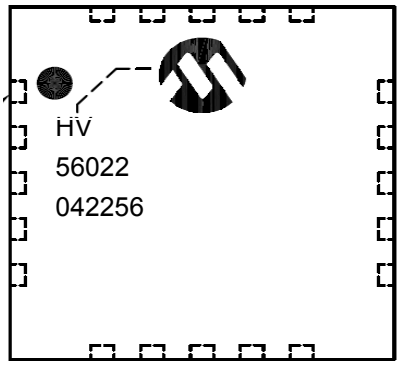
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

20-Lead VQFN



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

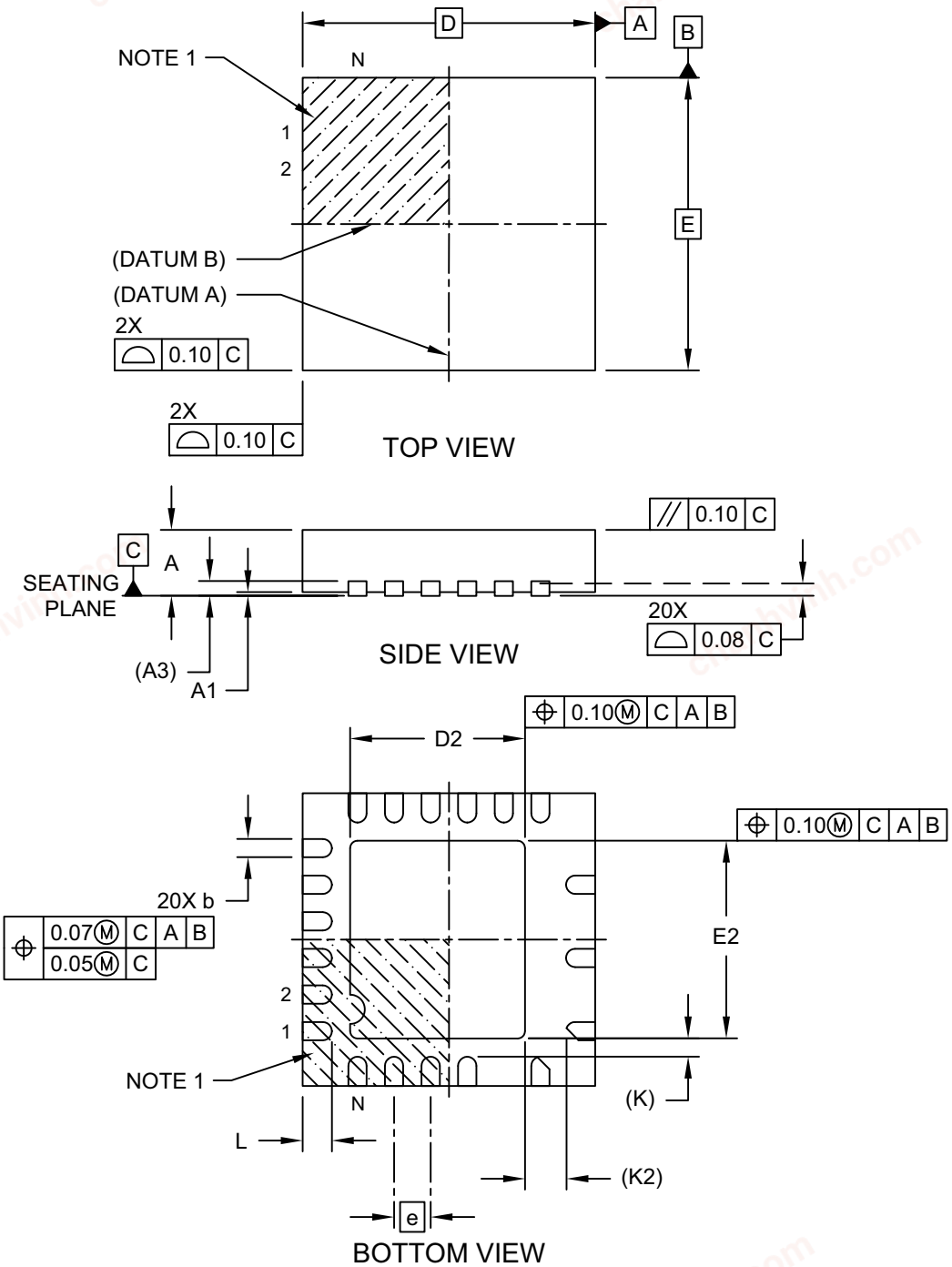
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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20-Lead Plastic Quad Flat, No Lead Package (KNX) - 4x4 mm Body [VQFN] 0.40 mm Terminal Length

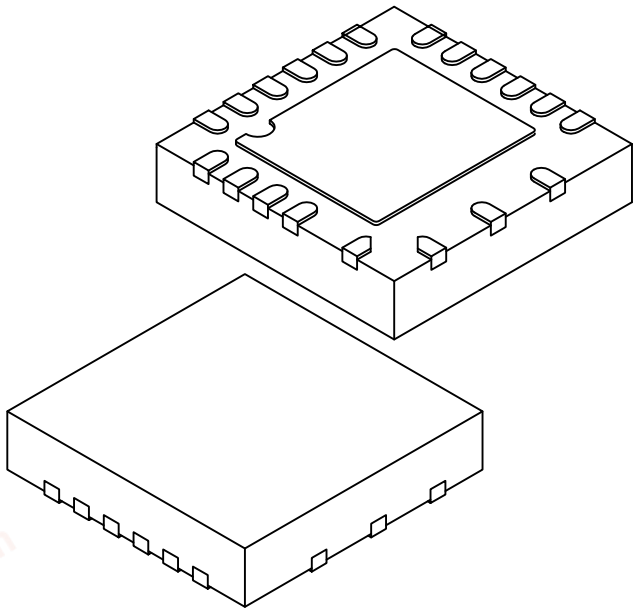
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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20-Lead Plastic Quad Flat, No Lead Package (KNX) - 4x4 mm Body [VQFN] 0.40 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.29	2.39	2.49
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed Pad	K		0.25 REF	
Terminal-to-Exposed Pad	K2		0.56 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

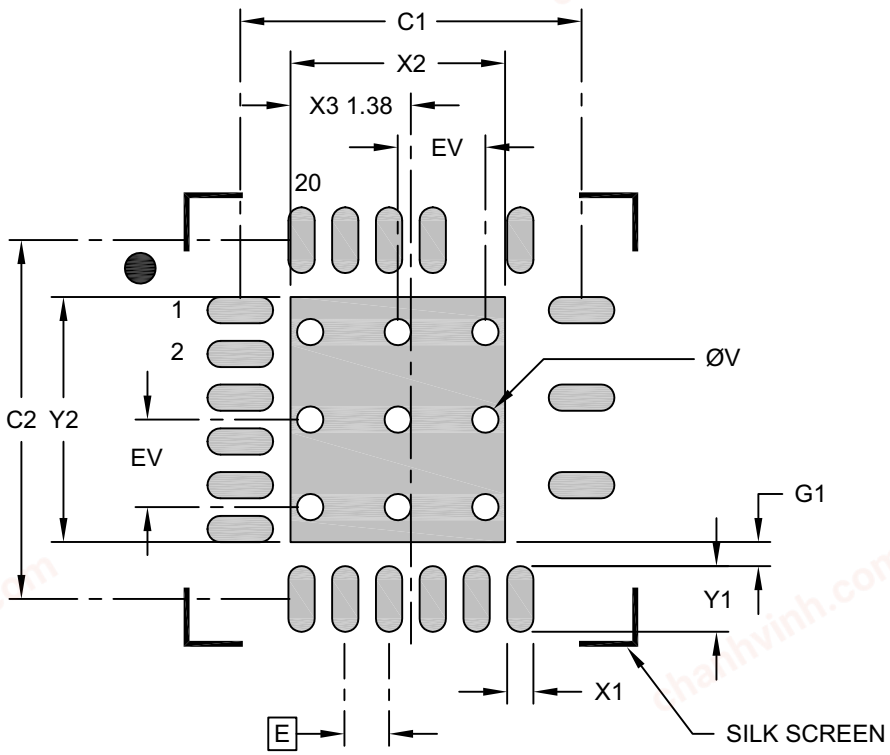
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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20-Lead Plastic Quad Flat, No Lead Package (KNX) - 4x4 mm Body [VQFN] 0.40 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			2.45
Center Pad Offset	X3			1.38
Center Pad Length	Y2			2.80
Contact Pad Spacing	C1		3.90	
Contact Pad Spacing	C2		4.10	
Contact Pad Width (X20)	X1			0.30
Contact Pad Length (X20)	Y1			0.75
Contact Pad to Center Pad (X20)	G1	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (March 2020)

- Initial release of this document.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-X	/XXX
Device	Tape and Reel Option	Temperature Range	Package

Device:	HV56022: Dual High Voltage Operational Amplifiers		
Media Type	T	=	3300/Reel for KNX Package
Temperature-Range:	V	=	-0°C to +125°C (Industrial) Lead (Pb)-free/RoHS Compliant
Package:	KNX	=	20-Lead Very Thin Quad Flatpack) 4 x 4 x 0.9 mm VQFN

Examples:

a)HV56022T-V/KNX: Dual High Voltage Operational Amplifiers
Industrial Temperature,
20-Lead VQFN Package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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