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MEC141x Family Device MECC Evaluation Board User's Guide

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Signed for and on behalf of Microchip Technology Inc. at Chandler, Arizona, USA

Derek Carlson
VP Development Tools

12-Sep-14
Date

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MEC141X FAMILY DEVICE MECC EVALUATION BOARD USER'S GUIDE

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Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our web site (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXA", where "XXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the MEC141x family device MECC evaluation board. Items discussed in this chapter include:

- Document Layout
- Audience
- Reference Documents
- Glossary
- The Microchip Web Site
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document describes how to use the MEC141x family device MECC evaluation board (ASSY-6760 Rev. A) to mate with Intel's latest generation reference board's MECC connector or use as standalone development board. The User Guide layout is as follows:

- **Chapter 1. "Overview"** – An introduction and overview of the MEC141x MECC Board.
- **Chapter 2. "Evaluation Boards"** – Includes hardware setup information and demonstration procedures.
- **Appendix A. "Intel Skylake Platform Rework Instructions"** - Provides the rework steps for the Intel Skylake RVP motherboard, eSPI configuration with the MEC141x MECC Add-In Board.

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AUDIENCE

This document is written for developers who are familiar with testing and design of Intel personal computer mobile systems, or generic embedded controller applications environment. The purpose of this document is to describe the functions and use of the MEC141x family device MECC evaluation board when connected to Intel's latest generation reference validation platform (RVP) that supports the MECC connector to perform the appropriate drivers, BIOS, and components development and validation, or running standalone for other embedded controller applications.

REFERENCE DOCUMENTS

- MEC140x/1x Data Sheet, Rev. A
- MEC140x/1x eSPI Addendum, Rev. A
- ASSY. 6760A - MEC141x 128 VTQFP eSPI MECC Card, Rev. A1.0 Schematics
- MPLABX IDE Tools Documentation
  - http://www.microchip.com/pagehandler/en-us/family/mplabx
- Intel eSPI Specification, June 2013, Revision 0.75 (Doc#: 327432-003)
- Intel Skylake Platform Design Guide, June 2014, Revision 0.9 (Doc#: 543016)
- Intel Skylake Ultrabook Platform Y-Series RVP3 CRB Schematic, March 2014, Revision 0.72 (Doc#: 544250)
- Intel Skylake Y EC AIC Enable Document for rework instructions to enable eSPI

GLOSSARY

This section describes glossary terms and acronyms used in this document.

TERM	DEFINITION
EVB	Evaluation Board
MECC	Modular Embedded Controller Card
ASSY.	Assembly Number Assigned to the Microchip EVB
ACPI	Advanced Configuration and Power Interface
BIOS	Basic Input/Output System
ASL	ACPI Source Language
EC	Embedded Controller
AIC	Add-In Card
LPC	Low Pin Count
eSPI	Enhanced Serial Peripheral Interface

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- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
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The Development Systems product group categories are:

- **Compilers** – The latest information on Microchip C compilers, assemblers, linkers and other language tools. These include all MPLAB C compilers; all MPLAB assemblers (including MPASM assembler); all MPLAB linkers (including MPLINK object linker); and all MPLAB librarians (including MPLIB object librarian).
- **Emulators** – The latest information on Microchip in-circuit emulators.This includes the MPLAB REAL ICE and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICkit 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are nonproduction development programmers such as PICSTART Plus and PIC-kit 2 and 3.

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- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at:
http://www.microchip.com/support

DOCUMENT REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS50002312B (10-24-16)	Document Release	

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Chapter 1. Overview

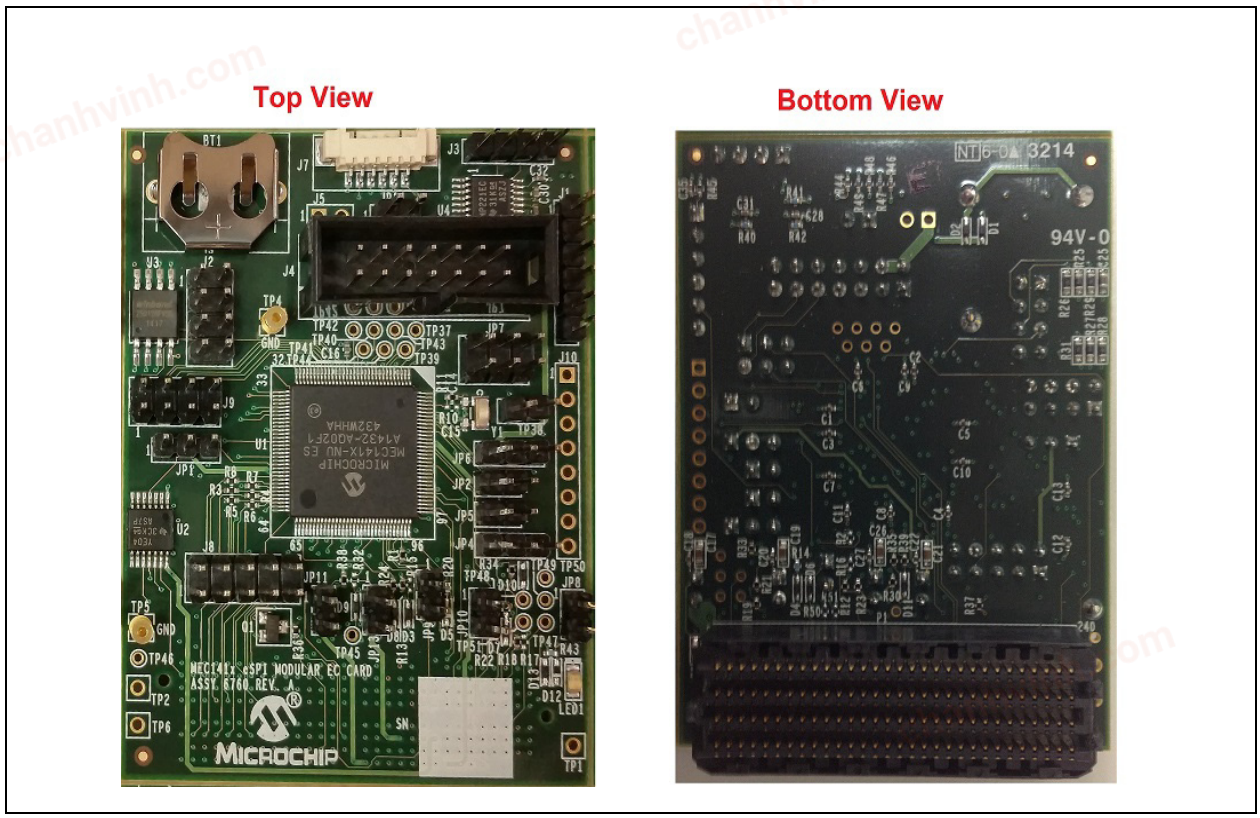
1.1 INTRODUCTION

The MEC141x family device MECC evaluation board (ASSY 6760A) is mainly designed to be used with the Intel Skylake Y-Series RVP platform. The MECC board is a vehicle to support the development of BIOS, drivers, firmware, and so forth. This evaluation board can be also used as a standalone embedded controller development board for embedded and industrial computing applications.

The purpose of this document is to describe the functions of the MEC141x MECC eSPI Plug-In card as well as the setup procedures for full system development, to validate applications, or to power-up as standalone board for application development.

There are several on-board LPC devices on the Intel Skylake RVP platform. There is also an on-board MECC (AIC) connector to provide the capability for other vendors to develop and test their LPC/eSPI devices. The MEC141x family device MECC evaluation board is designed to plug into the MECC connector to demonstrate the operation of the MEC141x family devices on this platform. This user manual focuses on the Keyboard Controller and Embedded Controller functions available on the plug-in card.

FIGURE 1-1: MEC141X MECC CARD (ASSY 6760A) TOP & BOTTOM VIEWS



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1.2 INTEL PLATFORM SETUP REQUIREMENTS

1.2.1 Hardware

- Intel Skylake Y-Series RVP Platform (with eSPI support)
- Microchip MEC141x family device MECC Card (ASSY 6760A)
- SPI Flash Programmer
  - Dediprog SF100 (http://www.dediprog.com/pd/spi-flash-solution/sf100)
- Skylake specific LCD Display or eDP support LCD Monitor
- 2.5" Notebook SATA HDD
- USB or PS/2 Keyboard & Mouse
- Optional - Microchip Pegasus Trace FIFO Debugger (Part#: PEGASUS-EVB)
- Optional - Select one of the Microchip Debugger Tools
  - PICKit3 (Part#: PG164130)
  - ICD3 (Part#: DV164035)
  - Real ICE (Part#: DV244005)
  - RJ11 to ICSP Adapter (Part#: AC164110) - Required for ICD3 or Real ICE

1.2.2 Software

- Microchip MPLABX IDE v2014-08-22 or later
- Microchip XC32 PRO Compiler v1.33 or later
- SPI Flash Programming Utility (ex: Dediprog utility)
- Microchip MEC141x SPI Flash Generator Utility
- Microchip MEC141x Firmware Sample Code

1.2.3 BIOS Support

Please contact Intel or your BIOS vendors if you need any BIOS related information or support.

1.3 STANDALONE SETUP REQUIREMENTS

1.3.1 Hardware

- Microchip MEC141x family device MECC Card (ASSY 6760A)
- External +3.3V Power Supply
- SPI Flash Programmer
  - Dediprog SF100 (http://www.dediprog.com/pd/spi-flash-solution/sf100)
- Optional - Microchip Pegasus Trace FIFO Debugger (Part#: PEGASUS-EVB)
- Optional - Select one of the Microchip Debugger Tools
  - PICKit3 (Part#: PG164130)
  - ICD3 (Part#: DV164035)
  - Real ICE (Part#: DV244005)
  - RJ11 to ICSP Adapter (Part#: AC164110) - Required for ICD3 or Real ICE

1.3.2 Software

- Microchip MPLABX IDE v2014-08-22 or later
- Microchip XC32 PRO Compiler v1.33 or later
- SPI Flash Programming Utility (ex: Dediprog utility)
- Microchip MEC141x SPI Flash Generator Utility
- Microchip MEC141x Firmware Sample Code

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Chapter 2. Evaluation Boards

This chapter describes the MEC141x family device MECC card (ASSY 6760A) detailed information.

2.1 FEATURES

The MEC141x MECC Evaluation Board has the following components and features:

2.1.1 MEC141x MECC Evaluation Board (ASSY. 6760A)

- MEC141x Embedded Controller
- 32 KHz Crystal
- SPI Flash (W25Q128FV)
- UART Transceiver
- Power LED
- Connectors / Headers:
  - Intel MECC (AIC) Connector
  - eSPI Access Header
  - Powers Isolation Headers
  - SPI Flash Programming header (for Dediprog SF100 pin-out)
  - Two pins UART header
  - Unused GPIO headers
  - JTAG/ICSP debugger headers
  - Pegasus debugger header

2.2 HARDWARE SETUP

2.2.1 Intel Skylake Y-Serial RVP

- Plug-In LCD Display or Monitor
- Plug-In USB or PS/2 Keyboard and Mouse
- Plug-In USB DVD-ROM if required to install Windows
- Plug-In 2.5" SATA HDD
- Plug-In Skylake platform power adapter
- Press the power button to make sure the platform is boot-able to UEFI Shell or Windows 8.x

2.2.2 MEC141x MECC Evaluation Board (ASSY 6760A)

- Refer to Table 2-1 for jumper settings.

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TABLE 2-1: JUMPER SETTINGS ON MEC141X MECC BOARD (ASSY 6760A)

Jumper	Function	Setting
JP1	VTR_33_18 Power Select	<1-2> for +1.8V <2-3> for +3.3V (Default)
JP2	ADC_DAC_VREF to +3.3V	<IN> Connected (Default) <OUT> Disconnected
JP4	PECI VREF_CPU power select	<1-2> Connect to Intel platform (Default) <2-3> Connect to ground
JP5	VTR to +3.3V	<IN> Connected (Default) <OUT> Disconnected
JP6	VBAT to +3.3V or Coin Battery	<IN> Connected (Default) <OUT> Disconnected
JP7	TFDP or UART signals select	<1-3 & 2-4> Connect to Pegasus TFDP header (Default) <3-5 & 4-6> Connect to UART header
JP8	+3.3V to V3.3V_EC_CORE	<IN> Connected (Default) <OUT> Disconnected
JP9	nRESET_IN Group Option	<IN> Connected to ground (use for SPI flash program) <OUT> Disconnected (Normal Operation)
JP10	System +3.3S to EC V3.3S power well	<IN> Connected (Default) <OUT> Disconnected
JP11	System +3.3A_RTC to EC V3.3A_RTC power well	<IN> Connected (Default) <OUT> Disconnected
JP13	System 1.8V_ESPI to EC RSVD_1.8V_ESPI power (Reserved for internal only)	<IN> Connected <OUT> Disconnected (Default)
JP14	Grounded ICSP_MCLR	<IN> Grounded <OUT> Not grounded (Default)
J1	Microchip ICSP Header	Connect to Microchip PICKit3 or ICD3 or Real ICE debugger
J2	SPI programming header	Connect to Dediprog SF100 SPI flash programmer
J3	Two pins UART header	Connect to UART (Null-modem) Cable
J4	Trace FIFO Debugger header	Connect to Microchip Pegasus board
J5	Ground the +5V Target Power	Not Used - Do Not Connect
J7	1x6 JTAG Header (Reserved for internal only)	Not Used - Do Not Connect
J8	eSPI Access Header	Not Used - Do Not Connect
J9	Unused GPIOs Header	Not Used - Do Not Connect
J10	Empty Header	Not Used - Do Not Connect
TP1	+V3.3A	Test Point for V3.3A power
TP2	EC_SPI_OE__N	Test Point for System EC_SPI_OE_N signal
TP4, TP5,	Ground	Test Points to ground
TP6	VREF_ADC	Test Point for VREF_ADC power

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2.3 SOFTWARE SETUP

2.3.1 Microsoft Windows 8.x on Intel SkyLake Platform

- Make sure the Intel Skylake platform is boot-able and able to complete the Microsoft Windows 8.x installation accordingly, and able to boot to the Windows 8.x.
- Please contact your Intel representative if you need any further assistance.

2.3.2 Microchip XPLABX IDE

- Install the beta version 2014-08-22 or later.
- Double click on the installation file, MPLABX-v2014-08-22-windows-installer.exe under the developer's windows machine.
- Follow the instructions to complete the installation.
- Please contact your Microchip representative if you need any further assistance.

2.3.3 Microchip XC32 PRO Compiler

- Install the beta version 1.33 (that supports the MEC141x family devices) or later.
- Double click on the installation file, xc32-v1.33-full-install-windows-installer.exe under the developer's windows machine after installing the MPLABX.
- Follow the instructions to complete the installation.
- At the end of installation, please follow the instruction to activate the XC32 PRO license key.
  - User can use xclm.exe in the compiler directory (ex: C:\Program Files (x86)\Microchip\xc32\v1.33\bin) to check the status by "xclm -status" command.
- Please contact your Microchip representative if you need any further assistance.

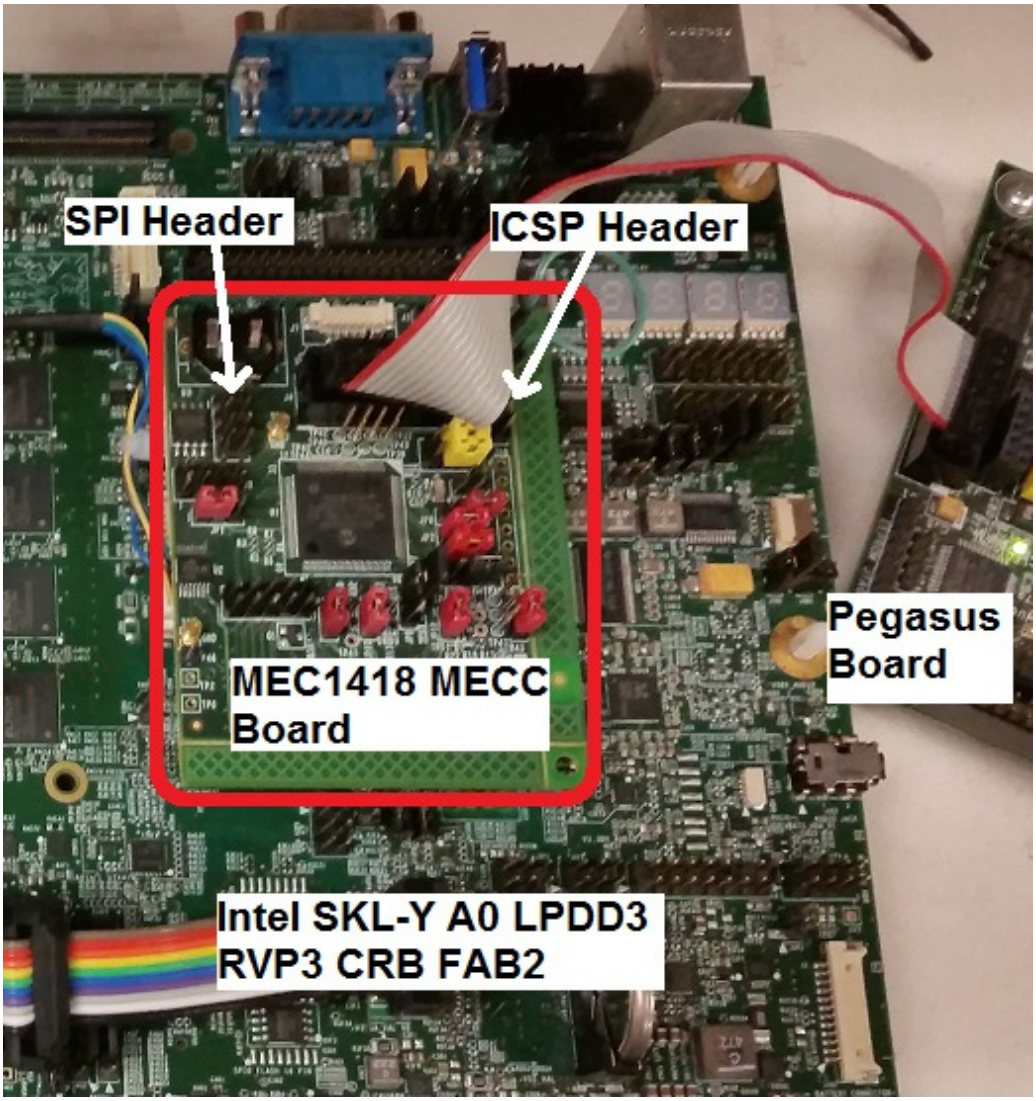
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2.4 HARDWARE CONNECTION

2.4.1 Intel Skylake Y-Serial RVP Connection

This section shows the hardware connection between Intel Skylake RVP platform and the Microchip MEC141x family device MECC evaluation board along with other components.



1. Connect Microchip Real ICE to the MECC J1 with RJ-11 to ICSP adapter
2. Connect Pegasus Trace Debugger to the MECC J4 – for trace debugging
3. Connect Dediprog SF100 to J2 for SPI flash programming

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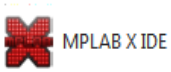
2.4.2 Standalone MEC141x MECC Card Connection

In the standalone setup, on top of steps 1 to 3 as described above for debug and development tools connections, we need to connect the power from external +3.3V power source since we don't have the sources from Intel platform.

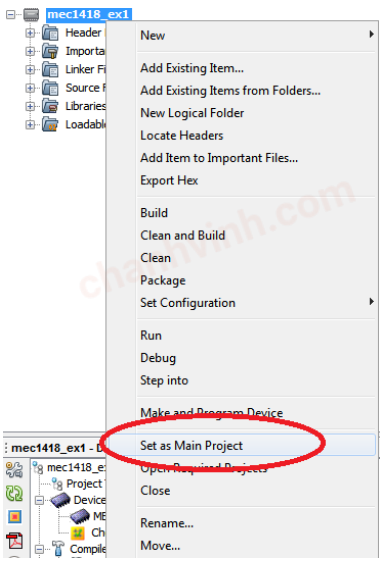
4. Connect MEC141x MECC Card JP8 Pin 1 (3.3_EC_CORE) to an external +3.3V power supply.
5. Connect a solid good ground source from the same power supply to the MEC141x MECC Card ground pin such as TP38 Pin 2, or TP4, or TP5, etc.

2.5 MPLAB IDE BRING UP

1. Launch the IDE - from Start →All Programs → Microchip → MPLAB X IDE →



2. Open Existing project – MPLabx IDE →File→ Open Project, Navigate the browser to the project setting files  which have the project name with .X extension. Right Click on project name and set Project as main project.

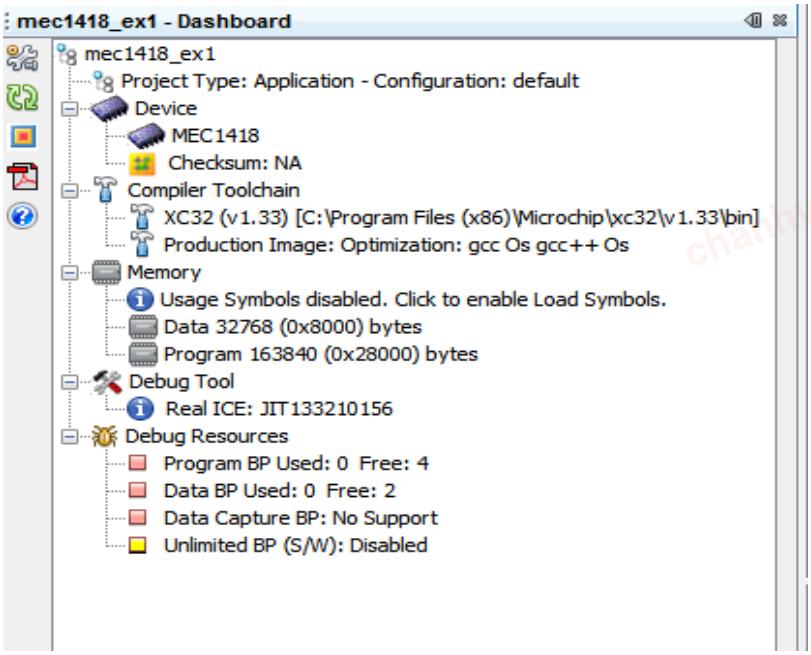


2.6 MPLAB IDE DASHBOARD

MPLABX IDE → Window → DashBoard will give details of the project for:

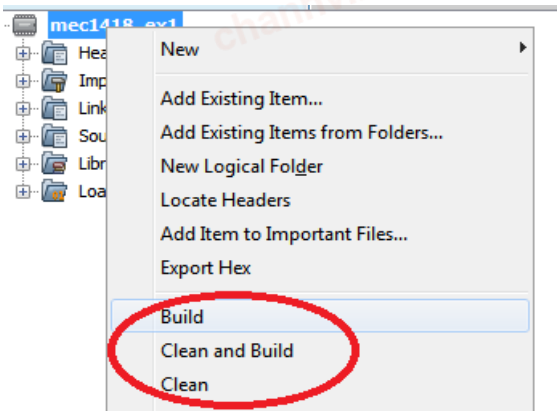
1. Compiler Toolchain
2. Memory Used
3. Debug tool
4. Debug resources

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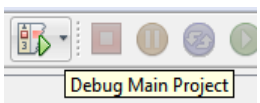
2.7 PROJECT CLEAN AND BUILD

To compile the project, right click on project name and choose either "Build", "Clean and Build", or "Clean" option. From Menu bar MPLABX IDE→ Run → Build Main Project / Clean and Build.



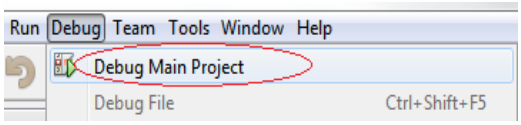
2.8 BUILD PROJECT FOR DEBUGGING

To debug the project with Real ICE, make sure the connection is correct and the proper Drivers are installed for the Debugger.

From the Menu Bar select 

or

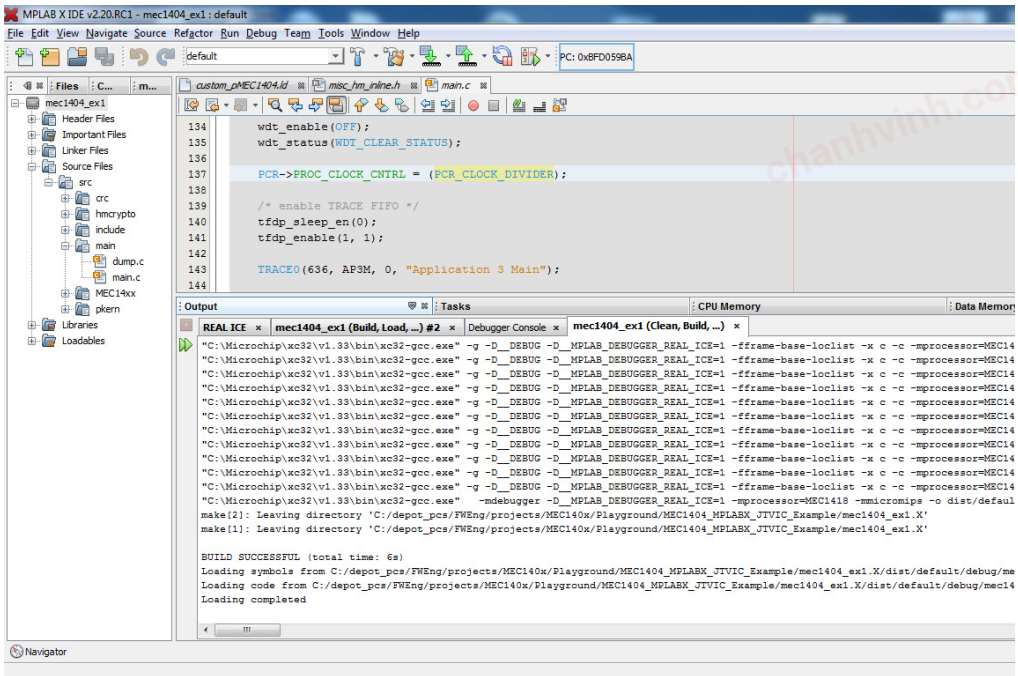
From MPLABX IDE →



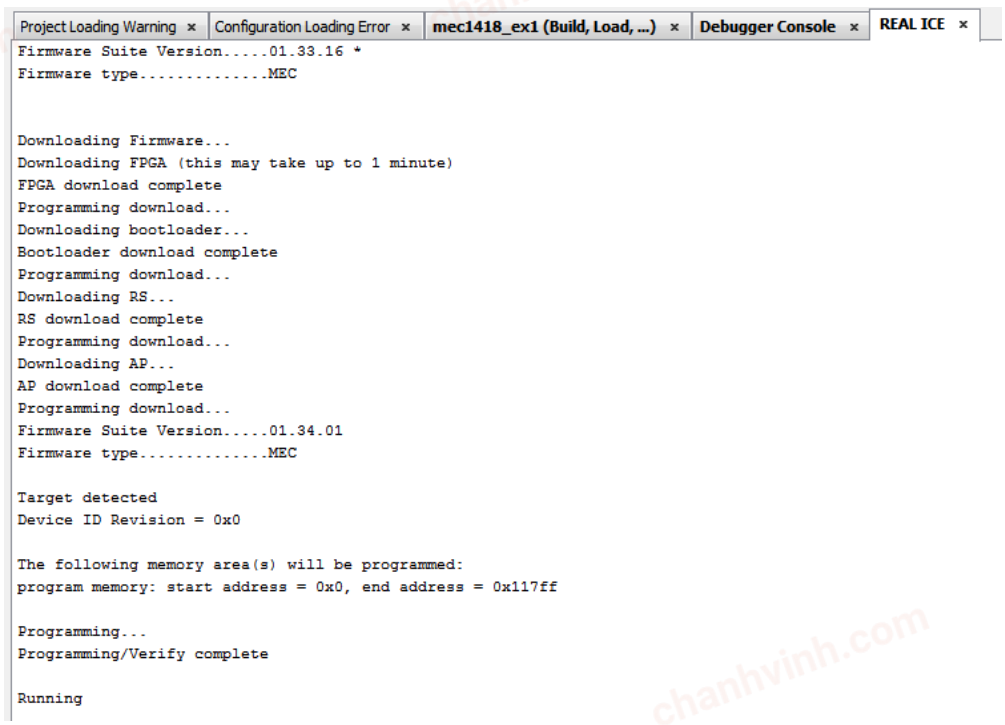
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Project will be rebuilt with debug option.



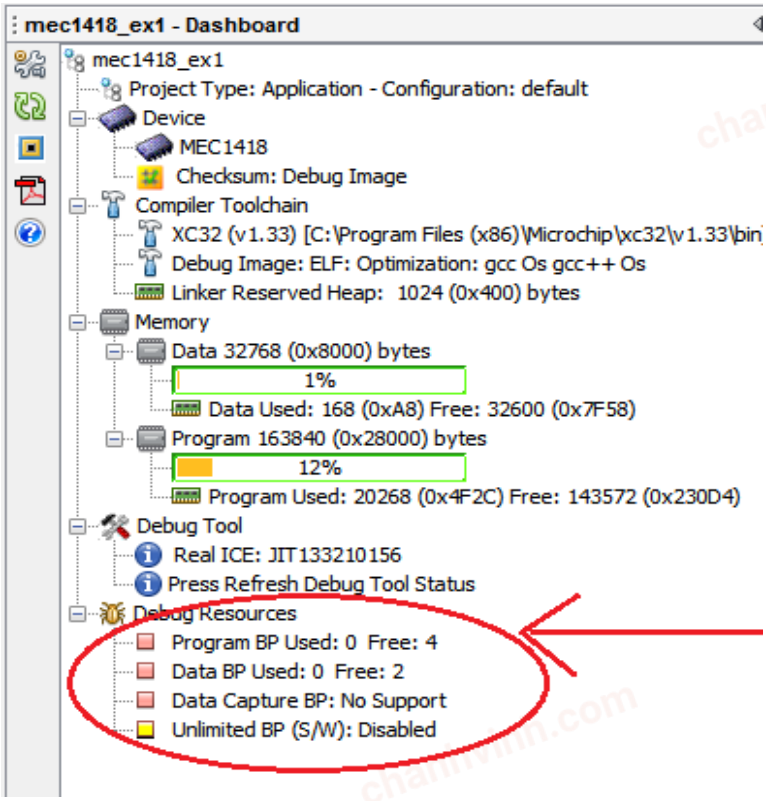
A successful build, if Real Ice is connected, will establish the connection and download the code to the target board for debugging.



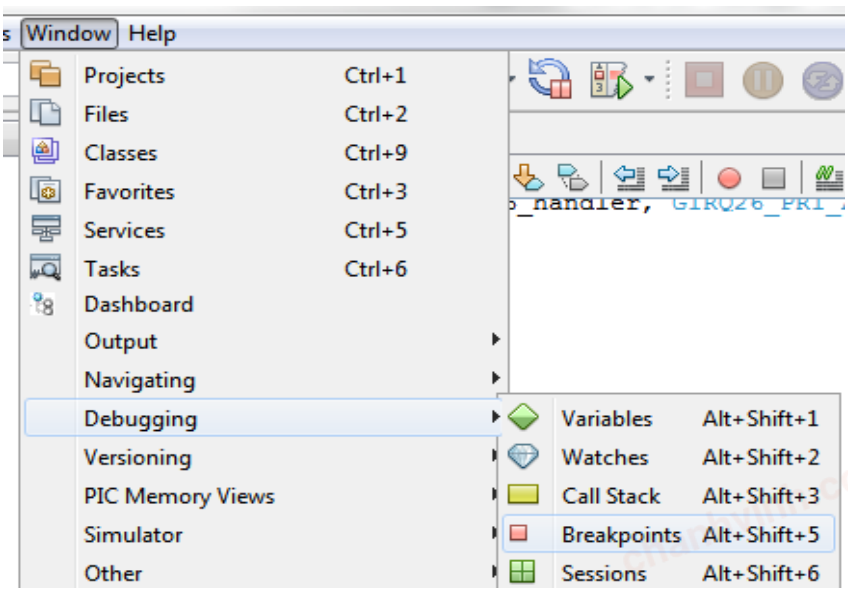
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2.8.1 Breakpoints

Breakpoints can be set before launching the debug option or while target device is halted. From Dashboard menu we can see the breakpoints available / used.



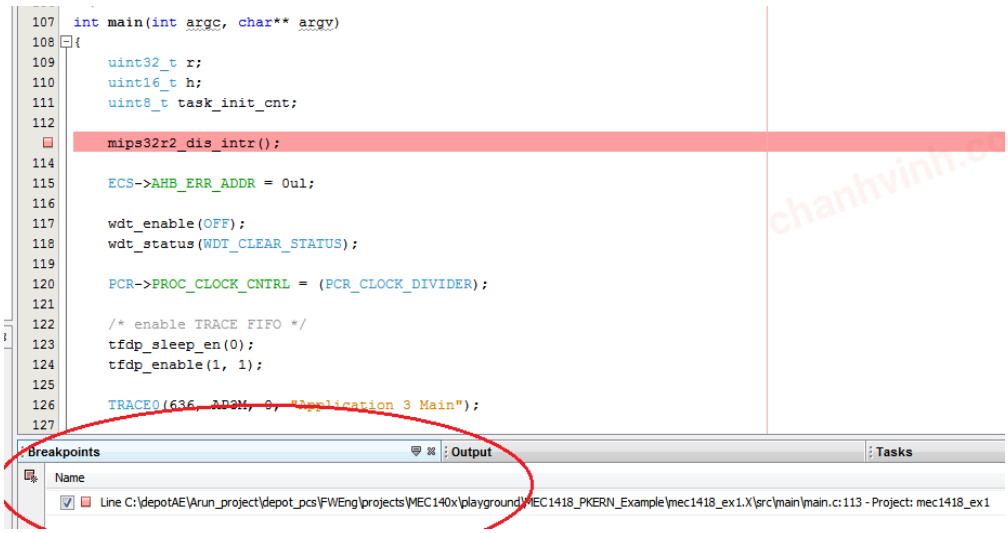
Set the break point as required – the break points can be viewed from Menu bar → Windows → Debugging → Breakpoints or short cut key Alt + Shift + 5.



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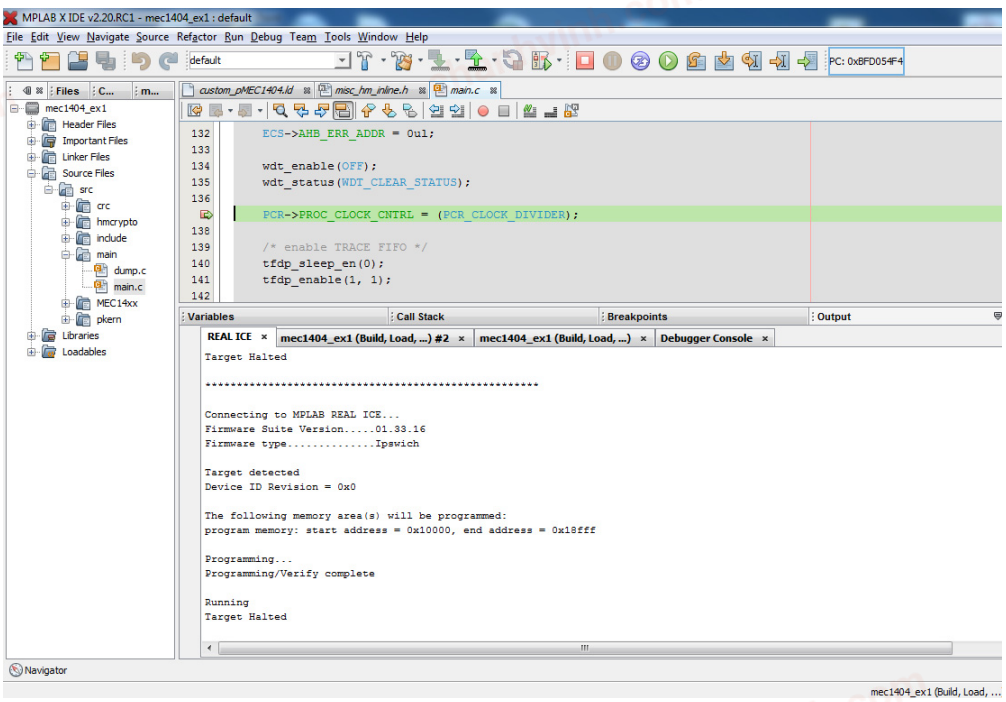
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Previously set Break points can be enabled or disabled using the select option.



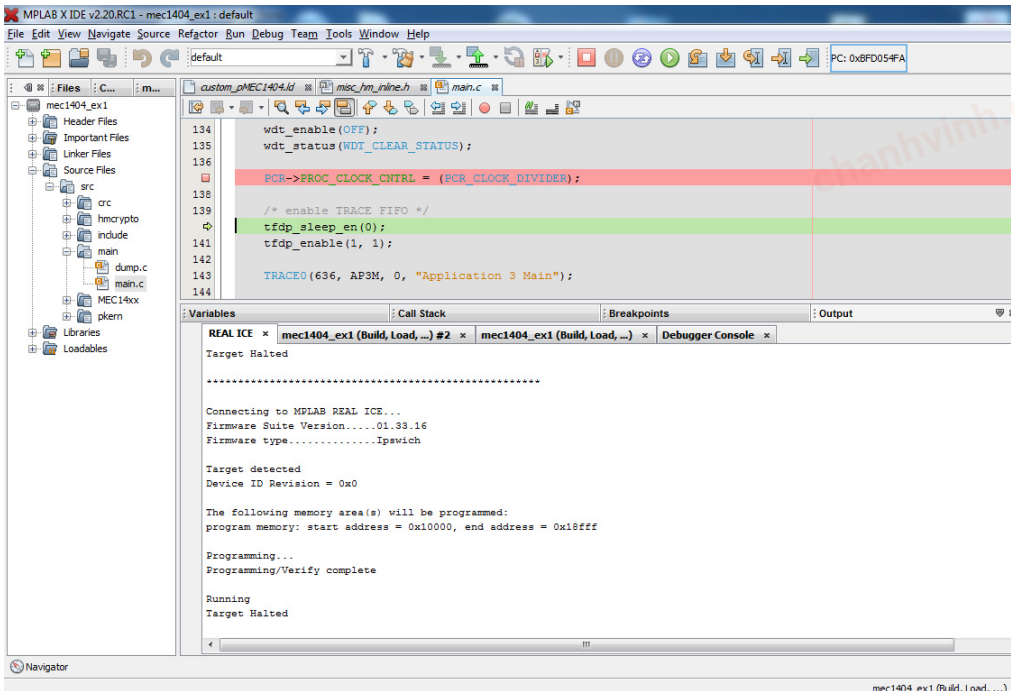
2.8.2 Enter Debug Task

Select Debug Project (project name xxx) from Menu Bar, IDE will connect ICE and project code into chip, then initiate to execute the code, code will be halted at the breakpoint which use previous settings.



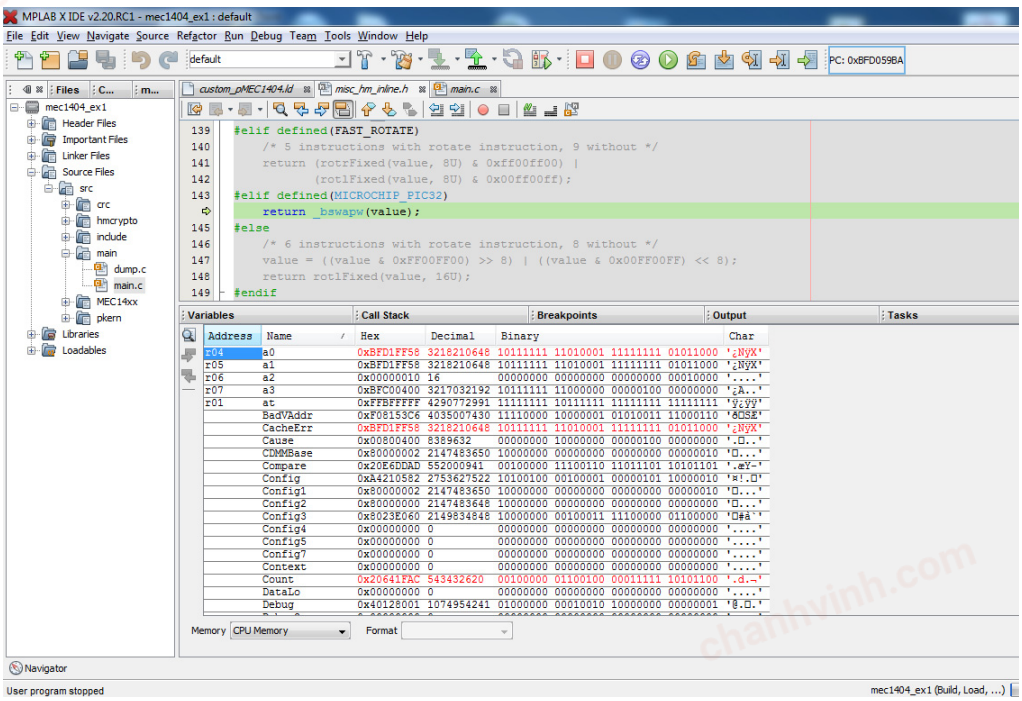
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User can debug code via "step over", "step into" or "continue".



2.8.3 View Memory or CPU Register Information

As user hits "Pause" to halt code execution, and select "Windows > PIC memory view > CPU registers", the registers windows will be shown as:



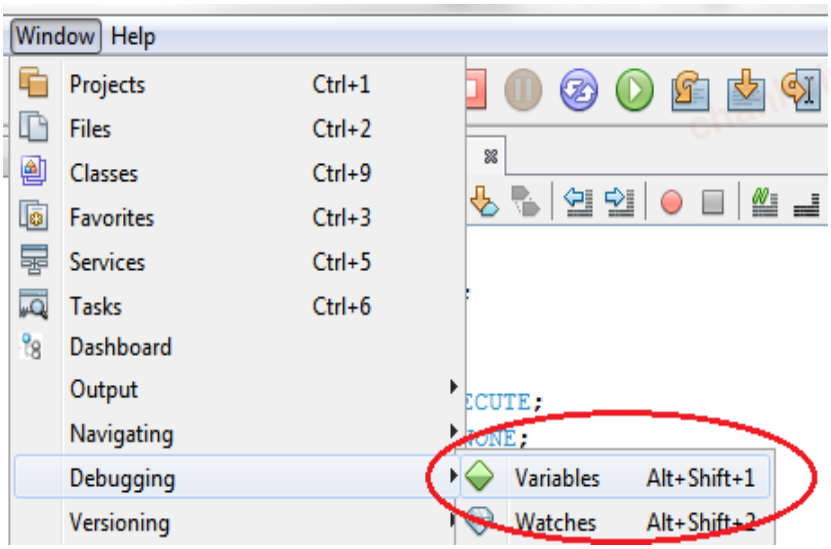
User can view other memory information, e.g. Data or code memory etc.

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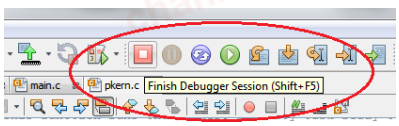
2.8.4 View Variable

For viewing or examining variables Menu bar → Windows → Debugging Variables or short cut Alt+ Shift + 1.



2.8.5 Exit Debug Task

Select “Finish debugger session”, IDE will terminate debugging task, and return to editor windows.



2.9 BUILD PROJECT FOR SPI FLASH IMAGE

Please refer to the MEC1418 Firmware Example Code Readme.txt for more detailed information.

Steps are shown as below:

1. Extract firmware binary from XC32 ELF output (refer to **Section 2.7 “Project Clean and build”**). Use XC32 OBJCOPY utility,

```
xc32-obcopy -O binary <ELF-File-Name> <Binary-File-Name>
```

2. Make sure TOML configuration file (ex: spi16M_cfg.toml) has the proper values for the firmware binary.
   - If you are loading into the start of MEC1418 Code SRAM then use 0xBFCF0000 for Load Address.
   - With the example projects linker file, the _reset entry point is also at 0xBFCF0000 and use this value for Entry Point Address.

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> **Note:** If you use the default MEC1418 XC32 linker file or change the location of _reset in the custom linker file, please remember to adjust value(s) in the TOML file!!!!

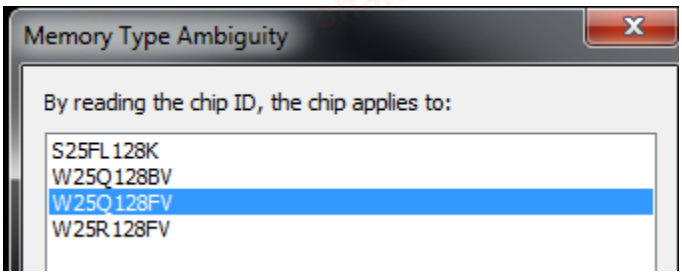
3. Run the SPI generator,

```
mec14xx_spi_gen -p MEC1418 -i <TOML file name> -o <output binary file name>
```

2.9.1 Program SPI Image to MECC Board SPI Flash

Now, we should have a SPI firmware image (16MB binary) from the build process as described above. Do the following to program the SPI image to the MECC board external SPI Flash image:

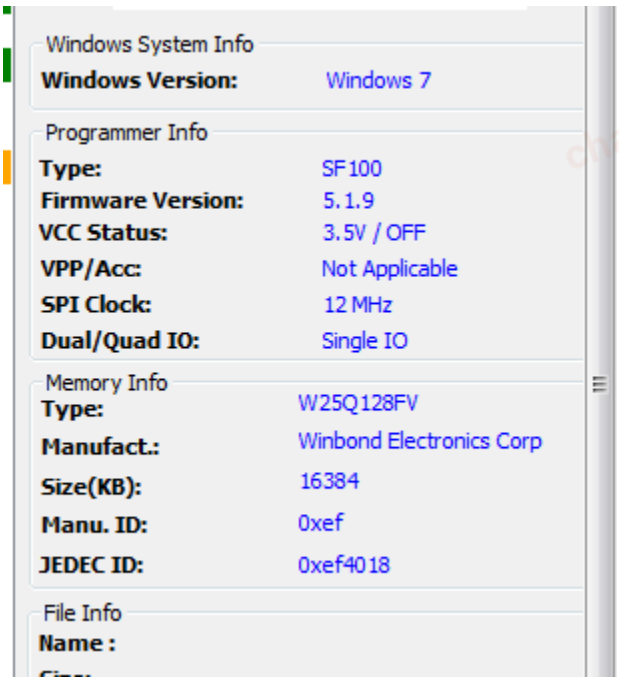
1. The MEC141x MECC Board has onboard 3V 128M-bit (16MB) SPI Flash (part#: Winbond W25Q128FV). If this is being replaced, please follow the example code then rebuild the binary with correct configuration.
2. Connect the Dediprog SF100 (or SF600) to the MEC141x MECC Board J2 header.
3. Plug-In a jumper to JP9 to hold the MEC141x in RESET state.
4. Plug-In the MEC141x MECC Board to the Intel Skylake RVP Platform or jumper wire JP8 Pin 1 (3.3_EC_CORE) to an external +3.3V power supply & ground pins (more is better) from MECC Board to power source.
5. Turn on the Intel Skylake RVP Platform or the external +3.3V power supply.
6. Run the Dediprog programming utility, "dedipro.exe", the chip selection window. will pop-up as shown below, please select the "W25Q128FV".



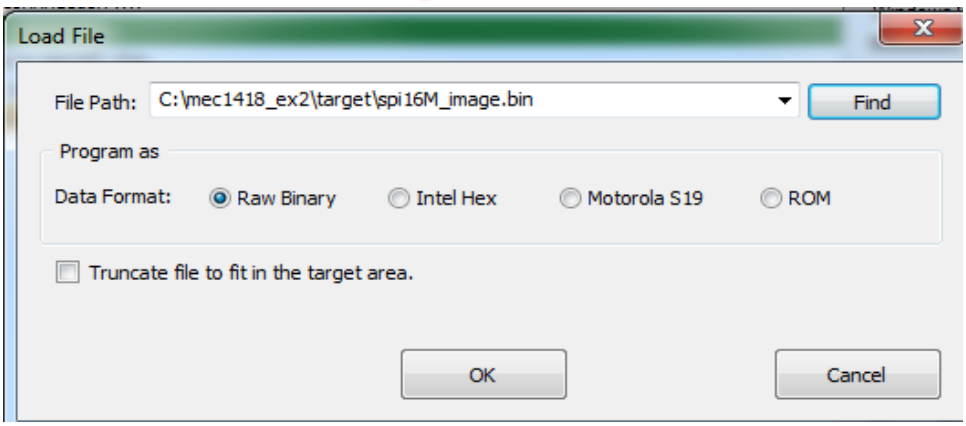
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7. The Info sessions on the right side should be shown as below:

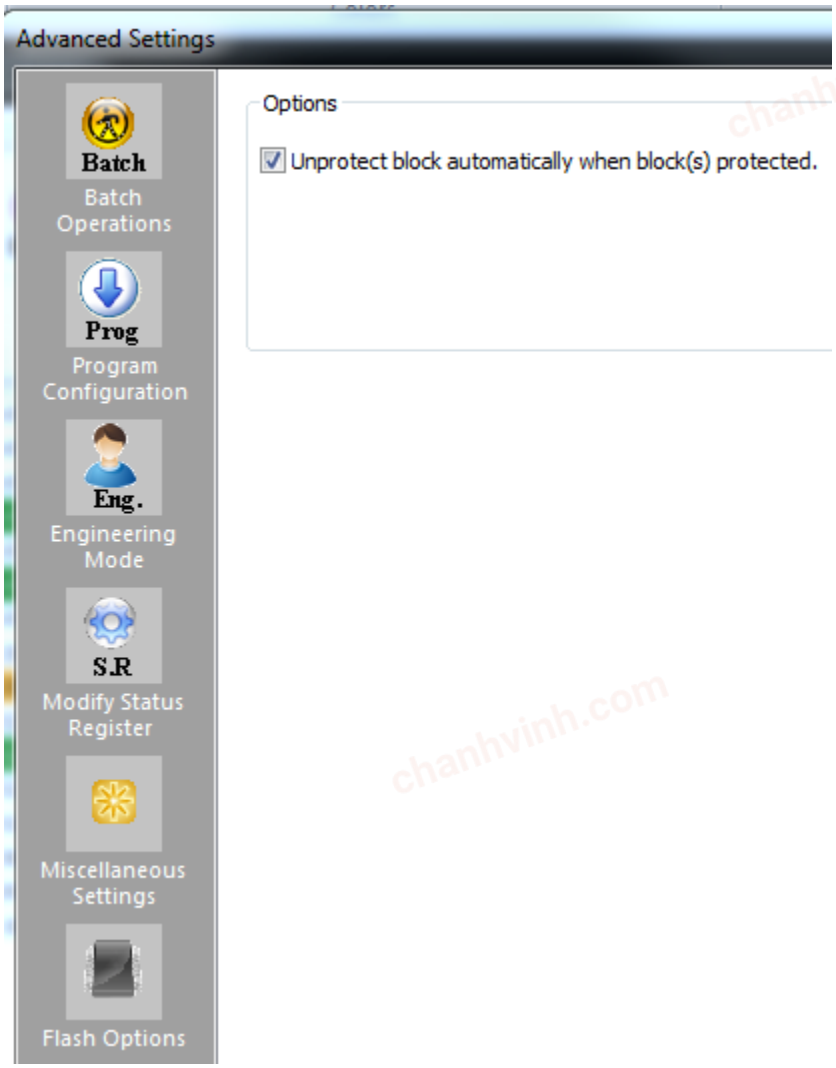


8. Go to “File” --> “Find” and select the 16MB firmware application binary file, set the data format as “Raw binary” as shown below:



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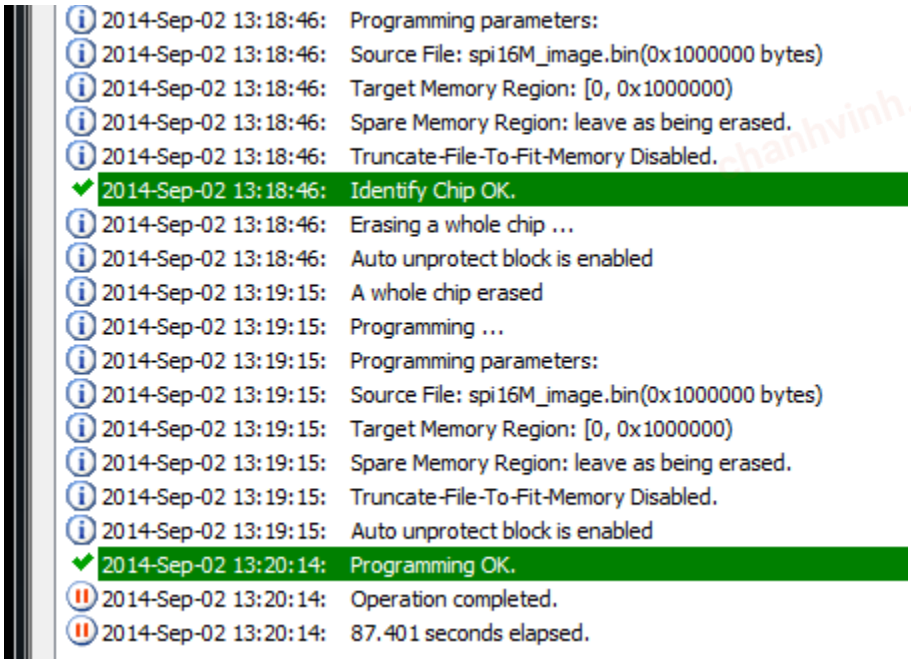
9. Go to "Config" --> "Flash Option", make sure "Unprotect block automatically when block(s) protected" option is selected.



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10. Click to the “Batch”, the SPI flash programming will start, and should complete successfully as shown below.



11. The firmware is now stored in the external SPI flash device. Please remove the JP9, and do a power cycle (please make sure to wait long enough to have power supply discharge before re-powering the MECC board). The new firmware should be loaded by the MEC141x internal ROM to the internal SRAM and start executing.

Please contact your Microchip representative if you need any further information or assistance.

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Appendix A. Intel Skylake Platform Rework Instructions

This section provides the rework steps for the Intel Skylake RVP motherboard, eSPI configuration with the MEC141x MECC Add-In Board.

Please refer to Intel "SKL_Y_EC_AIC_ENABLE.pdf" file, and Skylake Reference Schematic, "544250_544250_SKL_Y_LPDDR3_RVP3_CRB_Schem_Rev0_72.pdf" documents.

Note: Highlighted items differ from Intel's instructions.

Intel Step Nos.	Parts	See Silkscreen Sheet #	Rework Action	Component: Value / Form / Tolerance	Notes
1, 2, 3	none	(n/a)	(None)	(n/a)	(Jumper settings only: Open J2B5, J2E1; Close J2B7.)
4, 5	R4D12	B2 or B3	Move resistor to position R4D11.	22-ohm / 402 / 5%	3 pads at right angles: Rotate the resistor to the other orientation.
6, 7	R3D17	B2 or B3	Move resistor to position R3D16	0-ohm / 402	3 pads in a line. Shift resistor to other position.
8, 9	R5E23	C2	Move resistor to position R5E22	0.05-ohm / 603 / 1%	3 pads in a line. Shift resistor to other position.
10	R8F35	C1	Replace 150K resistor w/ 4.7K resistor.	(FYI was 150K / 402 / 5%) now 4.7K / 402 / 5%	New 4.7K resistor needed, not supplied.
11	R4E24, R4E6, R4E13, R4E12, R4E5, R3D32	B2	Remove resistors.	(FYI 0-ohm / 402)	
12	R4D17, R4D15, R4D18, R4D16, R4D19, R4D13	B3	Remove resistors.	(FYI 0-ohm / 402)	
13, 14	(n/a)	(n/a)	(None)	(n/a)	Rework not required
14a (new)	R3E2	B3	Remove resistor.	(FYI - 10K / 402 / 5%)	Rework required
15	R5E65, R4E4, R2N11	C2 B2 Underside	Remove resistors.	(FYI - 10K / 402 / 5%)	
16	R5F30	C2	Remove resistor.	(FYI - 8.2K / 402 / 5%)	

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